

Course Name:	Digital Electronics	Semester:	III
Date of Performance:		Batch:	A - 3
Faculty Name:		Roll no.:	16014022050
Faculty Sign & Date:		Grade/Marks:	___ / 25

Experiment no.: 6

Title: Study of FF and Asynchronous Counter using JK FF

Aim and Objective of the Experiment:

- To verify the truth table and timing diagram of SR, JK, T and D flip-flops by using NAND.
- Implementation of mod 6 asynchronous counter using JK FF.

COs to be Achieved:

CO3: Design sequential circuits using MSI devices.

Theory:

A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

- S-R flip flop
- D flip flop
- J-K flip flop
- T flip flop

S-R flip-flop –

The basic NAND gate SR flip flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs. The SR flip flop actually has three inputs, SET, RESET and its current output Q relating to its current state.

D flip flop –

A D flip flop has a single data input. This type of flip flop is obtained from the SR flip flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop and is shown below. From the truth table of SR flip-flop, we see that the output of the SR flip-flop is in unpredictable state when the inputs are same and high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other.

J-K flip flop –

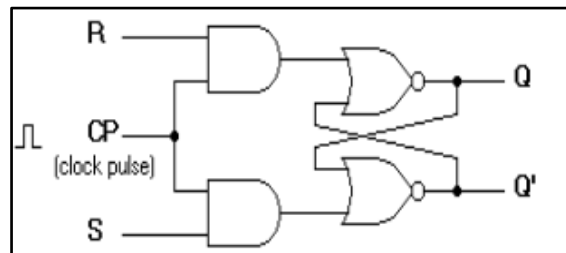
The JK Flip-flop is similar to the SR Flip-flop but there is no change in state when the J and K inputs are both LOW. The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”. Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”.

T flip flop –

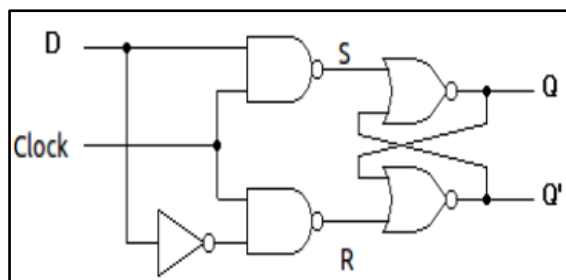
These flip-flops are called T flip-flops because of their ability to complement its state (i.e.) Toggle, hence the name Toggle flip-flop. A T flip flop is like JK flip-flop. These are basically a single input version of JK flip flop. This modified form of JK flip-flop is obtained by connecting both inputs J and K together. This flip-flop has only one input along with the clock input.

Circuit Diagram/Block Diagram:

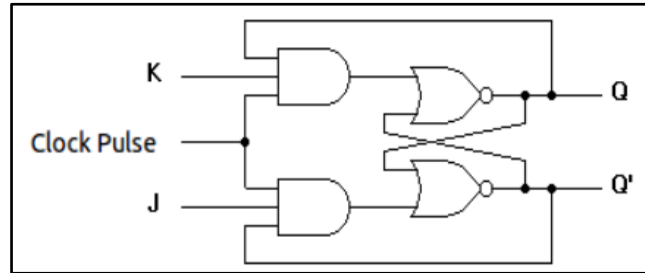
SR flip-flop using AND and NOR gate –



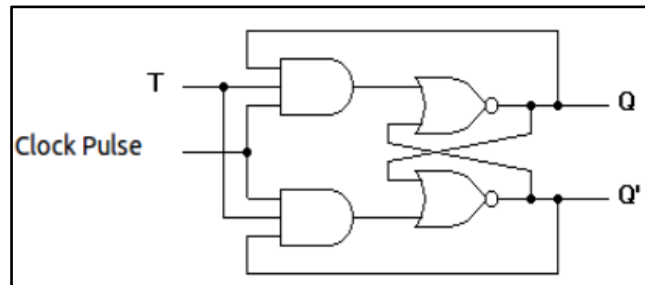
D flip-flop using NAND gate –



JK flip-flop using AND and OR gate –

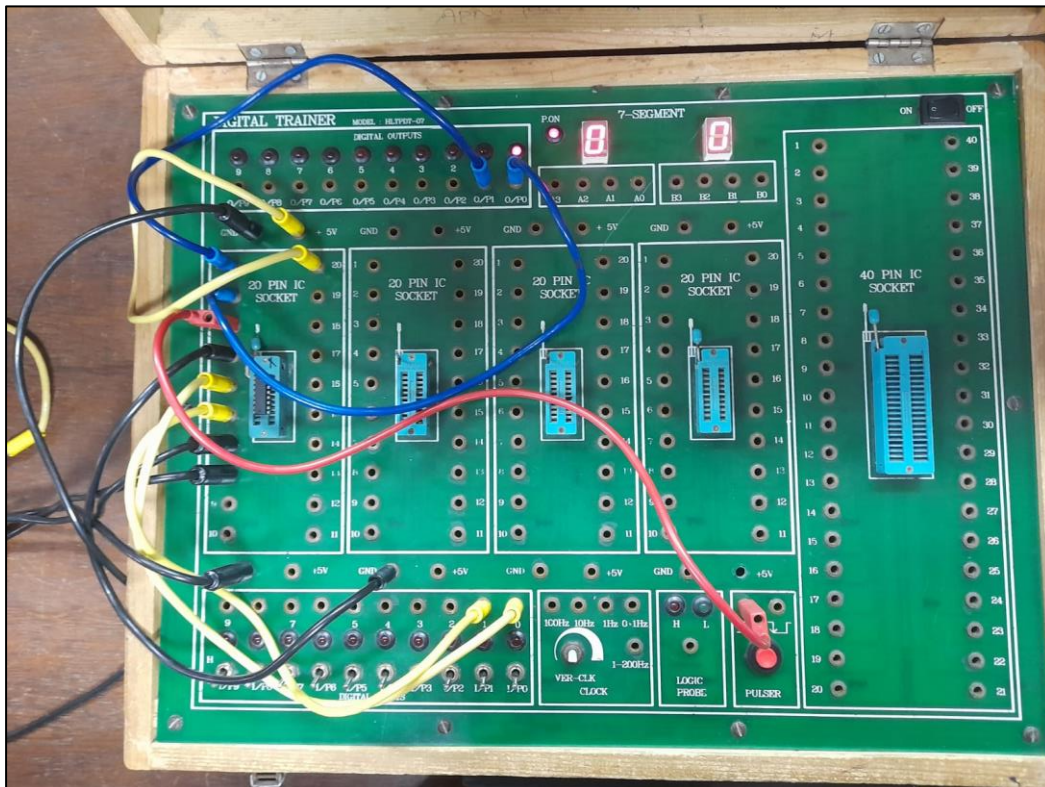


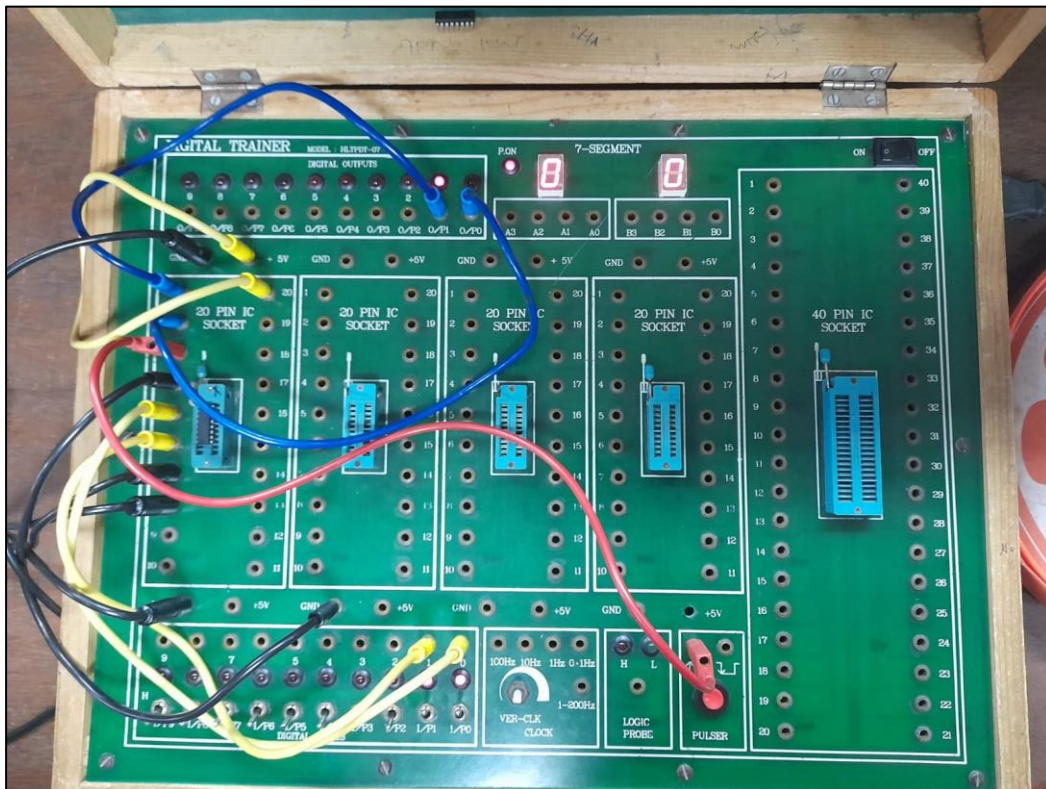
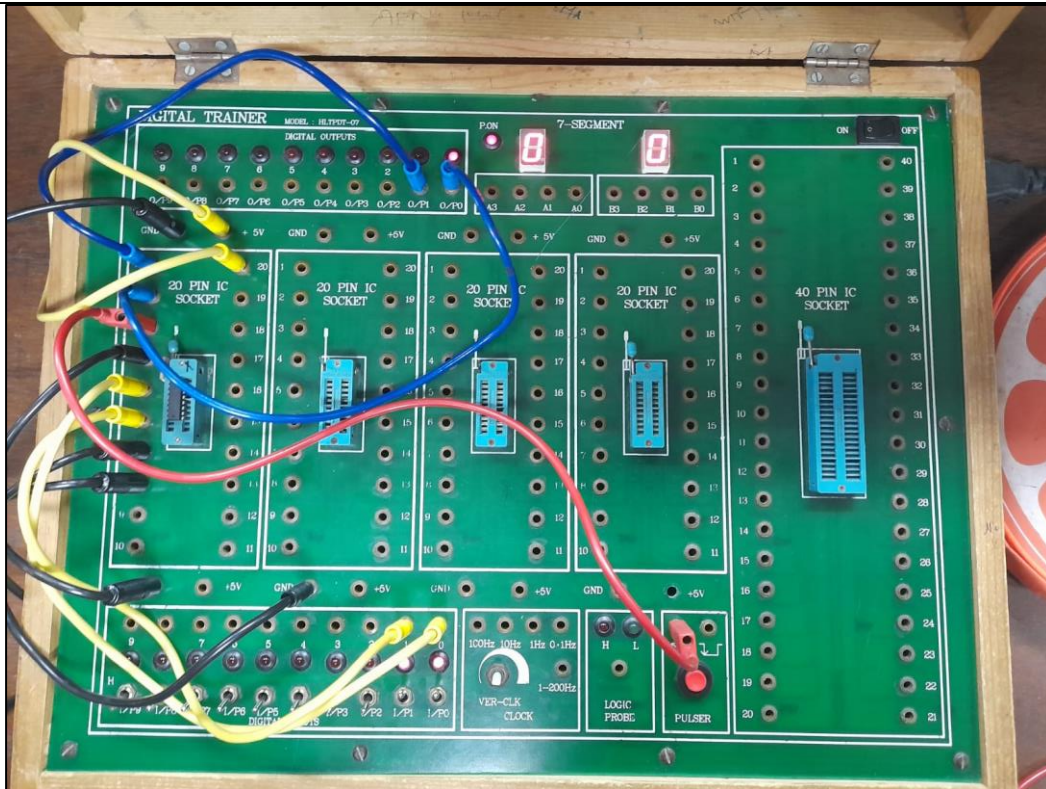
T flip-flop using AND and OR gate –

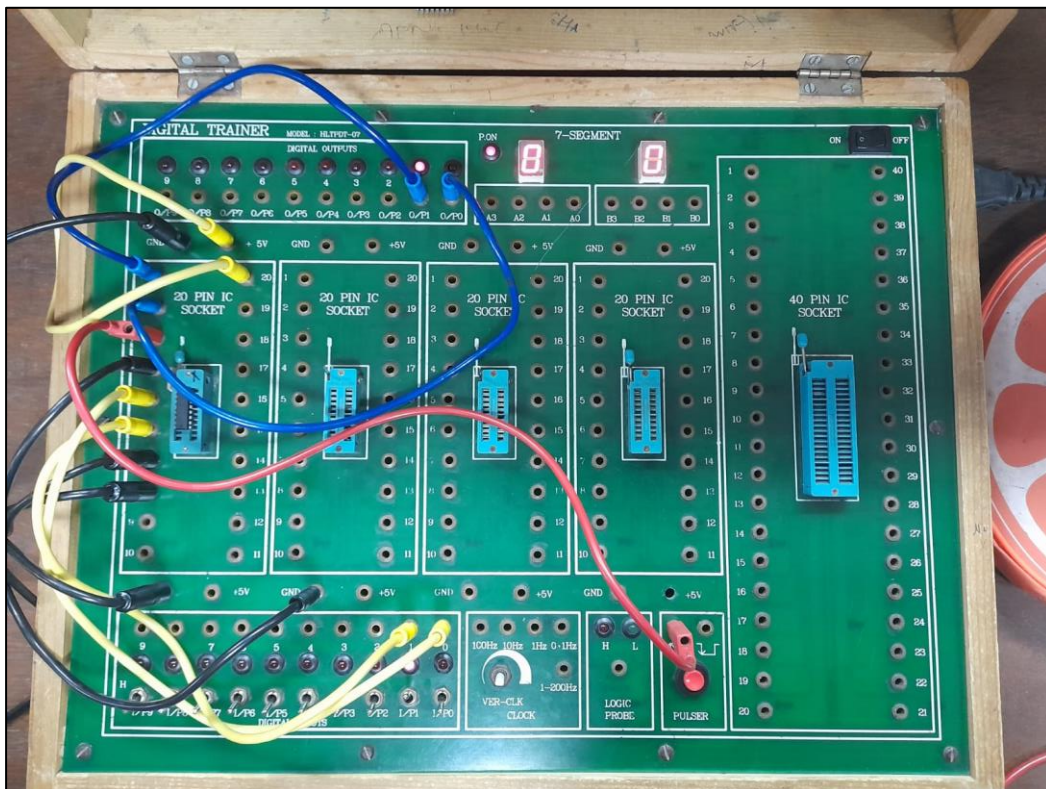
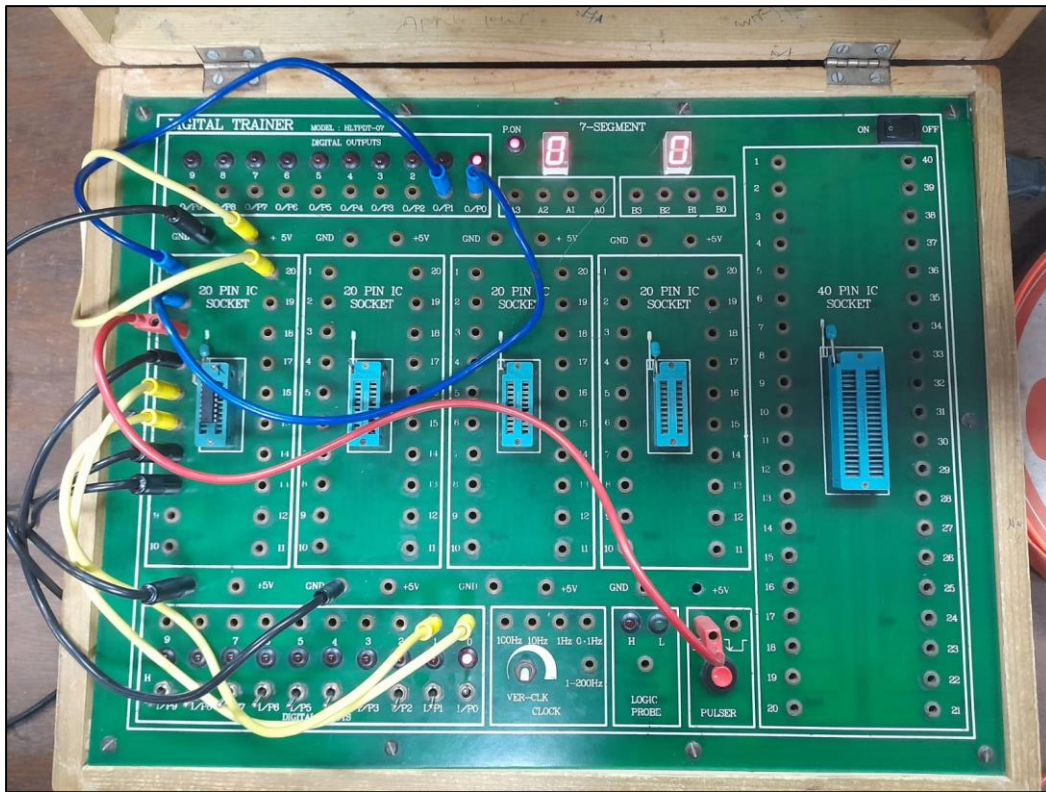


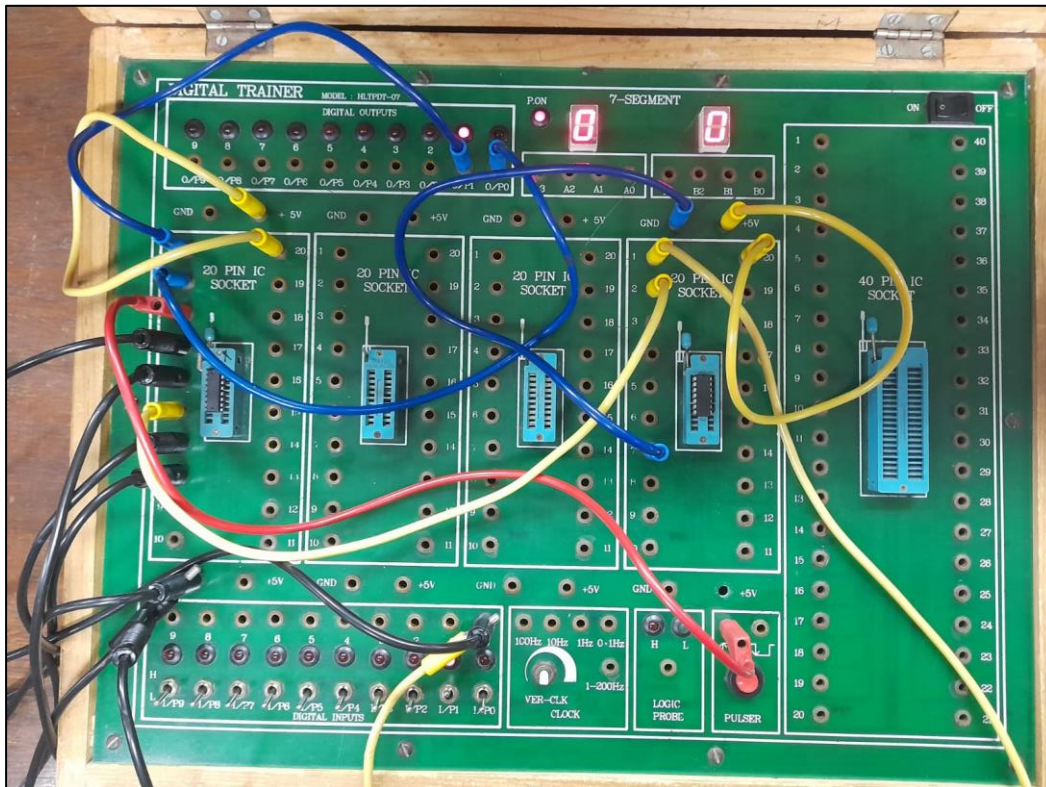
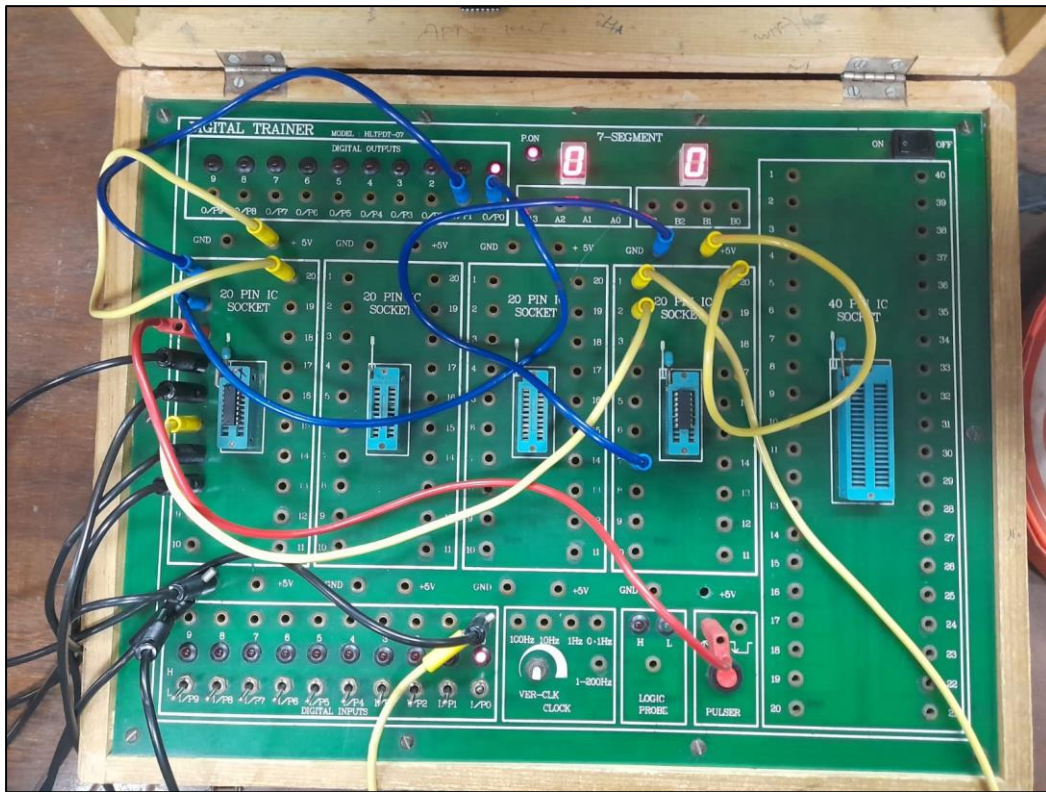
Stepwise – Procedure:

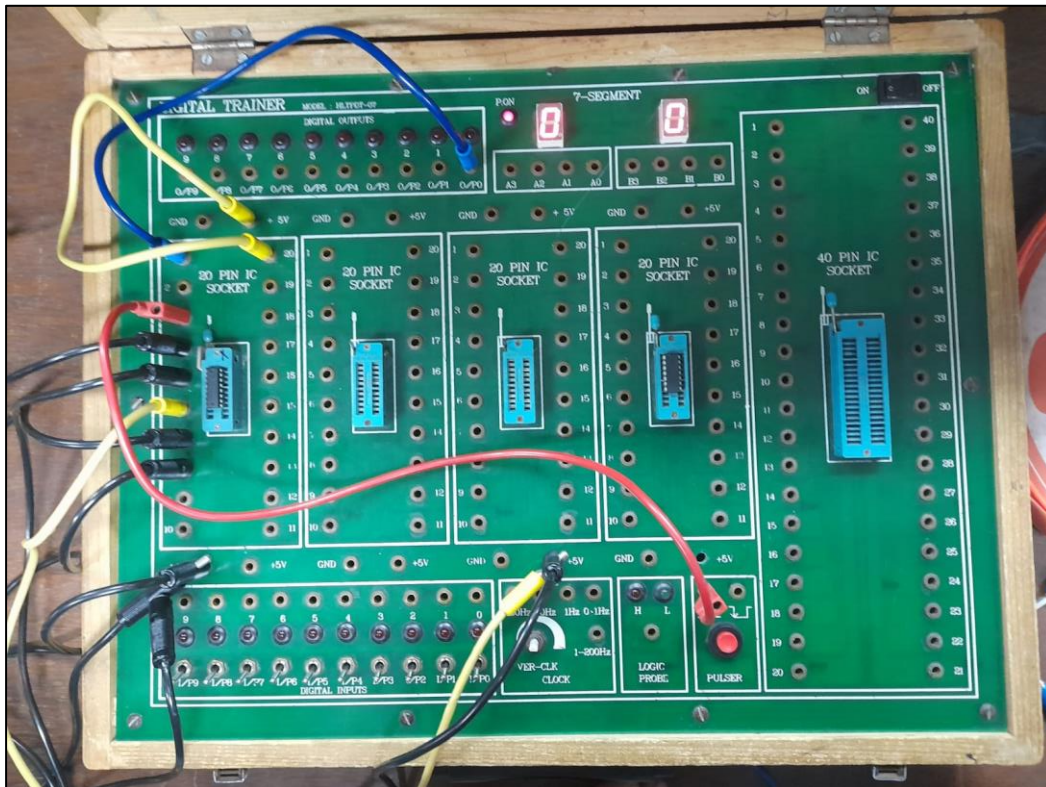
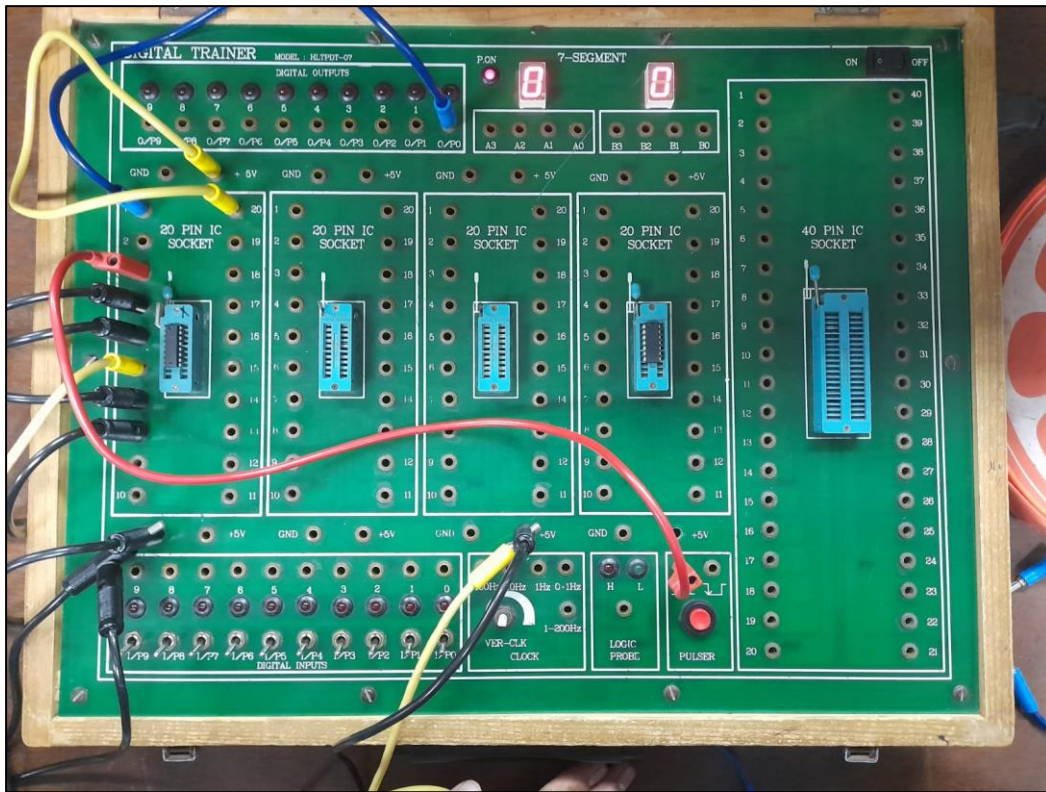
1. Implement the flip-flops using given circuits.











2. Verify Truth Table of each of them. (VERIFIED in above question)
a. SR FF –

Input			Output	State
Clock	S	R	Q	
X	0	0	No change	Previous
⊕	0	1	0	Reset
⊕	1	0	1	Set
⊕	1	1	-	Forbidden

b. D FF –

Input			Output	
D	Reset	Clock	Q	\bar{Q}
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

c. JK FF –

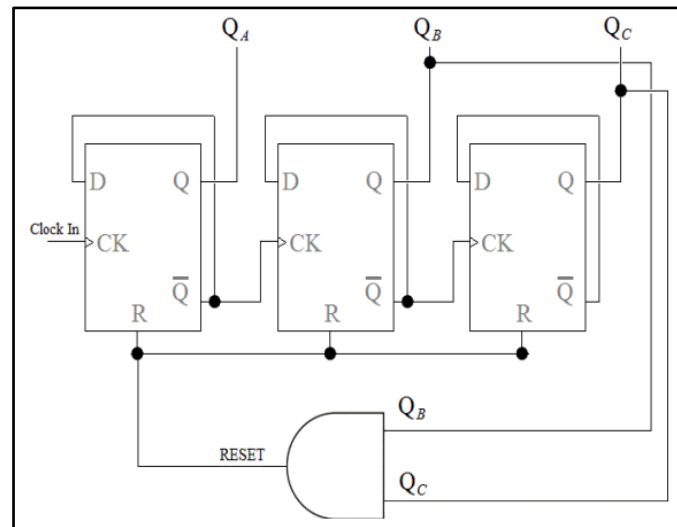
Trigger	Input		Output				Inference
			Present State		Next State		
Clock	J	K	Q	\bar{Q}	Q	\bar{Q}	
0	X	X	-		-		Latched
1	0	0	0	1	0	1	No change
			1	0	1	0	
1	0	1	0	1	0	1	Reset
			1	0	0	1	
1	1	0	0	1	1	0	Set
			1	0	1	0	

1	1	1	0	1	1	0	Toggles
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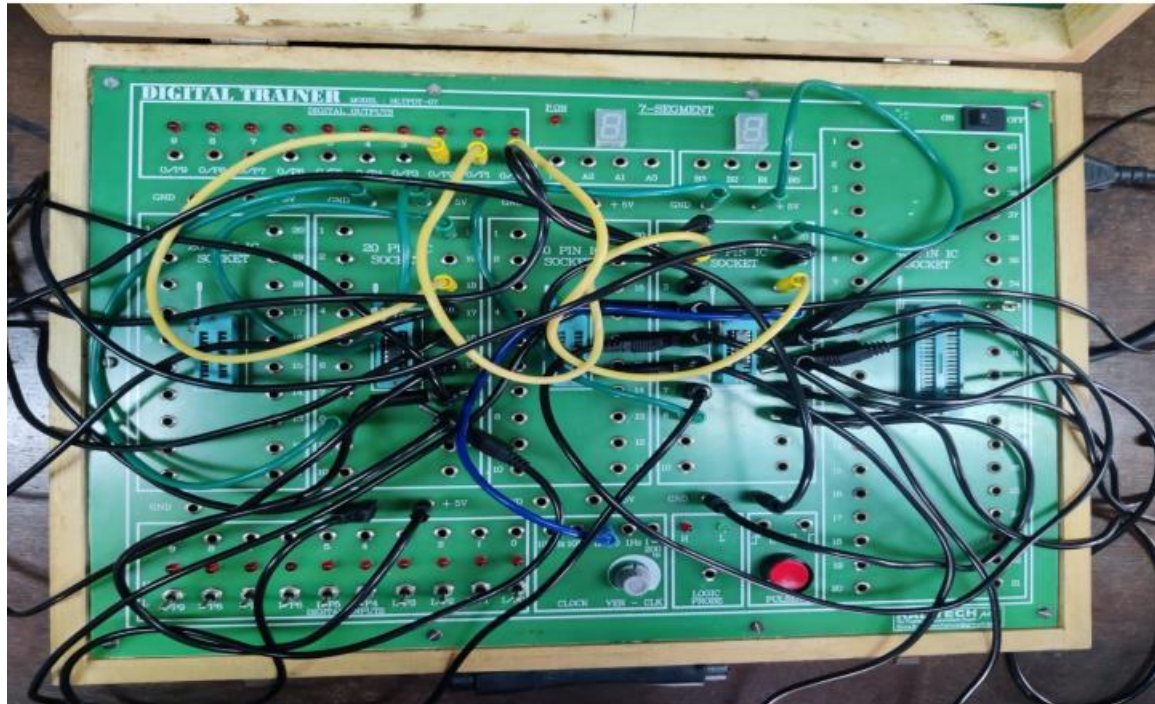
d. T FF –

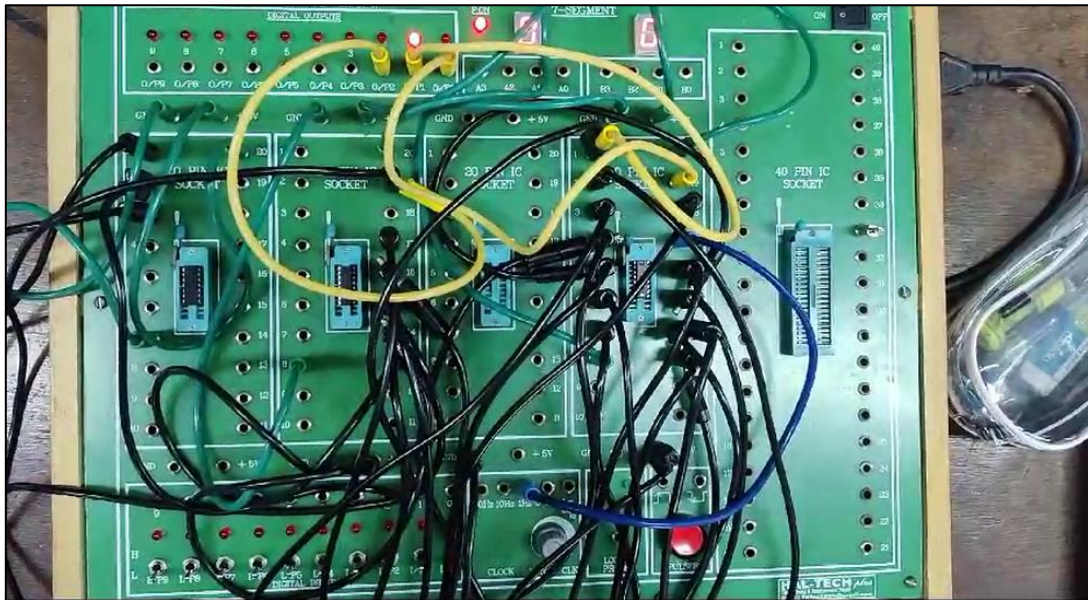
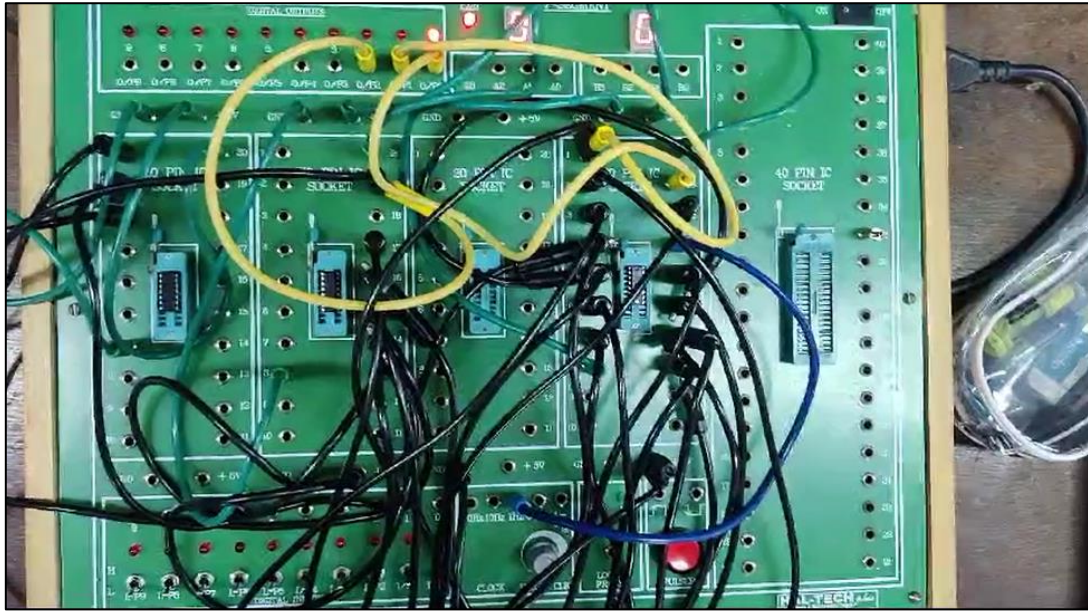
T	Clock	Q	\bar{Q}
0	\otimes	Q	\bar{Q}
1	\otimes	\bar{Q}	Q
X	\otimes	Q	\bar{Q}

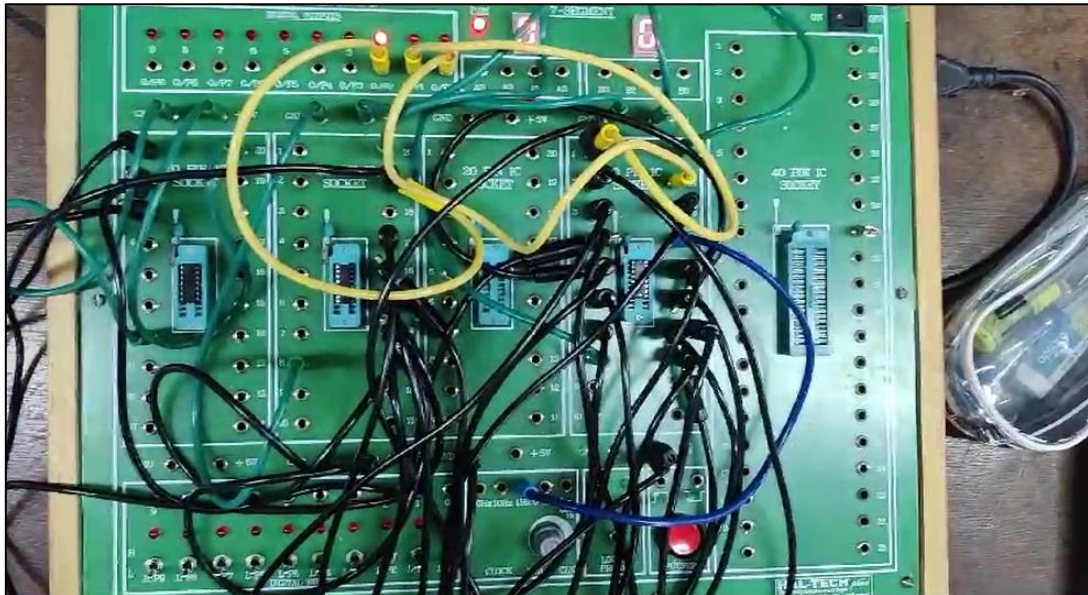
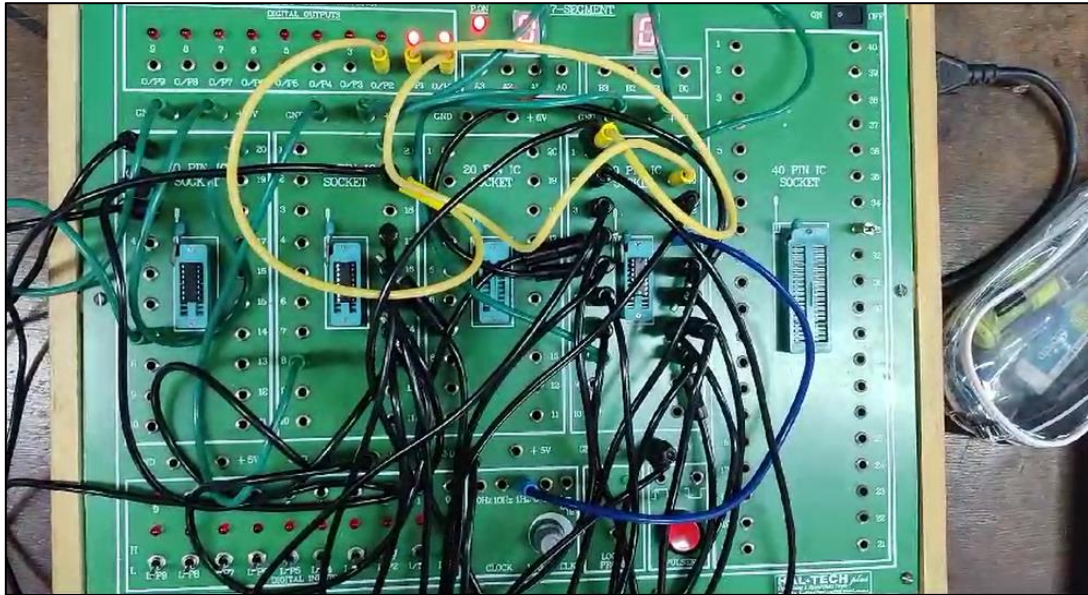
3. Implement the mod 6 asynchronous counter using JK Flip Flops.

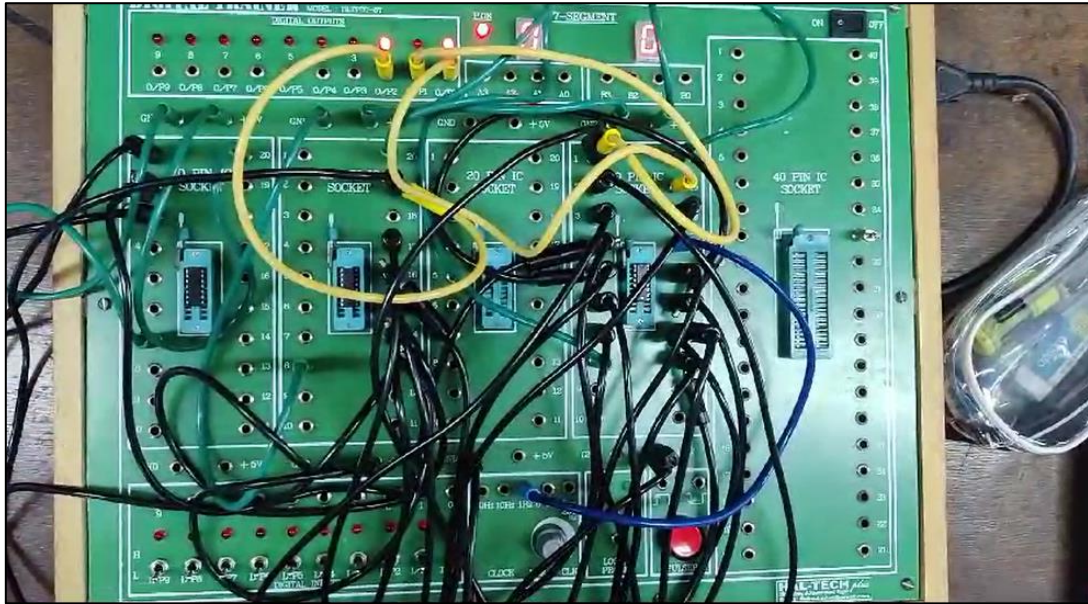


Asynchronous Mod 6 Counter –

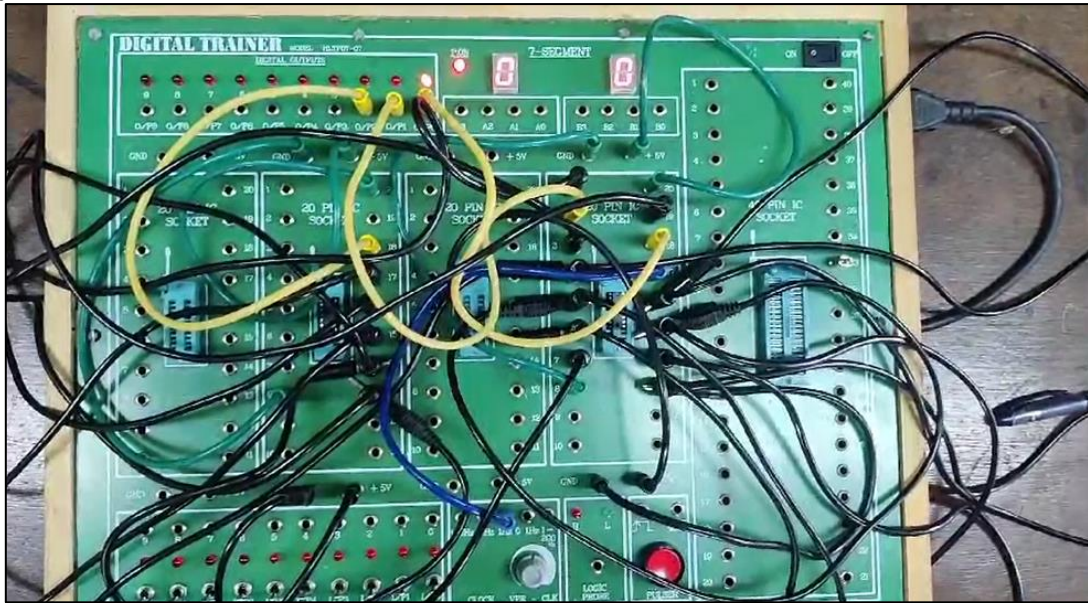


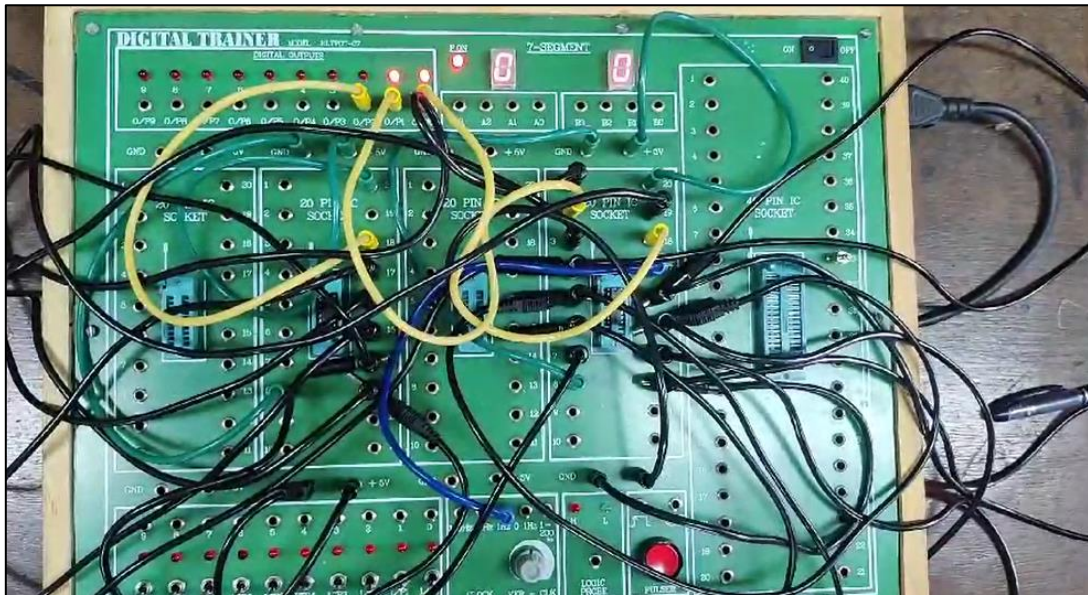
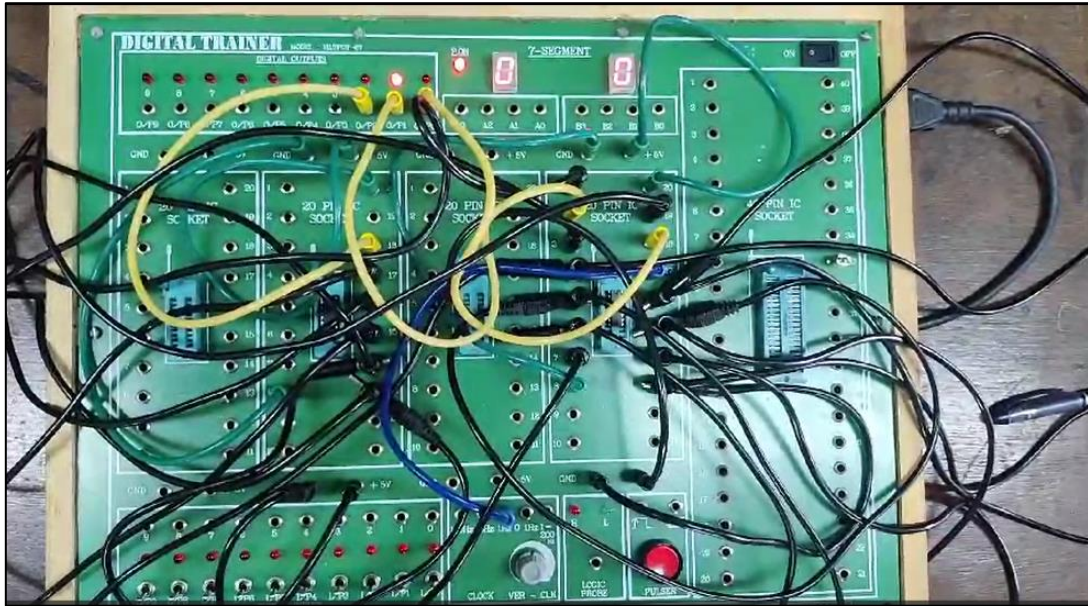


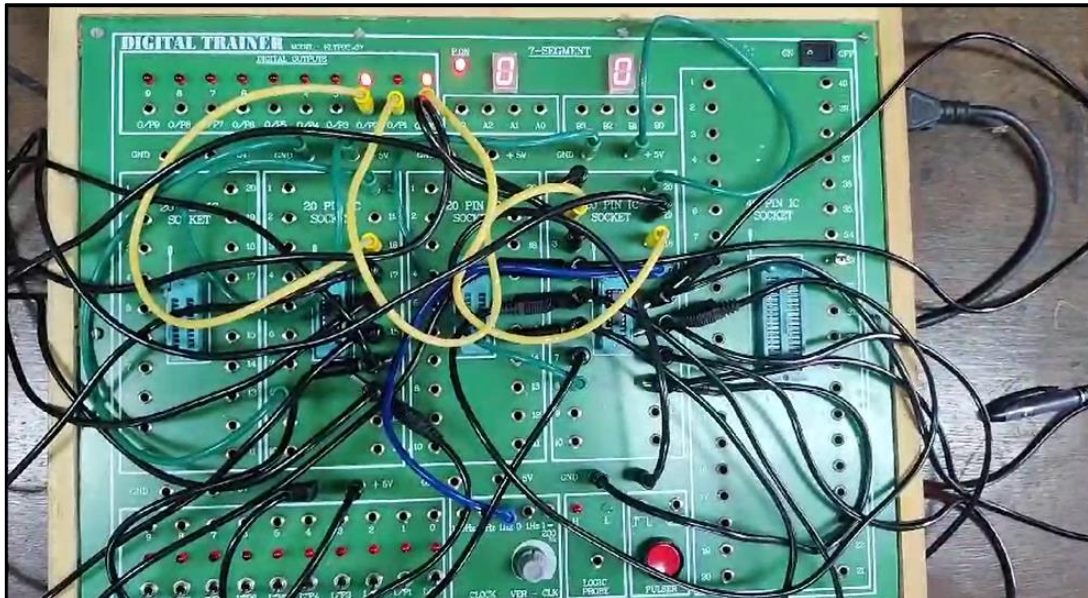
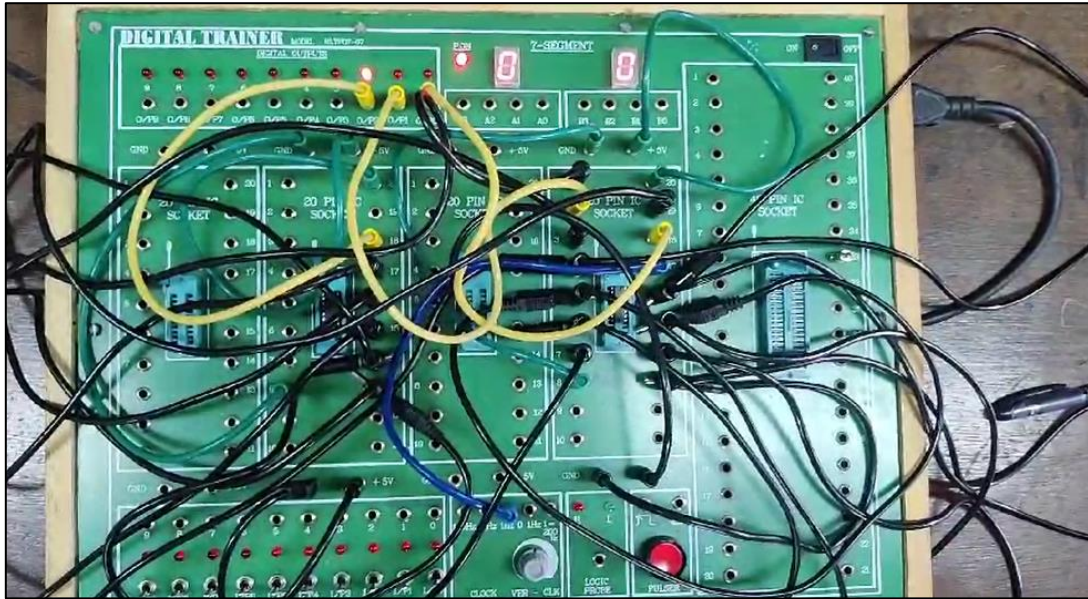


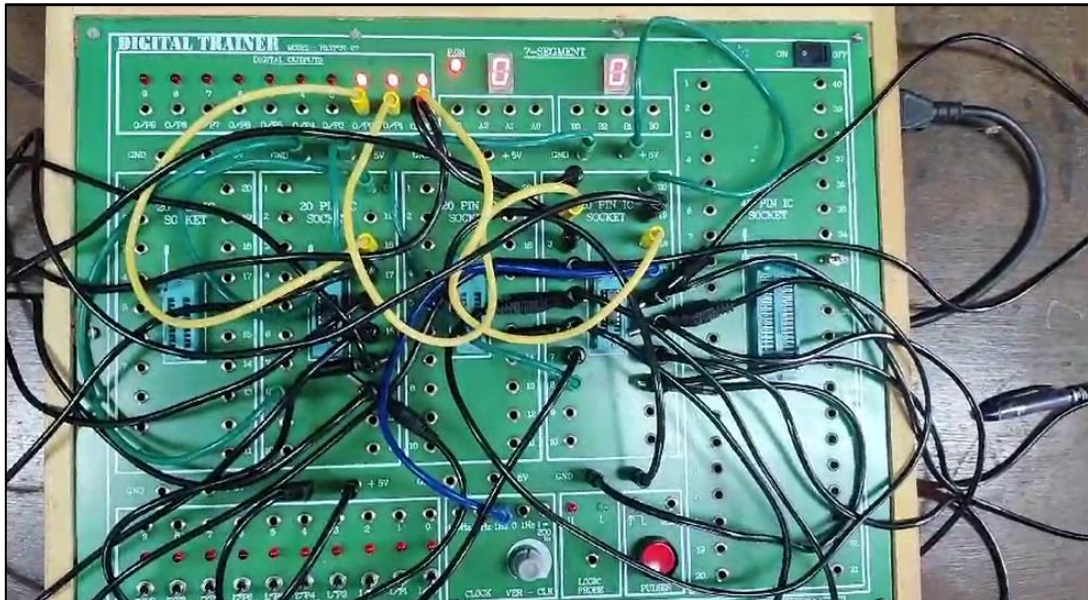
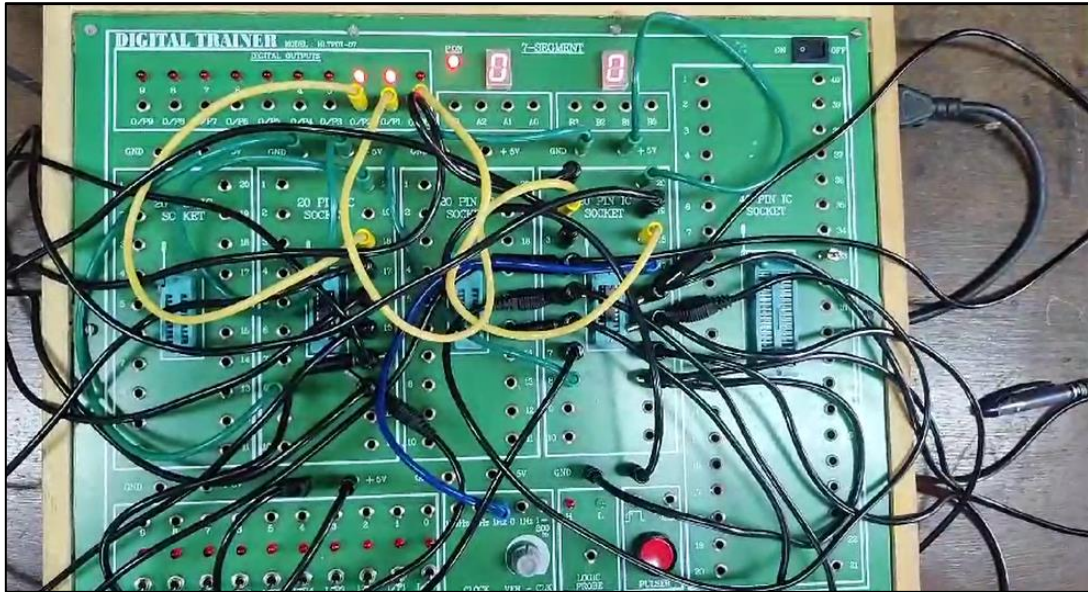


Asynchronous Counter –

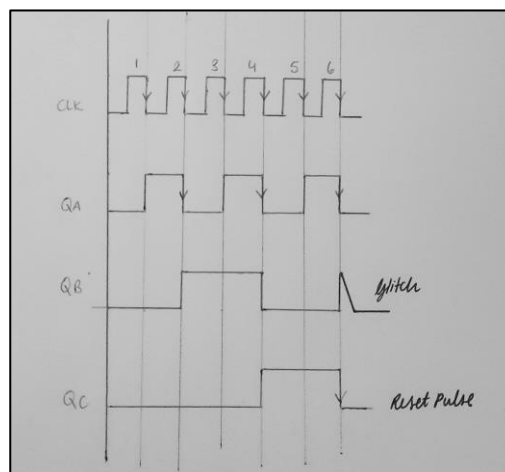








4. Draw timing diagram and mark glitches.



Post Lab Subjective/Objective type Questions:

1. Which of the following is correct for a gated D-type flip-flop?
 - a. The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
 - b. The output complement follows the input when enabled
 - c. Only one of the inputs can be HIGH at a time
 - d. The output toggles if one of the inputs is held HIGH
2. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
 - a. AND or OR gates
 - b. Ex-OR or Ex-NOR gates
 - c. NOR or NAND gates
 - d. AND or NOR gate
3. The truth table for an S-R flip-flop has how many valid entries?
 - a. 1
 - b. 2
 - c. 3
 - d. 4
4. The flip-flops which have not any invalid states are _____.
 - a. S-R, J-K, D
 - b. S-R, J-K, T
 - c. J-K, D, S-R
 - d. J-K, D, T
5. Both the J-K & the T flip-flop is derived from the basic _____.
 - a. S-R flip-flop
 - b. S-R latch
 - c. D latch
 - d. d flip-flop

Conclusion:

We have thoroughly studied and analyzed types of flip-flops (SR, JK, T, D), including their use cases and advantages of each other. We practically implemented T and D flip-flops using JK flip-flop and then validated their corresponding truth tables and timing diagram. We also saw how counter work and successfully designed an asynchronous counter, along with mod 6 asynchronous counter using 3 JK FF and AND gate.

Signature of faculty in-charge with Date: