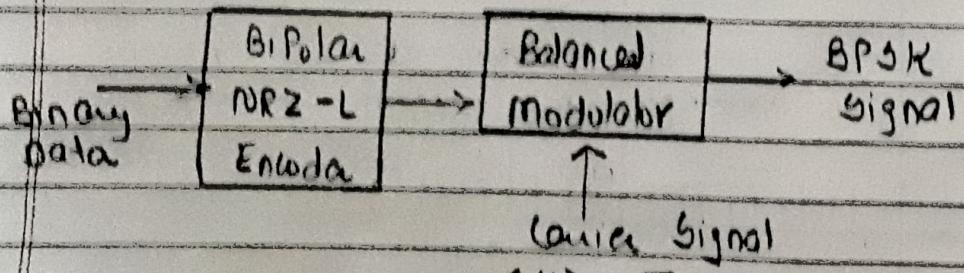


* 5.1 (BPSK, DPSK, QPSK, BFSK, BASK)

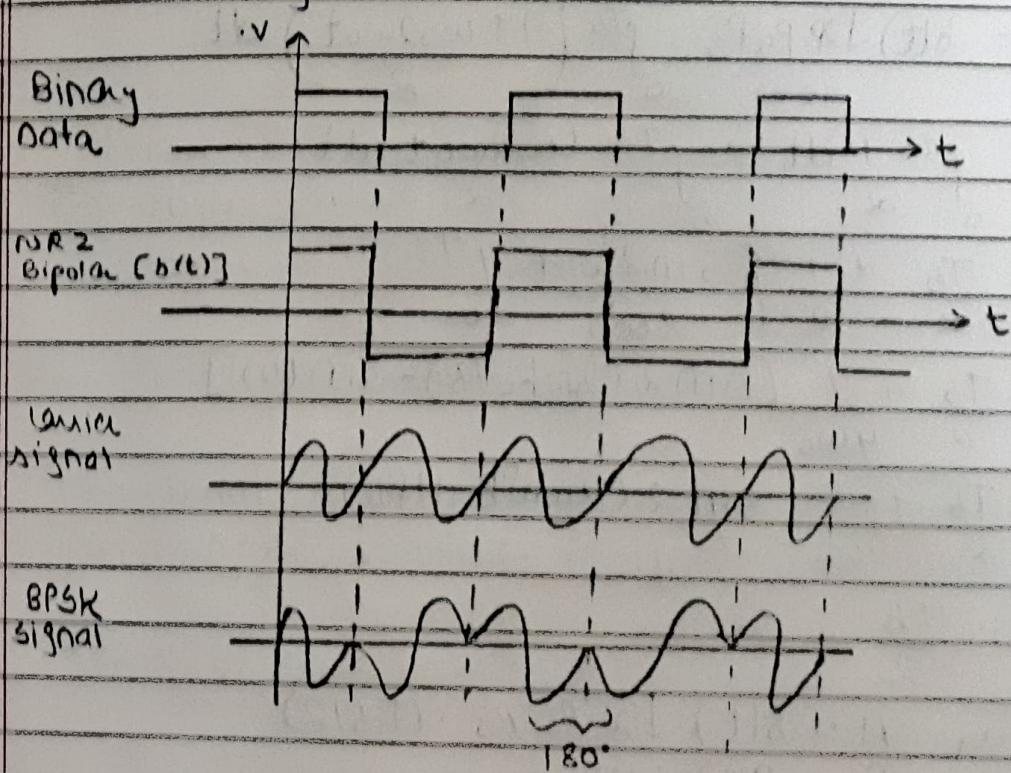
- (*) Binary Phase Shift Keying (BPSK)
- 1) BPSK is called as 2-phase PSK.
 - 2) In this, the sine wave source takes two phase reversal such as 0° and 180° .
 - 3) BPSK is basically a Double Side Band Suppressed carrier modulation scheme.
 - 4) No. of bits taken at time = N
No. of combination can be made = 2^N
If $N=1$: ...
 $m=2^1$
 $m=2$
 - This is BPSK
 - 5) Bit duration is T_b
Bit Rate is $\frac{1}{T_b} = f_b$
 - Phase Shift = $\frac{2\pi}{m}$

* BPSK Modulator

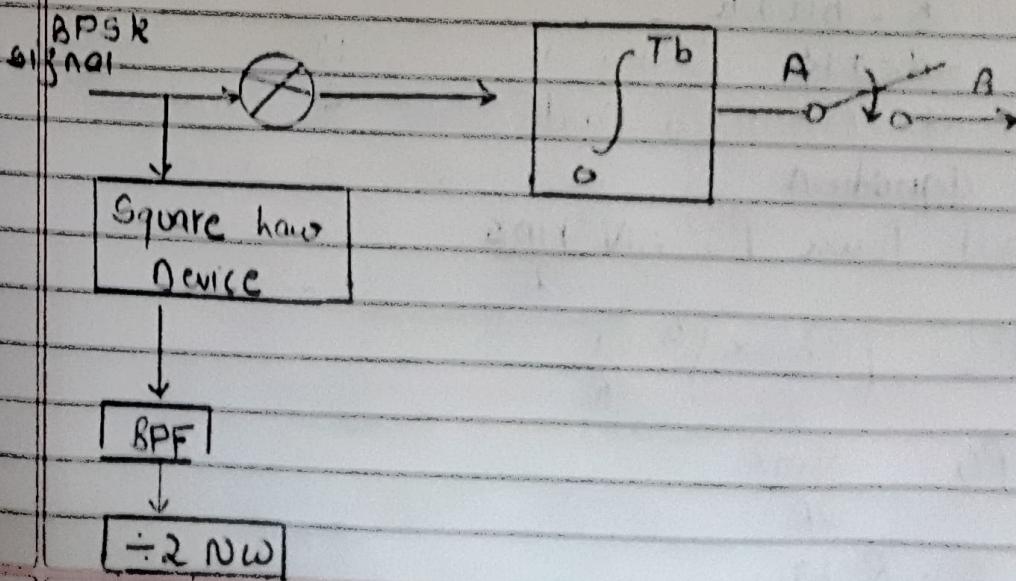


- 1) The binary message signal is fed to the bipolar NRZ level encoder that converts the Binary data input into equivalent bipolar NRZ sequence, $m(t)$

- 2) This bipolar NRZ signals is fed to the balanced modulator along with carrier wave
- 3) Thus the binary signal modulates the carrier wave that generates a phase shifted modulated signal termed as BPSK signal



BPSK Demodulation



1) Let us consider, the signal at the input of the receiver is

$$S(t) = b(t) \sqrt{2} P_s \cos \omega_0 t$$

2) At A switch

$$A = \int_0^{T_b} b(t) \sqrt{2} P_s \cos^2 \omega_0 t dt$$

$$A = b(t) \sqrt{2} P_s P_s \int_0^{T_b} \left(\frac{1 + \cos 2\omega_0 t}{2} \right) dt$$

$$A = \int_0^{T_b} \frac{1}{2} dt + \int_0^{T_b} \frac{\cos 2\omega_0 t}{2} dt$$

$$A = \frac{T_b}{2} + \frac{1}{2} \left[\frac{\sin 2\omega_0 t}{2\omega_0} \right]_0^{T_b}$$

$$A = \frac{T_b}{2} + \frac{1}{2 \cdot 4\omega_0} [\sin 2(2\pi f_0 T_b) - \sin(0)]$$

$$A = \frac{T_b}{2} + \frac{1}{4\omega_0} \sin 2(2\pi f_0 T_b)$$

$$A = \frac{T_b}{2}$$

Thus $A = b(t) \sqrt{2} P_s \cdot (T_b/2)$

$$A = b(t) K$$

3) At point switch B

$$B = b(t) K$$

$$B = \pm K$$

* BPSK Equation

i) Signal Power ' P_S ' = $\frac{V^2_{rms}}{2}$

$$\therefore P_S = \left(\frac{V_{max}}{\sqrt{2}} \right)^2 \cdot \frac{1}{R}$$

$$P_S = \frac{V^2 m^2}{2R}$$

For $R = k_2$

$$P_S = \frac{V_m^2}{2}$$

$$\therefore V_m^2 = 2 P_S$$

$$V_m = \sqrt{2 P_S}$$

$$\therefore \omega_0 = 2\pi f_0$$

Q) $f_0 = n f_b$.. where f_0 = carrier freq
 n = integer
 f_b = bit rate

$$\therefore V_{BPSK}(t) = b(t) \sqrt{2 P_S} \cos \omega_0 t$$

$$\text{For logic 1} :- + \sqrt{2 P_S} \cos \omega_0 t$$

$$\text{logic 0} :- - \sqrt{2 P_S} \cos \omega_0 t$$

OR

$$V_{BPSK}(t) = b(t) \sqrt{2 P_S} (\omega_0 t + \phi_0)$$

* Geometrical Representation of BPSK | Signal Space Representation | Signal Constellation

$$V_{BPSK}(t) = b(t) \sqrt{2 P_S} \cos \omega_0 t$$

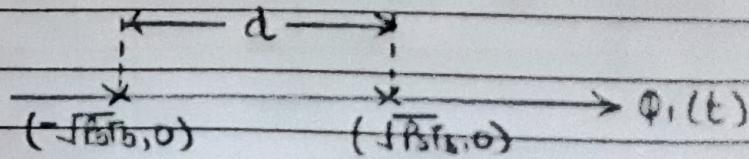
$$= [\sqrt{P_S T_b} \ b(t)] \sqrt{\frac{2}{T_b}} \cos \omega_0 t$$

$$= [\sqrt{P_S T_b} \ b(t)] \phi_1(t) \quad \text{.. where } \phi_1(t)$$

is orthogonal
 carrier signal

$$\text{For logic 1} : V_{BPSK}(t) = + \sqrt{P_S T_b} \phi_1(t)$$

$$\text{logic 0} : V_{BPSK}(t) = - \sqrt{P_S T_b} \phi_1(t)$$



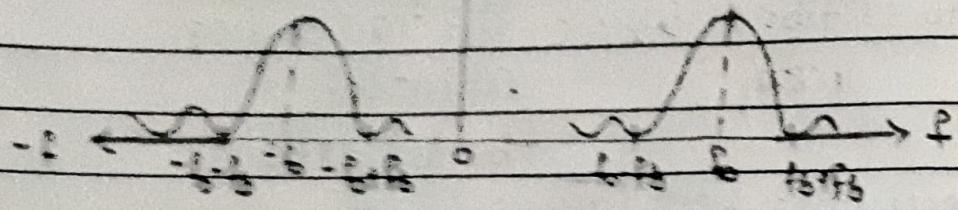
Bit Energy 'E_b' :- $P_S T_b$

$$d = 2 \sqrt{n} E_b \sin \left(\frac{\pi}{m} \right)$$

$$d = 2fEb$$

* Plot of base spatial density (PSD) of block.

→ $S_{\text{PSD}}(k)$



$$BLO = 2f_b$$

f_b

$$\frac{\pi \omega}{2f_b}$$

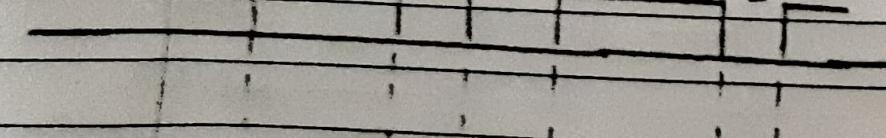
For $N = 1$

$$BLO = 2f_b$$

= Differential Phase Shift Key (DPSK)

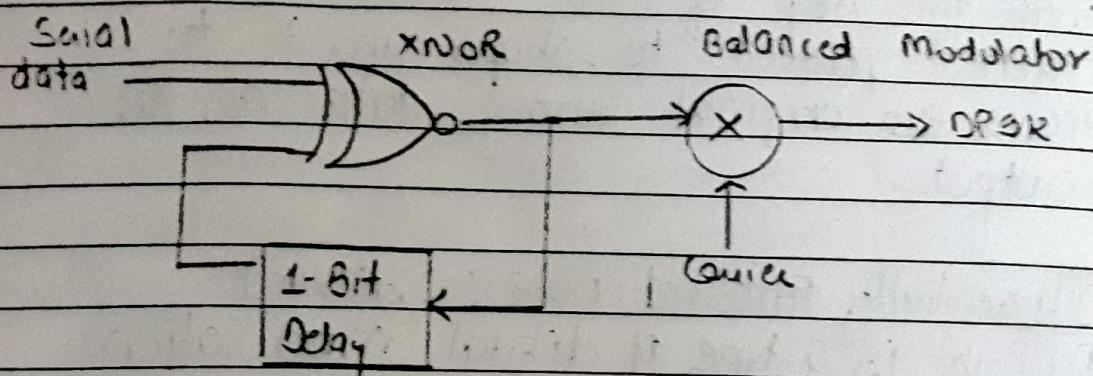
- 1) In Differential Phase Shift Keying DPSK the phase of the modulated signal is shifted relative to the previous signal element
- 2) No reference signal is considered here
- 3) The signal phase follows the high or low state of the previous element
- 4) If the data bit is low i.e 0, then the phase of signal is not reversed
- 5) But if data is high i.e 1 then the phase of the signal is reversed

$$\underline{0} \underline{0} = \underline{1} \quad \underline{0} = \underline{0} \quad \underline{0} \quad \underline{0} \quad \underline{1} \quad \underline{0}$$



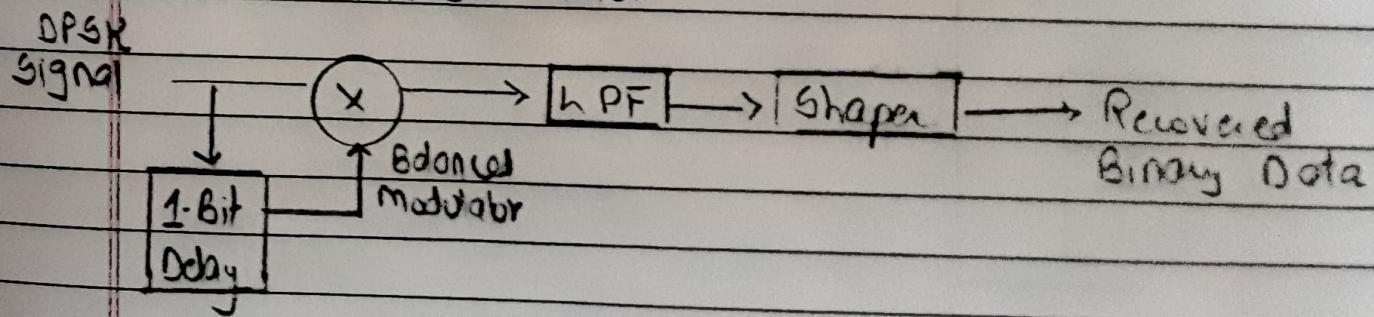
~~DATA AND MODULATION~~

I) DPSK Demodulator



- 1) DPSK encodes two distinct signals i.e. the carrier and the modulating signal with 180° phase shift each.
- 2) The serial data input is given to the XNOR gate and the output is again fed back to the other input through 1-bit delay.
- 3) The output of the XNOR gate along with the carrier signal is given to the balanced modulator, to produce the DPSK modulated signal.

II) DPSK Demodulator



- 1) In DPSK demodulator, the phase of the reversed bit is compared with phase of the previous bit.
- 2) The balance modulator is given the DPSK signal along with 1-bit delay input.
- 3) That signal is made to confine to lower

- 4) with the help of LPF
Then it passed to Shaper circuit to recover the original binary data as the output.

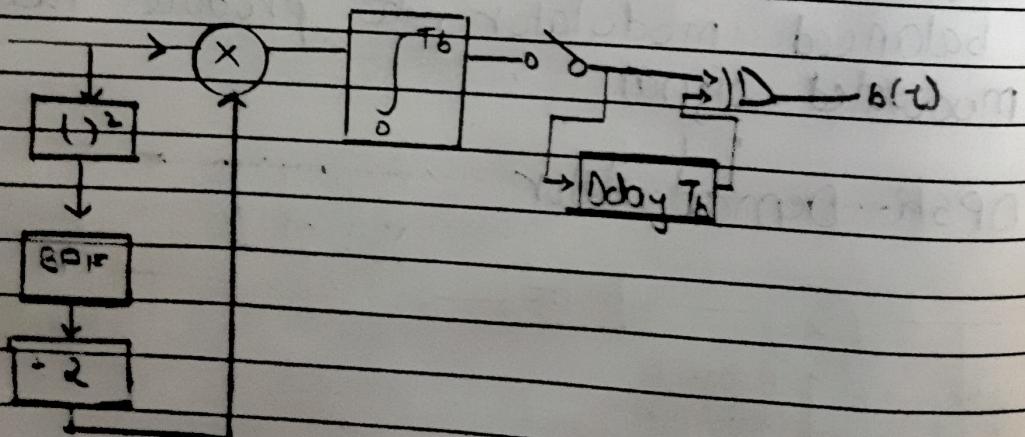


Differentially Encoded PSK (DEPSK)

DEPSK is a type of digital modulation technique where it uses the phase difference between phase difference between successive symbol to encode the data.

I) DEPSK modulation
(same as DPSK)

II) DEPSK Demodulation



* BFSK & BASK
(PVC POF)

* S-2 :- QPSK, M-PSK, M-FSK, QAM, MSK, GMSK

* QPSK

- 1) Quadrature Phase Shift Keying (QPSK) is a digital modulation scheme where four different phase shifts represents binary digits.
- 2) Each symbol carries 2 bits, doubling data rate compared to binary modulation.
- 3) If $N=1$, $M=2^1=2 = \text{BPSK}$
 $N=2$, $M=2^2=4 = \text{QPSK}$

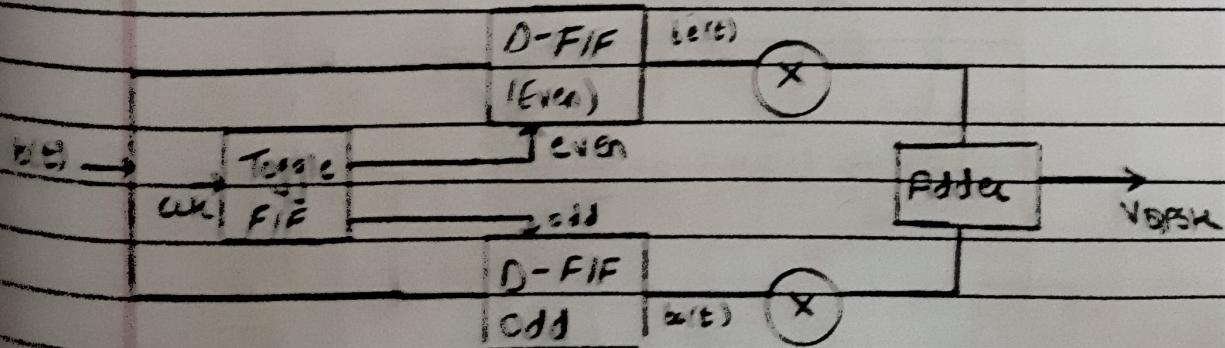
$$\text{Symbol duration} = T_S = N T_b = 2 T_b$$

$$\text{Symbol Rate} = f_S = \frac{1}{T_S} = \frac{1}{2 T_b} = \frac{f_b}{2} = \frac{f_b}{N}$$

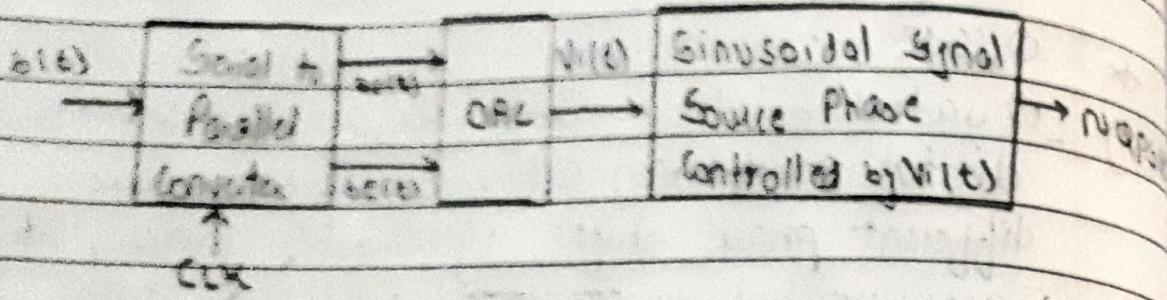
$$\text{Phase shift shift} = \frac{\theta}{M} = \frac{2\pi}{4} = \frac{360}{4} = 90^\circ$$

I) QPSK Transmission / Modulation

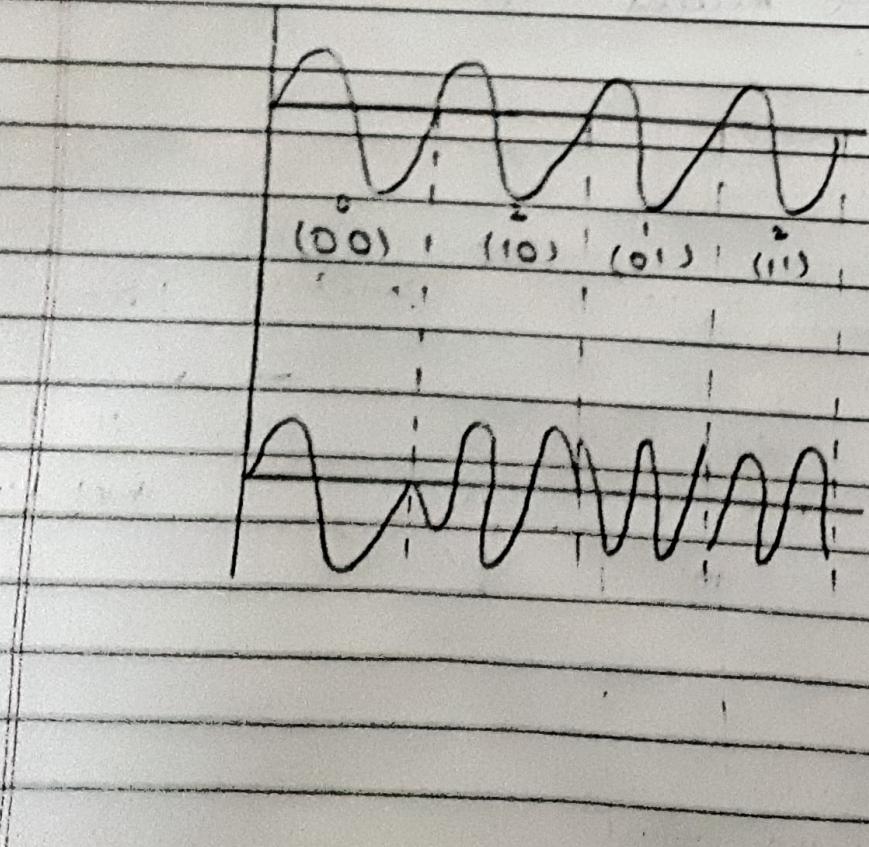
i) Offset QPSK Transmission



2) Non offset QPSK Transmitter

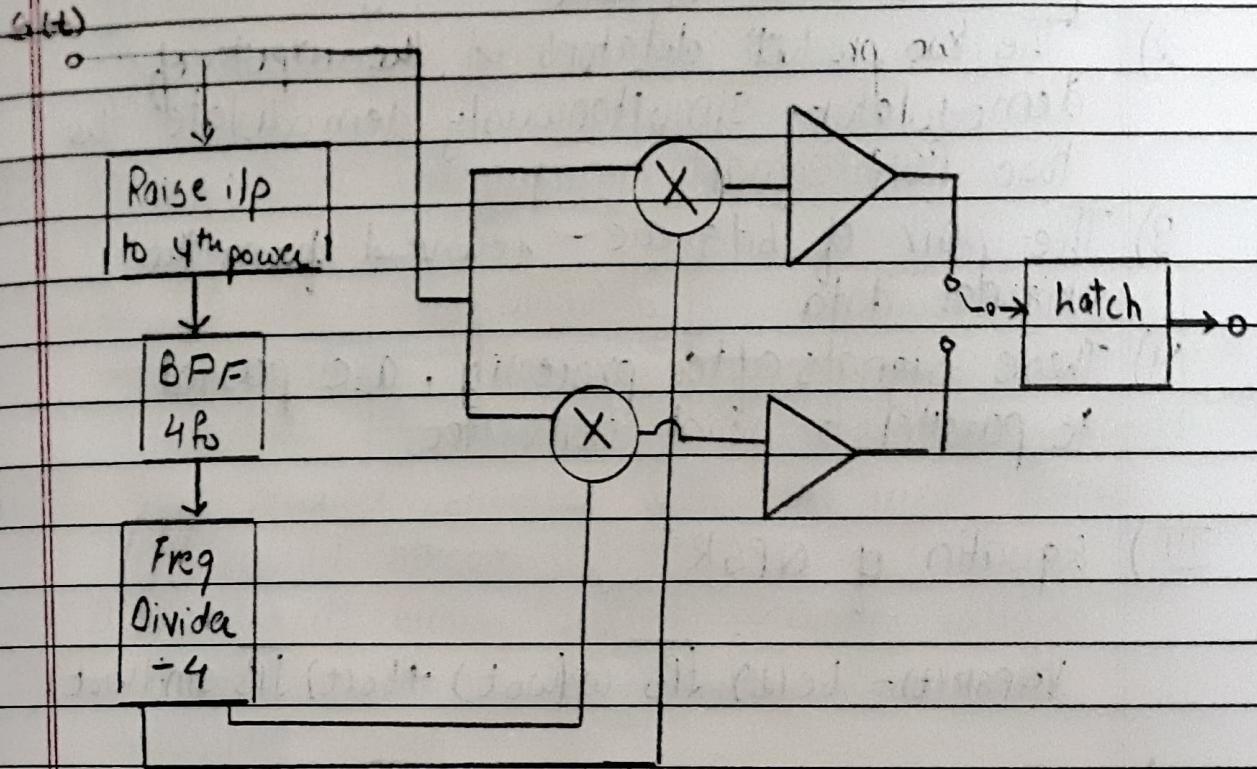


- 1) The QPSK Modulator uses a bit-splitter, two multipliers and local oscillator, 2-bit serial to parallel converted and summed circuit
- 2) At the modulator's input the message signal's even bits and odd bits are separated by the bits splitter and are multiplied with the same carrier to generate odd BPSK and even BPSK
- 3) The PSK signal is phase shifted by 90° before being modulated

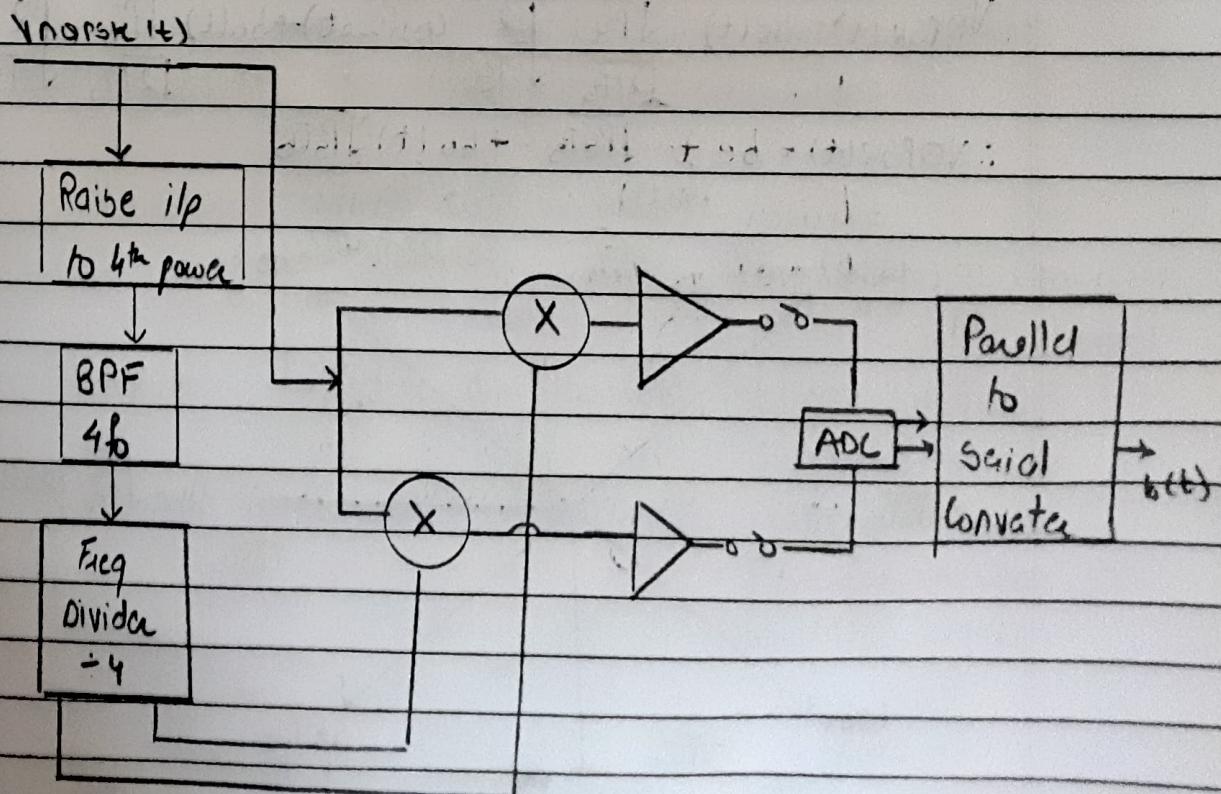


II) QPSK Receiver Demodulation

1) Offset QPSK Receivers



2) Nonoffset QPSK Receivers



- 1) The QPSK receiver uses two product demodulator circuit with local oscillator, two band pass filter, one integrator circuit and a 2-bit modulator to send compare.
- 2) The two product detectors of the input of demodulator simultaneously demodulate the two PSK signal.
- 3) The pair of bits are recovered from the original data.
- 4) These signals after processing, are passed to parallel to serial converter.

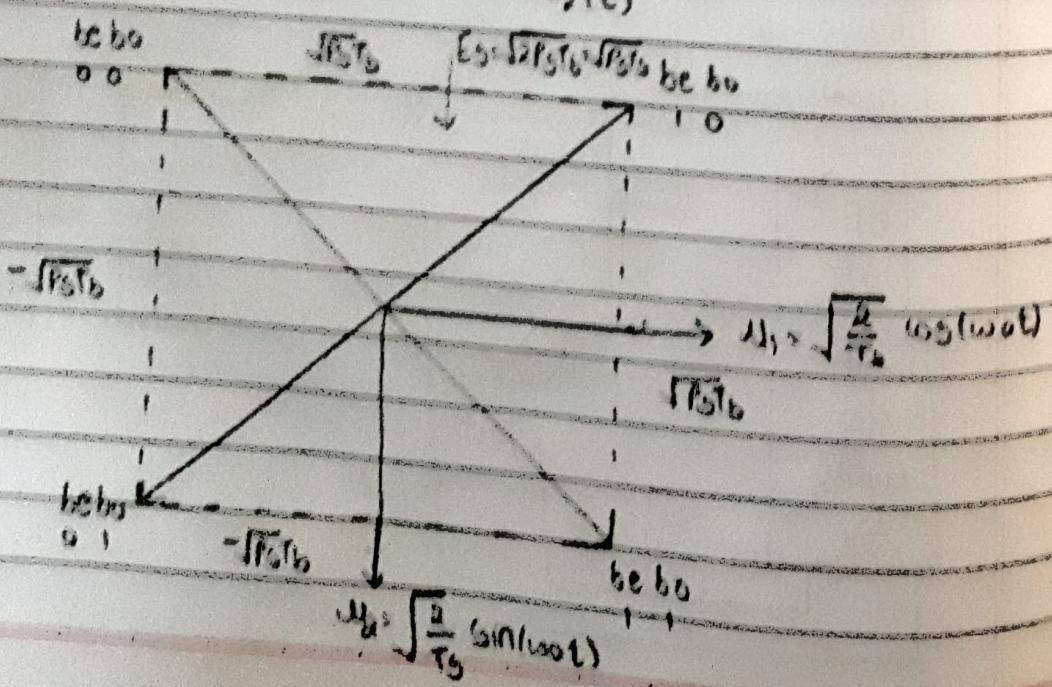
III) Equation of QPSK

$$V_{QPSK}(t) = b_1(t) \sqrt{P_s} \cos(\omega_c t) + b_0(t) \sqrt{P_s} \sin(\omega_c t)$$

IV) Signal Space Diagram

$$V_{QPSK}(t) = b_1(t) \frac{\sqrt{P_s}}{\sqrt{2T_b}} \int_{T_b}^0 \cos(\omega_c t) + b_0(t) \frac{\sqrt{P_s}}{\sqrt{2T_b}} \int_{T_b}^0 \sin(\omega_c t)$$

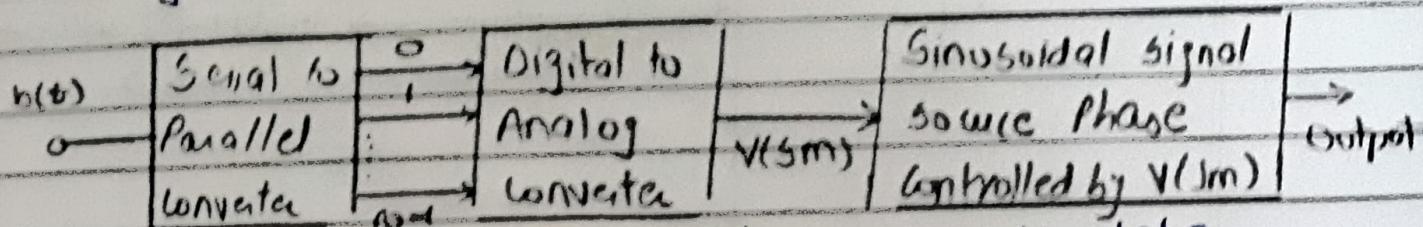
$$\therefore V_{QPSK}(t) = b_1(t) \frac{\sqrt{P_s T_b}}{\sqrt{2}} \cos(\omega_c t) + b_0(t) \frac{\sqrt{P_s T_b}}{\sqrt{2}} \sin(\omega_c t)$$



M-Ary PSK

- i) M-Ary PSK is a variant of phase shift keying where the constellation points are symmetrically positioned around the circle in the complex plane

M-Ary PSK Transmission / Modulation



- 1) Serial to parallel converter splits the input data into parallel stream
- 2) DAC converts binary signal to analog voltages
- 3) Sinusoidal signal source generates a continuous sinusoidal signal
- 4) Adjusts the phase of the sinusoidal signal based on the input data
- 5) Results in the MPSK signal with varying phase shifts, encoding the data for transmission

$$V_{MPSK}(t) = \sqrt{2P_s} \cos(\omega_0 t + \phi_m) \dots \text{where}$$

$$\phi_m = (2m+1) \frac{\pi}{M} \quad m=0, 1, 2, \dots, M-1$$

$$\therefore V_{MPSK} = \sqrt{2P_s} (\cos \phi_m) \cos \omega_0 t - (\sqrt{2P_s} \sin \phi_m) \sin \omega_0 t$$

$$\therefore V_{MPSK} = P_e \cos \omega_0 t - P_o \sin \omega_0 t \quad \text{where,}$$

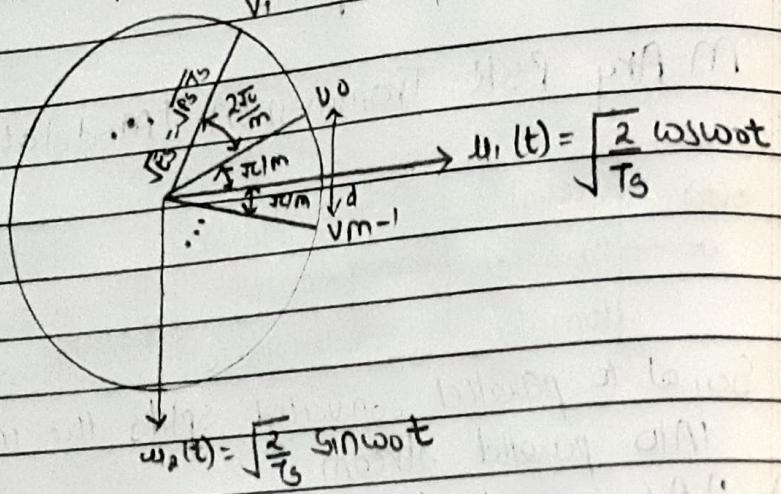
$$P_e = \sqrt{2P_s} \cos \phi_m$$

$$P_o = \sqrt{2P_s} \sin \phi_m$$

II) MPSK Receiver / Demodulation

Same AS QPSK

III) Signal Space Representation



IV) Euclidean Distance

$$\sin\left(\frac{\pi}{m}\right) = \frac{d/2}{\sqrt{E_S}}$$

$$d = 2\sqrt{E_S} \sin\left(\frac{\pi}{m}\right)$$

$$d = \sqrt{4 E_S \sin^2\left(\frac{\pi}{m}\right)}$$

$$d = \sqrt{4 N E_b \sin^2\left(\frac{\pi}{m}\right)}$$

$$E_S = P_S T_S$$

$$E_S = P_S (N T_b)$$

$$E_S = P_S T_b N$$

$$E_S = N E_b$$

V) Bandwidth

$$B.W = \frac{2}{T_S} = \frac{2}{N T_b} = \frac{2 f_b}{N}$$

Thus No of bits (N) \uparrow , BW \downarrow
 $N \uparrow$ $f_b \downarrow$

$$m = 2^N T ; d \downarrow$$

∴ Symbol will hardly spaced
∴ Probability of Error (P_E) ↑