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| **Course Name:** | **Digital Electronics** | **Semester:** | **III** |
| **Date of Performance:** |  | **Batch:** | **A - 3** |
| **Faculty Name:** |  | **Roll no.:** | **16014022050** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_ / 25** |

**Experiment no.: 9**

**Title: Synchronous Counter**

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| **Aim and Objective of the Experiment:** |
| * Implementation of 4-bit synchronous counter using MSI device (IC 74163). * 4 Bit Synchronous counters. |

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| **COs to be Achieved:** |
| **CO3:** Design sequential circuits using MSI devices.  **CO4:** Analyze and design synchronous sequential circuits using flip flops. |

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| **Theory:** |
| **Synchronous Counter –**  The circuit diagram of a 4-bit synchronous counter is shown in figure. In synchronous counter all the flip flops are clocked together. The speed of operation is better than ripple counter as clock is synchronous. From the truth table, the LSB A changes with every clock which can be achieved by giving J =K = 1 (assuming we use a JK FF). In second column, B changes whenever A changes from 1 to 0. So, connect A to the inputs, J and K of next FF. similarly C changes when both A and B are 1. So, J and K of C FF is A and B. Similarly, a change happens in D FF when A, B and C are high. So, input to D is A and B and C.  Since it is a 4-bit counter we require 4 FFs. One FF can store 1 bit.   |  |  |  |  | | --- | --- | --- | --- | | **D** | **C** | **B** | **A** | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 1 | | 0 | 0 | 1 | 0 | | 0 | 0 | 1 | 1 | | 0 | 1 | 0 | 0 | | 0 | 1 | 0 | 1 | | 0 | 1 | 1 | 0 | | 0 | 1 | 1 | 1 | | 1 | 0 | 0 | 0 | | 1 | 0 | 0 | 1 | | 1 | 0 | 1 | 0 | | 1 | 0 | 1 | 1 | | 1 | 1 | 0 | 0 | | 1 | 1 | 0 | 1 | | 1 | 1 | 1 | 0 | | 1 | 1 | 1 | 1 |   Synchronous Counter: Definition, Working, Truth Table & Design  **74163 – 4bit synchronous counter**    74163 has a synchronous clear and present. RC will be 1 when output reaches maximum count. |

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| **Stepwise – Procedure:** |
| 1. **Implement 4-bit counter using 74163 IC.**                1. **Implement mod 11 counter using 74163 (Make use of preset inputs).** 2. **Design the 4-bit synchronous counter on paper using JK FF.**     **\**                 1. **Connect the circuit on bread board/digital trainer.** 2. **First reset the counter to 0 by giving clear input (clear = 0 for JKFF 7476).** 3. **Keep the clear input high for counting.** 4. **Verify the truth table for each clock. (VERIFIED)** |

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| **Post Lab Subjective/Objective type Questions:** |
| 1. **Design a 3-bit binary synchronous up/down counter using T flip-flop and gates.** 2. **Implement a mod 6 counter using a 4-bit synchronous counter IC** 3. **Design a Mod-5 synchronous counter using JK flip-flop and gates.** 4. **What will be the counting sequence?** |

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| **Conclusion:** |
| We have successfully implemented a 4-bit synchronous counter, first using IC 74163 followed by 4 JK Flip Flops i.e., IC CD4027 and then cross examined the corresponding truth tables for each clock. |

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| **Signature of faculty in-charge with Date:** |