|  |  |  |  |
| --- | --- | --- | --- |
| **Course Name:** | **Digital Electronics** | **Semester:** | **III** |
| **Date of Performance:** |  | **Batch:** | **A - 3** |
| **Faculty Name:** |  | **Roll no.:** | **16014022050** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_ / 25** |

**Experiment no.: 8**

**Title: Study of Sift Registers**

|  |
| --- |
| **Aim and Objective of the Experiment:** |
| * Design and Implementation of shift register using Flip Flop and MSI devices   (IC 74194). |

|  |
| --- |
| **COs to be Achieved:** |
| **CO3**: Design sequential circuits using MSI devices. |

|  |
| --- |
| **Theory:** |
| * **Shift Registers –**   In Serial In Parallel Out (SIPO) shift registers, the data is stored into the register serially while it is retrieved from it in parallel-fashion. Figure 1 shows an n-bit synchronous SIPO shift register sensitive to positive edge of the clock pulse. Here the data word which is to be stored (Data in) is fed serially at the input of the first flip-flop (D1 of FF1). It is also seen that the inputs of all other flip- flops (except the first flip-flop FF1) are driven by the outputs of the preceding ones like the input of FF2 is driven by the output of FF1. In this kind of shift register, the data stored within the register is obtained as a parallel-output data word (Data out) at the individual output pins of the flip-flops (Q1 to Qn).     * **Types of Inputs and Outputs –**   Depending on input and output of shift registers they are classified as Parallel In Serial Out (PISO), Serial In Parallel Out (SIPO) parallel In Parallel Out (PIPO) and Serial In Serial Out (SISO)  Whenever input or output is serial, the data will take number of clock cycles to be inputted or outputted hence the access time will depend on width of the shift register   * **Left shift, Right Shift –**   When the number / data is shifted from LSB to MSB it is left shift and when it is shifted from MSB to LSB it is right shift.  In left shift we insert new bits from LSB, in right shift we insert new bits from MSB.  Since in positional numbers bits on left have more weight when the data is shifted left its value increases, when it is shifted right its value decreases.  Left Shift in Binary = Multiplication of 2 (Bit inserted is zero) Right shift in Binary = Division by 2 (Bit inserted is zero)   * **Rotate, Ring counters –**   If we insert LSB to MSB in right shift or insert MSB in LSB in Left shift, then the same bits rotate and that is called as ring counter.   * **Universal Shift Registers (IC 74194) –**   The IC 74194 are high-speed Si-gate CMOS. The functional characteristics of the IC 74194 4-bit bidirectional universal shift registers are indicated in the logic diagram and function table. The registers are fully synchronous.  The synchronous operation of the device is determined by the mode select inputs (S0, S1). As shown in the mode select table, data can be entered and shifted from left to right (Q0 → Q1 → Q2, etc.) or, right to left (Q3 → Q2 → Q1, etc.) or parallel data can be entered, loading all 4 bits of the register simultaneously.  When both S0 and S1 are LOW, existing data is retained in a hold (“do nothing”) mode. The first and last stages provide D-type serial data inputs (DSR, DSL) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.  Mode selects and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.  The four parallel data inputs (D0 to D3) are D-type inputs. Data appearing on the D0 to D3 inputs, when S0 and S1 are HIGH, is transferred to the Q0 to Q3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset (MR) overrides all other input conditions and forces the Q outputs LOW. |

|  |
| --- |
| **Circuit Diagram/Block Diagram:** |
|  |

|  |
| --- |
| **Stepwise – Procedure:** |
| 1. **Implement 4-bit Serial In Parallel out Shift Register using hardware.**    1. **Loading**      * 1. **DSR**        * 1. **DSL**        * 1. **Hold**      1. **Implement 4-bit Parallel in Serial Out shift register using hardware.**      1. **Implement a Ring counter using 4-bit Serial In Serial Out Shift register.**      1. **Verify function table of IC 74194 and also implement a twisted ring counter using it.** |

|  |
| --- |
| **Post Lab Subjective/Objective type Questions:** |
| 1. **How can parallel data be taken out of a shift register simultaneously?**    1. **Use the Q output of the first FF**    2. **Use the Q output of the last FF**    3. **Tie all of the Q outputs together**    4. **Use the Q output of each FF** 2. **The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains**     1. **01110**    2. **00001**    3. **00101**    4. **00101** 3. **Make a MOD-5 Ring Counter using shift register in simulator.**      1. **Using IC 74194 Universal Shift Register implement 8-bit Johnson counter.** |

|  |
| --- |
| **Conclusion:** |
| Through this experiment we have gained a proper understanding of the design and implementation of a shift register with the use of flip-flops and MSI devices (IC 74194). |

|  |
| --- |
| **Signature of faculty in-charge with Date:** |