

Tutorial Week 3: Logical Clocks

Notes

Clock Condition. For all events a, b : if $a \rightarrow b$ then $C(a) < C(b)$. This is satisfied if the following two conditions hold:

- $C1$. If a and b are events in process p_i and a comes before b , then $C_i(a) < C_i(b)$
- $C2$. If a is the sending of a message by process P_i and b is the receipt of that message by process P_j , then $C_i(a) < C_j(b)$

Exercises

10. This question is from last weeks tutorial, please attempt if you haven't already. An NTP server B receives server A 's message at 16:34:23.480 bearing a timestamp 16:34:13.430 and replies to it. A receives the message at 16:34:15.725, bearing B 's timestamp 16:34:25.7. Estimate the offset between B and A and the accuracy of the estimate.

11. Consider the following sequence of events at processes p_0, p_1, p_2 and p_3 . Here s_i and r_i are corresponding send and receive events for all i , while a and b are internal events.

p_0	:	s_1	s_2	r_5		
p_1	:	r_2	s_5			
p_2	:	r_1	a	s_4	r_3	r_6
p_3	:	s_3	r_4	b	s_6	

Use Lamport's logical clock to assign clock values to these events (A diagram may help).

12. By considering a chain of zero or more messages connecting events e and e' and using induction, show that $e \rightarrow e' \Rightarrow L(e) < L(e')$

13. Using the same sequence of events from exercise 10, draw a send/receive diagram to give Vector timestamps to each of the events.

14. Show that:

- (a) $V_j[i] \leq V_i[i]$ for all i, j
- (b) $e \rightarrow e' \Rightarrow V[e] < V[e']$
- (c) $V(e) < V(e') \Rightarrow e \rightarrow e'$

