

TELECOMMUNICATIONS ENGINEER

**Design a power amplifier for IEEE 802.16a
STANDARD**

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**Design a power amplifier for IEEE 802.16a
STANDARD**

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O Επιβλέπων

Patras, 2013.

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that the present thesis, with title:

Design a power amplifier for IEE 802.16a STANDARD

It has been realized and wrote by this student under my supervision, and i authorized it presentation.

Patras, 2013.

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Chapter 1

INTRODUCTION:

As the wireless communication becomes even more preferable, there has been an increased attention and demand for low-cost, high-efficiency, and compact systems. Among all the necessary parts involved in the wireless communication systems, the RF power amplifier is known to be one of the most critical building blocks in the signal transmitters and the most power-consuming component in the system.

More than 6 years ago, IEEE802.16 which was a standard created for a new wide band wireless technology (LMDS), started to take shape.

Day by day it is being more relevant, that is one of the points that make me design an amplifier that would be able to work under one of the standard version, IEEE802.16a. This version considers the transmission on OFDM and operates in a band between 2GHz to 11 GHz with a bandwidth of 28 MHz per channel.

The first part of the theses is an introduction that speaks about this standard, its evolution, the different versions of it and the main features of each version. Also we will comment about WiMAX.

The main purpose of this theses is to design a pre-power for WiMAX in the 5.65 GHz frequency range. The pre-power amplifier main features are moderate linearity and output power. Another goal of the theses is to design the phisical layout of the amplifier for PCB presentation.

The second chapter give the general theory and background fo power amplifiers.

The third chapter explains how to design the amplifier. We will consider the steps we have to follow in order to design an amplifier, such as: our targets and the specifications that we have to take into account, ie. the gain, the compression point at 1 dB, the noise etc; we have to choose the function in the whole circuit, defining if it would be a transmission, reception, low noise, or power amplifier and which class it will be; furthermore we have to choose a suitable transistor; the bias point that makes our transistor work properly, after that design our bias network; consider stability issues of the transistor; design the input and output matching network in order to obtain our targets; uncouple the RF signal from DC.

The following sections of the chapter explain in detail all the steps mentioned above, characterized by our target in order to design a power amplifier to operate as a pre-amplifier, class AB and at 5.65 GHz with a gain of around 10 dB with an approximate bandwidth of 300 MHz.

In order to make our design we used ADS (Advanced Design System) and Matlab (in order to make faster some calculations).

ADS helps us design the matching networks and make the neccesary simulations during the design and it later analysis.

In order to decide which transistor is better suited for the final implementation, we decided to simulate designs with two different transistors. The simulation results for the two designs will help to choose the one that will give us the best Output Power, considering that the target is the design of a Power

Amplifier.

In this chapter we can find the simulations that we realized with ADS in order to see the most important characteristics, like this we can see that the amplifier has been characterized.

Once we choose the transistor that suits better the targets; we proceed to the Layout design, in order to implement the PCB and be able to take some measurements and see if our design finally will work properly.

1.1 IEEE802.16

1.1.1 STANDARD IEEE802.16

The standard IEEE 802.16 gathers the specifications of a radio interface for wireless networks in metropolitan areas. This radio interface is used for give wide band, so it is consider a Broadband Wireless Access technology, BWA.

The first motivation in order to start developing the standard, was the creation of a technology that would allow to achieve the wide band services to remote places where other wide band¹ access technologies couldn't arrive so fast. The use of wireless medium it was a good solution because it allowed to reduce the infrastructure cost and it arrives to places with difficult access (the cable access technology found difficulties).

Nowadays, this technology doesn't give wide band service only in places with difficult access, its use have been extended in order to give services in urban environment, competing with other technologies as xDSL (Digital Subscriber Line), cable, or HSDPA (High- Speed Downlink Packet Access) and HSUPA (High-Speed Uplink Packet Access).

¹we understand as wide band, following the rules, the instant availability of a bandwidth higher than 1 MHz for the transmission of bit rate higher than 1.5 Mbps.

IEEE 802.16 standard speaks about the specifications related to the MAC (Medium Access Control) and the PHY (Physical Layer), we can see it in *Figure 1.1*.

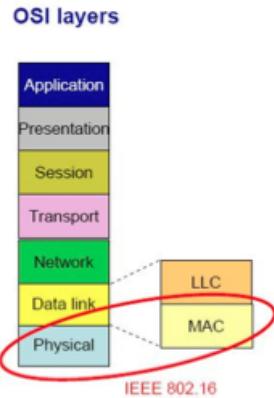


Figure 1.1: IEEE 802.16 layers

1.1.2 HISTORICAL EVOLUTION OF THE IEEE802.16 STANDARD

In 1998, IEEE formed a work team, 802.16, in order to develop the homonym standard. However, it wasn't until December 2001 when the first version was approved. In this first version, the system used modulation techniques with a single carrier (SC) in high frequencies (between 10 and 66 GHz). The use of this high frequencies, generated that only could establish links in environments with direct line of sight (LOS)², and it wasn't good for urban environments. Also, due to the high attenuation that the signal suffers at these frequencies, it is necessary to use of high transmission power in order to have big ranges, and it supposed high cost in the final user terminal. Because of this reason the standard was expanded in order to be able to operate in a frequency range between 2 and 11 GHz, but they maintain the system with a single carrier. This allowed links that didn't need direct line of sight (NLOS) and resulted to the

²The higher frequency, the higher attenuation that the signal suffers when it has to cross and obstacle, so it has less penetration capability.

reduction of transmission power making cheaper the terminal cost.

In 2003, it was developed the IEEE 802.16a amendment, and this included the IEEE 802.16c amendment. In this amendment it was modified the initial standard in order to include the use of OFDM as transmission scheme, this scheme introduce robustness against the multi path phenomenon that affects wireless communication. With OFDM, they improve the system performance, when they were working on NLOS conditions.

In 2004 they made an revision to the IEEE 802.16a standard that drove them to the IEEE 802.16-2004 standard (IEEE 802.16d). Finally, the investigations that they developed in order to afford mobility ended up, in December of 2005, in the last amendment, IEEE 802.16e-2005 (IEEE 802.16e).

Nowadays there exist drafts, one of the most interesting is the IEEE P802.16m, in this one it is defined an improved radio interface.

1.1.3 Physical Layer Specifications (PHY).

We have defined different physical layers, which difference each other with the frequency range that they use, the need of license and the transmission schemes that they use. Now we are going to analyze the most important characteristic of them.

- **WirelessMAN-SC.** It is the physical layer from the original system. It uses only one carrier that is situated between 10 and 66 GHz. Due to high working frequencies we need direct vision conditions (LOS).
- **WirelessMAN-SCa.** It is using a single carrier but it is situated at frequencies under 11 GHz, this lets us use it without the direct vision conditions (NLOS).
- **WirelessMAN-OFDM.** In this case, it is used OFDM as transmission techniques. The sub-carriers are situated under 11GHz that allows the use of NLOS environments.

- **WirelessMAN-OFDMA.** If we compare it with the previous one, this incorporate a sub-channelization system that allows the efficient use of the spectrum by multiple users. It is still using OFDM as transmission technique but increase the number of sub-carriers that can be used, this sub-carriers are situated under 11 GHz so we can use it in NLOS conditions.
- **WirelessMAN-HUMAN.** With this appellation we refer to the result of the adaptation of WirelessMAN-SCa, WirelessMAN-OFDM and WirelessMAN-OFDMA in order to use them in non-license band. An important difference is that we have to use Time Division Duplex (TDD), because the other layers can use Frequency Division Duplex (FDD) and TDD.

1.1.3.1 Physical Layer Parameters.

The fist step is to understand the use of OFDM in the standard. In order that it will be possible it is necessary to analyze each one of the parameters that define the system. In this section we try to explain this parameters that are more important. In order to explain better this parameters, we are going to use *Figure 1.2*, where is graphically represented the meaning of each parameter in the frequency domain.

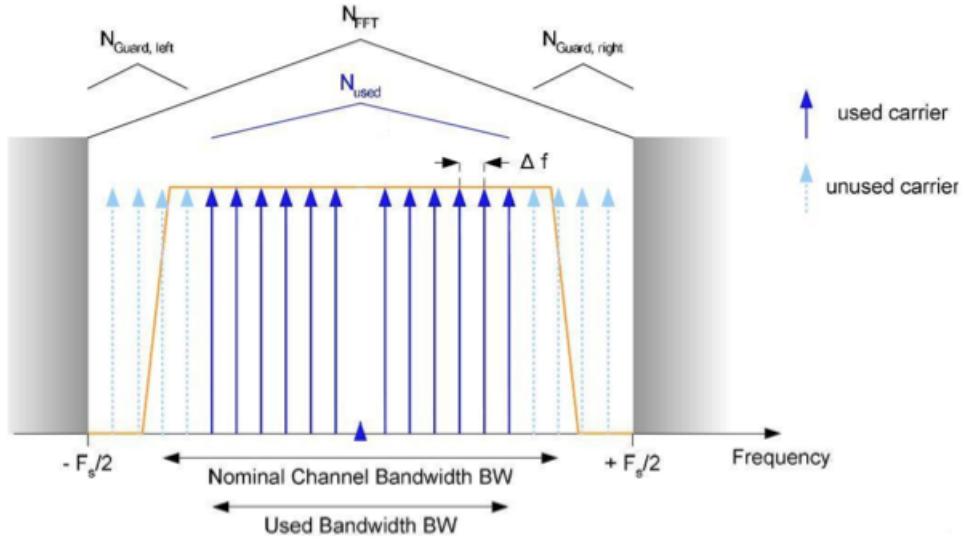


Figure 1.2: Parameters description in OFDM system of IEEE 802.16 in the frequency domain

- **Nominal Bandwidth, BW.** This is the bandwidth that the system can use for its operation. It is related with frequency and sampling factor with the following expression:

$$BW = \frac{F_s}{n} \quad (1.1)$$

It exists different values that we can have, and this values we can see them in the table 1.6.

- **Sample frequency, Fs.** It is the system operating frequency. This is the frequency that generates samples in the D/A converter. It is related with the sample factor and the bandwidth by the following expression:

$$F_s = \left\lfloor n \frac{BW}{8000} \right\rfloor 8000 \quad (1.2)$$

We will see that the sample frequency is bigger than the nominal bandwidth and it can take multiple values because depends on it.

- **Sample factor, n.** This parameter relate the sample frequency and the nominal bandwidth following the next expression:

$$n = \frac{F_s}{BW} \quad (1.3)$$

Its value depends on the value that the nominal bandwidth will take³, but always is greater than one (that's why $F_s > BW$).

- **Number of sub-carriers, Nfft.** In WirelessMAN-OFDM physic layer, its value is constant, and is 256. In WirelessMAN-OFDMA physic layer its value depends on the nominal bandwidth that we use, and it is chosen in a way that the sub-carriers separation will have a fixed value of 11.94KHz.
- **Sub-carriers separation, Δf.** The frequency separation between sub-carriers can be defined by $\Delta f = F_s / N_{fft}$. In WirelessMAN-OFDMA its value depends on F_s value because N_{fft} is fixed. As mentioned before, in WirelessMAN-OFDMA N_{fft} has a fixed value (11.94KHz).
- **Useful OFDM symbol time, $T_{s,OFDM}$.** $T_{s,OFDM} = N_{fft} / F_s = 1 / \Delta f$
- **Guard reason, G.** It is the reason between the cyclic prefix, T_g , and the useful symbol time, $T_{s,OFDM}$. $T_{s,OFDM} \cdot T_g = G \cdot T_{s,OFDM}$
- **Total OFDM symbol time, TOFDM.**

$$T_{s,OFDM} = (1 + G)T_{s,OFDM} = T_g + T_{s,OFDM} \quad (1.4)$$

In *Table 1.1* we have a summary of the values that can take some of this parameters and values for another parameters that are important too.

³n wirelessMAN-OFDMA its value is fixed and equal to 8/7

Parameter	Value
N_{fft}	256
N_{used}	200
$N_{guard,inf}$	28
$N_{guard,sup}$	27
$G = T_g/T_{sOFDM}$	1/4, 1/8, 1/16, 1/32
N_{pilot}	8

Table 1.1: Basic parameters of WirelessMAN-OFDM physical layer

We can see that from the 256 carriers that are specified, 8 are used as pilot sub-carriers , 55 as guard sub-carriers and 200 as data sub-carriers, also we have the DC sub-carrier, that is not used in data transmission.⁴ The pilot sub-carriers are used to estimate the channel and synchronization (we will see later on detail). In *Figure 1.3* we have the spectrum of the OFDM signal.

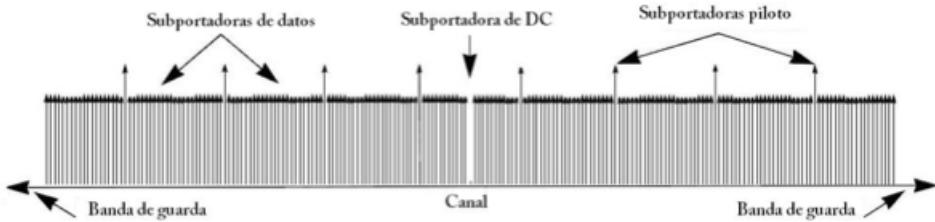


Figure 1.3: Frequency description of OFDM signal. The pilot sub-carriers are transmitted with the same power level as the data sub-carrier, in the figure they are different in order to distinguish them better.

We can see that the bandwidth that occupies the OFDM signal has to be contained on the nominal bandwidth that has for its transmission. From equation (1.5), we can see that this relation is always true. In this equation we have to take into account that the pilot sub-carriers and the DC sub-carriers contribute to the occupied bandwidth.

⁴The DC component is used to be a problem, if we think in the electronic, when we try to design the receiver. That is why it is transmitted without modulate.

$$(N_{used} + N_{pilots} + 1)\Delta f \leq BW \quad (1.5)$$

It is important to realize that the sub-carriers number N_{fft} is fixed at 256; if we change the nominal bandwidth, the separation between the sub-carriers and the OFDM symbol duration will change.⁵ That is why, depending on the BW that the system will use, the way that it will be affected by the channel will change because the relation between the OFDM symbol duration and the channel coherence time, and between the coherence BW and the separation between sub-carriers, changes.

1.1.3.2 Frame structure.

In order to understand how the data is transmitted, it is necessary to study the frame structure in the physical layer. However, we will not see how the MAC layer organize the information for higher levels ins this frames.

In most of the applications that are based on the standard we use TDD as duplexing mode. In this case. the frame is divided on two sub-frames, the first one correspond to the downlink (DL) and the second to the uplink (UL); they are transmitted one after the other, it is showed in *Figure 1.4*. We have a transmit transition gap (TTG) between the the sub-frame DL and UL and RTG (Receive Transition Gap) that it separates the sub-frame DL and UL from the next frame.

⁵Previously, we commented that in WirelessMAN-OFDMA it is not happening, because we use different number of sub-carriers depending on the used BW in order that the separation between them remains constant and equal to 11.94 KHz.

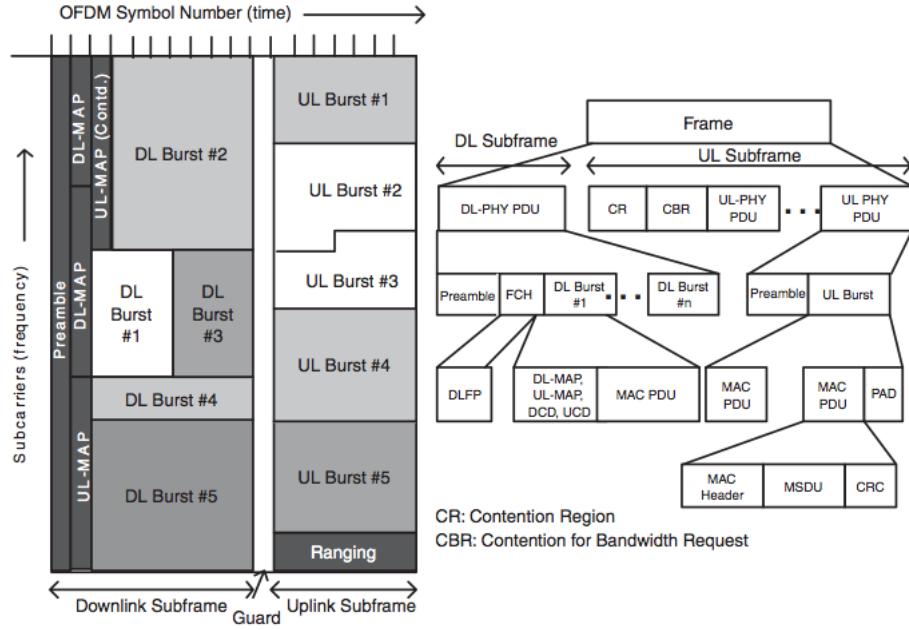


Figure 1.4: A sample TDD frame structure for mobile WiMAX

1.1.3.3 Channel codification.

The communication channel distorts the signal that is transmitted across it, and also adds AWGN noise. This makes that the error probability in the receiver gets bigger. In order to reduce it, we use codification channel techniques that protect the signals against the channel adversities. The losses in the spectral and energetic efficiency due the use of channel codification is smaller than the losses that we will have if we should retransmit (if the application allows it) the data frames that arrive with errors in the receiver.

In the WirelessMAN-OFDM, the channel codification is composed by 3 stages: randomization, FEC and interleaving. These operations have to be done in this transmission order and the complementary operations have to be done in the receiver in the opposite way. Now we are going to describe them.

- **Randomization:** With this step we want to improve the source entropy,

that means that we want to make equal the transmission probability of zeros and ones. The ML detector (maximum-likelihood) that we use in the receiver will be equivalent to a MAP detector (maximum a posteriori) and it will be optimum. As a process consequence, the long strings of consecutive ones and zeros that could exits in the transmitted binary sequence are eliminated.

In order to do the randomization process we use a pseudo random bit sequence (PRBS) (*Figure 1.5*). It is described by the polynomial

$$1 + X^{14} + X^{15}$$

The initialization sequence that we use, is composed by the station base identifier (BSID), DIUC or UIUC (if we are in an uplink or downlink) and the frame number that we are transmitting.

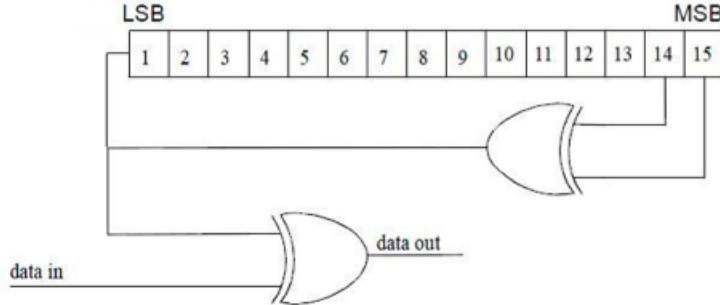


Figure 1.5: PRBS generator for randomization process

In *Figure 1.6* we can see the initialization sequence for both links. It is important to realize that only the data is randomized.

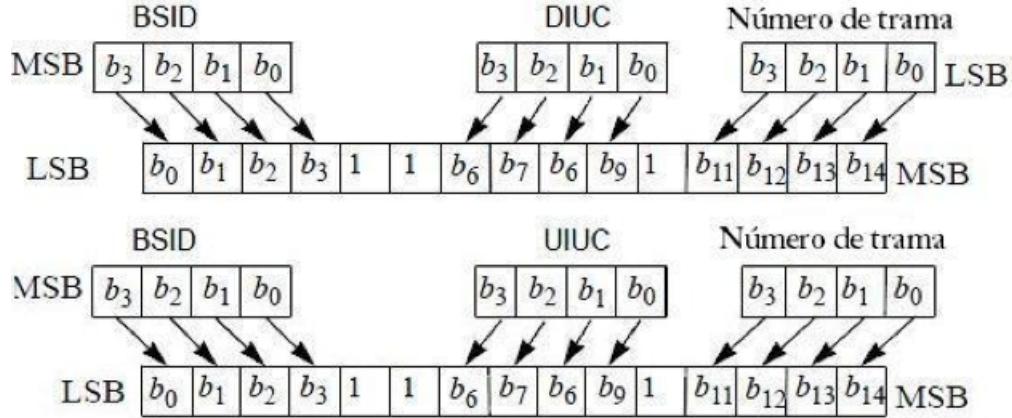


Figure 1.6: initialization sequence for the up and down link.

- **FEC codification:** It is the next step, and protects the randomized data by adding redundancy. This step will allow the receiver correct some errors that could be introduced by the channel. The codifier is formed by a Reed-Solomon code (as internal code) and a convolutional code (as external code).

The RS code is a block code that has to be derived from a systematic RS code⁶ ($N=255$, $K=239$, $T=8$) that uses a Galois Field, where N is the bytes number of the output block, K is the number of bytes of the input block and T represents the maximum number of wrong data bytes that can be corrected in a block. We can see that the codifier works at code rate $K/N=239/255$. In the standard is explained how to make shorter this code (and reduce the obtained redundancy) in order to obtain RS codes with bigger rates than the original. In order to generate these codes we use the following polynomials:

$$\text{code generator polynomial: } g(x) = (x+\lambda^0)(x+\lambda^1)(x+\lambda^2)\dots(x+\lambda^{2T-1}), \lambda=02_{\text{HEX}}$$

$$\text{field generator polynomial: } p(x) = x^8 + x^4 + x^3 + x^2 + 1$$

⁶For this code we distinguish the redundant bits from the data ones. (we have the original data block and we add another block that contains the redundant bits; this block goes before or after the data block.)

Once that the data goes through the RS codifier, the next process is a convolutional codification. The convolutional codifier is binary, with $1/2$ rate and restriction length 7, as the one that we show in *Figure 1.7*.

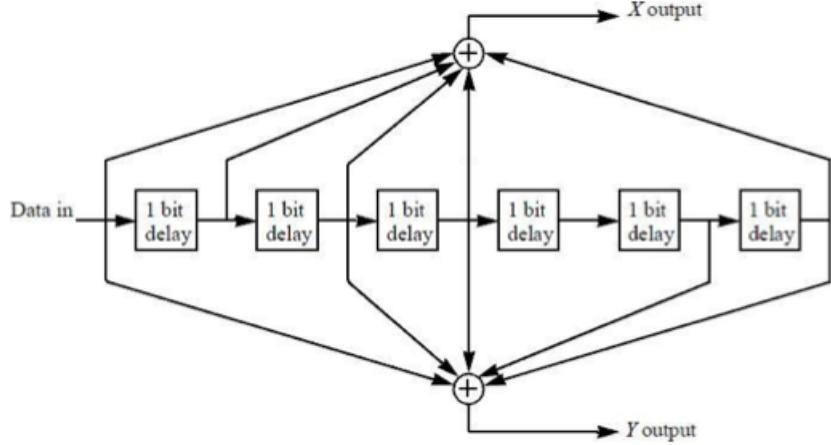


Figure 1.7: Convolutional codifier with $1/2$ rate.

In the standard, the use of puncturing is considered, in order to achieve different code rates. This process consist of deleting some stream bits from the codified output, it depends on some patterns that we can see in *Table 1.2*. In this table, the number 1 denote a transmitted bit while a 0 denotes a deleted bit, and X and Y are the convolutional codifier outputs in reference to *Figure 1.7*.

Code rate				
Rate	$1/2$	$2/3$	$3/4$	$5/6$
d_{free}	10	6	5	4
X	1	10	101	10101
Y	1	11	110	11010
XY	$X_1 Y_2$	$X_1 Y_1 Y_2$	$X_1 Y_1 Y_2 X_3$	$X_1 Y_1 Y_2 X_3 Y_4 X_5$

Table 1.2: Puncturing patterns that are specified on the standard

- **Interleaving:** The output bits from the codifier are interleaving. The interleaving that is describe on the standard is different than the one that

is used on the single carrier, but the main idea remains constant.

In the single carrier system, it is used in order to reduce the selective fading effects on the time that affects the signal. This will make that the channel introduce attenuation that will affect the consecutive symbols that are transmitted in the channel during this time. As consequence, we will receive long strings of bits that will be wrong. This string will overpass the capability of bits correction (RS and convolutional) so it will not be able to correct them. The interleaving process works over a bits block, making a temporal shuffled of the bits on the transmitter in order that when they are unshuffled in the receiver, the burst errors will be dispersed and the error corrector codes will be able to correct them.

In a multiple carrier system, a consecutive bits sequence is transmitted in the same time instant by different sub-carriers. In this case, the error burst on the receiver will not be produced by the selective fading on the time, it will be produced by the selective fading on frequency. Due to this, the symbols that will be transmitted by the adjacent sub-carriers could suffer a big attenuation and this will generate a error burst in the receiver.

The interleaving process that is specified in the standard is divided in two stages:

1. In the first stage, the output bits from the convolutional codifier is distributed between the different sub-carriers, like this the consecutive bits will not be transmitted by the adjacent sub-carriers.
 2. In the second stage, we ensure that the adjacent bits are mapped in more significant bit (MSb) and less significant bit (LSb) in the constellation, like this we reduce long bits stream with low reliability.
- **Modulation Schemes:** This process consist on mapping k input bits to $M=2^k$ complex symbols on a constellation, and it depends on the

modulation scheme that we use. The IEEE 802.16 standard propose four schemes that can be used for data modulation: BPSK, QPSK, 16-QAM and 64-QAM. Whatever is the modulation that we use, the bits map is realized by Gray coding, this allows to minimize the error bit probability from a given error symbol probability. In *Figure 1.8* we can see the modulation explained on the standard.

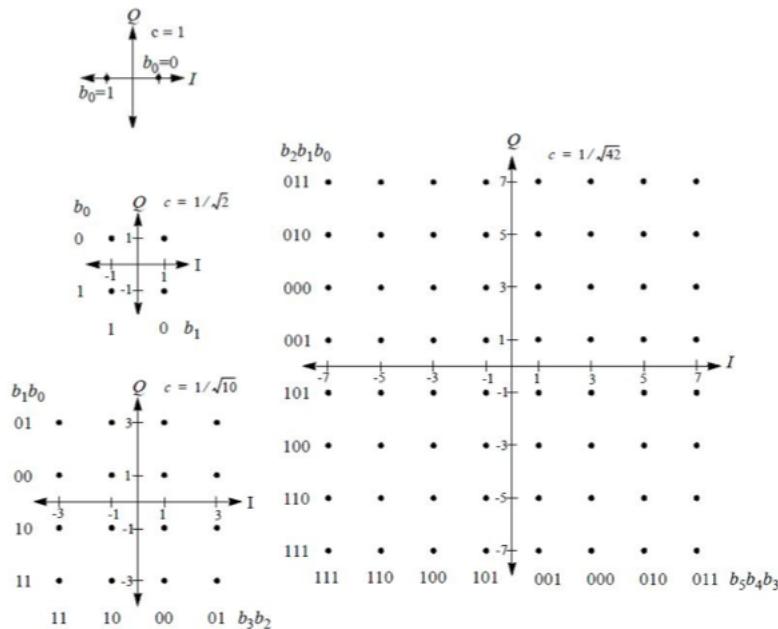


Figure 1.8: BPSK, QPSK, 16-QAM, and 64-QAM

We note that a factor “c” is specified. This factor normalizes the symbols in order that all the constellations have the medium energy equal to the unit.

The mapped symbols modulate each sub-carrier from the OFDM scheme. In order to do this, we use a block that implements the IFFT.

In the receiver, we realize the complementary processes in the inverse order, once that we have done the FFT and we decide the symbols, we will demodulate them, the interleaving on the resulting bits, its decoding (using a Viterbi

decoding for the convolutional codification) and the derandomization.

1.2 WiMAX

A lot of times we use the WiMAX term (Wireless Interoperability for Microwaves Access) in order to refer on the technology based on the IEEE 802.16 standard.

However, we have to underline the differences between them.

The WiMAX Forum is a World-wide consortium (chip manufacturer, software developers, equipment manufacturer, service providers...). Its objective is the interoperability promotion of products based on the a-normalized standard IEEE 802.16/ETSI HiperMAN. The product interoperability allows the economy of scale and that allows the introduction of high performance products in a competitive price. With this, WiMAX Forum is contributing to the acceleration of the the WiMAX use. In order to achieve this purpose, WiMAX Forum has certification laboratories in all the World, this labs realize interoperability test and they are trying to adequate the standard.

Last but not least, we explain the differences between the IEEE 802.16 standard and WiMAX technology. In the IEEE 802.16 standard, it exists multiple optional possibilities and characteristics on the PHY layer and on the MAC layer, and this point make difficult the interoperability between products from different manufacturer that are based on the same standard. WiMAX Forum reduces the optional characteristics in order to make easier the interoperability. The specifications are grouped into two groups:

- **System profiles:** It includes characteristics and parameters on the MAC and PHY layers from the IEEE 802.16 standard that constitute the specifications from the WiMAX system (we can see the profiles on *Table 1.3*). We can see that WiMAX only uses the OFDM and OFDMA technology.

System profile	Fixed WiMAX	developed WiMAX	Mobile WiMAX
standard base	IEEE 802.16-2004	IEEE 802.16-2005	IEEE 802.16-2005
multiplexing	OFDM	OFDM	OFDMA
FFT	256	256	512, 1024, 2048
duplexing	TDD, FDD, HFDD	TDD	TDD
modulation	BPSK, QPSK, 16-QAM, 64-QAM BPSK	QPSK, 16-QAM, 64-QAM (optional)	BPSK, QPSK, 16-QAM, 64-QAM (optional on UL)

Table 1.3: System profiles from WiMAX Forum

- **Certification profiles:** There are specifications subsets of the system profiles that collect the characteristics that the products have to follow in order to obtain the interoperability certificated of the WiMAX Forum. As we can see on *Table 1.4*, this characteristics depends on the operation frequencies band, bandwidth and duplexing mode.

Certification profiles	frequency	range duplexing	channel BW	
Fixed WiMAX	3.4-3.6 GHz	TDD	3.5 MHz	
			3.5 MHz	
		FDD	10 MHz	
			7 MHz	
	5.725-5.85 GHz	TDD	10 MHz	
developed WiMAX	4.935-4.99 GHz	TDD	10 MHz	
Mobile WiMAX	2.3-2.4 GHz	TDD	5.1 MHz (dual)	
			8.75 MHz	
	2.496-2.69 GHz		5.1 MHz (dual)	
			5MHz	
	3.4-3.6 GHz		7 MHz	

Table 1.4: Certification profiles from WiMAX Forum

Chapter 2

RF POWER AMPLIFIER THEORY

In this chapter, basic background and some definitions are mentioned for power amplifiers. Firstly, general transceiver architecture and the role of power amplifier are explained. Then, the main characteristics of an amplifier such as power output capability, power added efficiency, total harmonic distortion are defined. Also basic linear power amplifier classes are mentioned shortly.

2.1 POWER AMPLIFIER BASIS

The RF pre-power amplifier (pre-PA), which is a critical element in a transmitter system, and is expected to provide a suitable output power at a good gain with high efficiency and linearity. The output power of a PA must be sufficient to drive the final PA and get a reliable transmission. High gain reduces the number of amplifier stages required to deliver the desired output power and hence reduces the size and manufacturing cost. Power amplifiers show variation in terms of linearity, output power or efficiency. Some parameters are important to quantify an amplifier's performance. These can be listed as power gain, power output capability, power added efficiency (PAE), 1-dB compression point, intermodulation distortion (IMD), Adjacent Channel Power Ratio (ACPR), and intercept point. All these characteristics are discussed in this chapter.

In general, a power amplifier transforms DC power supplied by DC supply to amplification capability of a RF signal. Basically, a power amplifier is composed of an active device, usually a single bipolar junction transistor (BJT) or a field effect transistor (FET), DC feed, output-matching network, and input-matching network. The active device acts as a current source driven by the appropriate DC bias and the input signal. The input and output matching networks optimize the source and the load to the transistor impedances to provide in most cases maximum gain and high output power. The overall efficiency of the transistor is defined as the ratio of RF power received by the load to the DC power used to feed the amplifier. On top of the efficiency measurement of the power amplifier, another important parameter for high efficient power amplifier is power added efficiency (PAE). Power added efficiency is a measurement of maximum output RF power to input RF power over the DC power used to feed the amplifier. Thus, it is important to be able to transfer the maximum amount of DC power to the load as RF power.

2.1.1 Requirements

Before the actual design of a high power amplifier, initial design goals must be defined.

- The PA must operate at a central frequency of 5.65 GHz,
- The PA must have at least 200MHz bandwidth, and return losses of 10 dB, in order to receive multiple channels, not only one.
- The PA must have around 10 dB gain.
- The PA must have an output power level around 2 Watts.

The transistor that will be used for this project is chosen to be a GaN HEMT transistor provided by CREE, the initial goals are developed from the datasheet of the transistor, but at the beginning we used a transistor provided by Avago, we discard it because we couldn't obtain the output power that we had specified

as a goal, even like this we will go through it design and we will see the obtained results for this transistor. Initial design goals are shown in *Table 2.1*.

Frequency	5.65 GHz
Pout	\simeq 2 Watts
Gain	\simeq 10 dB
BW	\simeq 200 MHz, with -10 dB RL

Table 2.1: Initial Design Goals

2.1.2 Gain

Because amplifiers have the ability to increase the magnitude of an input signal, it is useful to be able to rate an amplifier's amplifying ability in terms of an output/input ratio. The technical term for an amplifier's output/input magnitude ratio is gain. As a ratio of equal units (power out / power in, voltage out / voltage in, or current out / current in), gain is naturally a unitless measurement.

If magnitude of the output signal is shown as X_O and input signal is shown as X_I , the gain will be their ratio as shown below.

$$G = \frac{X_O}{X_I} \quad (2.1)$$

2.1.3 1-dB compression point (P_{1-dB})

A constant gain for a given frequency means the linear region of an amplifier . In the real behavior of an amplifier, this linear region ends at a specific frequency; so after this frequency, increasing the input signal does not make the output increase. The input 1dB compression point is defined as the power level for which the input signal is amplified 1 dB less than the linear gain (*Figure 2.1*). The gain decreases rapidly after this 1dB compression point. After this point, amplifier is in the nonlinear region. This means the 1dB compression point is a measure of the linear range of operation.

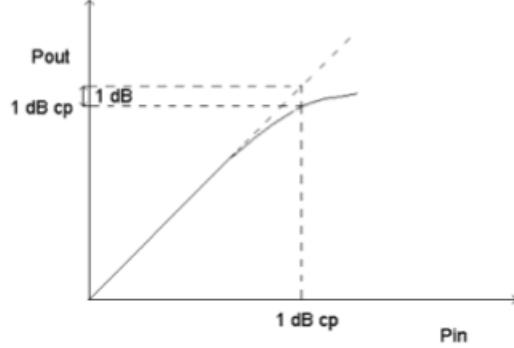


Figure 2.1: 1-dB compression point

2.1.4 Power Added efficiency (PAE)

Power-Added Efficiency (PAE) is a measure of the power conversion efficiency of power amplifiers. Ideally, all supplied power to the amplifier is converted into output power. However, that is not the case in reality. As such, PAE is an important performance parameter for power amplifiers, and is commonly defined as

$$PAE = \frac{P_{RF,OUT} - P_{RF,IN}}{P_{DC}} \quad (2.2)$$

Between linear and saturation regions of operation, there is a point where the power amplifier is most efficient. Up to a certain point, output power is improved while input power is increased. Beyond that point, increased input power will only generate more heat for the device. The objective of PAE measurement is to find this optimal point, the point where the power amplifier is most efficient in transferring input power into output power.

2.1.5 Intercept Point (IP)

In the logarithmic input-output power curve, the fundamental frequency and intermodulation frequency behaviors of an amplifier can be shown together. The slopes of these two curves meet on a point which is defined as the intercept

point. In this point, fundamental and intermodulation products have equal amplitude at the output of a linear circuit. But practically, these amplitudes start decreasing before this point. As a result, the third order intercept point (IP3) is defined as a meeting point of linear extrapolation of the output characteristics for small input amplitude. In this point, which is shown in *Figure 2.2*, is important to analyze the effects of third order nonlinearities. It can be shown as input or output referred.

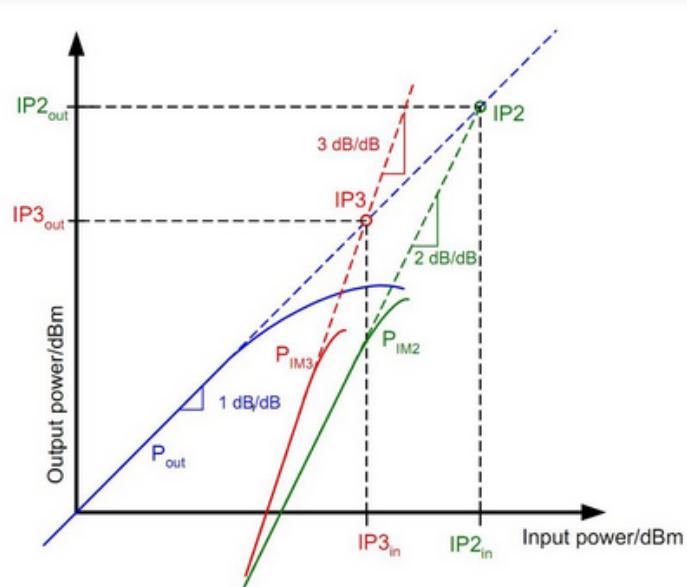


Figure 2.2: 2nd and 3rd Order Intercept Point

2.1.6 Power Output Capability (C_p)

The power output capability is defined as the output power produced when the device has a peak collector voltage of 1 Volt and a peak collector current of 1 Ampere. If the power amplifier uses two or more transistors, then the number of devices is included in the denominator.

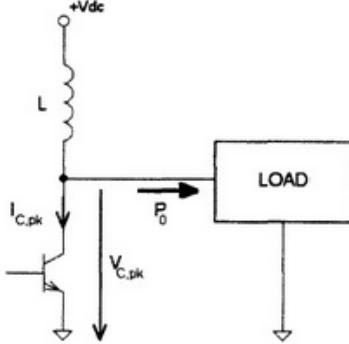


Figure 2.3: Power output capability in RF power amplifiers.

In *Figure 2.3*, if P_0 is the RF output power, $I_{C,pk}$ is the peak collector current, $V_{C,pk}$ is the peak collector voltage, and N is the number of transistors in the circuit, then the power output capability is given by

$$C_p = \frac{P_0}{NI_{C,pk}V_{C,pk}} \quad (2.3)$$

Power transistors are the most expensive components in power amplifiers. In cost-driven designs, designers are constrained to use the lowest cost transistors. This means the devices have to be used as close as possible to their maximum voltage and current ratings. Therefore, the larger the power output capability of the circuit, the less expensive its practical implementation.

2.1.7 Total harmonic distortion

The total harmonic distortion, or THD, of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

$$THD = \frac{\sum \text{harmonics, power}}{\text{fundamental, frequency, power, } P_1} = \frac{P_2 + P_3 + P_4 + \dots + P_n}{P_1} \quad (2.4)$$

Measurements for calculating the THD are made at the output of a device under specified conditions. The THD is usually expressed in percent as distortion factor or in dB as distortion attenuation.

2.1.8 Intermodulation distortion

The linear combinations of the fundamental frequency and all harmonics present in the input signal compose a nonlinear distortion. Intermodulation distortion is characterized by this distortion. If f_1 and f_2 are the fundamental frequencies, then the intermodulation products are seen at frequencies given by

$$f_{IMD} = m f_1 \pm n f_2 \quad (2.5)$$

where m and n are integers from 1 to ∞ .

Figure 2.4 shows the higher order intermodulations. Intermodulation is specified by the ratio of power in the intermodulation product to the power in one of the fundamental frequencies. The third order intermodulation products (at frequencies $2f_1 - f_2$ and $2f_2 - f_1$) are typically the most critical ones because they are the closest products to the fundamentals and it is hard to filter them out from the pass band.

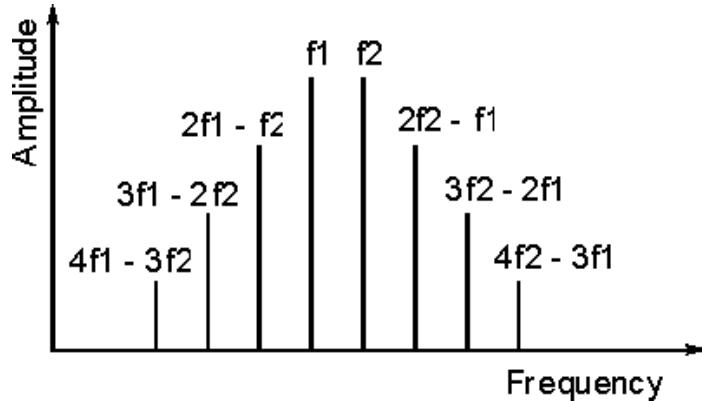


Figure 2.4: Intermodulation distortion

2.2 Amplifier design techniques

Microwave amplifiers are used to obtain low noise, high gain, or high power for different applications in communication systems. In a transceiver system, when the amplifier is used in the receiver side, its gain must be high and the noise

is low. Its signal level and output power are also low. In the other hand, the transmitter side needs high power amplifier to send its output signal for long range communication.

There are some parameters to take into account in the design of a small-signal microwave amplifier. DC bias point is one of the most important parameters which defines the characteristic of the amplifier. Scattering parameters (s-parameters) of a transistor (or a two-port network) are also important for the performance of the amplifier. Stability, input and output matching network designs are based on these s-parameters.

2.2.1 Bias network, class AB amplifier.

Traditionally, the power amplifiers subdivision have been done by “classes”, we do this subdivision attending to the polarization point. In RF the class is identified by capital letter, so we can find the A, B, AB, C, D, E, or F class, this division goes from very linear amplifiers, with low efficiency, to non-linear amplifiers with a high efficiency. For our design it is not very important the fact to have a very high efficiency, but we need a high linearity and a high gain in the desired bandwidth, that's why we decided to use a class A/B amplifier.

2.2.1.1 The class AB amplifier.

If the trade-off between Class A and B make trouble for the designer, Class AB would be a solution for linearity and efficiency. The operating point is chosen between the former classes. Of course, the optimum point is decided according to the application. As estimated, the conduction angle of this class is between π - 2π . Generally it is chosen close to the threshold voltage of the device.

The waveforms can be seen in *Figure 2.5*.

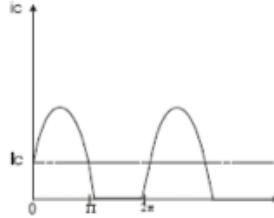


Figure 2.5: Class AB amplifier waveform

If it is compared to the other ones, Class AB has higher power efficiency than Class A and wider transistor response than Class B. In telecommunication applications, this class of operation is widely used.

The class-AB amplifier is a compromise between class A and class B in terms of efficiency and linearity. The transistor is biased as close to pinch-off as possible, typically at 10 to 15 percent of IC. In this case, the transistor will be on for more than half a cycle, but less than a full cycle of the input signal.

2.2.1.2 S-parameters basics.

S-parameters are important in microwave design because they are easier to measure and to work with at high frequencies than other kinds of two-port parameters. They are conceptually simple, analytically convenient and capable of providing detailed insight into a measurement and modeling problem.

The S-parameters are defined as:

$$b_1 = s_{11}a_1 + s_{12}a_2 \quad (2.6)$$

$$b_2 = s_{21}a_1 + s_{22}a_2 \quad (2.7)$$

where, 1 and 2 show the first and the second ports of the transistor, “a” is the power wave traveling towards the two-port gate and “b” the power wave reflected back from the two-port gate.

This means that S-parameters do relate traveling waves (power) to a two-port's reflection and transmission behavior. Since the two-port is imbedded in a characteristic impedance of Z_0 , these 'waves' can be interpreted in terms of normalized voltage or current amplitudes.

$$a_1 = \frac{V_{TOWARDS,TWOPORT}}{\sqrt{Z_0}} \quad (2.8)$$

$$b_1 = \frac{V_{AWAY,FROM,TWOPORT}}{\sqrt{Z_0}} \quad (2.9)$$

In order to understand the meaning of the different S-parameters we have

Figure 2.6

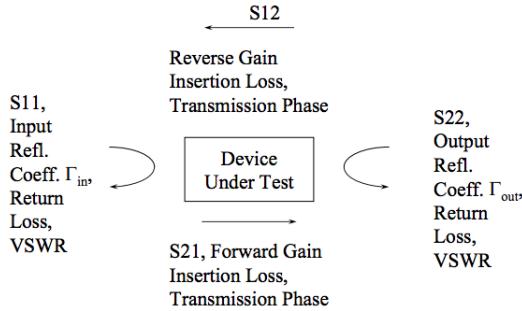


Figure 2.6: S-parameters

2.2.1.3 Amplifier stability

In a two-port network, oscillations are possible when either the input or output presents a negative resistance. The oscillation starts when a reflection coefficient (S_{11} or S_{22}) becomes greater than one, $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. In order to have stability, the input and output reflection coefficients must be smaller than one for all the values of Γ_L and Γ_S using passive matching circuits.

An amplifier can be unconditionally stable or conditionally stable. If for all passive load and source impedances, the real part of the input and output impedances are greater than zero, it is unconditionally stable. But for any load or source impedance, if it becomes less than zero, it means conditionally stable.

In terms of reflection coefficients, the conditions for unconditional stability at given frequency are:

$$|\Gamma_s| < 1 \quad (2.10)$$

$$|\Gamma_L| < 1 \quad (2.11)$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \quad (2.12)$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right| < 1 \quad (2.13)$$

These parameters are shown in *Figure 2.7*, where all the coefficients are normalized to the same characteristic impedance Z_0 .

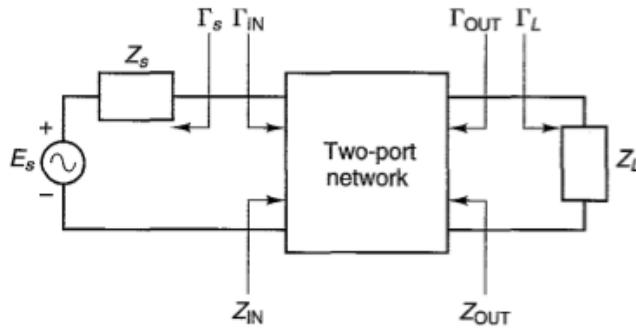


Figure 2.7: Stability of two-port network

In order to measure the stability we can use the stability circles, where $|\Gamma_{IN}| = 1$ and $|\Gamma_{OUT}| = 1$. These two circles reflect the boundary between conditional and unconditional stable. So, they indicate the boundaries of the geometrical plane that make the network being unconditional stable or conditional stable.

Another way to study the stability, using S-parameters, is by using the Rollet factor, k.

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (2.14)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (2.15)$$

This equations defines the unconditional stability with $k=1$ indicating the boundary between unconditional and conditional stability. We can use this analysis only on a single-stage amplifier. If we have more than one amplifier, the k-factor analysis is not enough for guarantee overall stability.

Besides the Rollet Factor, we have another criterion that can be used to prove the unconditional stability, the μ -factor, is defined as

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22}S_{11}^* \Delta| + |S_{12}S_{21}|} > 1 \quad (2.16)$$

μ indicates the minimum distance between the origin of the Unit Smith Chart and the unstable region. As result, for $\mu>1$ the unstable region is outside the Smith Chart resulting in unconditional stability.

In contrast, the Rollet Factor can not give secure prediction about unconditional stability, thats why if we use the Rollet factor we need an auxiliary condition as such $|\Delta| < 1$ is sufficient and necessary for unconditional stability of a two-port.

Maximum Available Gain.

If we want to improve the k-factor we will have,as a result, a reduction of the maximum available gain (MAG). MAG can be calculated as:

$$MAG = G_{T_{MAX}|k \geq 1} = \left| \frac{S_{21}}{S_{12}} \right| \left(k - \sqrt{k^2 - 1} \right) \quad (2.17)$$

Maximum Stable Gain. (MSG)

This value is reached when the two-port approaches the boundary between unconditional and conditional stability ($k=1$), so the MAG tends towards its maximum stable value,

$$MSG = G_{T_{MAX}|k=1} = \left| \frac{S_{21}}{S_{12}} \right| \quad (2.18)$$

Power gain equations.

The **transducer power gain**, called G_T , is defined as the ratio of the power delivered to a load to the power available from the source. And the equation that allow us to find it is:

$$G_T = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{OUT}\Gamma_L|^2} \quad (2.19)$$

$$G_T = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_{IN}\Gamma_s|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad (2.20)$$

Where Γ_{OUT} and Γ_{IN} are:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (2.21)$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (2.22)$$

The **power gain** G_p is defined as the ratio of the power delivered to the load P_L to the input power to the network P_{IN} .

$$G_P = \frac{1}{1 - |\Gamma_{IN}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{22}\Gamma_L|^2} \quad (2.23)$$

The available power gain G_A is defined as the ratio of the power available from the network P_{AVN} to the power available from the source P_{AVS} . The power available from the network is the power delivered by the network to a conjugate matched load.

$$G_A = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|^2} |S_{21}|^2 \frac{1}{|1 - |\Gamma_{OUT}|^2} \quad (2.24)$$

Chapter 3

POWER AMPLIFIER DESIGN

In this chapter we proceed with the ADS design of the amplifier with two different transistors. This will help us to make a decision, which one will be used for implementation depending on the results that we will obtain.

The transistors to use in this design are ATF-521P8, from AVAGO and CGH55015F1/CGH55015P1, from CREE (we can see the transistor datasheets on the annex D)

3.1 Bias Point.

Once that we decided which transistor we are going to use, the next step that we have to follow in the amplifier design is to choose the bias point that will make our transistor work, this means that we have to find the V_{DS} and I_{DS} that will make the transistor work, in order to achieve our targets: high gain, good return losses for the desired bandwidth and good output power.

3.1.1 ATF-521P8 transistor.

As we can see on the transistor datasheet, the manufacturer give us for different V_{DS} and I_{DS} the S-parameters for different frequencies. So, we can make a theoretical estimation of the gain without the need of measuring it on the

transistor and like this know which voltage and current it will accomplish the targets that we have for the present project.

Previously we defined the transducer power gain (equations 2.19 and 2.20) and we should use it in order to find the gain value for the different S-parameters that the company gives us. Another option, and at the same time easier, is the use the equation that refers to the unilateral case.

We are in the unilateral case when $S_{12} = 0$; if we use equation (3.1) our transducer power gain would be:

$$G_{TU} = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_{IN}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad (3.1)$$

And we will have the maximum transducer power gain when:

$$\Gamma_s = S_{11}^*$$

$$\Gamma_L = S_{22}^*$$

$$G_{TU} = \frac{1 - |\Gamma_s|^2}{1 - |S_{11}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{1 - |S_{22}|^2} \quad (3.2)$$

If we check the S-Parameters at the central frequency, we can see that their values are not exactly zero, that is a necessary condition if we want to apply the unilateral case. However they are close to zero and we can use (equation 3.2) in order to obtain an approximation. We can see the results on Table 3.1.

Also we can evaluate the **Unilateral Figure of Merit**, U , at the design frequency (equation 3.3). It is a quick calculation that can be used to determine where this simplification can be made without significantly affecting the accuracy of the complete gain formula. If the relative gain ratio is near unity (typically, within 10 percent of unity), the two-port may be treated as unilateral, (equation 3.4).

$$U = \frac{|S_{11}S_{22}S_{12}S_{21}|}{\left| (1 - |S_{11}|^2)(1 - |S_{22}|^2) \right|} \quad (3.3)$$

$$\frac{1}{(1+U)^2} < \frac{G_T}{G_{TU}} < \frac{1}{(1-U)^2} \quad (3.4)$$

f=5.65GHz	a) V _{DS} = 4V I _{DS} = 200mA	b)V _{DS} = 4V I _{DS} = 200mA	a)V _{DS} = 4.5V I _{DS} = 200mA	b)V _{DS} = 4.5V I _{DS} = 200mA	V _{DS} = 4.5V I _{DS} = 120mA	a)V _{DS} = 3V I _{DS} = 200mA	b)V _{DS} = 3V I _{DS} = 200mA	V _{DS} = 4.5V I _{DS} = 280mA
S ₁₁	0.92	0.897	0.915	0.897	0.89	0.918	0.897	0.895
S ₁₂	0.059	0.061	0.059	0.061	0.06	0.061	0.065	0.058
S ₂₁	0.65	1.381	0.676	1.381	1.375	0.563	1.248	1.412
S ₂₂	0.66	0.584	0.657	0.584	0.569	0.703	0.667	0.543
G _{TUmax} (dB)	5.587	10.928	5.672	10.755	10.774	4.533	10.205	10.985

Table 3.1: S-parameters for a f=5.65GHz and maximum unilateral gain

Taking into account the previous table (assuming that these values are approximations), and the fact that we want around 10-15 dB gain, we should chose an V_{DS} = 4.5V and I_{DS} = 280mA. Note that some gain may be lost due to an increase in bandwidth.

The Unilateral Figure of Merit for the chosen bias point is represented on table 3.2. As we commented before we would need a ratio close to the unity, within 10 percent of unity; this is not the case, so we cannot use the unilateral approximation; but we used the unilateral results only as an approximation in order to see which one can give us a better gain result, but we are not going to use the unilateral design.

frequency	UFM_minus	U	UFM_plus
5.65 GHz	-2.176	0.285	2.910

Table 3.2: Unilateral Figure of Merit for ATF-521P8 transistor

Once we fix these two parameters, we only have to establish an appropriate V_{GS}, considering that we want an **AB class amplifier**. so we have to choose a value that is inside the active region, that is between the cut off and the saturation region, trying to place it in the middle point. This will allow to have the same dynamic range to arrive to the cut off region and saturation region.

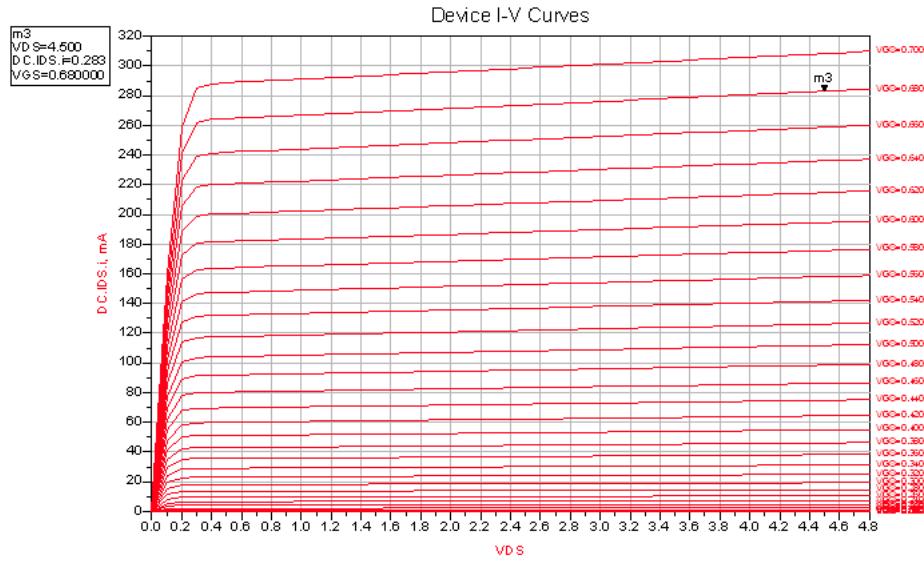


Figure 3.1: I-V Curves and bias point ATF-521P8 transistor.

If we examine Figure 3.1, the values that we finally chose are:

$$V_{DS} = 4.5V$$

$$I_{DS} = 280mA$$

$$V_{GS} = 0.68V$$

3.1.2 CGH55015F1/CGH55015P1 transistor.

For this transistor, the company gives us the S-parameters only for $V_{DS} = 28V$ and $I_{DS} = 115mA$.

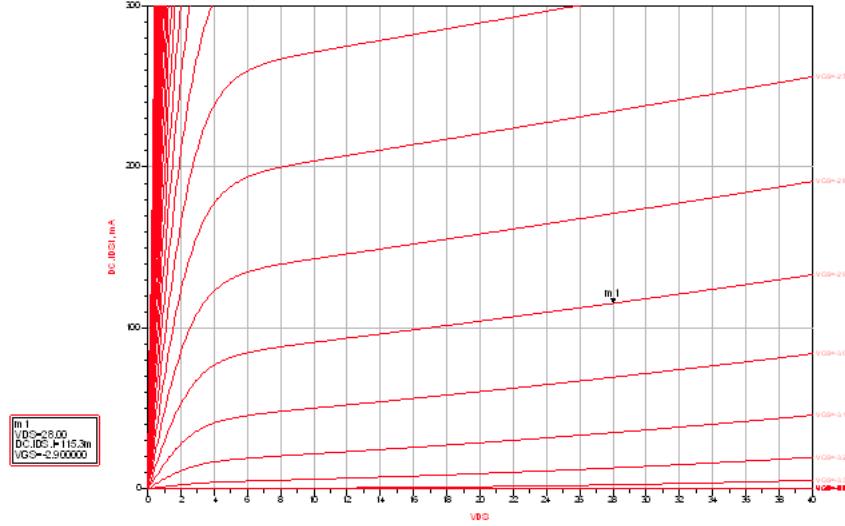


Figure 3.2: I-V Curves and bias point for CGH55015F1/CGH55015P1 transistor.

If we examine Figure 3.2, the values that we finally chose are:

$$V_{DS} = 28V$$

$$I_{DS} = 115mA$$

$$V_{GS} = -2.9V$$

We can check here the Unilateral Figure of Merit too, in order to see if we can make an unilateral design or not. Checking the results that are represented on table 3.3, we see that we can consider the unilateral case.

frequency	UFM_minus	U	UFM_plus
5.65 GHz	-0.880	0.107	0.979

Table 3.3: Unilateral Figure of Merit for CGH55015F1/CGH55015P1 transistor

3.2 Bias circuit.

In order for the transistor to operate properly we have to bias it correctly. Therefore, once that we chose the bias point and the feeding voltage, the next step is to design a bias network that allows the transistor to work in the desired

zone. There are two kinds of bias circuits, the active and passive circuits.

A **passive circuit** would be the one that is shown in *Figure 3.3*. But, with these kind of circuits we can have problems. For example, we know that the bias point depend on the temperature and the current that the transistor consumes; so if the transistor starts to consume more power or there is a temperature change, the bias point will change, therefore the transistor will not be properly fed and the circuit will stop working in the correct way.

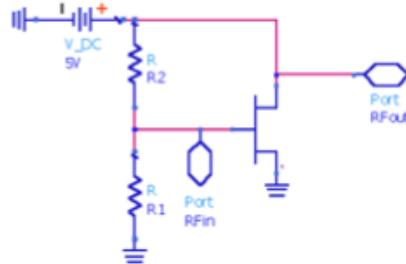


Figure 3.3: Passive polarization circuit

These circuits are not often used for RF applications because the biasing resistances also load the circuit and reduce the gain. Therefore, circuit techniques that permit use of a directly grounded source or emitter connection are preferred for high frequency amplifiers when implemented using discrete components on PC boards.

Another kind of biasing circuits are the **active circuits**, that can help preventing the problems that we just commented. The main advantage of an active biasing network is the ability to hold the drain to source current constant over a wide range of temperature variations.

3.2.1 ATF-521P8 transistor.

The one that we will use is the one that is illustrated on *Figure 3.4*. This biasing network is recommended by the manufacturer, and appears in the datasheet, so we decided to use this one.

We can see that on the network we have a current mirror composed by two PNP bipolar transistors. Due resistors R_2 and R_4 , the circuit doesn't act as a current mirror, but if the voltage that drops across the two resistors is kept identical, then it still displays some characteristics of a current mirror. The transistor Q_2 acts as a PN junction cause the base and the collector are tied together. This transistor helps temperature compensate the Emitter-Base junction of Q_1 .

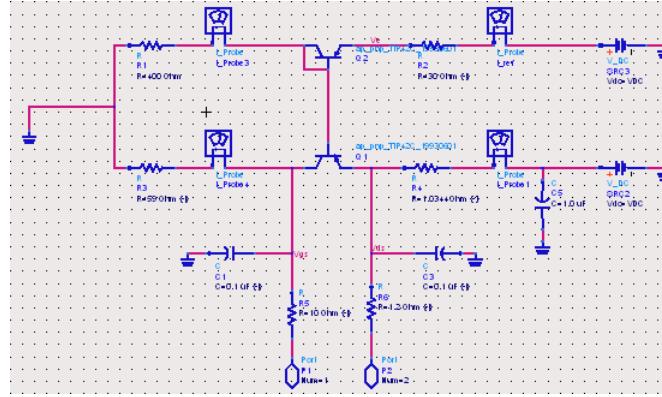


Figure 3.4: Active polarization circuit

Now we have to calculate the values of R_1 , R_2 , R_3 and R_4 . In order to find these values we have to take into account some considerations:

- I_{DS} is the device drain-to-source current. $I_{DS} = 280mA$.
- I_R is the reference current for the active bias. $I_R = 10mA = I_{C,1} = 10I_G$
- V_{dd} is the power supply voltage available. $V_{dd} = 5V$.
- V_{DS} is the device drain-to-source voltage. $V_{DS} = 4.5V$.

- V_g is the gate bias. $V_g = 0.68V$.
- V_{be1} is the Base-Emitter turn on voltage for Q_1 and Q_2 .

Following this considerations we calculate the R_4 value, that sets the desired device drain current.

$$R_4 = \frac{V_{dd} - V_{DS}}{I_{DS} + I_{C,1}} = 1.72413\Omega$$

We have to take into account that the voltage drop across R_2 must be equal to the voltage drop across R_4 but with a current I_R .

$$R_2 = \frac{V_{dd} - V_{DS}}{I_R} = 50\Omega$$

R_1 sets the bias current through Q_2 .

$$R_1 = \frac{V_{DS} - V_{be1}}{I_R} = 377.636\Omega$$

and R_3 sets the gate voltage for our amplifier.

$$R_3 = \frac{V_g}{I_{C,1}} = 69.366\Omega$$

Hence, by forcing the emitter voltage of Q_2 to be equal to V_{DS} , this circuit regulates the drain current similar to a current mirror; as long as Q_1 operates in the forward active mode, this statement is true. The collector-base junction of Q_1 must be kept reversed biased.

We have to observe that the theoretical values and the ones that appear on the network are different because we did some tuning in order to obtain accurate values. In addition we have to take into account the resistor values, setting them to commercial values, in case that we want to make the design on a PCB.

3.2.2 CGH55015F1/CGH55015P1 transistor.

For this transistor, we will not have bias network, we are going to connect directly the voltage we need in order to feed the transistor.

We want to guarantee that the voltage remains constant so we will use capacitors that have high values, because the highest the capacitance, the more energy can storage, and consequently we can control better the voltage differences that can appear, and try to maintain the voltage constant.

3.3 Stability study.

After finding out the bias point and the biasing network we proceed to make a stability study for both transistors. In order to find the stability we have to follow the subsection 3.2.1 (Amplifier Stability).

3.3.1 ATF-521P8 transistor.

In order to check the stability we are going to use the Rollet Factor, we can see the results on *Figure 3.5*. If we sweep over a range of frequencies, we can see that our transistor will be stable above 1.85 GHz; because k is higher than 1 after this frequency, and $\Delta < 1$ for all the analyzed frequencies.

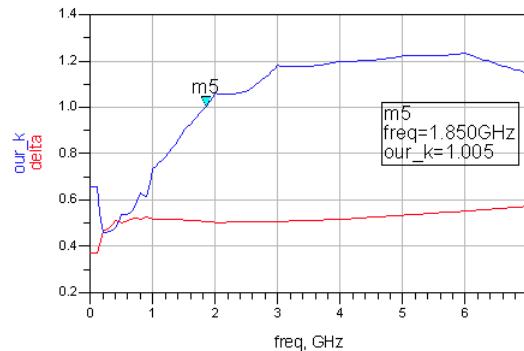


Figure 3.5: Rollet Factor for ATF-521P8 transistor.

Also we plot MSG (the Maximum stable gain) and the intrinsic transducer gain (GTi) with both Γ_S and $\Gamma_L = 0$ (Figure 3.6). In the regions where $K < 1$, the max_gain function plots MSG. When unconditionally stable, it plots MAG.

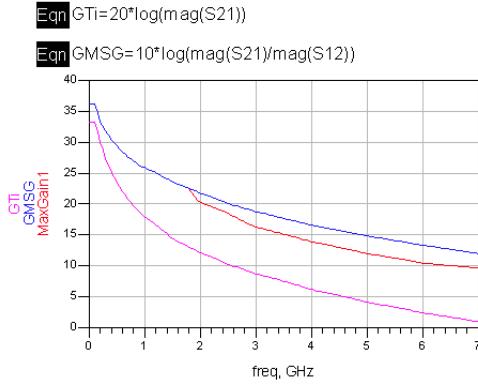


Figure 3.6: GTi, GMSG and MAG for ATF-521P8 transistor.

If we would have instability on the desired frequency, there exist different ways to solve the problem, as introducing a resistor between drain and source, but we would lose bandwidth. Also we can put a resistor connected to the ground on the amplifier input, between the input matching network and the transistor gate, which will help to stabilize the network but we will lose bandwidth.

3.3.2 CGH55015F1/CGH55015P1 transistor.

For this amplifier we follow the same steps that we followed for the ATF-521P8 transistor.

If we check *Figure 3.7*, we see that our amplifier is stable for frequencies higher than 3.75GHz, so for our central frequency the amplifier will be stable due to $k > 1$ and Δ always smaller than 1.

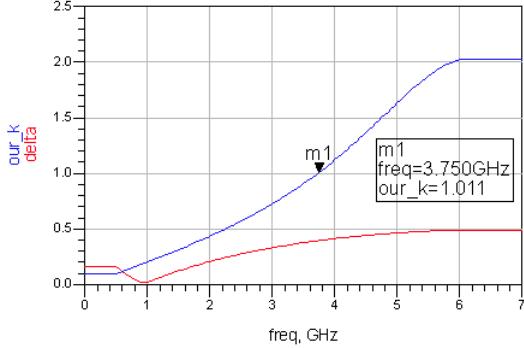


Figure 3.7: Rollet Factor for CGH55015F1/CGH55015P1 transistor.

Finally, we are going to represent MSG and the intrinsic transducer gain (GTi) for this transistor. The results are illustrated in *Figure 3.7*. We can observe that in the regions where $K < 1$, (ie. for frequencies bellow 3.75 GHz), the max_gain function plots MSG. When it is unconditionally stable, after 3.75 GHz it plots MAG.

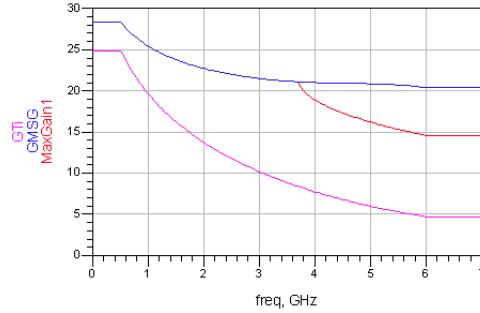


Figure 3.8: GTi, GMSG and MAG for CGH55015F1/CGH55015P1 transistor.

3.4 Input and Output Matching Networks.

The next step in order to continue with our amplifier design is to design a input and output matching network. The matching networks allow us to match the input and output from the transistor to the desired reflexion coefficients, in order to achieve our targets. The matching networks can be designed with discrete

components, that are reactive so they do not include resistors only lumped elements and capacitors; or with transmission lines. At high frequencies is better to use transmission lines, because the values from the discrete values that we would need to use would be difficult to find in practice. We can see a diagram in *Figure 3.9*.

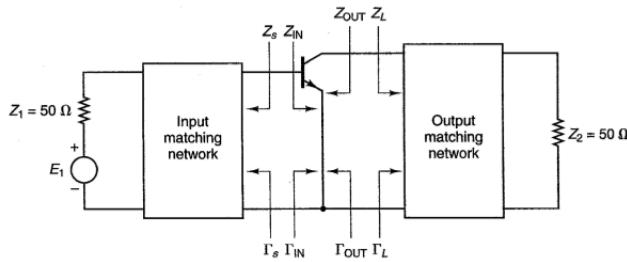


Figure 3.9: Matching network.

The matching network can be designed following different procedures, as a matching network for the stability, for the gain or for the noise. Also we can match for a specific source and load impedance. We will take into account the last case because in order to take measurements on the laboratory the equipment has 50Ω as characteristic impedance, but we will choose a design procedure in order to obtain good gain, low return losses and high output power, always taking into account stability.

The next step in the simulation is the design of the matching networks. The idea of the matching networks is to match the arbitrary impedance from the generator to known impedance at the load. When the impedances of the transistor are matched to load, it will be much convenient to match it to a bigger system since all the components will be matched to the same impedances. There are several ways to design the matching networks. The simplest technique is to use the lumped circuit elements. Another method is to use microstrip line

either single-stub or double-stub matching technique.

I have chosen to use microstrip line over the lumped circuit element matching because of the easy of implementation of the actual circuit on the board. As mentioned earlier, there are two types of matching for microstrip line matching: single-stub and double- stub matching. For such matching technique, the conventional way is to use the Smith Chart. However, ADS conveniently provides smith chart utility tool that could be used to match the arbitrary source to any load with various components that could be placed on the schematic.

In addition, this matching technique is reasonably stable and furthermore it provides ease of tuning after the circuit is built. This is because the open circuit is easier to implement on the actual circuit board and the split of stub into two will shorten the length of the stub, which would eventually take up less space on the board.

With this method we had a problem, we couldn't obtain a good bandwidth so we tried to design the input and output network with Chebishev $\lambda/4$ transformers and a stub, in order to delete the imaginary part of the impedance that we see from the transistor input and from the output.

In order to explain how the Chebishev $\lambda/4$ transformers work, first we have to explain how a $\lambda/4$ *transformers* works.

A transmission line that is terminated in some impedance, Z_L , that is different from the characteristic impedance, Z_0 , will result in a wave being reflected from the termination back to the source. At the input to the line the reflected voltage adds to the incident voltage and the reflected current subtracts (because the wave is traveling in the opposite direction) from the incident current (we can see it in the figure 3.10). The result is that the input impedance of the line (ratio of voltage to current) differs from the characteristic impedance and for a line of length d is given by:

$$Z_{IN}(d) = \frac{V(d)}{I(d)} = Z_0 \frac{Z_L + jZ_0 \tan(\beta d)}{Z_0 + jZ_L \tan(\beta d)} \quad (3.5)$$

An important property of a transmission line is the ability of the transmission line to change a load impedance to another value of impedance at its input.

In order to have a quarter-wave transmission line we have a line length of $d = \lambda/4$, and it will give us an input impedance:

$$Z_{IN}(\lambda/4) = \frac{Z_0^2}{Z_L} \quad (3.6)$$

Equation 3.6 shows that if we want to transform a real impedance Z_L to another real impedance given by $Z_{IN}(\lambda/4)$, a quarter-wave line with real characteristic impedance of value $Z_o = \sqrt{Z_{IN}(\lambda/4)Z_L}$ can be used.

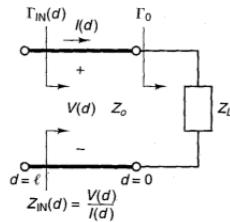


Figure 3.10: Input impedance of the transmission line at any position d.

Once we know the purpose of the $\lambda/4$ transformers, we continue with explaining the *Chebyshev multisection quarter-wave transformers*.

We consider an N-section impedance transformer connected between a transmission line of characteristic impedance of Z_0 and load R_L , we can see it on *Figure 3.11*. The length of every section is the same, but the characteristic impedances are different.

We need a systematic method to determine the location of each zero for a maximum permissible reflection coefficient, ρ_M , and the number of quarter-wave sections, N. In order to have the magnitudes of all minor lobes in the passband equal, section reflection coefficients are determined by the characteristics of Chebyshev functions.

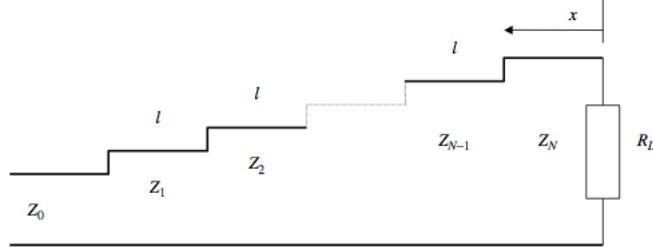


Figure 3.11: N-section impedance transformer.

These functions satisfy the following differential equation:

$$(1 - x^2) \frac{d^2 T_m(x)}{dx^2} - x \frac{dT_m(x)}{dx} + m^2 T_m(x) = 0 \quad (3.7)$$

Chebyshev functions of degree m , represented by $T_m(x)$, are m th-degree polynomials that satisfy equation 3.7. The first four of these and a recurrence relation for higher-order Chebyshev polynomials are given as:

$$T_m(x) = \begin{cases} \cos(m \cos^{-1} x) & -1 \leq x \leq 1 \\ \cosh(m \cosh^{-1} x) & x \geq 1 \\ (-1)^m \cosh(m \cosh^{-1} |x|) & x \leq -1 \end{cases} \quad (3.8)$$

The characteristics of Chebyshev polynomials are utilized to design an impedance transformer that has ripples of equal magnitude in its passband. The number of quarter-wave sections determines the order of Chebyshev polynomials. With x_0 properly selected (equation 3.10), $|T_m(x)|$ corresponds precisely to $\rho(\beta l)$. We obtain this by linking βl to x of Chebyshev polynomial: $x = x_0 \cos(\beta l)$, it is to be noted that Chebyshev variable x and angle φ on the complex w -plane are related through that equation because φ is equal to $-2\beta l$.

For a m -section impedance transformer we have the following relation, where ρ_M is the maximum allowed reflection coefficient in the passband.

$$T_m(x_0) = \left| \frac{R_L - Z_0}{R_L + Z_0} \right| \frac{1}{\rho_M} \quad (3.9)$$

So, using equation 3.8 we can locate the value of x_0 as:

$$x_0 = \cosh \left[\frac{1}{m} \cosh^{-1} T_m(x_0) \right] \quad (3.10)$$

Once that we have the x_0 value, zeros of the reflection coefficient are the same as those of $T_m(x)$. Since Chebyshev polynomials have zeros in the range $-1 < x < 1$, zeros of $\rho(\varphi)$ can be determined from 3.8. Hence, we have the equation 3.11 and 3.12 where x_n is the location of the nth zero.

$$T_m(x_0) = 0 \Rightarrow x_n = \pm \cos \left[(2n - 1) \frac{\pi}{2m} \right] \quad (3.11)$$

$$\varphi_n = 2 \cos^{-1} \frac{x_n}{x_0} \quad (3.12)$$

The zeros of $\rho(\varphi), w_n$, on the complex w-plane are now known because $w_n = e^{i\varphi_n}$. After that, we obtain with this the reflections coefficients Γ_n and therefore we obtain Z_n values for the transmission lines.

$$\Gamma_N = \frac{Z_{n+1} - Z_n}{Z_{n+1} + Z_n} \Rightarrow Z_n = \frac{1 - \Gamma_N}{1 + \Gamma_N} Z_{n+1}$$

In order to do the previous calculations for the input and output network i have written a Matlab Script that appear in the Annex A.

We followed the same steps in order to design the input and output network for both transistors, so we will describe the process generally and after that we will check the values that we obtain for each transmission line, the s-parameters.

3.4.1 Input Network.

With the transistor we have to find the input impedance. In addition we want a maximum transfer of power from the generator to the load, and for this reason the load has to be conjugated matched to the generator, that is $Z_L = Z_{th}^*$.

We want to transform this impedance value to 50 Ohms. The input impedance will have real and imaginary part, so the first thing that we have to do is to place a stub (short circuited stub, open circuited stub or radial stub), in order to eliminate the imaginary part.

We decided to use a radial stub. A radial stub is an open-circuit stub realized in radial transmission line instead of straight transmission line. It is a very useful element, primarily for providing a clean broadband short circuit, with no spurious resonances, much broader than a simple open-circuit stub. It is especially useful on bias lines in high-frequency amplifiers and similar components. Radial stubs are used almost exclusively in microstrip circuits. Although radial stubs are shorter than uniform stubs, they cannot be folded or bent; therefore they take up a lot of substrate area. For this reason radial stubs are used primarily at high frequencies, where they are relatively small.

After placing the stub, we will have a different input impedance with only real part. So, now it is when we are going to use the *Chebyshev multisection quarter-wave transformers*, in order to arrive to the 50 Ohms impedance. When increasing the number of transmission lines the bandwidth increases.

We decided finally to design our matching network with microstrip lines. Microstrip are transmission lines that are composed by a metallic track over a dielectric subtract, (see Annex B for characterization), that has a ground plane on the other side. This kind of lines have a disadvantage, due to the metallic track is touching from one side the air and from the other side the dielectric, resulting in different waves velocity that can cause problems. This problem can be solved by using striplines, which the metallic track is surrounded by the dielectric. At first, we don't think that this effect would produce problems and we decided to use microstrip. The microstrip lines are characterized by their width, W, and their length, L. The width is determined by the dielectric substrate and the characteristic impedance of the line, and the length depends on the matching or the results that we want to achieve.

3.4.1.1 ATF-521P8 transistor.

Now we can see the input matching network for the ATF-521P8 transistor and the S-parameters that we obtain.

The actual value of the length and width of the microstrip can be easily determined using a special program called LineCalc. This feature will calculate the length and the width of microstrip line with respect to the given material relative dielectric, height of the dielectric material, the cutoff or the operating frequency, and the characteristic impedance of the microstrip.

Since we have a *Chebyshev multisection quarter-wave transformers (N=3)* we don't have the same impedances on the transmission lines, so we have to find out these impedance values, and we obtain them with the Script that I mention before. Having the impedance values we will use the LineCalc tool in order to find the width and the length of the lines, due that we have that their electrical lenght are 90°. The results are the following:

	TL2	TL3	TL4	Stub1
W (mm)	0.707632	0.323596	0.143544	0.55625
L (mm)	7.95326	8.15188	8.28069	3.25
Angle 65.1°				

Table 3.4: W and L, input network ATF-521P8 transistor.

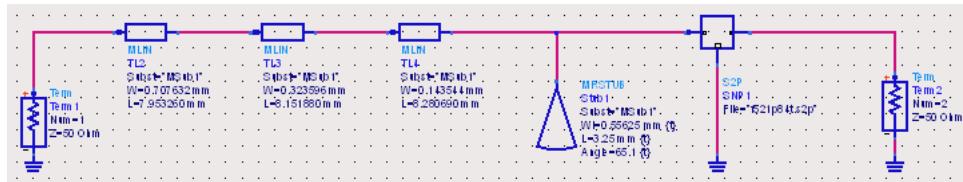


Figure 3.12: Input Matching network ATF-521P8 transistor.

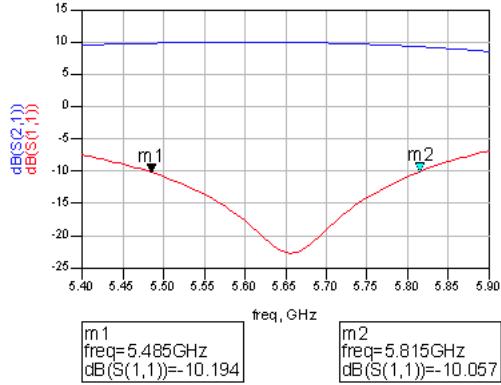


Figure 3.13: S-parameters for the Input Matching network ATF-521P8 transistor.

In the S-parameters results indicate that we are obtaining the desired targets. The $|S_{11}|$ is the return losses, and we wanted that our return losses had -10dB and a bandwidth at least of 200 MHz; we can see from the theoretical result that we obtain a 300 MHz bandwidth. Also we wanted a 15 dB gain, and obtained 10 dB. This is associated with the $|S_{21}|$ parameter.

3.4.1.2 CGH55015F1/CGH55015P1 transistor.

For this transistor we use the same steps in order to design the input network. The first thing that we have to calculate is the input impedance of the transistor. Once we find this impedance we have to transform it to 50 Ohms, and obtain matching.

The impedance that we have at the input of our transistor in our central frequency is $13.983+j7.597$ Ohms and we have to achieve 50 Ohms. First, we have to make conjugate matching in order to obtain the maximum transfer of power.

In order to have matching we are going to use the *Chebyshev multisection quarter-wave transformers N=2*, and we can calculate the impedances with the script and after that we can use LineCalc to find out the width and the length

of the lines. We have the input matching network in *Figure 3.14* also we see in *table 3.5* the value of the transmission lines and the stub that we use.

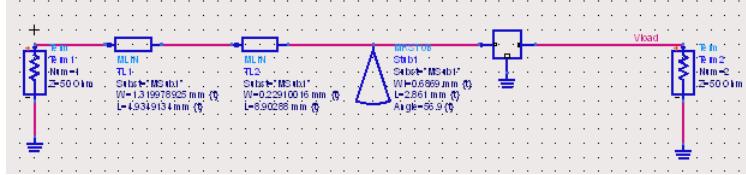


Figure 3.14: Input Matching network CGH55015F1/CGH55015P1 transistor.

	TL1	TL2	Stub
W (mm)	1.319978925	0.22910016	0.6869
L (mm)	4.9349134	8.5087072	2.861
Angle 56.9°			

Table 3.5: W and L, input network CGH55015F1/CGH55015P1 transistor.

Now in *Figure 3.15* we can see the results that we obtain from the input network simulation.

In *Figure 3.15* the S-parameters results show us that we obtain the desired targets. The $|S_{11}|$ is the return losses, and we wanted that our return losses is below -10dB and a bandwidth at least of 200 MHz; we can see that we obtain 218 MHz bandwidth. If we try to increase the BW adding more sections at *Chebyshev multisection quarter-wave transformers* the results don't suffer enough changes to increase it. Also we wanted a 15 dB gain, and obtained 12 dB, (see the $|S_{21}|$ parameter).

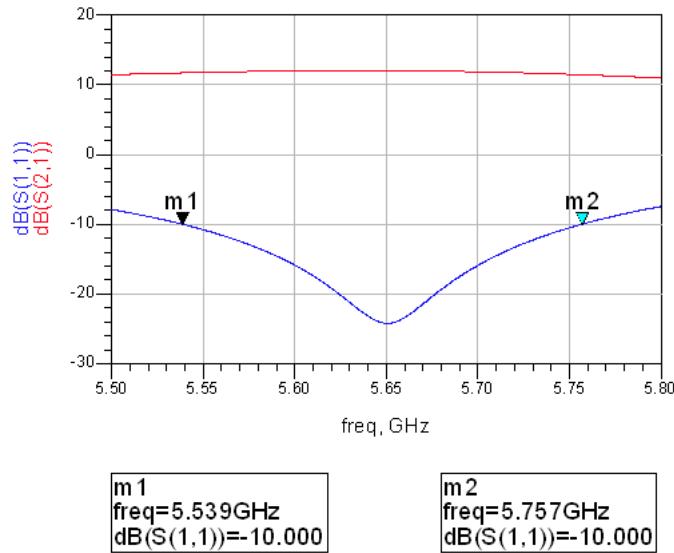


Figure 3.15: S-parameters for the Input Matching network CGH55015F1/CGH55015P1 transistor.

In *Figure 3.16* is illustrated the result of the impedance matching. The impedance before (blue line) and after (red line) the input matching network. The normalized impedance value after introducing the input matching network is close to 1 in the Smith Chart representation for the desired bandwidth.

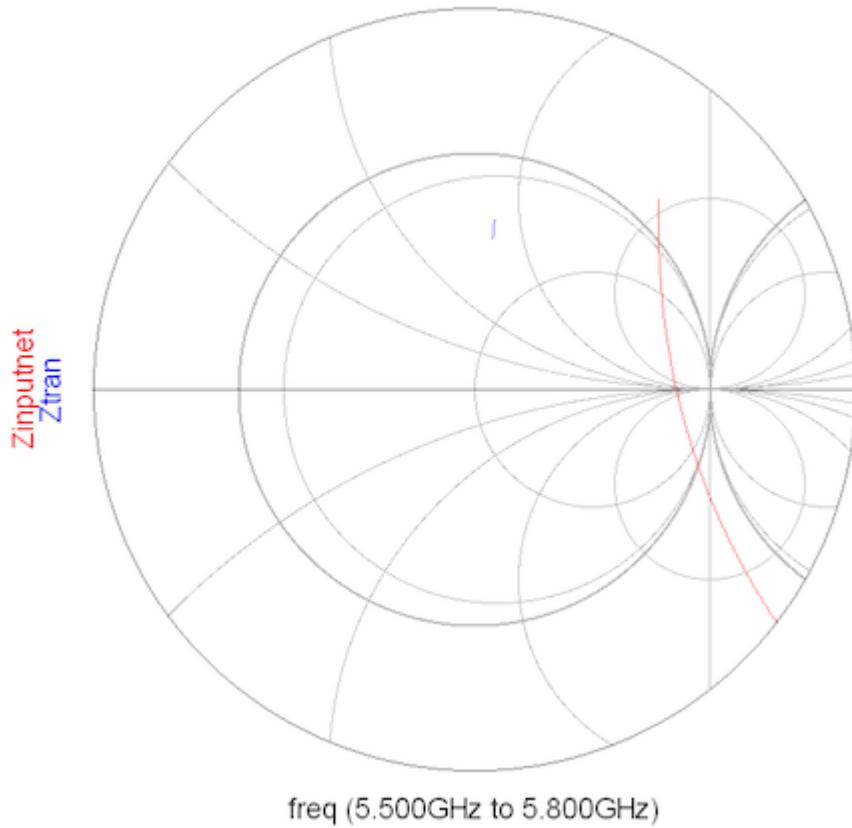


Figure 3.16: Normalized Impedance before and after the Input Matching network CGH55015F1/CGH55015P1 transistor.

3.4.2 Output Network.

3.4.2.1 ATF-521P8 transistor.

In order to design the output network, we have to obtain the impedance that we see from our output of the transistor. Once that we have this impedance we have to match it to 50 Ohms, this we will manage, as the input matching, using a radial stub and *Chebyshev multisection quarter-wave transformers with N=3*. We can see the results for the impedance, the width and the length of the lines in *Table 3.6*; and the output circuit in *Figure 3.17*.

	TL6	TL7	TL8	Stub1
W (mm)	1.048865	2.12644	1.5191	0.3125
L (mm)	4.9509172	7.6138	7.738010	0.2095
Angle 24°				

Table 3.6: W and L, output network ATF-521P8 transistor.

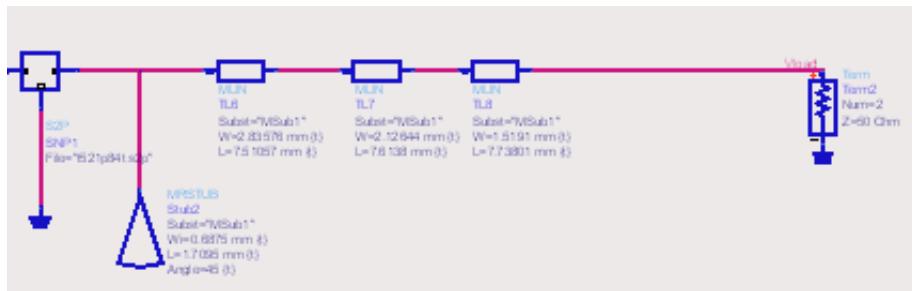


Figure 3.17: Output Matching network ATF-521P8 transistor.

As we see in *Figure 3.18* our central frequency has suffer changes. This happens because we cannot control the real behavior of the transmission lines, the inductor and capacitor behavior that are related to them.

In order to have our central frequency we have to do some optimization, so we have to use the tuning tool that ADS provide us. We can see the results in *Figure 3.18*. The results that we obtain are the results for the input and output network, them represent the results for the final design network. After that we have to introduce the decoupling network and see which will be the results and check if we need some optimization or not.

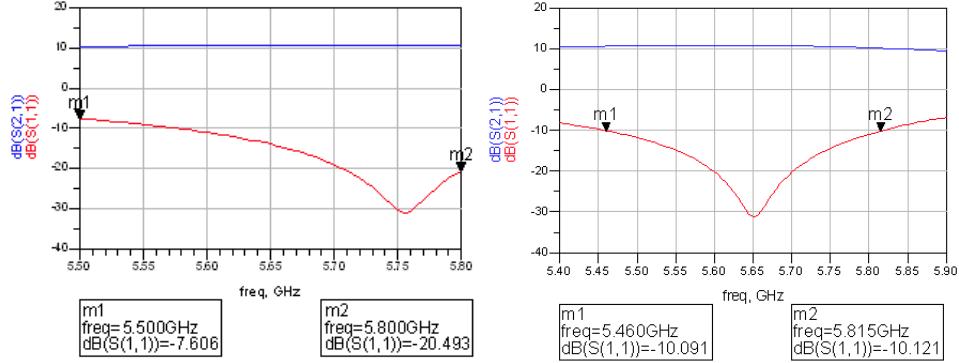


Figure 3.18: S-parameters for the Input and Output Matching network ATF-521P8 transistor.

As we can see in *Figure 3.18* we obtain 10 dB gain and for a 355 MHz bandwidth the return losses are less than -10 dB, so we accomplish the target related with the bandwidth.

3.4.2.2 CGH55015F1/CGH55015P1 transistor.

After the design of our input matching network we have to proceed with the design of the output network.

The first thing that we have to check is the impedance that we see from the output of the transistor, once that we have this impedance we place a radial stub in order to eliminate the imaginary part of this impedance. After that, we design a *Chebyshev multisection quarter-wave transformers (N=3)* in order to maintain the bandwidth. In *table 3.7* we have final results of the transmission lines after do some optimization from the input network that we can see at *Figure 3.19*.

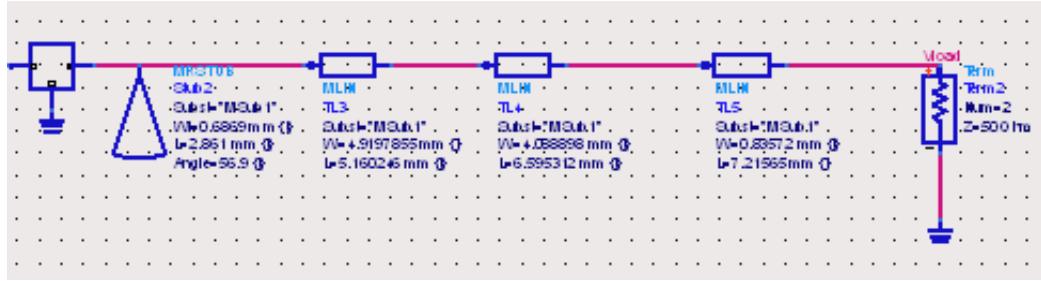


Figure 3.19: Output Matching network for CGH55015F1/CGH55015P1 transistor.

	TL3	TL4	TL5	Stub1
W (mm)	4.9197855	4.0888098	0.83572	0.6869
L (mm)	5.160246	6.595312	7.21565	2.861
Angle 56.9°				

Table 3.7: W and L, output network for CGH55015F1/CGH55015P1 transistor.

In *Figure 3.19* we have the S-parameters results that show us that we accomplish the desired targets. The $|S_{11}|$ is the return losses, and we wanted that to be below -10dB. The request bandwidth of at least 200 MHz; we obtain 208 MHz bandwidth. Also we wanted a 15 dB gain, and obtained 13 dB, we can see it if we check the $|S_{21}|$ parameter.

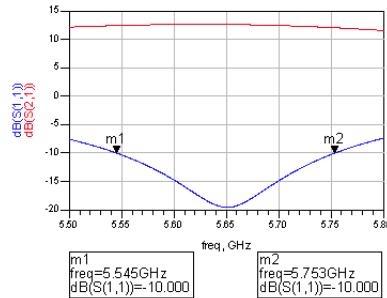


Figure 3.20: S-parameters for the Output Matching network CGH55015F1/CGH55015P1 transistor.

3.5 Decoupling Network between the RF signal and the DC signal.

When we design a RF amplifier we have to take into account that it doesn't use only RF signals, also it works with DC, that is part of the circuit feeding. This situation generates problems, because we don't want to have interferences between them. First of all, we cannot let that DC signal flows across the RF circuit, because it could affect the circuits that are connected with our circuit. On the other hand, we cannot let the RF signal goes to the DC, because it could propagate across the feeding cables and due to their lengths they would act as antennas and they would be radiating, so they would be affecting RF equipment that would be close enough to the circuit.

In order to avoid these problems we have some available solutions. We should take into account that capacitors at high frequencies act as a short-circuit, so it lets pass across it the RF signal; at low frequencies it acts as open circuit and doesn't let the DC signal pass across it. In general, this is the reason that at the input and output of a radio frequency amplifier we have decoupling capacitors, which function is to avoid the DC signal going through to the RF circuit.

The other decoupling elements that we need, we can find them in the junction between feeding and the transistor, where we have an inductor in series working as short circuit at low frequencies letting pass the DC signal, whereas at high frequencies it works as open circuit and doesn't let pass the RF signal to the feeding cables.

In order to have a stronger decoupling, we should have capacitors connecting to ground, like this if the RF signal pass across the decoupling inductors, it will arrive to the capacitor, that will let pass the RF signal, that will go to ground. In order to do the simulation, at the beginning we use the real inductors and capacitors that ADS provide use, after that we will decide which transistor are going to use, depending on the Output Power that they will provide us, so in

our final circuit we will have to change the capacitors and inductors that we used for the decoupling network for real components.

3.5.1 ATF-521P8 transistor.

We can see our final network in *Figure 3.21*

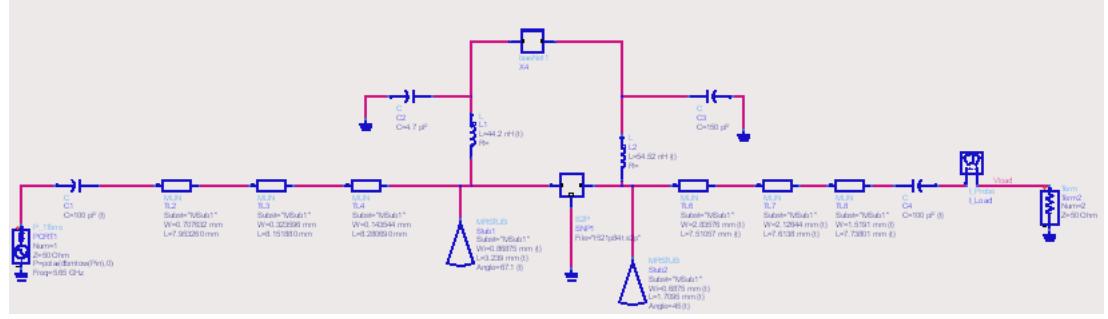


Figure 3.21: Final network ATF-521P8 transistor, with bias network, input and output matching network and decoupling network between DC and RF.

The decoupling capacitors at the input and the output network will result in our central frequency so we have to do some optimization, we can see the final results in *Figure 3.22*. We can see that we obtain almost a flat gain with 10 dB gain (S_{21}), also we can see that out return losses (S_{11}) are under -10 dB with a bandwidth of 350 MHz, also in the figure appear the reflection coefficient at the output (S_{22}) that is under -10 dB during all the bandwidth, that's means that we have a good output matching.

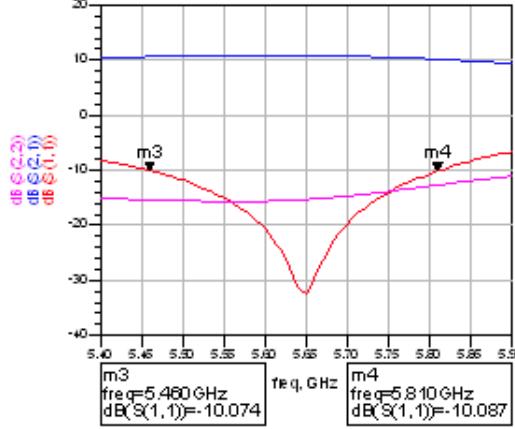


Figure 3.22: Final results for ATF-521P8 transistor, with bias network, input and output matching network and decoupling network between DC and RF.

Now we have to check if the amplifier is stable. In Section 3.3 we show that our transistor was unconditionally stable at our desired frequency, so no matter which will be the input and output matching network, the amplifier should continue being stable. The results are represented in *Figure 3.23* and we can check that the designed amplifier continues being unconditionally stable, because $K>1$ and $\Delta<1$ in our frequency range.

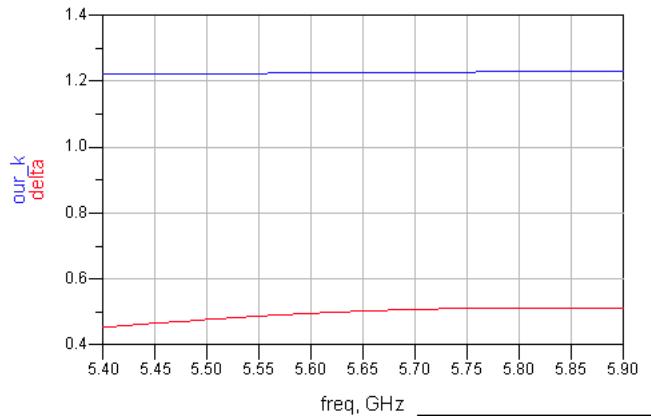


Figure 3.23: Stability for ATF-521P8 transistor using Rollet Factor

It is also important that we characterize the isolation, which is related with the $|S_{12}|$. It would be equivalent to introduce the input through the output and take measurements at the input. We can see the results in *Figure 3.24*. As we see we obtain good isolation, always under -15 dB.

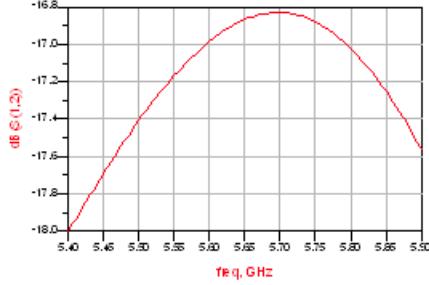


Figure 3.24: Isolation simulation for ATF-521P8.

Another parameter that we can measure is the noise factor NF. As we said noise it is not a critical factor for the transistor that is designed as a transmitter system. But we can see in *Figure 3.25*, the noise that our amplifier dispels at the output. We can see that it is quite small, under 4 dB.

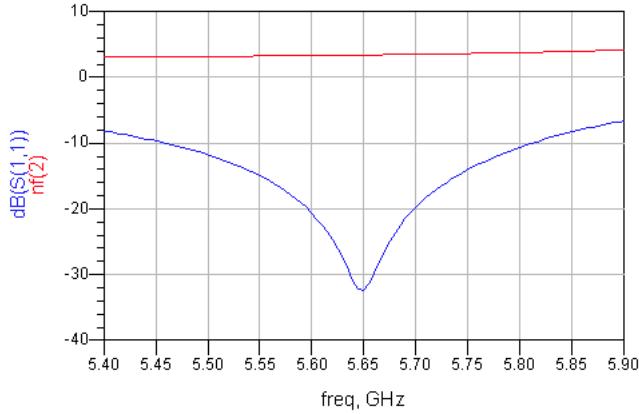


Figure 3.25: Noise for ATF-521P8.

We can also find the PAE (Power Added efficiency). As we commented at *Section 3.3* PAE is a measure of the power conversion efficiency of power

amplifiers. We can see the results in *Figure 3.26*. The results show us that between linear and saturation regions we have a zone that the amplifier is most efficient. We can see that for our amplifier it is between 14 and 24 dBm input power, and it is true because our transistor, as we will see now will have 1-dB compression point at 14.8 dBm.

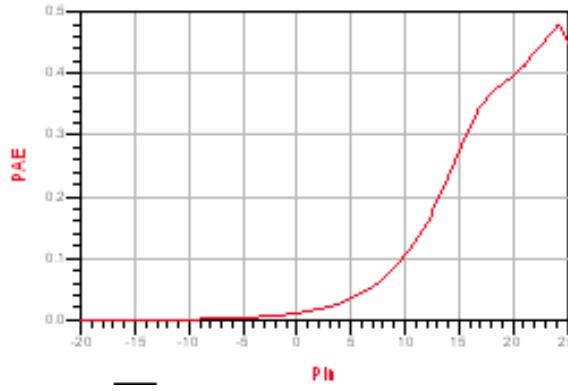


Figure 3.26: PAE ATF-521P8 transistor.

We proceed to calculate the output power from the network. In order to understand the output power we should reference to *Section 2.1.3*. We can see the results in *Figure 3.27*.

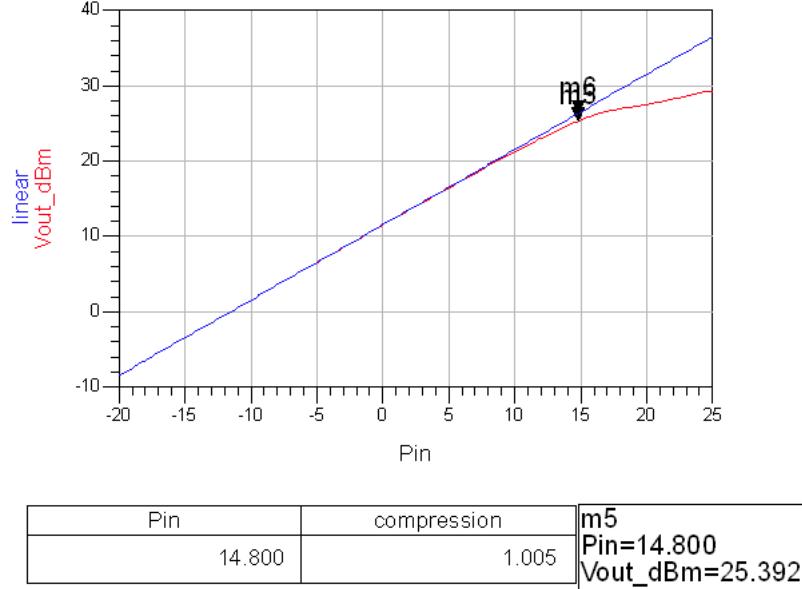


Figure 3.27: Output Power for ATF-521P8.

As we see in *Figure 3.27* the output power related with the input power is a straight line, if the amplifier gives at the output a proportional power that we have at the input, This proportional value would be the amplifier gain. But in our real amplifier it doesn't happens. We can see that there is a zone where we have a lineal behavior. This happens when we have small power levels, but after a certain point the amplifier will be at the saturation zone and stops to amplifier the input power. In our figure we can see that the gain suffers compression at high power.

In our amplifier this situation happens when that $\text{Pin} = 14.8 \text{ dBm}$ and we obtain $\text{Pout} = 25.392 \text{ dBm}$.

When the amplifiers start to be at the saturation zone, they start to have a non linear behavior, that are translated as spurious at the output. If we apply just one tone as input signal, this non linear behavior introduce harmonic

distortion. This means that at the output we have harmonics from the input signal generated by the amplifier. This harmonic distortion is not such a big problem cause it is not close to the desired signal, and it can be suppress using a band pass filter or high pass filter that would be connected at the output.

The non linear behavior of an amplifier not only generates harmonics, depending the input signal, it can appear spurious inside the passband that we cannot delete them using filters.

One way to quantify the distortion consist on the third intermodulation distortion with two tones, IP3.

IP3 is defined as the point where the theoretical lines from the util signal power intersects with the intermodulation power. It is the amplitude value from input signal should has in order that at the output, the third order term has the same amplitude as the desired signal. The bigger the IP3 value, the most linear our transistor will be.

If we introduce at the amplifier input a signal composed by two synodal tones with really close frequencies, at the output we will have different harmonics and spurious. It is supposed that with a band pass filters we can delete most of them, but we will not be able to delete the rest, this are the ones that correspond with the cubic power of the input signal, that are the ones related with the third order harmonic distortion.

Also the amplitude of this term grows with the cubic power of the input signal amplitude.

ADS has a tool that lets us find the IP3 point at the output. Using it for our amplifier, the result is:

$$IP3 = 31.802 dBm$$

A rule-of-thumb that holds for many linear radio frequency amplifiers is that the 1 dB compression point falls approximately 10 dB below the third-order intercept point. As we can see in our amplifier the difference between them is

6.41 dBm, so we will have some interference between our desired output signal and the third order intermodulation.

3.5.2 CGH55015F1/CGH55015P1 transistor.

The final network for this transistor is represented in *Figure 3.28*

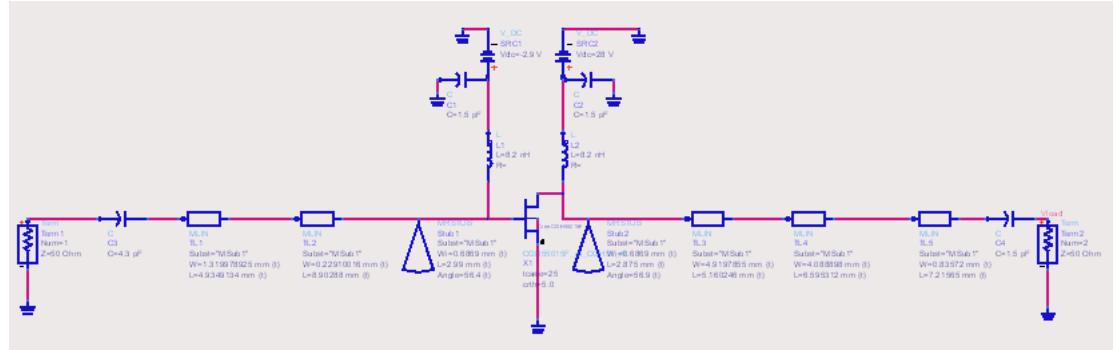
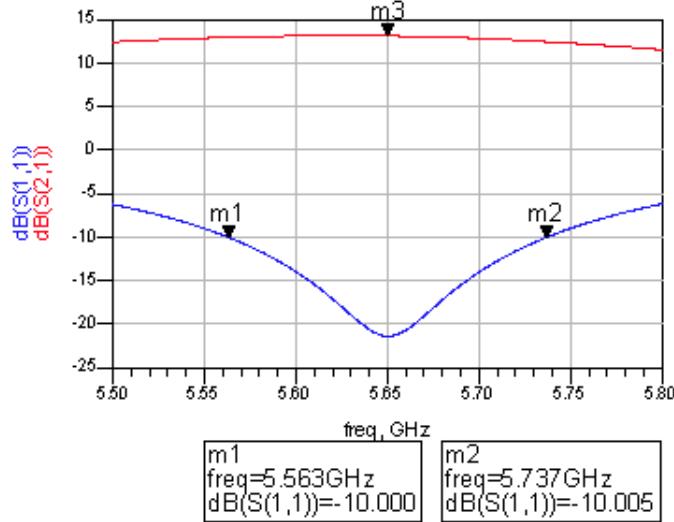


Figure 3.28: Final network CGH55015F1/CGH55015P1 transistor, input and output matching network and decoupling network between DC and RF.

We have to do some optimization, because the decoupling capacitors, being real capacitors with parasitic, make the central frequency changes a little bit. We can see the final results in *Figure 3.29*. We can see that we obtain almost a flat gain with 13 dB gain (S_{21}), also we can see that out return losses (S_{11}) are under -10 dB with a bandwidth of 174 MHz.



Now we have to check our amplifier stability. As we see in Section 3.3 our transistor was unconditionally stable at our desired frequency, so the input and output matching network will not change this situation and the amplifier should continue being stable. The results are represented in *Figure 3.30* and we can check that at our frequency range the designed amplifier continues being unconditionally stable, because $K > 1$ and $\Delta < 1$ in our frequency range.

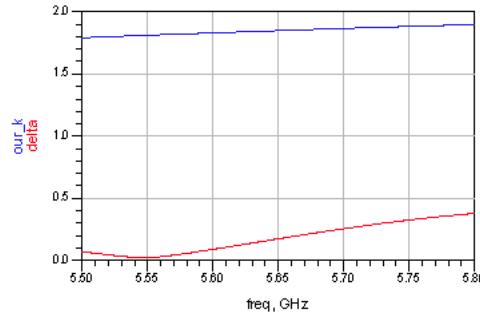


Figure 3.30: Stability for CGH55015F1/CGH55015P1 transistor using Rollet Factor

It is also important that we characterize the isolation. As we show with the other transistor this data is related with the $|S_{12}|$ and it would be equivalent to introducing the input through the output and take measurements at the input. We can see the results in *Figure 3.31*. As we see we obtain good isolation, always under around -28dB.



Figure 3.31: Isolation simulation for CGH55015F1/CGH55015P1 transistor.

Another parameter that we can measure is the noise factor NF, but CREE didn't give enough information about noise. Noise it is not a critical factor for the transistor that is designed as a transmitter system.

We can find PAE (Power Added efficiency) for this transistor too. PAE is a measure of the power conversion efficiency of power amplifiers. We can see the results in *Figure 3.32*. The results show that between linear and saturation regions we have a zone that the amplifier is most efficient. We can see that for our amplifier it is between 20 and 25 dBm input power, and it is true because our transistor has a 1-dB compression point at 21 dBm.

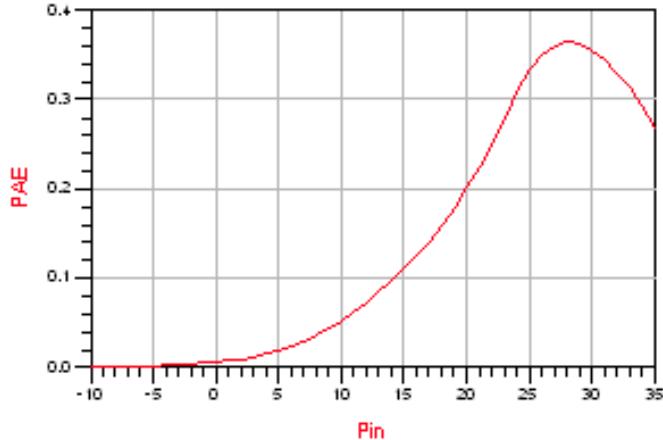


Figure 3.32: PAE CGH55015F1/CGH55015P1 transistor.

We proceed to calculate the output power from the network. We can see the results in *Figure 3.33*.

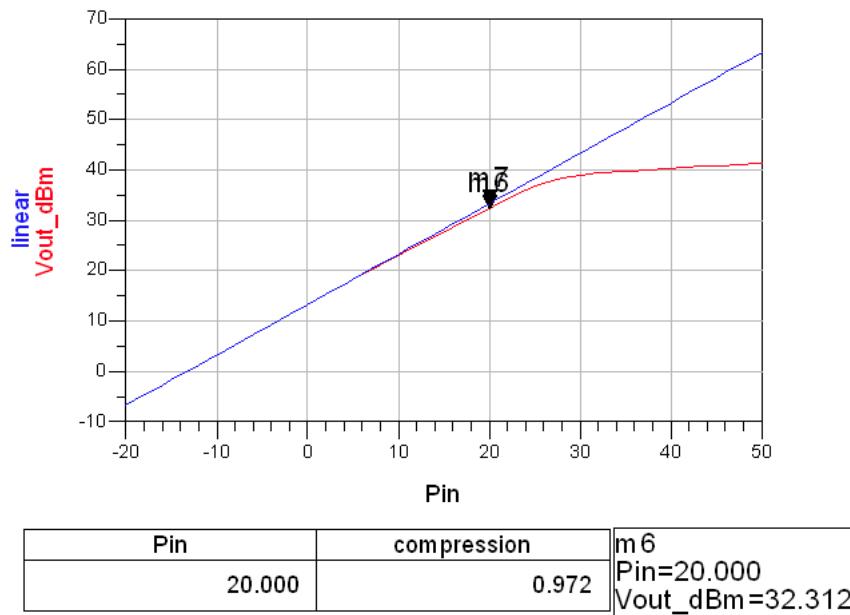


Figure 3.33: Output Power for CGH55015F1/CGH55015P1 transistor

As we see in *Figure 3.33* the output power related with the input power is a straight line. If the amplifier gives at the output a proportional power with respect to the input, that means that this proportional value would be the amplifier gain. But in our real amplifier it doesn't happen. We can see that there is a zone where we have a lineal behavior (happens when we have small power levels), but after a certain point the amplifier will be at the saturation zone and stops to amplify the input power. In our figure we can see that the gain suffers compression at high power.

In our amplifier this situation happens when that $P_{in} = 20 \text{ dBm}$ and we obtain $P_{out} = 32.312 \text{ dBm}$, so from 0.1 Watts at the input we obtain 1.7029425619 Watts at the output.

For this transistor we have to find out the IP3 point at the output too. So as we did before we will use the tool that ADS provide us. And the results are the following:

$$IP3 = 44.702 \text{ dBm}$$

So comparing it with the rule-of-thumb we have that the 1 dB compression point falls approximately 12.39 dBm below the third-order intercept point.

Chapter 4

Final results. Layout design.

As we can see at the two last points, we have a better Output Power for the CGH55015F1/CGH55015P1 transistor, so even if we obtain less bandwidth than with the ATF-521P8 transistor, and we don't full accomplish this targets, we decided to use CREE transistor.

So the next step is to search for the actual capacitors that are to be used in order to create our layout, and finally the PCB. After some research we decided to use components from MURATA Company, we can see which components we used in the Annex C.

Once we find out which components we are going to use, we have to add traces at the bias network in order to design a path for the DC components in the PCB; also the traces should overlap onto the components a bit to ensure that there are no gaps. The minimum trace width will depend on the frequency at which the circuit will be used. A minimum trace width of 20 – 25 mils is fairly safe.

PCB effects can be divided into two broad categories—those that most noticeably affect the static or dc operation of the circuit, and those that most noticeably affect dynamic or ac circuit operation, especially at high frequencies.

So we tried to design the DC path as far as possible from the RF circuit, specially the DC input and the capacitors that we put in order to stabilize the DC input voltage.

So we can see in *Figure 4.1* the final result with the traces, the capacitors and inductors that finally we are going to use.

Once we start the creation of the layout we realized that we couldn't connect the RF connectors directly with the capacitor, so we would need an extra transmission line at the RF input and output. This would change the behavior of our matching networks that we already designed, so we choose to change the place of the capacitors, such that we can connect the connector with the transmission lines.

In our Layout we have to create a substrate, that in our case would be the same that we have in the schematic from which we create the layout. If we check in our substrate we have designed VIA HOLE. This is important because it will connect the conductor with the ground layer, due it connect two metallization layers in case we need it.

A microstrip-based circuit requires multiple ground connections, which are drilled through the PCB. These are called bias, or via holes, and the performance of these connections has a very important effect on the overall circuit behavior. The via is made by drilling a small hole (or more) and inserting metallization around the hole. The holes that we have in our circuit introduce parasitics, so a good way to model them would be as a parallel LC circuit.

We also add a grounding plane. In order to do it ADS provides the “Create Clearance” tool. It has been added with uniform clearance around traces/components, also the bottom plane will be a ground plane. This ground plane that is in the top layer, has to be connected with the bottom ground layer. In order to do this we place bias. The placement of this bias is critical for achieving the desired

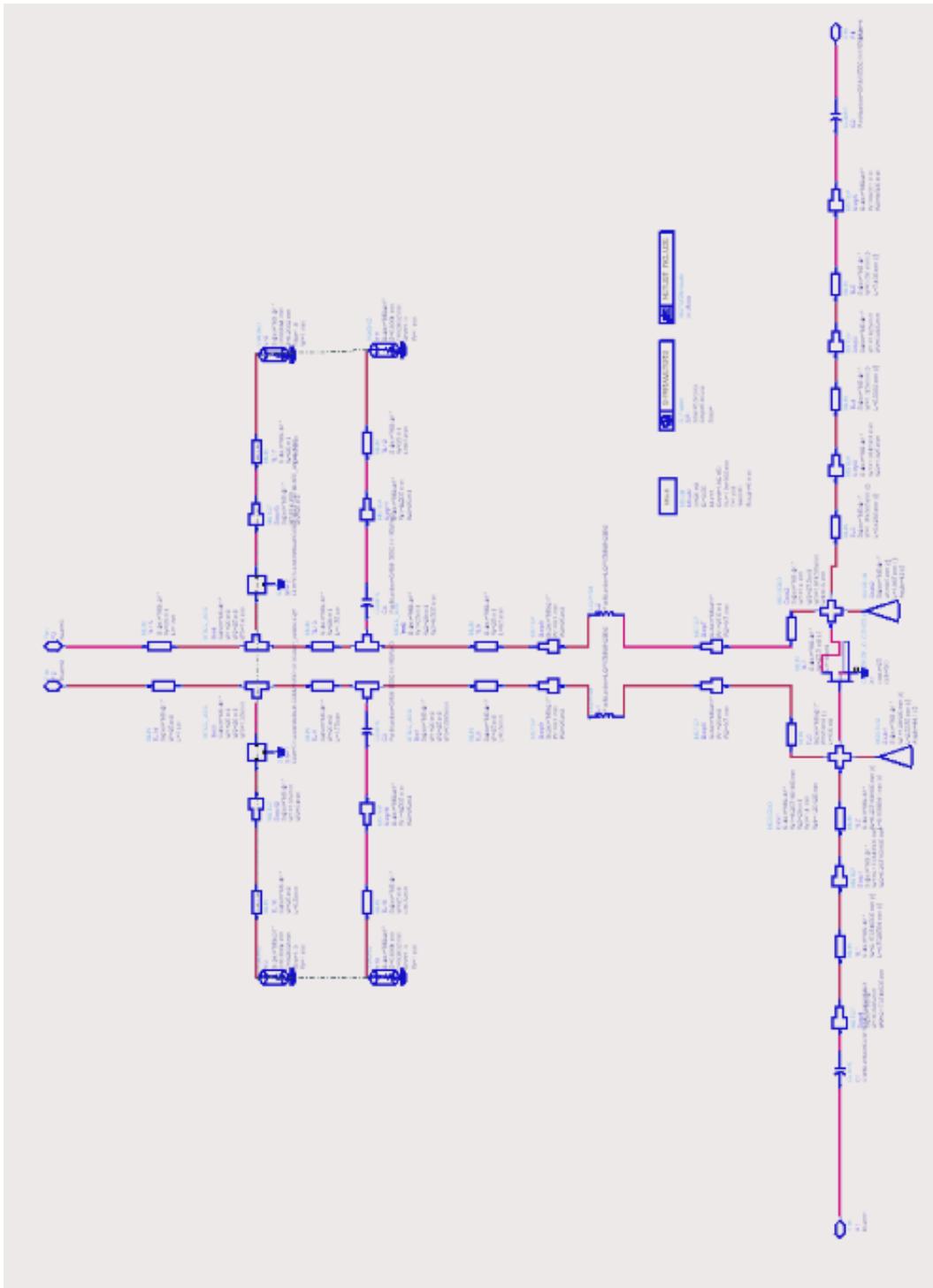


Figure 4.1: Schematic with traces for CGH55015F1/CGH55015P1 transistor

impedance and loss characteristics, as well as for suppressing parasitic wave modes. The clearance is important because with it we can separate the grounding plane in the top with our current circuit; and the reason that we need a grounding plane in the top layer is to have better grounding for our circuit.

The ground plane in the upper layer is placed because the large amount of metal will have as low a resistance as is possible. Due to the large flattened conductor pattern, we have as low an inductance as possible, resulting in minimizing spurious ground difference voltages across the conducting plane.

In *Figure 4.2* we can see the upper part from our design and in *Figure 4.3* its corresponding bottom side.

Once we made this changes we proceed to use a very powerful tool that ADS provide us, MOMENTUM. This tool allow us to evaluate and design modern communications systems products. It accepts arbitrary design geometries (including multi-layer structures) and uses frequency-domain Method of Moments (MoM) technology to accurately simulate complex EM effects including coupling and parasitics.

Apart from acting as a low impedance return path for decoupling high frequency currents it also minimizes the electromagnetic interferences.

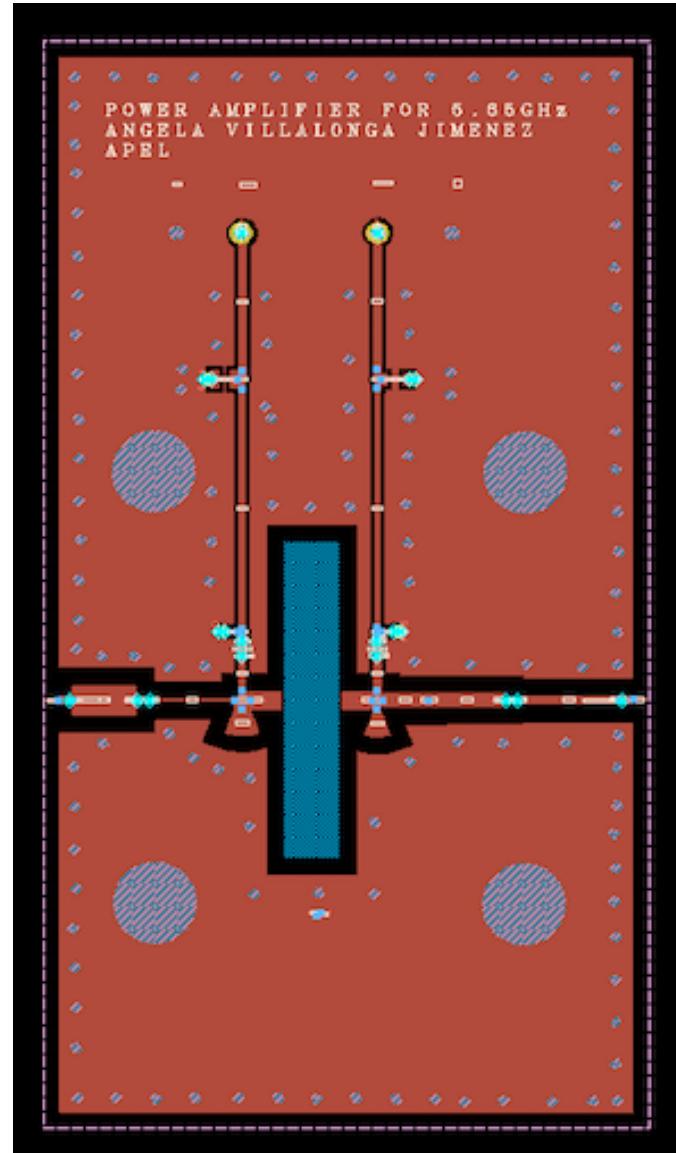


Figure 4.2: Final Layout (upper layer)

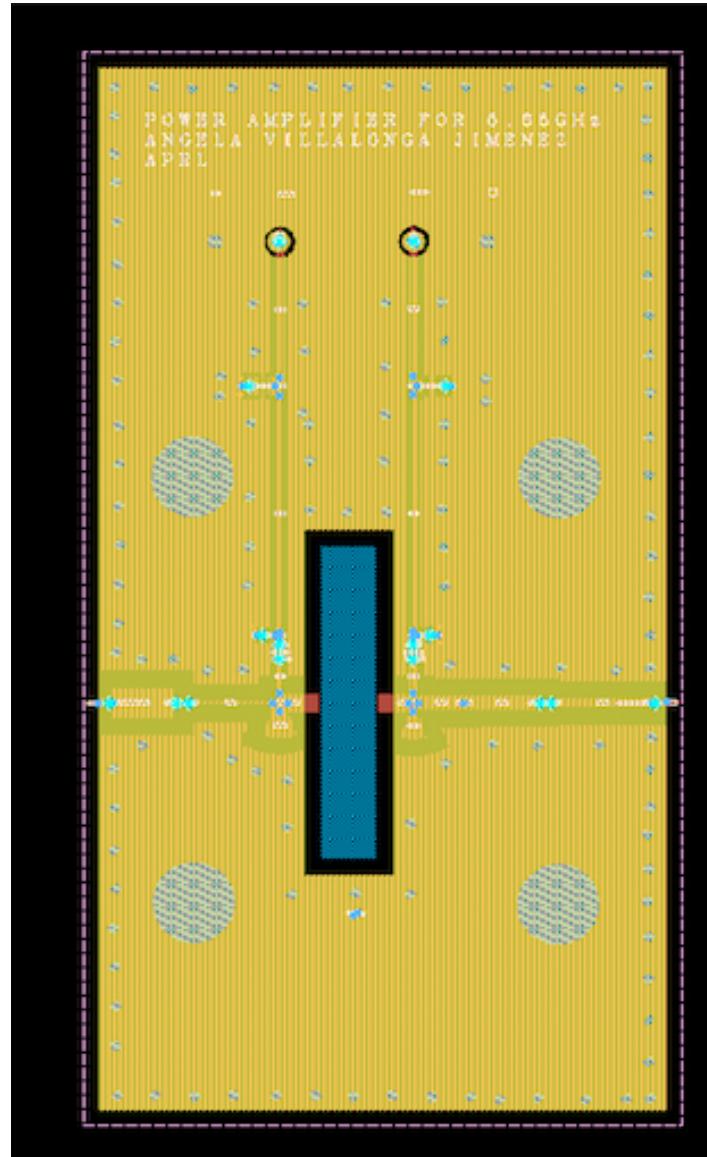


Figure 4.3: Final Layout (bottom layer)

It is an electromagnetic simulator that computes S-parameters for general planar circuits; and topologies connecting bias between layers, so one can simulate multilayer RF/microwave printed circuit boards. Momentum gives a complete tool set to predict the performance of high-frequency circuit boards.

Momentum identifies parasitics coupling between components, it goes beyond simple analysis and verification to design automation of circuit performance and visualize current flow and 3-Dimensional displays of far-field radiation.

We should make a short introduction about the method of moments (MOM). This method is based on the decomposition of the Green's functions in two parts: quasi-static in the near field region and the dynamic contribution in the far field region. Using this decomposition of Green's functions, the method of moment matrix entries can be reduced to a sum of two integrals, it means that a numerical technique is used to convert these integral equations into a linear system that can be solved numerically using a computer.

The first one is expressed in the spatial field and corresponds to the quasi-static contribution. It is analytically evaluated after a development in Taylor series of the exponential terms in the function to be integrated. The integrals expressed in the spectral field and corresponding to the dynamic part have the advantage of being calculated on a finite range and this is independent of the choice of the basis and test functions. The integrals expressed in the spectral field are performed by using numerical integration.

Another useful characteristic that we used is the EM/Circuit co-simulation. With this tool we can make the simulation using the results from momentum (that take in account the results that we will obtain if we have the pbc) and from the other side we will be able to place the components that we want to use because in the layout we only can take in account the footprint effects and not the effects of our component. So this tool allow us to have closer results to reality.

Due to the fact that we consider the effects of the layout, we have changes on the bandwidth and the central frequency, that's moved. A way to fix this is trying to make some optimization with the tuning tool, but now it is not so obvious. We will try to explain it.

Once we have our layout we should create a component from it, because this allows us to use it as a component in the schematic, taking into account the results from momentum, the resulting circuit is in *Figure 4.5*. After that we go to the schematic and we need to create a data base, because we realized that every time that you were changing a parameter it has to do the complete simulation in momentum all over again. In order to obtain this data base we make an sweep of the desired parameters (in our case, i took width, length and angle from the input and output radial stub). After the simulation I realized that the only parameter that was introducing changes on the central frequency was the length from the input matching network stub. So I created another data base that will sweep this parameter but in a more accurate way, considering more points in the simulation, we can see it in *Figure 4.4*

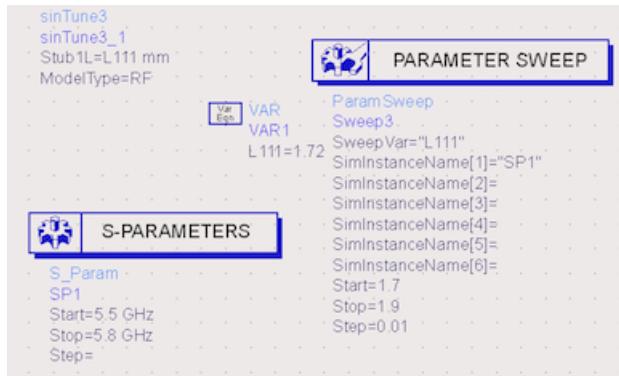


Figure 4.4: Parameter Sweep for the Layout Cosimulation

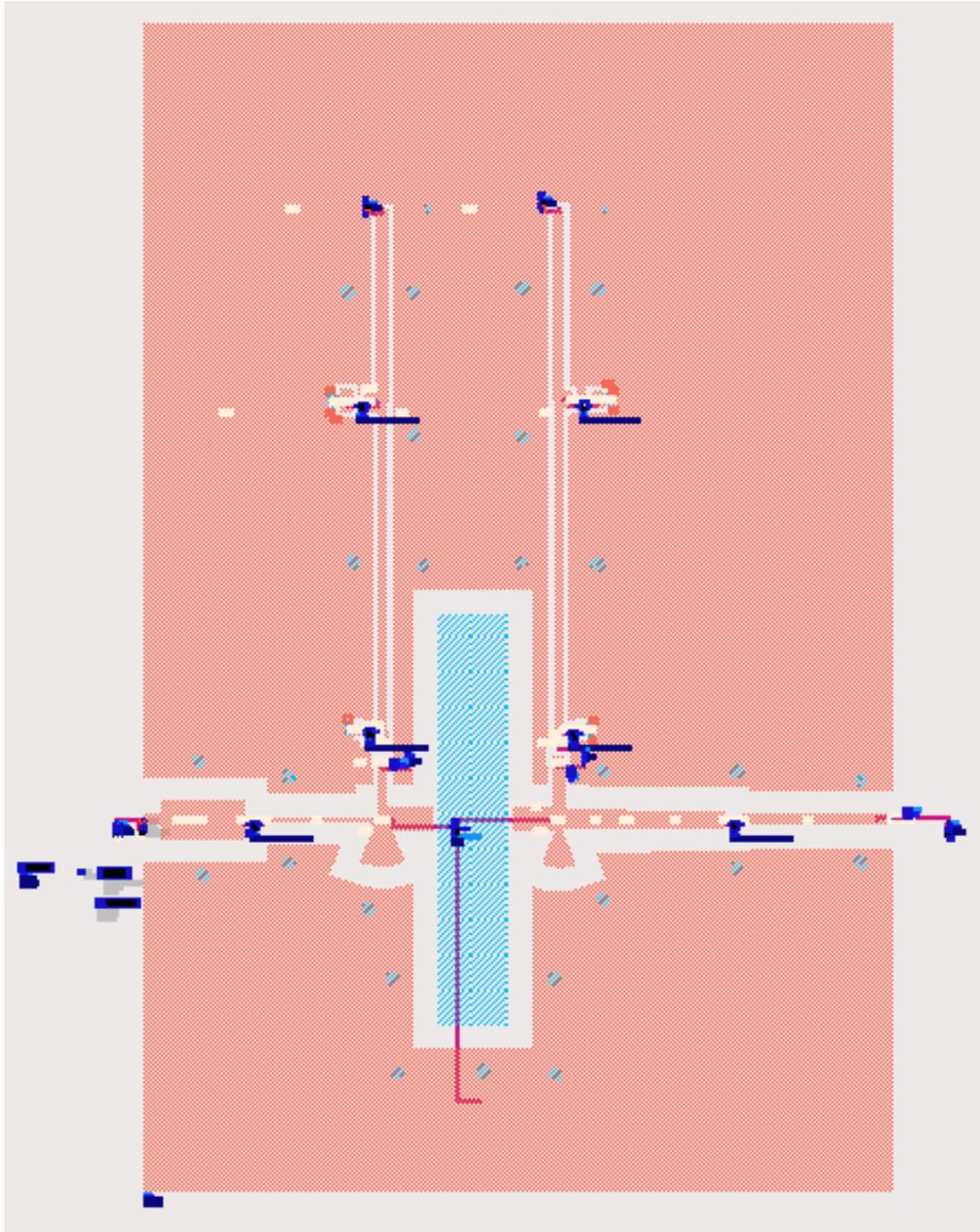


Figure 4.5: Parameter Sweep for the Layout Cosimulation

After that we create another schematic with the optimized circuit, obtaining the following results. As we can see in *Figure 4.6* we obtain the central frequency

close to the desired value at 5.675 GHz and we obtain a bandwidth of 173MHz.

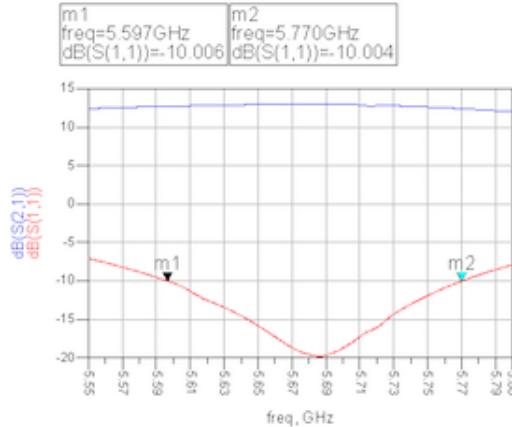


Figure 4.6: Layout final S11 and S21 parameters.

With this results that we just obtain we proceed to obtain the output power, IP3 point, Power Added efficiency, isolation, and stability, to see if we suffer big changes with the actual coupling and decoupling components.

First we will check the stability. The results are represented in *Figure 4.7* and we can see that at our frequency the designed amplifier continues being unconditionally stable, because $K>1$ and $\Delta<1$ all over the frequency range.

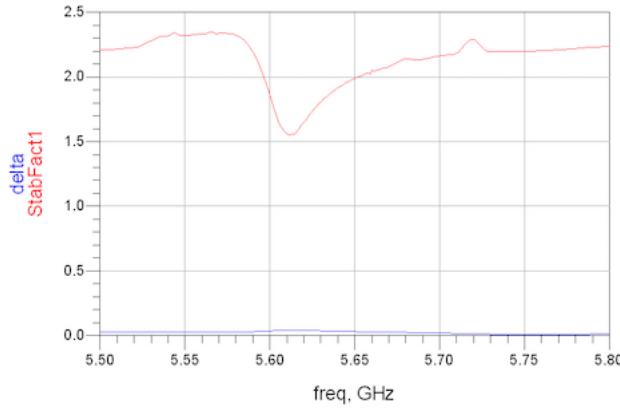


Figure 4.7: Stability for Cosimulation Circuit

Another point that we characterized before is the isolation, and we can see the results in *Figure 4.8*. As we see we obtain good isolation, always under around -27dB, where in the schematic results was under -28dBm.

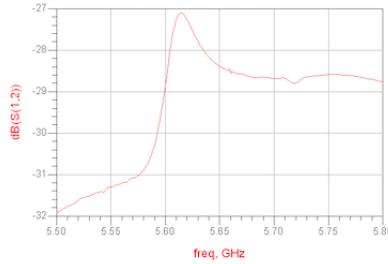


Figure 4.8: Isolation for Cosimulation Circuit .

We also find the PAE (Power Added efficiency). As illustrated in *Figure 4.9*. In the schematic simulation we had an efficiency around 0.4 when now the efficiency is almost 0.49.

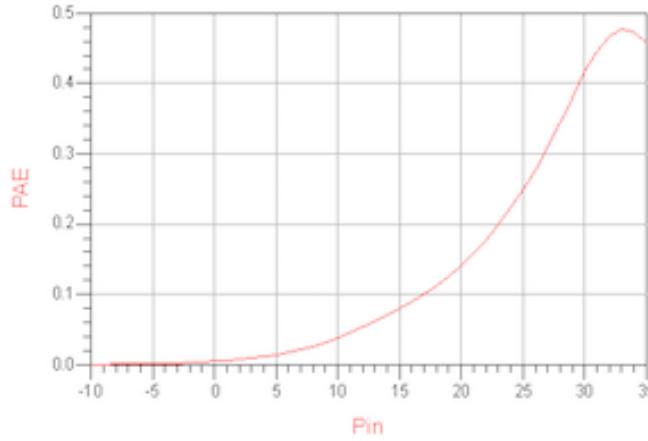


Figure 4.9: PAE for Cosimulation Circuit .

One of our last parameters that we have to check is the output power. The results are in *Figure 4.10*.

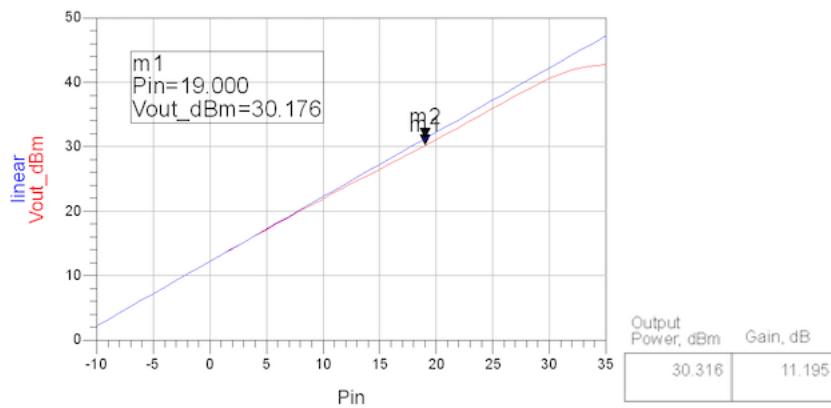


Figure 4.10: Output Power for Cosimulation Circuit

As we see in *Figure 4.10* the output power that we obtain is 30.316 dBm when Pin=19 dBm more or less, so as we can see our 1-dB compression point has been reduced from the values that we obtained on the schematic simulation.

That was Pin= 20 dBm and we obtain Pout=32.312dBm.

The last parameter that we want to calculate is the IP3 point at the output.

- . The results are the following:

$$IP3 = 46.278dBm$$

This value that we obtain differs from the previous value that was 44.702dBm, but comparing it with the rule-of-thumb we have that the 1 dB compression point falls approximately 15.962 dBm below the third-order intercept point, so the results are different but still valid.

Chapter 5

Conclusions

The purpose of this diploma theses was to design a pre-power amplifier in order to be the stage that precedes the power amplifier. We described that for a pre-PA we need to obtain a high efficiency, moderate gain, and enough output power in order to drive the power amplifier.

Our targets from the beginning were to obtain a gain around 10 dB, a -10 dB return losses all over the bandwidth and obtain an output power around 2 Watts.

Once we described our goals we decided to make the design for two different transistors, ATF-521P8 transistor and CGH55015F1/CGH55015P1 transistor.

During the design of the amplifier several methods have been studied and tested in simulation. Finally for both transistors we decided to use the *Chebyshev multisection quarter-wave transformers* for the input and output matching network.

As we can see in the final results for both designs, only the CREE transistor is capable of providing us the desired output power, because the transistor from AVAGO it is not suitable for the design of a pre power amplifier, but we have to clarify that the other required targets were accomplished by both of the transistors.

After evaluating the results we decided to use CREE transistor, even if we obtained less bandwidth than the desired one.

In conclusion, the final results we obtain a 13 dB gain with return losses -10 dB all over 173MHz bandwitdth, with a 5.675 GHz central frequency and an Output Power of 30.316 dBm.

The final step after all the research will be the manufacture of the PCB, which is something that will be done in a close future.

Annex

Annex A. Matlab script for *Chebyshev multisection quarter-wave transformers.*

```
%Define impedances
%OUTPUT
Zo=50;
%INPUT;
Zl= 286.1216;
%order. It can takes n=2, 3, 4.
N=3;
%reflection coefficient at the input
%G=-10;
%rm=10^(G/10);
rm=0.1;
%We calculate Tm (m=N)
Tm0= (1/rm)*abs((Zl-Zo)/(Zl+Zo));
%determinate x0
x0= cosh((1/N)*acosh(Tm0));
%find the zero positions, the number of zeros is the order of the
%polynomials
solposi=zeros(1,N);
anguloposi=zeros(1,N);
realpartposi=zeros(1,N);
```

```

imagpartposi=zeros(1,N);
for i= 1: ceil(N/2)
    solposi(i)= cos((2*i-1)*(pi/(2*N)));//positive result for i
    anguloposi(i)=2*acos(solposi(i)/x0);% positive angle result
    solposi(i+N-1)=-solposi(i);%negative result for i
    anguloposi(i+N-1)=2*acos(solposi(i+N-1)/x0);% negative angle negative
    realpartposi(i)=cos(anguloposi(i));
    realpartposi(i+N-1)=cos(anguloposi(i+N-1));
    imagpartposi(i)=sin(anguloposi(i));
    imagpartposi(i+N-1)=sin(anguloposi(i+N-1));
end
%-----WITH N=2
if (N==2)
    w1=realpartposi(1)+1i*imagpartposi(1);
    w2=realpartposi(2)+1i*imagpartposi(2);
    res1=-w2-w1;
    res2=w1*w2;
    gammaTotal=res1+res2+1;
    gamma2=(1/gammaTotal)*((Zl-Zo)/(Zl+Zo));
    gamma1=res1*gamma2;
    z2=((1-gamma2)/(1+gamma2))*Zl
    z1=((1-gamma1)/(1+gamma1))*z2
end
%-----WITH N=3
if (N==3)
    w1=realpartposi(1)+1i*imagpartposi(1);
    w2=realpartposi(2)+1i*imagpartposi(2);
    w3=realpartposi(3)+1i*imagpartposi(3);
    res1=-w2-w1-w3;
    res2=w1*w2+w2*w3+w1*w3;
    res3=-w1*w2*w3;

```

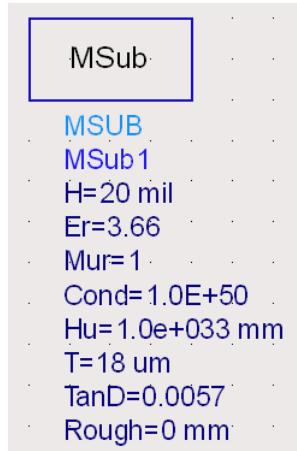
```

gammaTotal=res1+res2+res3+1;
gamma3=(1/gammaTotal)*((Zl-Zo)/(Zl+Zo));
gamma2=res1*gamma3;
gamma1=res2*gamma2;
z3=((1-gamma3)/(1+gamma3))*Zl
z2=((1-gamma2)/(1+gamma2))*z3
z1=((1-gamma1)/(1+gamma1))*z2
end
%-----WITH N=4
if (N==4)
w1=realpartposi(1)+1i*imagpartposi(1);
w2=realpartposi(2)+1i*imagpartposi(2);
w3=realpartposi(4)+1i*imagpartposi(4);
w4=realpartposi(5)+1i*imagpartposi(5);
res1=-w3-w4-w2-w1;
res2=w3*w4+w2*w3+w2*w4+w1*w3+w1*w4+w1*w2;
res3=-w3*w4*w2-w1*w3*w4-w1*w2*w3-w1*w2*w4;
res4=w1*w2*w3*w4;
gammaTotal=res4+res3+res2+res1+1;
gamma4=(1/gammaTotal)*((Zl-Zo)/(Zl+Zo));
gamma3=res1*gamma4;
gamma2=res2*gamma4;
gamma1=res3*gamma4;
z4=((1-gamma4)/(1+gamma4))*Zl
z3=((1-gamma3)/(1+gamma3))*z4
z2=((1-gamma2)/(1+gamma2))*z3
z1=((1-gamma1)/(1+gamma1))*z2
end

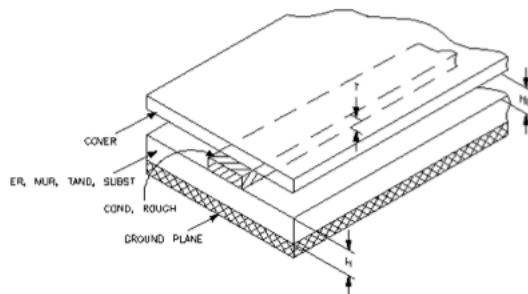
```

Annex B. Dielectric subtract.

The subtract that we are going to use is **Rogers RO4350**. The characteristics from our subtract are the following:



Now we can see a small explanation about the previous values:



H = subtract thickness.

Er = relative dielectric constant.

Mur = relative permeability.

Cond = conductor conductivity (Siemens/meters).

Hu = cover height.

T = conductor thickness.

TanD = dielectric loss tangent.

Rough = conductor surface roughness

Annex C. MURATA components.

For our design, as we commented before, we are going to use components from MURATA Company. So now, we proceed to name them.

1. For the input matching network we use a capacitor of 4.3 pF: GJM1555C1H4R3WB01D.
2. For the output matching network we use a capacitor of 1.5 pF: GRM1555C1H1R5WA01D.
3. For the coupling a decoupling of the bias network we use two capacitors of 1.5 pF: GRM1555C1H1R5WA01D, and two inductors of 8.2 nH: LQP15MN8N2B02.
4. For the capacitors that we use in order to guarantee the constant voltage we use one of 1uF: GRM2195C1H103JA01D, and another of 4.7 uF: GCM21BR71H474KA55L.

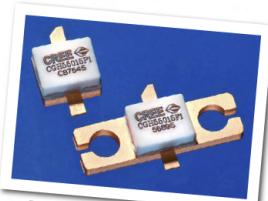
Annex D. Transistors Datasheet. ATF-521P8 and CGH55015F1/CGH55015P1 transistor



CGH55015F1 / CGH55015P1

15 W, 5500-5800 MHz, GaN HEMT for WiMAX

Cree's CGH55015F1/CGH55015P1 is a gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically for high efficiency, high gain and wide bandwidth capabilities, which makes the CGH55015F1/CGH55015P1 ideal for 5.5-5.8 GHz WiMAX and linear amplifier applications. The transistor is available in both screw-down, flange and solder-down, pill packages. Based on appropriate external match adjustment, the CGH55015F1/CGH55015P1 is suitable for 4.9 - 5.5 GHz applications as well.



Package Type: 440196 & 440166
PN: CGH55015P1 & CGH55015F1

Typical Performance 5.5-5.8GHz ($T_c = 25^\circ\text{C}$)

Parameter	5.50 GHz	5.65 GHz	5.80 GHz	Units
Small Signal Gain	10.7	11.0	10.7	dB
EVM at $P_{\text{AVE}} = 23 \text{ dBm}$	1.9	1.8	2.0	%
EVM at $P_{\text{AVE}} = 33 \text{ dBm}$	1.5	1.5	1.7	%
Drain Efficiency at $P_{\text{AVE}} = 33 \text{ dBm}$	25	25	25	%
Input Return Loss	11.5	14.5	10.5	dB

Note:

Measured in the CGH55015-TB amplifier circuit, under 802.16 OFDM, 3.5 MHz Channel BW, 1/4 Cyclic Prefix, 64 QAM Modulated Burst, 5 ms Burst, Symbol Length of 59, Coding Type RS-CC, Coding Rate Type 2/3, PAR = 9.8 dB @ 0.01 % Probability on CCDF.

Features

- 5.5 - 5.8 GHz Operation
- 15 W Peak Power Capability
- >10.5 dB Small Signal Gain
- 2 W $P_{\text{AVE}} < 2.0\%$ EVM
- 25 % Efficiency at 2 W Average Power
- Designed for WiMAX Fixed Access 802.16-2004 OFDM Applications
- Designed for Multi-carrier DOCSIS Applications



Large Signal Models Available for SiC & GaN

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1



Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units	Conditions
Drain-Source Voltage	V_{DSS}	84	Volts	25°C
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts	25°C
Power Dissipation	P_{DSS}	7	Watts	
Storage Temperature	T_{STG}	-65, +150	°C	
Operating Junction Temperature	T_J	225	°C	
Maximum Forward Gate Current	I_{GMAX}	4.0	mA	25°C
Maximum Drain Current ¹	I_{DMAX}	1.5	A	25°C
Soldering Temperature ²	T_S	245	°C	
Screw Torque	τ	60	in-oz	
Thermal Resistance, Junction to Case ³	R_{JJC}	8.0	°C/W	85°C
Case Operating Temperature ³	T_C	-40, +150	°C	30 seconds

Note:

¹ Current limit for long term, reliable operation.

² Refer to the Application Note on soldering at www.cree.com/products/wireless_appnotes.asp

³ Measured for the CGH55015 at $P_{DSS} = 7\text{W}$.

Electrical Characteristics ($T_c = 25^\circ\text{C}$)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics⁴						
Gate Threshold Voltage	$V_{GS(\text{th})}$	-3.8	-3.0	-2.3	V_{DC}	$V_{GS} = 10\text{ V}$, $I_D = 3.6\text{ mA}$
Gate Quiescent Voltage	$V_{GS(Q)}$	—	-2.7	—	V_{DC}	$V_{GS} = 28\text{ V}$, $I_D = 115\text{ mA}$
Saturated Drain Current	I_{DS}	2.9	3.5	—	A	$V_{GS} = 6.0\text{ V}$, $V_{DS} = 2.0\text{ V}$
Drain-Source Breakdown Voltage	V_{BR}	120	—	—	V_{DC}	$V_{GS} = -8\text{ V}$, $I_D = 3.6\text{ mA}$
RF Characteristics^{5,6} ($T_c = 25^\circ\text{C}$, $F_d = 5.65\text{ GHz}$ unless otherwise noted)						
Small Signal Gain	G_{RS}	8.5	11.0	—	dB	$V_{DD} = 28\text{ V}$, $I_{DQ} = 115\text{ mA}$
Drain Efficiency ⁷	η	20.6	25	—	%	$V_{DD} = 28\text{ V}$, $I_{DQ} = 115\text{ mA}$, $P_{Ave} = 2.0\text{ W}$
Error Vector Magnitude	EVM	—	2.0	2.5	%	$V_{DD} = 28\text{ V}$, $I_{DQ} = 115\text{ mA}$, $P_{Ave} = 2.0\text{ W}$
Output Mismatch Stress	VSWR	—	—	10 : 1	Ψ	No damage at all phase angles, $V_{DD} = 28\text{ V}$, $I_{DQ} = 115\text{ mA}$, $P_{Ave} = 2.0\text{ W}$
Dynamic Characteristics						
Input Capacitance	C_{GS}	—	4.5	—	pF	$V_{GS} = 28\text{ V}$, $V_{GS} = -8\text{ V}$, $f = 1\text{ MHz}$
Output Capacitance	C_{DS}	—	1.3	—	pF	$V_{GS} = 28\text{ V}$, $V_{GS} = -8\text{ V}$, $f = 1\text{ MHz}$
Feedback Capacitance	C_{GD}	—	0.2	—	pF	$V_{GS} = 28\text{ V}$, $V_{GS} = -8\text{ V}$, $f = 1\text{ MHz}$

Notes:

¹ Measured on wafer prior to packaging.

² Measured in the CGH55015-TB test fixture.

³ Under 802.16 OFDM, 3.5 MHz Channel BW, 1/4 Cyclic Prefix, 64 QAM Modulated Burst, 5 ms Burst, Symbol Length of 59, Coding Type RS-CC, Coding Rate Type 2/3, PAR = 9.8 dB @ 0.01 % Probability on CCDF.

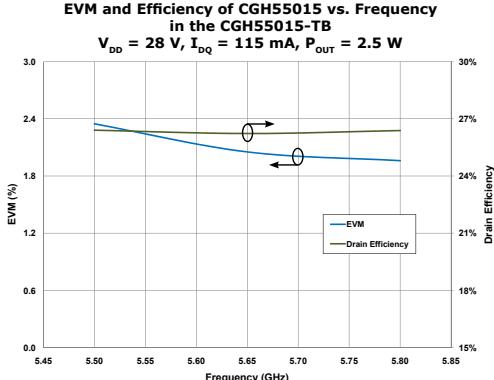
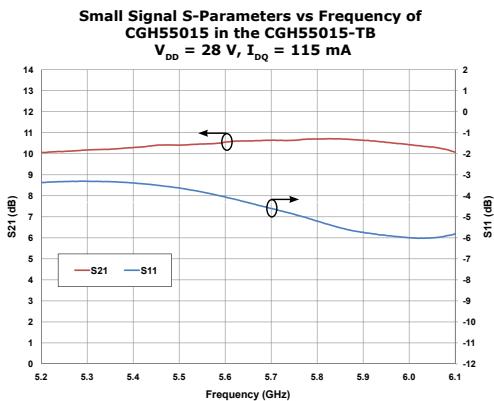
⁴ Drain Efficiency = P_{out} / P_{dc} .

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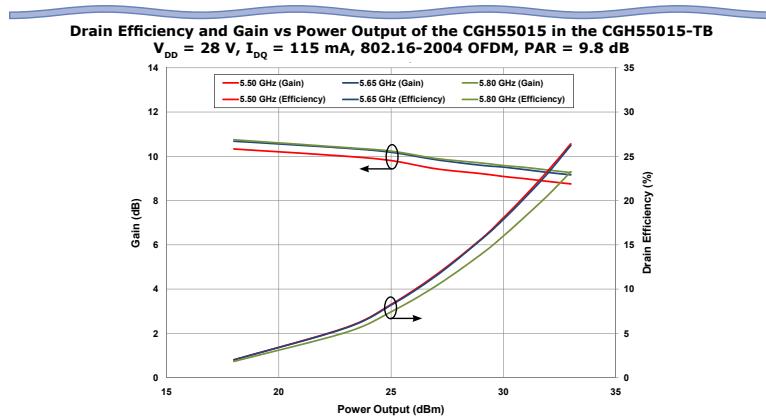
Typical WiMAX Performance



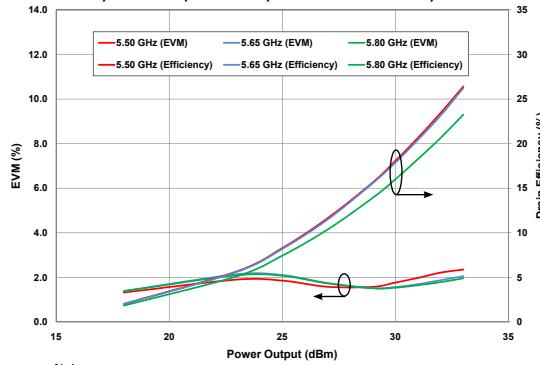
Note:
Under 802.16 OFDM, 3.5 MHz Channel BW, 1/4 Cyclic Prefix, 64 QAM Modulated Burst, Symbol Length of 59, Coding Type RS-CC, Coding Rate Type 2/3, PAR = 9.8 dB @ 0.01 % Probability on CCDF.



Typical WiMAX Performance



Typical EVM and Drain Efficiency vs Output Power of CGH55015 in the CGH55015-TB at 5.50 GHz, 5.65 GHz, 5.80 GHz, 802.16-2004 OFDM, PAR=9.8 dB



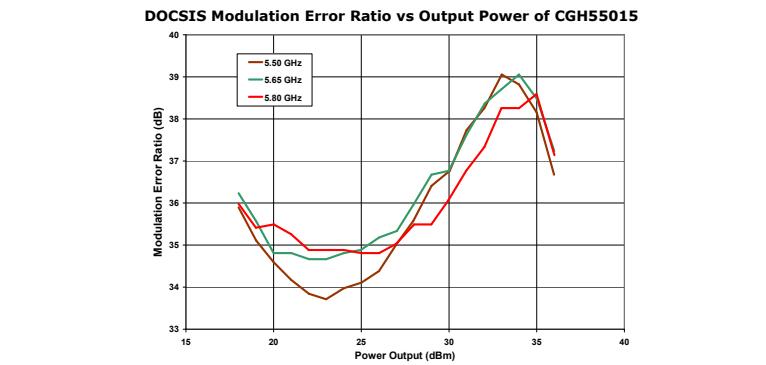
Note:
Under 802.16 OFDM, 3.5 MHz Channel BW, 1/4 Cyclic Prefix, 64 QAM
Modulated Burst, Symbol Length of 59, Coding Type RS-CC, Coding
Rate Type 2/3, PAR = 9.8 dB @ 0.01 % Probability on CCDF.

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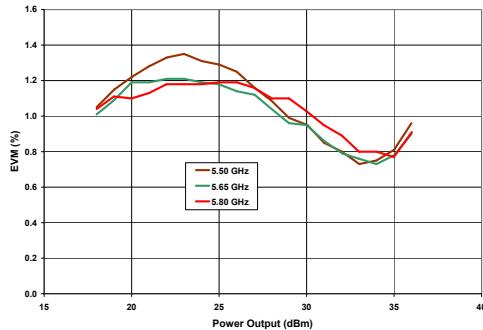
Typical DOCSIS Performance



Note:

MER is the metric of choice for cable systems and can be related to EVM by the following equation:
 $EVM(\%) = 100 \times 10^{-((MERdB + MTAdB)/20)}$. MTA is the "maximum-to-average constellation power ratio" which varies with the modulation type: MTA = 0 for BPSK and QPSK; 2.55 for 16QAM and 8QAM-DS; 3.68 for 64QAM and 32QAM-DS; 4.23 for 256QAM and 128QAM-DS

DOCSIS EVM vs Output Power of CGH55015 in Broadband Amplifier Circuit



Note:

Under DOCSIS, 6.0 MHz Channel BW, 64 QAM, PN23, Filter Alpha 0.18, PAR = 6.7dB.

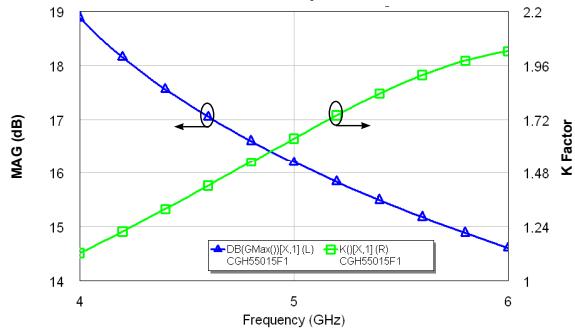
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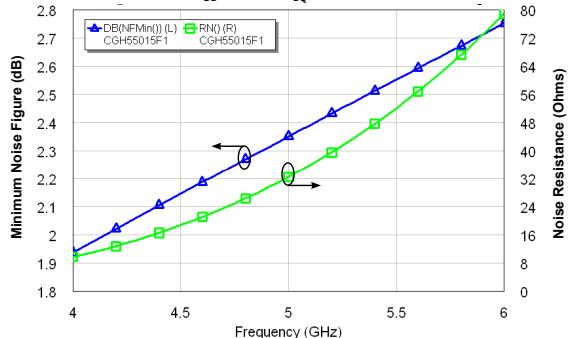
Typical Performance

Simulated Maximum Available Gain and K Factor of the CGH55015F1/P1
 $V_{DD} = 28$ V, $I_{DQ} = 115$ mA



Typical Noise Performance

Simulated Minimum Noise Figure and Noise Resistance vs Frequency of the CGH55015F1/P1
 $V_{DD} = 28$ V, $I_{DQ} = 115$ mA

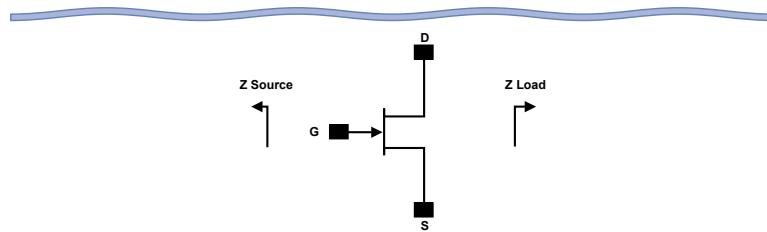


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Source and Load Impedances



Frequency (MHz)	Z Source	Z Load
5500	8.7 - j30.2	21.6 - j4.7
5650	10.2 - j26.9	24.2 - j5.5
5800	12.3 - j24.3	26.5 - j7.5

Note 1. $V_{DD} = 28V$, $I_{DD} = 115\text{ mA}$ in the 440166 package.

Note 2. Impedances are extracted from the CGH55015-TB demonstration amplifier and are not source and load pull data derived from the transistor.

Electrostatic Discharge (ESD) Classifications

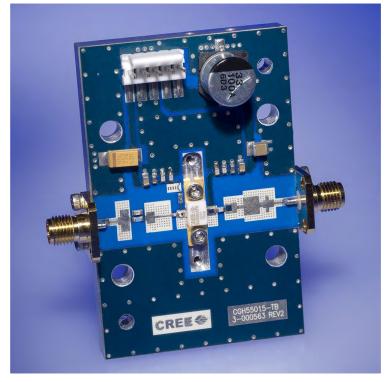
Parameter	Symbol	Class	Test Methodology
Human Body Model	HBM	1A > 250 V	JEDEC JESD22 A114-D
Charge Device Model	CDM	1 < 200 V	JEDEC JESD22 C101-C



CGH55015-TB Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
C1	CAP, 1.2pF, +/-0.1 pF, 0603, ATC 600S	1
C2	CAP, 0.3pF, +/-0.05 pF, 0402, ATC 600L	1
C9	CAP, 0.5pF, +/-0.05pF, 0603, ATC 600S	1
C4,C11	CAP, 18pF, +/-5%, 0603, ATC 600S	2
C5,C12	CAP, 39pF +/-5%, 0603, ATC 600S	2
C6,C13	CAP, CER, 180pF, 50V, +/-5%, COG, 0603	2
C7,C14	CAP, CER, 0.1UF, 50V, +/-10%, X7R, 0805	2
C8	CAP, 10UF, 16V, SMD TANTALUM	1
C15	CAP, 1.0UF +/-10%, 100V, 1210, X7R	1
C16	CAP, 33UF, 100V, ELECT, FK, SMD	1
R1	RES, 1/16W, 0603, 1% 562 OHMS	1
R2	RES, 1/16W, 0603, 1%, 22 OHMS	1
J1	HEADER RT> PLZ .1 CEN LK 5 POS	1
J3,J4	CONN, SMA, FLANGE	2
-	PCB, RO4350B, Er = 3.48, h = 20 mil	1
-	CGH55015	1

CGH55015-TB Demonstration Amplifier Circuit

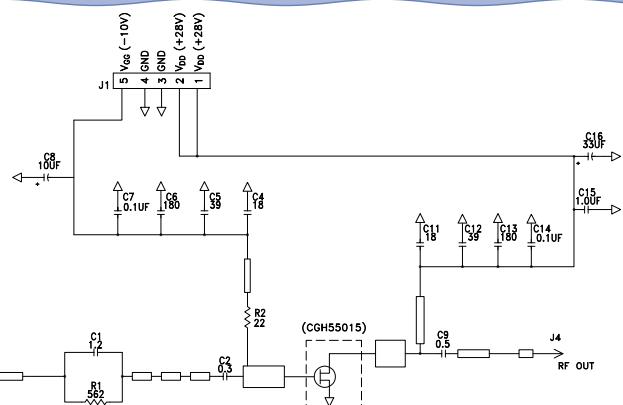


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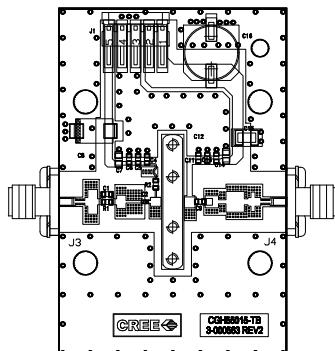
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CGH55015-TB Demonstration Amplifier Circuit Schematic



CGH55015-TB Demonstration Amplifier Circuit Outline



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Typical Package S-Parameters for CGH55015
(Small Signal, $V_{DS} = 28$ V, $I_{DQ} = 115$ mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.909	-125.16	17.56	107.52	0.026	20.86	0.330	-95.81
600 MHz	0.903	-134.72	15.15	101.24	0.027	15.25	0.318	-103.71
700 MHz	0.898	-142.24	13.28	95.96	0.027	10.66	0.312	-109.87
800 MHz	0.895	-148.34	11.79	91.38	0.027	6.76	0.309	-114.77
900 MHz	0.893	-153.43	10.58	87.30	0.028	3.37	0.310	-118.75
1.0 GHz	0.891	-157.78	9.59	83.58	0.028	0.34	0.312	-122.07
1.2 GHz	0.889	-164.93	8.06	76.89	0.028	-4.92	0.320	-127.35
1.4 GHz	0.888	-170.72	6.94	70.90	0.027	-9.46	0.332	-131.53
1.6 GHz	0.888	-175.64	6.08	65.34	0.027	-13.51	0.347	-135.09
1.8 GHz	0.888	-179.99	5.41	60.10	0.027	-17.20	0.362	-138.30
2.0 GHz	0.889	176.04	4.86	55.09	0.026	-20.60	0.378	-141.33
2.2 GHz	0.889	172.35	4.42	50.24	0.025	-23.76	0.394	-144.27
2.4 GHz	0.890	168.84	4.05	45.53	0.025	-26.70	0.410	-147.16
2.6 GHz	0.891	165.46	3.73	40.93	0.024	-29.44	0.426	-150.04
2.8 GHz	0.891	162.16	3.46	36.41	0.024	-31.97	0.441	-152.92
3.0 GHz	0.892	158.90	3.23	31.95	0.023	-34.32	0.455	-155.81
3.2 GHz	0.893	155.67	3.03	27.55	0.022	-36.45	0.469	-158.73
3.4 GHz	0.893	152.43	2.85	23.19	0.021	-38.38	0.482	-161.68
3.6 GHz	0.894	149.18	2.70	18.85	0.021	-40.07	0.494	-164.66
3.8 GHz	0.894	145.89	2.56	14.53	0.020	-41.52	0.506	-167.68
4.0 GHz	0.894	142.54	2.44	10.22	0.019	-42.71	0.516	-170.74
4.1 GHz	0.895	140.85	2.38	8.07	0.019	-43.19	0.521	-172.29
4.2 GHz	0.895	139.14	2.33	5.91	0.019	-43.59	0.526	-173.85
4.3 GHz	0.895	137.40	2.28	3.75	0.018	-43.92	0.530	-175.43
4.4 GHz	0.895	135.65	2.23	1.58	0.018	-44.16	0.535	-177.02
4.5 GHz	0.895	133.88	2.18	-0.59	0.018	-44.32	0.539	-178.62
4.6 GHz	0.895	132.08	2.14	-2.77	0.017	-44.38	0.543	179.75
4.7 GHz	0.895	130.26	2.10	-4.96	0.017	-44.35	0.546	178.11
4.8 GHz	0.895	128.41	2.06	-7.15	0.017	-44.23	0.550	176.45
4.9 GHz	0.895	126.53	2.03	-9.36	0.017	-44.02	0.553	174.77
5.0 GHz	0.895	124.63	1.99	-11.58	0.016	-43.71	0.556	173.07
5.1 GHz	0.895	122.69	1.96	-13.81	0.016	-43.30	0.559	171.35
5.2 GHz	0.895	120.72	1.93	-16.05	0.016	-42.81	0.561	169.60
5.3 GHz	0.895	118.73	1.90	-18.31	0.016	-42.22	0.564	167.83
5.4 GHz	0.895	116.70	1.87	-20.59	0.016	-41.56	0.566	166.04
5.5 GHz	0.895	114.63	1.84	-22.89	0.016	-40.83	0.568	164.21
5.6 GHz	0.895	112.53	1.81	-25.20	0.016	-40.05	0.570	162.36
5.7 GHz	0.895	110.39	1.79	-27.53	0.016	-39.22	0.572	160.47
5.8 GHz	0.895	108.22	1.77	-29.89	0.016	-38.35	0.574	158.55
5.9 GHz	0.895	106.00	1.74	-32.27	0.016	-37.48	0.575	156.60
6.0 GHz	0.895	103.75	1.72	-34.67	0.016	-36.62	0.576	154.61

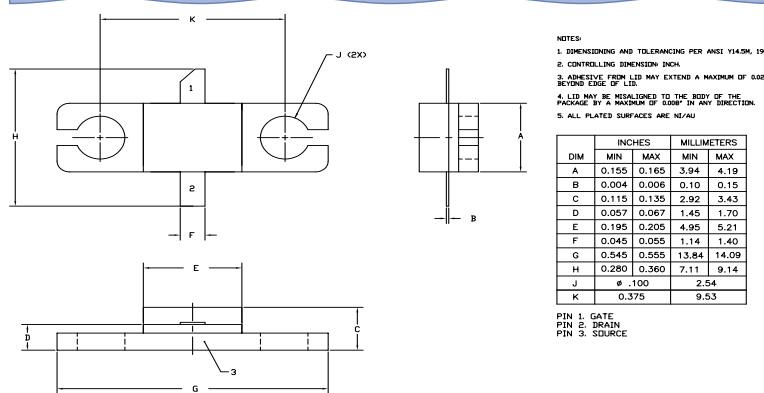
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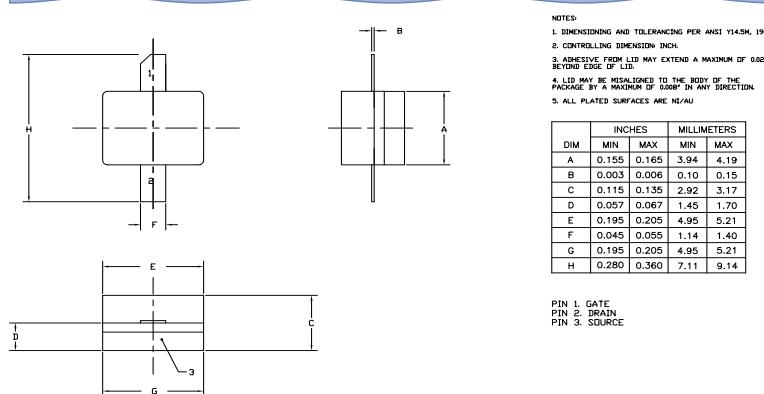
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Product Dimensions CGH55015F1 (Package Type — 440166)



Product Dimensions CGH55015P1 (Package Type — 440196)



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ATF-521P8

High Linearity Enhancement Mode^[1] Pseudomorphic HEMT
in 2x2 mm² LPCC^[3] Package



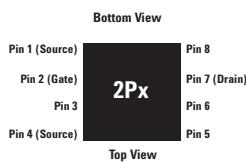
Data Sheet

Description

Avago Technologies' ATF-521P8 is a single-voltage high linearity, low noise E-pHEMT housed in an 8-lead JEDEC standard leadless plastic chip carrier (LPCC^[3]) package. The device is ideal as a medium-power, high-linearity amplifier. Its operating frequency range is from 50 MHz to 6 GHz.

The thermally efficient package measures only 2mm x 2mm x 0.75mm. Its backside metalization provides excellent thermal dissipation as well as visual evidence of solder reflow. The device has a Point MTTF of over 300 years at a mounting temperature of +85°C. All devices are 100% RF & DC tested.

Pin Connections and Package Marking



Note:

Package marking provides orientation and identification
"2P" = Device Code
"X" = Month code indicates the month of manufacture.

Note:

1. Enhancement mode technology employs a single positive V_{gs} eliminating the need of negative gate voltage associated with conventional depletion mode devices.
2. Refer to reliability datasheet for detailed MTTF data
3. Conform to JEDEC reference outline MO229 for DRP-N
4. Linearity Figure of Merit (LFOM) is essentially OIP3 divided by DC bias power.

Features

- Single voltage operation
- High linearity and P1dB
- Low noise figure
- Excellent uniformity in product specifications
- Small package size: 2.0 x 2.0 x 0.75 mm³
- Point MTTF > 300 years^[2]
- MSL-1 and lead-free
- Tape-and-reel packaging option available

Specifications

- 2 GHz; 4.5V, 200 mA (Typ.)
- 42 dBm output IP3
- 26.5 dBm output power at 1 dB gain compression
- 1.5 dB noise figure
- 17 dB Gain
- 12.5 dB LFOM^[4]

Applications

- Front-end LNA Q2 and Q3, driver or pre-driver amplifier for Cellular/PCS and WCDMA wireless infrastructure
- Driver amplifier for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E-pHEMT for other high linearity applications



ATF-521P8 Absolute Maximum Ratings^[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain – Source Voltage ^[2]	V	7
V_{GS}	Gate – Source Voltage ^[2]	V	-5 to 1
V_{GD}	Gate Drain Voltage ^[2]	V	-5 to 1
I_{DS}	Drain Current ^[2]	mA	500
I_{GS}	Gate Current	mA	46
P_{diss}	Total Power Dissipation ^[3]	W	1.5
$P_{in\ max}$	RF Input Power	dBm	27
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
$\theta_{ch,b}$	Thermal Resistance ^[4]	°C/W	45

Notes:

1. Operation of this device in excess of any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. Board (package belly) temperature T_b is 25°C. Derate 22 mW/°C for $T_b > 83^\circ\text{C}$.
4. Channel to board thermal resistance measured using 150°C Liquid Crystal Measurement method.
5. Device can safely handle +27dBm RF Input Power provided I_{GS} is limited to 46mA. I_{GS} at P1dB drive level is bias circuit dependent.

Product Consistency Distribution Charts^[5,6]

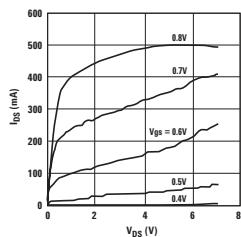


Figure 1. Typical I-V Curves.
($V_{GS} = 0.1\text{ V per step}$)

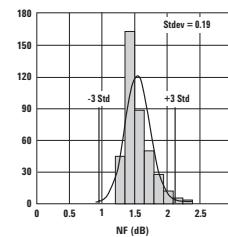


Figure 2. NF @ 2 GHz, 4.5 V, 200 mA.
Nominal = 1.5 dB.

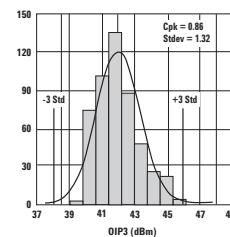


Figure 3. OIP3 @ 2 GHz, 4.5 V, 200 mA.
Nominal = 41.9 dBm, LSL = 38.5 dBm.

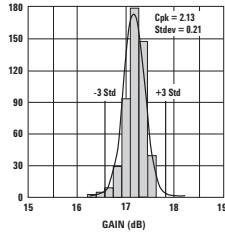


Figure 4. Gain @ 2 GHz, 4.5 V, 200 mA.
Nominal = 17.2 dB, LSL = 15.5 dB,
USL = 18.5 dB.

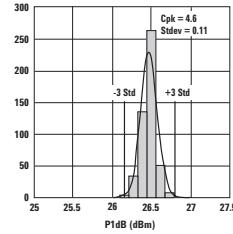


Figure 5. P1dB @ 2 GHz, 4.5 V, 200 mA.
Nominal = 26.5 dBm, LSL = 25 dBm.

Notes:

5. Distribution data sample size is 500 samples taken from 5 different wafers. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
6. Measurements are made on production test board, which represents a trade-off between optimal OIP3, P1dB and VSWR. Circuit losses have been de-embedded from actual measurements.

ATF-521P8 Electrical Specifications

$T_A = 25^\circ\text{C}$, DC bias for RF parameters is $V_{ds} = 4.5\text{V}$ and $I_{ds} = 200\text{ mA}$ unless otherwise specified.

Symbol	Parameter and Test Condition	Units	Min.	Typ.	Max.
V_{gs}	Operational Gate Voltage $V_{ds} = 4.5\text{V}, I_{ds} = 200\text{ mA}$	V	—	0.62	—
V_{th}	Threshold Voltage $V_{ds} = 4.5\text{V}, I_{ds} = 16\text{ mA}$	V	—	0.28	—
I_{dss}	Saturated Drain Current $V_{ds} = 4.5\text{V}, V_{gs} = 0\text{V}$	μA	—	14.8	—
G_m	Transconductance $V_{ds} = 4.5\text{V}, G_m = \Delta I_{dss}/\Delta V_{gs};$ $V_{gs} = V_{gs1} - V_{gs2}$ $V_{gs1} = 0.55\text{V}, V_{gs2} = 0.5\text{V}$	mmho	—	1300	—
I_{gss}	Gate Leakage Current $V_{ds} = 0\text{V}, V_{gs} = -4\text{V}$	μA	-20	0.49	—
NF	Noise Figure ^[1] $f = 2\text{ GHz}$ $f = 900\text{ MHz}$	dB	—	1.5	—
G	Gain ^[1] $f = 2\text{ GHz}$ $f = 900\text{ MHz}$	dB	15.5	17	18.5
OIP3	Output 3 rd Order Intercept Point ^[1] $f = 2\text{ GHz}$ $f = 900\text{ MHz}$	dBm	38.5	42	—
P1dB	Output 1dB Compressed ^[1] $f = 2\text{ GHz}$ $f = 900\text{ MHz}$	dBm	25	26.5	—
PAE	Power Added Efficiency $f = 2\text{ GHz}$ $f = 900\text{ MHz}$	%	45	60	—
ACLR	Adjacent Channel Leakage Power Ratio ^[1,2] Offset BW = 5 MHz Offset BW = 10 MHz	dBc	—	-51.4	—
		dBc	—	-61.5	—

Notes:

1. Measurements obtained using production test board described in Figure 6.

2. ACLR test spec is based on 3GPP TS 25.141 V5.3.1 (2002-06)

– Test Model 1

– Active Channels: PCCPCH + SCH + CPICH + PICH + SCCPCH + 64 DPCH (SF=128)

– Freq = 2140 MHz

– Pin = -5 dBm

– Chan Integ Bw = 3.84 MHz

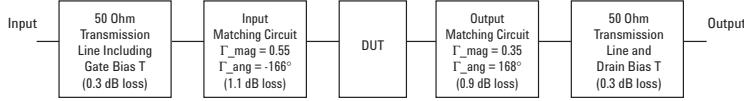


Figure 6. Block diagram of the 2 GHz production test board used for NF, Gain, OIP3, P1dB and PAE and ACLR measurements. This circuit achieves a trade-off between optimal OIP3, P1dB and VSWR. Circuit losses have been de-embedded from actual measurements.

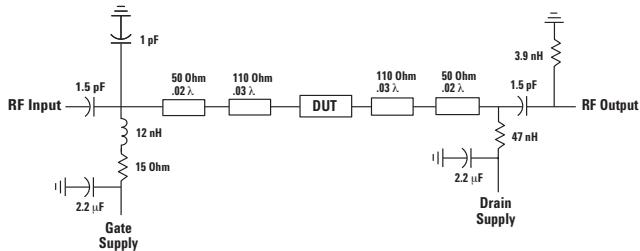


Figure 7. Simplified schematic of production test board. Primary purpose is to show 15 Ohm series resistor placement in gate supply. Transmission line tapers, tee intersections, bias lines and parasitic values are not shown.

Gamma Load and Source at Optimum OIP3 and P1dB Tuning Conditions

The device's optimum OIP3 and P1dB measurements were determined using a Maury load pull system at 4.5V, 200 mA quiescent bias:

Freq (GHz)	Optimum OIP3		OIP3 (dBm)	Gain (dB)	P1dB (dBm)	PAE (%)
	Gamma Source Mag	Ang (deg)				
0.9	0.413	10.5	0.314	179.0	42.7	16.0
2	0.368	162.0	0.538	-176.0	42.5	15.8
2.4	0.318	169.0	0.566	-169.0	42.0	14.1
3.9	0.463	-134.0	0.495	-159.0	40.3	9.6
					27.3	43.9

Freq (GHz)	Optimum P1dB		OIP3 (dBm)	Gain (dB)	P1dB (dBm)	PAE (%)
	Gamma Source Mag	Ang (deg)				
0.9	0.587	12.7	0.613	-172.1	39.1	14.5
2	0.614	126.1	0.652	-172.5	39.5	12.9
2.4	0.649	145.0	0.682	-171.5	40.0	12.0
3.9	0.552	-162.8	0.670	-151.2	38.1	9.6
					27.9	39.1

**ATF-521P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal OIP3**

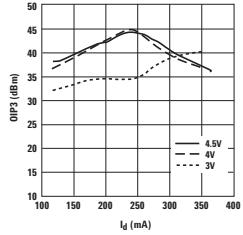


Figure 8. OIP3 vs. I_{ds} and V_{ds} at 2 GHz.

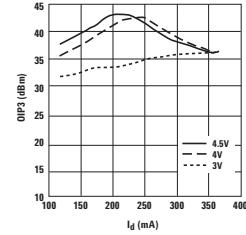


Figure 9. OIP3 vs. I_{ds} and V_{ds} at 900 MHz.

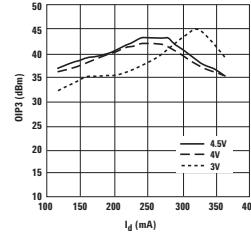


Figure 10. OIP3 vs. I_{ds} and V_{ds} at 3.9 GHz.

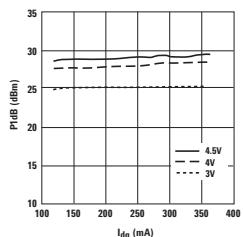


Figure 11. P1dB vs. I_{dq} and V_{ds} at 2 GHz.

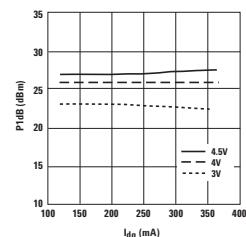


Figure 12. P1dB vs. I_{dq} and V_{ds} at 900 MHz.

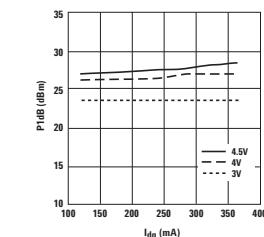


Figure 13. P1dB vs. I_{dq} and V_{ds} at 3.9 GHz.

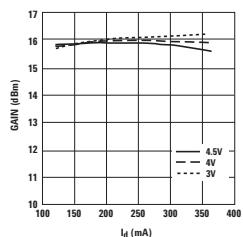


Figure 14. Small Signal Gain vs. I_{ds} and V_{ds} at 2 GHz.

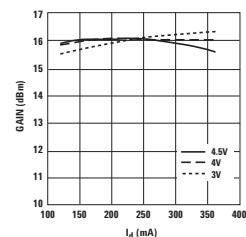


Figure 15. Small Signal Gain vs. I_{ds} and V_{ds} at 900 MHz.

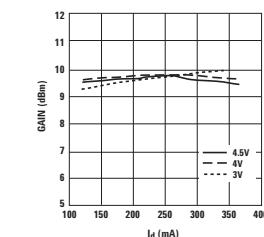


Figure 16. Small Signal Gain vs. I_{ds} and V_{ds} at 3.9 GHz.

Note:

Bias current for the above charts are quiescent conditions. Actual level may increase depending on amount of RF drive.

**ATF-521P8 Typical Performance Curves, continued (at 25°C unless specified otherwise)
Tuned for Optimal OIP3**

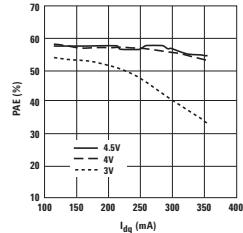


Figure 17. PAE @ P1dB vs. I_{dq} and V_{ds} at 2 GHz.

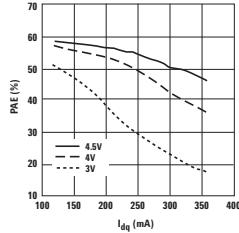


Figure 18. PAE @ P1dB vs. I_{dq} and V_{ds} at 900 MHz.

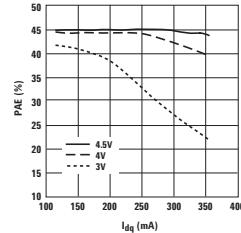


Figure 19. PAE @ P1dB vs. I_{dq} and V_{ds} at 3.9 GHz.

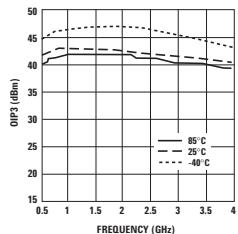


Figure 20. OIP3 vs. Temp and Freq tuned for optimal OIP3 at 4.5V, 200 mA.

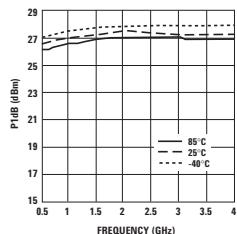


Figure 21. P1dB vs. Temp and Freq tuned for optimal OIP3 at 4.5V, 200 mA.

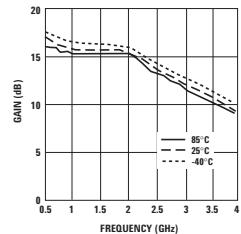


Figure 22. Gain vs. Temp and Freq tuned for optimal OIP3 at 4.5V, 200 mA.

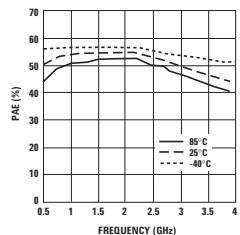


Figure 23. PAE vs Temp and Freq tuned for optimal OIP3 at 4.5V, 200 mA.

Note:

Bias current for the above charts are quiescent conditions. Actual level may increase depending on amount of RF drive.

**ATF-521P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal P1dB**

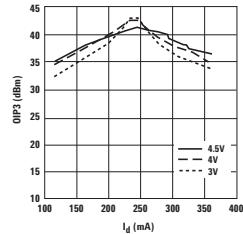


Figure 24. OIP3 vs. I_{ds} and V_{ds} at 2 GHz.

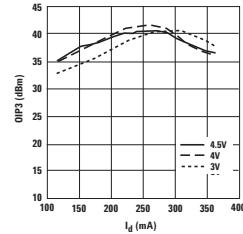


Figure 25. OIP3 vs. I_{ds} and V_{ds} at 900 MHz.

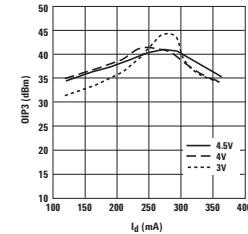


Figure 26. OIP3 vs. I_{ds} and V_{ds} at 3.9 GHz.

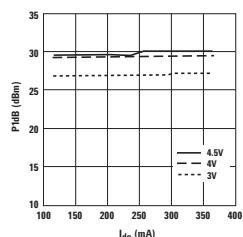


Figure 27. P1dB vs. I_{dq} and V_{ds} at 2 GHz.

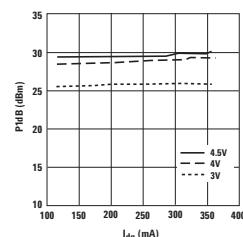


Figure 28. P1dB vs. I_{dq} and V_{ds} at 900 MHz.

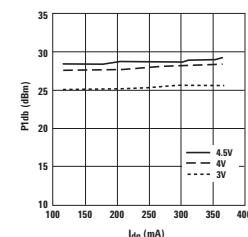


Figure 29. P1dB vs. I_{dq} and V_{ds} at 3.9 GHz.

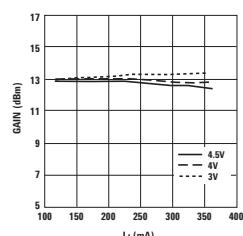


Figure 30. Gain vs. I_{ds} and V_{ds} at 2 GHz.

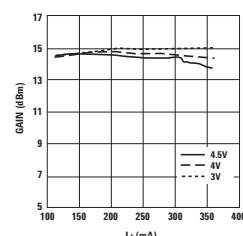


Figure 31. Gain vs. I_{ds} and V_{ds} at 900 MHz.

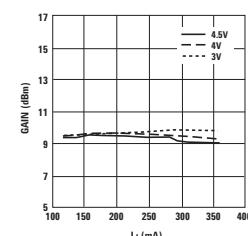


Figure 32. Gain vs. I_{ds} and V_{ds} at 3.9 GHz.

Note:

Bias current for the above charts are quiescent conditions. Actual level may increase depending on amount of RF drive.

ATF-521P8 Typical Performance Curves, continued (at 25°C unless specified otherwise)
Tuned for Optimal P1dB

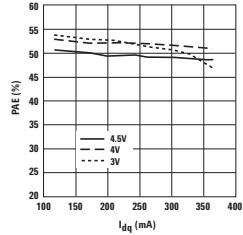


Figure 33. PAE @ P1dB vs. I_{dq} and V_{ds} at 2 GHz.

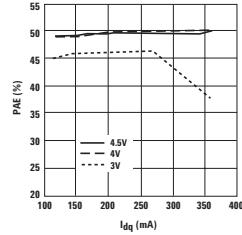


Figure 34. PAE @ P1dB vs. I_{dq} and V_{ds} at 900 MHz.

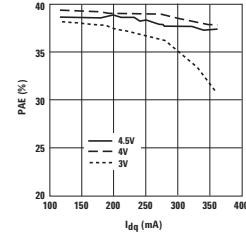


Figure 35. PAE @ P1dB vs. I_{dq} and V_{ds} at 3.9 GHz.

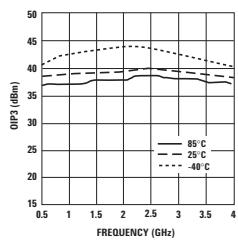


Figure 36. OIP3 vs. Temp and Freq tuned for optimal P1dB at 4.5V, 200 mA.

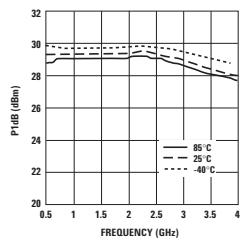


Figure 37. P1dB vs. Temp and Freq (tuned for optimal P1dB at 4.5V, 200 mA).

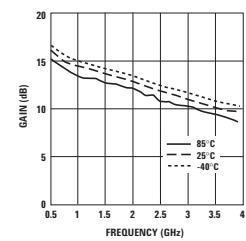


Figure 38. Gain vs. Temp and Freq tuned for optimal P1dB at 4.5V, 200 mA.

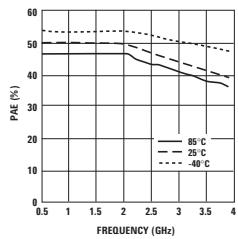


Figure 39. PAE vs Temp and Freq tuned for optimal P1dB at 4.5V.

Note:
Bias current for the above charts are quiescent conditions. Actual level may increase depending on amount of RF drive.

ATF-521P8 Typical Scattering Parameters at 25°C, V_{DS} = 4.5V, I_{DS} = 280 mA

Freq. GHz	S ₁₁			S ₂₁			S ₁₂			S ₂₂			MSG/MAG dB
	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.		
0.1	0.613	-96.9	33.2	45.79	141.7	-39.5	0.011	51.3	0.317	-108.3	36.2		
0.2	0.780	-131.8	30.0	31.50	121.6	-36.7	0.015	37.1	0.423	-138.5	33.2		
0.3	0.831	-147.2	27.3	23.26	111.0	-36.2	0.015	30.6	0.466	-152.4	31.9		
0.4	0.855	-156.4	25.1	18.04	104.1	-35.4	0.017	28.2	0.483	-159.9	30.3		
0.5	0.860	-162.0	23.5	14.98	99.7	-35.2	0.017	27.4	0.488	-163.8	29.5		
0.6	0.878	-166.7	22.0	12.62	95.6	-35.0	0.018	26.1	0.496	-167.0	28.5		
0.7	0.888	-170.2	20.8	10.95	92.8	-34.6	0.019	27.4	0.497	-169.9	27.6		
0.8	0.887	-172.6	19.7	9.63	90.0	-34.3	0.019	28.9	0.500	-171.7	27.0		
0.9	0.894	-174.5	18.7	8.65	87.9	-33.7	0.021	28.5	0.501	-173.6	26.1		
1.0	0.886	-177.2	17.9	7.82	85.4	-33.8	0.020	30.3	0.502	-175.7	25.9		
1.5	0.892	175.0	14.3	5.20	76.3	-32.8	0.023	34.6	0.502	178.8	23.5		
2.0	0.883	168.7	12.1	4.01	68.4	-31.2	0.027	36.7	0.492	173.6	20.2		
2.5	0.890	162.8	10.2	3.24	61.5	-30.0	0.032	36.8	0.499	169.8	18.5		
3.0	0.884	157.2	8.6	2.71	54.5	-28.9	0.036	39.2	0.494	165.7	16.2		
4.0	0.890	146.6	6.1	2.02	40.6	-27.0	0.045	36.1	0.505	157.8	13.8		
5.0	0.893	137.0	4.1	1.60	27.6	-25.5	0.053	32.4	0.529	150.3	11.9		
6.0	0.896	127.9	2.3	1.31	15.4	-24.2	0.061	28.2	0.551	142.9	10.4		
7.0	0.906	119.5	0.9	1.11	3.7	-22.9	0.071	22.9	0.570	135.5	9.6		
8.0	0.882	105.6	-0.8	0.92	-9.8	-21.3	0.086	14.5	0.567	127.3	6.8		
9.0	0.887	96.4	-1.7	0.82	-22.2	-20.1	0.098	7.2	0.585	117.8	6.2		
10.0	0.887	84.6	-2.9	0.72	-33.6	-19.3	0.109	-1.0	0.593	107.3	5.0		
11.0	0.882	72.3	-3.9	0.64	-45.8	-18.5	0.119	-10.5	0.617	97.1	3.9		
12.0	0.878	62.2	-5.0	0.56	-57.0	-18.0	0.126	-19.8	0.636	86.0	2.8		
13.0	0.894	52.0	-6.4	0.48	-67.8	-17.8	0.130	-28.6	0.662	74.7	2.1		
14.0	0.888	42.0	-7.6	0.42	-76.2	-17.3	0.137	-36.1	0.697	67.5	0.9		
15.0	0.884	34.6	-8.3	0.38	-84.3	-16.6	0.147	-42.9	0.732	58.7	0.3		
16.0	0.830	24.7	-9.5	0.34	-92.8	-16.1	0.156	-52.4	0.752	51.9	-1.8		
17.0	0.708	11.0	-9.0	0.35	-99.5	-15.4	0.169	-63.8	0.816	46.1	-2.2		
18.0	0.790	-12.7	-10.3	0.31	-93.1	-16.4	0.152	-82.8	0.660	41.2	-4.3		

Typical Noise Parameters at 25°C, V_{DS} = 4.5V, I_{DS} = 280 mA

Freq. GHz	F _{min} dB	R _{opt} Mag.	R _{opt} Ang.	R _n	G _a dB
0.5	1.20	0.47	170.00	2.8	22.8
1.0	1.30	0.53	-177.00	2.6	20.1
2.0	1.61	0.61	-166.34	2.7	17.3
3.0	1.68	0.69	-155.85	4.0	14.4
4.0	2.12	0.67	-146.98	8.4	11.6
5.0	2.77	0.71	-134.35	19.0	9.9
6.0	2.58	0.79	-125.22	26.7	8.8
7.0	2.85	0.82	-115.35	47.2	7.5
8.0	3.35	0.73	-105.76	65.2	5.7

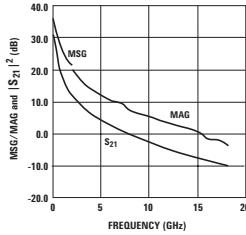


Figure 40. MSG/MAG and |S₂₁|² vs. Frequency at 4.5V, 280 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{min}'s below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Typical Scattering Parameters, $V_{ds} = 4.5V$, $I_{ds} = 200\text{ mA}$

Freq. GHz	S_{11}			S_{21}			S_{12}			S_{22}			MSG/MAG dB
	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	
0.1	0.823	-89.9	34.4	52.21	135.6	-37.9	0.013	46.2	0.388	-113.0	36.0		
0.2	0.873	-128.7	30.5	33.39	115.7	-35.6	0.017	32.0	0.478	-143.2	32.9		
0.3	0.879	-145.5	27.6	23.90	106.3	-34.9	0.018	27.0	0.507	-156.0	31.2		
0.4	0.885	-155.1	25.2	18.25	100.5	-34.7	0.018	25.8	0.518	-163.1	30.1		
0.5	0.883	-161.1	23.6	15.12	96.6	-34.4	0.019	24.8	0.519	-166.7	29.0		
0.6	0.897	-165.9	22.1	12.66	92.9	-34.1	0.020	24.2	0.525	-169.6	28.0		
0.7	0.895	-169.5	20.8	10.95	90.5	-33.7	0.021	24.2	0.526	-172.2	27.2		
0.8	0.894	-171.9	19.6	9.59	88.0	-33.6	0.021	25.3	0.528	-174.0	26.6		
0.9	0.900	-174.7	18.7	8.64	86.2	-33.1	0.022	26.2	0.528	-175.6	25.9		
1	0.893	-176.6	17.8	7.78	83.7	-33.1	0.022	27.6	0.529	-177.7	25.5		
1.5	0.894	175.3	14.3	5.17	75.7	-32.1	0.025	32.6	0.527	177.2	23.2		
2	0.889	168.5	12.0	4.00	67.8	-30.8	0.029	33.6	0.516	172.1	21.4		
2.5	0.888	162.6	10.2	3.22	61.3	-29.8	0.032	35.2	0.514	168.1	18.4		
3	0.892	157.0	8.6	2.69	54.5	-28.6	0.037	35.6	0.517	164.0	16.7		
4	0.884	146.5	6.0	2.00	40.7	-26.8	0.046	34.4	0.526	156.0	13.5		
5	0.891	137.0	4.0	1.59	28.3	-25.2	0.055	30.5	0.548	148.3	11.9		
6	0.889	127.9	2.3	1.30	16.4	-24.0	0.063	26.4	0.568	141.0	10.1		
7	0.902	119.6	0.9	1.11	4.8	-22.8	0.072	21.0	0.584	133.5	9.4		
8	0.881	105.6	-0.9	0.90	-8.8	-21.3	0.086	13.3	0.580	124.9	6.7		
9	0.891	96.0	-1.7	0.83	-20.1	-20.2	0.098	5.6	0.594	115.8	6.4		
10	0.876	83.9	-2.9	0.72	-32.1	-19.3	0.108	-3.2	0.600	105.3	4.6		
11	0.885	73.1	-3.6	0.66	-43.7	-18.5	0.119	-12.1	0.622	95.0	4.2		
12	0.885	60.9	-4.8	0.57	-54.1	-18.0	0.126	-21.6	0.641	84.1	3.0		
13	0.893	53.0	-6.3	0.48	-66.2	-17.7	0.131	-29.9	0.663	73.1	2.1		
14	0.889	42.2	-7.2	0.44	-74.0	-17.2	0.138	-36.7	0.698	65.7	1.2		
15	0.894	34.3	-7.8	0.41	-80.6	-16.9	0.143	-44.1	0.732	57.4	1.0		
16	0.840	25.0	-8.4	0.38	-83.4	-16.2	0.154	-54.3	0.750	51.0	-0.8		
17	0.719	9.1	-10.0	0.32	-90.1	-15.4	0.171	-64.8	0.815	44.5	-3.2		
18	0.794	-8.1	-12.2	0.25	-102.3	-16.7	0.147	-84.1	0.655	40.4	-5.9		

Typical Noise Parameters, $V_{ds} = 4.5V$, $I_{ds} = 200\text{ mA}$

Freq. GHz	F_{min} dB	Γ_{opt} Mag.	Γ_{opt} Ang.	R_n	G_a dB
0.5	0.60	0.30	130.00	2.8	20.2
1.0	0.72	0.35	150.00	2.6	18.4
2.0	0.96	0.47	-175.47	1.9	16.5
3.0	1.11	0.57	-162.03	2.1	13.8
4.0	1.44	0.62	-150.00	4.5	11.2
5.0	1.75	0.69	-136.20	10.0	9.8
6.0	1.99	0.74	-127.35	17.0	8.7
7.0	2.12	0.80	-116.83	28.5	7.5
8.0	2.36	0.69	-108.38	35.6	5.7

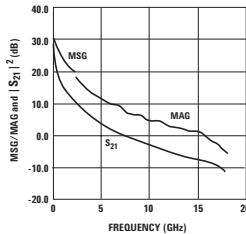


Figure 41. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 4.5V, 200 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{min} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NPS test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.

2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Typical Scattering Parameters, $V_{ds} = 4.5V$, $I_{ds} = 120\text{ mA}$

Freq. GHz	S_{11}			S_{21}			S_{12}			S_{22}			MSG/MAG dB
	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.		
0.1	0.913	-84.6	34.2	51.26	135.4	-36.4	0.015	49.0	0.423	-106.6	35.3		
0.2	0.900	-125.0	30.3	32.80	115.4	-33.9	0.020	31.2	0.499	-139.4	32.1		
0.3	0.896	-142.0	27.4	23.39	106.1	-33.4	0.021	25.3	0.522	-153.4	30.5		
0.4	0.893	-152.3	25.1	17.89	100.3	-32.9	0.023	23.5	0.530	-161.1	28.9		
0.5	0.882	-158.4	23.4	14.75	96.3	-32.6	0.023	22.5	0.531	-165.0	28.1		
0.6	0.895	-164.2	21.8	12.36	92.9	-32.7	0.023	20.6	0.537	-168.4	27.3		
0.7	0.893	-167.8	20.6	10.71	90.5	-32.4	0.024	20.4	0.537	-171.2	26.5		
0.8	0.895	-170.8	19.5	9.39	88.0	-32.3	0.024	21.1	0.539	-173.1	25.9		
0.9	0.897	-173.0	18.5	8.44	86.1	-32.2	0.025	22.1	0.539	-174.8	25.3		
1	0.895	-175.5	17.6	7.59	83.6	-31.8	0.026	23.0	0.540	-176.9	24.7		
1.5	0.893	176.0	14.1	5.07	75.3	-31.1	0.028	25.5	0.538	177.4	22.6		
2	0.889	169.2	11.8	3.89	67.8	-30.0	0.032	27.9	0.528	172.2	20.8		
2.5	0.882	163.6	10.0	3.15	61.2	-29.0	0.036	30.2	0.526	168.1	19.4		
3	0.888	157.9	8.4	2.62	54.6	-28.2	0.039	30.2	0.528	163.9	16.9		
4	0.883	146.8	5.9	1.97	40.7	-26.5	0.047	29.7	0.536	155.7	13.6		
5	0.885	137.7	3.8	1.55	28.2	-25.2	0.055	26.3	0.556	148.1	11.6		
6	0.892	128.0	2.1	1.28	16.7	-24.0	0.063	21.9	0.576	140.5	10.2		
7	0.894	120.4	0.6	1.08	5.1	-22.8	0.072	18.2	0.591	133.1	8.9		
8	0.880	105.7	-1.0	0.89	-8.7	-21.2	0.087	10.6	0.585	124.3	6.6		
9	0.876	96.5	-1.9	0.81	-20.8	-20.1	0.099	3.2	0.602	114.9	5.7		
10	0.879	84.4	-3.0	0.71	-32.7	-19.3	0.108	-5.2	0.605	104.5	4.7		
11	0.889	72.8	-3.8	0.65	-44.3	-18.6	0.118	-13.5	0.624	94.2	4.3		
12	0.881	62.4	-5.2	0.55	-56.0	-18.1	0.125	-23.1	0.642	83.4	2.7		
13	0.893	54.0	-6.3	0.48	-66.6	-17.7	0.130	-31.4	0.664	72.4	2.2		
14	0.891	42.1	-7.2	0.44	-72.6	-17.3	0.136	-38.4	0.697	65.1	1.2		
15	0.888	34.1	-8.3	0.39	-79.2	-16.8	0.144	-45.9	0.732	56.7	0.4		
16	0.845	25.3	-9.1	0.35	-89.6	-16.1	0.157	-55.0	0.751	50.4	-1.5		
17	0.828	13.2	-11.2	0.28	-95.9	-15.6	0.167	-64.2	0.821	44.0	-3.9		
18	0.827	-10.2	-11.0	0.28	-92.5	-16.6	0.147	-86.1	0.654	39.9	-4.3		

Typical Noise Parameters, $V_{ds} = 4.5V$, $I_{ds} = 120\text{ mA}$

Freq. GHz	F_{min}		Γ_{opt}		R_n		G_a	
	dB	Mag.	Mag.	Ang.	dB			
0.5	0.60	0.19	162.00	3.0	20.0			
1.0	0.72	0.30	164.00	2.6	18.3			
2.0	0.81	0.44	176.97	2.0	15.9			
3.0	0.92	0.56	-164.98	2.0	13.6			
4.0	1.24	0.59	-155.51	3.4	11.1			
5.0	1.50	0.70	-136.55	11.1	9.7			
6.0	1.60	0.75	-128.59	16.0	8.7			
7.0	1.88	0.81	-117.31	24.0	7.6			
8.0	2.02	0.68	-109.54	28.8	5.6			

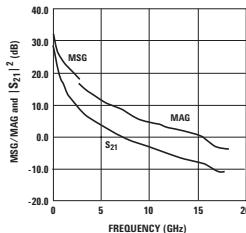


Figure 42. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 4.5V, 120 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{min} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NPS test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.

2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Typical Scattering Parameters, $V_{ds} = 4V$, $I_{ds} = 200 \text{ mA}$

Freq. GHz	S_{11}			S_{21}			S_{12}			S_{22}			MSG/MAG dB
	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB		
0.1	0.843	-90.5	34.3	51.89	134.8	-37.7	0.013	46.5	0.408	-118.1	36.0		
0.2	0.879	-129.3	30.3	32.88	115.0	-35.4	0.017	32.1	0.507	-146.1	32.9		
0.3	0.888	-146.1	27.4	23.48	105.8	-35.1	0.018	26.0	0.539	-158.3	31.2		
0.4	0.892	-155.6	25.1	17.91	100.1	-34.4	0.019	25.1	0.549	-164.8	29.7		
0.5	0.886	-161.5	23.4	14.80	96.3	-34.2	0.020	24.6	0.551	-168.2	28.7		
0.6	0.896	-165.7	21.8	12.37	92.7	-34.2	0.020	24.1	0.556	-170.9	27.9		
0.7	0.897	-169.5	20.6	10.74	90.5	-33.6	0.021	24.7	0.557	-173.5	27.1		
0.8	0.898	-172.2	19.5	9.39	88.1	-33.5	0.021	24.4	0.559	-175.2	26.5		
0.9	0.896	-174.9	18.6	8.47	85.9	-33.3	0.022	26.5	0.559	-176.9	25.9		
1	0.896	-176.7	17.6	7.61	84.0	-32.9	0.023	26.3	0.560	-178.7	25.2		
1.5	0.898	175.2	14.1	5.06	75.7	-32.1	0.025	29.9	0.558	176.0	23.1		
2	0.887	168.0	11.8	3.91	68.1	-30.7	0.029	35.2	0.547	170.9	21.3		
2.5	0.893	162.8	10.0	3.15	61.7	-29.5	0.034	35.8	0.545	166.9	18.9		
3	0.886	156.9	8.4	2.63	55.1	-28.4	0.038	35.8	0.547	162.6	16.3		
4	0.887	146.6	5.9	1.97	41.5	-26.7	0.046	33.2	0.554	154.3	13.6		
5	0.894	136.8	3.9	1.57	29.4	-25.1	0.056	29.6	0.572	146.6	11.9		
6	0.898	127.4	2.1	1.28	17.7	-23.9	0.064	25.5	0.590	139.0	10.3		
7	0.896	119.7	0.7	1.09	6.3	-22.6	0.074	20.4	0.603	131.6	8.9		
8	0.879	105.4	-0.9	0.90	-7.1	-21.1	0.088	12.4	0.594	122.7	6.6		
9	0.888	95.0	-1.7	0.82	-19.3	-20.1	0.099	4.7	0.609	113.2	6.1		
10	0.872	84.1	-2.9	0.72	-30.9	-19.2	0.110	-4.3	0.610	102.9	4.4		
11	0.880	72.4	-3.8	0.65	-42.8	-18.6	0.118	-12.9	0.629	92.6	3.8		
12	0.875	60.4	-4.8	0.58	-53.3	-18.0	0.126	-22.8	0.647	81.9	2.8		
13	0.908	52.4	-6.2	0.49	-63.4	-17.7	0.130	-31.4	0.666	71.0	2.6		
14	0.898	41.3	-7.1	0.44	-73.5	-17.2	0.138	-38.0	0.699	64.0	1.5		
15	0.888	34.1	-8.2	0.39	-80.2	-16.8	0.144	-45.6	0.734	55.9	0.5		
16	0.815	24.1	-8.9	0.36	-85.3	-16.2	0.156	-54.7	0.750	49.3	-1.7		
17	0.725	11.3	-9.9	0.32	-90.9	-15.5	0.167	-66.0	0.809	43.5	-3.1		
18	0.792	-9.8	-10.2	0.31	-95.1	-16.6	0.147	-84.8	0.652	39.7	-4.2		

Typical Noise Parameters, $V_{ds} = 4V$, $I_{ds} = 200 \text{ mA}$

Freq. GHz	F_{min} dB	Γ_{opt} Mag.	Γ_{opt} Ang.	R_n	G_s dB
0.5	0.67	0.21	155.00	2.8	20.1
1.0	0.74	0.30	164.00	2.6	18.4
2.0	0.96	0.46	-176.61	2.1	16.4
3.0	1.24	0.57	-162.19	2.8	13.9
4.0	1.44	0.62	-152.18	4.5	11.4
5.0	1.62	0.69	-135.43	10.0	10.0
6.0	1.83	0.74	-127.94	17.0	8.7
7.0	1.99	0.82	-117.20	27.7	7.7
8.0	2.21	0.71	-108.96	35.3	5.9

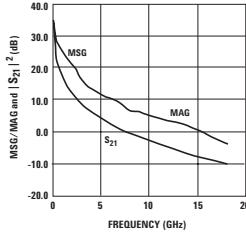


Figure 43. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 4V, 200 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{min} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Typical Scattering Parameters, $V_{ds} = 3V$, $I_{ds} = 200\text{ mA}$

Freq. GHz	S_{11}			S_{21}			S_{12}			S_{22}			MSG/MAG dB
	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	
0.1	0.867	-94.6	33.7	48.20	132.4	-36.8	0.014	45.1	0.482	-132.4	35.4		
0.2	0.894	-132.9	29.4	29.66	113.2	-34.9	0.018	28.5	0.601	-154.2	32.2		
0.3	0.899	-148.2	26.5	21.06	104.4	-34.1	0.020	23.2	0.636	-163.8	30.2		
0.4	0.896	-157.2	24.1	16.00	99.1	-34.0	0.020	23.7	0.647	-169.2	29.0		
0.5	0.892	-162.8	22.4	13.20	95.6	-33.6	0.021	24.5	0.650	-171.9	28.0		
0.6	0.910	-167.4	20.8	11.00	92.3	-33.2	0.022	22.9	0.655	-174.4	27.0		
0.7	0.906	-170.8	19.6	9.51	90.2	-33.2	0.022	23.9	0.657	-176.7	26.4		
0.8	0.902	-173.6	18.4	8.35	87.8	-33.0	0.022	24.6	0.658	-178.2	25.8		
0.9	0.907	-175.2	17.5	7.51	86.3	-32.9	0.023	27.0	0.660	-179.5	25.1		
1	0.902	-177.7	16.6	6.76	84.2	-32.5	0.024	26.9	0.659	-178.6	24.5		
1.5	0.900	174.2	13.1	4.50	76.4	-31.5	0.027	32.7	0.656	173.4	22.2		
2	0.896	168.1	10.8	3.49	69.1	-29.9	0.032	32.9	0.647	167.9	20.4		
2.5	0.896	162.3	9.0	2.82	63.0	-29.0	0.036	34.3	0.642	163.7	18.6		
3	0.887	156.7	7.4	2.35	56.9	-27.7	0.041	35.0	0.643	159.2	15.6		
4	0.890	145.7	4.9	1.76	43.8	-26.1	0.050	32.2	0.645	150.4	12.9		
5	0.898	136.3	3.0	1.41	32.1	-24.5	0.059	28.3	0.659	142.1	11.3		
6	0.896	127.4	1.3	1.16	21.6	-23.4	0.068	23.5	0.671	134.3	9.5		
7	0.904	119.4	-0.2	0.98	10.3	-22.1	0.078	17.7	0.677	126.6	8.5		
8	0.877	104.9	-1.6	0.83	-2.3	-20.7	0.092	9.0	0.651	117.0	5.9		
9	0.883	94.8	-2.4	0.76	-13.0	-19.8	0.102	1.3	0.661	107.2	5.3		
10	0.877	83.1	-3.5	0.67	-26.0	-18.9	0.113	-7.3	0.657	96.8	4.0		
11	0.875	71.7	-4.4	0.60	-36.3	-18.3	0.121	-16.6	0.670	86.7	3.1		
12	0.863	60.6	-5.4	0.54	-47.4	-17.8	0.128	-25.1	0.680	76.2	1.9		
13	0.910	51.6	-6.5	0.47	-57.9	-17.6	0.132	-33.6	0.694	65.9	2.3		
14	0.868	40.9	-7.5	0.42	-62.8	-17.2	0.138	-40.4	0.721	59.3	0.2		
15	0.863	33.4	-8.1	0.39	-74.7	-16.8	0.144	-47.6	0.748	51.3	-0.2		
16	0.835	25.2	-9.6	0.33	-78.2	-16.3	0.154	-56.8	0.758	44.9	-2.1		
17	0.720	11.2	-9.5	0.33	-90.8	-15.8	0.161	-67.6	0.818	39.4	-2.6		
18	0.780	-7.7	-11.6	0.26	-92.8	-17.0	0.142	-85.1	0.655	37.1	-5.7		

Typical Noise Parameters, $V_{ds} = 3V$, $I_{ds} = 200\text{ mA}$

Freq. GHz	F_{min} dB	Γ_{opt} Mag.	Γ_{opt} Ang.	R_n	G_a dB
0.5	0.66	0.22	147.00	2.9	20.0
1.0	0.72	0.30	160.00	2.6	18.3
2.0	0.87	0.42	-179.94	1.9	16.0
3.0	1.00	0.59	-163.63	1.6	13.7
4.0	1.32	0.63	-153.81	3.7	11.3
5.0	1.49	0.72	-135.10	10.0	9.9
6.0	1.59	0.74	-128.97	15.0	8.5
7.0	1.79	0.78	-117.68	25.1	7.6
8.0	1.96	0.70	-110.04	29.2	5.6

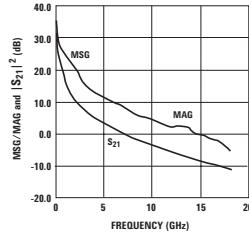


Figure 44. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 3V, 200 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{min} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NPS test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.

2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Applications Information

Description

Avago Technologies' ATF-521P8 is an enhancement mode PHEMT designed for high linearity and medium power applications. With an OIP3 of 42 dBm and a 1dB compression point of 26 dBm, ATF-521P8 is well suited as a base station transmit driver or a first or second stage LNA in a receive chain. Whether the design is for a W-CDMA, CDMA, or GSM basestation, this device delivers good linearity in the form of OIP3 or ACLR, which is required for standards with high peak to average ratios.

Application Guidelines

The ATF-521P8 device operates as a normal FET requiring input and output matching as well as DC biasing. Unlike a depletion mode transistor, this enhancement mode device only requires a single positive power supply, which means a positive voltage is placed on the drain and gate in order for the transistor to turn on. This application note walks through the RF and DC design employed in a single FET amplifier. Included in this description is an active feedback scheme to accomplish this DC biasing.

RF Input & Output Matching

In order to achieve maximum linearity, the appropriate input (Γ_i) and output (Γ_o) impedances must be presented to the device. Correctly matching from these impedances to 50Ω s will result in maximum linearity. Although ATF-521P8 may be used in other impedance systems, data collected for this data sheet is all referenced to a 50Ω system.

The input load pull parameter at 2 GHz is shown in Figure 1 along with the optimum S11 conjugate match.

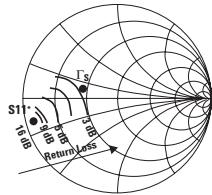


Figure 1. Input Match for ATF-521P8 at 2 GHz.

Thus, it should be obvious from the illustration above that if this device is matched for maximum return loss i.e. $S11^*$, then OIP3 will be sacrificed. Conversely, if ATF-521P8 is matched for maximum linearity, then

return loss will not be greater than 10 dB. For most applications, a designer requires VSWR greater than 2:1, hence limiting the input match close to $S11^*$. Normally, the input return loss of a single ended amplifier is not critical as most basestation LNA and driver amplifiers are in a balanced configuration with 90° (quadrature) couplers.

Proceeding from the same premise, the output match of this device becomes much simpler. As background information, it is important to note that OIP3 is largely dependant on the output match and that output return loss is also required to be greater than 10 dB. So, Figure 2 shows how both good output return loss and good linearity could be achieved simultaneously with the same impedance point.

Of course, these points are valid only at 2 GHz, and other frequencies will follow the same design rules but will have different locations. Also, the location of these points is largely due to the manufacturing process and partly due to IC layout, but in either case beyond the scope of this application note.

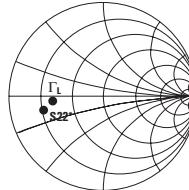


Figure 2. Output Match at 2 GHz.

Once a designer has chosen the proper input and output impedance points, the next step is to choose the correct topology to accomplish this match. For example to perform the above output impedance transformation from 50Ω to the given load parameter of $0.53\angle-176^\circ$, two possible solutions exist. The first potential match is a high pass configuration accomplished by a shunt inductor and a series capacitor shown in Figure 3 along with its frequency response in Figure 4.

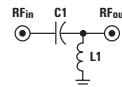


Figure 3. High Pass Circuit Topology.

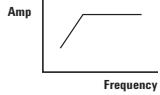


Figure 4. High Pass Frequency Response.

The second solution is a low pass configuration with a shunt capacitor and a series inductor shown in Figure 5 and 6.

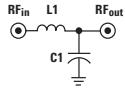


Figure 5. Low Pass Circuit Topology.

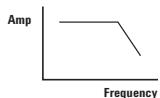


Figure 6. Low Pass Frequency Response.

The actual values of these components may be calculated by hand on a Smith Chart or more accurately done on simulation software such as ADS. There are some advantages and disadvantages of choosing a high pass versus a low pass. For instance, a high pass circuit cuts off low frequency gain, which narrows the usable bandwidth of the amplifier, but consequently helps avoid potential low frequency instability problems. A low pass match offers a much broader frequency response, but it has two major disadvantages. First it has the potential for low frequency instability, and second it creates the need for an extra DC blocking capacitor on the input in order to isolate the device gate from the preceding stages.

Figure 7 displays the input and output matching selected for ATF-521P8. In this example the input and output match both essentially function as high pass filters, but the high frequency gain of the device rolls off precipitously giving a narrow band frequency response, yet still wide enough to accommodate a CDMA or WCDMA transmit band. For more information on RF matching techniques refer to MGA-53543 application note.

Passive Bias [1]

Once the RF matching has been established, the next step is to DC bias the device. A passive biasing example is shown in Figure 8. In this example the voltage drop across resistor R3 sets the drain current (I_d) and is calculated by the following equation:

$$R_3 = \frac{V_{dd} - V_{ds}}{I_{ds} + I_{bb}} \quad (1)$$

where,

V_{dd} is the power supply voltage;

V_{ds} is the device drain to source voltage;

I_{ds} is the device drain to source current;

I_{bb} for DC stability is 10X the typical gate current;

A voltage divider network with R1 and R2 establishes the typical gate bias voltage (V_g).

$$R_1 = \frac{V_g}{I_{bb}} \quad (2)$$

$$R_2 = \frac{(V_{dd} - V_g) \times R_1}{V_g} \quad (3)$$

Often the series resistor, R4, is added to enhance the low frequency stability. The complete passive bias example may be found in reference [1].

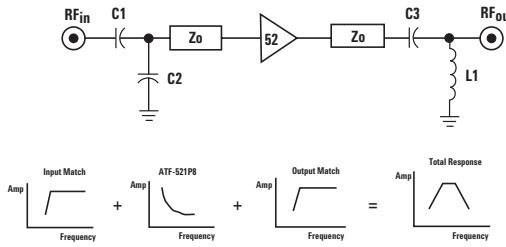


Figure 7. Input and Output Match for ATF-521P8 at 2 GHz.

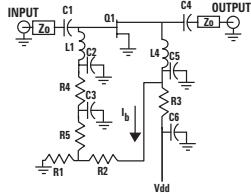


Figure 8. Passive Biasing.

Active Bias^[2]

Due to very high DC power dissipation and small package constraints, it is recommended that ATF-521P8 use active biasing. The main advantage of an active biasing scheme is the ability to hold the drain to source current constant over a wide range of temperature variations.

A very inexpensive method of accomplishing this is to use two PNP bipolar transistors arranged in a current mirror configuration as shown in Figure 9. Due to resistors R1 and R3, this circuit is not acting as a true current mirror, but if the voltage drop across R1 and R3 is kept identical then it still displays some of the more useful characteristics of a current mirror. For example, transistor Q1 is configured with its base and collector tied together. This acts as a simple PN junction, which helps temperature compensate the Emitter-Base junction of Q2.

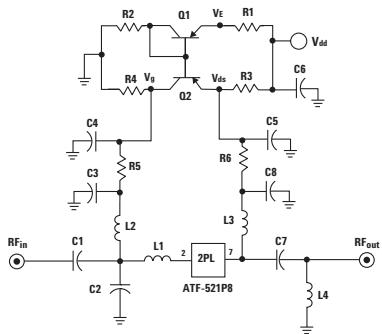


Figure 9. Active Bias Circuit.

To calculate the values of R1, R2, R3, and R4 the following parameters must be known or chosen first:

I_{ds} is the device drain-to-source current;

I_r is the Reference current for active bias;

V_{dd} is the power supply voltage available;

V_{ds} is the device drain-to-source voltage;

V_g is the typical gate bias;

V_{be1} is the typical Base-Emitter turn on voltage for Q1 & Q2;

Therefore, resistor R3, which sets the desired device drain current, is calculated as follows:

$$R3 = \frac{V_{dd} - V_{ds}}{I_{ds} + I_{c2}} \quad (4)$$

where,

I_{c2} is chosen for stability to be 10 times the typical gate current and also equal to the reference current I_r .

The next three equations are used to calculate the rest of the biasing resistors for Figure 9. Note that the voltage drop across R1 must be set equal to the voltage drop across R3, but with a current of I_r :

$$R1 = \frac{V_{dd} - V_{ds}}{I_r} \quad (5)$$

R2 sets the bias current through Q1.

$$R2 = \frac{V_{ds} - V_{be1}}{I_r} \quad (6)$$

R4 sets the gate voltage for ATF-521P8.

$$R4 = \frac{V_g}{I_{c2}} \quad (7)$$

Thus, by forcing the emitter voltage (V_e) of transistor Q1 equal to V_{ds} , this circuit regulates the drain current similar to a current mirror. As long as Q2 operates in the forward active mode, this holds true. In other words, the Collector-Base junction of Q2 must be kept reversed biased.

PCB Layout

A recommended PCB pad layout for the Leadless Plastic Chip Carrier (LPCC) package used by the ATF-521P8 is shown in Figure 10. This layout provides plenty of plated through hole vias for good thermal and RF grounding. It also provides a good transition from microstrip to the device package. For more detailed dimensions refer to Section 9 of the data sheet.



Figure 10. Microstripline Layout.

RF Grounding

Unlike SOT packages, ATF-521P8 is housed in a leadless package with the die mounted directly to the lead frame or the belly of the package shown in Figure 11.

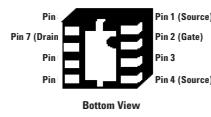


Figure 11. LPCC Package for ATF-521P8.

This simplifies RF grounding by reducing the amount of inductance from the source to ground. It is also recommended to ground pins 1 and 4 since they are also connected to the device source. Pins 3, 5, 6, and 8 are not connected, but may be used to help dissipate heat from the package or for better alignment when soldering the device.

This three-layer board (Figure 12) contains a 10-mil layer and a 52-mil layer separated by a ground plane. The first layer is Getek RG200D material with dielectric constant of 3.8. The second layer is for mechanical rigidity and consists of FR4 with dielectric constant of 4.2.

High Linearity Tx Driver

The need for higher data rates and increased voice capacity gave rise to a new third generation standard known as Wideband CDMA or UMTS. This new standard requires higher performance from radio components such as higher dynamic range and better linearity. For example, a WCDMA waveform has a very high peak to average ratio which forces amplifiers in a transmit chain to have very good Adjacent Channel Leakage power Ratio or ACLR, or else operate in a backed off mode. If the amplifier is not backed off then the waveform is compressed and the signal becomes very nonlinear.

This application example presents a highly linear transmit driver for use in the 2.14GHz frequency range. Using the RF matching techniques described earlier, ATF-521P8 is matched to the following input and output impedances:

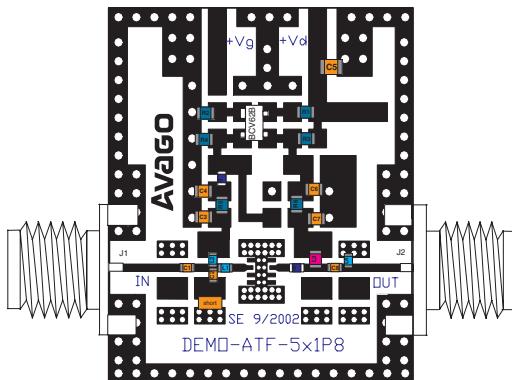


Figure 12. ATF-521P8 demoboard.

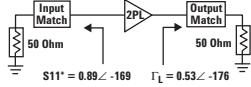


Figure 13. ATF-521P8 Matching.

As described previously the input impedance must be matched to S_{11}^* in order to guarantee return loss greater than 10 dB. A high pass network is chosen for this match. The output is matched to Γ_L with another high pass network. The next step is to choose the proper DC biasing conditions. From the data sheet, ATF-521P8 produces good linearity at a drain current of 200mA and a drain to source voltage of 4.5V. Thus to construct the active bias circuit described, the following parameters are given:

$$I_{ds} = 200 \text{ mA}$$

$$I_h = 10 \text{ mA}$$

$$V_{dd} = 5 \text{ V}$$

$$V_{ds} = 4.5 \text{ V}$$

$$V_g = 0.62 \text{ V}$$

$$V_{be1} = 0.65 \text{ V}$$

Using equations 4, 5, 6, and 7, the biasing resistor values are calculated in column 2 of table 1, and the actual values used are listed in column 3.

Table 1. Resistors for Active Bias.

Resistor	Calculated	Actual
R1	50Ω	49.9Ω
R2	385Ω	383Ω
R3	2.38Ω	2.37Ω
R4	62Ω	61.9Ω

The entire circuit schematic for a 2.14 GHz Tx driver amplifier is shown below in Figure 14. Capacitors C4, C5, and C6 are added as a low frequency bypass. These terminate second order harmonics and help improve linearity. Resistors R5 and R6 also help terminate low frequencies, and can prevent resonant frequencies between the two bypass capacitors.

Performance of ATF-521P8 at 2140 MHz

ATF-521P8 delivers excellent performance in the WCDMA frequency band. With a drain-to-source voltage of 4.5V and a drain current of 200 mA, this device has 16.5 dB of gain and 1.55 dB of noise figure as shown in Figure 15.

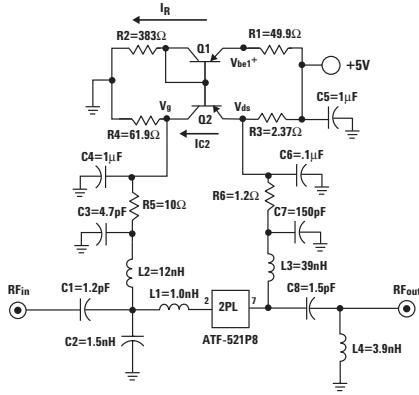


Figure 14. 2140 MHz Schematic.

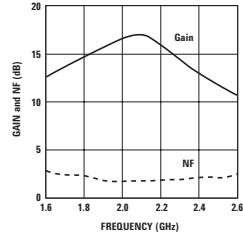


Figure 15. Gain and Noise Figure vs. Frequency.

Input and output return loss are both greater than 10 dB. Although somewhat narrowband, the response is adequate in the frequency range of 2110 MHz to 2170 MHz for the WCDMA downlink. If wider band response is need, using a balanced configuration improves return loss and doubles OIP3.

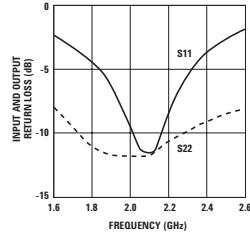


Figure 16. Input and Output Return Loss vs. Frequency.

Perhaps the most critical system level specification for the ATF-521P8 lies in its distortion-less output power. Typically, amplifiers are characterized for linearity by measuring OIP3. This is a two-tone harmonic measurement using CW signals. But because WCDMA is a modulated waveform spread across 3.84 MHz, it is difficult to correlated good OIP3 to good ACLR. Thus, both are measured and presented to avoid ambiguity.

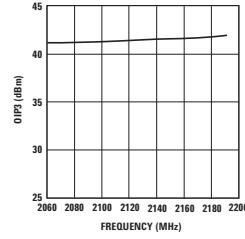


Figure 17. OIP3 vs. Frequency in WCDMA Band (Pout = 12 dBm).

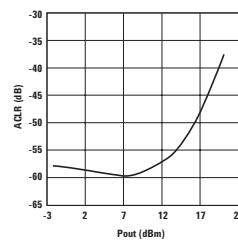


Figure 18. ACLR vs. Pout at 5 MHz Offset.

Table 2. 2140 MHz Bill of Material.

C1=1.2 pF	Phycomp 0402CG129C9B200
C2,C8=1.5 pF	Phycomp 0402CG159C9B200
C3=4.7 pF	Phycomp 0402CG479C9B200
C4,C6=.1 μ F	Phycomp 06032F104M8B200
C5=1 μ F	AVX 0805ZC105KATZA
C7=150 pF	Phycomp 0402CG151J9B200
L1=1.0 nH	TOKO LL1005-FH1n0S
L2=12 nH	TOKO LL1005-F512N
L3=39 nH	TOKO LL1005-F539
L4=3.9 nH	TOKO LL1005-FH3N9S
R1=49.9 Ω	Rohm RK73H1J49R9F
R2=383 Ω	Rohm RK73H1J3830F
R3=2.37 Ω	Rohm RK73H1J2R37F
R4=61.9 Ω	Rohm RK73H1J61R9F
R5=10 Ω	Rohm RK73H1J10R0F
R6=1.2 Ω	Rohm RK73H1J1R21F
Q1, Q2	Philips BCV62B
J1, J2	142-0701-851

Using the 3GPP standards document Release 1999 version 2002-6, the following channel configuration was used to test ACLR. This table contains the power levels of the main channels used for Test Model 1. Note that the DPCH can be made up of 16, 32, or 64 separate channels each at different power levels and timing offsets. For a listing of power levels, channelization codes and timing offset see the entire 3GPP TS 25.141 V3.10.0 (2002-06) standards document at: <http://www.3gpp.org/specs/specs.htm>

Table 3. ACLR Channel Power Configuration.

3GPP TS 25.141 V3.10.0 (2002-06)	Type	Pwr (dB)
P-CCPCH+SCH		-10
Primary CPICH		-10
PICH		-18
S-CCPCH containing PCH (SF=256)		-18
DPCH-64ch (SF=128)		-1.1

Thermal Design

When working with medium to high power FET devices, thermal dissipation should be a large part of the design. This is done to ensure that for a given ambient temperature the transistor's channel does not exceed the maximum rating, T_{ch} , on the data sheet. For example, ATF-521P8 has a maximum channel temperature of 150°C and a channel to board thermal resistance of 45°C/W, thus the entire thermal design hinges from these key data points. The question that must be answered is whether this device can operate in a typical environment with ambient temperature fluctuations from -25°C to 85°C. From Figure 19, a very useful equation is derived to calculate the temperature of the channel for a given ambient temperature. These calculations are all incorporated into Avago Technologies AppCAD.

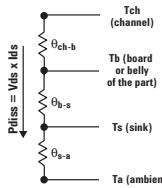


Figure 19. Equivalent Circuit for Thermal Resistance.

Hence very similar to Ohms Law, the temperature of the channel is calculated with equation 8 below.

$$T_{ch} = P_{diss} (\theta_{ch-b} + \theta_{b-s} + \theta_{s-a}) + T_{amb} \quad (8)$$

If no heat sink is used or heat sinking is incorporated into the PCB board then equation 8 may be reduced to:

$$T_{ch} = P_{diss} (\theta_{ch-b} + \theta_{b-a}) + T_{amb} \quad (9)$$

where,

θ_{b-a} is the board to ambient thermal resistance;

θ_{ch-b} is the channel to board thermal resistance.

The board to ambient thermal resistance thus becomes very important for this is the designer's major source of heat control. To demonstrate the influence of θ_{b-a} thermal resistance is measured for two very different scenarios using the ATF-521P8 demoboard. The first case is done with just the demoboard by itself. The second case is the ATF demoboard mounted on a chassis or metal casing, and the results are given below:

Table 4. Thermal resistance measurements.

ATF Demoboard	θ_{b-a}
PCB 1/8" Chassis	10.4°C/W
PCB no HeatSink	32.9°C/W

Therefore calculating the temperature of the channel for these two scenarios gives a good indication of what type of heat sinking is needed.

Case 1: Chassis Mounted @ 85°C

$$\begin{aligned} T_{ch} &= P \times (\theta_{ch-b} + \theta_{b-a}) + T_{amb} \\ &= .9W \times (45+10.4)^\circ\text{C}/\text{W} + 85^\circ\text{C} \end{aligned}$$

$$T_{ch} = 135^\circ\text{C}$$

Case 2: No Heatsink @ 85°C

$$\begin{aligned} T_{ch} &= P \times (\theta_{ch-b} + \theta_{b-a}) + T_{amb} \\ &= .9W \times (45+32.9)^\circ\text{C}/\text{W} + 85^\circ\text{C} \end{aligned}$$

$$T_{ch} = 155^\circ\text{C}$$

In other words, if the board is mounted to a chassis, the channel temperature is guaranteed to be 135°C safely below the 150°C maximum. But on the other hand, if no heat sinking is used and the θ_{b-a} is above 27°C/W (32.9°C/W in this case), then the power must be derated enough to lower the temperature below 150°C. This can be better understood with Figure 20 below. Note power is derated at 13 mW/°C for the board with no heat sink and no derating is required for the chassis mounted board until an ambient temperature of 100°C.

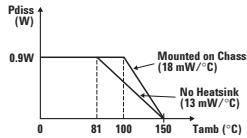


Figure 20. Derating for ATF-521P8.

Thus, for reliable operation of ATF-521P8 and extended MTBF, it is recommended to use some form of thermal heatsinking. This may include any or all of the following suggestions:

- Maximize vias underneath and around package;
- Maximize exposed surface metal;
- Use 1 oz or greater copper clad;
- Minimize board thickness;
- Metal heat sinks or extrusions;
- Fans or forced air;
- Mount PCB to Chassis.

Summary

A high linearity Tx driver amplifier for WCDMA has been presented and designed using Agilent's ATF-521P8. This includes RF, DC and good thermal dissipation practices for reliable lifetime operation. A summary of the typical performance for ATF-521P8 demoboard at 2140 MHz is as follows:

Demo Board Results at 2140 MHz

Gain	16.5 dB
OIP3	41.2 dBm
ACLR	-58 dBc
P1dB	24.8 dBm
NF	1.55 dB

References

- [1] Ward, A. (2001) **Avago Technologies ATF-54143 Low Noise Enhancement Mode Pseudomorphic HEMT in a Surface Mount Plastic Package**, 2001 [Internet], Available from:
<http://www.avagotech.com>
- [2] **Biassing Circuits and Considerations for GaAs MESFET Power Amplifiers**, 2001 [Internet], Available from:
http://www.rf-solutions.com/pdf/AN-0002_ajp.pdf
[Accessed 22 August, 2002]

Device Models

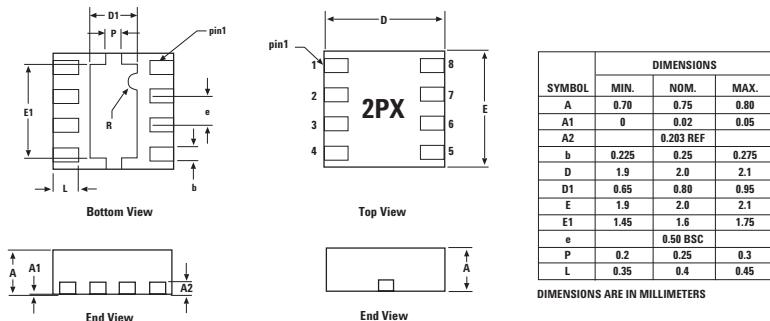
Refer to Avago Technologies' Web Site:

www.avagotech.com

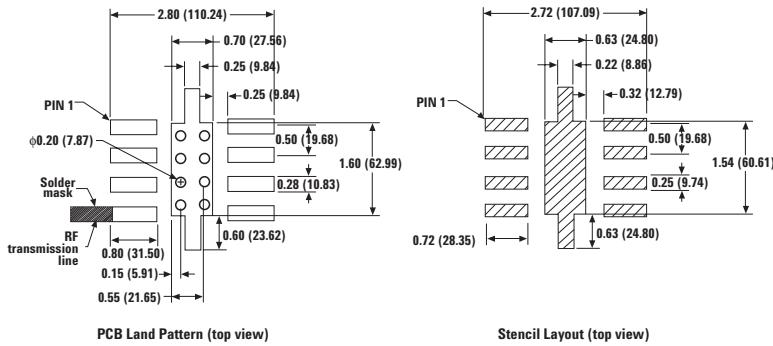
Ordering Information

Part Number	No. of Devices	Container
ATF-521P8-TR1	3000	7" Reel
ATF-521P8-TR2	10000	13" Reel
ATF-521P8-BLK	100	antistatic bag

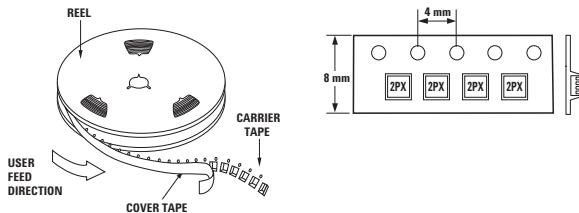
2x2 LPCC (JEDEC DFP-N) Package Dimensions



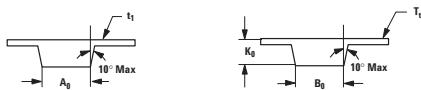
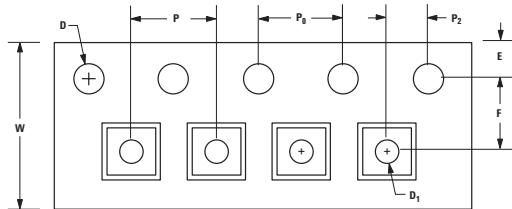
PCB Land Pattern and Stencil Design



Device Orientation



Tape Dimensions



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (inches)
CAVITY	LENGTH	A ₀	2.30 ± 0.05	0.091 ± 0.004
	WIDTH	B ₀	2.30 ± 0.05	0.091 ± 0.004
	DEPTH	K ₀	1.00 ± 0.05	0.039 ± 0.002
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D ₁	1.00 ± 0.25	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.060 ± 0.004
	PITCH	P ₀	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30 8.00 - 0.10 0.254 ± 0.02	0.315 ± 0.012 0.315 ± 0.004 0.010 ± 0.0008
	THICKNESS	t ₁		
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	t ₁	0.062 ± 0.001	0.0025 ± 0.0004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P ₂	2.00 ± 0.05	0.079 ± 0.002

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