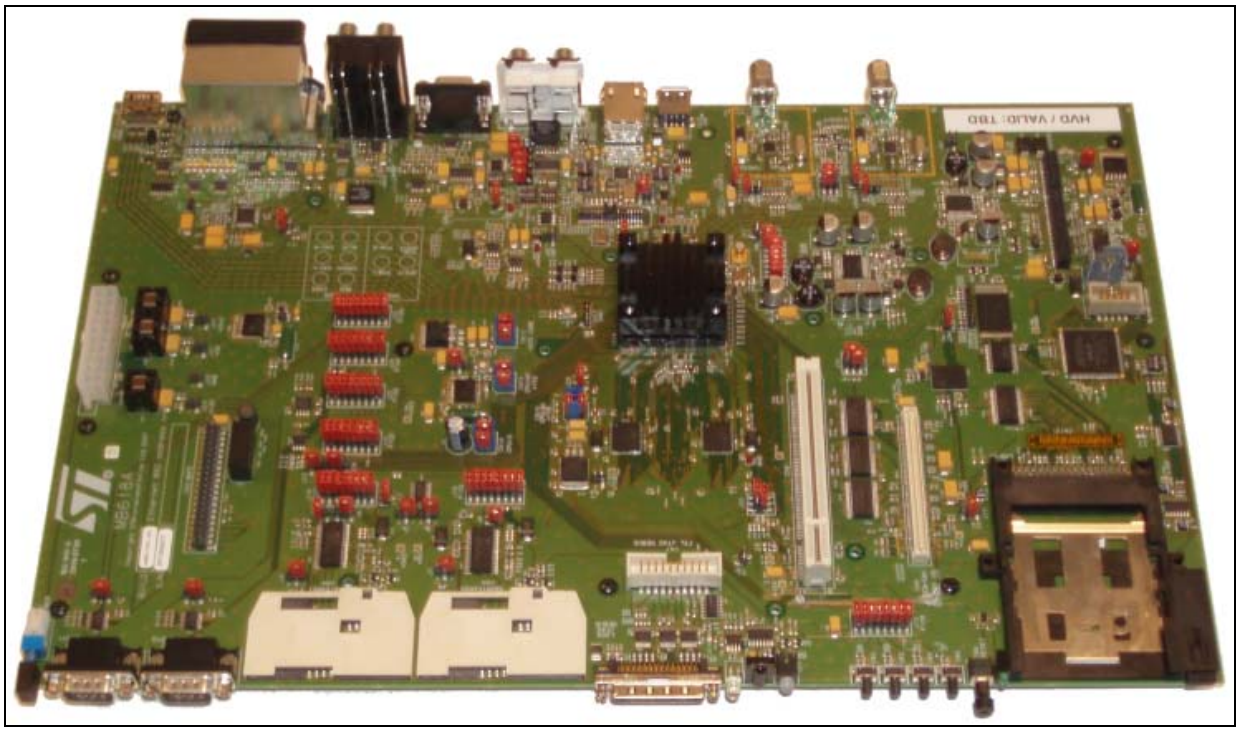
STi7111-MBoard

Evaluation board for low cost HD TV decoder using the STi7111 SoC



Features

- Interfaces supporting digital audio and video applications, including:
  - HDMI output
  - I^2C
  - Smartcard
  - Infrared receiver
  - RS232 (UART)
  - MII Ethernet and USB
  - S/PDIF output
  - SD and HD video
  - 2x ST6110a tuner front ends
  - On-board 64-Mbyte NAND, NOR and serial Flash memory
  - PCI capability
  - DiSEqC 2.0^{TM} interfaces and FSK modem for FTM
  - 1x NIM2 interface
  - DVB-CI
  - STEM
  - LMI 0 SDRAM (512 MBytes)
  - Dual SCART
- Diagnostic support:
  - JTAG on-chip low voltage differential signalling (LVDS)
- Power isolation and low power consumption

Description

The STi7111-MBoard provides a set-top-box application development platform for low-end HDTV applications using the STi7111 SoC.

The STi7111-MBoard, can be used for:

- STi7111 validation
- STi7111 demonstration
- Software application development

Contents

1 Introduction

The STi7111-MBoard has been designed and engineered to provide a high definition set-top box product.

The STi7111-MBoard consists of:

- an MB618 STi7111 evaluation board
- an ATX power supply, described in *Section 3.2: Power supply on page 9*

A block diagram of the STi7111-MBoard is shown in *Section 3.1: System block diagram on page 9*.

The STi7111 SoC contains a master ST40-300 core and two ST231 cores for audio/video decoding. These support the embedded STB, cable modem, networking and applications. For more information on the SoC, see the *STi7111 datasheet* (ADCS 8065030).

1.1 Target audience

The target audience includes the following:

- software application and validation teams
- marketing
- board manufacturing services (debug)
- field application engineers
- other electronic manufacturers (OEM)

1.2 References

STi7111 datasheet (ADCS 8065030)

MB618 STi7111-Mboard EPLD definition and equation (ADCS 8088375)

ST40 Micro Toolset user manual (ADCS 7379953)

ST Micro Connect 2 datasheet (ADCS 7912386)

Migrating to the ST Micro Connect 2 application note (ADCS 8042002)

2 System overview

Figure 1. STi7111-MBoard debug setup and interconnection block diagram

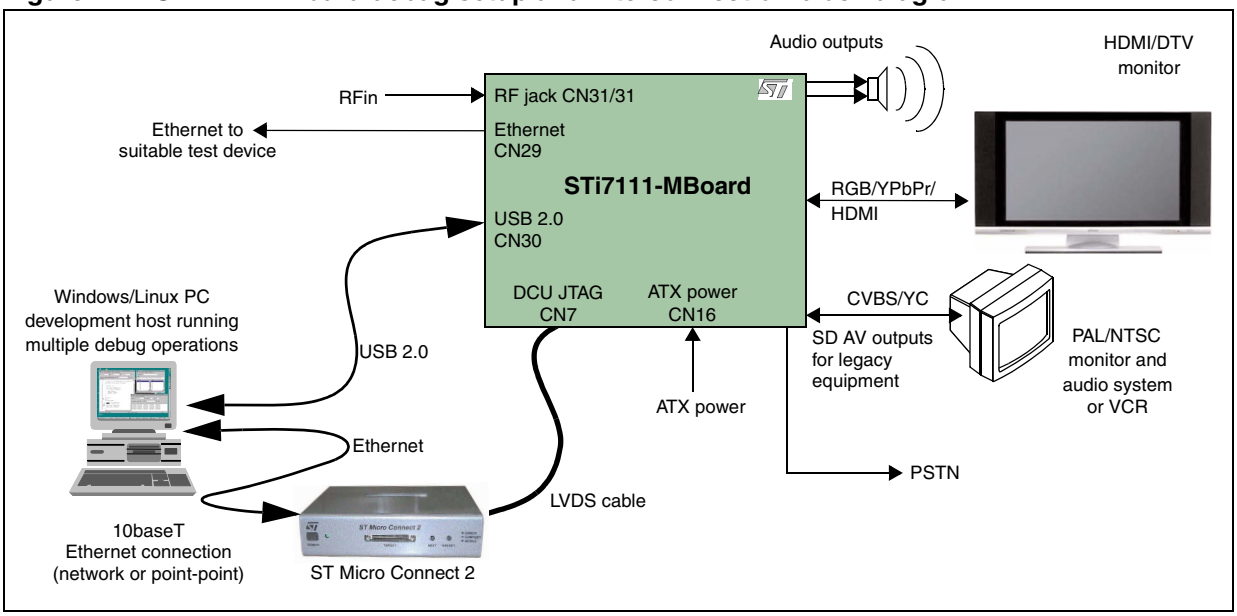


Table 1. System requirements for using the ST40 Toolset on the STi7111-MBoard

Component	Description	Supplier	Part number
PC/Linux development host	Supported configuration: Windows 2000/XP OS Pentium class PC, RedHat Linux Enterprise V3.0 or higher for Linux development (minimum Pentium II processor at > 300 MHz with 32 Mbytes of RAM, >120 Mbytes disk free space).	Any PC supplier	Not applicable
STi7111-MBoard	STi7111 evaluation and software application platform.	STMicroelectronics	STi7111-MBoard
ST Micro Connect 2	Hardware interface from Ethernet to motherboard under test.	STMicroelectronics	STMC2-20/40/200
ST40 Micro Toolset	Embedded core development tools.	STMicroelectronics	Contact your local ST sales office
ST40 STLinux	ST40 STLinux distribution and development environment.	STMicroelectronics from www.stlinux.com	Not applicable
HDMI/DVi monitor	HD ready monitor	Any OEM monitor	Not applicable
PAL/NTSC TV	(Legacy) Monitor with SD, composite video input, SCART, S-Video or VGA	Any OEM monitor	Not applicable
Reference software	STi7111 software modules, STAPI tree for DVB	STMicroelectronics	STi7111-STDVB
Packet injector and front-end	Tuner, QPSK demodulation and FEC for satellite bitstream reception, development board with STEM or NIM interface	STMicroelectronics	PI-NIM, STV6130-NIM

2.1 Equipment and software

The following are required:

- an ST Micro Connect 2 (STMC2) with an LVDS cable to link the STMC2 to the STi7111-MBoard
- a Windows/Linux capable PC
- Ethernet cable to link the PC to the STMC2 and STi7111-MBoard
- ST40 Micro Toolset R4.0.2 or later

The STMC2 is a host-target interface that connects to the STi7111-MBoard's JTAG port and provides host software with the ability to start up the board, download programs and debug them on the target. The STMC2 can support multiple concurrent debuggers, connecting to the different cores on the STi7111 chip.

For further information on STMC2, please refer to *ST Micro Connect 2 datasheet* (ADCS 7912386). How to carry out multicore debugging is described in the *Migrating to the ST Micro Connect 2 application note* (ADCS 8042002).

For information on the ST40 toolset, refer to the *ST40 Micro Toolset user manual* (ADCS 7379953).

2.2 Electrostatic discharge (ESD) protection

If the board is used in a standalone manner on the workbench, it must be in a static-free environment, whilst maintaining antistatic precautions at all times. For example, the board must be placed on a grounded antistatic mat and the user must always wear the wrist strap connected to the mat.

3 MB618 STi7111-MBoard evaluation board

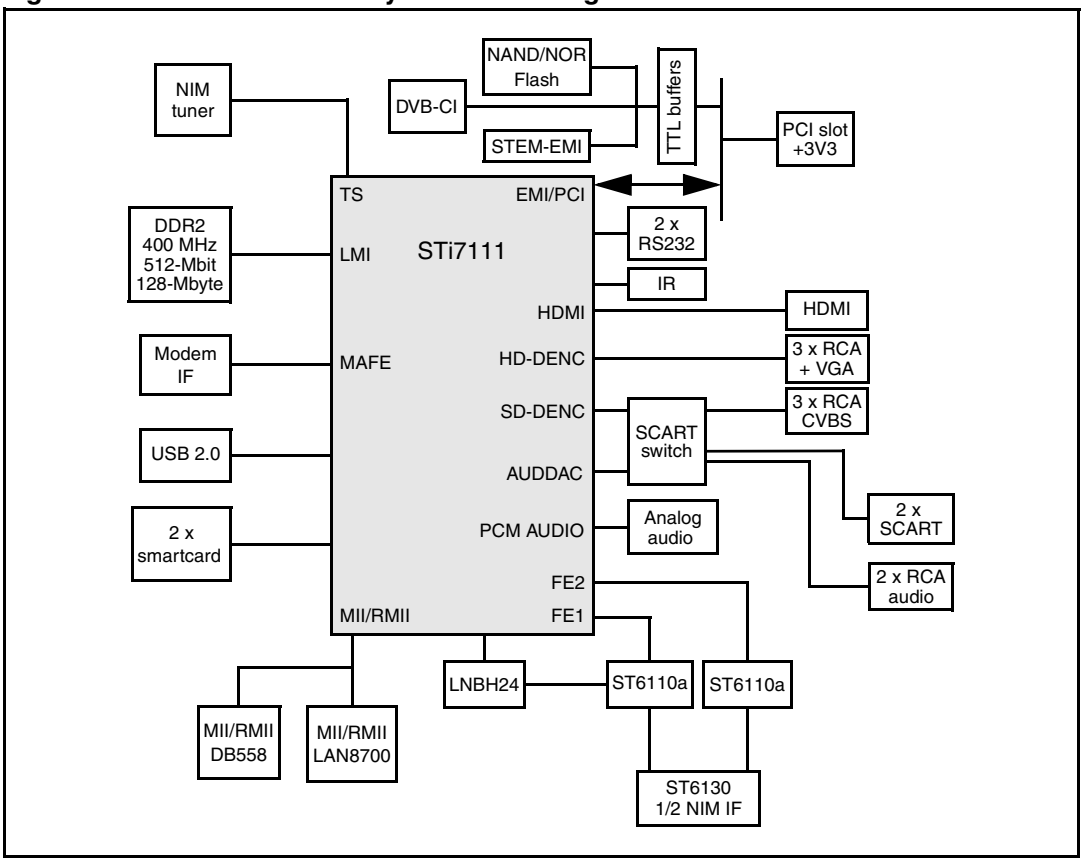
The STi7111-MBoard includes the following subsystems and functions:

- power supplies
- reset
- memory interfaces, including:
  - local memory interface (LMI)
  - external memory interface (EMI)
- SATA and ATAPI interfaces
- interfaces:
  - tuner interface
  - USB
  - MII/RMII Ethernet
  - UART RS232
  - modem analog front end (MAFE)
  - DVB-CI/POD stream
  - smart cards
  - I^2C
  - direct access arrangement (DAA) connector
  - infrared receiver
  - NIM2 interface
- video I/O
- PIO
- clocks
- interrupts
- debug facilities

3.1 System block diagram

A block diagram of the STi7111-MBoard is shown in *Figure 2*.

Figure 2. STi7111-MBoard system block diagram



3.2 Power supply

An ATX power supply provides +12V, +5V and +3V3 to the MB618. Other voltages are derived from on-board voltage regulators and converters.

The STi7111 core implements a separate power supply to the rest of the board. An isolated voltage (CPUINT) varies from 1.2V +/- 10% for example 1.1V and 1.3V. The standard voltage supply tolerance for the STi7111 is +/- 5%, but the voltage supply variation, as a worst case for validation is +/- 10%.

An isolated 3V3 voltage supply, CPUIO, is provided for the STi7111 I/O, but the LMI I/O interface has a regulated 1V8 voltage supply, CPULMI.

All other board power supplies are shared. Preparation of processor supply isolation, allows for an external source to be connected.

Precautionary measures must be undertaken to protect the STi7111 against 5V input signals, whilst connecting any 5V device.

All power rails incorporate test points for manufacturing test purposes.

3.3 Reset control

The reset sources are:

- power on reset
- front panel, push button reset
- JTAG/TAP debug reset
- watchdog reset out

An EPLD controls the overall board reset, from these sources.

The reset signals are managed by the PLD audio.

The output reset signals are:

- NAND Flash memory
- NIM interfaces
- SPDIF input interface
- Ethernet PHY
- DVB-CI

3.4 Clocks

The STi7111 has two separate clock inputs.

- The SYSACLKIN/SYSACLKOSC pair is for the system clock. With the internal VCXO feature, this pair of clock inputs is fed by a 30 MHz crystal. The 30 MHz clock input is selected by jumpers.
- The SYSBCLKIN/SYSBCLKOSC pair, mainly for USB features, is from a 30 MHz crystal.

RTCCLKIN (real time clock) is not supported on this chip.

SYSCLKOUT, programmable output clock pin for debug, is available on TP40.

For more information, see the *STi7111 datasheet* (ADCS 8065030).

3.5 Interrupts

The interrupt sources on the board are:

- two STEM interrupts (STEM Int0 and STEM Int1)
- MII/RMII Ethernet interrupts
- MAFE
- SPDIF
- SCART
- DVB-CI
- I^2C PIO expander

Interrupt handling is performed on-board. For further information on interrupts, please refer to *MB618 STi7111-MBoard EPLD definition and equation document* (ADCS 8088375).

3.6 Debug

Software debugging is performed through a standard JTAG connection. Debug is provided using the STMC2, supported through the LVDS connection interface. The STi7111-MBoard has a common JTAG port for all the embedded cores.

Logic analyzer access for EMI signals (address/data/control) is provided by a STEM logic analyzer module (DB493).

EMI signals that are not provided through the DB493 STEM module, are accessible on test points.

3.7 Memory interfaces

The STi7111 provides two host memory interfaces:

- local memory interface (LMI) provides on-board local DDRAM
- external memory interface (EMI) provides access to on-board NAND/NOR Flash and peripheral devices

3.7.1 LMI

The STi7111 CPU validation board has one independent LMI. The memory capacity of the LMI is up to 512-Mbyte DDR2 or SDRAM (400 MHz), that can be organized in 1 x 32-bit or 2 x 16-bit chips.

DDR2 SDRAM can self refresh.

3.7.2 EMI

The STi7111 EMI provides:

- NAND or NOR Flash access through the board
- DVB-CI
- peripheral expansion interface

Up to five banks are available. Each bank has a dedicated strobe timing configuration and chip select signal. The EMI memory map is shown in *Table 2*.

Table 2. EMI memory map

Bank	Function
Bank 0 (boot area)	NAND or NOR Flash
Bank 1	STEM-EMI
Bank 2	DVB-CI
Bank 3	Boards register/STEM
Bank 4	PCI

3.8 Interfaces

The following STi7111 SoC interfaces are accessible through connectors on the board:

- tuner interface
- one USB2.0
- one MII/RMII Ethernet
- two serial RS232
- MAFE interface
- DVB-CI/POD stream interface
- smartcards
- I^2C interface
- DAA interface
- infrared
- NIM
- PCI interface

3.8.1 Tuner interface

The STi7111 incorporates two internal DVB-S demodulators (dual DVB-S1 or DVB-S2 and one DVB-S1) and supports one separate bi-directional transport stream.

- On Revision D and later boards only, the demodulators are fully supported using two STV6110a (provision to support the STV6130 wide band tuner, is provided on one FE). The LNB circuit is provided by the LNBH23/4 device.
- The transport stream interface (TS) is supported through a single ST-NIM2 interface. This provides power and LNB stream signals to the network interface module.
- The transport signals for the STi7111 are taken to the new mini standard TS TTL headers. The TTL connectors allow general transport stream, based front ends to connect directly to the STi7111 TS inputs.
- Both tuner I^2C buses are connected to their respective tuner and test GUI headers.
- Diseq2 is supported by the STi7111 for both integrated tuner front ends.

Note: I^2C signals are buffered for signal integrity.

3.8.2 USB2.0 host

The STi7111 supports one USB2.0 host interface. A USB power controller device supplies power to the USB interface.

3.8.3 MII/RMII Ethernet

The STi7111 has one MII/RMII Ethernet interface. An on-board LAN8700 device supports the validation of this interface. Support for the DB558 or similar daughter board is also provided for evaluation of other Physical Interfaces (PHYs).

LED output functions are user selectable. Up to two LED functions can be selected at one time. The LED output functions are:

- activity
- full duplex
- 10BASE T or 100BASE TX Ethernet transmit protocol

3.8.4 Serial RS232 UART interfaces

Two RS232 interfaces are provided. RX, TX, RTS and CTS signals are supported on both connectors.

Both ports are connected through PIO jumpers, which ensures that all of the ASC ports of the STi7111, are available for validation. These ports are connected to two of the STi7111 ASC ports. UART2 and UART3 on the PIO pins of STi7111 are connected to these two ASC ports by default.

3.8.5 MAFE interface

The MAFE interface is supported by an IDC header for connection to an external MAFE board.

3.8.6 DVB-CI stream interface

DVB-CI support is provided. The STi7111 primary tuner stream is fed to TSOUT. This output is routed to DVB-CI slots, which in turn output a decoded CA stream to TSIN.

3.8.7 Smartcards

Two smartcard slots are provided on the board. The ST8024 is used, which is a low cost analog interface for asynchronous 3V and 5V smart cards. Banking or ICAM format is supported.

3.8.8 I^2C interfaces

The STi7111 supports five serial I^2C buses. These are configured as:

- SPI bus connected to a SPI Flash device (M25P32)
- I^2C bus connected to tuner 0
- I^2C bus connected to tuner 1
- I^2C bus connected to NIM tuner, and associated LNB's
- I^2C bus connected to the HDMI, EEPROM

3.8.9 DAA interface

This interface is supported by a DAA header (CN17) for connection to an external DAA module.

3.8.10 NIM

The NIM has a single tuner with all RF and demodulator electronics on-board.

The NIM connector provides the NIM board with all required power supplies, LNB, I^2C and transport stream signals. The RF connector is mounted directly on the NIM.

The STi7111-MBoard supports one NIM2 compatible slot. The NIM2 format uses a 2 x 42-pin connector to provide additional voltage levels required for new technologies. The NIM2 format is backwards compatible (that is, a NIM1 daughterboard can be fitted onto a NIM2 motherboard).

3.8.11 IrDA receiver module

One infrared (IR) receiver/transmitter module, with a frequency of 36 Hz is supported.

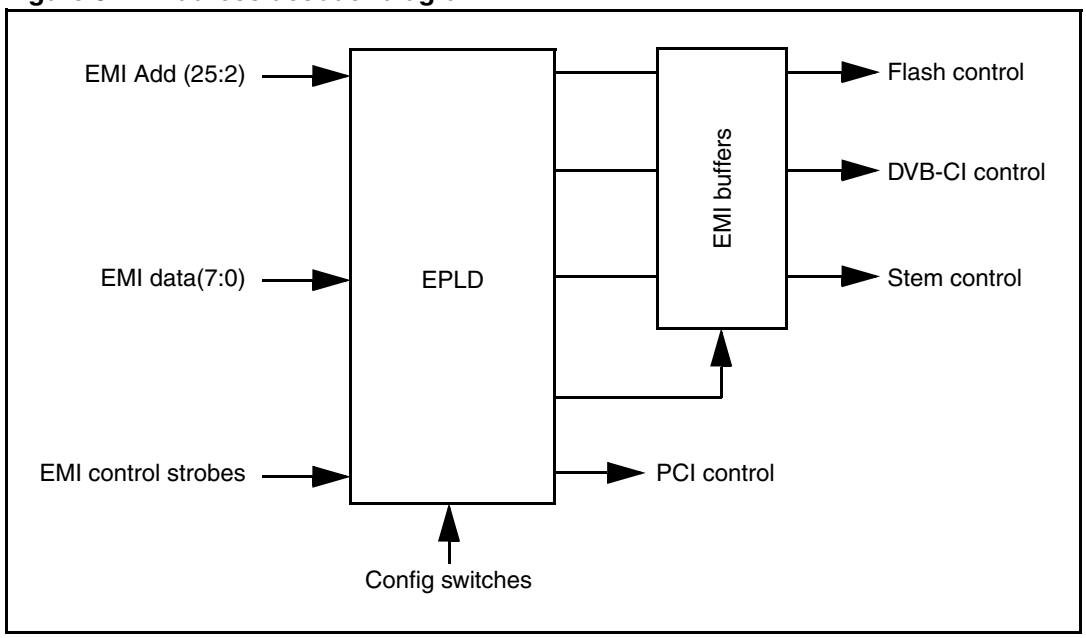
The IR device is located on the front panel of the box, and consist of an IR receiver and an IR transmitter.

3.8.12 PCI

The PCI interface, which is shared with the EMI bus, supports a single +3V, 32-bit 33 MHz PCI card slot.

Note: SW16:3 is PCI enable, see Section B.3: Switches on page 62. When SW16:3 is On, EMI loading is reduced as EMI buffers are disabled. When the switch is Off, EMI buffers are enabled.

Figure 3. Address decoder diagram



3.9 Transport stream and DVB-CI multiplexing

All transport stream signals are routed through an EPLD, which allows the routing of any source transport stream signals to any destination transport stream signals, individually or in parallel. Routing configurations are coded in the EPLD and options are chosen using the switches connected to the EPLD, see the *MB618 STi7111-MBoard EPLD definition and equation document* (ADCS 8088375).

Transport stream multiplexer settings for Revision A to C boards are listed in *Table 3* and the settings for Revision D and later boards are listed in *Table 4*.

Figure 4. Transport stream and DVB-CI block diagram

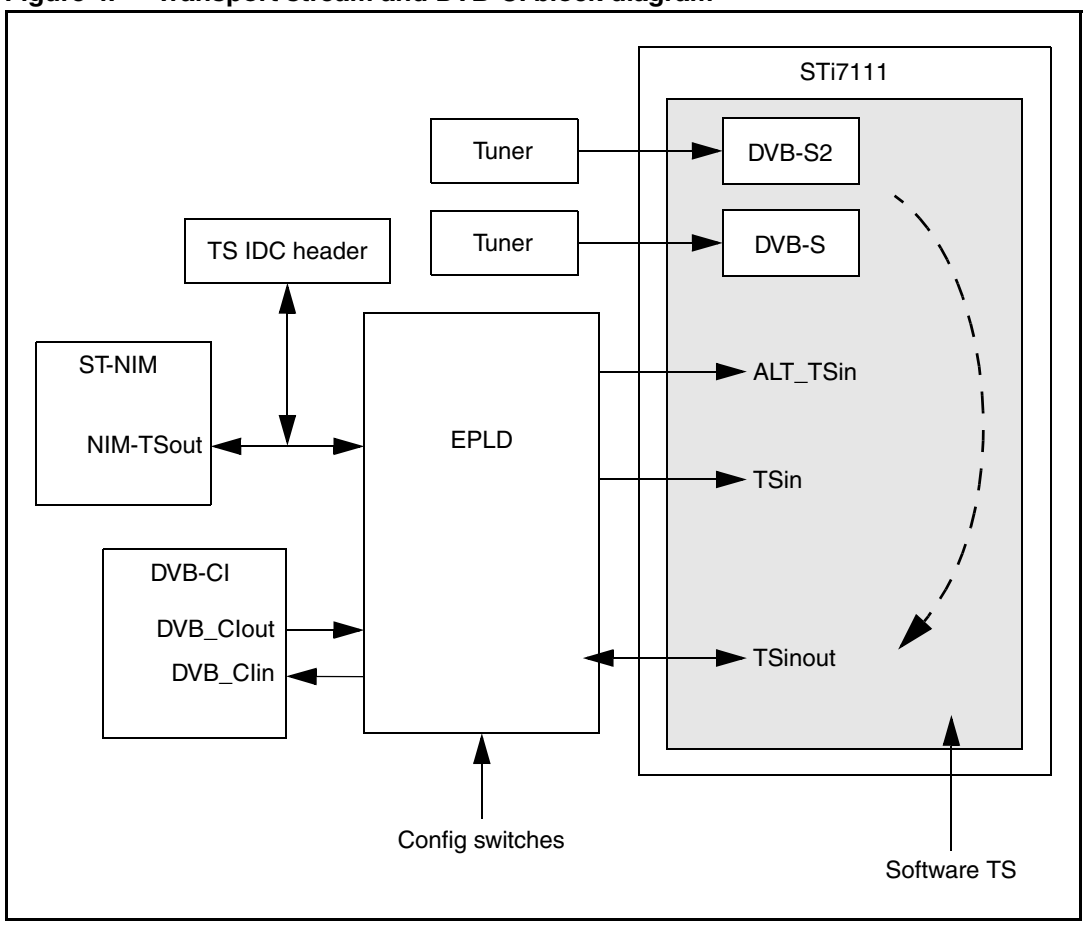


Table 3. Transport stream multiplexer settings for Rev A to C boards

Hardware control		Software control			Transport steam configuration setting
SW7:1	SW7:0	Conf2	Conf1	Conf0	
On	On	0	0	0	DVB_CIout connected toTS0inout NIM-TS0out connected to DVB_CIin TS0In tri-state ALT_TS0in tri-state
On	Off	0	0	1	DVB-CIout connected toTS0in TS0inout connected to DVB-CIin ALT_TS0in tri-state

Table 3. Transport stream multiplexer settings for Rev A to C boards (continued)

Hardware control		Software control			Transport steam configuration setting
SW7:1	SW7:0	Conf2	Conf1	Conf0	
Off	On	0	1	0	NIM-TSout connected to TS0inout TS0In tri-state ALT_TS0in tri-state
Off	Off	0	1	1	DVB_CIout connected toTS0inout NIM-TSout connected to DVB_CIin TS0In tri-state ALT_TS0in tri-state

Table 4. Transport stream multiplexer settings for Rev D and later boards

Hardware control			Software control			Transport steam configuration setting
SW7:0	SW16:1	SW16:0	Conf2	Conf1	Conf0	
On	On	On	0	0	0	DVB_CIout connected toTS0inout NIM-TS0out connected to DVB_CIin TS0In tri-state ALT_TS0in tri-state
On	On	Off	0	0	1	DVB-CIout connected toTS0in TS0inout connected to DVB-CIin ALT_TS0in tri-state
On	Off	On	0	1	0	NIM-TSout connected to TS0inout TS0In tri-state ALT_TS0in tri-state
On	Off	Off	0	1	1	DVB_CIout connected toTS0inout NIM-TSout connected to DVB_CIin TS0In tri-state ALT_TS0in tri-state
Off	On	On	1	0	0	DVB_CIout connected to ALT_TS0in NIM-TSout connected to DVB_CIin TS0In tri-state
Off	On	Off	1	0	1	NIM-TSout connected toTS0in TS0inout tri-state ALT_TS0in tri-state
Off	Off	On	1	1	0	NIM-TSout connected to ALT_TS0in TS0In tri-state TS0inout tri-state
Off	Off	Off	1	1	1	Reserved

Note: 1 During board level reset, all transport streams connected to the STi7111 are tri-state.

2 When PhyEn (SW7:3 on Revision A to C boards and SW16:3 on Revision D and later boards) is On, transport stream TSOin is tri-state.

3 For information on switches, see Section B.3: Switches on page 62.

3.10 PIO

PIO signals can be assigned alternative functions. This enables the STi7111 to be configured for different architectures. Some PIO pins can be programmed as:

- inputs and outputs
- alternative functions

A complete list of PIO assignments is available in the *STi7111 datasheet* (ADCS 8065030).

The PIO functions used by the STi7111-MBoard are given in *Appendix C: PIO alternate functions on page 66*.

Inputs connected to the alternative function inputs are permanently connected to the input pin. Output signals from a peripheral are only connected when the PIO bit is configured into either push pull or open drain driver, alternative function mode.

Some alternative function signals are available on more than one PIO port.

In addition to the multiplexing on the PIO pins, the STi7111 uses other pin multiplexing to provide different signal options, which depend on the device application.

3.11 Programming EPLDs

The EPLD supports the transport stream multiplexer, interrupt handler, address decoder and Ethernet physical interface.

For more information on the EPLDs, refer to the *MB618 STi7111-Mboard EPLD definition and equation* (ADCS 8088375).

The EPLDs can be updated or programmed remotely. There are two different methods of programming the EPLDs.

- Connection from the PC to an Altera ByteBlaster interface. This interface connects to the EPLD connector (CN20) through a ribbon cable, see *Figure 5*.
- Alternatively the STMC2 is connected directly to the ByteBlaster connector (CN20) using an STMC2 I/O convertor (MB552), see *Figure 6*. This is described in the *ST Micro Connect 2 datasheet* (ADCS 7912386).

Figure 5. EPLD ByteBlaster programming connectivity

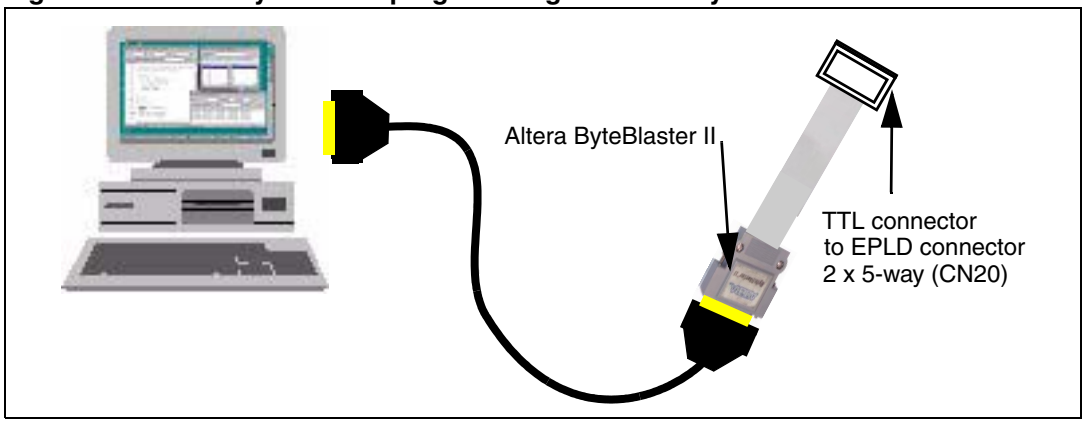
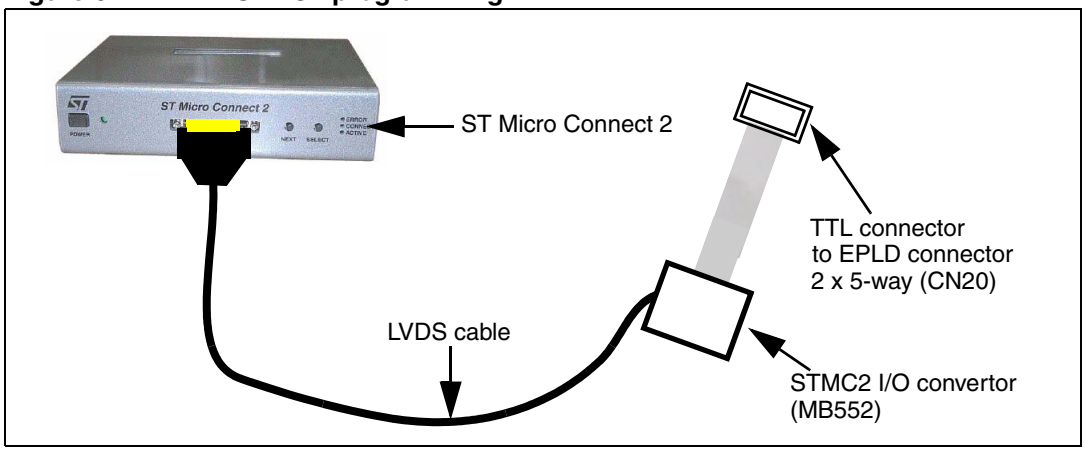


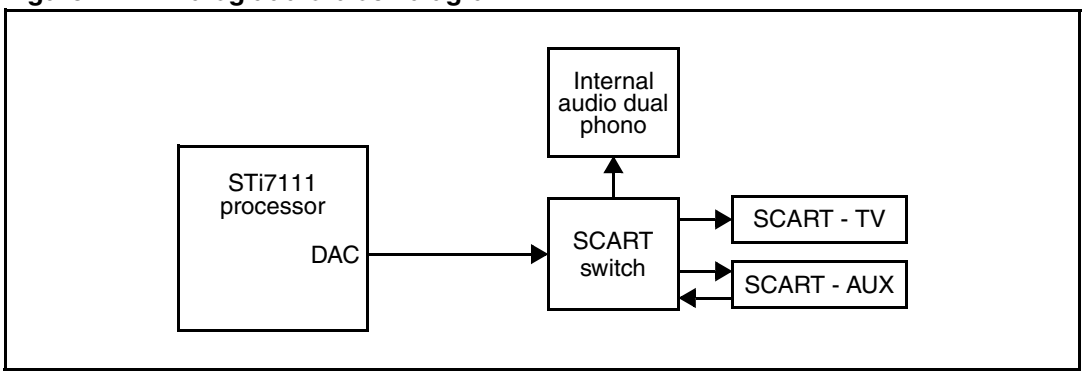
Figure 6. EPLD STMC2 programming



3.12 Analog audio

The audio DACs of the STi7111 are buffered with Op-Amp circuitry, which is connected directly to the SCART switch. This drives two RCA phonos (left and right), along with the dual SCART audio outputs.

Figure 7. Analog audio block diagram



3.13 Digital audio

The following digital audio options are available:

- SPDIF out
- PCM out

SPDIF out

The SPDIF output is provided with an RCA/phono socket, and an optical connector. This output can be connected to an external decoder and amplifier system.

PCM out

The PCM audio output is connected to a 24-bit hybrid DAC. If the frequency is in a range of up to 96 KHz, the output is also connected to RCA/phono sockets.

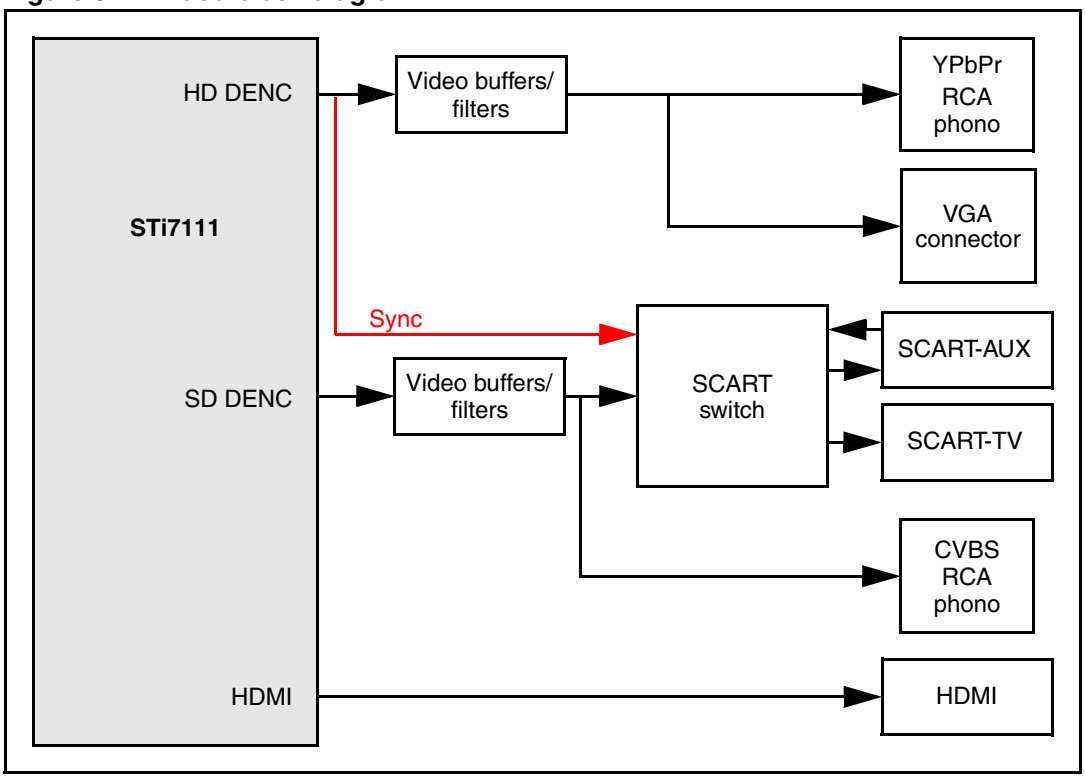
3.14 Video

The following video outputs are available:

- standard definition (SD) analog video output
- high definition (HD) analog video output

The video block diagram is shown in *Figure 8*. Red indicates changes implemented on Revision D and later boards only.

Figure 8. Video block diagram



3.14.1 SD analog video output

The STi7111-MBoard supports a single SD output. All SD analog signals are buffered and filtered. The SD analog output (YCvCb/RGB) drives video signals to a SCART switch and RCA phono connectors. The STi7111-MBoard supports dual SCARTs (upstream and downstream), through an STV6417 SCART switch.

3.14.2 HD analog video output

A single HD analog video output is supported on the board. All HD signals are buffered and filtered using suitable circuitry. The HD analog output (RGB-YPbPr) drives video signals to the RCA phono connectors and a standard 15-pin, high density, D-type connector with VGA connector compatible pinout.

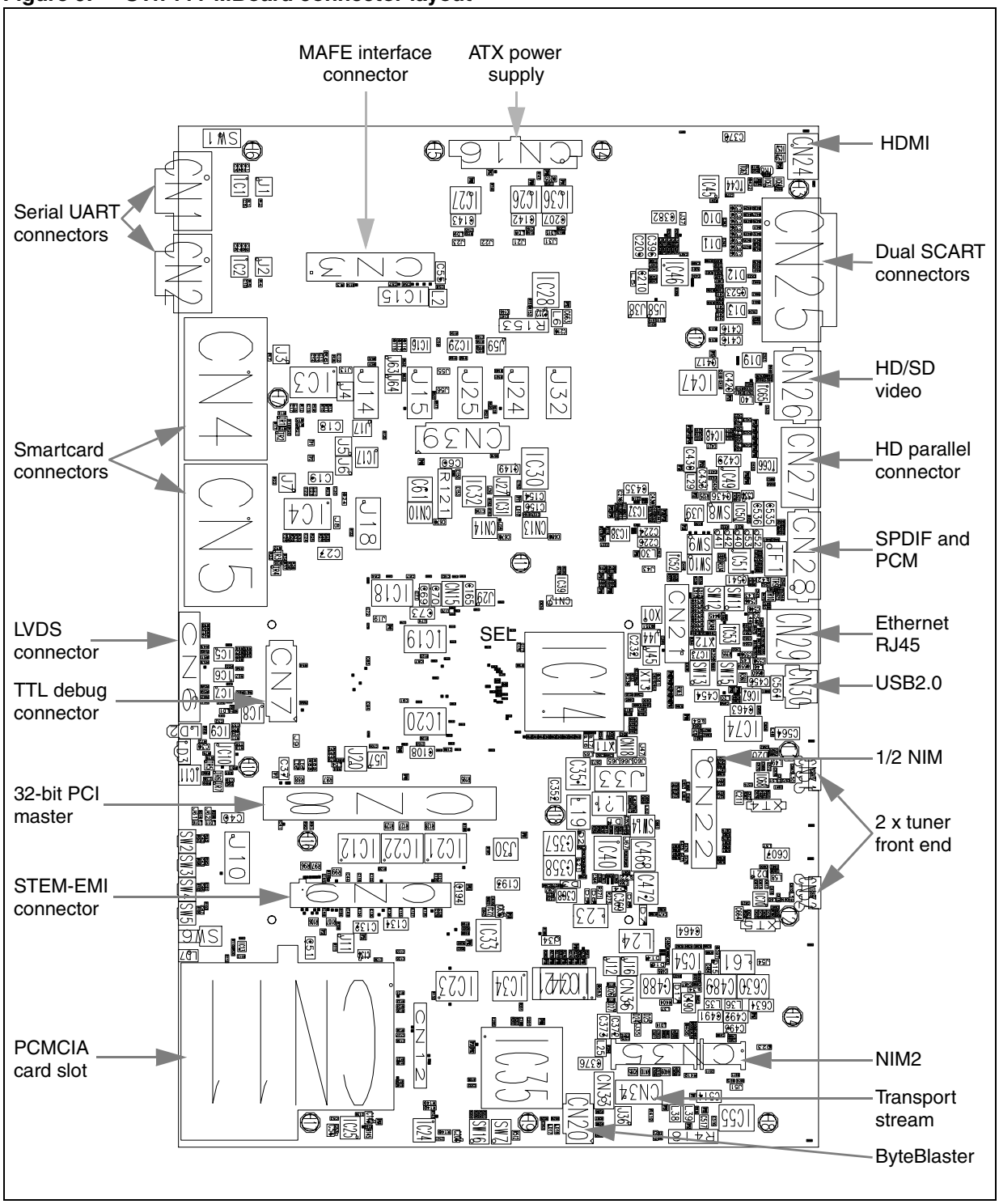
3.14.3 HDMI

HDMI output connector is supported on the STi7111-MBoard and includes CMC filters for 1080p25 and 1080p30 standards (Higher speed than 1080i standard).

Appendix A MB618 STi7111-MBoard connectors

A.1 Connector layout

Figure 9. STi7111-MBoard connector layout



A.2 Front and rear panel layout

The front panel is shown in *Figure 10* and the rear panel of the STi7111-MBoard assembly is shown in *Figure 11*.

Figure 10. Front panel layout

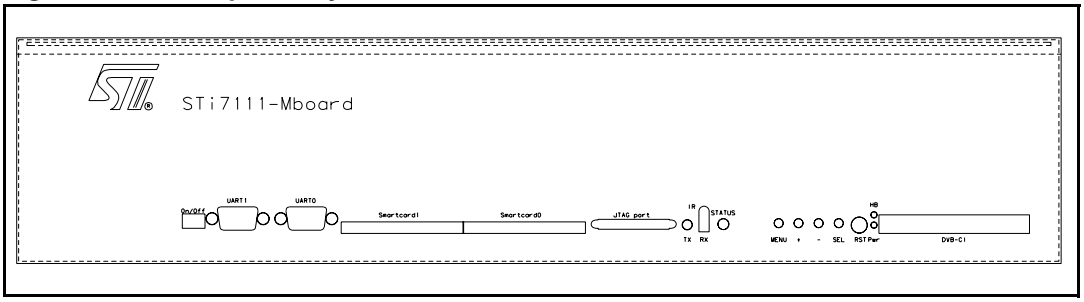
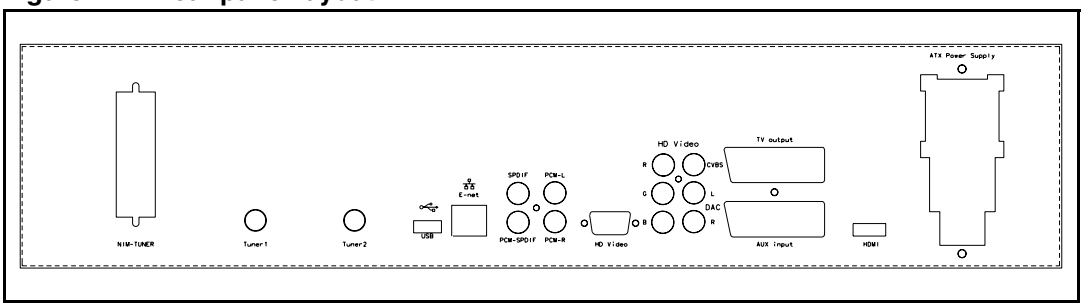


Figure 11. Rear panel layout



A.3 Connectors

The connectors that are fitted to the STi7111-MBoard are listed in *Table 5*, *Table 6* and *Table 7*.

Table 5. Internal connectors

Type of connector	Connector number	Reference
MAFE interface connector	CN3	*Section A.3.2 on page 24*
DCU TTL JTAG debug connector	CN7	*Section A.3.5 on page 27*
PCI 32-bit master connector	CN8	*Section A.3.6 on page 28*
STEM-EMI connector	CN9	*Section A.3.7 on page 30*
Power ground isolator connector - 3V3 CPU input/output	CN10	*Section A.3.8 on page 33*
DVB-CI debug port	CN12	*Section A.3.10 on page 35*
Power ground isolator connector - 2V5 core voltage	CN13	*Section A.3.8 on page 33*
Power ground isolator connector - 1V2 CPU internal	CN14	*Section A.3.8 on page 33*
Power ground isolator connector - 1V8 CPU local	CN15	*Section A.3.8 on page 33*

Table 5. Internal connectors (continued)

Type of connector	Connector number	Reference
DAA connector	CN17	*Section A.3.12 on page 38*
External clock connector	CN18	*Section A.3.13 on page 38*
ByteBlaster interface connector	CN20	*Section A.3.14 on page 39*
MII connector	CN21	*Section A.3.15 on page 40*
I^2C tuner NIM interface connector	CN33	*Section A.3.25 on page 48*
Transport stream interface connector	CN34	*Section A.3.26 on page 48*
Front end I^2C tuner interface connector	CN36	*Section A.3.25 on page 48*
The following connectors are only supported on Revision D boards and later		
1/2 NIM interface connector	CN22	*Section A.3.16 on page 41*
SBAG connector	CN39	*Section A.3.28 on page 51*

Table 6. Front panel connectors

Type of connector	Connector number	Reference
Serial UART RS232-1/0 connector	CN1/CN2	*Section A.3.1 on page 24*
Smartcard 1/ 0 connector	CN4/CN5	*Section A.3.3 on page 25*
LVDS JTAG debug connector	CN6	*Section A.3.4 on page 26*
PCMCIA card socket	CN11	*Section A.3.9 on page 34*

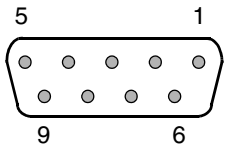
Table 7. Rear panel connectors

Type of connector	Connector number	Reference
ATX power supply connector	CN16	*Section A.3.11 on page 37*
HDMI connector	CN24	*Section A.3.17 on page 42*
Dual SCART connectors	CN25	*Section A.3.18 on page 43*
SD video connector/ HD video connector	CN26	*Section A.3.19 on page 44*
HD video parallel connector	CN27	*Section A.3.20 on page 45*
SPDIF and PCM connector	CN28	*Section A.3.21 on page 46*
Ethernet RJ45 connector	CN29	*Section A.3.22 on page 46*
USB2.0 Type A connector	CN30	*Section A.3.23 on page 47*
RF2/1 input connector	CN31/CN32	*Section A.3.24 on page 47*
NIM2 connector	CN35	*Section A.3.27 on page 49*

A.3.1 RS232 connectors CN1/ CN2

Two 9-pin male D-type connectors, provide RS232 interfaces.

Figure 12. RS232 connector



Viewed from front panel

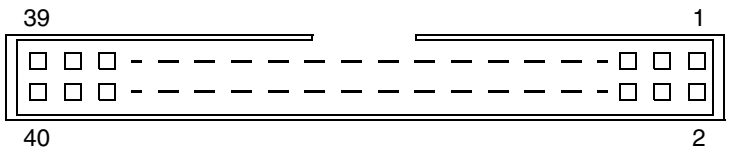
Table 8. RS232 connector pin allocation

Pin	Description	Pin	Description
1	Not connected	6	Not connected
2	R2IN	7	T1OUT
3	T2OUT	8	R1IN
4	Not connected	9	Not connected
5	GND		

A.3.2 MAFE interface connector CN3

A 40-pin SAMTEC connector provides a MAFE interface.

Figure 13. MAFE interface connector



Viewed from above PCB

Table 9. MAFE interface connector pin allocation

Pin	Description	Pin	Description
Even pins	GND	21	+3V3
1	MAFESCLK	23	
3	MAFEFS	25	
5	MAFEHC1	27	+VOUT
7	MAFEDOUT	29	TP36
9	MAFEDIN	31	-VOUT

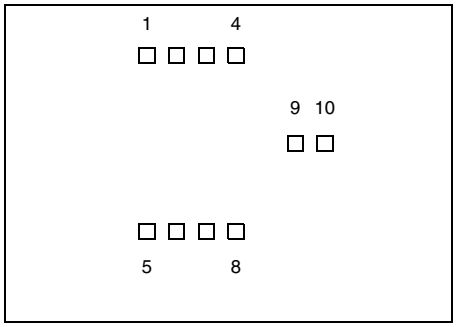
Table 9. MAFE interface connector pin allocation (continued)

Pin	Description	Pin	Description
11	NOT_MAFERESET	33	TP35
13	NOT_MAFEPD	35	TP37
15	MAFEINTR	37	TP34
17	Not connected	39	TP33
19	Not connected		

A.3.3 Smartcard 1/0 socket CN4/CN5

Two 10-pin smartcard sockets.

Figure 14. Smartcard socket connector



Viewed from above PCB

Table 10. Smartcard pin allocation

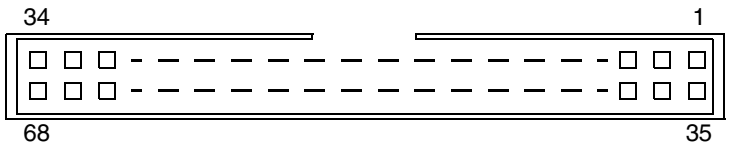
Pin	Description	Pin	Description
1	VCC	6	SC*n*VPP(1)
2	RST	7	IO
3	CLK	8	AUX2
4	AUX1	9	GND
5	GND	10	PRES/NOT_PRES

1. Where *n* is 0 or 1.

A.3.4 LVDS JTAG debug connector CN6

A 68-pin connector for debug functions. ST Micro Connect 2 is supported using this interface.

Figure 15. Debug connector



Viewed from front panel

Table 11. Debug connector pin allocation

Pin	Description	Pin	Description
1	LVDS_SPAREIN+	35	LVDS_SPAREIN-
2	Not connected	36	Not connected
3	LVDS_TRIGIN+	37	LVDS_TRIGIN-
4	Not connected	38	Not connected
5	LVDS_USERIN+	39	LVDS_USERIN-
6	Not connected	40	Not connected
7	LVDS_TMS+	41	LVDS_TMS-
8	Not connected	42	Not connected
9	LVDS_USEROUT+	43	LVDS_USEROUT-
10	Not connected	44	Not connected
11	LVDS_TRIGOUT+	45	LVDS_TRIGOUT-
12	Not connected	46	Not connected
13	LVDS_TDO+	47	LVDS_TDO-
14	Not connected	48	Not connected
15	GND	49	GND
16	LVDSBUF_NOTEN	50	
17	TP3	51	TP3
18		52	
19	LVDS_CLKOUT+	53	LVDS_CLKOUT-
20	GND	54	GND
21	LVDS_CLKIN+	55	LVDS_CLKIN-
22	GND	56	GND
23	LVDS_TDI+	57	LVDS_TDI-
24	Not connected	58	Not connected

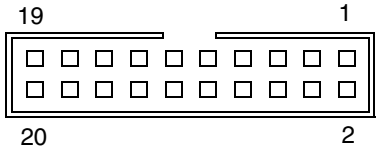
Table 11. Debug connector pin allocation (continued)

Pin	Description	Pin	Description
25	LVDS_NOTRESET+	59	LVDS_NOTRESET-
26	Not connected	60	Not connected
27	LVDS_NOTTRST+	61	LVDS_NOTTRST-
28	Not connected	62	Not connected
29		63	
30		64	
31		65	
32		66	
33	GND	67	GND
34		68	

A.3.5 DCU TTL JTAG debug connector CN7

A 20-pin ST Micro Connect 2 debug connector, provides a JTAG standard debug interface for the ST40 CPU core.

Figure 16. JTAG debug connector



Viewed from above PCB

Table 12. JTAG debug connector pin allocation

Pin	Description	Pin	Description
Even pins	GND	11	TCK
1	Reserved	13	TDI (data into the board)
3	TRIGOUT	15	TDO (data out of the board)
5	TRIGIN	17	JTAG_NOTRST
7	ASEBRK	19	NOT_TRST
9	TMS		

A.3.6 PCI slot connector CN8

A 68-pin PCI connector.

Figure 17. PCI connector

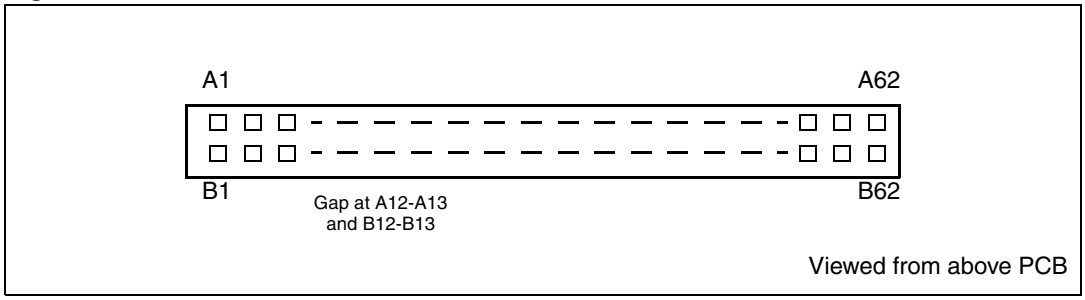


Table 13. PCI connector pin allocation

Pins row A	Description	Pins row B	Description
1	NOTTRST	1	Not connected
2	TCK	2	TCK
3	TMS	3	Not connected
4	TDI	4	TDO
5	Not connected	5	Not connected
6	NOTINTA	6	
7	NOTINTC	7	NOTINTB
8	Not connected	8	NOTINTD
9	RESERVED_CLKC	9	NOTPRSNT1_NOTREQ3
10	Not connected	10	RESERVED_NOTREQ1
11	RESERVED_CLKD	11	NOTPRSNT2_NOTGNT3
12	Not available	12	Not available
13	Not available	13	Not available
14	3V3AUX_NOTGNT1	14	RESERVED_CLKA
15	NOTRST	15	Not connected
16	Not connected	16	CLK_CLKB
17	NOTGNT_NOTGNT0	17	Not connected
18	Not connected	18	NOTREQ_NOTREQ0
19	NOTPME_NOTREQ2	19	Not connected
20	AD30	20	AD31
21	Not connected	21	AD29
22	AD28	22	Not connected
23	AD26	23	AD27

Table 13. PCI connector pin allocation (continued)

Pins row A	Description	Pins row B	Description
24	Not connected	24	AD25
25	AD24	25	Not connected
26	IDSEL_NOTGNT2	26	C_NOTBE3
27	Not connected	27	AD23
28	AD22	28	Not connected
29	AD20	29	AD21
30	Not connected	30	AD19
31	AD18	31	Not connected
32	AD16	32	AD17
33	Not connected	33	C_NOTBE2
34	NOTFRAME	34	Not connected
35	Not connected	35	NOTIRDY
36	NOTTRDY	36	Not connected
37	Not connected	37	NOTDEVSEL
38	NOTSTOP	38	Not connected
39	Not connected	39	NOTLOCK
40		40	NOTPERR
41		41	Not connected
42		42	NOTSERR
43	PAR	43	Not connected
44	AD15	44	C_NOTBE1
45	Not connected	45	AD14
46	AD13	46	Not connected
47	AD11	47	AD12
48	Not connected	48	AD10
49	AD9	49	M66EN
50	Not connected	50	Not connected
51		51	
52	C_NOTBE0	52	AD8
53	Not connected	53	AD7
54	AD6	54	Not connected
55	AD4	55	AD5
56	Not connected	56	AD3
57	AD2	57	Not connected

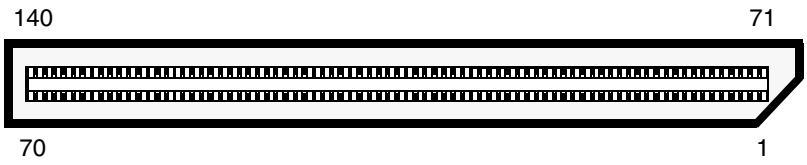
Table 13. PCI connector pin allocation (continued)

Pins row A	Description	Pins row B	Description
58	AD0	58	AD1
59	Not connected	59	Not connected
60	NOTREQ64	60	NOTACK64
61	Not connected	61	Not connected
62		62	

A.3.7 STEM EMI CN9

A 140-pin board-to-board connector.

Figure 18. STEM EMI connector



Viewed from above PCB

Table 14. STEM EMI connector pin allocation

Pin	Description	Pin	Description
1	NOTBS	71	NOTFRAME
2	SDRAM_CLK	72	NOTCAS
3	SDRAM_CLKEN	73	NOT_RESET
4	MEZZ_PRESENT0	74	MEZZ_PRESENT1
5	GND	75	GND
6	DACK2	76	DACK3
7	DACK0	77	DACK1
8	DRAK0	78	DRAK1
9	DREQ0	79	DREQ1
10	GND	80	GND
11	MEMWAIT	81	AUX_CLK
12	+3V3 (VCC)	82	+3V3 (VCC)
13	MEMGRANTED	83	MEMREQ
14	NOTINTR0	84	NOTINTR1
15	GND	85	GND
16	FLASH_CLK	86	FBAA

Table 14. STEM EMI connector pin allocation (continued)

Pin	Description	Pin	Description
17	GND	87	GND
18	NOTWR	88	NOTOE
19	GND	89	GND
20	NOTCS0	90	NOTCS1
21	GND	91	GND
22	A25	92	A24
23	A23	93	A22
24	+3V3 (VCC)	94	+3V3 (VCC)
25	A21	95	A20
26	A19	96	A18
27	GND	97	GND
28	A17	98	A16
29	A15	99	A14
30	+3V3 (VCC)	100	+3V3 (VCC)
31	A13	101	A12
32	A11	102	A10
33	GND	103	GND
34	A9	104	A8
35	A7	105	A6
36	+3V3 (VCC)	106	+3V3 (VCC))
37	A5	107	A4
38	A3	108	A2
39	GND	109	GND
40	A1_NOTBE3	110	A0_NOTBE2
41	NOTBE1	111	NOTBE0
42	GND	112	GND
43	D31 (NC)	113	D30 (NC)
44	D29 (NC)	114	D28 (NC)
45	GND	115	VCC
46	D27 (NC)	116	D26 (NC)
47	D25 (NC)	117	D24 (NC)
48	GND	118	GND
49	D23 (NC)	119	D22 (NC)
50	D21 (NC)	120	D20 (NC)
51	GND	121	VCC

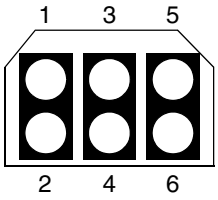
Table 14. STEM EMI connector pin allocation (continued)

Pin	Description	Pin	Description
52	D19 (NC)	122	D18 (NC)
53	D17 (NC)	123	D16 (NC)
54	GND	124	GND
55	D15	125	D14
56	D13	126	D12
57	GND	127	VCC
58	D11	128	D10
59	D9	129	D8
60	GND	130	GND
61	D7	131	D6
62	D5	132	D4
63	GND	133	VCC
64	D3	134	D2
65	D1	135	D0
66	GND	136	GND
67	MPX_CLK	137	ALE_NOTRAS
68	GND	138	GND
69	+12 V (VCC)	139	+12 V (VCC)
70	+12 V (VCC)	140	+12 V (VCC)

A.3.8 Power ground isolators CN10/CN13/CN14/CN15

Four 6-pin headers.

Figure 19. Power ground isolator



Viewed from above PCB

Table 15. Power ground isolator CN10 pin allocation

Pin	Description	Pin	Description
1	+3V3	4	GND_ISOL
2	CPUIO	5	+3V3
3	GND_BRD	6	CPUIO

Table 16. Power ground isolator CN13 pin allocation

Pin	Description	Pin	Description
1	+2V5	4	GND_ISOL
2	+2V5_CORE	5	+2V5
3	GND_BRD	6	+2V5_CORE

Table 17. Power ground isolator CN14 pin allocation

Pin	Description	Pin	Description
1	+1V2	4	GND_ISOL
2	CPUINT	5	+1V2
3	GND_BRD	6	CPUINT

Table 18. Power ground isolator CN15 pin allocation

Pin	Description	Pin	Description
1	+1V8	4	GND_ISOL
2	CPULMI	5	+1V8
3	GND_BRD	6	CPULMI

A.3.9 PCMCIA card connector CN11

A 68-pin PCMCIA connector.

Figure 20. PCMCIA card connector

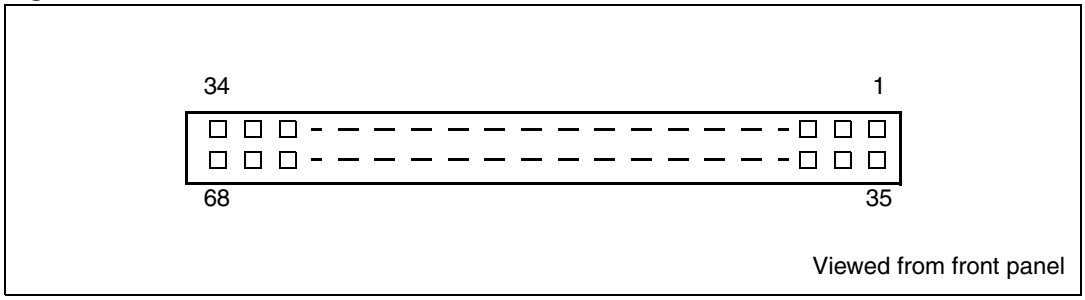


Table 19. PCMCIA card connector pin allocation

Pin	Description	Pin	Description
1	Not connected	35	Not connected
2	DATA3	36	NOTCD1
3	DATA4	37	TS_OUT_DATA3
4	DATA5	38	TS_OUT_DATA4
5	DATA6	39	TS_OUT_DATA5
6	DATA7	40	TS_OUT_DATA6
7	NOTCE1	41	TS_OUT_DATA7
8	A10	42	NOTCE2
9	NOTOE	43	VS1 (NC)
10	A11	44	NOTIORD
11	A9	45	NOTIOWR
12	A8	46	TS_IN_STRT
13	A13	47	TS_IN_DATA0
14	A14	48	TS_IN_DATA1
15	NOTWE	49	TS_IN_DATA2
16	NOTIREQ	50	TS_IN_DATA3
17	VCC1	51	VCC0
18	VPP1	52	VPP0
19	TS_IN_VAL	53	TS_IN_DATA4
20	TS_IN_CLK	54	TS_IN_DATA5
21	A12	55	TS_IN_DATA6
22	A7	56	TS_IN_DATA7
23	A6	57	TS_OUT_CLK
24	A5	58	CARD_RESET

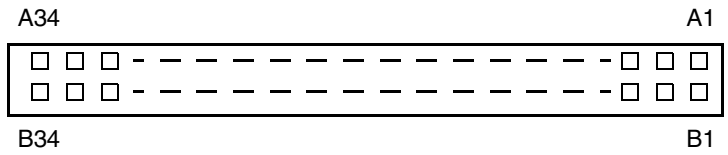
Table 19. PCMCIA card connector pin allocation (continued)

Pin	Description	Pin	Description
25	A4	59	NOTWAIT
26	A3	60	NOTINPACK (NC)
27	A2	61	NOTREG
28	A1	62	TS_OUT_VAL
29	A0	63	TS_OUT_STRT
30	DATA0	64	TS_OUT_DATA0
31	DATA1	65	TS_OUT_DATA1
32	DATA2	66	TS_OUT_DATA2
33	NOTIOIS16	67	NOTCD2
34	Not connected	68	Not connected

A.3.10 P6960 series high-density logic probe land pattern CN12

A 34-channel, Tektronix P6960 series high-density logic probe land pattern.

Figure 21. P6960 series logic probe land pattern



Viewed from above PCB

Table 20. P6960 series logic probe land pattern pin allocation

Pin row A	Description	Pin row B	Description
1	DATA2	1	Not connected
2	DATA1	2	DATA0
3	Not connected	3	A0
4	A1	4	Not connected
5	A2	5	NOTDVBREG
6	Not connected	6	A3
7	CK1+	7	Not connected
8	CK1-	8	NOTDVBWAIT
9	Not connected	9	A4
10	NOTDVBRESET	10	Not connected
11	A5	11	A6

Table 20. P6960 series logic probe land pattern pin allocation (continued)

Pin row A	Description	Pin row B	Description
12	Not connected	12	A7
13	A12	13	Not connected
14	NOTDVBCE1	14	NOTDVBINTR
15	Not connected	15	NOTDVBIOWE
16	A14	16	Not connected
17	A13	17	A8
18	Not connected	18	NOTDVBIOWR
19	A9	19	Not connected
20	A11	20	CK2-
21	Not connected	21	CK2+
22	NOTDVBIORD	22	Not connected
23	A10	23	NOTDVBIOOE
24	Not connected	24	DATA7
25	DATA6	25	Not connected
26	DATA4	26	DATA5
27	Not connected	27	DATA3
28		28	Not connected
29		29	
30		30	
31		31	
32		32	
33		33	
34		34	

A.3.11 ATX power connector CN16

An ATX 20-pin Mini-Fit Jnr. PCB mounting plug.

Provides power to the board from a standard PC-type power supply.

Figure 22. ATX power connector

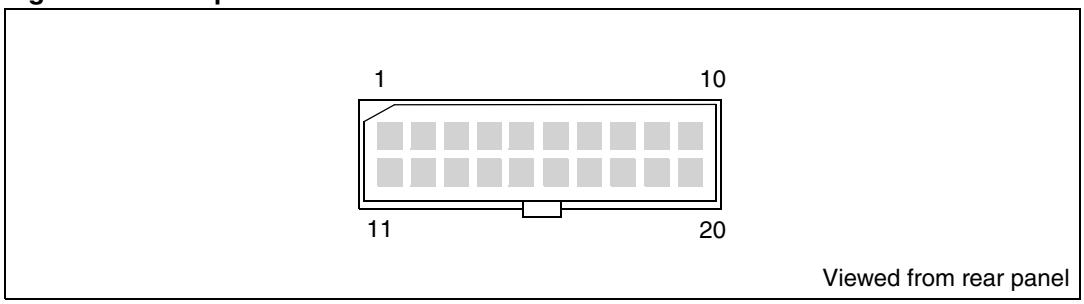


Table 21. ATX power connector pin allocation

Pin	Description	Pin	Description
1	+3V3_A	11	+3V3_C
2	+3V3_B	12	-12V
3	GND	13	GND
4	+5V_A	14	NOTPS_ON
5	GND	15	GND
6	+5V_B	16	GND
7	GND	17	GND
8	PW_OK (LED 11)	18	-5V
9	+5VSB	19	+5V_C
10	+12V	20	+5V_D

A.3.12 DAA connector CN17

A 4-pin header.

Figure 23. DAA connector

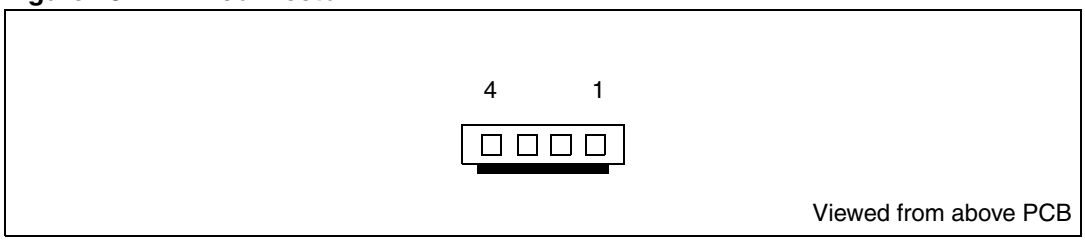


Table 22. DAA connector pin allocation

Pin	Description	Pin	Description
1	GND	3	DAA_C1A
2	DAA_C2A	4	GND

A.3.13 External clock connector CN18

A single SMB socket.

Figure 24. External clock connector

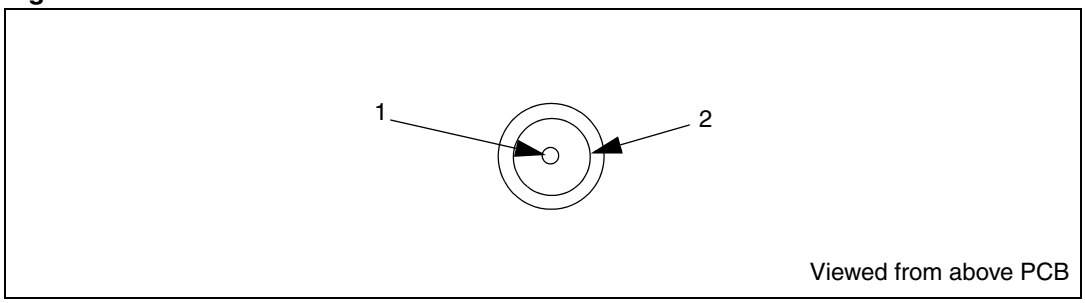


Table 23. External clock connector pin allocation

Pin	Description	Pin	Description
1	CLKIN	2	GND

A.3.14 ByteBlaster connector CN20

A 10-way IDC connector.

The EPLD can be programmed through the ISP header.

Figure 25. ByteBlaster connector

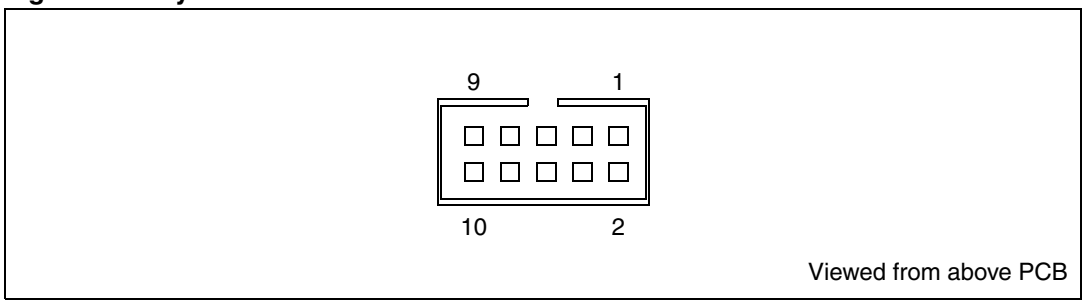


Table 24. ByteBlaster connector pin allocation

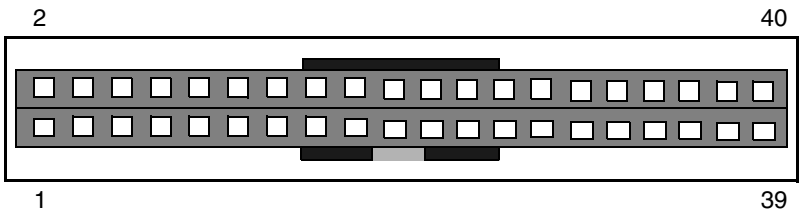
Pin	Description	Pin	Description
1	DCLK_TCK	2	GND
3	CONFDONE_TDO	4	VCC
5	NOTCONFIG_TMS	6	NOTCE_NC_AUXTDO
7	Not connected	8	Not connected
9	ASDI_DATA0_TDI	10	GND

A.3.15 Ethernet dongle MII connector CN21

Surface mount, vertical male connector. Double row of 20 pins, 1.27mm pitch. Mates with FFSD connector.

Connector orientation has the notched blade side the same side as pin 1.

Figure 26. MII connector



Viewed from above PCB

Table 25. MII connector pin allocation

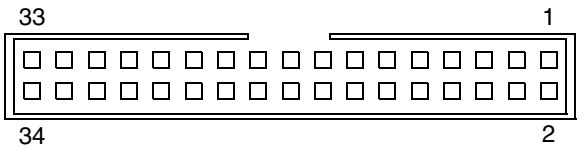
Pin	Description	Pin	Description
1	GND	2	GND
3	3V3_PHY	4	+5V
5	3V3_PHY	6	+5V
7	MII_COL	8	MII_CRS
9	MII_TXD0	10	MII_TXD1
11	MII_TXD2	12	MII_TXD3
13	GMII_TXD4 (NC)	14	GMII_TXD5 (NC)
15	GMII_TXD6 (NC)	16	GMII_TXD7 (NC)
17	GND	18	MII_TX_EN
19	MII_TXCLK	20	GND
21	MII_RXCLK	22	MII_RX_ER
23	MII_RX_DV	24	GND
25	MII_RXD0	26	MII_RXD1
27	MII_RXD2	28	MII_RXD3
29	GMII_RXD4 (NC)	30	GMII_RXD5 (NC)
31	GMII_RXD6 (NC)	32	GMII_RXD7 (NC)
33	GND	34	MII_MDC
35	MII_MDIO	36	NOTRESET
37	NOTINT	38	RMIIMODE
39	GMIIMODE	40	GND

A.3.16 1/2 NIM front-end connector CN22

Note: This connector is only supported on Revision D and later boards.

A 1/2 NIM front-end connector (optional for specific functions). IDC header, 2 x 17 way, vertical, no latches, low profile, PCB mounting.

Figure 27. 1/2 NIM connector



Viewed from above PCB

Table 26. 1/2 NIM connector pin allocation

Pin	Description	Pin	Description
1	FSK_FILTER	2	NC
3	FE2_AGC	4	FE2_CLKOUT
5	+5V	6	+3V3RF2
7	FE2_SCLK	8	FE2_SDATA
9	GND	10	GND
11	FE2_QM	12	FE2_QP
13	FE2_IM	14	FE2_IP
15	GND	16	GND
17	FE2_FSK_IN	18	FE2_FSK_OUT
19	GND	20	GND
21	NC	22	NC
23	FE1_AGC	24	FE1_CLKOUT
25	NC	26	NC
27	FE1_SCLK	28	FE1_SDATA
29	GND	30	GND
31	FE1_QM	32	FE1_QP
33	FE1_IM	34	FE1_IP

A.3.17 HDMI connector CN24

A HDMI receptacle (male), right angled, no flange, surface mount, 19-pin and 6 shield. The high-definition multimedia interface is a trademark of HDMI Licensing, LLC.

Figure 28. HDMI connector

Table 27. Digital video HDMI connector pin allocation

Pin	Description	Pin	Description
1	D2+	11	CKS (GND)
2	D2S (GND)	12	CK-
3	D2-	13	CEC
4	D1+	14	NC
5	D1S (GND)	15	SCL
6	D1-	16	SDA
7	D0+	17	GND
8	D0S (GND)	18	+5V
9	D0-	19	HPG
10	CK+		

A.3.18 SCART connectors CN25

Dual 21-pin SCART connectors.

Figure 29. SCART connector

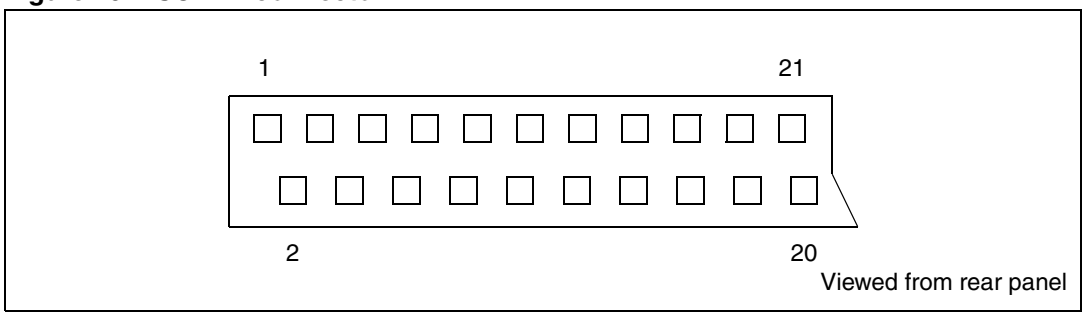


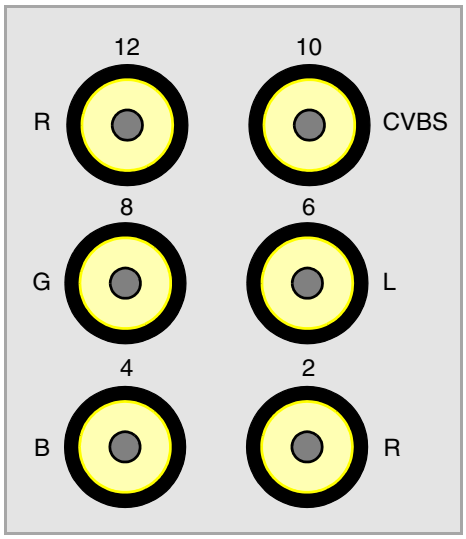
Table 28. SCART connector pin allocation

Pin	Description	Pin	Description
1	AUDIO_OUT_R	2	AUDIO_IN_R
3	AUDIO_OUT_L	4	AUDIO_GND
5	BLUE_GND	6	AUDIO_IN_L
7	BLUE	8	FUNCTION_SWITCH
9	GREEN_GND	10	NC
11	GREEN	12	NC
13	RED_GND	14	COMM_GND
15	RED	16	BLANKING
17	VIDEO_GND	18	BLANKING_GND
19	VIDEO_OUT	20	VIDEO_IN
21	SCREEN		

A.3.19 HD and SD video out sockets CN26

Two 3-way video phono sockets.

Figure 30. HD and SD video out sockets



Viewed from rear panel

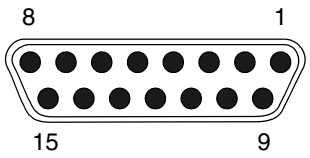
Table 29. HD and SD video out sockets pin allocation

Pin	Description	Pin	Description
Odd pins	GND	8	HD_GREEN
2	ROUT_TV	10	CVBS_DALC
4	HD_BLUE	12	HD_RED
6	LOUT_TV		

A.3.20 VGA HD parallel connector CN27

A 15-pin D-type VGA socket.

Figure 31. VGA HD video parallel connector



Viewed from rear panel

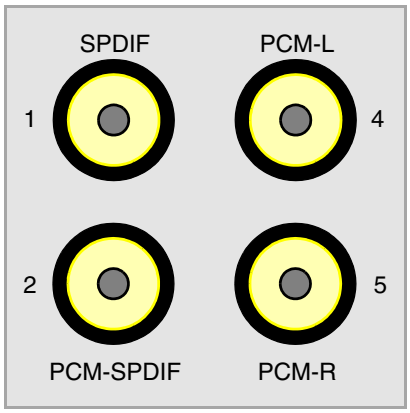
Table 30. VGA HD video parallel connector pin allocation

Pin	Description	Pin	Description
1	RED	9	NC
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	
5	GND	13	HD_HSYNC
6		14	HD_VSYNC
7		15	NC
8			

A.3.21 SPDIF and PCM audio output sockets CN28

Two 2-way audio sockets.

Figure 32. SPDIF and PCM audio sockets



Viewed from rear panel

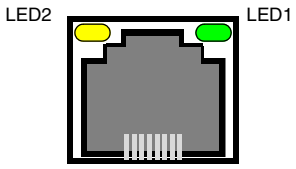
Table 31. SPDIF and PCM audio sockets pin allocation

Pin	Description	Pin	Description
1	SPDIFOUT	4	PCM_LOUT
2	PCM_SPDIFOUT	5	PCM_ROUT
3	GND		

A.3.22 MII Ethernet connector CN29

An RJ45 connector provides a 10/100 BaseT Ethernet physical layer (PHY) interface.

Figure 33. Ethernet connector



Viewed from rear panel

Table 32. Ethernet connector pin allocation

Pin	Description	Pin	Description
1	TD+	7	GND
2	TD_CT	8	
3	TD-	9	LED2_YA
4	RD+	10	LED2_YK

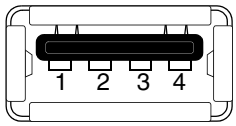
Table 32. Ethernet connector pin allocation (continued)

Pin	Description	Pin	Description
5	RD_CT	11	LED1_GA
6	RD-	12	LED1_GK

A.3.23 USB connector CN30

A USB2.0 Type A connector.

Figure 34. USB2.0 Type A connector



Viewed from rear panel

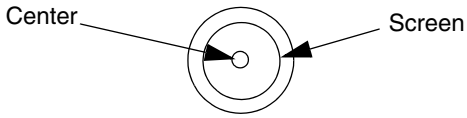
Table 33. USB connector pin allocation

Pin	Description	Pin	Description
1	VBUS	3	DP
2	DM	4	GND

A.3.24 RF in connectors CN31/CN32

F type coaxial connectors for RF input signal.

Figure 35. RF connector



Viewed from rear panel

Table 34. RF connector pin allocation

Pin	Description	Pin	Description
Center	RFIN	Screen	GND

A.3.25 I²C connectors CN33/CN36

Two 4-pin headers provide I²C interfaces.

Figure 36. I²C connector

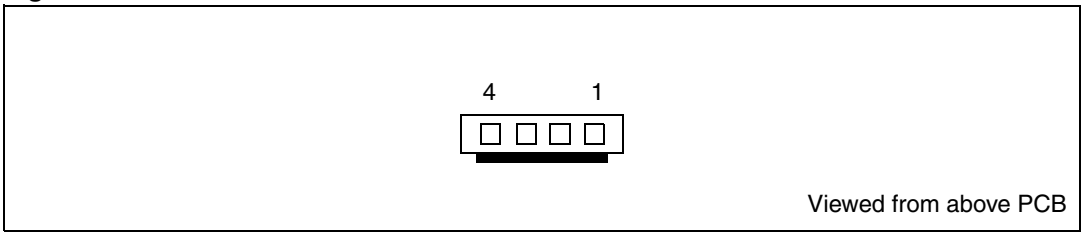


Table 35. I²C connector pin allocation

Pin	Description	Pin	Description
1	+5 V	3	SCL
2	SDA	4	GND

A.3.26 Transport stream data connector CN34

A 20-pin connector provides transport stream data output.

Figure 37. Transport stream data connector

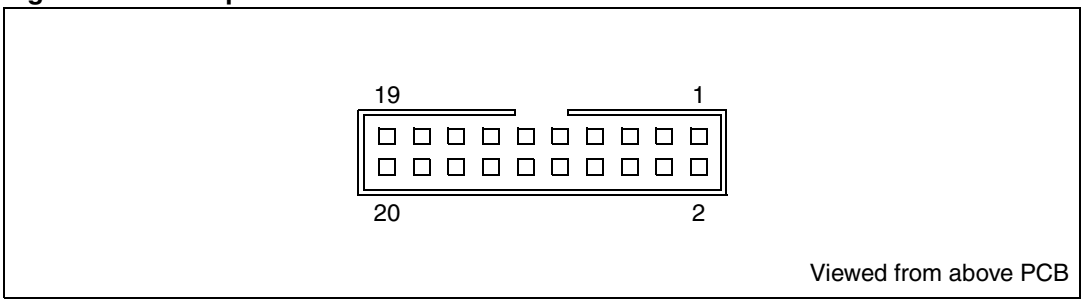


Table 36. Transport stream data connector pin allocation

Pin	Description	Pin	Description
1	SDA	2	SCL
3	NOTRST	4	Not connected
5	DATA0	6	DATA1
7	DATA2	8	DATA3
9	DATA4	10	Not connected
11	DATA5	12	DATA6
13	DATA7	14	Not connected
15	TSERROR	16	TSCLK
17	TSVALID	18	Not connected
19	TSPACKETCLK	20	AS1

A.3.27 NIM2 connector CN35

An 84-pin connector.

The connector is made up, on the board, with two separate, female connectors:

- a SAMTEC 28-pin
- a SAMTEC 54-pin

The two connectors are arranged, and the pins are numbered, as shown in *Figure 38*.

Pins 15 and 57 are not available.

Figure 38. NIM2 connector

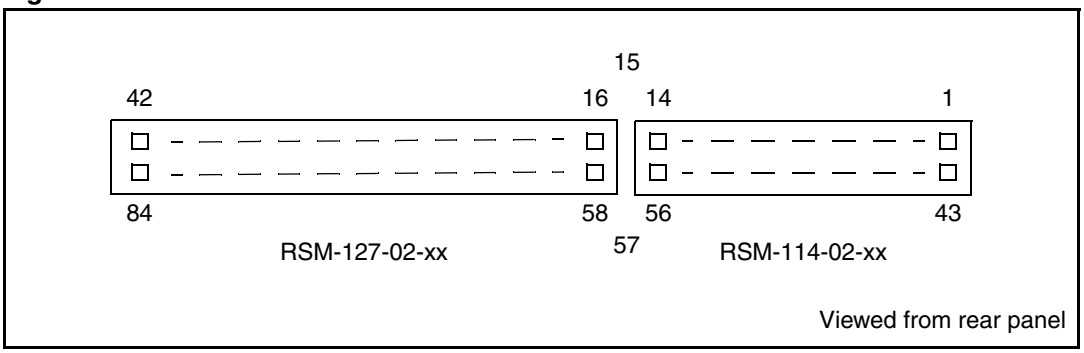


Table 37. NIM2 connector pin allocation

Pin	Description	Pin	Description
1	LNBRF	**43**	**Key1**
2	GNDA1	44	VCORESEL_COM
3	GNDA2	45	VCORESEL_1V2
4	GNDA3	46	VCORESEL_1V0
5	LNBSUPPLY5V	47	RESERVED1 (NC)
6	GNDA4	48	RESERVED2 (NC)
7	GNDA5	49	SRX (NC)
8	GNDA6	50	DRX (NC)
9	VCC3V3A	51	ITX (NC)
10	GNDA7	52	QTX (NC)
11	GNDA8	53	ETX (NC)
12	VCORE_A1	54	VCORE_A2
13	ANALOG5V	55	CTX (NC)
14	VTUNE32V (NC)	56	OOB_RESERVED (NC)
15	**Key3**	**57**	**Key4**
16	DISEQCRX	58	RESERVED3 (NC)
17	ADDRESS0	59	ADDRESS1
18	DISEQCTX	60	RESERVED4 (NC)

Table 37. NIM2 connector pin allocation (continued)

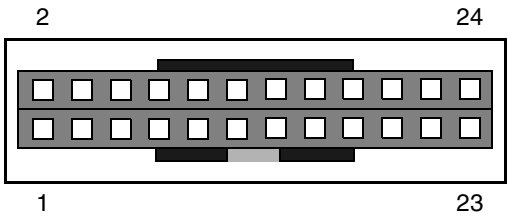
Pin	Description	Pin	Description
19	OP1 (NC)	61	RESERVED5 (NC)
20	OP0 (NC)	62	RESERVED6 (NC)
21	OP2 (NC)	63	RESERVED7 (NC)
22	GNDD1	64	GNDD4
23	VCORE_D1	65	VCORE_D3
24	PACKETCLK	66	PACKETCLK_2 (NC)
25	BYTECLKVALID	67	BYTECLKVALID_2 (NC)
26	BYTECLK	68	BYTECLK_2 (NC)
27	ERROR	69	ERROR_2 (NC)
28	GNDD2	70	GNDD5
29	VCORE_D2	71	VCORE_D4
30	DATA7	72	DATA7_2 (NC)
31	DATA6	73	DATA6_2 (NC)
32	DATA5	74	DATA5_2 (NC)
33	DATA4	75	DATA4_2 (NC)
34	DATA3	76	DATA3_2 (NC)
35	DATA2	77	DATA2_2 (NC)
36	DATA1	78	DATA1_2 (NC)
37	DATA0	79	DATA0_2 (NC)
38	GNDD3	80	GNDD6
39	VCC3V3D	81	RESERVED8 (NC) on Revision A to C boards +12V on Revision D and later boards
40	SCL	82	SCL2 (NC)
41	SDA	83	SDA2 (NC)
42	NOTRESET	**84**	**Key2**

A.3.28 SBAG connector CN39

Note: This connector is not present on Revisions A to C of the board.

A 24-way, vertical terminal strip surface mount pin header connector. Double row, 2 x 12 pins, unshrouded, with a pitch of 2.54 mm.

Figure 39. SBAG connector



Viewed from above PCB

Table 38. SBAG connector pin allocation

Pin	Description	Pin	Description
1	PIO33_IRIN_SBA_DAT0	2	NC
3	PIO27_MAFE_SCLK_SBA_DAT1	4	
5	PIO26_MAFE_FS_SBA_DAT2	6	
7	PIO25_MAFE_DIN_SBA_DAT3	8	
9	NC	10	
11		12	
13		14	PIO34_UHF_TTL_IN_SBA_CLK
15		16	NC
17		18	
19		20	
21		22	
23	PIO37_RMII_REF_CLK_PCIINT0_ SBA_SYNC	24	

Appendix B Jumpers, option resistors, switches and LEDs

B.1 Jumpers

The STi7111-MBoard includes the jumpers listed in *Table 39*.

Table 39. Jumper settings

Jumper	Description	Default	
		Rev A to C boards	Rev D and later boards
J1	RS232 ASC 1 driver enable: 1-2 = low - disabled 2-3 = high - enabled	2-3	
J2	RS232 ASC 0 driver enable: 1-2 = low - disabled 2-3 = high - enabled	2-3	
J3	Smartcard1 presence detect connectivity: 1-2 = PRES 2-3 = NOTPRES	2-3	
J4	PIO1/2: 1-2 = configured SMARTCARD_EXTCLK 2-3 = configured PCI_NOTLOCK	1-2	
J5	Smartcard1 reset invert: 1-2 = not inverted 2-3 = inverted	2-3	
J6	Smartcard0 reset invert: 1-2 = not inverted 2-3 = inverted	1-2	
J7	Smartcard0 presence detect connectivity: 1-2 = PRES 2-3 = NOTPRES	1-2	
J8	Smartcard0 DATAIN/OUT	Off	
J9	+3V3 test header	Do not fit	
J10	PIO6 isolation headers: A = PIO6(0) B = PIO6(1) C = PIO6(2) D = PIO6(3) E = PIO6(4) F = PIO6(5) G = PIO6(6) H = PIO6(7)	 On On On On On On On On	

Table 39. Jumper settings (continued)

Jumper	Description	Default	
		Rev A to C boards	Rev D and later boards
J11	EMI NOTCSD connectivity: 1-2 = STEM NOTCS1 2-3 = DVB-CI NOTCE2	1-2	
J12	PIO3(0) use: 1-2 = configured as SCLK1 2-3 = configured as PCI_NOINTD	1-2	
J13	Smartcard1 DATAIN/OUT	Off	
J14	PIO1 isolation headers: A = PIO1(0) B = PIO1(1) C = PIO1(2) D = PIO1(3) E = PIO1(4) F = PIO1(5) G = PIO1(6) H = PIO1(7)	 On On On On On On On On	
J15	PIO3 isolation headers: A = PIO3(0) B = PIO3(1) C = PIO3(2) D = PIO3(3) E = PIO3(4) F = PIO3(5) G = PIO3(6) H = PIO3(7)	 On On On On On On On On	
J16	PIO3(1) use: 1-2 = configured as SDATA1 2-3 = configured as PCI_NOINTC	1-2	
J17	PIO1(7) use: 1-2 = configured as HDMI_CEC 2-3 = configured as SMARTCARD1 detect	2-3	
J18	PIO0 isolation headers: A = PIO0(0) B = PIO0(1) C = PIO0(3) D = PIO0(2) E = PIO0(4) F = PIO0(5) G = PIO0(6) H = PIO0(7)	 On On On On On On On On	

Table 39. Jumper settings (continued)

Jumper	Description	Default	
		Rev A to C boards	Rev D and later boards
J19	GND testpoint	Do not fit	
J20-A	PCI_IDSEL select A: 1-2 = taken from PCI slot 2-3 = set to P_AD31	1-2	
J20-B	PCI_IDSEL select B: 5-6 = set to P_AD30 4-5 = NOTGNT2 (master mode)	5-6	4-5
J21	+5V test point	Do not fit	
J22	GND test point	Do not fit	
J23	+12V test point	Do not fit	
J24	PIO4 isolation headers: A = PIO4(0) B = PIO4(1) C = PIO4(2) D = PIO4(3) E = PIO4(4) F = PIO4(5) G = PIO4(6) H = PIO4(7)	 On On On On On On On On	 On On On On Off On On On
J25	PIO2 isolation headers: A = PIO2(0) B = PIO2(1) C = PIO2(2) D = PIO2(3) E = PIO2(4) F = PIO2(5) G = PIO2(6) H = PIO2(7)	On On On On On On On On	
J26	GROUND_SENSE to GROUND solder link	Soldered	
J27	GND sense connectivity: 1-2 = GND 2-3 = STi7111 DGND1V0SENSE pin	1-2	2-3
J28	VCC_SENSE to +1V2 solder link	Soldered	
J29	VCC sense connectivity: 1-2 = CPULMI 2-3 = STi7111 DVDD1V0SENSE pin	1-2	Do not fit

Table 39. Jumper settings (continued)

Jumper	Description	Default	
		Rev A to C boards	Rev D and later boards
J30-B	STEMnotCS0 connectivity 1-2 =STEMnotCS0 connects to EMInotCSD 2-3 = STEMnotCS0 connects to EMInotCSA via J30	4-5	5-6
J30-A	EMI notCSA connectivity 1-2 = notCSA connects to STEMnotCS0 via J25 2-3 = notCSA connects to NOR FLash (IC24)	2-3	
J31	+3V3 testpoint	Do not fit	
J32	PIO5 isolation headers: A = PIO5(0) B = PIO5(1) C = PIO5(2) D = PIO5(3) E = PIO5(4) F = PIO5(5) G = PIO5(6) H = PIO5(7)	 On On On On On On On On	
J33	PIO7 isolation headers: A = Not used B = Not used C = PIO7(5) D = PIO7(4) E = PIO7(3) F = PIO7(2) G = PIO7(1) H = PIO7(0)	 Do not fit Do not fit On On On On On On	 On On On On On On On On
J34	EMINOTCSD connectivity: 1-2 = NOTCSD connects to STEMNOTCS1 2-3 = NOTCSD connects to DVB-CI	2-3	
J35	GND testpoint	Do not fit	
J36	Serial transport stream NIM bit select: 1-2 = TS_Data7 connected to NIM TS_Data7 2-3 = TS_Data7 connected to NIM TS_Data0	1-2	
J37	GND testpoint	Do not fit	

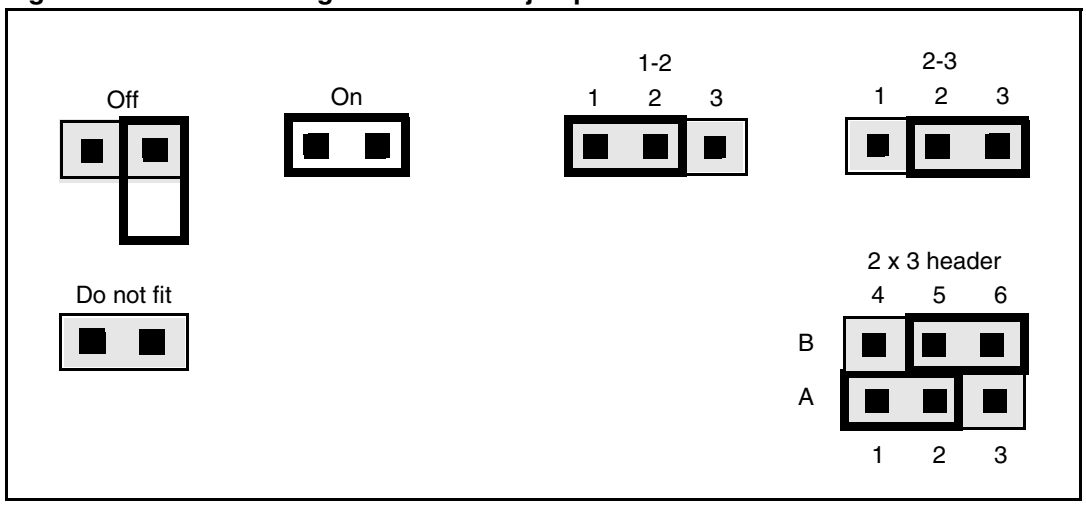
Table 39. Jumper settings (continued)

Jumper	Description	Default	
		Rev A to C boards	Rev D and later boards
J38	**Revision A to C boards:** CVBS select: 1-2 = SCART 2-3 = PHONO **Revision D and later boards:** SD/HD CVBS/Sync DAC select on SCART 1-2 = HD DAC Sync 2-3 = SD DAC CVBS/Sync	1-2	2-3
J39	AK4386 De-emphasis filter enable: 1-2 = low - disabled 2-3 = high - enabled	1-2	
J40	CS8406 I^2C clock select: 1-2 = GND 2-3 = CLOCK	1-2	
J41	CS8406 RXP_SFMTO select: 1-2 = GND 2-3 = +3V3	1-2	
J42	CS8406 I^2C data select: 1-2 = GND 2-3 = DATA	1-2	
J43	+5V testpoint	Do not fit	
J44	FE_DVDD voltage select: 1-2 = CPUINT, 1V2 2-3 = 1V from MIC49300 (IC20)	2-3	1-2
J45	SMSC LAN8700 Clock source: 1-2 = Use crystal (XT3) 2-3 = Use PII_PHYCLK from STi7111	1-2	2-3
J46	Tuner RF2 5V isolator on Revision A to C boards only	On	N/A
J47	GND testpoint	Do not fit	
J48	Tuner interface connector supply voltage on CN22 on Revision A to C boards only: 1-2 = +5VRF2 2-3 = +3V3	1-2	N/A
J49	Tuner RF1 5V isolator on Revision A to C boards only	On	N/A
J50	Tuner Interface connector supply voltage on CN23 on Revision A to C boards only: 1-2 = +5VRF1 2-3 = +3V3	1-2	N/A

Table 39. Jumper settings (continued)

Jumper	Description	Default	
		Rev A to C boards	Rev D and later boards
J51	NIM2 VCORESEL voltage select source: On = sense defined on MB636 Off = sense defined on NIM module	On	
J52	CS8406 U/TEST mode: 1-2 = GND 2-3 = +3v3	2-3	
J53	CS8406 I^2C addr1 or CDIN/TEST: 1-2 = GND 2-3 = +3V3	1-2	
J54	+12V testpoint	Do not fit	
SW14-A	DISEQC_RX/FSK_OUT select: 1-2 = FSK_OUT 2-3 = DISEQC_RX	2-3	
SW14-B	DISEQC_DET/FSK_IN select 4-5 = FSK_IN 5-6 = DISEQC_DET	5-6	
The following jumpers are only applicable for Revision D and later boards:			
J55	Reserved	N/A	Do not fit
J56	Reserved	N/A	Do not fit
J57	IDSEL for cut 2.0 Silicon 1-2 = IDSEL from PIO4_4 2-3 = normal mode	N/A	2-3
J58	SD CVBS select 1-2 = SCART 2-3 = Phono	N/A	1-2
J59	PIO6_7 SPI/UART function select 1-2 = ASC4_TxD 2-3 = SPI_notS	N/A	2-3
J60	Test header for UART5	N/A	Do not fit
J61	PIO6_2 Spare Heartbeat LED	N/A	Do not fit
J62	PIO6_3 Spare Heartbeat LED	N/A	Do not fit
J63	Reserved	N/A	Do not fit
J64	Reserved	N/A	Do not fit
J65	FSK UART Tx	N/A	Do not fit
J66	FSK UART Rx	N/A	Do not fit
J67	1/2 NIM FSK config jumper	N/A	Do not fit

Figure 40. Default configurations of the jumpers



B.2 Option resistors

The STi7111-MBoard includes the resistor options listed in *Table 40*.

Table 40. Option resistor settings

Resistor	Description	Default
R6	R6 Smartcard1 5V or 3V IO select: 1-2 = high - 5V IO 2-3 = low - 3V IO	1-2
R24	Smartcard0 5V or 3V IO select: 1-2 = high = 5V IO 2-3 = low = 3V IO	1-2
R82	NOTPRSNT2_NOTGNT3 select: 1-2 = NOTPRSNT1 2-3 = NOTGNT3 (master mode)	1-2
R83	NOTPRSNT1_NOTREQ3 select: 1-2 = NOTPRSNT1 2-3 = NOTREQ3 (master mode)	1-2
R115	I^2C EEPROM (IC12) address select E1: 1-2 = high 2-3 = low	1-2
R116	I^2C EEPROM (IC12) address select E3 1-2 = high 2-3 = low	1-2
R117	I^2C EEPROM (IC12) address select E2: 1-2 = high 2-3 = low	1-2
R141	I^2C EEPROM (IC24) address select A1: 1-2 = high 2-3 = low	1-2
R142	I^2C expander (IC24) address select A2: 1-2 = high 2-3 = low	1-2
R146	I^2C EEPROM (IC24) address select A0: 1-2 = high 2-3 = low	1-2
R225	MODE22 (R226) and MODE21 (R225) chip operating mode selection on Revision A to C boards only: 1-2 = high 2-3 = low 00 = standard 01 = FE standalone 10 = BE standalone 11 = FE+BE validation	2-3
R226		2-3

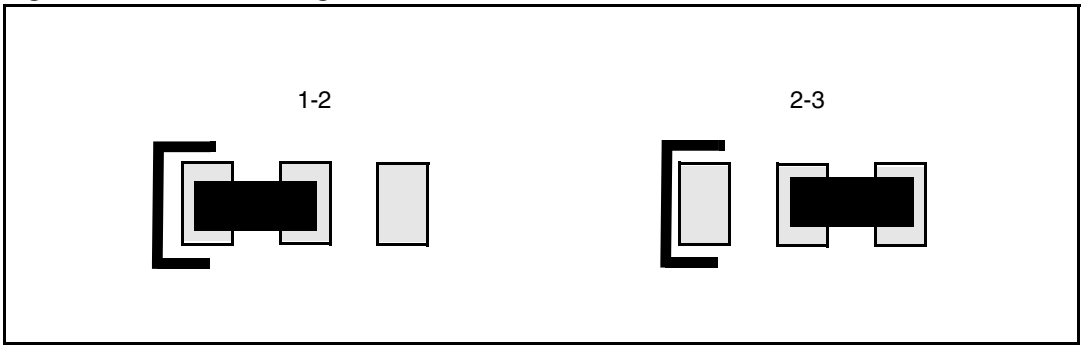
Table 40. Option resistor settings (continued)

Resistor	Description	Default
R227	MODE19 - EMI grant retraction enable on Revision A to C boards only: 1-2 = high 2-3 = low	2-3
R228	MODE20 - FE clock direction selection DIRCLOCK on Revision A to C boards only: 1-2 = high 2-3 = low	2-3
R234	SYSB_CLKIN source select: 1-2 = Crystal (XT2) 2-3 = Tuner RF2 clock output	1-2
R256	SYSA_CLKOSC (XT1) load capacitor pull up/down select: 1-2 = +2V5_CORE 2-3 = GND	2-3
R283	NAND Flash READYnotBUSY: 1-2 = high 2-3 = low	2-3
R344	MODE13 - EMI Serial Flash type selection: 1-2 = high - ST Flash 2-3 = low - Atmel	2-3
R345	MODE12 - NAND Flash controller address size selection: 1-2 = high 2-3 = low	2-3
R346	MODE11 select EMI NAND Flash controller page size: 1-2 = high 2-3 = low	2-3
R347	MODE7 (R348) and MODE6 (R347) - Reset bypass mode selection: 1-2 = high 2-3 = low	2-3
R348		2-3
R350	MODE15 EMI boot master/slave selection: 1-2 = high 2-3 = low	2-3
R352	MODE18 - EMI boot master/slave clock selection: 1-2 = high 2-3 = low	2-3
R356	MODE8 - RESETOUT mode selection: 1-2 = high 2-3 = low	2-3
R361	SYSB_CLKOSC (XT3) load capacitor pull up/down select: 1-2 = +2V5_CORE 2-3 = GROUND	2-3

Table 40. Option resistor settings (continued)

Resistor	Description	Default
R397	LNBH23 (IC26) I^2C address select: 1-2 = high 2-3 = low	2-3
R406	NIM2 I^2C address select0: 1-2 = high 2-3 = low	2-3
R412	NIM2 I^2C address select1: 1-2 = high 2-3 = low	2-3
R417	AS1 voltage select: 1-2 = +3V3 2-3 = GND	1-2
R422	HDMI I^2C logic level select: 1-2 = 5V 2-3 = 3V	1-2

Figure 41. Default configurations of the resistors



B.3 Switches

The STi7111-MBoard includes the switches listed in *Table 41*.

Table 41. Option switch settings

Switch reference		Description	Default
SW1		ATX power on/off switch	N/A
SW2		Front panel push button connected to PIO7(2)	N/A
SW3		Front panel push button connected to PIO7(3)	N/A
SW4		Front panel push button connected to PIO7(4)	N/A
SW5		Front panel push button connected to PIO7(5)	N/A
SW6		Front panel reset	N/A
SW8	1	AK4386 (IC50) DIF1 select (On = low, Off = high)	Off
	2	AK4386 (IC50) DIF0 select (On = low, Off = high)	
	3	AK4386 (IC50) DFS1 select (On = low, Off = high)	On
	4	AK4386 (IC50) DFS0 select (On = low, Off = high)	
SW9	1	CS8406 (IC51) AD0_notCS/TEST (On = low, Off = high)	On
	2	CS8406 (IC51) AD2_notEMPH (On = low, Off = high)	Off
	3	CS8406 (IC51) TEST/APMS (On = low, Off = high)	On
	4	CS8406 (IC51) TEST/CEN (On = low, Off = high)	
SW10	1	Spare	Off
	2	CS8406 (IC51) HnotS (On=low, Off=high)	
	3	Spare	
	4	CS8406 (IC51) DGND_SFMT1 (On=low, Off=high)	

Table 41. Option switch settings (continued)

Switch reference		Description	Default
SW11	1	Mode 1 and Mode 0 - Clockgena ref clock selection 00 = SYSA_CLKIN 01 = SYSB_CLKIN 10 = SYSA_ALTCLKIN 11 = Reserved	On
	2		
	3	Mode 3 and Mode 2 - PLL0 startup configuration (FPLL/FOSC in MHz) 00 = 900/27 01 = 604.8/27 10 = 900/30 11 = 600/30	
	4		
SW12	1	Mode 5 and Mode 4 - PLL1 startup configuration (FPLL/FOSC in MHz) 00 = 799.2/27 01 = 399.6/27 10 = 800/30 11 = 400/30	On
	2		
	3	Mode 10 and Mode 9 - BOOT mode selection: 00 = ST40 boot first 01 = Video ST231 boot first 10 = Audio ST231 boot first	
	4		
SW13	1	Mode 14 - EMI Boot device port size: 0 = 16 bits 1 = 8 bits	On
	2	Mode 17 and Mode 16 - EMI Boot mode selection 00 = NOR Flash (EMI controller) 01 = MPX (EMI controller) 10 = Serial Flash (SPI controller) 11 = NAND Flash (NAND controller)	
	3		
	4	Unused	N/A
The following switch is only available on Revision A to C boards			
SW7	1	notDvbMuxAEn (On=low, Off=high)	Off
	2	notDvbMuxBEn (On=low, Off=high)	
	3	PCI_Enable (On=low, Off=high)	On
	4	Mode3 or RMIInotMII select (On=low, Off=high)	

Table 41. Option switch settings (continued)

Switch reference		Description	Default
The following switches are only available on Revision D and later boards			
SW7	1	EPLD user defined pins	On
	2		Off
	3		On
	4		Off
SW15	1	Mode 19 - EMI grant retraction enable: On = 0	On
	2	Mode 20 - FE clock direction select: On = 0	
	3	Mode 21 and Mode 22, chip operating mode selection: On = 0	
	4	00 = standard 01 = FE standalone 10 = BE standalone 11 = FE+BE validation	
SW16	1	NOTDVBMUXAEN (SW7:1) and NOTDVBMUXBEN (SW7:2) (On=low, Off=high) 00 = NIM->DVB->TS0in 01 = TSInOut->DVB->TS0in 10 = NIM->TSinOut 11 = NIM->DVB->TSInOut	On
	2		Off
	3	PCI_Enable (On=low, Off=high)	Off
	4	Mode3 or RMIInotMII select: (On=low, Off=high) (Note that On disables the PushButton for STi7111 Reset.)	On

B.4 LEDs

The STi7111-MBoard includes the LEDs in *Table 42*.

Table 42. LEDs

LED	Color	Description
IC11	Red_green	PIO status LED
LD1	Green	LVDS_SPARE_IN
LD2		IR TX
LD3		IR RX
LD4	Green	PCI reset
LD5	Green	PCI granted signal
LD6	Green	PCI request
LD7	Green	EPLD (On = during reset, Off after reset is completed
LD8	Green	+5V power indication
LD9	Green	+12V power indication
LD10	Green	+2V5 power indication
LD11	Green	+3V3 power indication
LD12	Green	Ethernet (On = 100 Mbps)
LD13	Green	Ethernet (On = full duplex mode)
LD14	Green	NIMD error

Appendix C PIO alternate functions

The following tables show the PIO alternate functions used by the board for PIO0 to PIO7. A complete list of PIO assignments is in the *STi7111 datasheet* (ADCS 8065030).

Functions shown in **bold** are the board default settings. Shaded cells indicate functions that are only available on revision D and later boards.

Table 43. PIO functions for PIO0

Bit	Alternate function				Comments
	1	2	3	4	
0	**SmartCard0 DataOut**	UART0 TxD			PIO isolation jumpers J18A to J18H.
1	**SmartCard0 DataIn**	UART0 TxD			
2	**SmartCard0 Ext Clock**		PCI notReq3	Alt TSin Byte Clk	
3	**SmartCard0 ClockOut**				
4	**SmartCard0 Reset**	UART0 CTS	PCI notReq2		
5	**SmartCard0 VCC**				
6	**SmartCard0 VPP**		PCI notReq1		
7	**SmartCard0 Detect**	UART0 RTS			

Table 44. PIO functions for PIO1

Bit	Alternate function				Comments
	1	2	3	4	
0	**SmartCard1 DataOut**	UART1 TxD			PIO isolation jumpers J14A to 14H.
1	**SmartCard1 DataIn**	UART1 TxD			
2	**SmartCard1 Ext Clock**		PCI notLock		
3	**SmartCard1 ClockOut**				
4	**SmartCard1 Reset**	UART1 CTS			
5	**SmartCard1 VCC**	UART1 RTS	PCI PME		
6	SmartCard1 DIR		**SmartCard1 VPP**		
7	HDMI CEC		**SmartCard1 Detect**	Alt TSin Data 3	

Table 45. PIO functions for PIO2

Bit	Alternate function				Comments
	1	2	3	4	
0	I2C0_SCL		**SPI Boot CLK**		PIO isolation jumpers J25A to J25H.
1	I2C0_SDA		**SPI DataOut**		
2			**SPI DataIn**		
3		**MAFE HC1**		Alt TSin Byte Clk Valid	
4		**MAFE Data Out**		Alt TSin Data 0	
5		**MAFE Data In**	PCI notGNT3	Alt TSin Data 1	
6		**MAFE FS**	PCI notGNT3	Alt TSin Data 2	
7		**MAFE SClk**	PCI notGNT3	Alt TSin Data 3	

Table 46. PIO functions for PIO3

Bit	Alternate function					Comments
	1	2	3	4	5	
0	**I2C1_SCL**	IR Blaster	Video - Main Href	Video - Aux Href	PCI IntD	PIO isolation jumpers J15A to J15H.
1	**I2C1_SDA**		Video - Main Vref	Video - Aux Vref	PCI IntC	
2			Video - Main BnotT	Video - Aux BnotT	PCI IntB	
3		**IR In**				
4	**NANDnotWP**	IRB UHF In				
5		**IRB IR Out**				
6		IRB IR Out OD				
7					**PCI IntA**	

Table 47. PIO functions for PIO4

Bit	Alternate function				Comments
	1	2	3	4	
0	**I2C2_SCL**				PIO isolation jumpers J24A to J24H and J57.
1	**I2C2_SDA**				
2	**UART2 RxD**				
3	**UART2 TxD**				
4	**UART2 CTS**				
5	**UART2 RTS**			PCI IDSEL	
6			PWM0 Out		
7		**HDMI HPD**			

Table 48. PIO functions for PIO5

Bit	Alternate function					Comments
	1	2	3	5	6	
0	**UART3 TxD**				Alt TSin Data 4	PIO isolation jumpers J32A to J32H and jumpers J65, J66, J59, J10-C, J10-D and J10-G.
1	**UART3 RxD**				Alt TSin Data 5	
2	**UART3 CTS**				Alt TSin Data 6	
3	**UART3 RTS**		SysB ClkOut		Alt TSin Data 7	
4				**PCI notReset**	Alt TSin Error	
5				**PCI notSERR**		
6		**USB OVRCUR Detect**				
7		**USB Power Enable**				

Table 49. PIO functions for PIO6

Bit	Alternate function			Comments
	1	2	3	
0	KB ScanOut0	**Bi LED Red**		PIO isolation jumpers J10A to J10H.
1	KB ScanOut1	**Bi LED Green**		
2	KB ScanOut2	**Front Panel Switch SW2**	UART3 TxD	
3	KB ScanOut3	**Front Panel Switch SW3**	UART3 TxD	
4	KB ScanIn0	**Front Panel Switch SW4**		
5	KB ScanIn1	**Front Panel Switch SW5**		
6	KB ScanIn2		UART3 TxD	
7	KB ScanIn3	**SPI CS**	UART3 TxD	

Table 50. PIO functions for PIO7

Bit	Alternate function			Comments
	1	2	3	
0	**FE GPIO 0**	FE SDA	DISEQ Rx1- FSK TX	PIO isolation jumpers J10A to J10H.and jumpers J60, J65 and J66.
1	**FE GPIO 1**	FE SCK	FE UART TxD	
2	**FE GPIO 2**		FE UART RxD	
3	**FE GPIO 3**		DISEQ Rx2	
4	**FE GPIO 4**		FE UART CTS	
5	**FE GPIO 5**		FE UART RTS	

Appendix D Glossary

ATAPI	Advanced technology attachment packet interface
ATX	Advanced technology extended (motherboard type)
BGA	Ball grid array
CVBS	Composite video blanking synchronization
DAA	Direct access arrangement
EMI	External memory interface
EPLD	Electrically programmable logic device
FPGA	Field programmable gate array
HD	High definition
HDMI	High definition multimedia interface
LMI	Local memory interface
LVDS	Low voltage differential signalling
MAFE	Modem analog front end
Mbs	Megabits per second
MCM	Multi chip module
MII	Media independent interface
NIM	Network interface module
PCI	Peripheral component interconnect
PCMCIA	Peripheral component microchannel interconnect architecture
RMII	Reduced media independent interface
SATA	Serial advanced technology attachment (hard disk interface)
SD	Standard definition
STEM	Set-top expansion module
TS	Transport stream
UART	Universal asynchronous receiver-transmitter
VHDCI	Very high density cable interconnect

Revision history

Table 51. Document revision history

Date	Revision	Changes
17-Dec-2008	B	Updated throughout for Revision D and later boards.
20-May-2008	A	Initial release.

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