Team ID:

Student1 ID name: B05502145
Student2 ID name: B05901065

RTL category		
Design Stage	*File*	*Description*
RTL Simulation	MEMC.v	Verilog (or VHDL) synthesizable RTL code
Gate-Level category		
Design Stage	*File*	*Description*
Pre-layout Gate-level Simulation	MEMC_syn.v	Verilog gate-level netlist generated by Synopsys Design Compiler
	MEMC_syn.sdf	Pre-layout gate-level sdf
Physical category		
Design Stage	*File*	*Description*
P&R	DBS.tar	**archive of the design database directory**
	MEMC_pr.gds	GDSII layout Attach the screenshot of streamout gds below below this table
	0	Number of DRC error(s) Attach the screenshot below this table
	0	Number of LVS error(s) Attach the screenshot below this table
Post-layout Gate-level Simulation	MEMC_pr.v	Verilog gate-level netlist generated by Cadence Encounter or Synopsys IC Compiler
	MEMC_pr.sdf	Post-layout gate-level sdf

Post-route Setup time screenshot:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.055  |  0.055  |  3.296  |  3.458  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  6873   |  3443   |  3457   |   15    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 65.082%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

Post-route Hold time screenshot:

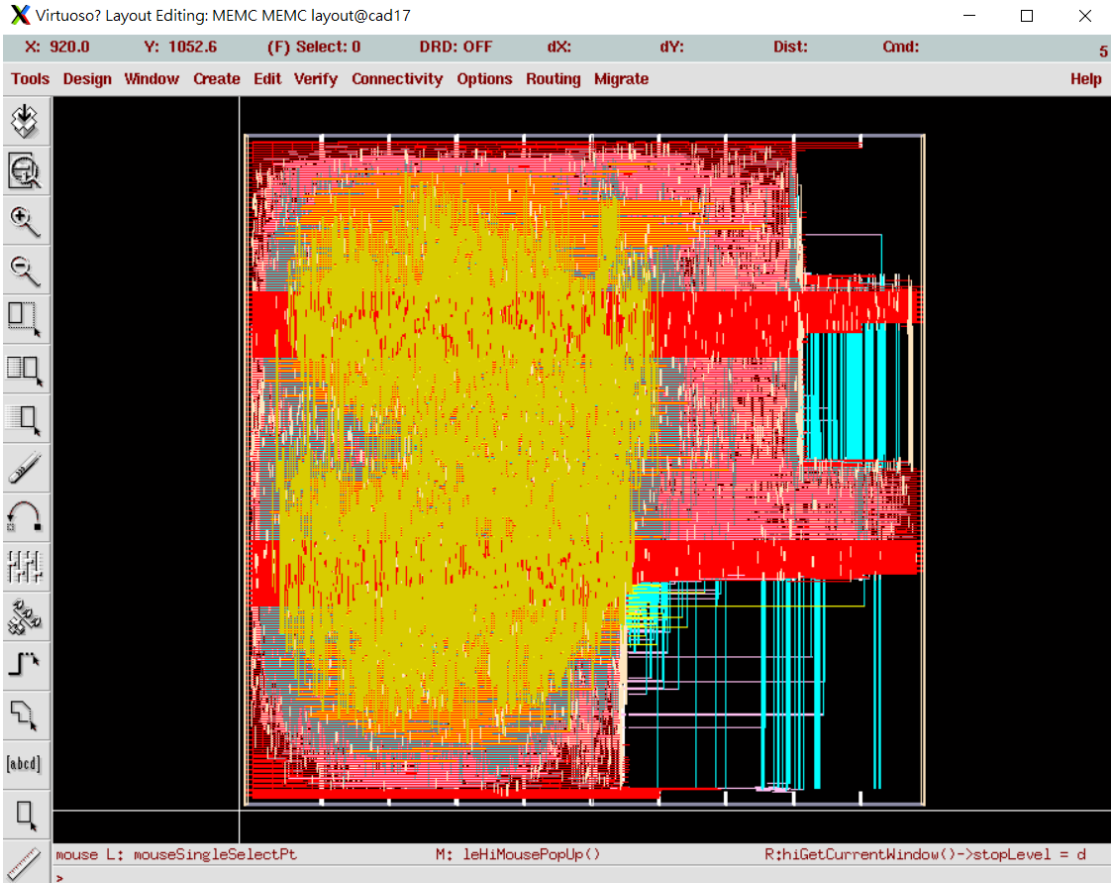
```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.326  |  0.428  |  0.326  |  1.165  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  6873   |  3443   |  3457   |   15    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 65.082%
------------------------------------------------------------
```

Stream out GDS screenshot:



DRC report screenshot:

```
innovus 1>  *** Starting Verify Geometry (MEM: 1785.4) ***

**WARN: (IMPVFG-257):   verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release.
update your script to use the new command.
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 8320
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 52.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:51.9  MEM: 1537.0M)
```

LVS report screenshot:

```
innovus 1> VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Tue Jan 14 00:22:35 2020

Design Name: MEMC
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (1024.8800, 1010.6500)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 00:22:36 **** Processed 5000 nets.
**** 00:22:37 **** Processed 10000 nets.
**** 00:22:37 **** Processed 15000 nets.
**** 00:22:37 **** Processed 20000 nets.
**** 00:22:38 **** Processed 25000 nets.
**** 00:22:38 **** Processed 30000 nets.
**** 00:22:39 **** Processed 35000 nets.
**** 00:22:39 **** Processed 40000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Tue Jan 14 00:22:40 2020
Time Elapsed: 0:00:05.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:05.1  MEM: -0.473M)
```

Annotation (optional, for TA to reproduce you design easily):

Briefly explain your design and the problem you encounter:

- RTL design:

Our algorithms calculate 8x8 blocks in order.
We apply the hexagon searching algorithm to find the best matched block.
SRAM read current frame and write previous frame can be done in the same time, and it can save a lot of time.
SAD calculation has been pipelined so it can run faster.
RTL problem:

- RTL encountered problem:

Tackle with boundary conditions is difficult and might easily cause overflow problem.

- Synthesis encountered problem:

Pipelining critical path in our design is difficult, need to keep fixing RTL code and re-synthesis.
Compile ultra may have slack 0 but need to pass the test bench for much more times than the time specified in sdc file.

- APR encountered problem:

NanoRoute may encounter cut short problem, add blockage and reroute to fixed the DRC.