An Energy Efficient ONU Implementation

Neelakandan Manihatty Bojan, D. Pham Van, L. Valcarenghi, and P. Castoldi
Scuola Superiore Sant'Anna,
Pisa, Italy
Email: n.manihattybojan@master.sssup.it, {d.phamvan, luca.valcarenghi, castoldi}@sssup.it

***Abstract*—This paper describes the implementation of an energy efficient Optical Network Unit (ECONU) on an Altera Stratix 4GT Field Programmable Gate Array (FPGA). An overview of the ECONU architecture along with its frame format design is also provided. The Finite State Machine (FSM) implementation for switching the ONU "on" and "off" is based on the sleep request encoded in the frames. The performance of the ECONU prototype is evaluated through hardware testbed and the obtained results are also discussed.**

***Keywords*-Energy Efficient Ethernet, PONs, FSM, Altera, FPGA**

I. Introduction

Telecom providers are seeking to reduce communication network energy consumption not only to lower greenhouse gas emissions but also to decrease their operating expense (OPEX). Access networks (fixed and mobile) are recognized as the major contributors to current communication networks energy consumption [1]. This is mainly due to the high number of involved elements (i.e., the customer premises equipments — CPEs). Access networks based on Passive Optical Networks (PON) are expected to drastically reduce the access network energy consumption with respect the ones based on digital subscriber line (DSL). However, fixed optical access networks are forecast to be the largest contributors to fixed optical communications networks energy consumption for the next ten years yet [2].

In Time Division Multiple Access (TDMA) PON, Optical Network Units (ONUs) (i.e., PON CPEs) are the devices with the highest energy consumption per bit. Indeed, they are numerous and often remain idle, because of the low utilization of PON capacity and the shared medium architecture. In [2] it is shown that the ONUs consume over 65% to the total PON power consumption. ONUs are therefore a major target for energy savings in PONs and significant improvement in energy efficiency can be achieved by just turning "off" idle ONUs.

Several papers have shown the advantages and the drawbacks of turning ONUs "on" and "off" [3]–[5]. Some experimental evaluations have been formerly presented in [6] and [7]. In [7], the cyclic sleep technique with adaptable sleep period is implemented by utilizing an SFP board transceiver at 1.25 Gb/s. The transceiver is connected to differential serial interface of an Altera Transceiver Signal Integrity Development Kit, Stratix IV GT Edition, capable of supporting a transmission rate of 1.25 Gb/s. The implemented ONU is capable of effectively receiving `SLEEP REQUEST` and replying with `NACK` and `ACK`. In [6], a sleep control (i.e., Sleep and Periodic Wake-up) in conjunction with Adaptive Link Rate (ALR) control for EPONs is implemented. Sleep control switches the ONU mode (i.e., active or sleep mode), depending on the presence or absence of traffic. The ALR switches between two downlink rates (i.e., 1G and 10G), depending on the quantity of traffic. The aim of such combination is to overcome the drawbacks of the sleep and ALR control functions when implemented individually.

This paper describes the implementation of an energy efficient Optical Network Unit (ECONU) on an Altera Stratix 4GT Field Programmable Gate Array (FPGA). The implementation is based on the Finite State Machine (FSM) described in [8] and it is a simplified version of the Low Power Idle (LPI) FSM defined in [9]. The design considers downstream traffic only. The FSM implementation for switching the ONU "on" and "off" is based on the sleep request encoded in the frames. Results show that the ECONU successfully switches between the FSM states based on the sleep request received from the OLT along with the predefined timers within the ONU.

II. ECONU Architecture

This section describes the ECONU architecture. The datapath from OLT to ONU is sketched followed by a brief description of the major components along the path. The packet format and the sleep FSM are described to show the transition among the ONU states.

A. Layer Stack

The ECONU implementation is based on IEEE 802.3az-2010 standard stack [9]. The implementation described in this paper considers downstream transmission only. The datapath from OLT transmitter to ONU receiver is illustrated in Fig. 1.

At the OLT transmitter, the client traffic is provided by an Ethernet packet generator that drives the 10GbE subsystem by transmitting a stream of Ethernet frames to the OLT transmitter FIFO. The transmitter 10Gb/s Ethernet MAC (10GbE MAC) receives the generated packets, stores them in the FIFO, and appends control fields to form an EPON

978-3-901882-46-3

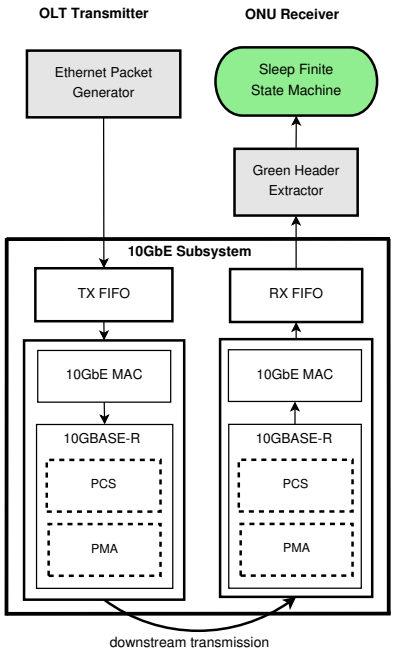

Figure 1. Layering Architecture

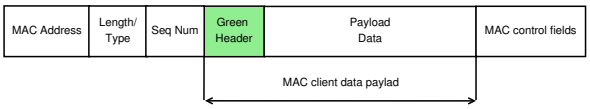

Figure 2. Packet Format

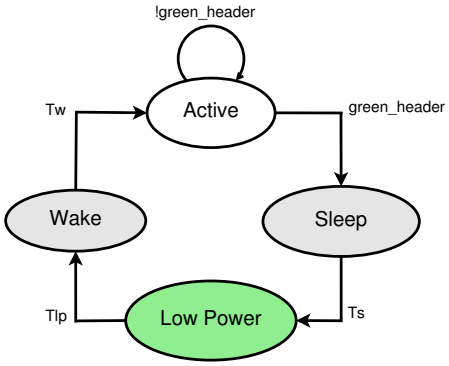

Figure 3. Sleep Finite State Machine

frame. It also pads bit to meet the minimum frame length, if necessary. The MAC frame is passed to the 10GBASE-R which is further divided into Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer. Both the PCS and the PMA process the frame, serialize the data, and transmit them along the medium to the ONU.

The ONU receiver works complementary to the OLT transmitter, with some significant modification done on the ONU to implement the sleep technique. After stripping off the control fields and padding, which were inserted at the MAC transmitter, the packet is stored in the ONU receiver FIFO in the same format as in the generator. A packet extractor module is implemented to extract the *green header* (control header), which regulates the ONU behavior. The content of the green header is processed by the Sleep FSM at the ONU side, that determines if the ONU must be switched to "on" or "off" state.

B. Packet Format

The frame sent by the OLT to the ONU is a standard Ethernet frame except for the inclusion of the green header as shown in Figure 2. The green header carries the control information that allows the OLT and ONU to exchange the sleep control signals maintaining the standard Ethernet packet format.

C. Sleep Finite State Machine

The sleep FSM implemented at the ONU receiver is based on [8] and it is a simplified version of the LPI FSM defined in [9]. At any given time, the ONU can only be in one of the four states as shown in Figure 3.

The ONU receives data only in Active state. Only after receiving a sleep request from the OLT, the ONU switches from Active state to Sleep state. The sleep request is carried by the green header in the EPON frame. The ONU stays in the Sleep state for a period of T_s, which is the time required by the ONU to turn off its transceivers. When the T_s expires, the ONU switches to the Low Power state and sleeps for a period T_{lp}, resulting in low power consumption. When the ONU is in Low Power state, the received downstream packets can either be buffered or ignored. This implementation adopts the latter. When the T_{lp} expires, the ONU switches from Low Power state to Wake state for a period of T_w, which is the time required by the ONU to turn on the transceivers and to synchronize with the network. The T_s, T_{lp} and T_w values are defined as in [9].

III. ECONU Implementation

The ECONU is implemented on an Altera Transceiver Signal Integrity Development Kit, Stratix IV GT edition board (EP4S1002F40I1). This board is capable of supporting 10GbE transmission rate. The Electronic Design Automation (EDA) tools used are ModelSim (for functional simulation and verification) and Quartus 2 (for synthesis and configuring the FPGA). Verilog Hardware Description Language (Verilog HDL) and System Verilog are used to model the behavior of the design in ModelSim EDA tool.

OLT and ONU functions partly use Altera Intellectual Property (IP cores), like Altera 10GbE MAC and Altera 10G BASE-R PHY IP cores. The 10GbE MAC implements the Ethernet MAC, while the 10GBASE-R PHY implements the physical layer functions, i.e., the PMA and PCS as specified in IEEE 802.3-2008 standard. Altera provides 10GbE subsystem (as a reference design), which integrates 10GbE

MAC and 10G BASE-R PHY. The design also includes transmitter and receiver FIFO buffers, MAC, PCS and PMA as shown in Figure 1.

The MAC frame format of the 10GbE IP core is different from the one defined in the IEEE 802.3-2008 standard as depicted in Figure 4. When compared to the standard Ethernet frame format, the packet received by the 10GbE TX MAC from the OLT FIFO has an additional 2-byte sequence number field. This allows Avalon-Streaming interface (Avalon-ST) to keep track of the generated packets.

The packet generator (implemented through the Avalon-ST protocol) generates a packet with MAC addresses (i.e., destination and source), length/type, payload data, sequence number, and it calculates and appends the CRC after the payload. The packet is then forwarded to the TX MAC. In addition, a 7-byte start of payload field and 1 byte green header are inserted at the beginning of the payload. The start of payload is defined as a sequence of 56 bit "1s", while the remaining 1 byte contains the green header which encodes the control bit. This control bit allows the OLT to request the ONU to switch to sleep state (when "1") or to maintain its current state (when "0").

The FIFO's temporarily store packets and it interfaces the Ethernet packet generator and the 10GbE MAC through Avalon Streaming (Avalon-ST) protocol. It connects the generator of the data stream (source) to a receiver of the data (sink).

The 10GbE MAC and the 10GBASE-R interface each other by using the single data rate (SDR) version of the 10 Gigabit Media Independent Interface (XGMII) protocol. The SDR XGMII consists of 64-bit data bus and 8-bit control bus operating at 156.25 MHz. The SDR XGMII is slightly different from the Double Data Rate (DDR) XGMII that utilizes two 32-bit interface with the frequency of 156.25 MHz as defined in IEEE 802.3-2008 Clause 46. All components use Avalon Memory-Mapped (Avalon-MM) control and status register interface. This is a master-slave interface that uses byte addressing to enable host PC to access 32-bit configuration and status registers, and statistics counters by means of Quartus II on-chip debugging tools.

At the ONU, the Avalon-ST FIFO receives, buffers and transmits data between the MAC and the client, i.e., the generator and the sleep FSM. This implementation uses FIFO buffers which are 64-bit wide and 512-word deep. The ONU receiver strips off the frame overheads and forwards the data to the header extractor module to extract the green header. The extractor examines every 64-bit data unit from the RX FIFO, and only those units whose first 56-bits have all "1's" are detected by the extractor module as green header. The extractor then forwards the green header to the Sleep FSM.

Based on the content of the green header's control bit, the Sleep FSM switches states. If a "1" is received in the Active state, the FSM switches to the Sleep state else it remains in

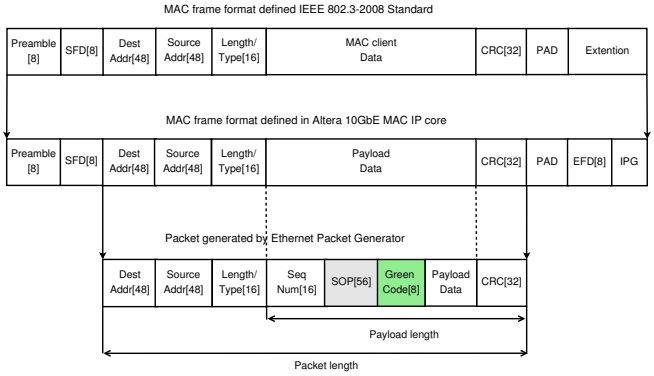

Figure 4. Frame Format

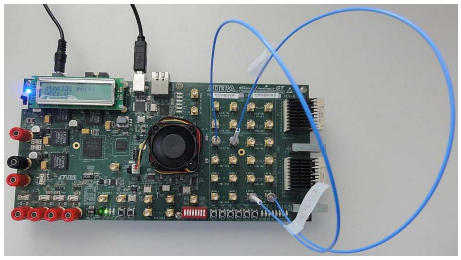

Figure 5. ECONU Testbed

the same state. Counters are used to implement the fixed values of the timers for regulating the sojourn time in the other states ($T_s = 2.88\mu s$, $T_{lp} = 39.68\mu s$ and $T_w = 4.48\mu s$) as recommended by IEEE 802.3az standard [9].

IV. ECONU Performance Evaluation

Figure 5 shows a picture of the ECONU prototype testbed. The OLT differential SMA transmitter and the receiver are directly connected through coaxial cables and not through an Optical Disribution Network (ODN). The 10Gb/s transmission link between OLT and ONU is realized on a single FPGA board with two modes: internal loopback and local loopback. The internal loopback mode is the one in which the transmission takes place within the board itself without an external coaxial cable. The local loopback mode is the one in which the OLT transmitter transmits data out of the board through SMA connectors and external coaxial cables (capable of supporting 10Gb/s links) to reach ONU receiver, again on the same board.

A. Hardware Test Scenario

The experimental results in terms of transmission statistics and the energy efficiency are collected by using the SignalTap II Embedded Logic Analyzer. SignalTap II Logic Analyzer is an on-chip debugging tool in Altera Quartus II that enables to capture and display the content of signals of a design running on the FPGA. The design can transmit packets in burst, with configurable packet length, number

Table I
PERCENTAGE OF EACH ONU STATE.

Test Config	Packet Size (bytes)	1500	1500	1500
	Transmitted Packets	100	1000	10000
State sojourn percentage (%)	Active	3.6	1.5	1.7
	Sleep	8.2	6.6	6.1
	Low Power	79.2	83.0	82.8
	Wake	9.0	8.9	9.4

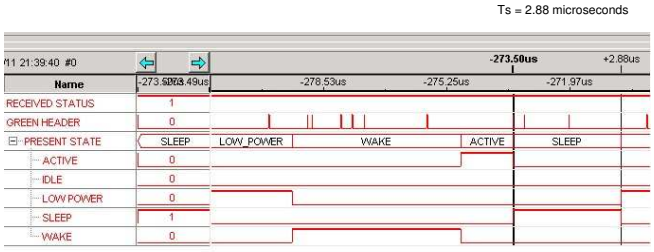

Figure 6. Transition of ONU state observed in SignalTap II Logic Analyzer

of packets to be transmitted, number of bursts, MAC destination and source address. The green header's control bit is generated by a Linear Feedback Shift Register (LFSR). The hardware test runs in both internal loopback and local loopback modes for various configurations of transmission. The test is run by transmitting 1500 byte fixed length packets at 10 Gbps by varying the burst size (i.e., the number of transmitted packets) from 100, 1000 to 10000 packets. The internal and local loopback modes give similar results, hence the statistics are shown regardless of the test mode.

B. Experimental Results

The energy efficiency statistics in terms of ONU state sojourn percentage in case of fixed packet length of 1500 bytes with various number of transmitted packets are presented in Table I. The results show that the ECONU is in the Low Power state most of time (i.e., up to 83%). The energy efficiency can be inferred from the state sojourn percentage, considering that the ONU consumes full power in all the states except the Low Power state. The energy efficiency when 1000 packets are transmitted is about 75% if 1/10 th ratio is assumed between full power and sleep power.

The transition among the states of the ECONU is verified in SignalTap II logic analyzer as shown in the Figure 6. The figure shows that the ONU switches among the states based on the control bit of the green header in the received frame. For example, the sleep time T_s is observed to be exactly $2.88\mu s$ as specified in the standard [9]. The other state durations also match with the recommended values.

V. CONCLUSION

This paper described an implementation of an energy efficient ONU on a Altera FPGA. The implementation has been detailed with the architecture for the proposed design, modules developed, EDA tools used, and the results obtained through hardware tests for different configurations. A specific packet format was defined with the insertion of the green header inside the user payload data of the Ethernet frame. This enabled the exchange of sleep request between OLT and ONU by driving the Sleep FSM. Results show that the Sleep FSM has been successfully implemented on this hardware.

ACKNOWLEDGMENT

The work was sponsored in part by the Tuscany regional project ARNO T3: Architecture of Networks and optical nodes for high-capacity transmission, the access-metro-core transport based integrated photonic technologies.

REFERENCES

[1] C. Lange, D. Kosiankowski, R. Weidmann, and A. Gladisch, "Energy consumption of telecommunication networks and related improvement options," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 17, no. 2, pp. 285–295, Mar.-Apr. 2011.

[2] R. Tucker, "Green optical communications—Part II: Energy limitations in networks," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 17, no. 2, pp. 261–274, Mar.-Apr. 2011.

[3] S. W. Wong, L. Valcarenghi, S. H. Yen, D. R. Campelo, S. Yamashita, and L. Kazovsky, "Sleep mode for energy saving PONs: Advantages and Drawbacks," in *GLOBECOM Workshops, 2009 IEEE*, 2009, pp. 1–6.

[4] B. Skubic and D. Hood, "Evaluation of ONU power saving modes for gigabit-capable passive optical networks," *Network, IEEE*, vol. 25, no. 2, pp. 20–24, Mar.-Apr. 2011.

[5] L. Shi, B. Mukherjee, and S. S. Lee, "Energy-efficient PON with sleep-mode ONU: progress, challenges, and solutions," *Network, IEEE*, vol. 26, no. 2, pp. 36–41, Mar.-Apr. 2012.

[6] R. Kubo, J. Kani, H. Ujikawa, T. Sakamoto, Y. Fujimoto, N. Yoshimoto, and H. Hadama, "Study and demonstration of sleep and adaptive link rate control mechanisms for energy efficient 10G-EPON," *Optical Communications and Networking, IEEE/OSA Journal of*, vol. 2, no. 9, pp. 716–729, Sep. 2010.

[7] M. Fiammengo, A. Lindstrom, P. Monti, L. Wosinska, and B. Skubic, "Experimental evaluation of cyclic sleep with adaptable sleep period length for PON," in *Optical Communication (ECOC), 2011 37th European Conference and Exhibition on*, sept. 2011, pp. 1–3.

[8] M. Marsan, A. Anta, V. Mancuso, B. Rengarajan, P. Vasallo, and G. Rizzo, "A simple analytical model for energy efficient ethernet," *Communications Letters, IEEE*, vol. 15, no. 7, pp. 773–775, Jul. 2011.

[9] *IEEE Std 802.3az-2010 (Amendment to IEEE Std 802.3-2008)*, pp. 1–302, Oct. 27 2010.