Graphic Dot Matrix Chip In Glass VFD   MN12864K

- ❑ **128 x 64 Graphic Dot Matrix**
- ❑ **Chip in Glass Driver IC**
- ❑ **High Brightness Green Display**
- ❑ **Synchronous Serial Interface**
- ❑ **Low Pinout Count**
- ❑ **Wide Operating Temperature**

This VF glass includes a 384 & a 48 bit serial shift register, latched drivers which connect to the anode and grid electrodes. An external host is required to provide a multiplexing data stream to refresh the display. The signal inputs can be connected to the ports of a CMOS microprocessor. The a.c. filament supply (F1, F2) can be derived from a source of 10KHz to 200KHz. Consult our application notes for further information.


Dimensions in mm. See full spec for tolerances
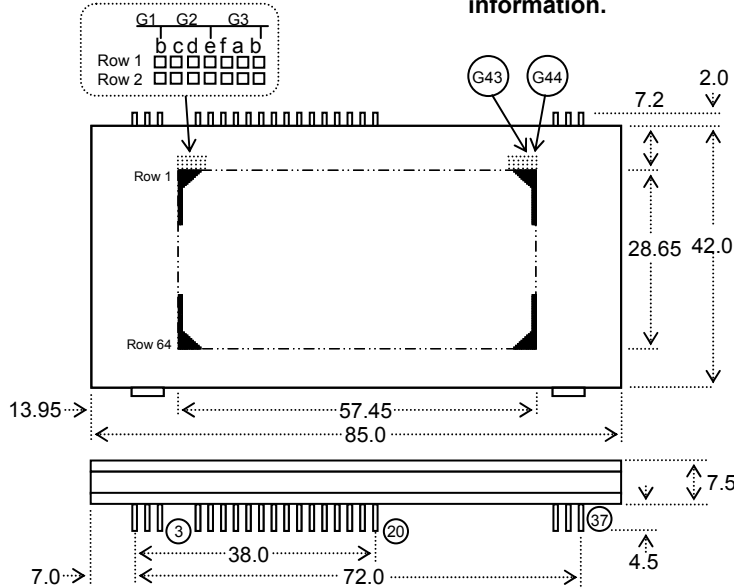
PIN OUT

Pin	Sig	Pin	Sig
1	F1	13	GCLK
2	F1	14	GLAT
3	F1	15	GBLK
4	NP	16	V$_{DD1}$
5	NP	17	V$_{SS}$
6	BLK	18	V$_{SS}$
7	LAT	19	V$_{DD2}$
8	CLK	20	V$_{DD2}$
9	SIN	35	F2
10	SOUT	36	F2
11	GSOUT	37	F2
12	GSIN		

ELECTRICAL SPECIFICATION

Parameter	Sym	Min	Typ	Max	Unit	Condition
Logic Voltage	V$_{DD1}$	4.5	5.0	5.5	V	V$_{SS}$=0V
Logic Current	I$_{DD1}$	-	4.0	8.0	mA	V$_{DD1}$=5V
Filament Voltage	E f	2.6	2.9	3.2	Vac	V$_{DD2}$=0V
Filament Current	I f	248	275	303	mAac	V$_{DD2}$=0V
Display Voltage	V$_{DD2}$	-	45.0	50.0	V	V$_{SS}$=0V
Display Current	I$_{DD2}$	-	20.0	30.0	mA	V$_{DD2}$=60V
Filament Bias	E$_K$	3.5	4.0	4.5	V	V$_{SS}$=0V
Logic High Input	V$_{IH}$	V$_{DD1}$+2.4	-	V$_{DD1}$	V	V$_{SS}$=0V
Logic Low Input	V$_{IL}$	0	-	+0.7	V	V$_{SS}$=0V
Logic High Input	I$_{IH}$	-	-	5.0	µA	V$_{DD1}$=5V
Logic Low Input	I$_{IL}$	-250	-70	-35	µA	V$_{DD1}$=5V
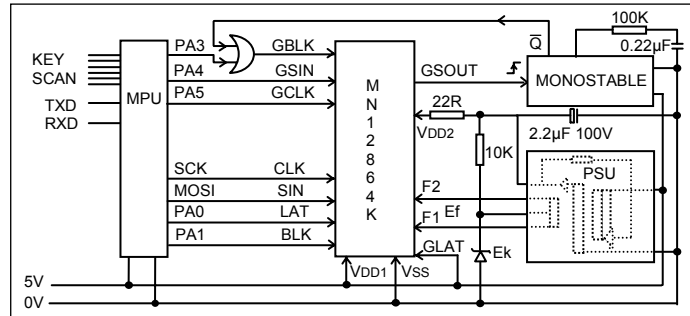
ENVIRONMENTAL and OPTICAL SPECIFICATION

Parameter	Value
Display Area (XxY mm)	57.45 x 28.65
Dot Size/Pitch (XxY mm)	0.3 x 0.3/0.45 x 0.45
Luminance	800 cd/m^2 Typ.
Colour of Illumination	Green (Filter for colours)
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +85°C
Operating Humidity (non condensing)	5 to 95% @ 25°C

1. The power on rise time should be less than 50ms.
2. The 22R resistor at the V$_{DD2}$ input is required to prevent current surge during switching.
3. If scanning of the display stops with V$_{DD2}$ applied, the BLK input must be set high to prevent damage to the display.

INTERFACE EXAMPLE
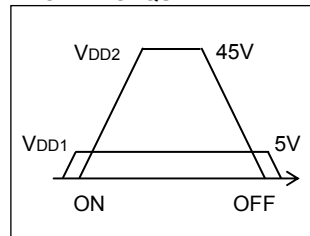

MULTIPLEX TIMING
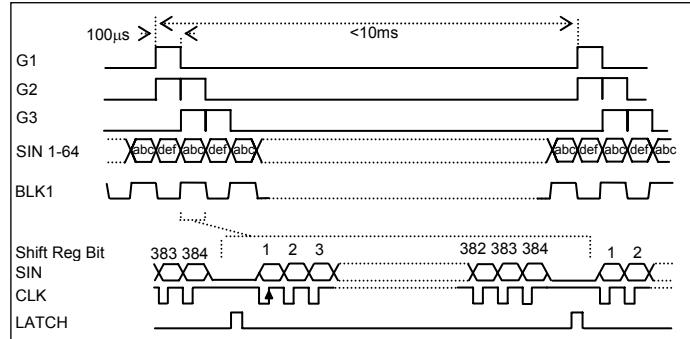
SHIFT REGISTER ASSIGNMENT

Electrode	Bit Numbers
Grid G1-G44	GSIN 1-44
Not Connected	GSIN45-48
Row 1 'afbecd'	SIN 1-6
Row 2 'afbecd'	SIN 7-12
Row 3 'afbecd'	SIN 13-18
:	:
Row 63 'afbecd'	SIN 373-378
Row 64 'afbecd'	SIN 379-384

INTERFACE TIMING

Parameter	Time
CLK Cycle	200ns min
CLK High	80ns min
CLK Low	80ns min
SIN Setup	40ns min
SIN Hold	30ns min
LAT High	300ns min
CLK then LAT	250ns min
BLK Hold	5µs min

POWER SEQUENCE

NORITAKE ITRON VFD   128 x 64 Dot Graphic