

J9

Pin	Signal
5	S3_I021
4	S3_I047
3	S3_I048
2	S3_I045
1	GND

Conn\_01x05\_Female

Conn\_01x06\_Female

J3

1

2 SPLCS

3 SPLCLK

4 SPLSI

5 SPLSO

6 HOST\_HRDY

GND

Diagram of J6 pin connections:

- Pin 7: +3.3V
- Pin 6: +3.3V
- Pin 5: SPI\_CS2
- Pin 4: SPI\_CLK
- Pin 3: SPI\_SI
- Pin 2: SPI\_SO
- Pin 1: HOST\_HRDY2

A ground symbol is shown next to the SPI signals.



5V

4

3

2

1

GND

DW X

DP X

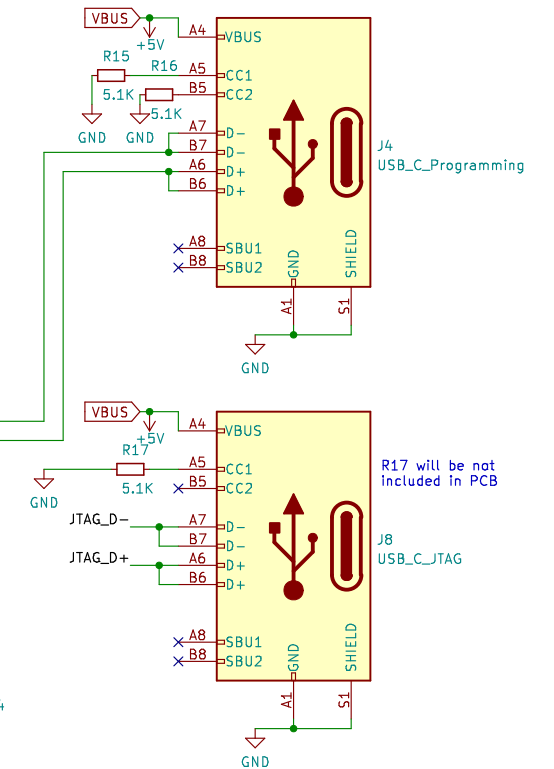
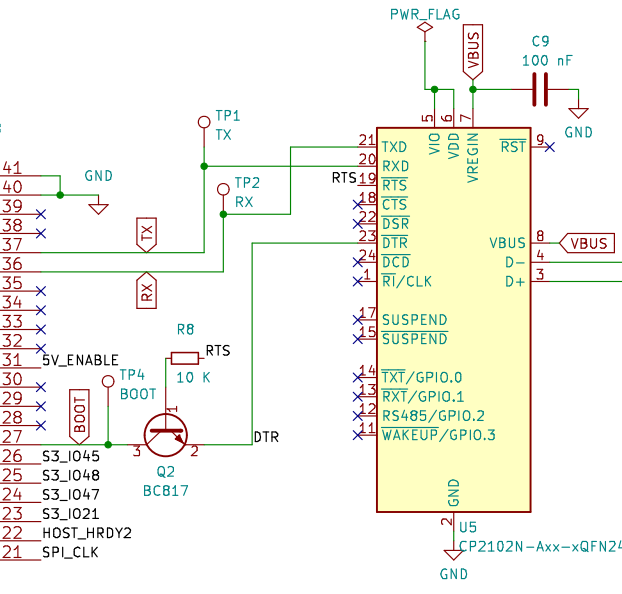
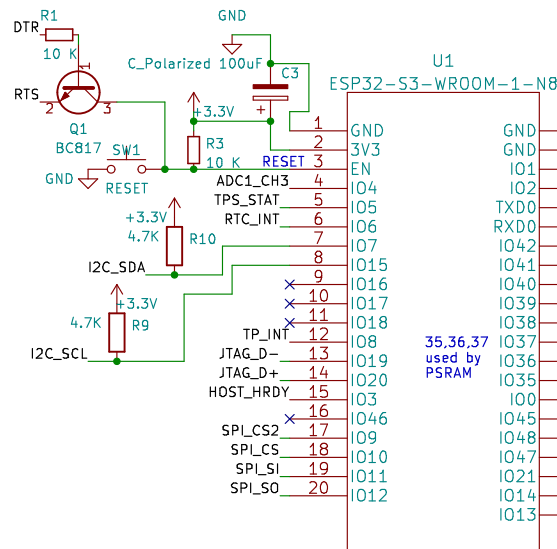
DP X

J2

Conn\_01x04\_Male POWER

Diagram of J7 connector pin connections. Pin 1 is connected to GND. Pin 2 is connected to GND. Pin 3 is connected to GND.

The diagram shows the internal circuit of the BAT+ pin. It is connected to a 442K resistor (R13) and a 160K resistor (R14) in series to ground. A green line connects the junction of the two resistors to the ADC1\_CH3 pin, which is also labeled GPIO4 In S3.



GPIO3 Controls where JTAG signal goes  
0: JTAG signal from on-chip JTAG pins  
1: JTAG signal from USB Serial/JTAG controller

A circuit diagram showing a DC Jack (J1) connected to a battery (BAT+) and ground (GND). The Jack-DC pin 1 is connected to GND, and pin 2 is connected to BAT+.



The diagram illustrates a battery management system (BMS) for a 3.3V S3 MCU. The system includes a TPS2113APWR (U2) connected to a BAT+ input and a TPS2113APWR (U4) connected to a +3.3V output. A TP4057ST26P (U9) is connected to the BAT+ input and a BAT+ output. The circuit includes various components like capacitors (C1, C2, C4, C5, C6), resistors (R2, R4, R5, R6, R7, R19), diodes (D1, D2, D3), and a Jumper (JP1). The BMS is connected to a 3.3V S3 MCU.

STAT is an open-drain output that is Hi if the IN2 switch is ON

[illegible]

STAT should be LOW if  
PWR\_OUT comes from USB

IMPORTANT: By default VBUS is not connected to 5V  
Solder jumper JP2 to allow 5V from USB