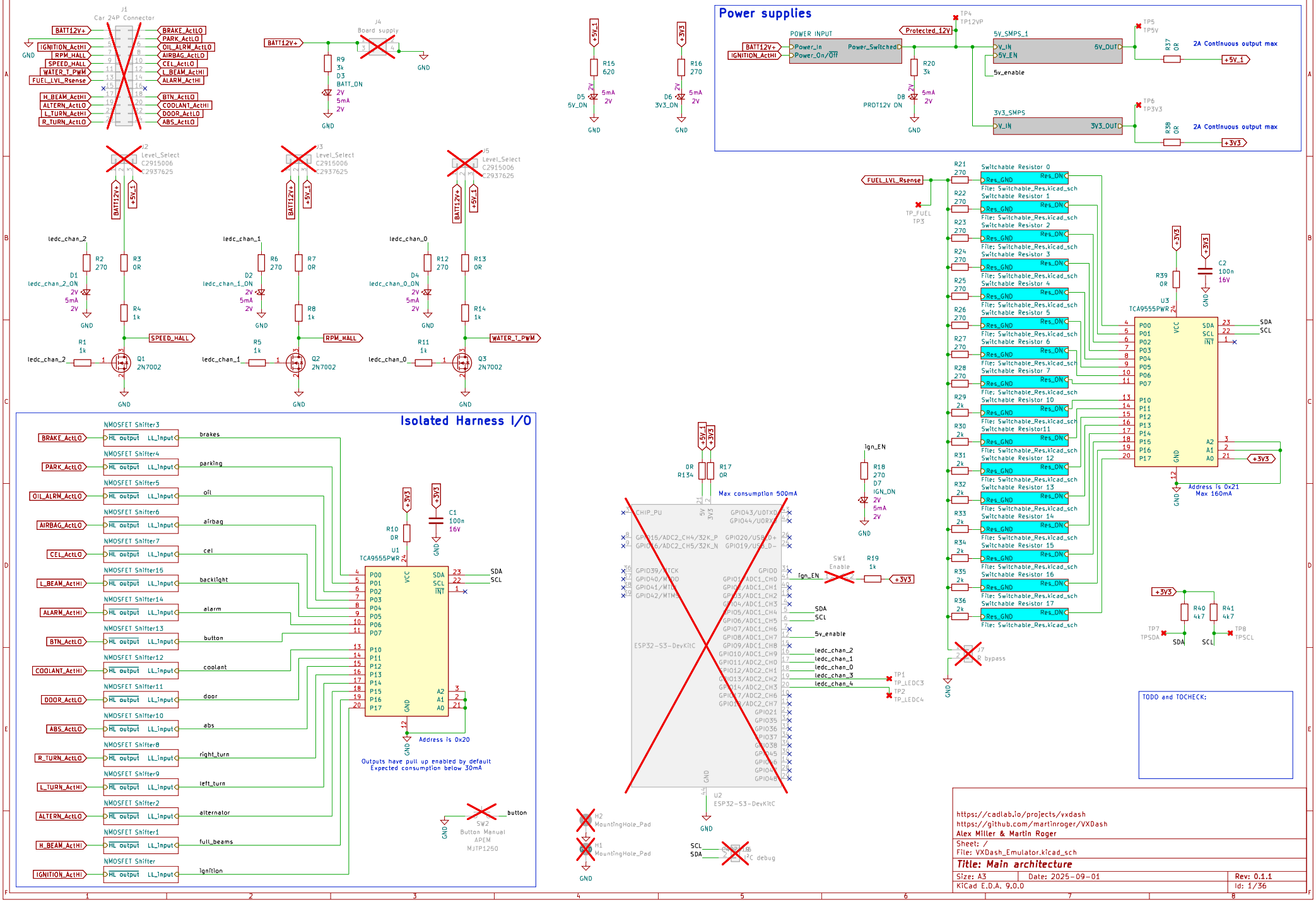
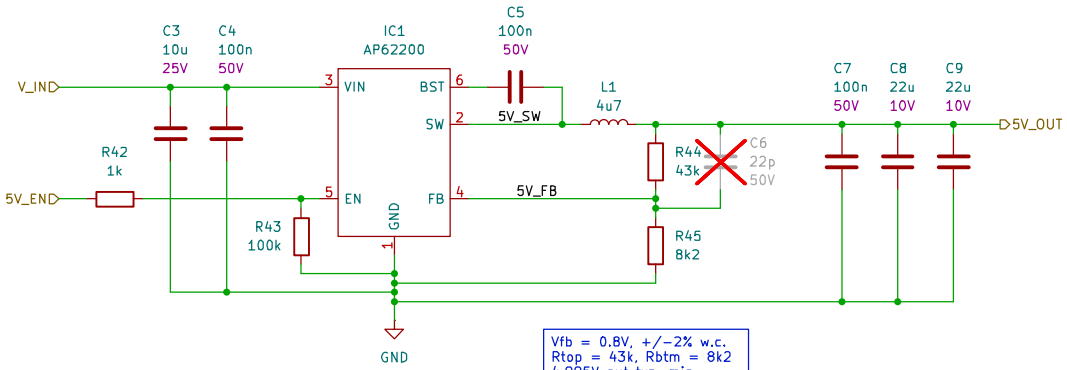

Power supplies
POWER INPUT
BATT12V+
IGNITION_ActHI
Power_In
Power_On/Off
Power_Switched
Protected_12V
5V_SMPS_1
V_IN
5V_EN
5V_OUT
5v_enable
3V3_SMPS
3V3_OUT
2A Continuous output max
Isolated Harness I/O
BRAKE_ActLO
PARK_ActLO
OIL_ALRM_ActLO
AIRBAG_ActLO
CEL_ActLO
L_BEAM_ActHI
ALARM_ActHI
BTN_ActLO
COOLANT_ActHI
DOOR_ActLO
ABS_ActLO
R_TURN_ActLO
L_TURN_ActHI
ALTERN_ActLO
H_BEAM_ActHI
IGNITION_ActHI
NMOSFET Shifter3
NMOSFET Shifter4
NMOSFET Shifter5
NMOSFET Shifter6
NMOSFET Shifter7
NMOSFET Shifter15
NMOSFET Shifter14
NMOSFET Shifter13
NMOSFET Shifter12
NMOSFET Shifter11
NMOSFET Shifter10
NMOSFET Shifter8
NMOSFET Shifter9
NMOSFET Shifter2
NMOSFET Shifter1
NMOSFET Shifter
HL output
LL_Input
brakes
parking
oil
airbag
cel
backlight
alarm
button
coolant
door
abs
right_turn
left_turn
alternator
full_beams
ignition
TCA9555PWR
Address is 0x20
Outputs have pull up enabled by default
Expected consumption below 30mA
Address is 0x21
Max 160mA
ESP32-S3-DevKitC
Max consumption 500mA
SW1
Enable
SW2
Button Manual
APEM
MJTP1250
I2C debug
Switchable Resistor 0
Switchable Resistor 1
Switchable Resistor 2
Switchable Resistor 3
Switchable Resistor 4
Switchable Resistor 5
Switchable Resistor 6
Switchable Resistor 7
Switchable Resistor 10
Switchable Resistor11
Switchable Resistor 12
Switchable Resistor 13
Switchable Resistor 14
Switchable Resistor 15
Switchable Resistor 16
Switchable Resistor 17
TODO and TOCHECK:
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger
Sheet: /
File: VXDash_Emulator.kicad_sch
Title: Main architecture
Size: A3
Date: 2025-09-01
Rev: 0.1.1
KiCad E.D.A. 9.0.0
Id: 1/36



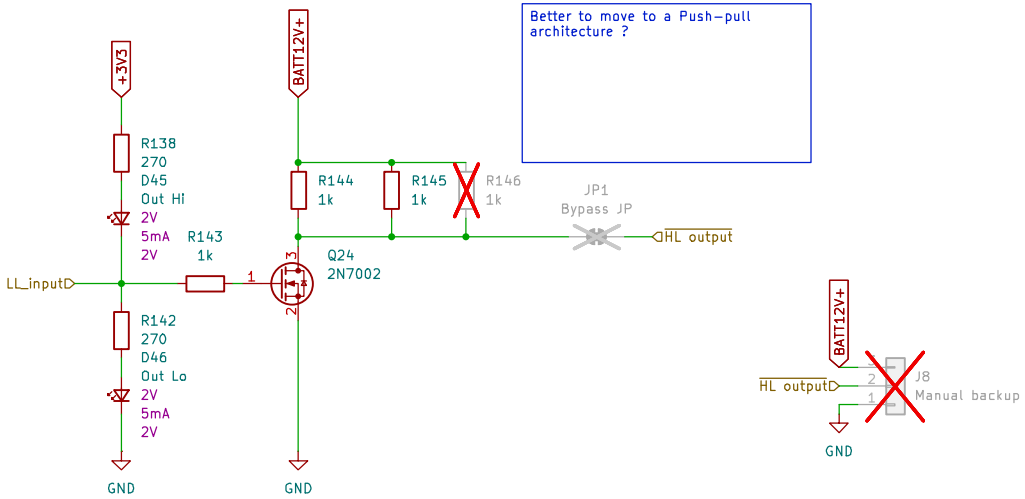
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /5V_SMPS_1/
File: 5V_SMPS.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 1.4**
KiCad E.D.A. 9.0.0		Id: 2/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



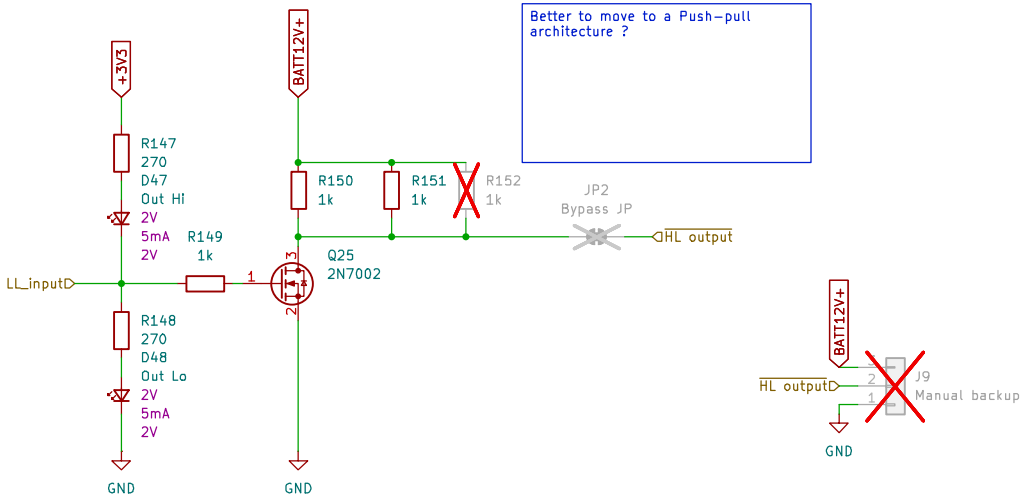
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter1/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 3/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



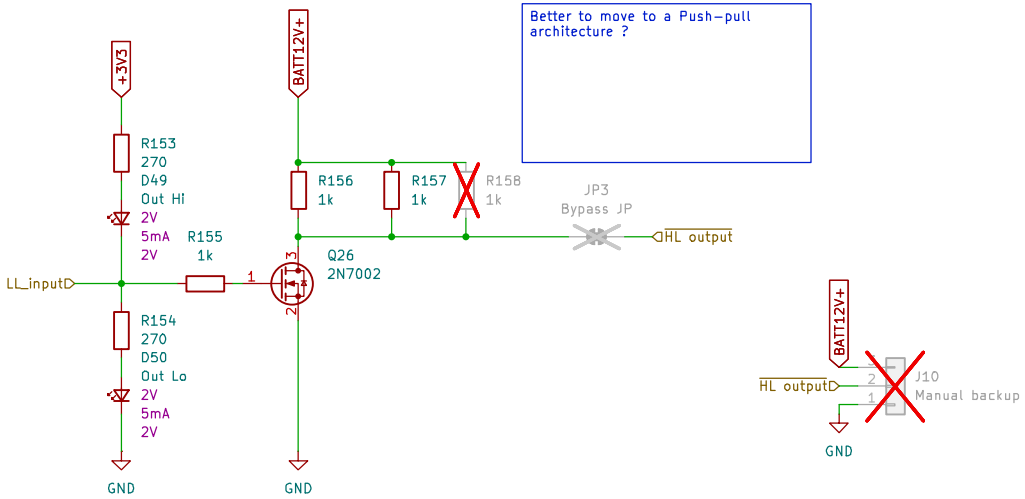
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter2/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 4/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



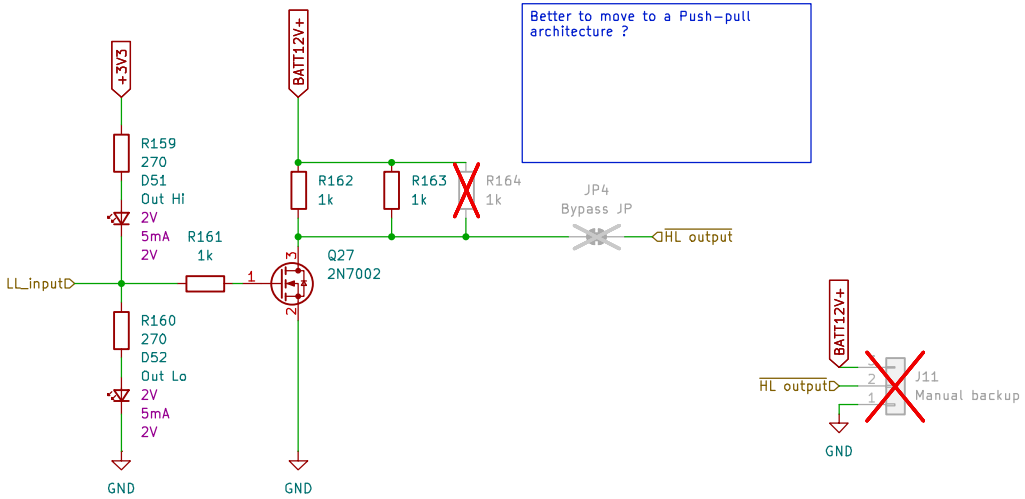
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter3/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 5/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



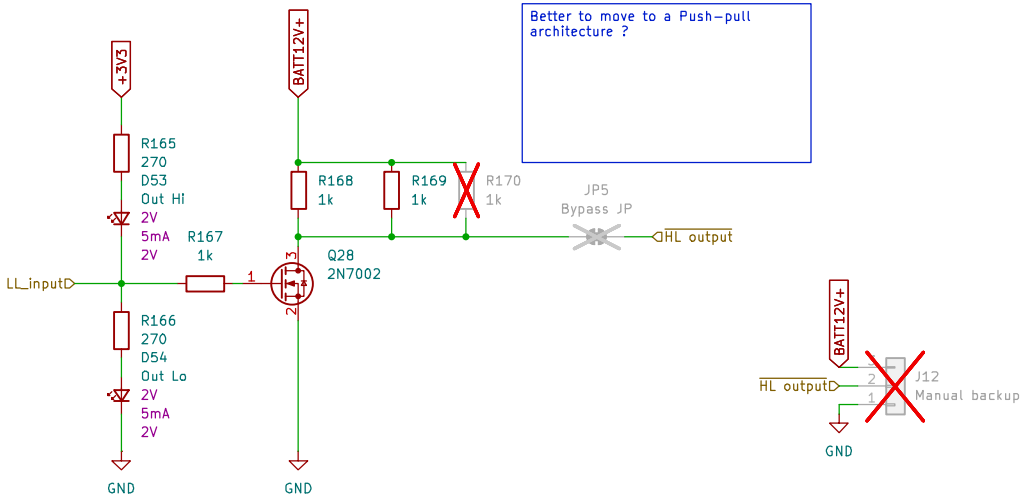
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter4/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 6/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



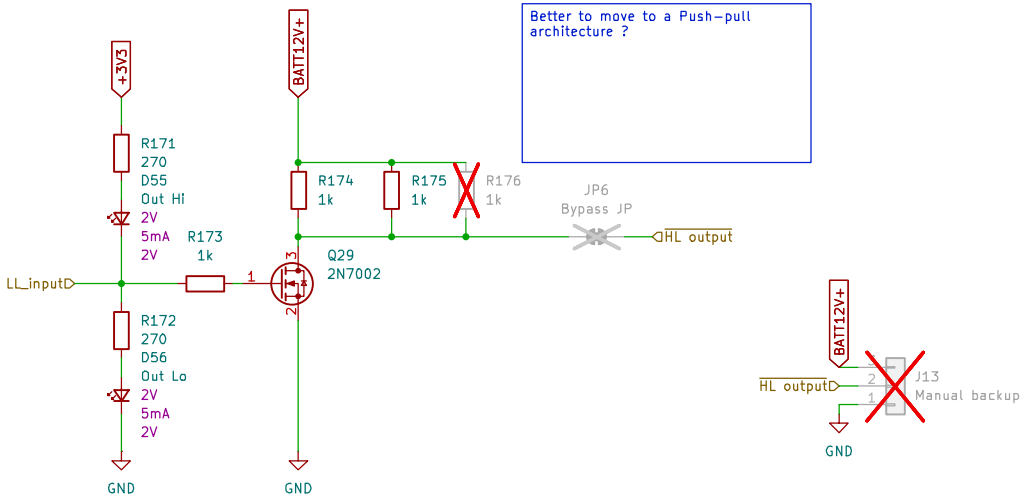
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter5/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 7/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



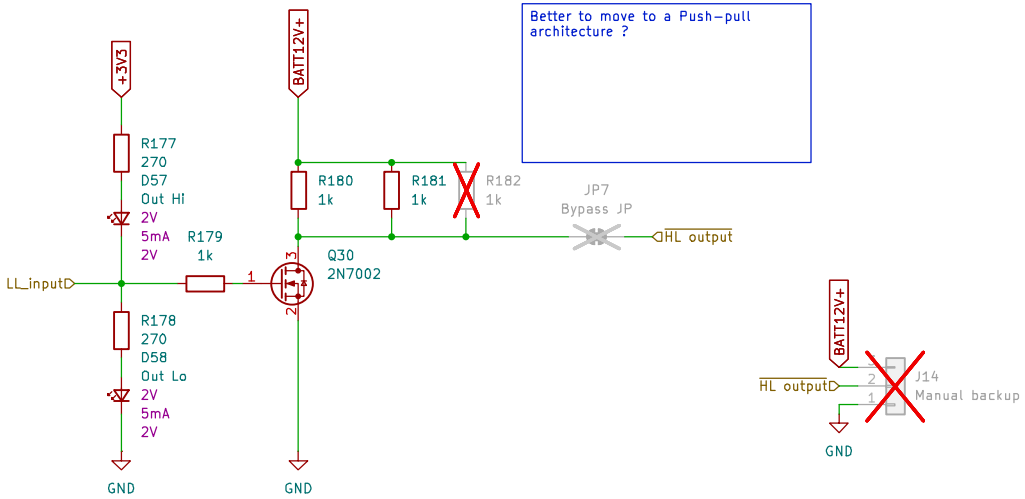
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter6/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 8/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



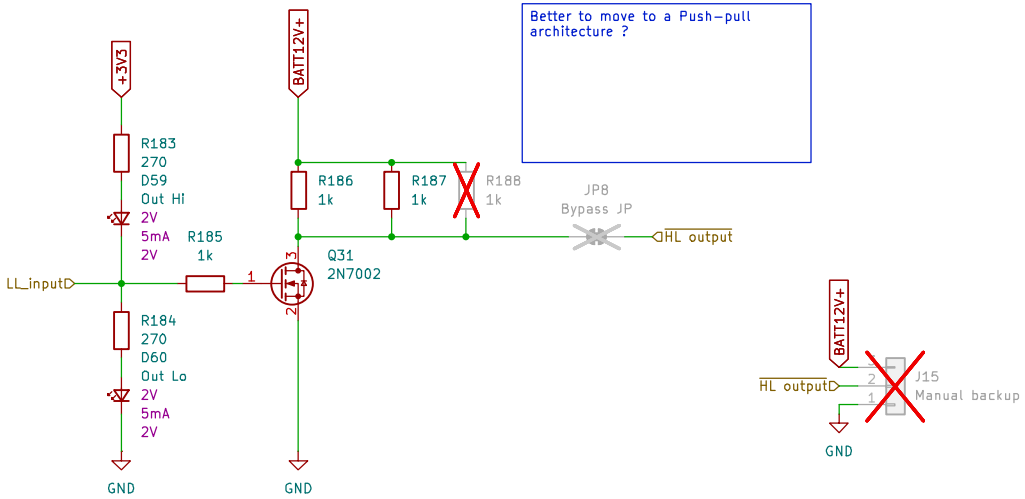
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter7/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 9/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



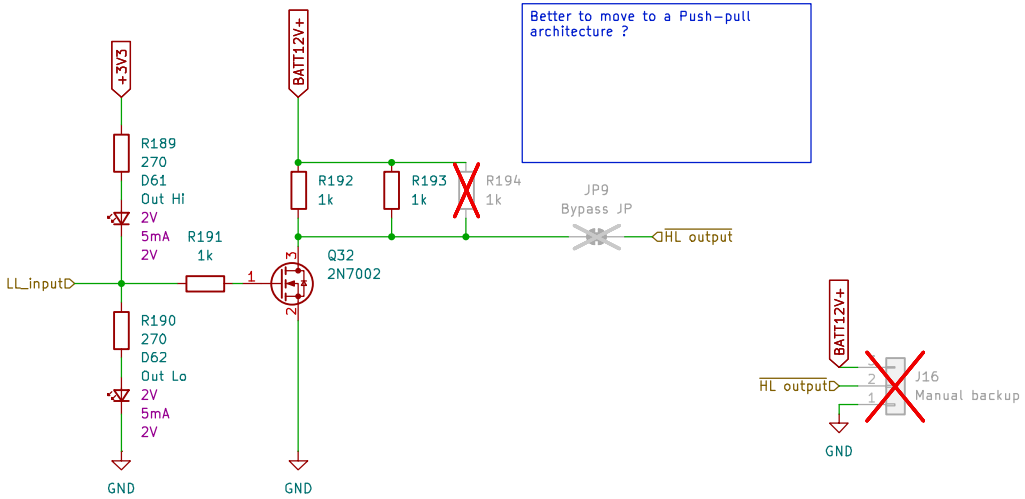
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter8/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 10/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



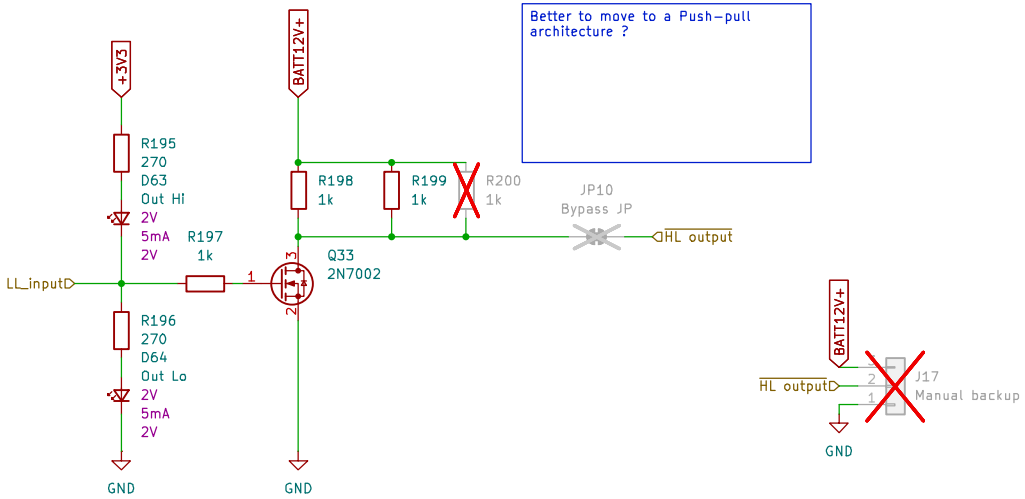
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter9/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 11/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



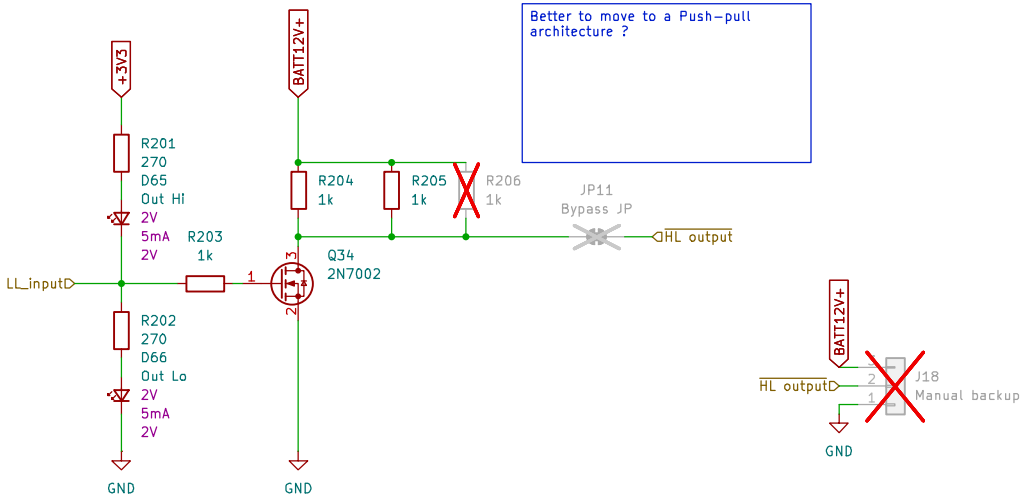
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter10/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 12/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



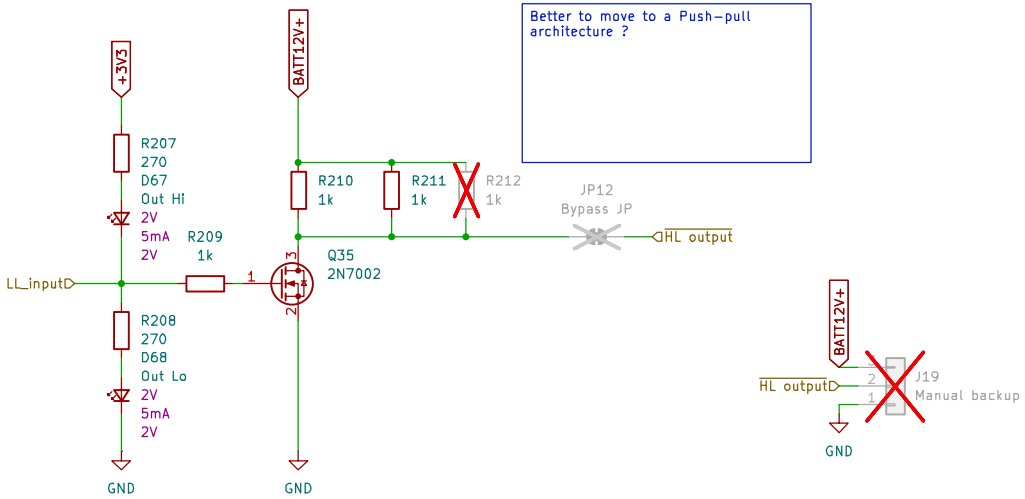
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter11/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 13/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



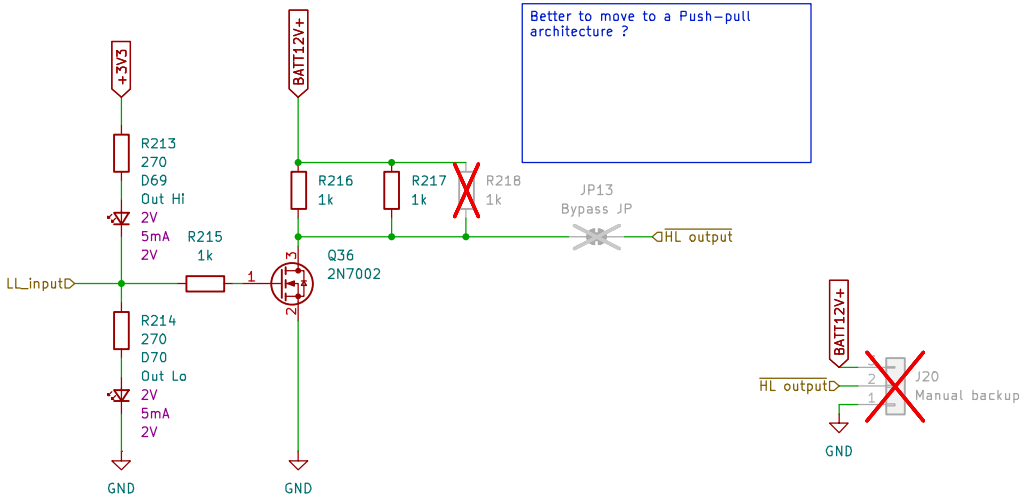
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter12/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 14/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



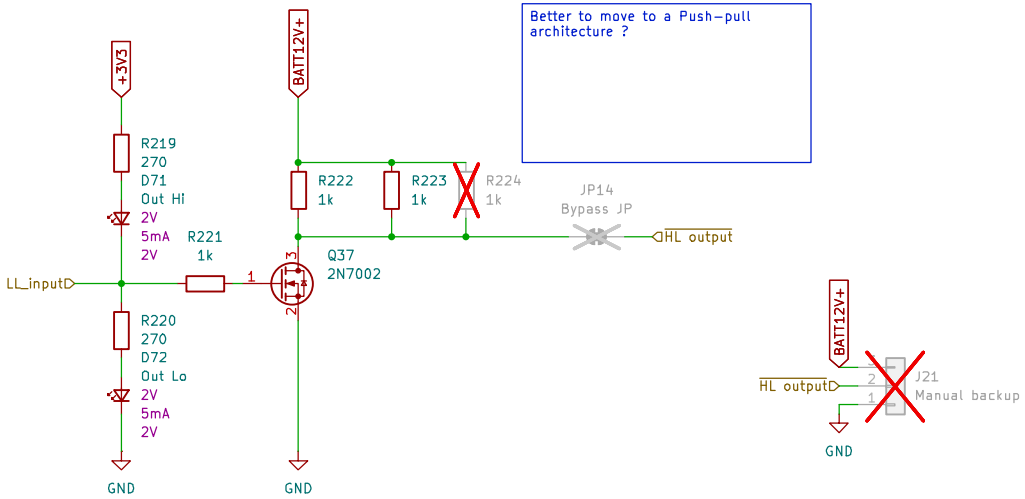
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter13/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 15/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



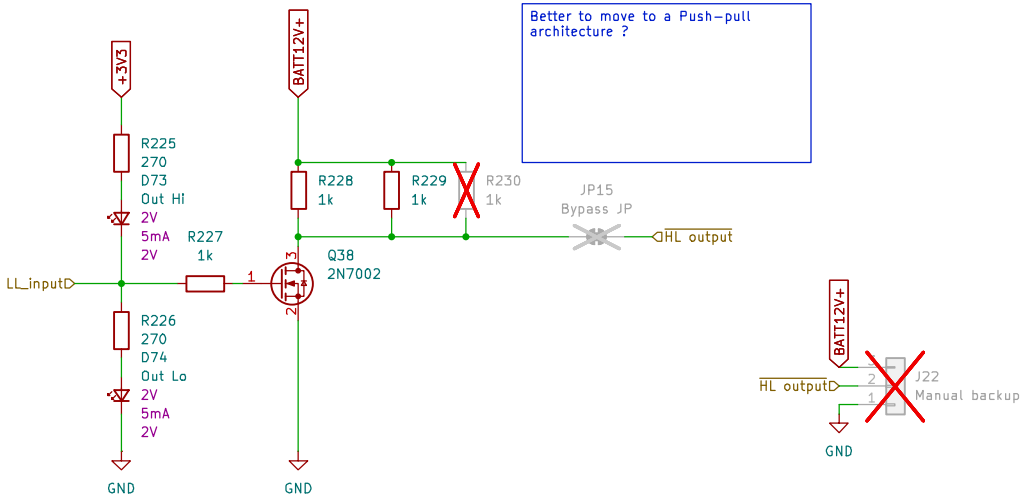
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter14/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 16/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level

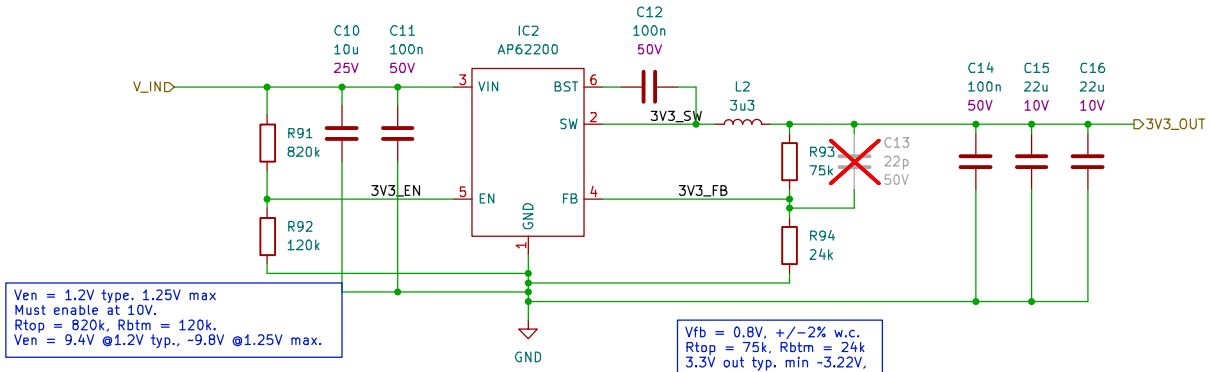


https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter15/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 17/36

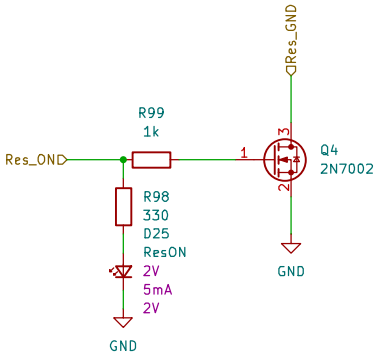


https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /3V3_SMPS/
File: 3V3_SMPS.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 1.4**
KiCad E.D.A. 9.0.0		Id: 18/36



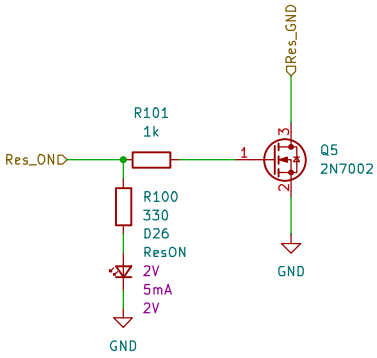
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 1/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 20/36



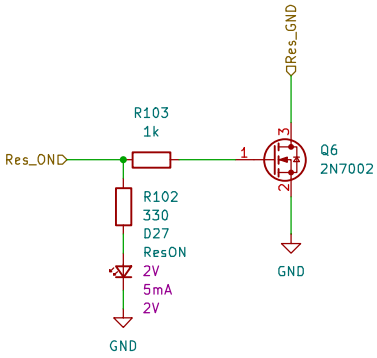
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 0/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 21/36



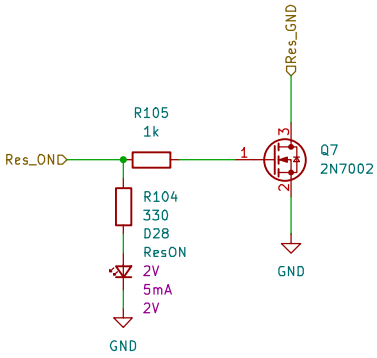
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 2/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 22/36



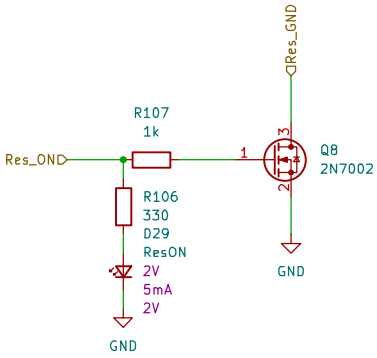
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 3/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 23/36



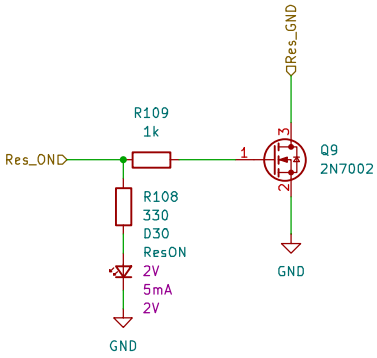
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 4/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 24/36



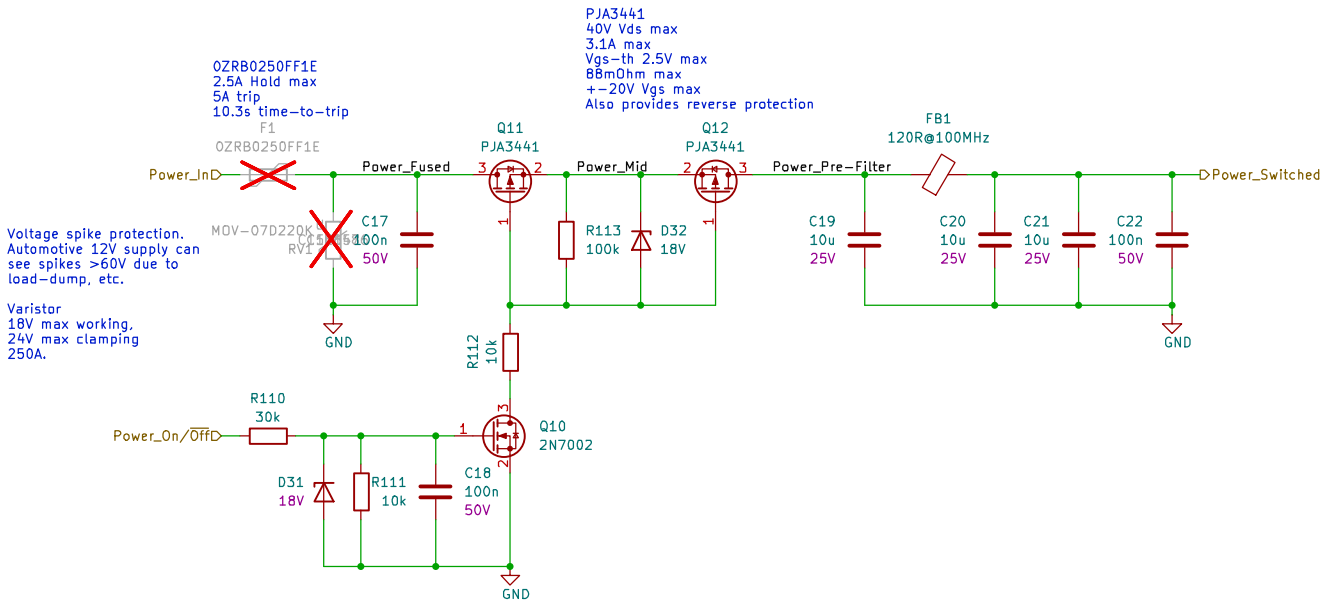
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 5/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 25/36

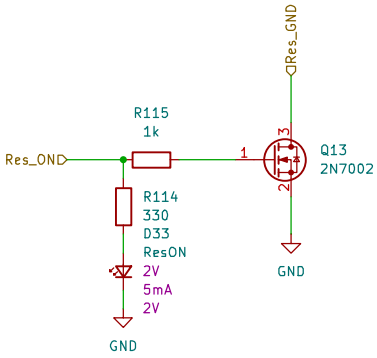


https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /POWER INPUT/
File: Power_Input.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 1.4**
KiCad E.D.A. 9.0.0		Id: 26/36



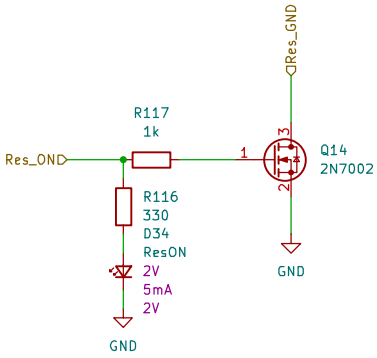
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 6/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 27/36



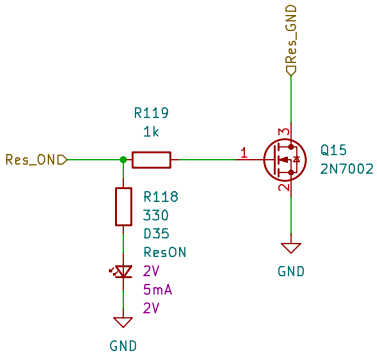
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 7/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 28/36



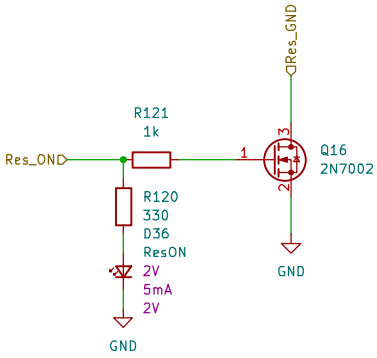
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 10/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 29/36



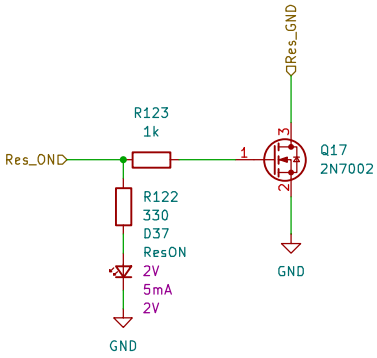
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor11/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 30/36



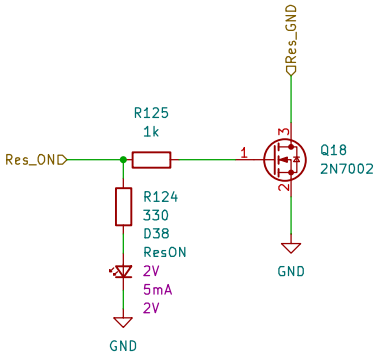
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 12/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 31/36



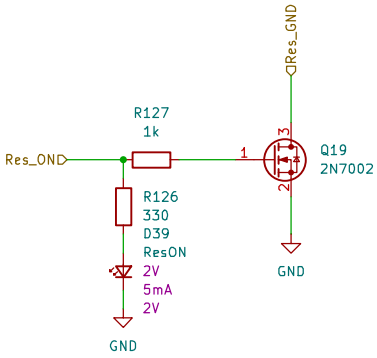
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 13/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 32/36



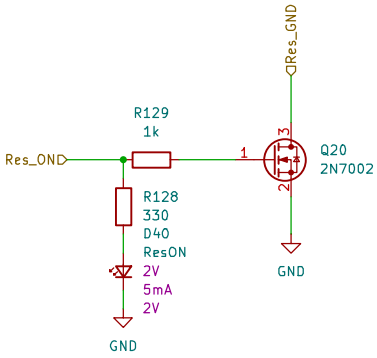
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 17/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 33/36



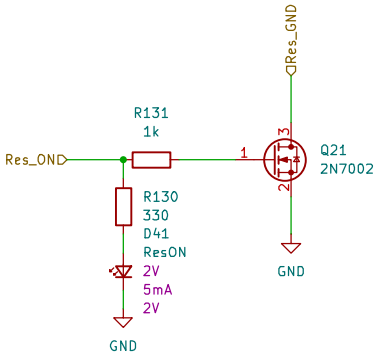
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 15/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 34/36



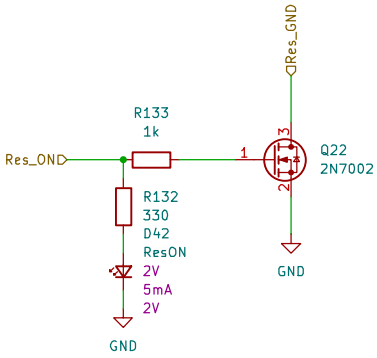
Approx 9mA consumption

https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 14/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 35/36



Approx 9mA consumption

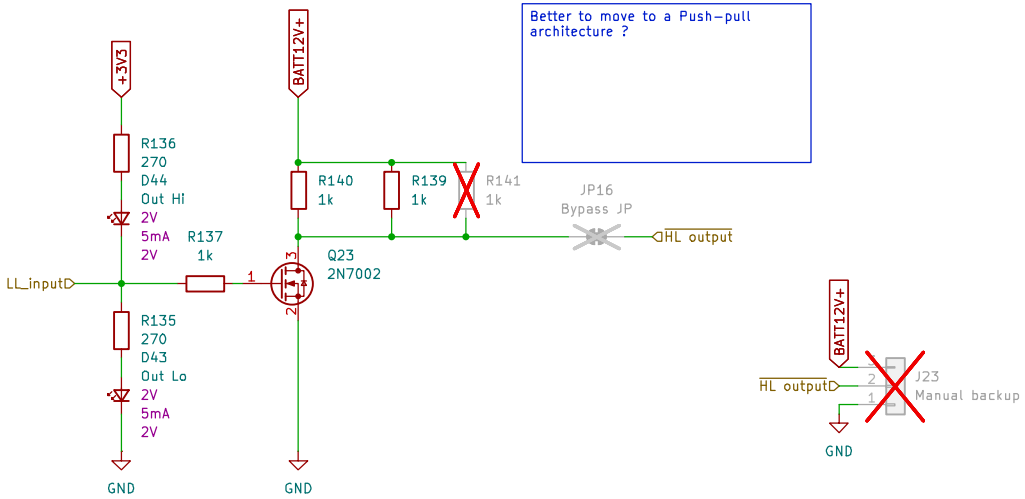
https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /Switchable Resistor 16/
File: Switchable_Res.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 36/36

Strategy is that these are all the same circuitry, active high/low logic is handled at software level



https://cadlab.io/projects/vxdash
https://github.com/martinroger/VXDash
Alex Miller & Martin Roger

Sheet: /NMOSFET Shifter/
File: FET_Active_Hi.kicad_sch

Title: Main architecture

Size: A4	Date: 2025-08-10	**Rev: 0.0**
KiCad E.D.A. 9.0.0		Id: 37/36