Design of digital integrated systems: optimisation of a 16 bit Brent-Kung adder

Your name here

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1 Schematic and optimisation

1.1 Optimisation

On this page you describe the optimisations you have used

- Architectural
  1. **Modification 1**
     - We changed the DotProduct (boolean optimization for NAND) VDD: 1 Worst Case delay = 836.5968 ps Worst Case Switching energy = 263.0274 fJ DC power consumption = 5.4792 nW
       * dit is een test
       * and like this
       * and like this
     - The main effects are
       * this
       * and this
  2. Sizing
- **Modification 2** we removed parts of the design where the propagate signal wasn't used any further. This saves gates.

  VDD: 1 Worst Case delay = 833.1871 ps Worst Case Switching energy = 260.9966 fJ DC power consumption = 5.1756 nW
- we increased the size of
  - this transistor
  - and this transistor
  - etc.

All in all you should have about two pages of explication (including the header).

2 Results

Please fill in table 1. Additional columns may be added, but provide at least one column with the data for the point with delay 650 ps.

2.1 Schematic

Figure 1: Schematic of the optimised adder

Delay	650 ps
Supply	x.xx V
Switching Energy	xxx fJ
DC power	x.xx nW

Table 1: Final performance of the circuit