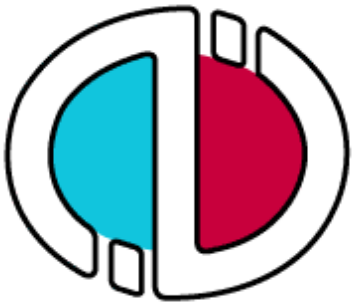

ANADOLU UNIVERSITY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EEM 334 – Digital Systems II

LAB 8 – FSM II

VENDING MACHINE

1. PURPOSE

In this lab, you will design and implement an FSM of a vending machine. The circuit that you will design will have the following characteristics. The block diagram of the circuit is given in Figure 1.

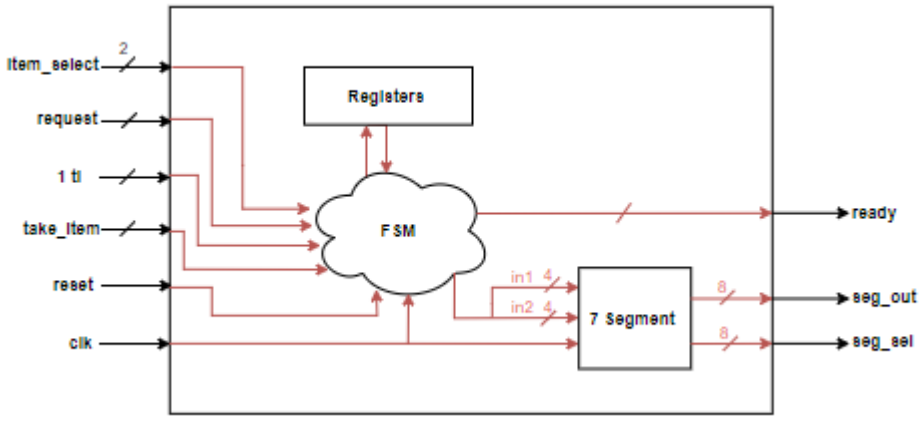

Figure 1: Block diagram of vending machine

The design will have **item_select**, **request**, **one_tl** (1 tl), **take_item** and asynchronous reset inputs in addition to the clock input. Only item_select is 2-bit, each of all other inputs is 1-bit. The switches will be used for item_select input. Other inputs will be controlled by the buttons. Your outputs will be connected to one of the LEDs and four 7-segment displays.

2. PROCEDURE

You will design a vending machine circuit according to the following specifications:

- An item is selected with two switches. Possible items and their costs are given in Table 1.

Table 1: List of items

Item	**Price (TL)**
Water	1
Chocolate	2
Coke	3
Cookies	4

- When an item is selected, it should be notified by the request button.
- The machine accepts only 1 TL. Depositing 1 TL is signaled by asserting one_tl input.
- After money is deposited, the machine waits for 1 second to calculate the total money.
- If the total money is enough to buy the corresponding item, one of the LEDs is turned on. Otherwise, the machine waits for the next 1 TL.
- The client can take the item, with the take_item button. When the item is taken, the LED is turned off.

You should show the current state on 7-segment display.

An asynchronous reset will put your circuit into a reset state, and clear all registers and outputs.

Steps:

1. Design your FSM.
2. Create top module and instantiate the seven segment inside it.
3. Code your FSM, make necessary connections between components and ports
4. Create a simulation to verify the functionality of the design.
5. Create .ucf file and assign the ports to pins.
6. Load the design on FPGA.
7. Verify your results and show them to your assistant.
8. Wait for a new task.

You can take advantage of the Xilinx example designs. You can access them by using language templates in edit menu of the ISE editor.