ADuC812 MicroConverter®
Parallel Programming Specification

Version 1.3
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This document details device configuration and timing specifications required to program the Flash/EE Memory of the ADuC812 MicroConverter in *parallel programming mode*. The ADuC812 datasheet includes other necessary product information not offered in this document. It can be found at http://www.analog.com/microconverter.

Note that *parallel programming mode* is only one of two methods to program the ADuC812. For details on the *in-circuit serial download mode*, refer to the ADuC812 datasheet and tech note uC004, both available at http://www.analog.com/microconverter.

Rise & Fall times on all timing diagrams in this document are specified as 10ns min / 100ns max.
All timing parameters are measured from the 50% level on a given signal.

CONTENTS:

Pin Configuration

The basic pin configuration for parallel programming is shown in Figure 1. The specific function of each pin and port is outlined below.

- **Port 0:** 8-bit bi-directional **DATA BUS** for programming and reading bytes
- **Ports 1 & 2:** 16-bit **ADDRESS BUS** input (Port 1 is the high-byte, Port 2 is the low-byte)
- **P3.1-P3.7:** 7-bit **COMMAND** input, for specifying erase, program, read, etc.
- **P3.0:** active-low **ENABLE COMMAND** input for strobing a command on P3.1-P3.7
- **ALE:** active-low **WRITE ENABLE** input, used in programming functions
- **$\overline{\text{EA}}$:** active-high **ENABLE HV** input, enables on-chip high-voltage charge-pump when high
- **XTAL1:** **STROBE CONFIG** input, used to latch the chip into parallel programming mode
- **$\overline{\text{PSEN}}$:** **MODE SELECT** input, used with XTAL1 to select parallel programming mode
- **RESET:** this pin must remain at the same potential as the VDD pins at all times

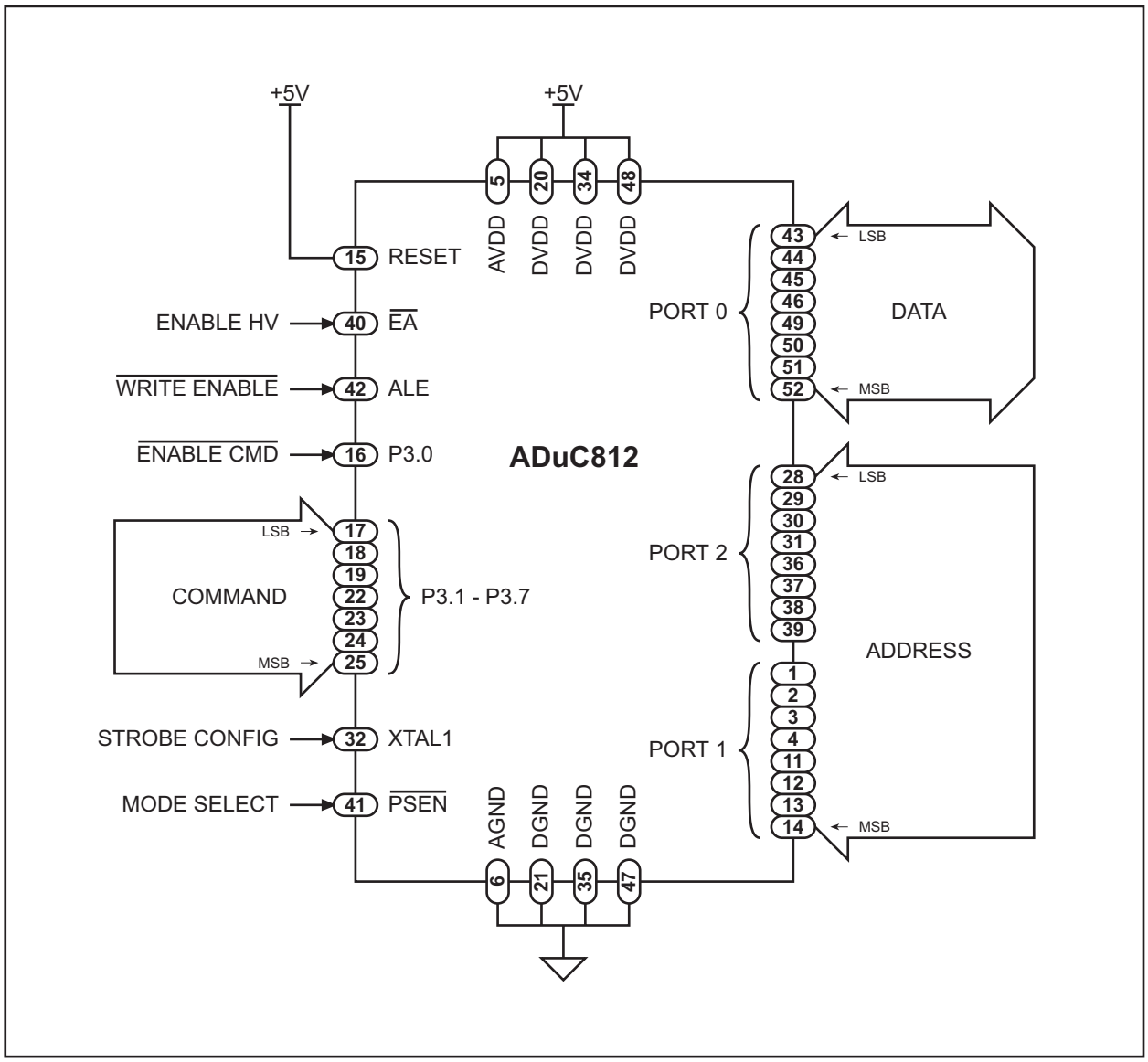

Figure 1: Pin Configuration for Parallel Programming

Power-Up & Power-Down Sequences

There are a number of requirements for correct application and removal of power for parallel programming mode. They are outlined in the below bullets and further details are illustrated in Figure 2.

- All four ground pins (DGND & AGND) must be treated as a single node.
- All four VDD pins (AVDD & DVDD) plus the RESET pin must all be treated as a single node.
- The voltage applied to any pin must never be greater than VDD or less than ground.
- Any time power is applied to the chip all signals must meet the requirements of Figure 2.
- During the "Command Sequences" section of Figure 2, the following reqirements must be met....
  - VDD and RESET must remain high.
  - $\overline{\text{PSEN}}$ must remain low.
  - XTAL1 must remain low.
  - ALE and P3.0 must remain high, except when pulsed low during specific command sequences.
  - $\overline{\text{EA}}$ must remain low, except when pulsed high during specific command sequences.

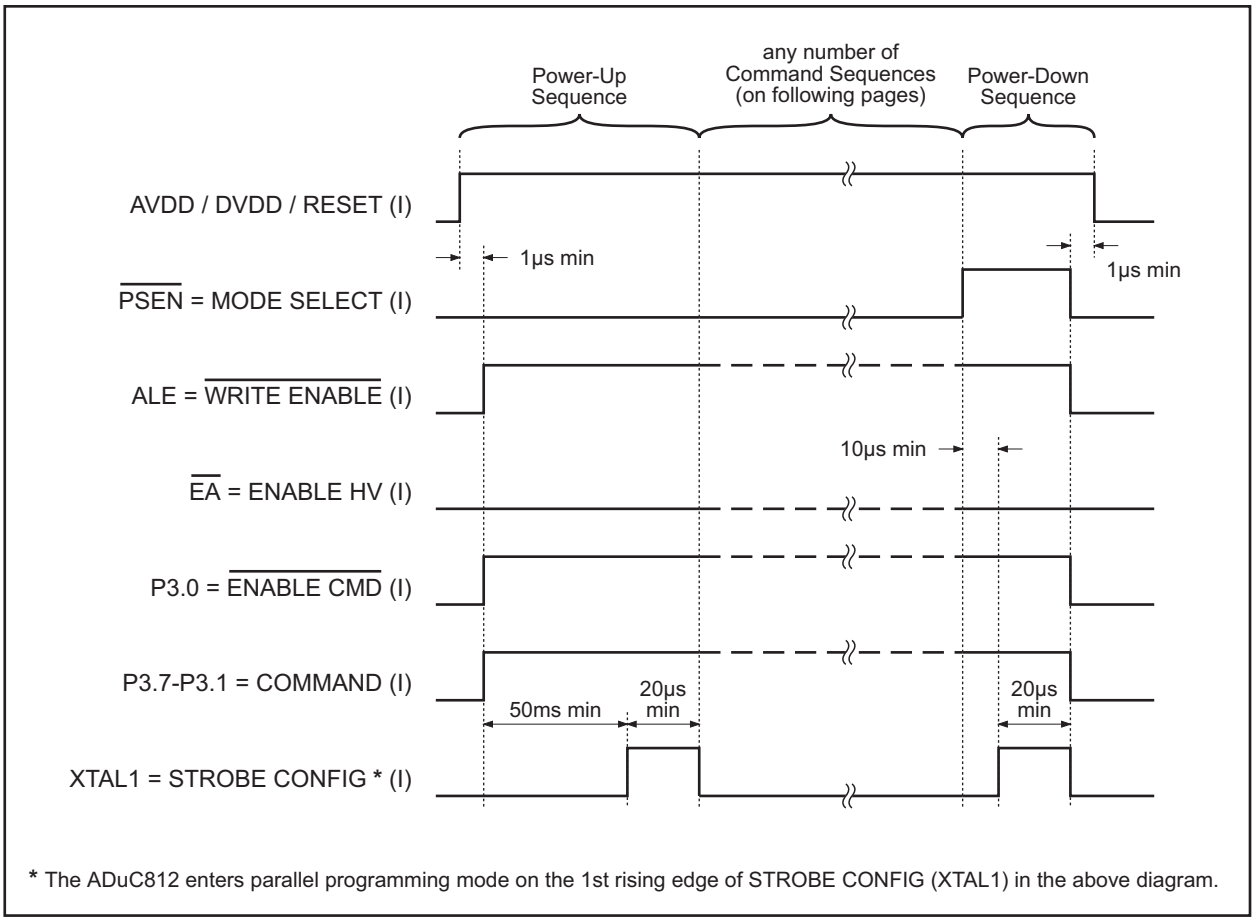

Figure 2: Power-Up & Power-Down Sequences for Parallel Programming

Memory Map

In parallel programming mode, the various areas of the ADuC812's internal Flash/EE memory are mapped into portions of the 64K byte addressable space as shown in Figure 3.

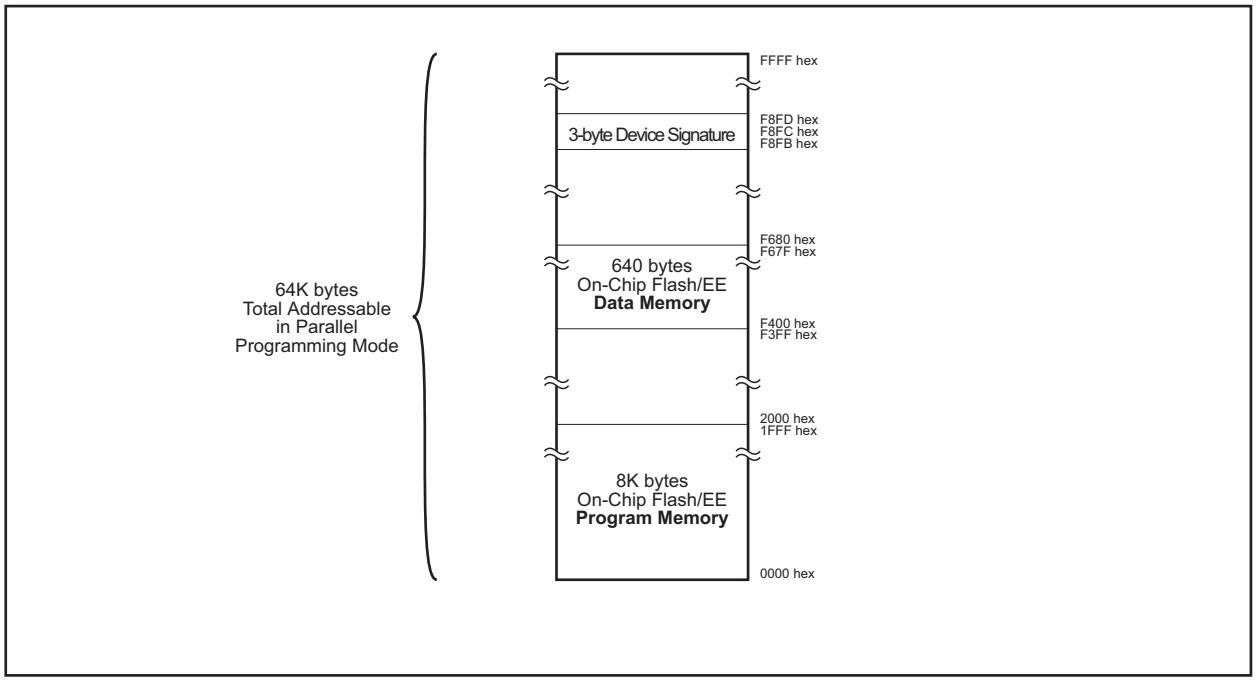

Figure 3: Parallel Programming Memory Map

Command Functions

The commands used to carry out various parallel programming functions are listed below.

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	Function	Page
1	1	1	1	1	1	1	default pullups – do nothing	–
1	1	1	1	0	0	0	**ERASE ALL** (code/data plus security bits)	7
1	1	1	1	0	0	1	**READ DEVICE SIGNATURE**	5
1	1	1	1	0	1	0	**PROGRAM BYTE**	8
1	1	1	1	0	1	1	**READ BYTE**	6
all others							reserved	–

Each of the above command functions is described in detail on the following pages.

Read Device Signature

Command Key:

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	Function
1	1	1	1	0	0	1	**READ DEVICE SIGNATURE**

You can read the device signature to ensure that the device inserted in the programmer is in fact an ADuC812. To do so, follow the timing shown in Figure 4, and read back addresses F8FB, F8FC, and F8FD hex. They should read back as the ASCII characters '8', '1', and '2' respectively, as shown in the below table. Using this command to read any addresses other than the three given below will return undefined results.

Device Signature Read-Back Values:

Address (hex)	Value (hex/dec/ASCII)
F8FB hex	38 hex / 56 dec / '8'
F8FC hex	31 hex / 49 dec / '1'
F8FD hex	32 hex / 50 dec / '2'

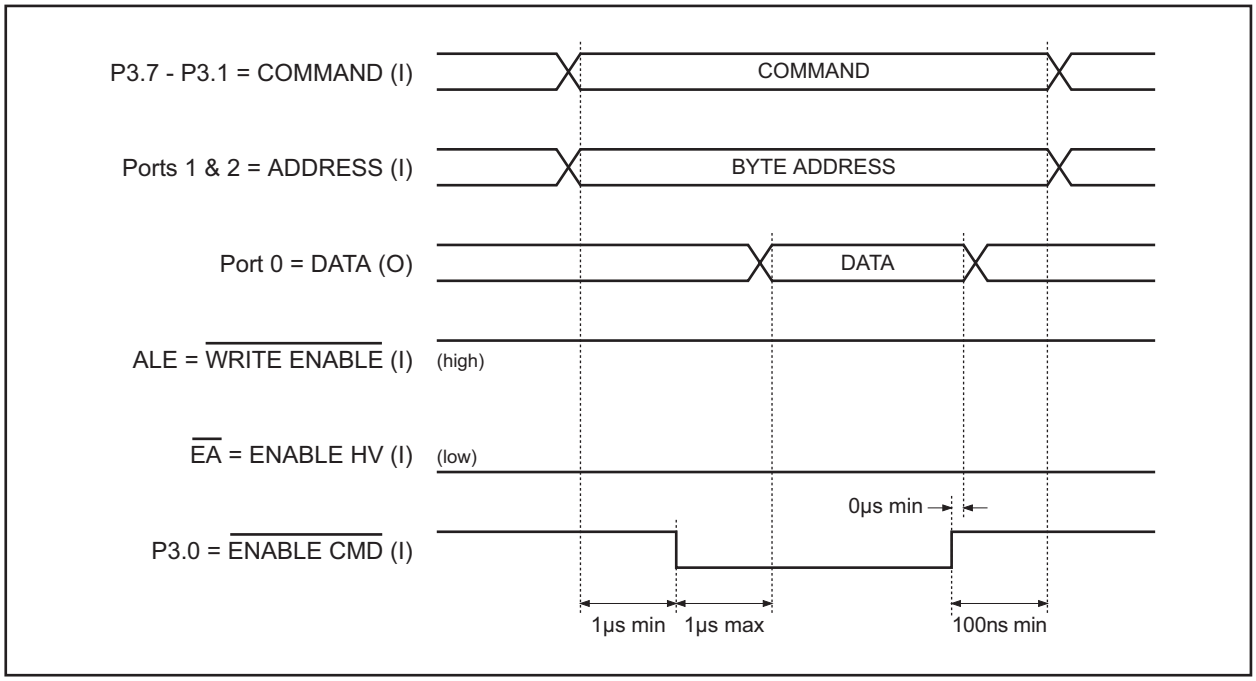

Figure 4: Read Device Signature Timing

Read Byte

Command Key:

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	Function
1	1	1	1	0	1	1	**READ BYTE**

To read data, one byte at a time, from the ADuC812, follow the timing shown in Figure 5.

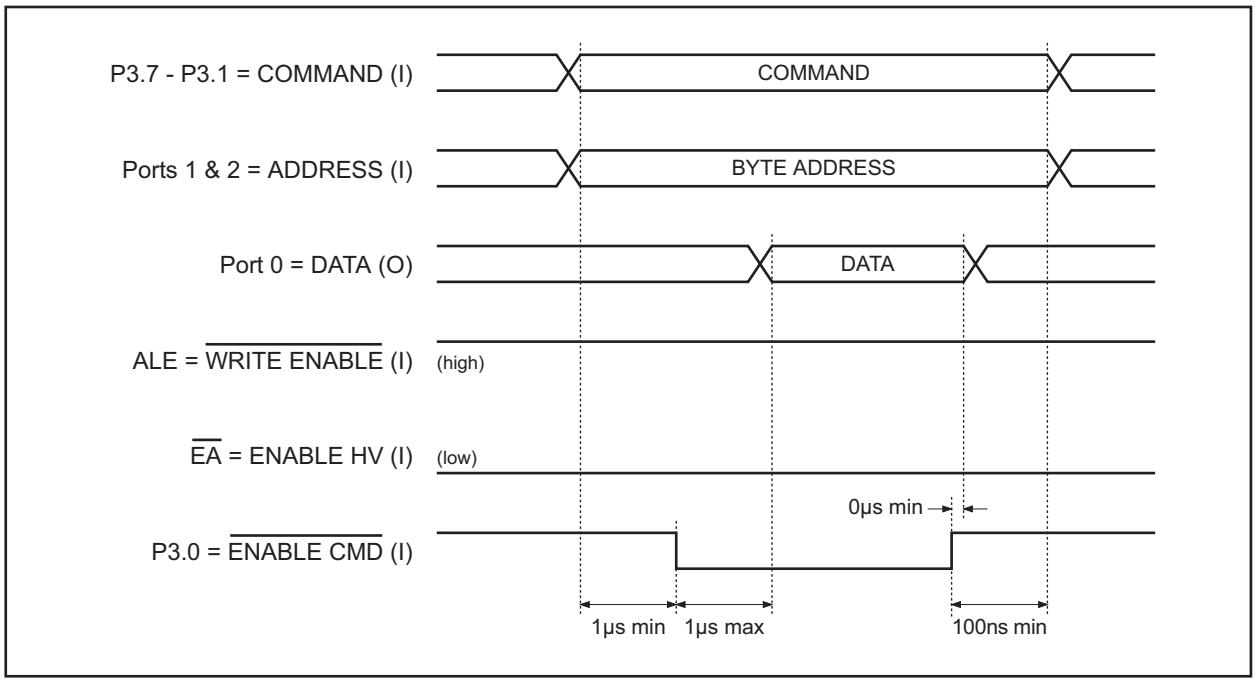

Figure 5: Read Byte Timing

Erase All

Command Key:

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	Function
1	1	1	1	0	0	0	**ERASE ALL** (code/data memory)

To erase the Flash/EE memory of the ADuC812, follow the timing given in Figure 6. This will erase the following areas....

- 8K byte Program Space
- 640 byte Data Space

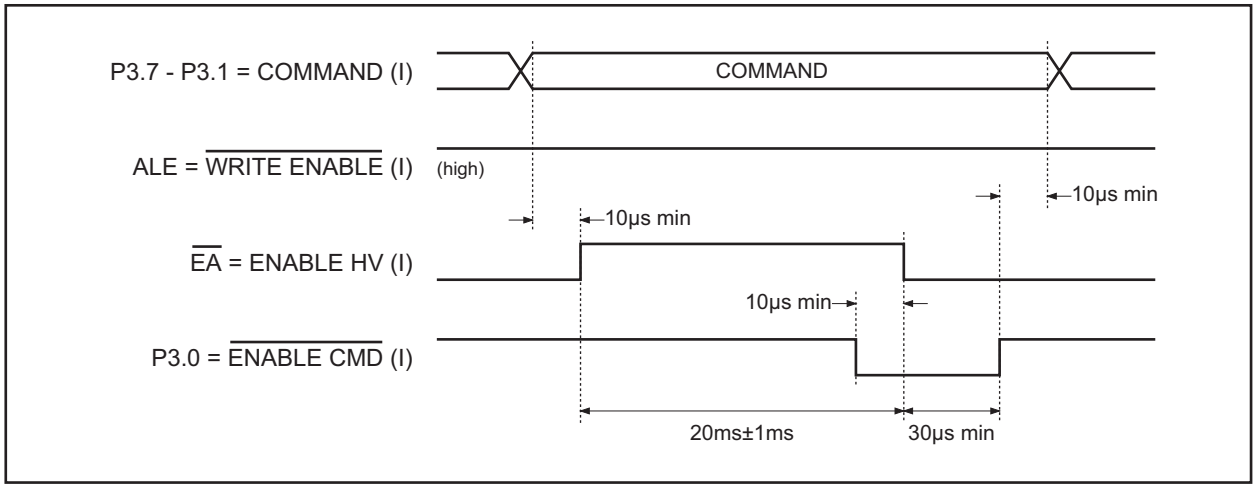

Figure 6: Erase All Timing

Program Byte

Command Key:

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	Function
1	1	1	1	0	1	0	**PROGRAM BYTE**

To program the ADuC812's program or data memory, one byte at a time, follow the timing shown in Figure 7.

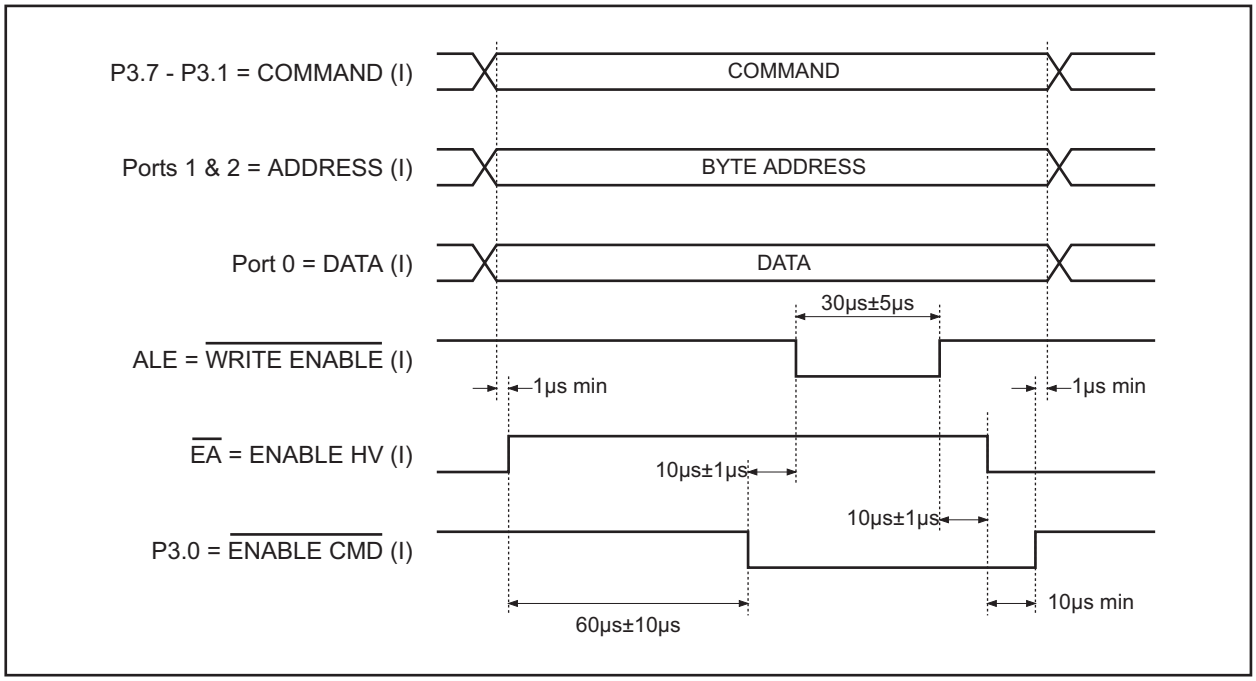

Figure 7: Program Byte Timing

Program Page

Command Key:

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	Function
1	1	1	1	0	1	0	**PROGRAM BYTE**

As an alternative to programming the ADuC812 a single byte at a time as in Figure 7, you can instead choose to utilise the page-programming function by following the timing shown in Figure 8. Note that the command byte is exactly the same as for a byte programming function, and in fact the page programming function is little more than a series of consecutive single bytes programmed in quick succession within strict timing constraints. If for any reason you cannot meet all the timing requirements of Figure 8, then use byte programming instead.

A page of program memory is 32 bytes in size, whereas a page of data memory is only 2 bytes in size*. For program memory, the first address of a page ends in the bits 00000, and the last address of a page ends in the bits 11111. For data memory, the first address of a page ends in a 0 bit, and the second (i.e. last) address in a page ends in a 1 bit. This is illustrated in the tables below. Page programming of the ADuC812 requires that all addresses in the page be programmed sequentially within a single sequence, starting with Address 0 and ending with Address 31 (or Address 1 for data memory).

One Page of Program Memory

Address 0	XXXXXXXXXX00000
Address 1	XXXXXXXXXX00001
Address 2	XXXXXXXXXX00010
...	...
Address 31	XXXXXXXXXX11111

One Page of Data Memory*

Address 0	XXXXXXXXXXXXXXX0
Address 1	XXXXXXXXXXXXXXX1

* In Parallel Programming Mode a page of Data Memory is 2 bytes, whereas in User Mode each page is 4 bytes.

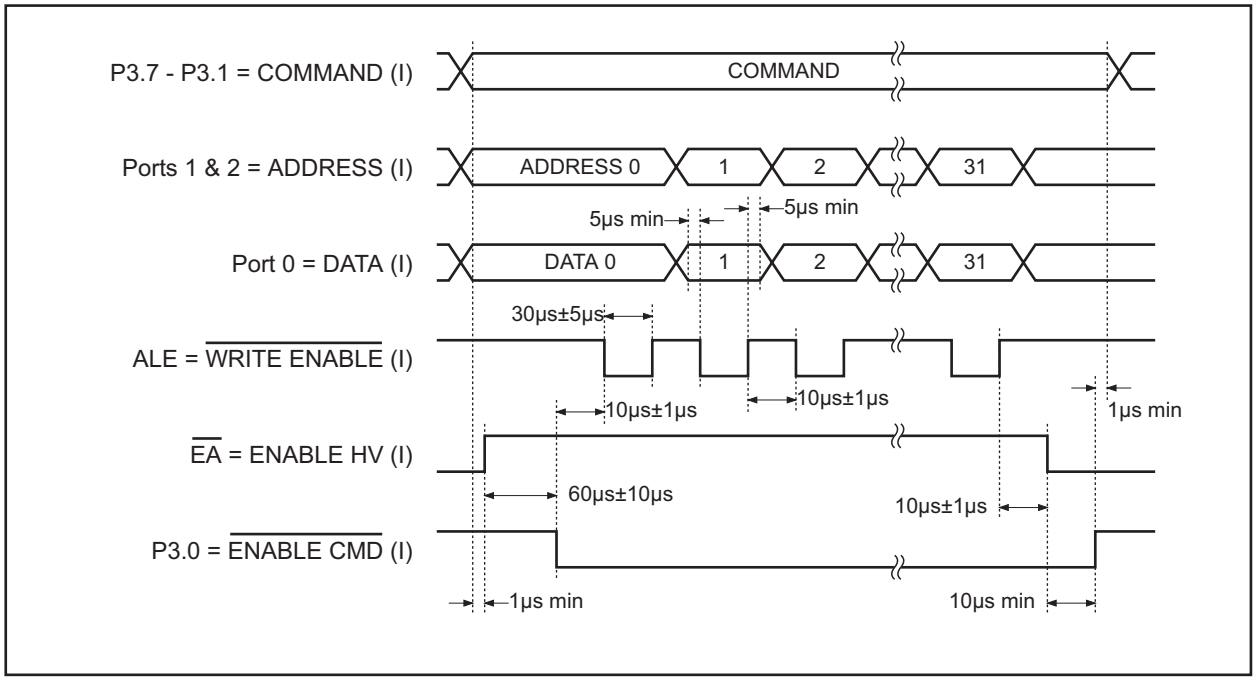

Figure 8: Program Page Timing