MicroConverter ® ADuC842 с 12—

FLASH- , 62

: 6 (
5
CLK=2.098),
15 (
3)

ADuC812/ADuC832

8052 (,
16MIPS) ,
12-
400

62 FLASH/ —
4 FLASH/

Flash/EE 100 ,
100 —
2304 ,
(RAM)

CSP
8 8
, -
52-
PQFP,
ADuC812/ADuC832

-
8- 12-
400 /
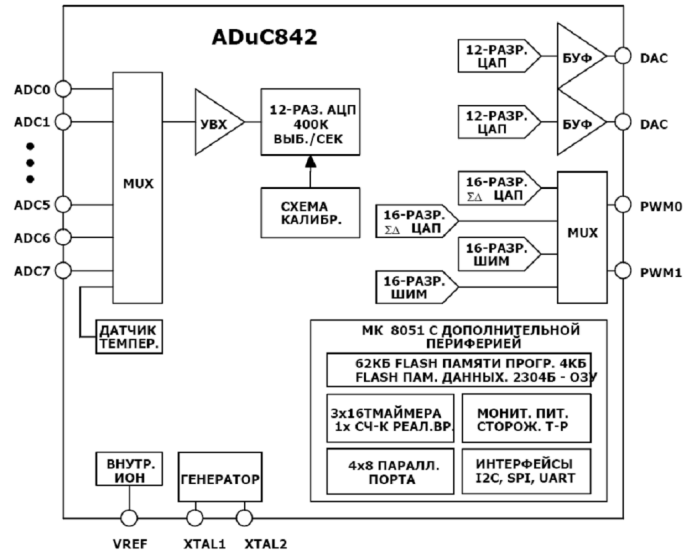20ppm/₀C
,
12- (—)

— 8051
8051 (
. 16.7)
,
(68%
)
32
12 2

, 11-

(TIC)
UART, I2C
SPI®
(WDT),
(PSM)

ADuC842

ADuC842

(16.77   )
8- -
(
8051).
32   ,   ,

— 16.77   .

,

8052,
16   MIPS.
62
Flash/EE   ,
4   Flash/EE
, 256
2
.

ADuC842
:   12-   ,

:   16-   ,   16-
-          ,   ,
,
/
(SPI I2C   UART).

(ADuC812,
ADuC832)   I2C   SPI

.
(I2C —
P3.3, P3.4,   SPI —   ).

UART,
—   .
ADuC842.

3   5
16.77   .

ADuC842

ADuC842

(AV$_{DD}$=DV$_{DD}$=2.7 — 3.3В   4.5 — 5.5 , REF=2.5В   , Fcore=16.77   ,
A =   ,   .)

	ADuC842 V$_{DD}$=			
	5В	3В		
:				
[2, 3]	12	12		Fsampl=120
	± 1	± 1	LSB .	. 2.5
	± 0.3	± 0.3	LSB	
	± 0.9	± 0.9	LSB .	. 2.5
	± 0.3	± 0.3	LSB	
[9]	± 3	± 1.5	LSB .	. 1
[9]	+1.5/-0.9	+1.5/-0.9	LSB .	. 1
	1	1	LSB	. -
[4, 5]	± 3	± 2	LSB .	
	± 1	± 1	LSB	
	± 3	± 2	LSB .	
	± 1	± 1	LSB	
- (SNR)[6]	71	71		Fin=10 . Fsampl=120
(THD)	-85	-85		
	-85	-85		
[7]	-80	-80		
	0 – Vref	0 – Vref		
	± 1	± 1	.	
	32	32	.	
(25 $_0$)[8]	700	700		
( )	-1.4	-1.4	/°	
	± 3	± 3	°	
				R$_L$=10 , C$_L$=100
[10]	12	12		
	± 3	± 3	LSB	
[11]	-1	-1	LSB .	12-
	± 1/2	± 1/2	LSB	
	± 50	± 50	. .	Vref
	± 1	± 1	% .	AVdd
	± 1	± 1	%	Vref
	0.5	0.5	%	% 1
0	0 – Vref	0 – Vref		= 2.5
1	0 – V$_{DD}$	0 – V$_{DD}$		= Vdd
	0.5	0.5		

3

	15	15		.
	10	10		0.5 LSB.
12, 13				
10	12	12		
	± 3	± 3	LSB	
11	-1	-1	LSB .	12-
	± 1/2	± 1/2	LSB	
	± 10	± 10	.	Vref
	± 1	± 1	%	Vref
	0.5	0.5	%	% 1
0	0 – Vref	0 – Vref		=2.5
/				
14	2.5	2.5		
	± 10	± 10	.	Vref ref
	65	67		
	± 15	± 15	ppm/°C	
	2	2		
15				
(Vref)[9]	1	1	.	
	Vdd	Vdd	.	
	20	20		
	1	1	.	
				ADCCON1.6
(PSM)				
AV_DD		2.93		4-
		3.08		
				1-0 PSMCON
DV_DD		± 2.5	%	
(WDT)[9]				
-	0	0	.	
	2000	2000	.	8
(FLASH/)[16]				
17	100000	100000		
18	100	100		
. . (V_INH)	2.4			
. . (V_INL)	0.8			
(0, 1,)	± 10			Vin=0 V_DD
	± 1	± 1		Vin=0 V_DD
.1 ( )	± 10			Vin=V_DD
	± 1	± 1		Vin=V_DD
.0 (2, 3)	-75	-25		V_IL=0
	-40	-15		V_IL=2
. 1-0 (2, 3)	-660	-250		V_IL=2
	-400	-140		
XTAL1				
, V_INL	0.8	0.4		
V_INH	3.5	2.5		
XTAL1	18	18		
XTAL2	18	18		
	16.78	8.38		
(V_OH)	2.4	2.4	.	V_DD=4.5 — 5.5 , Isrc=80
	4.0	2.6		V_DD=2.7 — 3.3 , Isrc=20

(V$_{OL}$)	0.4	0.4	.	Isink=1.6
ALE, 0, 2	0.2	0.2	.	Isink=1.6
3	0.4	0.4	.	Isink=4
SCLOCK/SDATA	0.4	0.4	.	Isink=8
« »	± 10	± 10	.	
«	± 1	± 1		
»	10	10		
	500	500		
	100	100		
:				
INT0	150	400		
SPI/I2C	150	400		
RESET	150	400		
	3	3		
WDT	3	3		WDCON SFR
[19, 20]				
AVdd/DVdd — AGND		2.7	.	AVdd/DVdd = 3 .
		3.3	.	
	4.5		.	AVdd/DVdd = 5 .
	5.5		.	
Dvdd [9]	10	4.5	.	CLK = 2.1
vdd [9]	1.7	1.7		CLK = 2.1
Dvdd	38	12		CLK = 16.8/8.4 5 /3
	33	10		CLK = 16.8/8.4 5 /3
AVdd	1.7	1.7		CLK = 16.8/8.4 5 /3
Dvdd [9]	4.5	2.2		CLK = 2.1
vdd [9]	3	2		CLK = 2.1
Dvdd [9]	12	5	.	CLK = 16.8/8.4 5 /3
	10	3.5		CLK = 16.8/8.4 5 /3
AVdd [9]	3	2		CLK = 16.8/8.4 5 /3
Dvdd	28	18	.	
	20	10		
Avdd	2	1		
Dvdd	50	22	.	
	40	15		
PSM	15	10		Avdd = Dvdd
	1.0	1.0	.	MCLK = 32
	2.8	1.8	.	MCLK = 2
	150	130		

ADuC842

:

1   -40   +85°C.

2   .

3   , LSB (   ) = Vref/2, 1LSB = 610   .   Vref=1 , 1LSB = 244   .

4   ,
                         .

5   ,   ,
                              .

6   (SNR)   .

7   .

8   ,
                         .

9   ,
         .

10   :
                              48   4095,   0   Vref
                              48   3995,   0   V_{DD}
         =10   100 .

11   :   0   Vref   0   Vdd.

12   .

13   I_{SINK},
     ,   ,   .

14   0.1   Vref   Cref.
                                                                      .

15   ADCCON1.6.
Vref   Cref   .

16   Flash/EE   Flash/EE   Flash/EE
         .

17   100 ,   JEDEC Std.   117
                -40° , +25°   +85° .   +25°   700 .

18   (Tj)=55°   JEDEC   117.
                                  ,   FLASH   0.6
                              ,   .27.

19   ,   :
                    : RESET=0.4 ,   / =   .   CD
     PLLCON.   .
                    : RESET=0.4 ,   / =   .   CD
     PLLCON PLLCON.0=1.   .
                    : RESET=   0=0.4 ,   .
          CD   PLLCON PLLCON.0=1.   . OSC   /   OSC_PD
     (PLLCON.7)   PLLCON SFR.

20   FLASH   ,   Dvdd,
                    3   (3)   10   (5).

(=25°C,   )

AV_{DD} AGND	-0.3 .. +7
DV_{DD} AGND	-0.3 .. +7
DV_{DD} DGND	-0.3 .. +7
AGND DGND	-0.3 .. +0.3
AV_{DD} DVDD	-0.3 .. +0.3
. AGND	-0.3 .. AVDD+0.3
AGND	-0.3 .. AVDD+0.3
DGND	-0.3 .. DVDD+0.3
DGND	-0.3 .. DVDD+0.3
	-40° .. +85°
	-65° .. +150°
	+150°
	90°C/
(60)	+215°
(15)	+220°

* —   .
                                                                                        .

!
                                                              (ESD).   4000 ,
                         ,   .

,   ADuC842   ,
                         .

ADuC842

DVDD	P	+3 +5 .
AVDD	P	+3 +5 .
Cref	I	. AGND 0.1 .
Vref	I/O	/ . . 2.5 . .
AGND	G	. .
P1.0-P1.7	I	1 (8) . 1 , 0 . 1 - .
ADC0-ADC7	I	. 8 . (SFR) ADCCON2.
T2	I	/ 2. 2 1-0 2.
T2EX	I	. / 2, 2.
SS	I	(Slave Select). (SPI).
SDATA	I/O	/ I2C SPI.
SCLOCK	I/O	I2C SPI.
MOSI	I/O	SPI / .
MISO	I/O	SPI / .
DAC0	O	0.
DAC1	O	1.
RESET	I	. 24 .
P3.0-P3.7	I/O	3 , . 3, 1 . , , 3 - .
PWMC	I	.
PWM0		PWM0. 2.6 2.7 3.3 3.4.
PWM1		PWM1. CFG 842.
RxD	I/O	(UART) / .
TxD	O	(UART)
INT0	I	. 0, / ; 2- . 0.
INT1	I	1, / ; 2- . 1.
T0	I	/ 0.
T1	I	/ 1.
CONVST	I	( ) . 0-1 .
WR	O	. 0 .
RD	O	. 0.
XTAL2	O	.
XTAL1	I	.
DGND	G	. .

ADuC842

P2.0-P2.7 (A8-A15) (A16-A23)	I/O	2 , . 2, 1 . . , , 2 , 24- .
PSEN/	O	. . 6 , .1 . . , RESET.
ALE	O	. (24- -)
EA	I	. =1, 0000 .. 1FFFH, =0, .
P0.0-P0.7 (A0-A7)	I/O	« ». 0 . 1 . 0 . . 1, .

:

$$SNR=(6.02N + 1.76) \ (\quad),$$

N-   .
,   12   SNR=74   .

,

.

:   ,   0.5LSB
,   —   0.5LSB
.   .

1   (1 LSB)   .

(000)   (001)
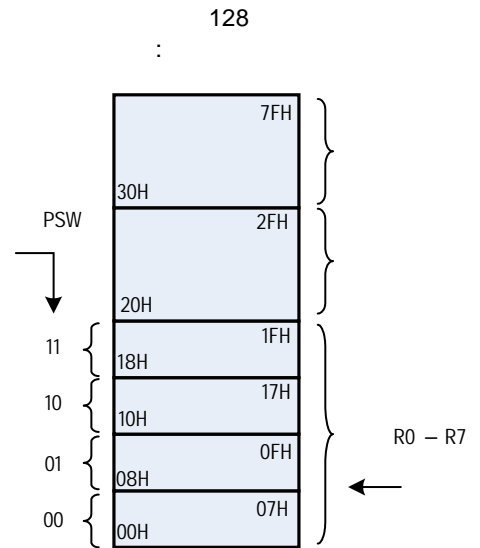. . +0.5LSB.   ,
.   .

,
(— 1.5LSB)   ,
.

/(+   )   .
(+
)   .   —   —

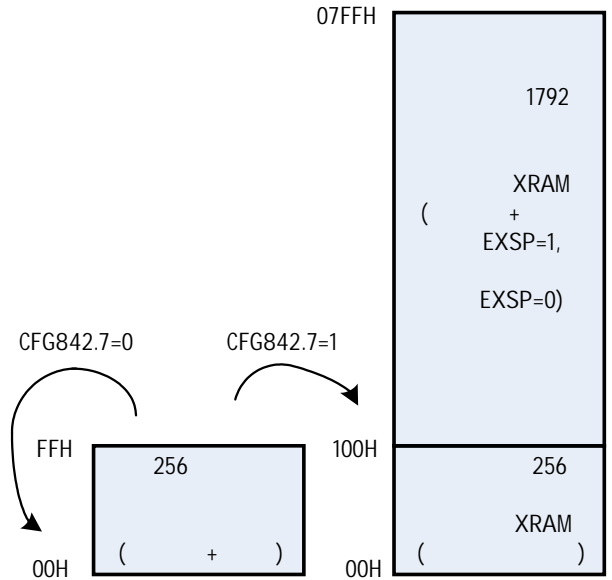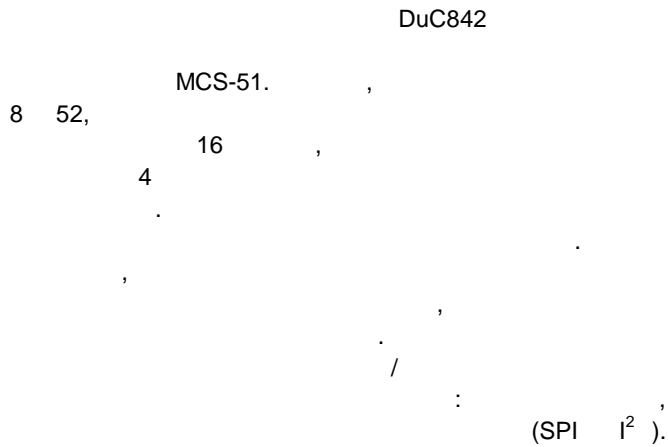Fs/2 — (   ),   .
.   (   ).

.   .   ,
.

Top pins (left to right, pins 52–40):

- 52 P0.7/AD7
- 51 P0.6/AD6
- 50 P0.5/AD5
- 49 P0.4/AD4
- 48 DVdd
- 47 DGND
- 46 P0.3/AD3
- 45 P0.2/AD2
- 44 P0.1/AD1
- 43 P0.0/AD0
- 42 ALE
- 41 PSEN
- 40 EA

Left pins (top to bottom, pins 1–13):

- 1 P1.0/ADC0/T2
- 2 P1.1/ADC1/T2EX
- 3 P1.2/ADC2
- 4 P1.3/ADC3
- 5 AVdd
- 6 AGND
- 7 Cref
- 8 Vref
- 9 DAC0
- 10 DAC1
- 11 P1.4/ADC4
- 12 P1.5/ADC5/SS
- 13 P1.6/ADC6

Center label:

ADuC842

ВИД СВЕРХУ

(Не в масштабе)

1 (ключ)

Right pins (top to bottom, pins 39–27):

- 39 P2.7/PWM1/A15/A23
- 38 P2.6/PWM0/A14/A22
- 37 P2.5/A13/A21
- 36 P2.4/A12/A20
- 35 DGND
- 34 DVdd
- 33 XTAL2
- 32 XTAL1
- 31 P2.3/A11/A19
- 30 P2.2/A10/A18
- 29 P2.1/A9/A17
- 28 P2.0/A8/A16
- 27 SDATA/MOSI

Bottom pins (left to right, pins 14–26):

- 14 P1.7/ADC7
- 15 RESET
- 16 R3.0/RxD
- 17 P3.1/TxD
- 18 P3.2/INT0
- 19 P3.3/INT1/MISO/PWM1
- 20 DVdd
- 21 DGND
- 22 P3.4/T0/PWMC/PWM0/EXTCLCK
- 23 P3.5/T1/CONVST
- 24 P3.6/WR
- 25 P3.7/RD
- 26 SCLOCK

-

- ADuC842 (, , ADuC812).

ADD A, Rn	1	1
ADD A, @Ri	1	2
ADDC A, Rn	1	1
ADDC A, @Ri	1	2
ADD A, dir	2	2
ADDC A, #data	2	2
SUBB A, Rn	1	1
SUBB A, @Ri	1	2
SUBB A, dir	2	2
SUBB A, #data	1	1
INC A	1	1
INC Rn	1	1
INC @Ri	1	2
INC dir	2	2
INC DPTR	1	3
DEC A	1	1
DEC Rn	1	1
DEC @Ri	1	2
DEC dir	2	2
MUL AB	1	9
DIV AB	1	9
DA A	1	2
ANL A,Rn	1	1
ANL A,@Ri	1	2
ANL A,dir	2	2
ANL A,#data	2	2
ANL dir,A	2	2
ANL dir,#data	3	3
ORL A,Rn	1	1
ORL A,@Ri	1	2
ORL A,dir	2	2
ORL A,#data	2	2
ORL dir,A	2	2
ORL dir,#data	3	3
XRL A,Rn	1	1
XRL A,@Ri	2	2
XRL A,dir	2	2
XRL A,#data	2	2
XRL dir,A	2	2
XRL dir,#data	3	3
CLR A	1	1
CPL A	1	1
SWAP A	1	1
RL A	1	1
RLC A	1	1
RR A	1	1
RRC A	1	1
MOV A,Rn	1	1
MOV A,@Ri	1	2
MOV Rn,A	1	1
MOV @Ri,A	1	2
MOV A,dir	2	2
MOV A,#data	2	2
MOV Rn,#data	2	2
MOV dir,A	2	2

ADuC842

MOV @Ri,#data		2	2
MOV dir,dir		3	3
MOV dir,#data		3	3
MOV DPTR,#data		3	3
MOVC A,@A+DPTR	DPTR	1	4
MOVC A,@A+PC	P	1	4
MOVX A,@Ri	(8)	1	4
MOVX A,@DPTR	(16)	1	4
MOVX @Ri,A	(8)	1	4
MOVX @DPTR,A	(16)	1	4
PUSH dir		2	2
POP dir		2	2
XCH A,Rn		1	1
XCH A,@Ri		1	2
XCHD A,@Ri		1	2
XCH A,dir		2	2
CLR C		1	1
CLR bit	bit	2	2
SETB C		1	1
SETB bit	bit	2	2
CPL C		1	1
CPL bit	bit	2	2
ANL C,bit	bit	2	2
ANL C,/bit	bit-	2	2
ORL C,bit	bit	2	2
ORL C,/bit	bit-	2	2
MOV C,bit	bit	2	2
MOV bit,C	bit	2	2
JUMP @A,DPTR	DPTR	1	3
RET		1	4
RETI		1	4
ACALL addr11l		2	3
AJMP addr11		2	3
SJMP rel	( )	2	3
JC rel	, =1	2	3
JNC rel	, =0	2	3
JZ rel	, =0	2	3
JNZ rel	, #0	2	3
DJNZ Rn,rel	, #0	2	3
LJMP		3	4
LCALL addr16		3	4
JB bit,rel	, bit=1	3	4
JNB bit,rel	, bit=0	3	4
JBC bit,rel	, bit=1	3	4
CJNE A,dir,rel	JNE	3	4
CJNE A,#data,rel	JNE	3	4
CJNE Rn,#data,rel	JNE	3	4
CJNE @Ri,#data,rel	JNE	3	4
DJNZ dir,rel	JNZ	3	4
NOP		1	1

:

1. .
2. MOV X 4 , 0. MOVX 4+n ,
   n .
3. LCALL 3 , LCALL .

13

DuC842

MCS-51. ,

8 52,

16 ,

4

.

.

,

,

. /

:

(SPI I^2).

,

.

.

62	4
	8- 12-
8051	128-
	: - -2 12 - -WDT -PSM -TIC -PWM
2304	

:
- 62 flash- ;
- 4 flash- ;
- 256 ;
- 2 XRAM .

CFG842,

:

07FFH

1792 XRAM (+ EXSP=1, EXSP=0)

CFG842.7=0   CFG842.7=1

FFH | 256 | 100H | 256
XRAM
( ) |
00H | (+) | 00H

128

:

7FH
30H
2FH
20H

PSW

11 { 18H | 1FH |
10 { 10H | 17H |
01 { 08H | 0FH |
00 { 00H | 07H |

R0 — R7

7FH.

: 32

,

RO —

R7.

RSO,

RS1 PSW. , 32

, ,

20H—2FH ,

—7FH.

. .

ADuC842

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 1	SPR1 F9H 0	SPR0 F8H 0	BITS
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS
I2CSI/MDO EFH 0	I2CGC/MDE EEH 0	I2C1O1MCO EDH 0	I2C1O0/MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS
ADCI DFH 0	DMA DEH 0	CCONV DDH 0	SCONV DCH 0	CS3 DBH 0	CS2 DAH 0	CS1 D9H 0	CS0 D8H 0	BITS
CY D7H 0	AC D6H 0	F0 D5H 0	RS1 D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 1	WDIR C3H 0	WDS C2H 0	WDE C1H 0	WDWR C0H 0	BITS
PSI BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH 0	PT0 B9H 0	PX0 B8H 0	BITS
RD B7H 1	WR B6H 1	T1 B5H 1	T0 B4H 1	INT1 B3H 1	INT0 B2H 1	TxD B1H 1	RxD B0H 1	BITS
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS
A7H 1	A6H 1	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	TI 99H 0	RI 98H 0	BITS
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS

SPICON[1] F8H 04H	DAC0L F9H 00H	DAC0H FAH 00H	DAC1L FBH 00H	DAC1H FCH 00H	DACCON FDH 04H	RESERVED	RESERVED
B[1] F0H 00H	ADCOFSL[3] F1H 00H	ADCOFSH[3] F2H 20H	ADCGAINL[3] F3H 00H	ADCGAINH[3] F4H 00H	ADCCON3 F5H 00H	RESERVED	SPIDAT F7H 00H
I2CCON[1] E8H 00H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ADCCON1 EFH 40H
ACC[1] E0H 00H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
ADCCON2[1] D8H 00H	ADCDATAL D9H 00H	ADCDATAH DAH 00H	RESERVED	RESERVED	RESERVED	RESERVED	PSMCON DFH DEH
PSW[1] D0H 00H	RESERVED	DMAL D2H 00H	DMAH D3H 00H	DMAP D4H 00H	RESERVED	RESERVED	PLLCON D7H 53H
T2CON[1] C8H 00H	RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
WDCON[1] C0H 10H	RESERVED	CHIPID C2H XXH	RESERVED	RESERVED	RESERVED	EDARL C6H 00H	EDARH C7H 00H
IP[1] B8H 00H	ECON B9H 00H	RESERVED	RESERVED	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H
P3[1] B0H FFH	PWM0L B1H 00H	PWM0H B2H 00H	PWM1L B3H 00H	PWM1H B4H 00H	NOT USED	NOT USED	SPH B7H 00H
IE[1] A8H 00H	IEIP2 A9H A0H	RESERVED	RESERVED	RESERVED	RESERVED	PWMCON AEH 00H	CFG841/CFG842 AFH 00H
P2[1] A0H FFH	TIMECON A1H 00H	HTHSEC A2H 00H	SEC A3H 00H	MIN A4H 00H	HOUR A5H 00H	INTVAL A6H 00H	DPCON A7H 00H
SCON[1] 98H 00H	SBUF 99H 00H	I2CDAT 9AH 00H	I2CADD 9BH 55H	NOT USED	T3FD 9DH 00H	T3CON 9EH 00H	NOT USED
P1[1,2] 90H FFH	I2CADD1 91H 7FH	I2CADD2 92H 7FH	I2CADD3 93H 7FH	NOT USED	NOT USED	NOT USED	NOT USED
TCON[1] 88H 00H	TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
P0[1] 80H FFH	SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H

2,

(   )   /   .   UART.

128

,   8   52   :

.

.   ,

,

.

,

80   —FFH.

,

.   ,

.

,

/ .

,

.

,

8   52   ADuC842

:

1.

,   ,   I2C   SPI,

EEPROM,   ;

2.   T2MOD, SADEN, SADDR,

IPH.

	,
PSW	,
IP	
IE	
2	2
SBUF	
SCON	
1	1
1	/ 1
	/
TL1	/ 1
TLO	/ 0
TMOD	/
TCON	/
PCON	
SP	
DPH, DPL	DPTR

-

8-   12-   -
2.4   .   13-   ,
,   .
.

0   +Vref.

Vref,   ,   .
,
2,5 .   ,
Vref—   (2,3   +
AVdd.   Vref   .
0   +Vref   ,
LSB (1/2LSB, 3/2LSBs, 5/2LSBs, .., FS-3/2LSBs).   Vref = +2,5 , 1LSB = 2.5 /4096 =
0.61   .   .

,

Vref.
.

1,6 $V_{DD} = 5$.

(
)   .
,
CONVST#.

2.

(DMA),

,   .
16   .
ADuC842

,
.
(ADCOFSL, ADCOFSH)   (ADCGAINL, ADCGAINH),
.

(8),   (9   10   ), Agnd   Vref (11   12).
: ADCCON1, ADCCON2   ADCCON3.
ADCDATAL, ADCDATAH.

111...111
111...110
111...101
111...100

$$1LSB = \frac{FS}{4096}$$

000...011
000...010
000...001
000...000

0V   1LSB   +FS

ADuC842

ADCCON1.   ADCCON1   ,   ,
         ,   ,   .

	7	6	5	4	3	2	1	0	
EFH	MD1	EXT_REF	CK1		AQ1	AQO	T2C	EXC	ADCCON1
.	0	1	0	0	0	0	0	0	
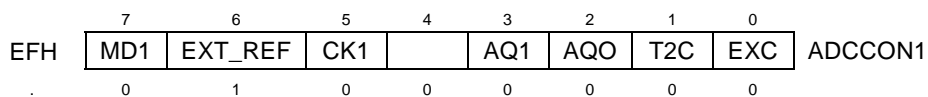
ADCCON1.7	MD1	:
		0
		1
ADCCON1.6	EXT_REF	:
		0
		1
ADCCON1.5	1	.
ADCCON1.4	0	
		.
		16 .
		1 0 MCLK
		0 0 1
		0 1 2
		1 0 4
ADCCON1.3	AQ1	. ,
ADCCON1.2	AQ0	:
		AQ1 AQO
		0 0 1
		0 1 2
		1 0 3
		1 1 4
		<8 ,
		AQ1=AQO=00 . 2—4 .
ADCCON1.1	2	2. ,
		2
		.
ADCCON1.0		. ,
		CONVST#
		(100).

ADuC842

ADCCON2.　　　　　　ADCCON2　　　　　　　　　　　　　　　　　　　,
　　　　　　　.

		7	6	5	4	3	2	1	0	
D8H		ADCI	DMA	CCONV	SCONV	CS3	CS2	CS1	CSO	ADCCON2
.		0	0	0	0	0	0	0	0	
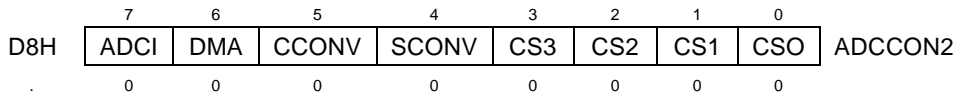
ADCCON2.7	ADCI	
		DMA. ADCI
		.
ADCCON2.6	DMA	DMA.
		DMA .
ADCCON2.5	CCONV	.
		.
		,
		.
ADCCON2.4	SCONV	.
		.
		.
ADCCON2.3	CS3	.
ADCCON2.2	CS2	. DMA
ADCCON2.1	CS1	.
ADCCON2.0	CSO	CS3　CS2　CS1　CSO
		0　　n2　　n1　　n0　　　　　　　　　　　(n2n1n0)
		1　　0　　0　　0
		1　　0　　0　　1　　　　　(0　　　)
		1　　0　　1　　0　　　　　(1　　　)
		1　　0　　1　　1　　Agnd
		1　　1　　0　　0　　Vref

　　　　　　　　　　　　　　　　　　　　　　　　　　　　　Vref　　Cref
　　　100　　(　　　　　　　　　　　　　　　　　　　　　　　　　　　Agnd.
　　　　　　　　　　　　　　.　　　　　　　　　　　　　Vref
　　　　　　　　　　　　　　　　　,　　　　　　　　　　　　　　　　　　　　.
　　,　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　,
　　　　　　　　　　　　　　　.
　　　　　　　　　　　　　　　　　　　　　　　　　　　　　ADCCON1-3
　　　　　　　　　　　　　　　　　　　　　　　12-
ADCDATAH(L).　　　　　　　　　　　　　　ADCDATAH　　　　　　　　　　.
　　　　　:

		7	6	5	4	3	2	1	0	
DAH				4				4		ADCDATAH

		7	6	5	4	3	2	1	0	
D9H					8					ADCDATAL
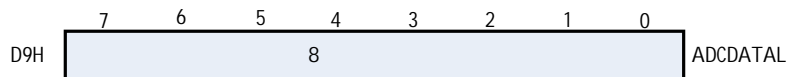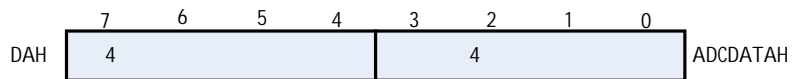
　　　　　　　　　　　　　　　　　　　　2,4　　　.　　　　　　　　　,
　　　(　　　　　　　　　　　　　　　　　　　　　　　　　　　　　)　　　2,4　　,
　　　　　　　　　　　　　　.　　　　　　　，
　　,　　　　　　　　　　　　　　　　.　　　　　DMA　　　　　　　　ADCCON2.6,
　　　　　　　　　　　　　　，
　　.

ADuC842

-

ADuC842   12-   .
DACCON,   DACOL/DAC1L   DACOH/DAC1H.
                                             (DACxL).
            ,   SYNC   DACCON.   8-   ,
        DACxL,   12-   .
    DACCON   ,   :

	7	6	5	4	3	2	1	0	
FDH	MODE	RNG1	RNG0	CLR1	CLR0	SYNC	PD1	PD0	ADCCON2
.	0	0	0	0	0	1	0	0	
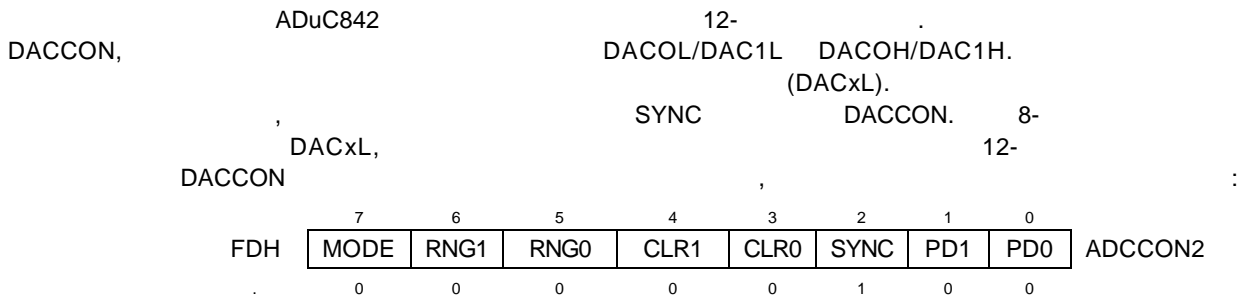
DACCON.7	MODE	MODE=1, 8- (8 DACxL). MODE =0, — 12- .
DACCON.6	RNG1	1. RNG1=1, 0..Vdd. RNG1=0, 0..Vref.
DACCON.5	RNG0	0 RNG0=1, 0..Vdd. RNG0=0, 0..Vref.
DACCON.4	CLR1	1 CLR1=1, 1 . CLR1=0, 1=0 .
DACCON.3	CLR0	0 CLR0=1 , 0 . CLR0=0, 0=0 .
DACCON.2	SYNC	0/1 SYNC=1, , DACxL. , DACxL/H SYNC=0, SYNC=1.
DACCON.1	PD1	1. PD1=1, 1 PD1=0, 1 .
DACCON.0	PD0	0 PD0=1 , 0 . PD0=0, 0 .

ADuC842

/

ADuC842 16- / : 0, 1, 2 3. / MCS-51. / ( ), ( ).

0 1. 0 1 / (=0,1) TMOD.

TLx .

(/ # = 0) TLx F_{osc}.

(/ # =1) TLx «1» «0».

$F_{osc}/2$.

0 1 TMOD TCON.

89H	7	6	5	4	3	2	1	0	
	GATE	C/T	M1	M0	GATE	C/T	M1	M0	TMOD
.	0	0	0	0	0	0	0	0	

88H	7	6	5	4	3	2	1	0	
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	TCON
.	0	0	0	0	0	0	0	0	

TMOD.7	GATE	1. GATE1=1 1 , TR1=1. GATE1=0 TR1=1 INT1#=1.
TMOD.6	C/T#	1. C/T#=1 , /T#=0 — .
TMOD.5	M1	1 1.
TMOD.4	M0	0 1.
TMOD.3	GATE	0. GATE0=1 0 TR0=1. GATE0=0 TR0=1 INT0#=1.
TMOD.2	C/T#	0. C/T#=1 , C/T#=0 — .
TMOD.1	M1	1 0.
TMOD.0	M0	0 0.

TCON.7	TF1	1. FFH . .
TCON.6	TR1	1. TR1=1 .
TCON.5	TF0	0. FFH . .
TCON.4	TR0	0. TRO=1 .
TCON.3	IE1	INT1#.
TCON.2	IT1	INT1#. I 1=1 "1"-"0", I 1=0 .
TCON.1	IE0	INT0#.
TCON.0	IT0	INT0#. I 0=1 "1"-"0", ITO=0 .

M1   0   /   :

1	0	
0	0	**0.** 8- / . TLx 5- .
0	1	**1**. 16- / . TLx .
1	0	**2.** 8- / TLx .
1	1	**3.** TL0 8- / , 0. 8- / , 1. 1 .

TRx,   GATEx=0.   «1»
«0»,   TFx.   GATEx=1
INTx#   .

.

2.   16-   /   ,   .
                                                    T2CON.

RCLK+TCLK	CAP2	TR2	
0	0	1	16- /
0	1	1	16- / ( )
1	X	1	
X	X	0	

                              2   2 TL2.   ,
            RCAP2H   RCAP2L,   T2CON.

T2CON.7	TF2	2. FFH 00 . . TF2 , RCLK=1 L =1.
T2CON.6	EXF2	2. "1"-"0" 2 , EXEN2=1. 2.
T2CON.5	RCLK	1 3. RCLK=1 2, RCLK=0 1.
T2CON.4	TCLK	1 3. L =1 2, TCLK=0 1.
T2CON.3	EXEN2	2. EXEN2=1 EXF2.
T2CON.2	TR2	/ 2. TR2=1 .
T2CON.1	CNT2	2. CNT2=1 , N 2=0 .
T2CON.0	2	2. 2#=1 "1"-"0" 2 . 2=0 "1"-"0" T2EX 2.

2   / 2#   T2CON.   / 2# = 1

,   / 2# = 0   .   2

(2=1),   (2=0).   (   )

2, TL2

RLAP2H, RLAP2L.

2   , TF2   EXF2.

2   .   TF2

2 (RCLK=TCLK=0),   EXF2   «1» - «0»

2   .

3.   3   ,

UART.   3   T3CON   T3FD.

UART   *BaudRate*,

DIV   *T3FD*   :

$$DIV = \log_2\left(\frac{f_{osc}}{16 \cdot BaudRate}\right) \qquad T3FD = \frac{2 \cdot f_{osc}}{2^{DIV-1} \cdot BaudRate} - 64$$

f_{osc} —   .

DIV   ,   *T3FD* —   .

DIV   *T3FD*   UART:

$$ActualBaudRate = \frac{2 \cdot f_{osc}}{2^{DIV-1} \cdot (T3FD + 64)}$$

	7	6	5	4	3	2	1	0	
9EH	T3BAUDEN	—	—	—	—	DIV2	DIV1	DIV0	T3CON
.	0	0	0	0	0	0	0	0	

	7	6	5	4	3	2	1	0	
9DH	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	T3FD
.	0	0	0	0	0	0	0	0	

T3CON.7	T3BAUDEN	3. T3BAUDEN=1, 3 UART, PCON.7, T2CON.4 T2CON.5 . T3BAUDEN=0, UART 8052.
T3CON.6	—	, .
T3CON.5	—	
T3CON.4	—	
T3CON.3	—	
T3CON.2		*DIV*
T3CON.1		DIV2 DIV1 DIV0 DIV
T3CON.0		0 0 0 0
		0 0 1 1
		0 1 0 2
		0 1 1 3
		1 0 0 4
		1 0 1 5
		1 1 0 6
		1 1 1 7

ADuC842

UART

UART

.   ,   UART   duC842
            8x52,   SADEN, SADDR   .
SBUF   UART.
        ,   .   SCON
            UART,   .

	7	6	5	4	3	2	1	0	
98H	SMO	SM1	SM2	REN	TB8	RB8	TI	RI	SCON
.	0	0	0	0	0	0	0	0	

	7	6	5	4	3	2	1	0	
99H	BUF7	BUF6	BUF5	BUF4	BUF3	BUF2	BUF1	BUF0	SBUF
.	0	0	0	0	0	0	0	0	

SCON.7	SM0	UART.
SCON.6	SM1	SM0 SM1
		0 0 8- fosc/2
		0 1 8-
		1 0 9- fosc/32 fosc/16
		1 1 9-
SCON.5	SM2	2
		3.
SCON.4	REN	.
SCON.3	TB8	9- 2 3.
SCON.2	RB8	9- 2 3.
SCON.1	TI	. «0»
		. «1»
		.
SCON.0	RI	. «1»
		.
		SBUF.

I²C

I²

«   »   1-10

«1» — «0»,   «1»:

MSB   LSB   MSB   LSB

SDATA

R/W

SCLOCK

3 - 6   2 - 7

1   2   7   8   9   1   8   9

ACK bit   ACK bit   Stop bit

Start bit
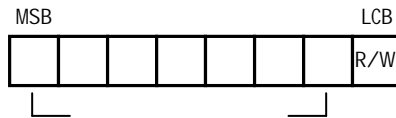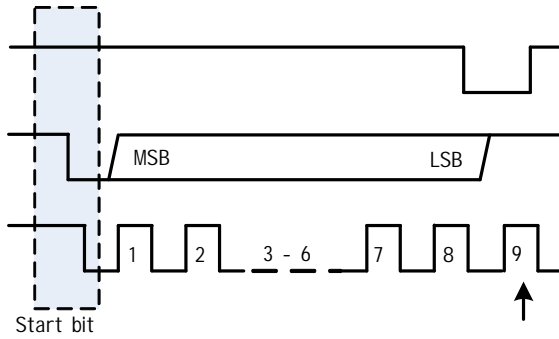
I²   SCLOCK,

(MSB),

R/W#.   :   R/W# = 0

,   R/W# = 1

MSB   LCB

R/W

/   ,

.

«0»   9-   .

MSB   LSB

1   2   3 - 6   7   8   9

Start bit

«STOP».

«0» — «1»   «1»   .

ADuC842   I²

I²   .

I2CDAT   ,   I2CADD   ,   I2CCON —

.   I2CCON   I² ,   .

	7	6	5	4	3	2	1	0	
9AH	DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0	I2CDAT
.	0	0	0	0	0	0	0	0	

	7	6	5	4	3	2	1	0	
9BH	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	I2CADD
.	0	0	0	0	0	0	0	0	

	7	6	5	4	3	2	1	0	
E8H	MDO	MDE	MCO	MDI	I2CM	I2CRS	I2CTX	I2CI	I2CCON
.	0	0	0	0	0	0	0	0	

ADuC842

I2CCON.7	MDO	.
I2CCON.6	MDE	.
I2CCON.5	MCO	.
I2CCON.4	MDI	.
I2CCON.3	I2CM	.
I2CCON.2	I2CRS	I2C.
I2CCON.1	I2CTX	.
I2CCON.0	I2CI	I2C

I2CCON.   ,

START,   ,

.

I2CCON

SCLOCK   SDATA.   ,   I2C

,   I2CCON.

ADuC842   ,
                                              .   ,
                    ,   (   )   :

PSMI		43	1 ( )
WDS		5BH	2
IE0	INT0	0	2
ADCI		33	3
TF0	0	0	4
IE1	INT1	13	5
TF1	1	1	6
I2CI/ISPI		3	7
RI/TI		23	8
	UART		
TF2/EXF2	2	2	9
TII		53H	11 ( )
	TIC		

         ,   ,   :
1.   ,
      (   ).
2.   IE   ( ) «1»;
3.   IE   IEIP2   «1».
                                                           IE, IP   IEIP2.   IE   IP
              ,   IE2   .   IE
                                       .
              «1».

	7	6	5	4	3	2	1	0	
A8H	IE	EADC	ET2	ES	ET1	EX1	ET0	EX0	IE
.	0	0	0	0	0	0	0	0	

IE.7	IE	.
		. =0,
		.
IE.6	EADC	.
IE.5	ET2	2.
IE.4	ES	UART.
IE.3	ET1	1.
IE.2	EX1	INT1.
IE.1	ET0	0.
IE.0	EX0	INT0 EX0.

ADuC842

IP   IEIP2   .
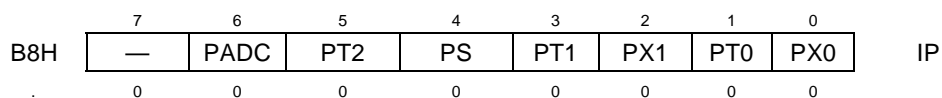
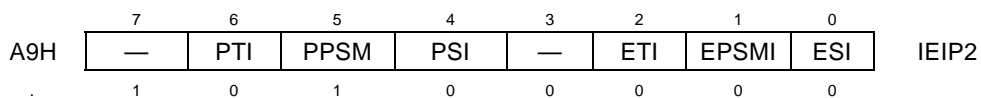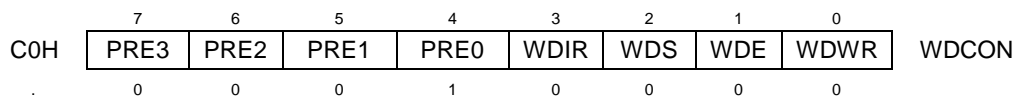«1»   , «0» —   .

.   IEIP2

SPI   I2 .

«1».   .

	7	6	5	4	3	2	1	0	
B8H	—	PADC	PT2	PS	PT1	PX1	PT0	PX0	IP
.	0	0	0	0	0	0	0	0	

IP.7	—	.
IP.6	PADC	.
IP.5	PT2	2.
IP.4	PS	UART.
IP.3	PT1	1.
IP.2	PX1	
		INT1.
IP.1	PT0	0.
IP.0	PX0	
		INT0.

	7	6	5	4	3	2	1	0	
A9H	—	PTI	PPSM	PSI	—	ETI	EPSMI	ESI	IEIP2
.	1	0	1	0	0	0	0	0	

IEIP2.7	—	.
IEIP2.6	PTI	
		TIC.
IEIP2.5	PPSM	.
IEIP2.4	PSI	SPI/I2C.
IEIP2.3	—	«0».
IEIP2.2	ETI	TIC.
IEIP2.1	EPSMI	.
IEIP2.0	ESI	SPI/I2C.

С

(WDT)   .
WDCON.

	7	6	5	4	3	2	1	0	
C0H	PRE3	PRE2	PRE1	PRE0	WDIR	WDS	WDE	WDWR	WDCON
.	0	0	0	1	0	0	0	0	

WDCON.7	PRE3	
WDCON.6	PRE2	PRE3 PRE2 PRE1 PRE0 ,
WDCON.5	PRE1	0 0 0 0 15,6
WDCON.4	PRE0	0 0 0 1 31,2
		0 0 1 0 62,5
		0 0 1 1 125
		0 1 0 0 250
		0 1 0 1 500
		0 1 1 0 1000
		0 1 1 1 2000
		1 0 0 0 0,0
		PRE3-0 > 1000
WDCON.3	WDIR	WDIR=1,
		.
WDCON.2	WDS	«1», .
		«0» .
WDCON.1	WDE	. «1»
		,
		.
WDCON.0	WDWR	.

,   WDE   WDCON.   PRE3—PRE0
,   .
.   ,
.   WDE.
,
.