

MAINTENANCE
MANUAL
SCORPION®

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**1/4" Streaming Tape Drive
MAINTENANCE MANUAL**

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CHAPTER 1

INTRODUCTION

1.1 SCOPE

This manual contains maintenance information for the Scorpion Intelligent and Basic 1/4-inch streaming cartridge tape drives (Figure 1-1). This manual applies to the models listed in Table 1-1. Included in this manual are physical description, specifications, theory of operations, maintenance procedures and field replaceable parts list.

Table 1-1 Equipment Model Identification

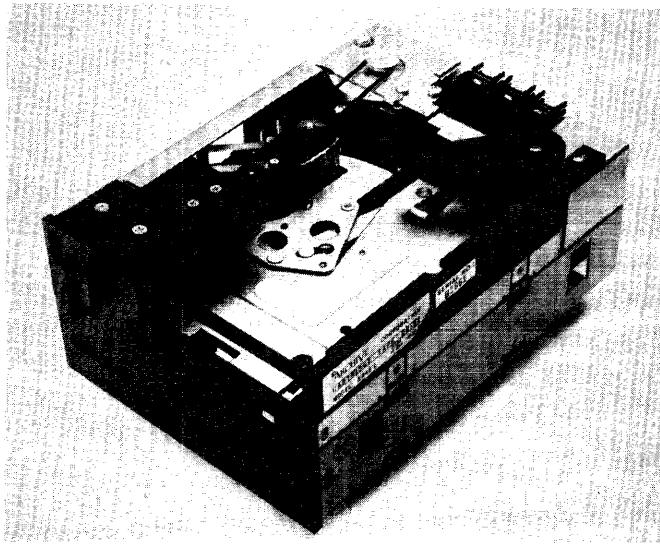
MODEL	PART NUMBER	TAPE FORMAT
5920-C	20232-XXX	—
5920L-1	20238-XXX	QIC-11
5920L-2	20279-XXX	QIC-11/QIC-24
5945C	20233-XXX	—
5945L-1	20239-XXX	QIC-11
5945L-2	20278-XXX	QIC-11/QIC-24

1.2 RELATED DOCUMENTS

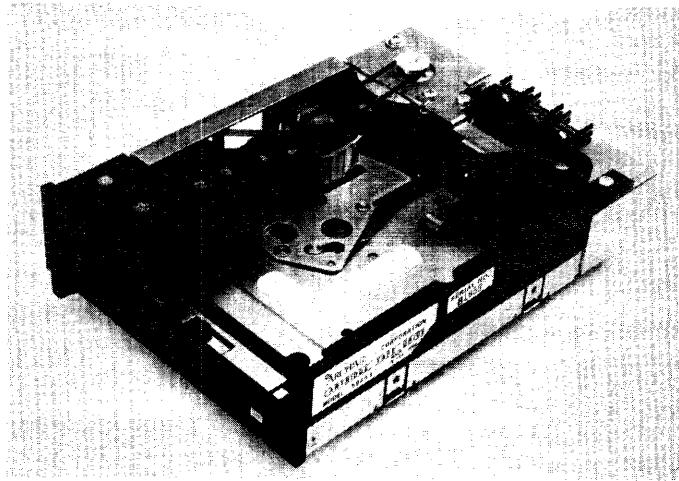
- Scorpion Product Description, Part Number 20271-001
- Recommended Procedures for Incoming Inspection, Part Number 20414-001

1.3 PHYSICAL DESCRIPTION

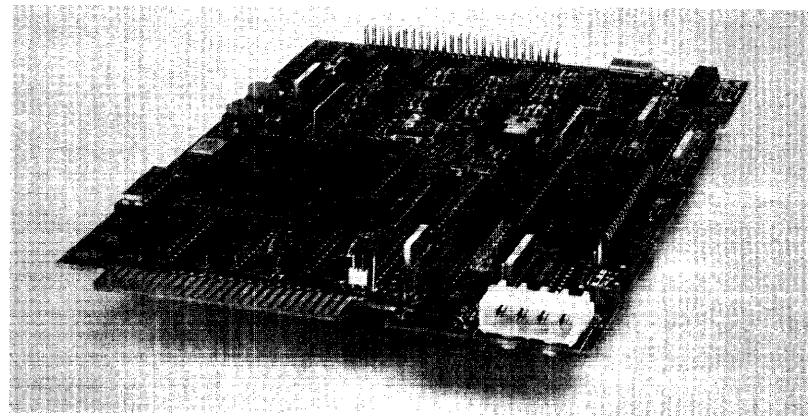
The Scorpion is a 1/4-inch streaming cartridge tape drive designed to be easily installed in the 5-1/4 inch floppy disk mounting space. Its primary function is dependable and efficient backup for Winchester disk drives in the 10 to 160 megabyte range. The Scorpion is available in two different configurations; Basic tape drive and Intelligent tape drive. The Scorpion uses a 1/4-inch cartridge tape to record data supplied by the host system.



Scorpion Intelligent 1/4-Inch Cartridge Streaming Tape Drive



Scorpion Basic 1/4-Inch Cartridge Streaming Tape Drive



Scorpion Stand-Alone Controller (SAC) PCB

Figure 1-1 Scorpion Tape Drive

1.3.1 Basic Tape Drive

The Basic tape drive (Figure 1-1) consists of a half-high compact metal chassis containing the head assembly, capstan drive motor, main PCB, motor driver PCB, tape hole sensors, and the cartridge in place with safe sensing switches. The Basic drive also contains mechanical devices to facilitate loading, positioning, and unloading the tape cartridge. The main PCB assembly is mounted below the tape cartridge loading area, and the capstan motor driver PCB is mounted behind the cartridge loading area. Interface to the Basic drive is through the industry standard QIC-36 interface.

1.3.2 Intelligent Tape Drive

The Scorpion Intelligent tape drive (Figure 1-1) is available in two optional configurations. The full-high Intelligent option combines the Basic tape drive (paragraph 1.3.1) with the Stand-Alone Controller (SAC) PCB. In this configuration the SAC is mounted in a metal chassis and is installed beneath the Basic tape drive.

The half-high Intelligent option (Figure 1-2) also uses the Basic tape drive and the SAC. However, in this configuration the SAC is mounted separately in a remote location and is interconnected with a ribbon cable. The maximum allowable separation for the ribbon cable is 9 feet, 10 inches (3 meters).

1.3.3 Stand-Alone Controller

The SAC PCB (Figure 1-1) contains independent read and write channels, buffer memories, QIC-02 host interface, QIC-36 drive interface, and a microcomputer. Large Scale Integration (LSI) is employed extensively in the SAC. The microcomputer makes tape formatting, tape error processing, tape positioning, and tape motion control invisible to the host system. In addition, the microcomputer provides statistical error data to monitor progressive deterioration to the tape system, caused by bad tapes and/or marginal components. Data commands and status information are transmitted via the industry standard QIC-02 interface.

1.3.4 Tape Cartridge

1/4-inch wide tape, contained in a cartridge, is used as a storage media. The cartridge is described mechanically by ANSI Standard X3.55-1982. The Scorpion uses the DC300XL or equivalent (450 feet long) or the DC600A or equivalent (600 feet long) 1/4-inch tape cartridge.

Different write currents are required for the two cartridges, due to the difference in oxide coating thickness and coercivity. The Intelligent tape drive automatically determines the cartridge type by measuring the distance between the Beginning Of Tape (BOT) and load point holes (3 feet for DC300XL and 4 feet for DC600A) and selects the appropriate write current for the cartridge that is inserted.

1.4 EQUIPMENT SPECIFICATIONS

The performance, environmental, power, and physical specifications of the equipment are listed in Tables 1-2 through 1-7.

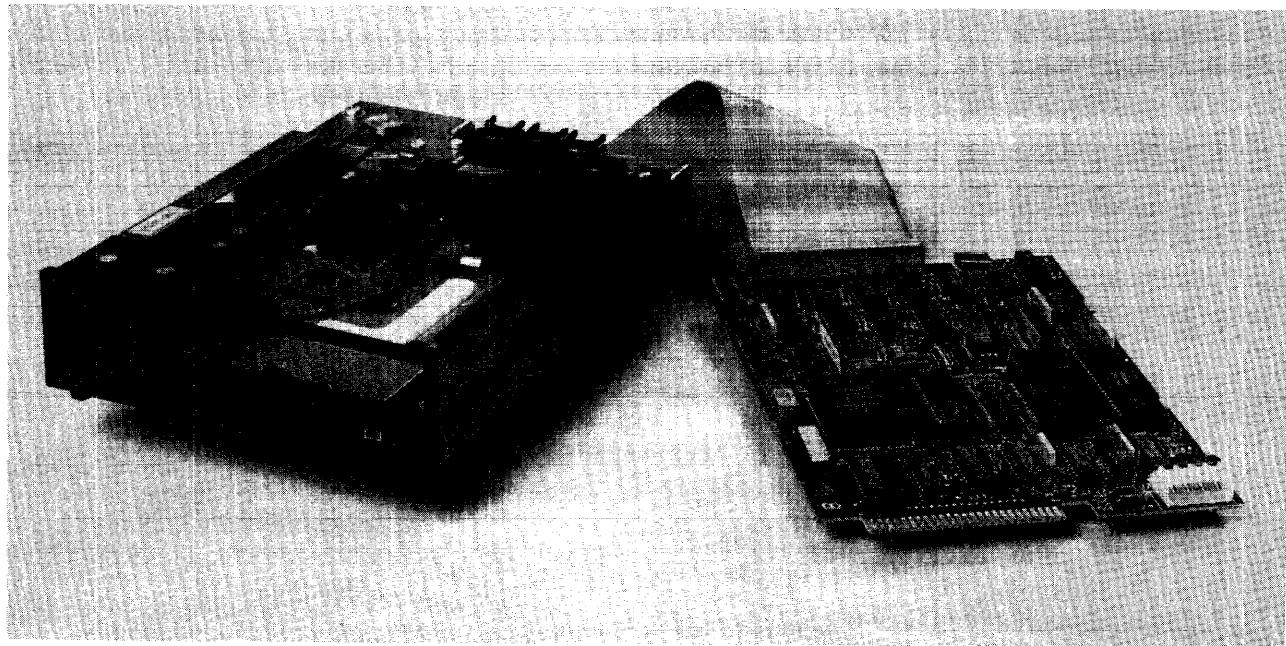


Figure 1-2 Half-High Basic Tape and SAC PCB

Table 1-2 Performance Specification Summary

ITEM	MODEL*	
	5920L-1 5920L-2 5920C	5945L-1 5945L-2 5945C
No. of Tracks	4	9
No. Channels**	2	2
Capacity DC300XL	20 megabytes	45 megabytes
Capacity DC600A	26.7 megabytes	60 megabytes
Backup Time DC300XL	4 minutes	9 minutes
Backup Time DC600A	5.2 minutes	12 minutes
Recording Mode	NRZI	NRZI
Recording Data Density	8,000 bpi	8,000 bpi
Encoding Method (Intelligent Scorpion)	4 to 5 RLL***	4 to 5 RLL***
Recording Density	10,000 ftpi	10,000 ftpi
Track Capacity DC300XL	5.0 megabytes	5.0 megabytes
Track Capacity DC600A	6.6 megabytes	6.6 megabytes
Data Transfer Rate	90K bytes/second	90K bytes/second
Tape Speed	90 ips	90 ips
Start/Stop Time	300 ms (max.)	300 ms (max.)

*C = Basic Scorpion tape drive

*L = Intelligent Scorpion tape drive

**Channel is defined as one write head gap followed by one read head gap.

***RLL is defined as 'Run Length Limited'.

Table 1-3 Environmental Requirements

CHARACTERISTIC	OPERATIONAL	NON-OPERATIONAL
Temperature	+ 5° to + 46°C (+ 41° to + 115°F)	- 40° to + 60°C (- 40° to + 140°F)
Relative Humidity	20 to 80% (non-condensing)	0 to 99% (non-condensing)
Thermal Gradient	1°C/min (33.8°F/hr)	
Altitude	- 1,000 ft to 15,000 ft	- 1,000 ft to 50,000 ft
Shock	2.5g max. (1/2 sine wave, 11 msec duration on any axis)	25g max. (1/2 sine wave, 11 msec duration on any axis)
Vibration	0.005 inch max. peak to peak displacement 0 to 45 Hz, 0.5g peak max. acceleration 45 to 600 Hz	0.5 inch max. peak to peak displacement, 0 to 8 Hz, 1.5g peak max. acceleration 17 to 600 Hz

Table 1-4 Basic Tape Drive Physical Specifications

CHARACTERISTIC	SPECIFICATION	
Depth	8.00 \pm 0.02 inches	(20.32 \pm 0.51 cm)
Width	5.75 \pm 0.02 inches	(14.605 \pm 0.51 cm)
Height	1.625 \pm 0.01 inches	(4.126 \pm 0.25 cm)
Weight	3.0 \pm 0.5 pounds	(1.36 \pm 0.23 kg)

Table 1-5 Basic Tape Drive Power Requirements

CHARACTERISTICS	DC VOLTAGE	
	+ 12 Volts	+ 5 Volts
Tolerance (includes 200 mv max. ripple)	$\pm 10\%$	$\pm 5\%$
Operational Current	1.6 \pm 0.8 amps (Cartridge Dependent)	0.6 amps max.
Tape Start or Stop Surge Current	4.4 amps max. up to 300 msec*	0.6 amps (no surge increase)

*May be longer if cartridge is defective.

Table 1-6 Intelligent Tape Drive Physical Specifications

CHARACTERISTICS	SPECIFICATION
Depth	8.45 \pm 0.02 inches (214.6 \pm 0.51 mm)
Width	5.75 \pm 0.02 inches (146.05 \pm 0.51 mm)
Height	3.25 \pm 0.02 inches (82.55 \pm 0.51 mm)
Weight	3.75 \pm 0.5 pounds (1.7 \pm 0.23 kg)

Table 1-7 Intelligent Tape Drive Power Requirements

CHARACTERISTICS	D.C. VOLTAGE	
	+12 Volts	+5 Volts
Tolerance (includes 200 mv max. ripple)	±5%	±5%
Operational Current	1.75 ± 0.8 (Cartridge Dependent)	2.4 amps max.
Tape Start or Stop Surge Current	4.0 amps max. up to 300 msec*	2.4 amps (no surge increase)
Power On Surge Current	Thru 1,200 uf max. capacitance	Thru 25 uf max. capacitance
Voltage Rise Time	100 ms max.	50 ms max., else RST-
Power Sequence	None	None
Power Dissipation (in continuous streaming mode)	19 watts (Typical)	3 watts (Typical)
Power Dissipation (during start or stop power surges)	48 watts	3 watts

*May be longer if cartridge is defective.

1.5 REQUIRED SUPPLIES, TOOLS, AND TEST EQUIPMENT

The following is a complete list of supplies, tools, and test equipment necessary to perform testing and maintenance as outlined in Chapters 6 and 7. These items will also be mentioned where used in a procedure.

1. A host system that will provide:
 - a. Power of +12 VDC and +5 VDC to the tape drive.
 - b. Diagnostic capability that includes: RESET, ERASE, RETENSION, WRITE, READ, and READ STATUS operations. The write operation must be able to alter the data pattern to those specified in testing.
2. A shop quality oscilloscope which must include 60MHZ minimum response, two channels, dual trace and accompanying X10 probes in its complement of functions and accessories.
3. One digital multimeter.
4. Model 09C tape cartridge. (Archive P/N 20121-001)
5. Azimuth alignment cartridge. (Archive P/N 20072-001)
6. Track zero alignment tape.
Nine track drives (Archive P/N 20180-001)
Four track drives (Archive P/N 20071-001)
7. Zenith alignment check tool. (Archive P/N 90098-xxx)
8. Shop tools must include:
 - a. Numbers one and two Phillips screwdrivers.
 - b. 5/64-inch (2 1/2-mm) Allen wrench.
9. Jumper clips for connecting adjacent pins on PCB jumper blocks.
10. 14 or 16-pin IC test clip.
11. Lintless cotton swabs.
12. Isopropyl alcohol.
13. Small vacuum cleaner.
14. Soft bristle brush.

CHAPTER 2

INSTALLATION AND OPERATION

2.1 PRELIMINARY CONSIDERATIONS

2.1.1 Power Requirements

The power requirements of the Basic tape drive and the Intelligent tape drive are listed in Tables 1-5 and 1-7, respectively. Power is plugged into the Basic tape drive at connector J2 on the motor driver PCB as shown in Figure 2-1. For the Intelligent tape drive, two separate but identical input power connectors are required (see Figure 2-2). Power is plugged into the Intelligent tape drive at connector J2 on the motor driver PCB and connector J2 on the SAC PCB.

The mating power connectors for the Basic and Intelligent tape drives are AMP type 1-48024-0 with AMP type 60619-1 female contact pins. The power connector pin assignments for both the Basic and Intelligent tape drives are listed in Table 2-1.

2.1.2 Space Requirements

The Scorpion Basic tape drive is designed to be installed in the half-high 5 1/4-inch floppy disk mounting space. The physical specifications of the Basic tape drive are listed in Table 1-4 and shown in Figure 2-3.

The Scorpion Intelligent tape drive is designed to be installed in the full-high 5 1/4-inch floppy disk mounting space. The physical specifications of the Intelligent tape drive are listed in Table 1-6 and shown in Figure 2-4.

The SAC PCB may be installed in the Archive supplied controller chassis as part of the full-high Scorpion Intelligent tape drive configuration, or installed separately in a remote location. The physical specifications for the SAC PCB are shown in Figure 2-5.

Free air flow is required for the Basic or Intelligent tape drive to prevent the ambient temperature from rising above 45 degrees C (113 degrees F) under operating conditions. Otherwise, forced-air cooling must be supplied to achieve the operating temperature requirements.

Table 2-1 Power Connector J2 Pin Assignments

PIN	FUNCTION
J2-1	+ 12 VDC
J2-2	+ 12 V RET
J2-3	+ 5 V RET
J2-4	+ 5 VDC

Note: Pins J2-2 and J2-3 are tied together on the PCB.

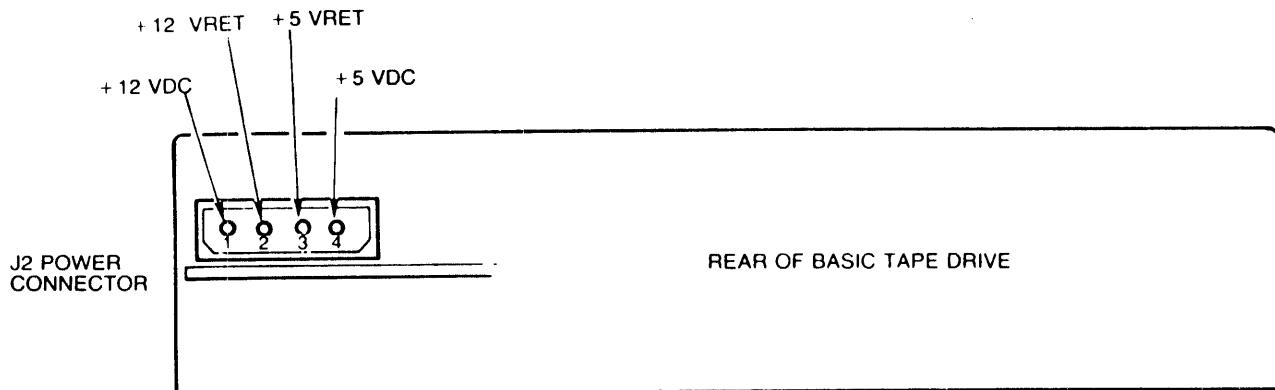


Figure 2-1 Basic Tape Drive Power Connector J2

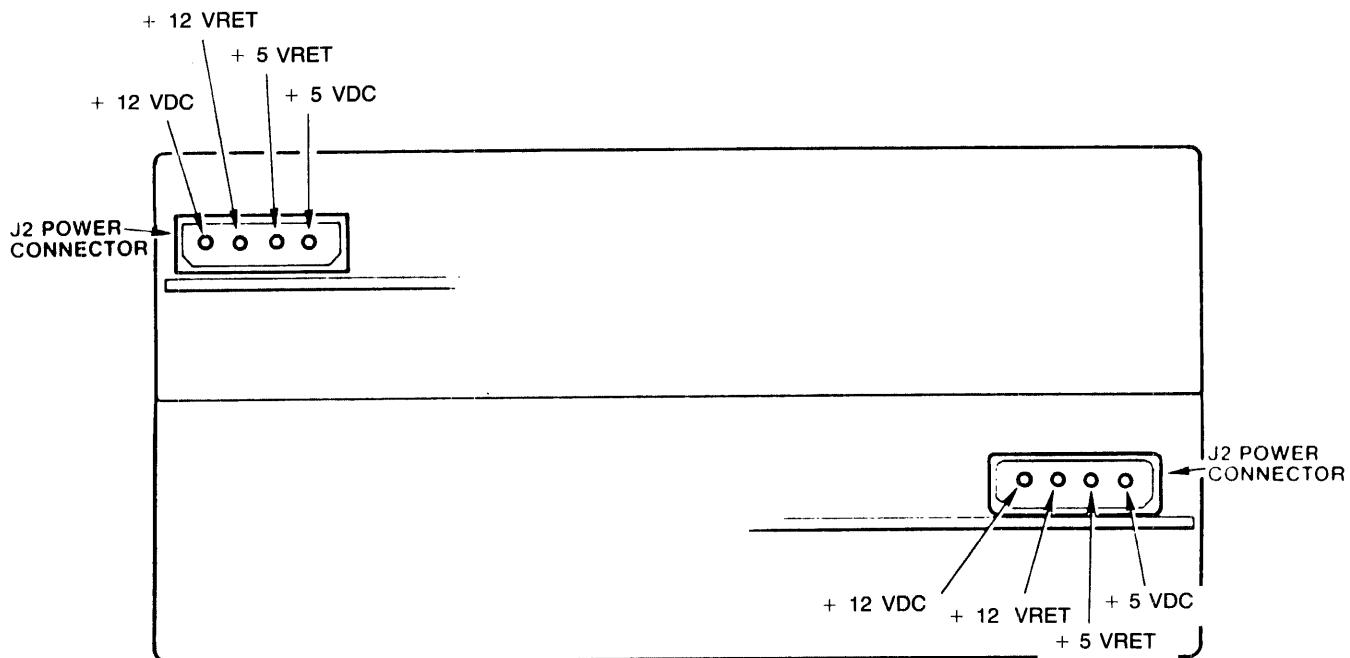


Figure 2-2 Intelligent Tape Drive Power Connector J2

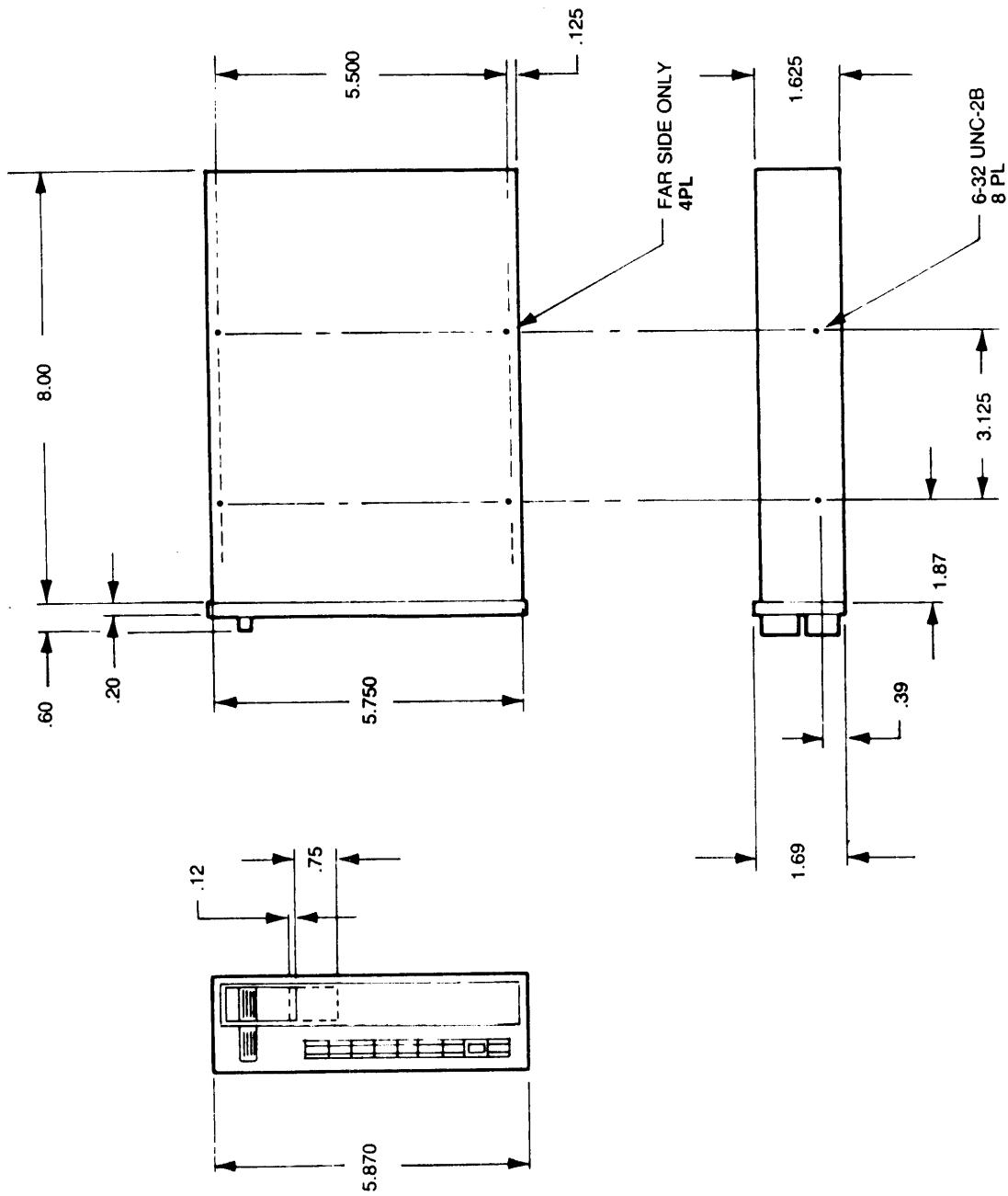


Figure 2-3 Basic Tape Drive Outline Drawing

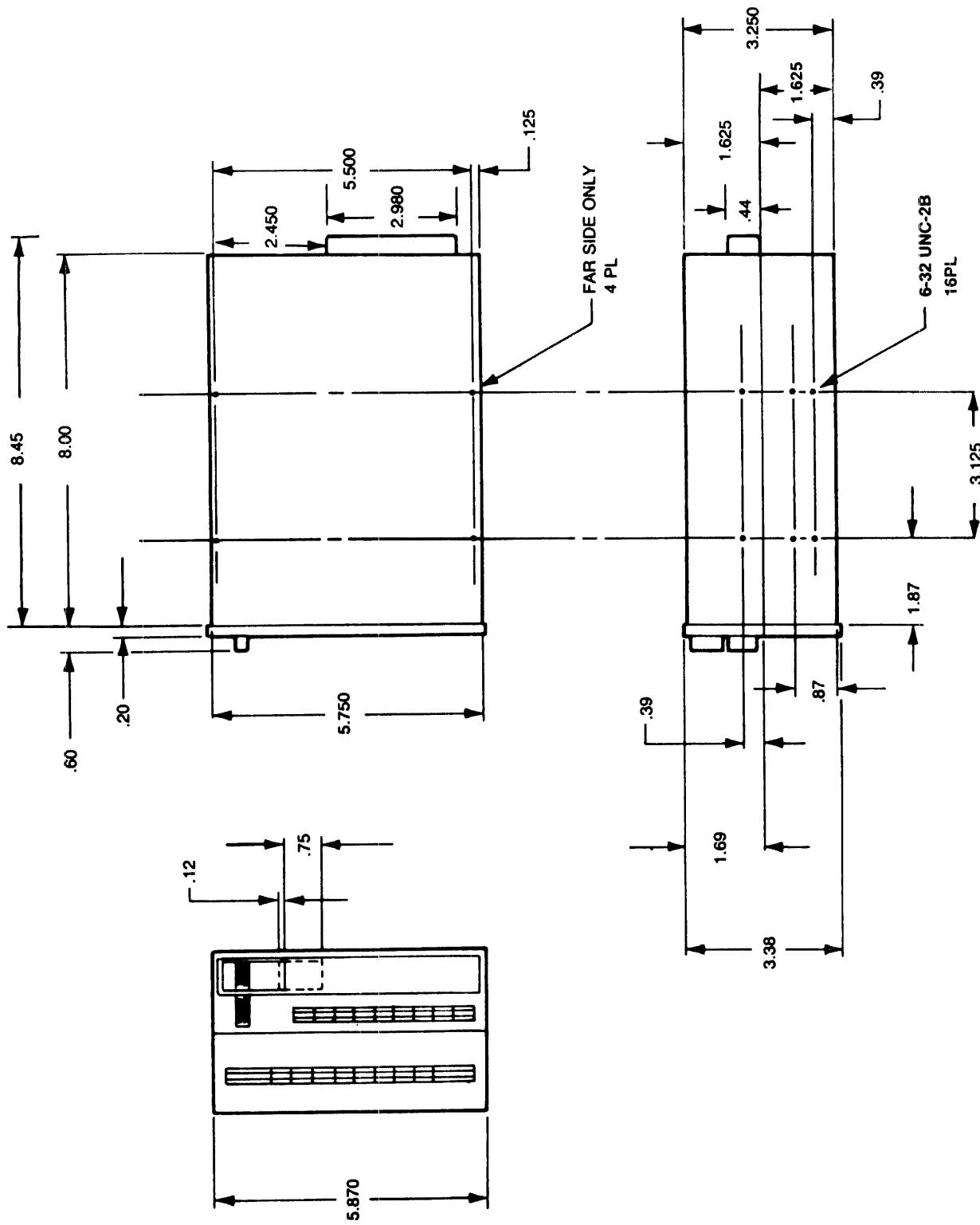
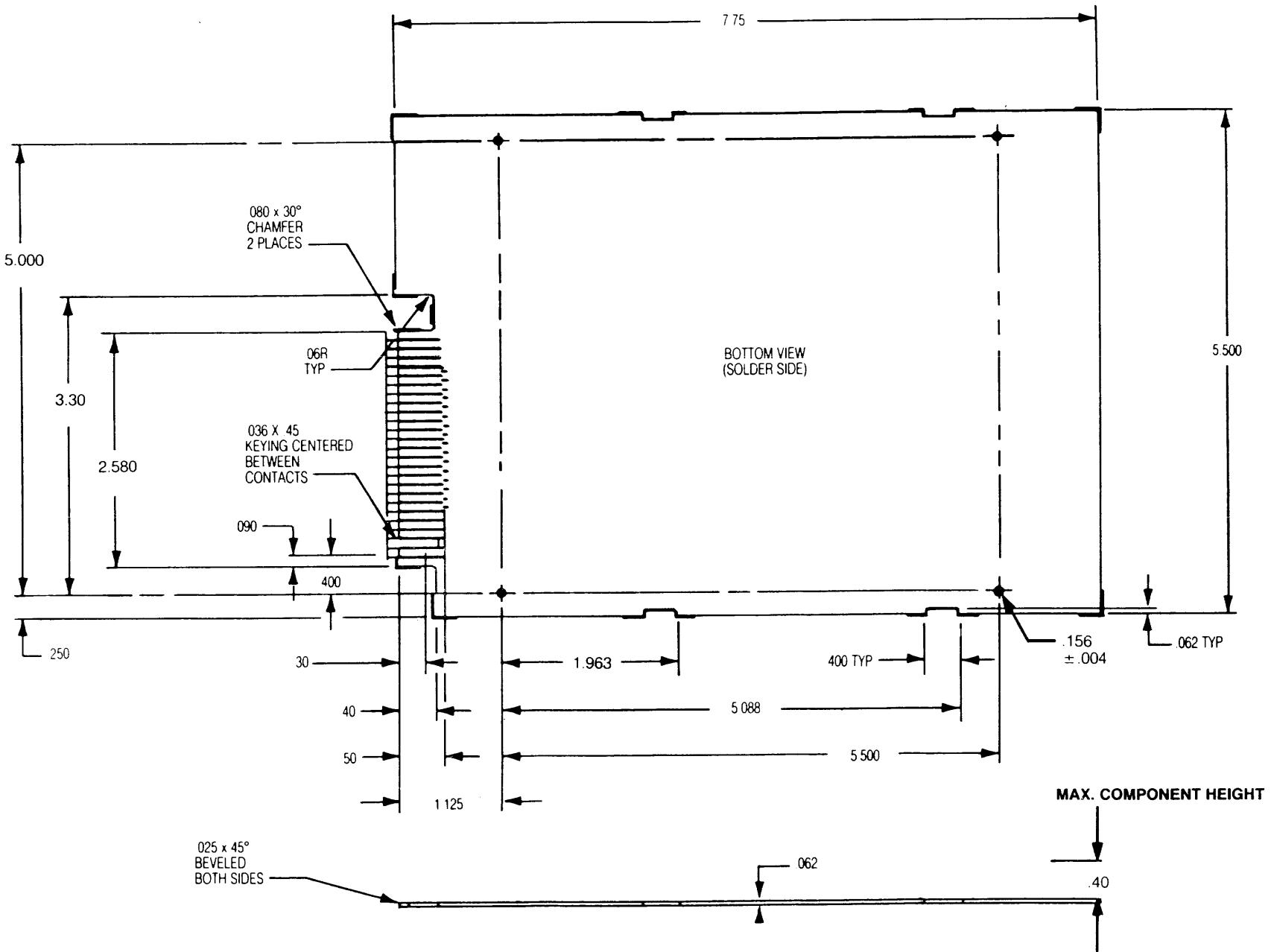


Figure 2-4 Intelligent Tape Drive Outline Drawing

2-5

Figure 2-5 Stand-Alone Controller Outline Drawing

2.1.3 System Connections

The Basic tape drive QIC-36 industry standard interface provides the required interconnection between the tape drive and the SAC. Fifteen lines are used for signals from the SAC and seven lines are used for signals that originate in the Basic tape drive. The Basic tape drive interface connector (J1) is shown in Figure 2-6. The interface connector pin assignments are listed in Table 2-2. The maximum allowable length of the Basic tape drive interface cable is 9 feet, 10 inches (3 meters).

The host QIC-02 industry standard interface provides the required interconnections between the SAC PCB and the host CPU. These requirements are applicable to the full-high Intelligent tape drive configuration and to the Intelligent tape drive in two separate assemblies (Basic tape drive with SAC). Control signals, data commands, and status information are transmitted to and from the Intelligent drive via the QIC-02 interface. The host-interface connector (J1) is shown in Figure 2-7 and the connector pin assignments are listed in Table 2-3. The connection is through a 50-pin PCB edge connector. The pins are numbered 1 through 50 with the even numbered pins located on the component side of the SAC PCB. There is a key slot located between pins 4 and 6 to ensure that the mating connector is installed in the correct position. The recommended mating connector is a 3M type 3415-001, 50-pin connector.

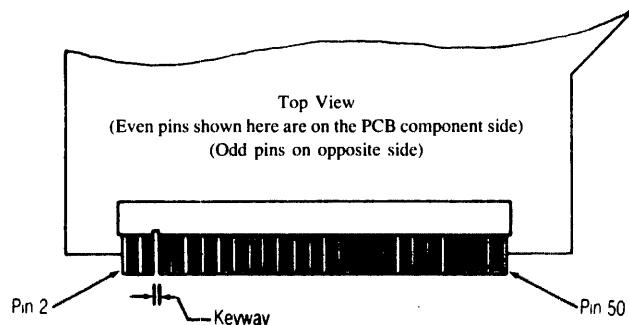


Figure 2-6 Basic Tape Drive QIC-36 Interface Connector J1

**Table 2-2 Basic Tape Drive QIC-36 Interface Connector
J1 Pin Assignments**

PIN#	MNEMONIC	TO	NAME
02	GO -	D	Go control for capstan servo
04	REV -	D	Direction control for capstan servo
06	TR3 -	D	Track select bit 3 (MSB)
08	TR2 -	D	Track select bit 2
10	TR1 -	D	Track select bit 1
12	TR0 -	D	Track select bit 0 (LSB)
14	RST -	D	Reset
16	RES	R	Reserved
18	RES	R	Reserved
20	RES	R	Reserved
22	DS0 -	D	Drive select control
24	HC -	D	High write current for DC 600A tape
26	RDP -	C	Read pulse output
28	UTH -	C	Upper tape position signal
30	LTH -	C	Lower tape position signal
32	SLD -	C	Selected response from the drive
34	CIN -	C	Cartridge in place
36	USF -	C	Unsafe — (Cartridge safe plug is in "unsafe" position, i.e. writing is enabled.)
38	TCH -	C	Capstan tachometer pulses
40	WDA -	D	Write data signal
42	WDA +	D	Inverse write data signal
44	THD -	D	Increases threshold for reading data off tape to qualify the read data output.
46	HSD -	D	High speed (90 ips)
48	WEN -	D	Write enable control
50	EEN -	D	Erase enable control

LEGEND: D = Drive
C = Controller
R = Reserved

Note: All odd-numbered pins are connected to signal ground.

Table 2-3 QIC-02 Interface Connector Pin Assignments

PIN#	TO	MNEMONIC	DESCRIPTION
02	R	SPR-	Reserved
04	R	SPR-	Reserved
06	R	SPR-	Reserved
08	R	SPR-	Reserved
10	R	HBP-	Reserved*
12	B	HB7-	Host Bus Bit 7
14	B	HB6-	Host Bus Bit 6
16	B	HB5-	Host Bus Bit 5
18	B	HB4-	Host Bus Bit 4
20	B	HB3-	Host Bus Bit 3
22	B	HB2-	Host Bus Bit 2
24	B	HB1-	Host Bus Bit 1
26	B	HB0-	Host Bus Bit 0
28	D	ONL-	Online
30	D	REQ-	Request
32	D	RST-	Reset
34	D	XFR-	Transfer
36	H	ACK-	Acknowledge
38	H	RDY-	Ready
40	H	EXC-	Exception
42	H	DIR-	Direction
44	R	SPR-	Reserved
46	R	SPR-	Reserved
48	R	SPR-	Reserved
50	R	SPR-	Reserved

Note: All odd-numbered pins are signal returns.
They are connected to signal GND at the Host.

R = Reserved
B = Bi-directional
D = Drive
H = Host

*Reserved for host odd parity.

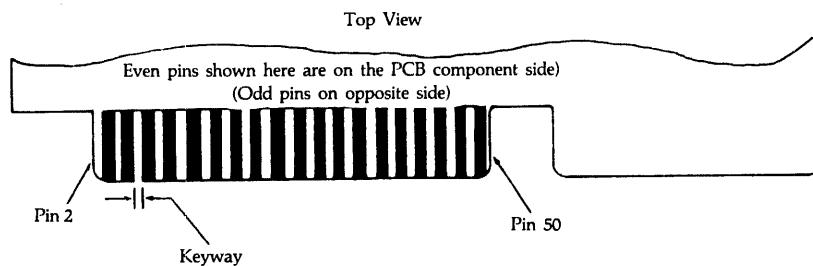


Figure 2-7 Host-Interface Connector J1

2.1.4 SAC and Basic Tape Drive Termination Requirements

The standard termination shall be 220 ohms to +5 VDC and 330 ohms to ground. Resistance tolerance shall be $\pm 5\%$. All signal lines to the controller shall be terminated at the controller, all signal lines to the drive shall be terminated at the drive.

Signals transmitted by the drive are capable of driving two TTL loads plus terminator. Signals received by the drive shall not exceed two TTL loads plus terminator.

2.1.5 Host and Tape Drive Termination Requirements

Signal terminations at the host are 220 ohms to +5 VDC and 330 ohms to ground. The host shall terminate the bi-directional data bus and the four control signal lines from the tape drive.

Signal terminations at the tape drive are 220 ohms to +5 VDC and 330 ohms to ground. These resistances are provided by a 16-pin resistor dual in-line package (DIP) located at socket 1E on the SAC PCB. The resistor DIP terminates the bi-directional data bus and 4 control signal lines from the host.

Signals from the host to the tape drive are loaded by no more than two milliamps and one terminator. The host shall not load the signals from the tape drive with more than two milliamps and one terminator.

2.1.6 PCB Jumper Configurations

The jumper locations on the main PCB and SAC PCB are established at the time of manufacture and must not be moved. The only exceptions are deliberate changes by qualified service personnel or during maintenance as described in this manual. The locations of the jumpers on the SAC PCB are shown in Figure 2-8. The SAC jumper configuration is listed in Table 2-4.

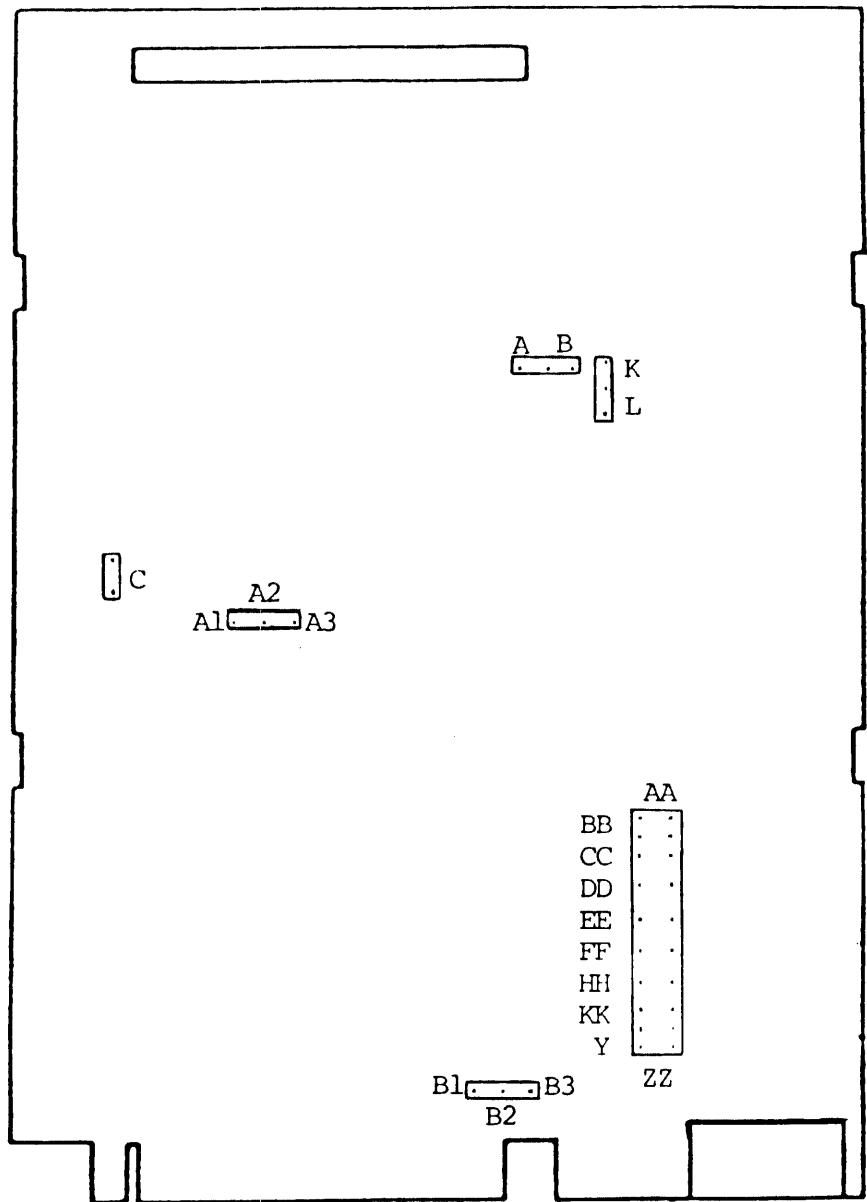


Figure 2-8 SAC PCB Jumper Block Location

Table 2-4 SAC Jumper Descriptions and Configuration

JUMPER	DESCRIPTION	AS-SHIPPED CONFIGURATION
A1, A2, A3 B1, B2, B3 C	* * PLL Gain Adjustment* PLL Feedback for Speed Select: Tape Speed = 30 ips Tape Speed = 90 ips K to Common L to Common	A1 to A2, IN B1 to B2, IN OUT (Customer Request) (Customer Request)
A to Common A to Common	Voltage Selection = $\pm 12V$ Voltage Selection = $\pm 24V$	(Customer Request) (Customer Request)
AA and BB	NOTE: +24V selection requires additional components.	
CC	Unit Selection Format Selection: IN = QIC-24 OUT = QIC-11	Both OUT IN
DD	Speed Definition for uProcessor: IN = 30 ips OUT = 90 ips	(Customer Request)
EE	Interface Parity: IN = Parity Enabled OUT = Parity Disabled NOTE: Presently not supported.	OUT
FF	Loop On Error*	OUT
HH	Test Configuration*	OUT
KK	Power-On Confidence Test*	OUT
Y	Track Selection: IN = 9 Track OUT = 4 Track	(Customer Request)
ZZ	Defines to uProcessor application program that there is an external memory.	IN

*For Archive Use Only

2.2 RECEIVING AND INSPECTION

2.2.1 Unpacking

To unpack the equipment, place the container on a flat stable surface. Remove the equipment from the container. If practical, save the container and packing materials for any future reshipment.

2.2.2 Inspection

Perform a complete visual inspection to assure that there is no physical damage caused during shipment (dents, scratches, broken parts, etc.).

2.2.3 Handling

It is often necessary to transport and handle the equipment after it is unpacked and prior to installation. Industry standard procedures for the handling of electronic equipment are sufficient to ensure the equipment is not subjected to physical shock or damage. Since the unit contains exposed components and assemblies, proper care should be taken to ensure their protection against physical damage and damage caused by electrostatic discharge introduced through handling.

2.3 INSTALLATION

When the tape drive is to be mounted in an enclosure, a number of precautions must be taken to ensure proper operation. Mounting instructions are explained in paragraphs 2.3.1 thru 2.3.2.

2.3.1 Horizontal Mounting

Mount the tape drive unit flat on the user-supplied frame with the tape cartridge slot facing forward (Figure 2-9). Secure the Intelligent drive using all four threaded holes provided in the bottom of the unit. When mounting the Basic unit any three, but only three, of the threaded holes should be used.

2.3.2 Vertical Mounting

Mount the tape drive unit on its right side (Figure 2-10) with the tape cartridge slot facing forward (slide lever at the top).

When installing the Basic tape drive any three, but only three, of the four mounting holes should be used. When the Basic tape drive is to be mounted by its side to the user-supplied frame, all four (two on each side) threaded mounting holes provided in the chassis sides may be used.

When installing the Intelligent tape drive, mounting holes may be selected from the 16 threaded holes (6 on each side and four on the bottom).

The SAC PCB portion of the Intelligent tape drive can be remotely mounted still attached to the Archive supplied chassis by selecting the required mounting holes from the 12 threaded holes provided in the chassis. The SAC PCB can also be remotely mounted using the four holes provided in the PCB.

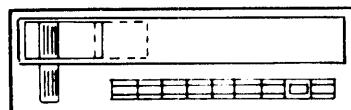


Figure 2-9 Horizontal Mounting Position

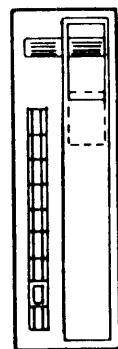


Figure 2-10 Vertical Mounting Position

2.4 OPERATION

The only operator intervention required to operate the Intelligent tape drive is to load the tape cartridge. All other functions are performed under software control from the host CPU.

2.4.1 Cartridge Loading/Unloading

The cartridge is inserted through the loading aperture so that the cartridge protective door is facing the slide lever side of the front panel and enters the drive first. The cartridge is inserted over a full width lip and when fully inserted, descends to be retained by the lip. The front slide lever is then moved toward the cartridge until it reaches the lever stop. This action secures the cartridge and brings the head assembly to its correct operating position. Before inserting the tape cartridge, position the write protect plug as shown in Figure 2-11, to enable or inhibit writing on the tape.

The safe switch is activated or not activated depending upon the write plug orientation. The cartridge-in switch is activated when the cartridge is in place and the slide lever is engaged.

The cartridge is removed by firmly moving the slide lever away from the cartridge until the lever stop is reached. The lever action causes the head assembly to retract away from the cartridge. The same action triggers an ejector which lifts the cartridge clear of the retaining lip and pushes it out of the aperture. The cartridge is completely unloaded by pulling it from the drive.

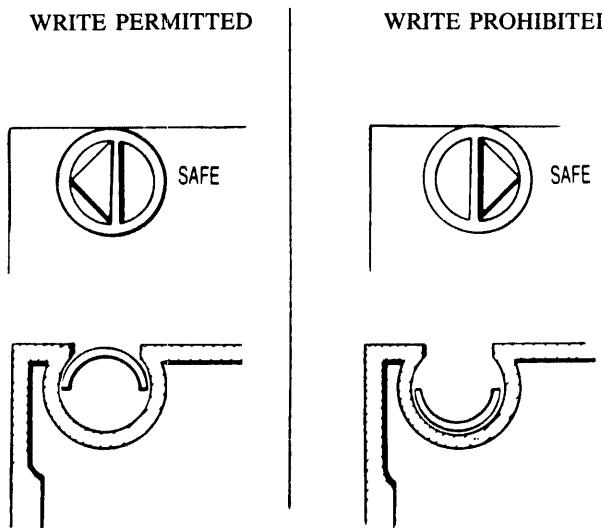


Figure 2-11 Write Protect Plug

2.5 INITIAL TESTS

There are no field adjustments for the tape drive. The adjustments listed in Chapter 6 are shop adjustments requiring special equipment. There are two field checks that are overall performance tests. These are the read test and the write test.

2.5.1 Equipment Required

1. A known good tape with known data written on a Master Drive (see Appendix 1). Number of read errors when tape is read on Master Drive should be known. This tape is used only for read testing.
2. A known good tape to be used for write testing.

2.5.2 Read Test

1. Using the read test tape, read a file from the tape.
2. Check soft error count. If tape was read with a comparable number of errors as were found on the Master Drive, the read channel is acceptable.

2.5.3 Write Test

1. Using the write test tape, write a known data pattern on one track in the forward direction and one track in the reverse direction.
2. Check the soft error count. If the data was written with a comparable number of rewrites as occurred with the Master Drive, then the write channel is acceptable.

2.6 PREVENTIVE MAINTENANCE

Preventive Maintenance consists of cleaning the read/write/erase heads and checking the soft error statistics to determine tape or tape drive deterioration.

2.6.1 Cleaning

Clean the read/write/erase head assembly and the tape hole sensor openings with a clean, lintless cotton swab dampened with a proper head cleaning solution or 95% isopropyl alcohol. Use the following schedule:

1. After an initial pass with a new tape cartridge.
2. If using all new tape cartridges, after every 2 hours of actual use.
3. After every 8 hours of normal use.

The procedure for cleaning the heads is as follows:

1. Ensure that power to the tape drive is off.
2. Move the slide lever to extend the head assembly into the cartridge area.
3. Use a six-inch or longer cotton swab. Move the swab in and out to clean the heads.
4. Take care that excess cleaner is not applied to adjacent parts and that all residue is completely removed prior to inserting the tape cartridge.

2.6.2 Soft Error Statistics

Read or write error statistics are available to the host through the Read Status command. Typically, the Read Status command should be executed after completion of each cartridge used and the statistics reported at least on an exception basis. An increase in the soft error rate normally indicates a deterioration of the recording media. If initializing the cartridge does not reduce the soft errors dramatically, a known good tape should be substituted. If the soft error rate is high on a known good tape, the tape drive is in need of servicing. If the soft write error rate is low on a known good tape, the cartridge with the high soft write error rate should be replaced with a new cartridge.

CHAPTER 3

SYSTEM INTERFACE

3.1 GENERAL

This chapter contains system interface information. Section I contains information explaining the Scorpion Basic drive interface to the controller/formatter. Section II provides interface information concerning communication between the Scorpion Intelligent drive and the host via the QIC-02 interface.

SECTION I

BASIC DRIVE INTERFACE

3.2 BASIC DRIVE INTERFACE

The following paragraphs provide explanation concerning control and data signal lines between the Scorpion Basic tape drive and the controller/formatter. Signal descriptions and interface requirements are also presented.

There are 22 signal lines in use at the Scorpion Basic interface. Fifteen lines are used for signals that come from the controller and 7 are used for signals that originate at the Basic tape drive as seen in Figure 3-1.

The Basic tape drive utilization of input signals to control internal operation and the generation of output signals is enabled upon the assertion of Drive Select (DS0-) from the controller (see paragraph 3.3.1).

The signals are sent via a 50-pin connector. Cable length must not exceed 9 feet 10 inches (3 meters).

Standard TTL levels are used on signal lines to the controller as follows:

- FALSE: Logic 0 (HIGH) = 2.4 to 5.25 VDC
- TRUE: Logic 1 (LOW) = 0 to 0.55 VDC

Standard TTL levels are required on signal lines to the drive as follows:

- FALSE: Logic 0 (HIGH) = 2.0 to 5.25 VDC
- TRUE: Logic 1 (LOW) = 0 to 0.8 VDC

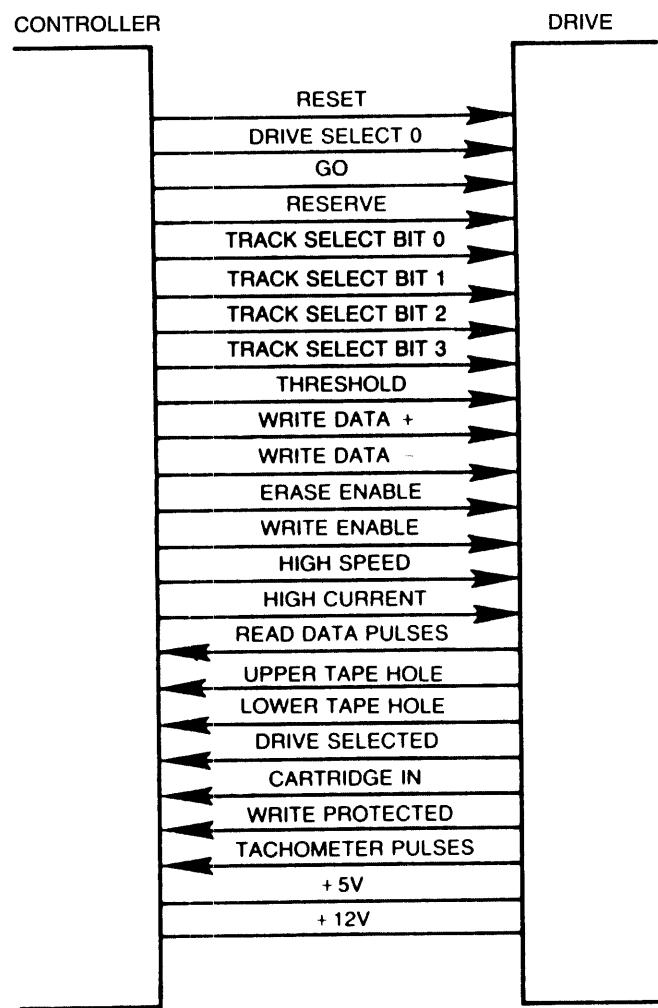


Figure 3-1 Basic Tape Drive Interface

3.3 CONTROLLER GENERATED SIGNALS

3.3.1 Drive Select 0 (DSO-)

The assertion of DSO- will allow Basic tape drive operations under microprocessor control to proceed. Erase and write current will be permitted under interface control, and the output interface signals to the controller will be enabled. The drive selected (SLD-) signal will be generated in the Basic drive and sent to the controller.

3.3.2 Reset (RST-)

Upon receiving a 70 microsecond or longer pulse on the RST-input signal line, the drive performs a 3 second initialization routine. This routine recalibrates the heads to track zero and conditions the drive electronic hardware and firmware to operational readiness on the SAC PCB.

3.3.3 Go (GO-)

Assertion of GO- causes a tape start sequence in the direction specified by the state of REV-. Typical tape motion timing is shown in Figure 3-2.

3.3.4 Reverse (REV-)

Assertion of REV- will cause a motion in the reverse direction if GO- is asserted. See motion timing Figure 3-2.

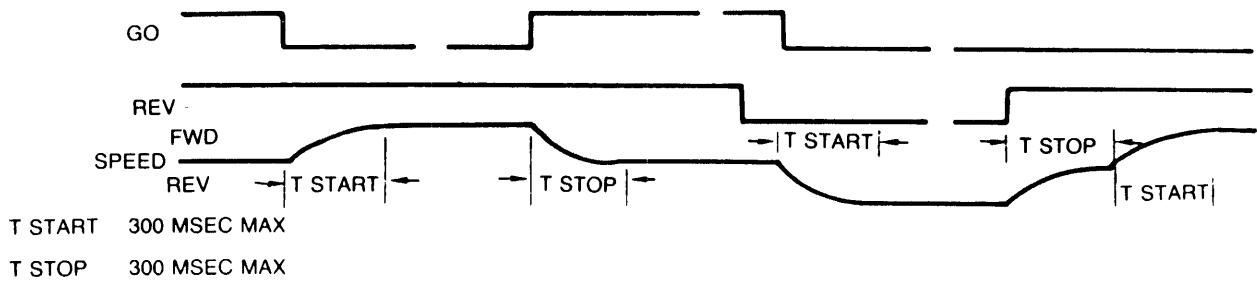


Figure 3-2 GO- and REV- Signals Timing Diagram

3.3.5 Track Select Bits 0, 1, 2 and 3 (TRO-, TR1-, TR2- and TR3-)

Track select bits TR0- and TR1- are used to select one track from tracks 0 thru 3 in four track drives. Track select bits TR0-, TR1-, TR2- and TR3- are used to select one track from tracks 0 thru 8 in nine track drives. The code combinations necessary to select the required track are shown in Table 3-1.

Table 3-1 Code Combinations for Track Selection

BINARY INPUT CODE										
TRACK SELECT	TRACK 0	TRACK 1	TRACK 2	TRACK 3	TRACK 4	TRACK 5	TRACK 6	TRACK 7	TRACK 8	
(LSB) TR0--	0	1	0	1	0	1	0	1	0	
TR1--	0	0	1	1	0	0	1	1	0	
TR2--	0	0	0	0	1	1	1	1	0	
(MSB) TR3--	0	0	0	0	0	0	0	0	1	

3.3.6 Write Data + (WDA +) and Write Data- (WDA-)

WDA+ and WDA- are differential signals sent to the basic interface at standard TTL voltage levels during the time WRITE ENABLE (WEN-) is asserted. The Basic tape drive read/write system is optimized to record GCR data at a nominal density of 10,000 flux transitions per inch (ftpi).

3.3.7 High Current (HC-)

Higher current is used to write data to tape when HC- is asserted from the controller as a result of detecting the insertion of a DC600A tape cartridge into the Basic tape drive.

3.3.8 Erase Enable (EEN-)

If EEN- is asserted and TRO- is false (track zero selected) the entire tape under the erase head will be erased.

3.3.9 Write Enable (WEN-)

The WEN- input must be asserted at the Basic drive interface for write data to be gated to the write head.

3.3.10 High Speed (HS-)

HS- is a signal provided to allow the 5320 Basic drive to move tape at 90 ips when performing tape motion operations which do not require reading or writing to tape such as erase, rewind, retension, and some repositioning routines. See 'Intelligent Drive Interface' Section II for an explanation of these operations.

3.3.11 Threshold (THD-)

When asserted, read threshold invokes a 35% qualifying amplitude threshold for the read signal off tape.

3.4 BASIC TAPE DRIVE GENERATED SIGNALS

3.4.1 Read Data Pulses (RDP-)

Read data is sent to the controller in a serial stream from the interface. Since no read enable is required, RDP- will be present any time data passes under the read head.

3.4.2 Upper Tape Hole (UTH-) and Lower Tape Hole (LTH-)

The UTH- and LTH- are output to the controller indicating specific positions of the tape. The BOT, load point, early warning and EOT holes produce an output code, as shown in Table 3-2, to inform the controller of the tape position.

Table 3-2 Tape Hole Signal Output Code

UTH	LTH	TAPE LOCATION
1	1	Beginning Of Tape — BOT holes nearest recording area just right of tape hole sensor
0	1	End Of Tape — EOT holes nearest recording area just left of tape hole sensor
1	0	Warning Zone — between BOT tape holes and load point hole or between early warning hole and EOT tape holes
0	0	Recording Zone — between load point hole and early warning hole providing that a BOT position or EOT position has occurred since the last cartridge insertion (CIN), otherwise this code means 'tape position unknown'.

3.4.3 Drive Selected (SLD-)

SLD- is enabled as a true output to the controller when the input DSO- is true from the controller at the Basic drive interface.

3.4.4 Cartridge In (CIN-)

CIN- is generated when a tape cartridge is fully inserted actuating the Cartridge In switch. CIN- becomes false when the tape cartridge is removed.

3.4.5 Write Protected (USF-)

USF- is an output that informs the controller whether or not the Basic drive will allow data to be written to tape. Writing will not be allowed if USF- is asserted. If USF- is not asserted, writing will be permitted. The factor that dictates the state of this output is the position of the write protect plug on the cartridge when the cartridge is inserted into the drive. See cartridge loading/unloading, Chapter 2.

3.4.6 Tachometer Pulses (TCH-)

Eight (six for older models) tachometer pulses are generated for each revolution of the capstan motor. During rotation of the capstan motor, these pulses inform the controller when tape is moving and how far it has moved. Each tachometer pulse indicates $145 \pm 3\%$ milli-inches of tape movement.

SECTION II

INTELLIGENT DRIVE INTERFACE

3.5 INTELLIGENT DRIVE INTERFACE

The following paragraphs provide explanation concerning control line signals between the Scorpion Intelligent drive and the host. Descriptions of the commands and data that can be transmitted on the 8-bit bi-directional bus are also provided.

Data commands and status information are transmitted to and from the drive and host via the industry standard QIC-02 interface (Figure 3-3). The QIC-02 interface contains an 8-bit bi-directional data/control bus and the following control lines.

- a. Four control lines from the host.
- b. Four control lines from the drive.

The bus and control signals between Scorpion drive and host are all standard TTL levels (LOW TRUE).

FALSE: Logic 0 (HIGH) = 2.4 to 5.25 VDC

TRUE: Logic 1 (LOW) = 0 to 0.55 VDC

3.6 HOST GENERATED SIGNALS

3.6.1 Request (REQ-)

REQ- is driven by the host to signal to the controller that a command is present on the interface and to handshake the command across the interface. REQ- is also used to handshake the six status bytes from the controller to the host.

3.6.2 Online (ONL-)

ONL- must be true prior to beginning a read or write operation. When ONL- becomes FALSE, the operation is terminated and the cartridge is rewound to BOT. If the drive is in the write mode when ONL- is dropped, a File Mark will also be written prior to rewinding to BOT.

3.6.3 Transfer (XFER-)

XFER- is the data handshake signal from the host. It is used with ACK- from the drive to transfer data across the bi- directional data bus.

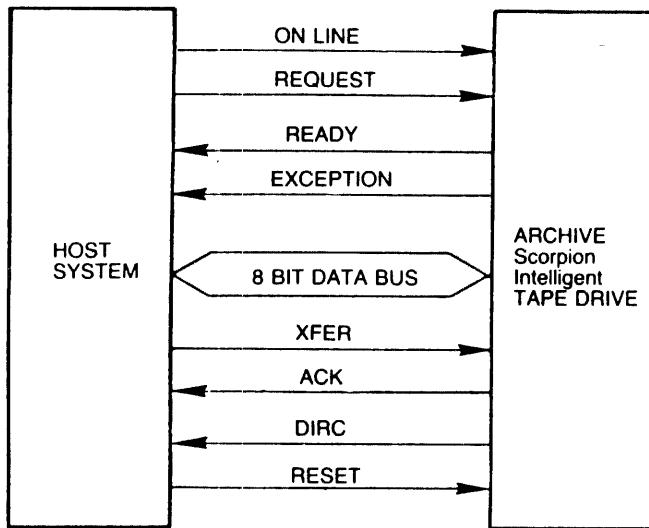


Figure 3-3 QIC-02 Interface

3.6.4 RESET

The RESET line is used to initialize the tape drive. A RESET causes the drive to recalibrate the heads to track zero and to initialize the firmware. If Jumper KK is present on the SAC PCB, a Power-On Confidence test will be run as described in Chapter 7 of this manual.

3.7 DRIVE GENERATED SIGNALS

3.7.1 READY

READY signals that the drive can accept a command and is used to handshake the command across the interface. During a read status operation it is used to handshake status information across the interface to the host. In the write mode READY indicates that a buffer in the drive is ready to be filled by the host. In the read mode READY indicates that a drive buffer is ready to be emptied by the host.

3.7.2 Exception (EXCPT-)

EXCPT- is used to alert the host to a condition which has terminated the execution of a command. The drive sets EXCPT- to signal the termination of an operation. The termination referred to may be a normal completion or an interruption due to an encountered fault (hard errors, write protected cartridges, etc.). The only acceptable response by the host to EXCPT- is to command Read Status. The cause of the Exception condition will be revealed in the drive status.

3.7.3 Acknowledge (ACK-)

ACK- is the data handshake signal from the drive. It is used with XFER- to transfer data across the bi-directional data bus.

3.7.4 Direction (DIRC-)

The state of DIRC- establishes the direction of signal flow before commands, data, or status are placed on the bus. The Intelligent Scorpion drive controls the direction of the bus. DIRC- is available to the host only to enable/disable the host bus drivers.

3.8 DATA BUS

The bi-directional bus lines are used to transfer commands, status, and data between the host system and the Intelligent Scorpion tape drive.

3.8.1 The Command Set

The Scorpion command set is shown in Table 3-3. All Scorpion commands are single byte commands and are QIC-02 compatible.

Table 3-3 Command Summary

BIT 7654 3210		DESCRIPTION
0000	0001	Soft Lock Off
0001	0010	Soft Lock On
0010	0001	BOT
0010	0010	Erase
0010	0100	Initialize Cartridge
0100	0000	Write
0010	0110	Select Q-11 Format*
0010	0111	Select Q-24 Format*
0110	0000	Write File Mark
1000	0000	Read
1010	0000	Read File Mark
1100	0000	Read Status

*Scorpion -2 models only (see Table 1-1).

3.8.2 Soft Lock Off/On

The Soft Lock feature assists the operator in preventing inadvertant cartridge removal by controlling the drive select light. The Select Soft Lock Off command will cause the select light to be on only when the tape is positioned away from BOT. The Select Soft Lock On command will cause the select light to remain on regardless of tape position. In addition, EXCPT- will be asserted when the cartridge is removed while the select light is on.

3.8.3 Select QIC-11 Format

The Select QIC-11 Format command sets the controller to QIC-11 format. This command is legal only at BOT (i.e. it shall not be possible to append in a different format).

3.8.4 Select QIC-24 Format

The Select QIC-24 Format command sets the controller format to QIC-24 format. This command is legal only at BOT (i.e. it shall not be possible to append in a different format).

3.8.5 Motion Commands (BOT, Erase, Initialize Cartridge)

Within the motion command type, there are three operations that can be performed.

1. Rewind the tape cartridge to BOT.
2. Completely erase a tape cartridge.
3. Manually initialize a tape cartridge.

The command to accomplish the first operation is called the BOT command. It will rewind the tape at high speed to BOT.

An Erase command will accomplish the second operation. The entire tape is erased with an erase bar the width of the tape.

To accomplish the third operation an Initialize Cartridge command is issued. This will rewind the tape first to BOT at high speed, then to EOT and back to BOT.

3.8.6 Write

The Write command instructs the drive to write data on the tape. While writing, data formatting and error correction are automatically performed.

The host asserts ONL- and issues the Write command. The READY line is activated when the controller is ready for a data block transfer. When the READY line is active, the host terminates transfer of write data by issuing a Write-File-Mark command. When the READY line is active, the host alternatively terminates transfer of write data by deactivating ONL-. Deactivating ONL- causes a File Mark to be written (if not preceded by a Write-File-Mark command) and the tape is rewound to BOT.

NOTE

A Write command following cartridge insertion or RESET shall commence recording at BOT, otherwise, recording shall commence at the current tape position. If the host starts transfer between blocks before READY is asserted, READY may not be asserted.

When the early warning hole of the last track is detected by the controller, the controller ceases to transfer additional data blocks from the host. The controller terminates the Write command and reports End Of Media (EOM-) by means of an Exception and Read Status.

3.8.7 Write File Mark

A Write File Mark command causes the Scorpion to write a File Mark on the tape. A File Mark may be used to identify the end of recorded data or a division between groups of data. The command may be given to conclude writing or to create a division between the data being written.

3.8.8 Read

The Read command instructs the drive to read data from the tape. During a read operation, error recovery will be automatically performed by the drive. The host asserts ONL- and issues the Read command. If the Read command is issued at BOT, the drive will start tape motion in search of data. When the first block has been read successfully, READY is asserted and data transfers to the host begin. The drive will continue reading and transmitting data to the host until a File Mark is encountered. When the drive reads a File Mark, the Read mode is exited and EXCPT- is asserted with ‘File Mark Detected’ in the status bytes.

If no data is present on the cartridge, the drive will assert EXCPT- and ‘No Data Detected’ will be set in the status bytes.

When READY is asserted, the host may terminate the Read command by deactivating ONL-. Deactivating ONL- during Read also causes the tape to be rewound to BOT. When READY is TRUE, the host may alternatively terminate the Read command by issuing a Read-File-Mark command. If a Read command is issued, the command is accepted and the drive continues reading.

NOTE

A Read command following cartridge insertion or RESET shall commence at BOT, otherwise the Read command commences from the current tape position. If the host starts transfer between blocks before READY is asserted, READY may not be asserted.

3.8.9 Read File Mark

The Read File Mark command allows the user to seek to the end of a file. During a Read File Mark operation, the controller will read the tape, search for a File Mark, but the data will not be transferred to the host. When a File Mark is detected, tape motion is stopped, EXCPT- is asserted, and the host learns that a File Mark was found by commanding Read Status.

3.8.10 Read Status Command

The Read Status command is used to transfer status information from the drive to the host. The status bytes are used to communicate such things as End Of Media, File Mark Detected, Write Protected Cartridge, etc. A Read Status operation may be initiated by the host at the completion of a command. The host must issue a Read Status command if EXCPT- is asserted by the drive.

3.8.11 Status Information

The Scorpion maintains six bytes of status information that are available to the host. The status bytes are requested by a Read Status command. When an Exception condition occurs, the host must perform a read status operation. An Exception condition is defined as any condition which prevents the performance or continuation of a command.

The host, however, is not limited to using the Read Status command only in response to an Exception condition. Within the limits of the interface protocol, the host may request status at any time.

The status bytes contain the following information:

STATUS BYTE 0

- | | |
|-------------|--|
| BIT 0: FIL— | File Mark Detected bit is set when a File Mark is detected during a Read Data or Read File Mark Sequence. The bit is reset by a Read Status Sequence. |
| BIT 1: BNL— | Block-in-error Not Located bit is set when an unrecoverable read error occurs and the controller cannot confirm that the last block transmitted was the block in error. The bit is reset by a Read Status Sequence. |
| BIT 2: UDE— | Unrecoverable Data bit is set when the controller experiences a hard error during read or write operations. The bit is reset by a Read Status Sequence. |
| BIT 3: EOM— | End Of Media bit is set when the logical early warning hole of the last track is detected during a write operation. This bit will remain set as long as the drive is at logical end of media. The EOM bit will not be reset by a Read Status Sequence. |
| BIT 4: WRP— | Write Protected bit is set if the cartridge write protect plug is set in the file protect ‘safe’ position. Operator must change the write protect plug position before the status bit will reset. |
| BIT 5: USL— | Drive Unselected bit is set if the selected drive is not physically connected or is not receiving power. Operator must correct the condition before the status bit will reset. |
| BIT 6: CNI— | Cartridge Not In place bit is set if a cartridge is not fully inserted into the drive. Operator must correct the condition before the status bit will reset. |
| BIT 7: STO— | Status Byte 0 bit is set if any other bit in Status Byte 0 is set. |

STATUS BYTE 1

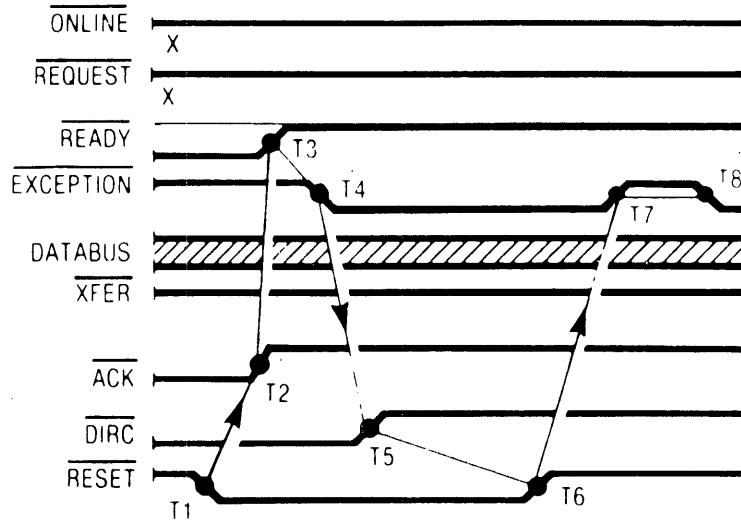
- BIT 0: POR— The Power-On Reset bit is set after the host asserts RESET or when the controller is powered up. The bit is reset by a Read Status Sequence.
- BIT 1: RES— Reserved
- BIT 2: RES— Reserved
- BIT 3: BOM— Beginning Of Media bit is set whenever the cartridge is logically at BOT, track 0. The bit is reset when the tape moves away from BOT. This bit does not set EXCPT- when it goes TRUE, nor is it reset by the Read Status Sequence.
- BIT 4: MBD— Marginal Block Detected bit is set when the controller determines that a data block is marginal. This bit is provided to indicate that eight or more retries were necessary. This bit does not set EXCPT- when it goes TRUE. This bit is reset by a Read Status Sequence.
- BIT 5: NDT— No Data Detected bit is set when an unrecoverable data error occurs due to lack of recorded data. Absence of recorded data is the failure to detect a data block within a controller timeout. This bit is reset by a Read-Status Sequence.
- Bit 6: ILL— Illegal Command bit is set if any of the following occurs. The bit is reset by a Read Status Sequence.
- a. ONL— not asserted when a Write, Write File Mark, Read or Read File Mark command is issued.
 - b. A command other than Write or Write File Mark is issued during the execution of a Write Data Sequence.
 - c. A command other than Read or Read File Mark is issued during the execution of a Read Data Sequence.
 - d. A Select command is issued when the cartridge in the drive is not at BOT, track 0.
 - e. Any unimplemented command is issued.
 - f. A Select Format command is issued when the cartridge in the drive is not at BOT, track 0.
- BIT 7: ST1— Status byte 1 bit is set if any other bit in Status byte 1 is set.

Status bytes 2 and 3 contain the data error counter (DEC) which accumulates the number of blocks rewritten for Write operations and the number of soft read errors during Read operations. These bytes shall be cleared by a Read Status Sequence. Status byte 2 contains the MSB and Status byte 3 contains the LSB.

Status bytes 4 and 5 contain the underrun counter (URC) which accumulates the number of times that streaming was interrupted because the host failed to maintain the minimum through-put rate. These bytes shall be cleared by a Read Status Sequence. Status byte 4 contains the MSB and Status byte 5 contains the LSB.

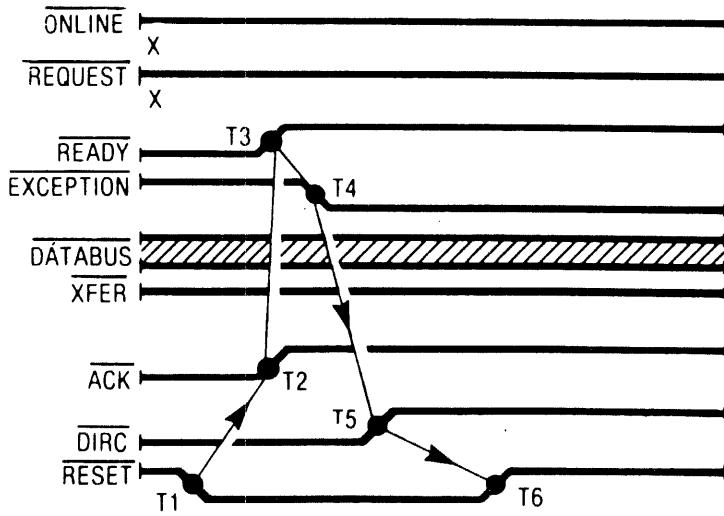
3.9 INTERFACE SIGNAL TIMING

Timing diagrams (Figures 3-4 thru 3-12) are included on the following pages for the reset control signal (with and without POC) and the QIC-02 REV D compatible command set.



ACTIVITY	CRITICAL TIMING
T1-HOST ASSERTS RESET	N/A
T2-CONTROLLER DISABLES ACK	T1-T2<1 U Sec.
T3-CONTROLLER DISABLES READY	T1-T3<1 U Sec.
T4-CONTROLLER ASSERTS EXCEPTION	T1-T4<3 U Sec.
T5-CONTROLLER DISABLES DIRC	T1-T5<3 U Sec.
T6-HOST DISABLES RESET	T1-T6>25 U Sec.
T7-CONTROLLER DISABLES EXCEPTION	T6-T7>0
T8-CONTROLLER ASSERTS EXCEPTION	T7-T8<5 Sec. For POC Pass
X-DON'T CARE	

Figure 3-4 Reset Timing with POC Enabled



ACTIVITY

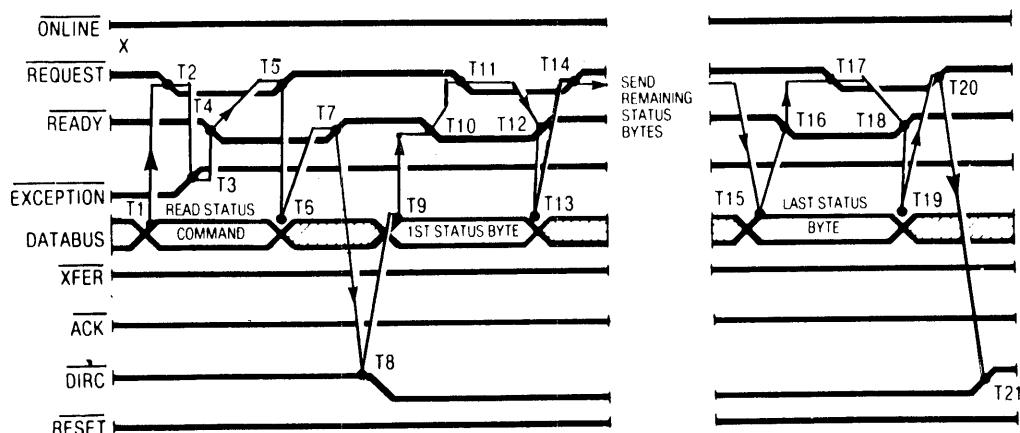
- T1-HOST ASSERTS RESET
- T2-CONTROLLER DISABLES ACK
- T3-CONTROLLER DISABLES READY
- T4-CONTROLLER ASSERTS EXCEPTION
- T5-CONTROLLER DISABLES DIRC
- T6-HOST DISABLES RESET

X-DON'T CARE

CRITICAL TIMING

- N.A.
- $T_1 - T_2 < 1 \text{ U Sec.}$
- $T_1 - T_3 < 1 \text{ U Sec.}$
- $T_1 - T_4 < 3 \text{ U Sec.}$
- $T_1 - T_5 < 3 \text{ U Sec.}$
- $T_1 - T_6 > 25 \text{ U Sec.}$

Figure 3-5 Reset Timing without POC Enabled



ACTIVITY

T1-HOST COMMAND TO BUS
 T2-HOST SETS REQUEST
 T3-CONTROLLER RESETS EXCEPTION
 T4-CONTROLLER SETS READY
 T5-HOST RESETS REQUEST
 T6-BUS DATA INVALID
 T7-CONTROLLER RESETS READY
 T8-CONTROLLER CHANGES BUS DIRECTION
 T9-1ST STATUS BYTE TO BUS
 T10-CONTROLLER SETS READY
 T11-HOST SETS REQUEST
 T12-CONTROLLER RESETS READY
 T13-BUS DATA INVALID
 T14-HOST RESETS REQUEST
 T15-LAST STATUS BYTE TO BUS
 T16-SAME AS T10
 T17-SAME AS T11
 T18-SAME AS T12
 T19-SAME AS T13
 T20-SAME AS T14
 T21-CONTROLLER CHANGES BUS DIRECTION
 T22-CONTROLLER SETS READY
 X-DON T CARE

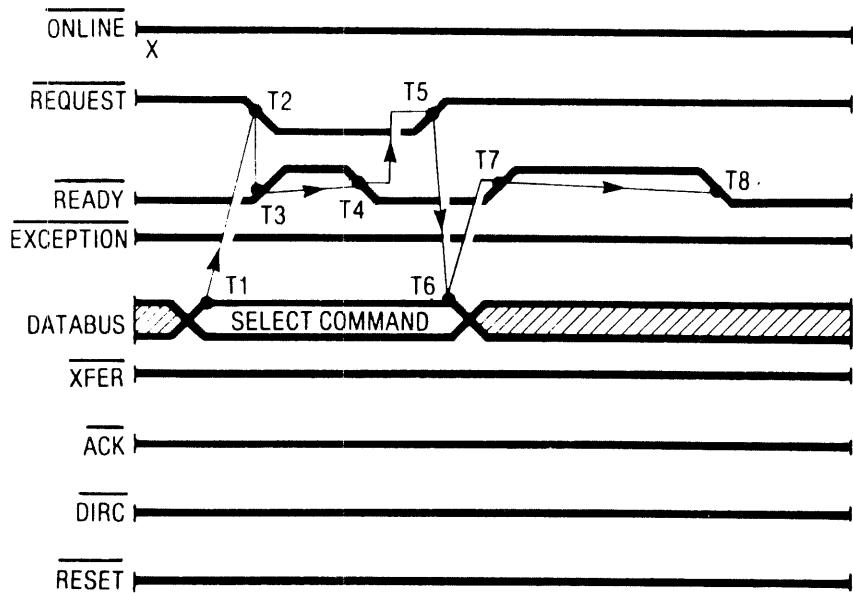
CRITICAL TIMING

N A
 T1-T2 > 0 U Sec
 T3-T4 > 10 U Sec
 20-T2-T4 < 500 U Sec *
 T4-T5 > 0 U Sec
 T4-T6 > 0 U Sec
 20-T5-T7 < 100 U Sec
 N A
 N A
 T7-T10 > 20 U Sec
 N A
 T11-T12 < 1 U Sec
 T11-T13 > 0 U Sec
 T11-T14 > 20 U Sec
 N A
 SAME AS T10
 SAME AS T11
 SAME AS T12
 SAME AS T13
 SAME AS T14
 N A
 T20-T21 ~ 0 U Sec
 T21-T22 ~ 0 U Sec

*NOTE This time may be > 500 M Sec if the following occurs

- a The online signal is deasserted
- b Retry sequence and no data detected
- c At end of the track and turn around or start up

Figure 3-6 Read Status Command Timing Diagram



ACTIVITY

- T1-HOST COMMAND TO BUS
- T2-HOST SETS REQUEST
- T3-CONTROLLER RESETS READY
- T4-CONTROLLER SETS READY
- T5-HOST RESETS REQUEST
- T6-BUS DATA INVALID
- T7-CONTROLLER RESETS READY
- T8-CONTROLLER SETS READY

X-DON'T CARE

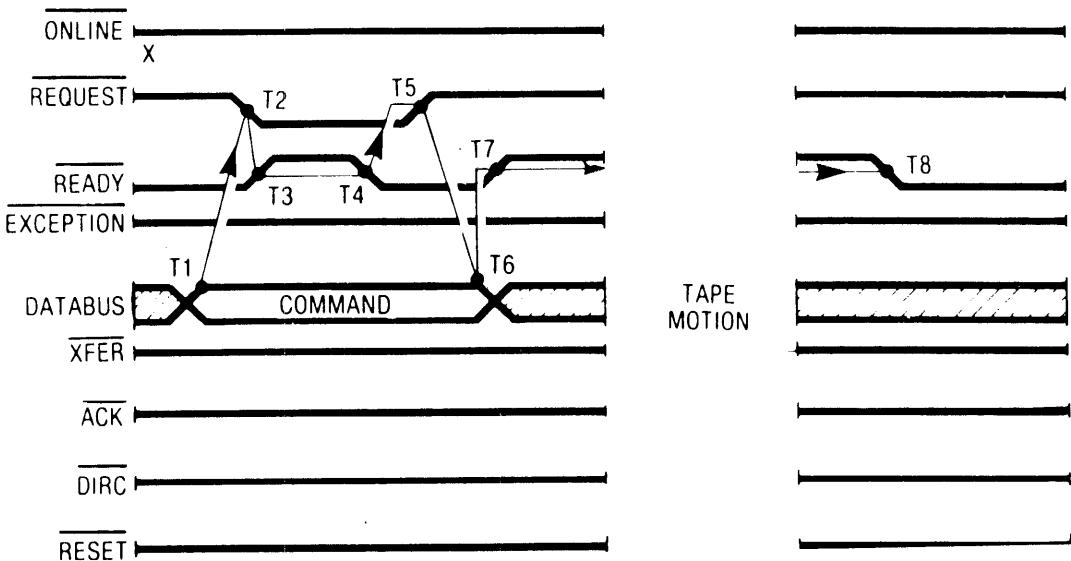
CRITICAL TIMING

- N/A
- $T_1 - T_2 > 0 \text{ U Sec.}$
- $T_2 - T_3 < 1 \text{ U Sec.}$
- $50 < T_3 - T_4 < 500 \text{ U Sec.}^*$
- $T_4 - T_5 > 0 \text{ U Sec.}$
- $T_4 - T_6 > 0 \text{ U Sec.}$
- $20 < T_5 - T_7 < 100 \text{ U Sec.}$
- $T_7 - T_8 > 20 \text{ U Sec.}$

*NOTE: This time may be $> 500 \text{ M Sec.}$ if the following occurs:

- The online signal is deasserted.
- Retry sequence and no data detected.
- At end of the track and turn around or start up.

Figure 3-7 Soft Lock and Select Format Command Timing Diagram



ACTIVITY

T1-HOST BUS DATA VALID
 T2-HOST SETS REQUEST
 T3-CONTROLLER RESETS READY
 T4-CONTROLLER SETS READY
 T5-HOST RESETS REQUEST
 T6-BUS DATA INVALID
 T7-CONTROLLER RESETS READY
 T8-CONTROLLER SETS READY

X-DON'T CARE

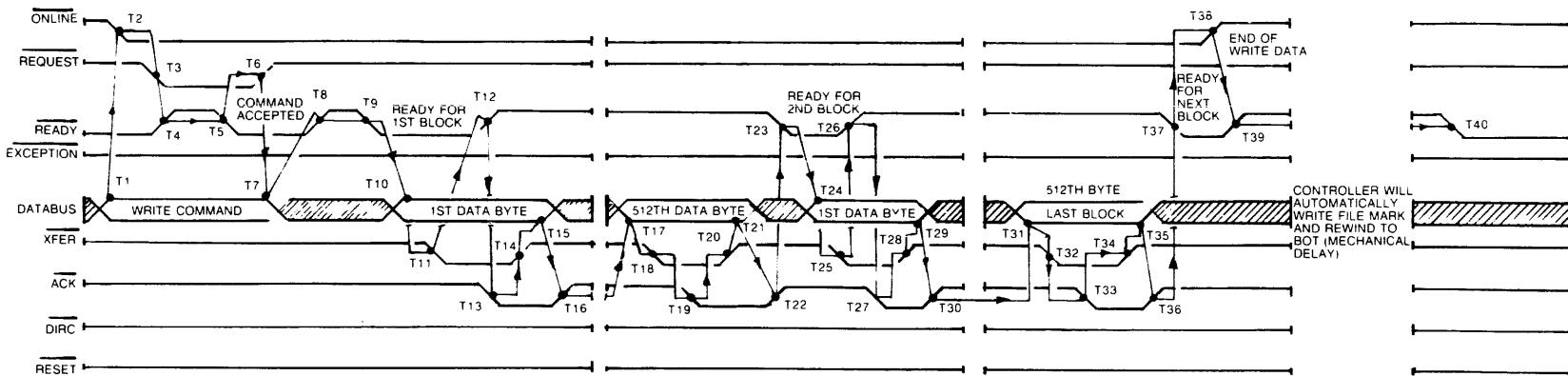
CRITICAL TIMING

N/A
 $T_1 - T_2 > 0 \text{ U Sec.}$
 $T_2 - T_3 < 1 \text{ U Sec.}$
 $20 < T_3 - T_4 < 500 \text{ U Sec.}^*$
 $T_4 - T_5 > 0 \text{ U Sec.}$
 $T_3 - T_6 > 0 \text{ U Sec.}$
 $20 < T_5 - T_7 < 100 \text{ U Sec.}$
 $T_7 - T_8 > 20 \text{ U Sec.}$

*NOTE: This time may be $> 500 \text{ M Sec.}$ if the following occurs:

- a. The online signal is deasserted
- b. Retry sequence and no data detected
- c. At end of the track and turn around or start up

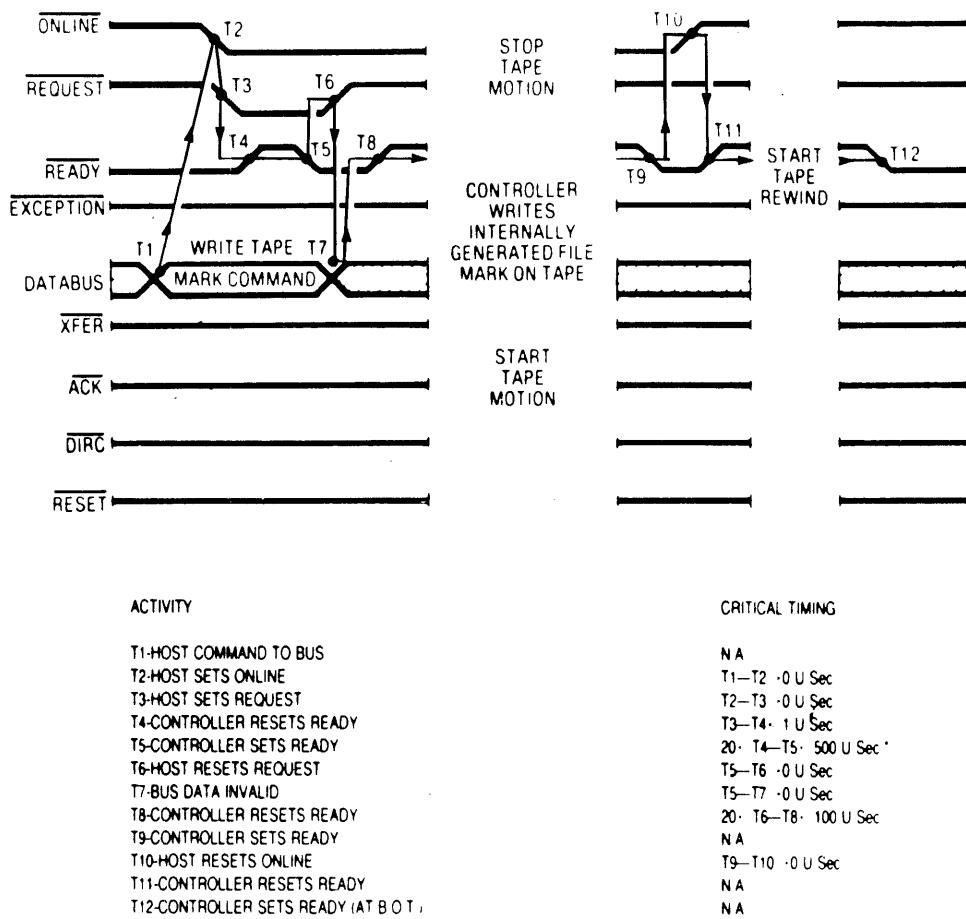
Figure 3-8 BOT, Retension, or Erase Command Timing Diagram

Figure 3-9 Write Data Command Timing Diagram

ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N A	T15-BUS DATA INVALID	T13-T15 > 0 U Sec.	T28-HOST RESETS XFER	SAME AS T14
T2-HOST SETS ONLINE	N A	T16-CONTROLLER RESETS ACK	0 < T14-T16 < 3 U Sec.	T29-BUS DATA INVALID	SAME AS T15
T3-HOST SETS REQUEST	T2-T3 < 0 U Sec.	T17-HOST DATA TO BUS	N A	T30-CONTROLLER RESETS ACK	SAME AS T16
T4-CONTROLLER RESETS READY	T3-T4 < 1 U Sec.	T18-SAME AS T11	SAME AS T11	T31-HOST DATA TO BUS	N A
T5-CONTROLLER SETS READY	20 < T4-T5 < 500 U Sec.*	T19-SAME AS T13	SAME AS T13	T32-HOST SETS XFER	SAME AS T18
T6-HOST RESETS REQUEST	T5-T6 < 0 U Sec.	T20-SAME AS T14	SAME AS T14	T33-CONTROLLER SETS ACK	SAME AS T19
T7-BUS DATA INVALID	T5-T7 > 0 U Sec.	T21-SAME AS T15	SAME AS T15	T34-HOST RESETS XFER	SAME AS T20
T8-CONTROLLER RESETS READY	20 < T6-T8 < 100 U Sec.	T22-SAME AS T16	SAME AS T16	T35-BUS DATA INVALID	N A
T9-CONTROLLER SETS READY	T8-T9 < 20 U Sec.	T23-CONTROLLER SETS READY	T22-T23 > 100 U Sec.	T36-CONTROLLER RESETS ACK	SAME AS T22
T10-HOST DATA TO BUS	N A	T24-HOST DATA TO BUS	N A	T37-CONTROLLER SETS READY	SAME AS T23
T11-HOST SETS XFER	T10-T11 > -40 NANO Sec.	T25-HOST SETS XFER	SAME AS T11	T38-HOST RESETS ONLINE	N A
T12-CONTROLLER RESETS READY	T11-T12 < 1 U Sec.	T26-CONTROLLER RESETS READY	SAME AS T12	T39-CONTROLLER RESETS READY	N A
T13-CONTROLLER SETS ACK	0.5 < T11-T13 < 100 U Sec.	T27-CONTROLLER SETS ACK	SAME AS T13	T40-CONTROLLER SETS READY	N A
T14-HOST RESETS XFER	T13-T14 < 0 U Sec.				

*NOTE: This time may be -500 M Sec. if the following occurs.

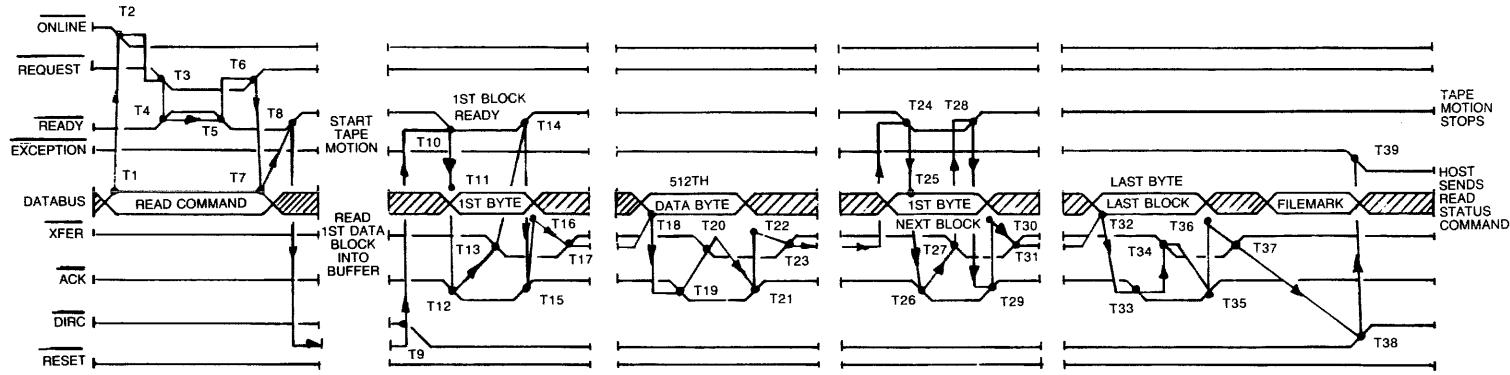
- The online signal is deasserted
- Retry sequence and no data detected
- At end of the track and turn around or start up.



*NOTE This time may be .500 M Sec if the following occurs

- The online signal is deasserted
- Retry sequence and no data detected
- At end of the track and turn around or start up

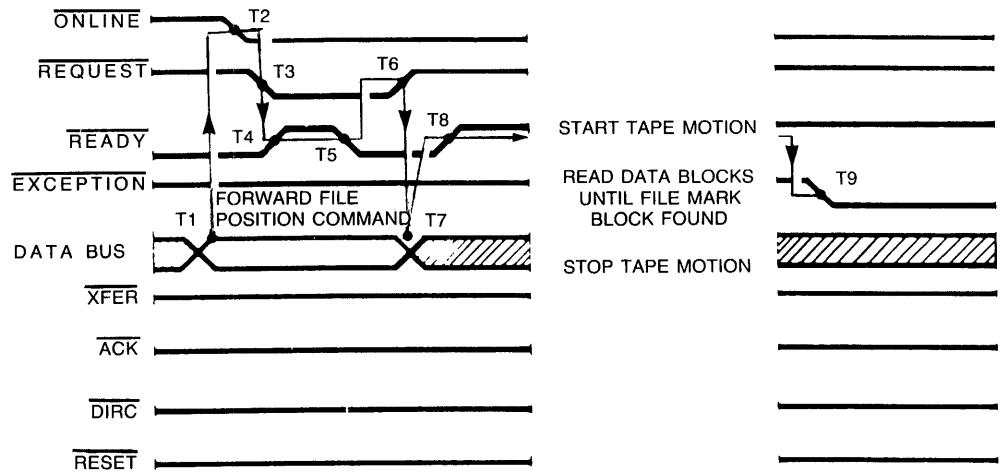
Figure 3-10 Write File Mark Command Timing Diagram

Figure 3-11 Read Data Command Timing Diagram

ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N.A	T14-CONTROLLER RESETS READY	T13-T14<1 U Sec.	T27-HOST SETS XFER	SAME AS T13
T2-HOST SETS ONLINE	N.A	T15-CONTROLLER RESETS ACK	0.5<T13-T15<3 U Sec.	T28-CONTROLLER RESETS READY	SAME AS T14
T3-HOST SETS REQUEST	T2-T3>0 U Sec.	T16-BUS DATA INVALID	T13-T16>0 U Sec.	T29-CONTROLLER RESETS ACK	SAME AS T15
T4-CONTROLLER RESETS READY	T3-T4<1 U Sec.	T17-HOST RESETS XFER	T15-T17>0 U Sec.	T30-BUS DATA INVALID	SAME AS T16
T5-CONTROLLER SETS READY	20<T4-T5<500 U Sec.*	T18-BUS DATA VALID	N/A	T31-HOST RESETS XFER	SAME AS T17
T6-HOST RESETS REQUEST	T5-T6>0 U Sec.	N/A		T32-LAST BYTE TO BUS	N/A
T7-BUS DATA INVALID	T5-T7>0 U Sec.	T19-CONTROLLER SETS ACK	SAME AS T12	T33-CONTROLLER SETS ACK	SAME AS T12
T8-CONTROLLER RESETS READY	20<T6-T8<100 U Sec.	T20-HOST SETS XFER	SAME AS T13	T34-HOST SETS XFER	SAME AS T13
T9-CONTROLLER CHANGES DIRC	N.A	T21-CONTROLLER RESETS ACK	SAME AS T15	T35-CONTROLLER RESETS ACK	SAME AS T15
T10-1ST DATA BYTE TO BUS	N.A	T22-BUS DATA INVALID	SAME AS T16	T36-BUS DATA INVALID	SAME AS T16
T11-CONTROLLER SETS READY	N.A	T23-HOST RESETS XFER	SAME AS T17	T37-HOST RESETS XFER	SAME AS T17
T12-CONTROLLER SETS ACK	T11-T12>70 NANO Sec.	T24-CONTROLLER SETS READY	N.A	T38-CONTROLLER SETS EXCEPTION	N.A
T13-HOST SETS XFER	T12-T13>0 U Sec.	T25-1ST BYTE TO BUS	N.A	T39-CHANGE BUS DIRECTION	N.A
		T26-CONTROLLER SETS ACK	SAME AS T12		

*NOTE: This time may be >500 M Sec. if the following occurs:

- a. The online signal is deasserted
- b. Retry sequence and no data detected
- c. At end of the track or turn around or start up



ACTIVITY

T1-HOST COMMAND TO BUS
 T2-HOST SETS ONLINE
 T3-HOST SETS REQUEST
 T4-CONTROLLER RESETS READY
 T5-CONTROLLER SETS READY
 T6-HOST RESETS REQUEST
 T7-BUS DATA INVALID
 T8-CONTROLLER RESETS READY
 T9-CONTROLLER SETS EXCEPTION

CRITICAL TIMING

N A
 T1-T3 : 0 U Sec
 T2-T3 : 0 U Sec
 T3-T4: 1 U Sec
 20. T4-T5: 500 U Sec **
 T5-T6 : 0 U Sec
 T4-T7 : 0 U Sec
 20. T6-T8: 100 U Sec
 N A

*System must issue read status command

**NOTE This time may be 500 M Sec if the following occurs

- a The online signal is deasserted
- b Retry sequence and no data detected
- c At end of the track and turn around or start up

Figure 3-12 Read File Mark Command Timing Diagram

CHAPTER 4

THEORY OF OPERATION

4.1 OVERVIEW

This chapter contains the general functional theory of operation. Theory of operation is provided for the Scorpion Basic drive and the Scorpion Intelligent drive.

4.2 SCORPION BASIC DRIVE THEORY

The Basic drive consists of the main PCB, motor driver PCB, and the drive mechanism. The Basic drive requires an external controller/formatter for interface with a host computer.

4.2.1 Drive Control

The Basic drive requires +5 VDC and +12 VDC to be supplied from the host. The Basic drive does not have an internal power supply. The clock signals on the main PCB are based upon a 10.74 MHz crystal controlled reference oscillator. The clock is then input to the LSI controller and divided down to 3.58 MHz for application to the microcomputer clock inputs.

Refer to Figure 4-1 during the following control discussion. When power is applied, and in response to reset (RESET-), the head positioning stepper motor is driven to its calibration point and then back to track 0 position. The host must provide write data on dual complementary lines as serial data and also receive read pulse signals on single lines as serial data. Any Intelligent controller must send QIC-36 control signals, listed in Table 2-2, to the Basic drive.

Since the Basic drive writes to or reads from one of four or nine tracks at a time, input track selector signals are required. The track selector signals select the appropriate read and write heads, control head positioning, and control the erase head. The erase head functions only when track 0 is selected and the erase enable input signal is present.

Once a Basic drive has been selected and a track specified (always track 0 initially), a (GO-) signal is required to cause the capstan motor to move the tape in the direction specified by the state of the (REV-) signal. A processed tachometer signal from the capstan is used by the microcomputer to maintain a constant capstan motor rotation at the selected speed. As the capstan motor rotates, the tape is moved past the read/write head, the capstan, and the tape hole sensors.

The tape in the tape cartridge (see Figure 4-2) is normally opaque because of the oxide coating. However, there are a number of precisely located holes near each end of the tape (Figure 4-3). These holes permit light from an LED (light emitting diode) to strike one or both of the light-activated transistors which generate a hole detected signal. These hole detected signals are used by circuits in the Basic drive to control tape motion, writing on the tape, and reading from the tape. Near the beginning of the tape are three pairs of holes. Each pair consists of an upper and lower tape hole located at 18-inch intervals. The Basic drive circuits recognize this hole configuration as Beginning Of Tape (BOT). A single upper tape hole between track 0 and track 1 placed 36 inches (DC300XL tapes) or 48 inches (DC600A tapes) beyond BOT marks the tape load point. Writing starts at this point. Near the other end of the tape are four holes. As the tape moves in the forward direction, the next upper tape hole (between track 0 and 1) is the early warning hole. Writing and reading may continue beyond this hole but will stop before the tape reaches the three End Of Tape (EOT) holes that are 48 inches beyond the early warning hole.

4.2.2 Data Transfer Control

When track 0 is selected and the erase enable signal (EEN-) is true, the erase head is activated and the tape is erased. When the Basic drive is slaved to an Intelligent controller, the tape is erased as track 0 is written. Therefore, normal operation is to erase the tape each time track 0 is written. This ensures that new data will not be written over old data. In order for the write circuits to be activated, the cartridge must not have the file protect cam in the safe position, and the write enable signal (WEN-) must be true (Figure 4-4).

To write data to tape in the Basic drive, a number of conditions must be satisfied. The drive must be selected (DSO-) at the interface, write enable (WEN-) must be active, and the cartridge write protect cam must be positioned to close the unsafe switch (USF). Differential write data (WD+ and WD-) must be available at the input interface. These signals are sent to the drive from the supplied controller.

The read circuits are always operating. The tape is read as it is being written (Read-After-Write) and during read operations. The difference in the use of the read data is left to the Intelligent controller or the host. Within the Basic drive, the read-after-write read data is qualified at the 35 percent threshold to ensure that the tape contains high-quality data. During the read mode, no qualifying threshold is applied. This allows the drive to retrieve data efficiently (Figure 4-5).

4.3 SCORPION INTELLIGENT DRIVE THEORY

The following paragraphs refer to the operation of the Intelligent tape drive. The Intelligent tape drive is a combination of the Stand-Alone Controller (SAC), PCB, and the Scorpion Basic drive.

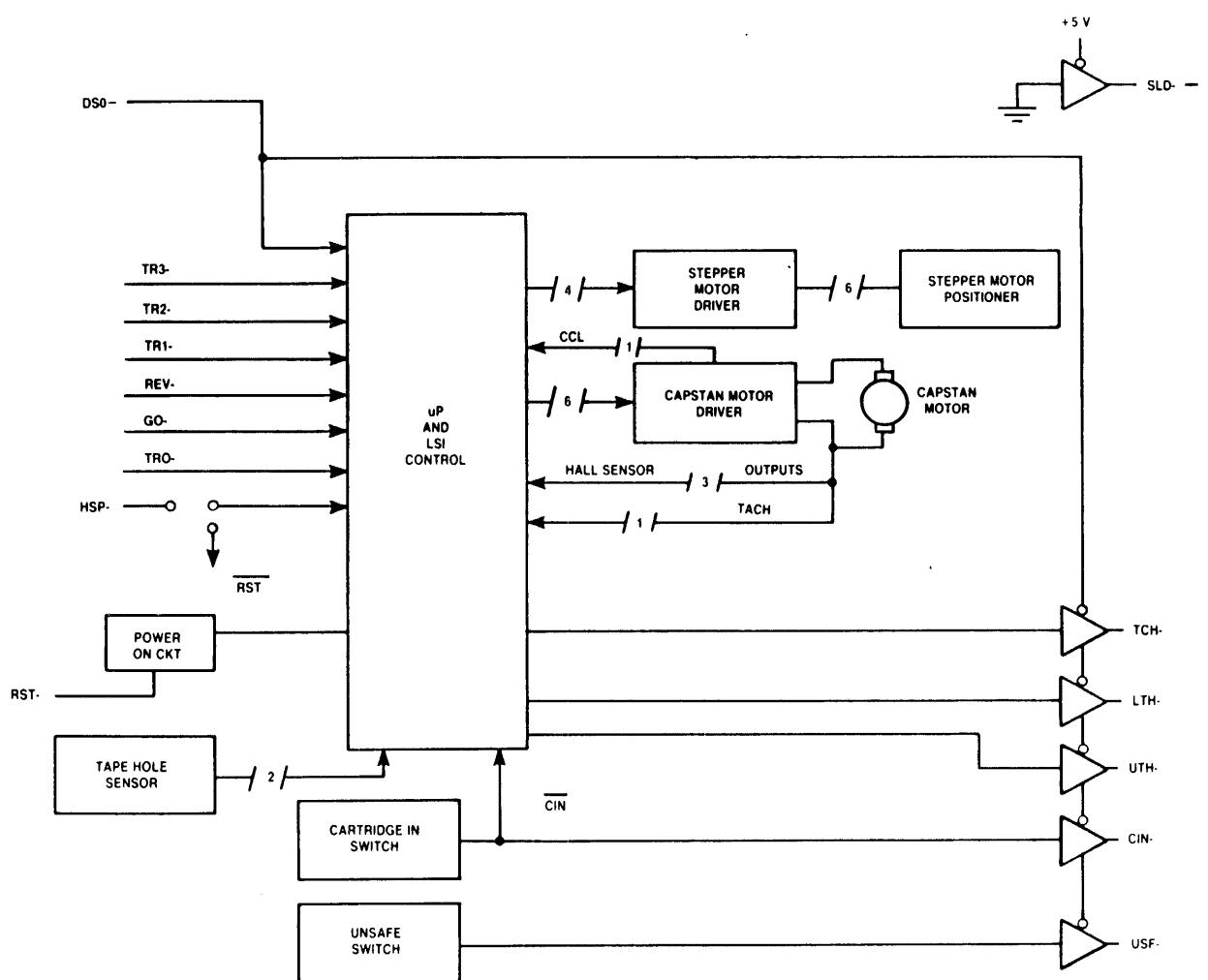


Figure 4-1 Scorpion Control Block Diagram

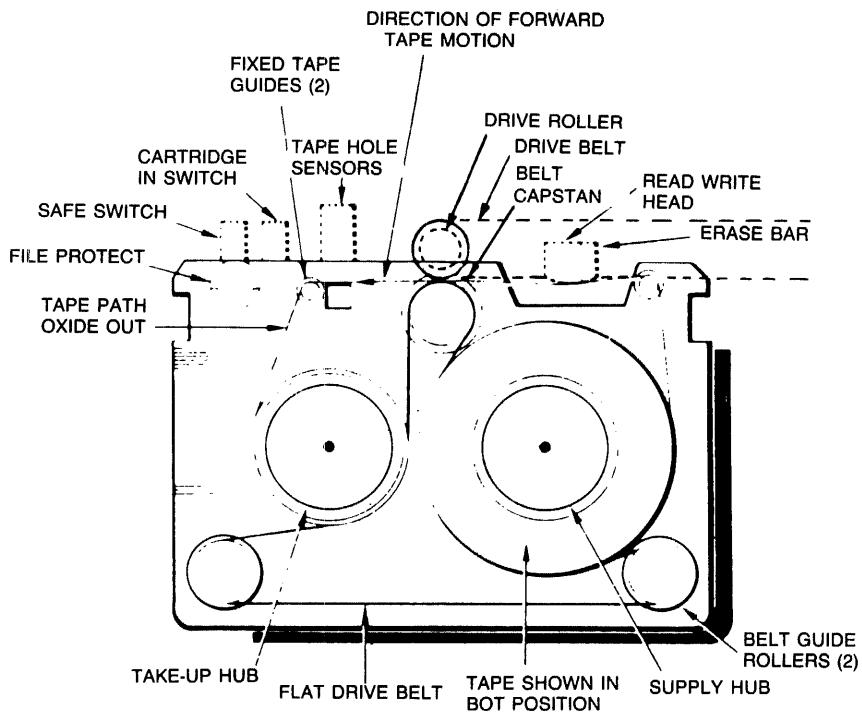


Figure 4-2 Internal View, 1/4-Inch Tape Cartridge

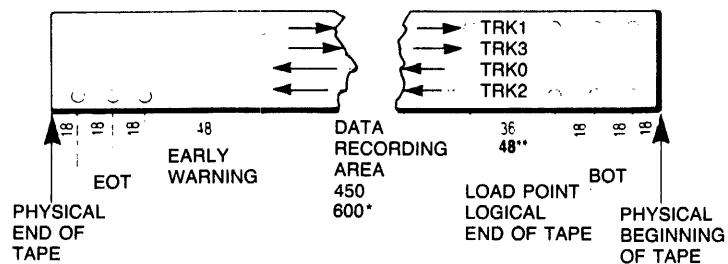


Figure 4-3 1/4-Inch Cartridge Tape Physical Format

4.3.1 Drive Control

Drive selection is accomplished with the SELECT SOFT LOCK OFF or SELECT SOFT LOCK ON command. One unit is selected. Drive 0 is automatically selected following a power-on sequence or a RESET to the drive. SOFT LOCK enables the operator to avoid inadvertent cartridge removal by controlling the drive select light. In the SOFT LOCK OFF state, the drive is selected, and the select light will be on only when the tape cartridge is positioned away from BOT. SOFT LOCK ON will select the drive and provide a soft cartridge lock. Soft cartridge lock means the front panel LED will remain on regardless of tape position. In either soft lock state, cartridge removal while the select light is on will cause EXCPT- to be asserted. In addition, EXCEPTION (EXCPT-) will be asserted when a locked cartridge is removed. Execution of the SELECT command or reset (RESET-) will unlock the cartridge.

Track selection is automatically performed by the drive in such a way as to appear to the host as one long track. Physical track 0 and all even numbered tracks are recorded by the drive in the forward direction. Odd numbered tracks are recorded by the drive in the reverse direction. Read and write operations start at the beginning of tape on track 0 (logical BOT) after cartridge insertion, reset, power on, and following off line sequence. Under all other circumstances, the read and write operations begin where the previous operation finished.

The serpentine recording pattern (Figure 4-6) is created by writing track 0 with the lower pair of heads enabled while moving from BOT to EOT. An erase bar which precedes these heads will do a full tape width erase on the first pass. When the end of tape holes are reached, the lower pair of heads and the erase bar are disabled and the upper pair of heads are enabled, the capstan motor is reversed, and, as the tape moves from EOT to BOT, track 1 is written. When the beginning of tape is reached, tape motion is stopped, the head assembly is stepped to the next track pair location, and the process is repeated until either four or nine tracks are written, depending on the drive type. The track layout of the Scorpion allows the nine track, 45/60MB drive to read tapes written on a four track, 20/26.7MB drive (Figure 4-7).

Commands which will generate a tape positioning operation are BOT, RETENSION, and ERASE. A BOT command will rewind the tape to the BOT holes (Figure 4-3) at the beginning of the tape. A RETENSION command will wind the tape to BOT then EOT and back to BOT. The ERASE command is used to erase the entire tape. This command will cause the drive to rewind the tape to BOT, erase from BOT to EOT, and then rewind the tape to BOT.

4.3.2 Data Transfer Control

Data transfer to and from the tape drive is in 512 byte blocks. The Intelligent drive automatically formats each block as it is written on the tape. The 512 byte data blocks are extracted from the formatted data as it is read from tape and sent to the host. Also, the drive automatically performs all error recovery operations.

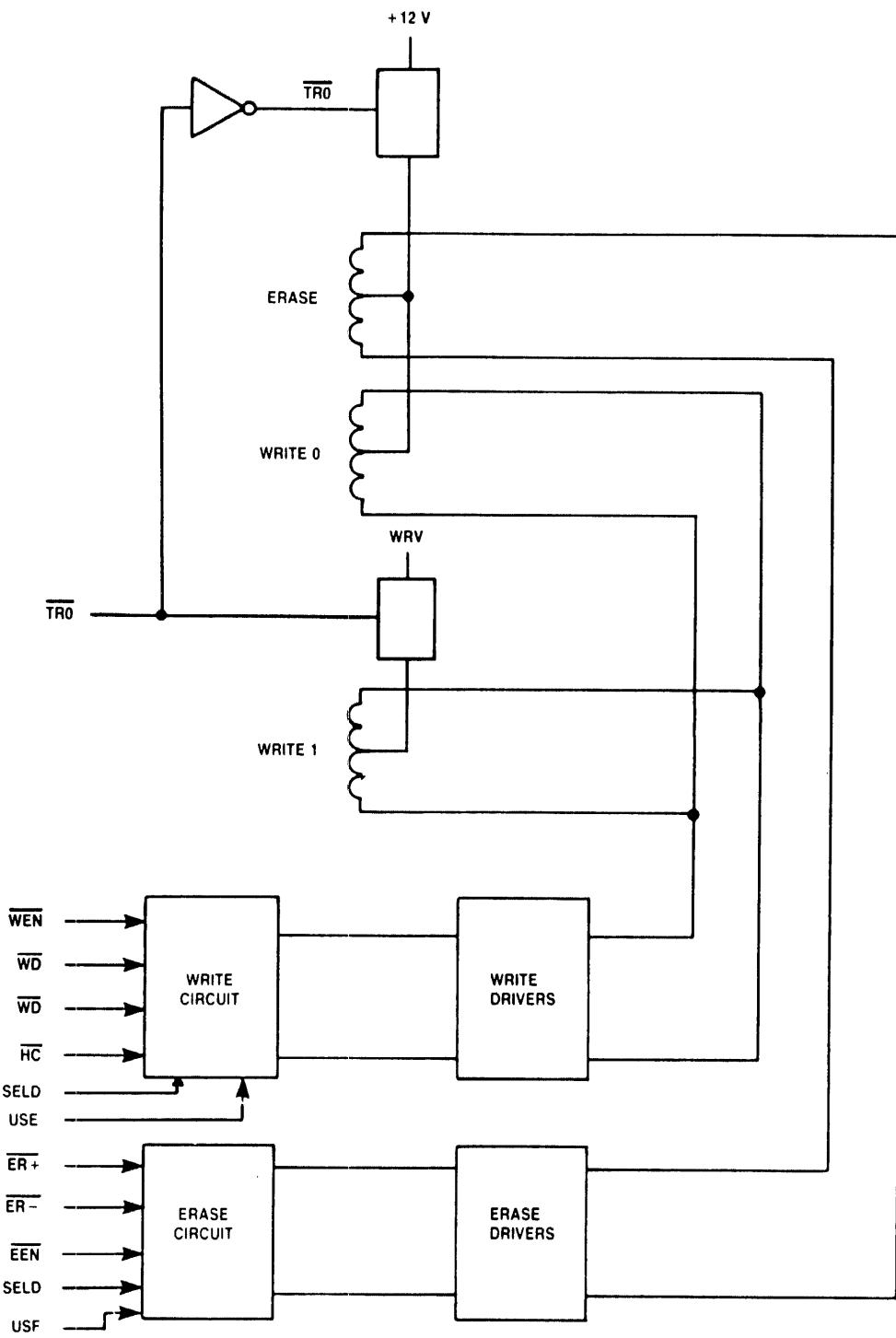


Figure 4-4 Write and Erase Block Diagram

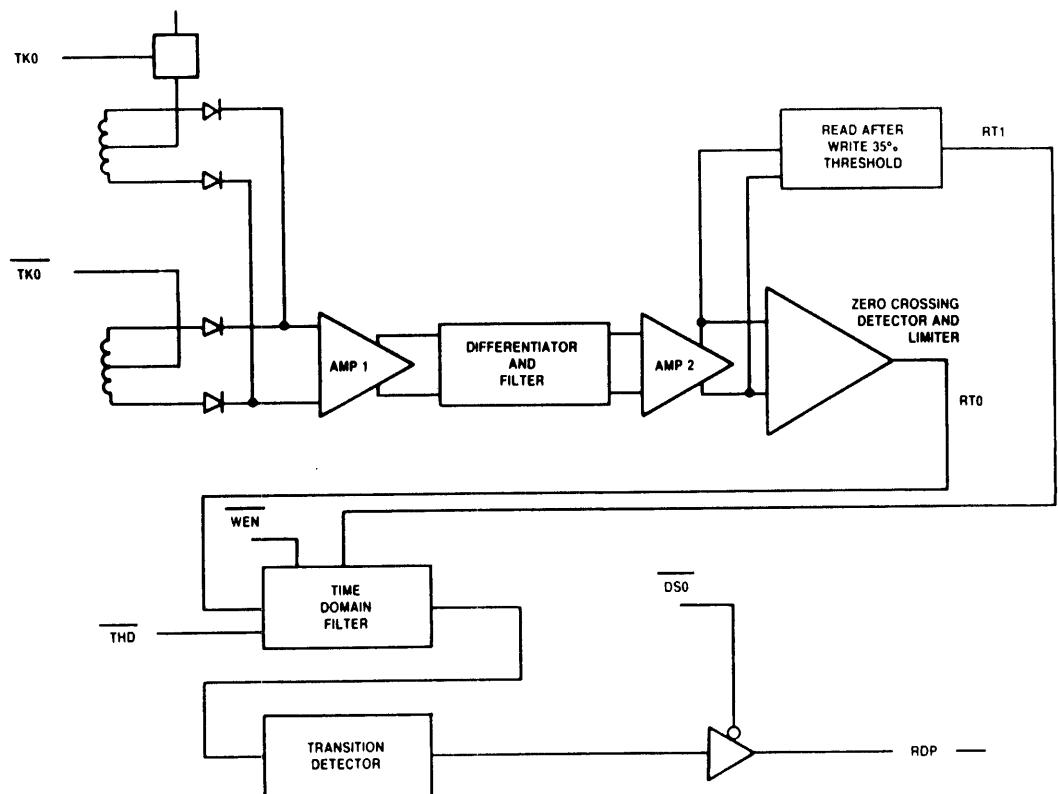
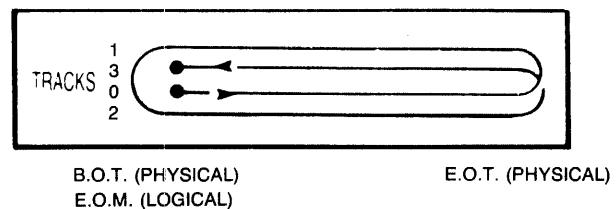
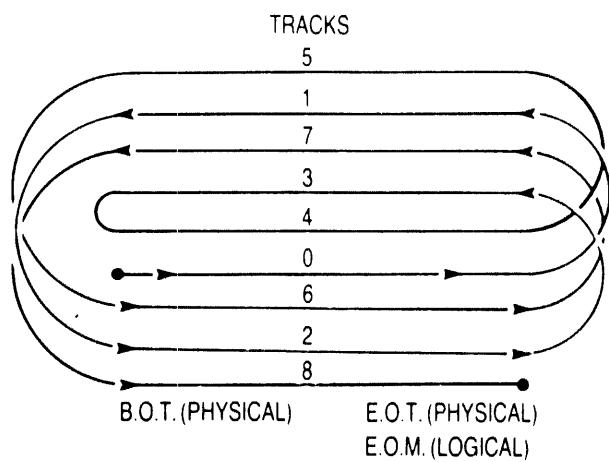


Figure 4-5 Read Block Diagram



A. Four track recording



B. Nine track recording

Figure 4-6 Serpentine Recording

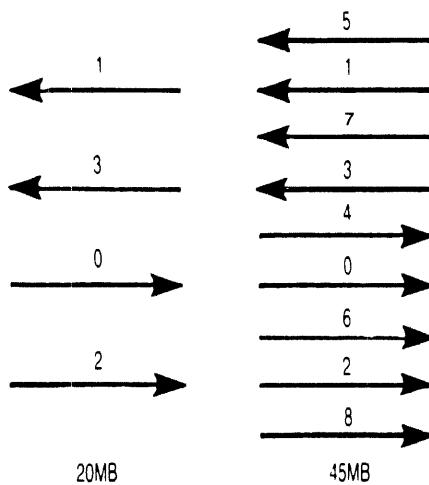


Figure 4-7 Comparative Track Layout

4.3.2.1 Data Transfer Formats

Each formatted block of data is written after the preceding block. A short preamble (12 to 30 bytes) is written at the beginning of each formatted block. The preamble is an all-ones pattern used for read data timing synchronization.

A long preamble (2300 bytes minimum) is written preceding the data block recorded after the load point marker and before the first data block for interchange on all even numbered tracks.

A long preamble (4000 bytes minimum) is recorded before the early warning marker on all odd numbered tracks. A long preamble (300 bytes minimum) is recorded after the early warning mark and before the first data block for interchange on odd tracks.

A long preamble (209 to 722 bytes) will be written when streaming resumes after an underrun or file mark sequence. The preamble will overlap the tail end of a long postamble and then continue until the first data block is dispensed to tape.

The data block marker is one byte and is recorded after the preamble to identify the start of the data block.

The block address is one byte in the QIC-11 tape format or four bytes in the QIC-24 format. The block address uniquely identifies each block in a group of 256 blocks in the QIC-11 format. The block address uniquely identifies each block in a group of 1,048,576 blocks in the QIC-24 format. It is used in error correction and tape positioning. The first block on the tape is block 1. Subsequent blocks are numbered sequentially.

The Cyclic Redundancy Check (CRC) is calculated over the 512 bytes of interchange data and the block address. The postamble is 0.5 to 2 bytes in length. It is recorded after the CRC and is used as a guard band.

A long postamble (364 to 508 bytes) is written after the last block when streaming is terminated by an underrun, file mark, or end of track sequence.

Long postambles and preambles are placed on the tape to compensate for mechanical and electrical properties of the tape or drive, and are invisible to the host.

4.3.2.2 Write Data Description

Each formatted block of data is written immediately after the preceding block. Assuming the proper control signal protocol is in progress, write may be commanded by the host under certain conditions. In any case, the drive will verify if the cartridge is in place and not write protected. If the host has not issued SELECT (SOFT LOCK) or position commands, the drive will default to SELECT (SOFT LOCK OFF) and BOT before writing can begin. One of the conditions under which WRITE can be commanded is a write from BOT. Writing after a BOT operation will always be recorded on track zero. Anytime the drive is recording on track zero, the write data will be preceded by a full tape width erase.

WRITE can also be commanded after writing a file to tape and terminating the file with a file mark. The drive will wait at the file mark vicinity until WRITE is commanded and the first block of new data is supplied. It will begin writing the preamble of the formatted data before the end of the file mark postamble.

Writing may also begin following a read operation (Read Data or Read File Mark). In this case, the drive must find the last file written on tape. The drive is designed to write previously recorded data. The drive will wait in the vicinity of the last data recorded. Write is commanded and data blocks supplied after the last block written on tape.

As the end of each track is detected, the blocks of write data remaining in the buffers are written to tape, and the next blocks of data are written by the other write head on the next track in the sequence.

A file mark is a unique data block created by the drive. The command may be given in one of two ways.

If the user wishes to write a file mark, a WRITE FILE MARK command is issued. The drive will write a file mark, stop tape motion, and exit write mode. The drive will not rewind the cartridge.

When the drive is in the write mode, the user can also write a file mark by simple deasserting ON LINE when READY is true. The drive will automatically write the file mark, exist write mode, and rewind to BOT.

To write in the streaming mode, the tape must be in constant motion. For tape motion to be constant, the flow of data from the host must be sufficient to keep the tape drives' buffers full of data. If data transfers from the host are interrupted, an underrun will occur. If the transfers of data from the host are under 90K bytes per second, the tape will not stop but the drive may, at intervals, write a duplicate of the preceding data block. The duplicate block is transparent to the host. If data from the host falls below 45K bytes per second, the drive will respond by writing a second copy of the last block and then writing an elongated postamble, stopping tape motion, changing direction and positioning back over already written data. When the data transfers resume, the drive will search for the end of the last block and begin writing.

Underruns should be avoided since the second copy of the last block and the elongated preamble both consume tape. The reposition routine also takes some time, reducing throughput.

When a write operation is in process and the early warning hole for the last track is sensed, the drive will stop accepting data from the host at the next block boundary. The drive will finish writing all data blocks contained in the buffers and then raise EXCPT- to the host. In response, the host will read the drive status which will inform the host that the end of media bit has been set.

At this point, the host may command the writing of one block of data or a file mark before the drive reports that the tape is at the end of media again, after which it may again issue the writing of another data block. This block, or blocks, of data may be used to describe the file as incomplete.

4.3.2.3 Read Data Description

When a READ command is given at the beginning of tape, the drive will start tape motion in search of data. When the first block has been successfully read, READY- is asserted and data transfers to the host begin. The drive will continue reading and transmitting data to the host until a file mark is encountered. When the drive reads a file mark, the read mode is exited and EXCPT- is asserted. If no data is present on the cartridge, the drive will assert EXCPT- and ‘No Data Detected’ will be set in the status bytes.

When a file has been read from the tape, the host may continue reading by issuing another Read command. The drive will search for data after the file mark. When the first block has been found, READY- will be asserted and data transfers to the host will begin.

If no data is present beyond the file mark, the drive will assert EXCPT- and ‘No Data Detected’ is reported in the status bytes.

To the tape drive, a READ FILE MARK command is the same as a READ DATA command except that no data is transferred to the host.

The drive reads the tape in search of a file mark. When a file mark is found, EXCPT- is asserted with ‘file mark found’ in the status bytes.

As long as the host can maintain the required data transfer rate, the drive will keep the tape in motion. If something should happen to interrupt the data transfer, the drive will stop tape motion, reverse tape direction, and position over previously read data. This is called a ‘read underrun’. When the host is able to begin transferring data, the drive will start tape motion and continue reading. The repositioning routine generated by the read underruns slow the average throughput.

4.3.2.4 Error Detection Description

As data is written on the tape, a read-after-write check is performed. Error detection is accomplished by a sixteen-bit CRC character which is appended to the data block and written on tape. If a block is found to have an error, it is rewritten without stopping tape motion. Because the read head follows the write head by 0.3”, the block following the block-in-error has already begun to be written. When this block is completed, the block-in-error is rewritten, along with a second iteration of the block following the block-in-error. If this effort is successful, writing continues. The drive will make 16 attempts to write the block-in-error before declaring a hard error. When a hard error occurs, the cartridge is rewound to BOT and EXCPT- with ‘Unrecoverable Data Error’ is detected.

During a Read operation, the drive verifies each block using the 16-bit CRC character. If an error occurs, either CRC or block sequence, the drive will read the next two blocks to see if the block-in-error was rewritten without error. If not, the drive stops the tape, backs up, and tries to read the block-in-error a second time.

The drive will make 16 attempts to re-read a block before declaring a hard error. When a hard error occurs, the drive will stop tape motion, assert EXCPT- with ‘Unrecoverable Data Error’ in the status bytes. After a hard error, the host may continue reading the balance of the tape by issuing a READ command.

Multiple read retries will cause the controller to set bit 4 of status byte one, the marginal block detected bit, in the status bytes if eight or more tries are required before an error is recovered from a block of data.

4.3.2.5 Intelligent Data Control

Intelligent data control refers to intelligent control of the data stream as it is processed by the LSI controller during write and read operations. See circuit description in paragraph 5.4.1.2 in Chapter 5.

CHAPTER 5

CIRCUIT DESCRIPTION

5.1 POWER CIRCUITS

All power to the main PCB, motor driver PCB, and the SAC PCB is supplied from an external (host) source. The main PCB, motor driver PCB, and SAC PCB supply local capacitive filtering for the required +5 VDC and +12 VDC. Refer to Figures A3-1 through A3-3 for distribution and filtering of power circuits.

5.2 CLOCK CIRCUITS

Independent clock and frequency control circuits are found on both the SAC PCB and main PCB. The SAC (see schematic, Figure A3-3) has a crystal controlled 10.74 MHz clock that provides a clock reference to the XTAL 2 input of the microcomputer (6D) and an internal 3.58 MHz CLK. The Voltage Control Oscillator (4B) operates at a center frequency of 28.8 MHz which can be shifted by the Phase Lock Loop (PLL) during read operations to enable data detection (see paragraph 5.4.1.4).

The main PCB (see schematic, Figure A3-1) has a crystal-controlled reference to the LSI controller (U5) at a frequency of 10.74 MHz.

5.3 SCORPION BASIC DRIVE CIRCUIT DESCRIPTION

5.3.1 Stepper Circuits

A head positioning stepper motor and associated control circuit step the head to a number of positions on the tape. This allows four and nine track serial read and write. Refer to Figure A3-1, sheet 2. Positioning of the stepper motor is determined by the output of microcomputer U6 from the track selection inputs TR0-TR3. U6 outputs the commands to U9 and U10 for control of the stepper motor positioning.

5.3.2 Drive and Track Selection Circuits

Refer to Figure A3-1, sheet 2, The Basic drive is selected by asserting the select DS0- (SEL0) input to U6. The assertion of DS0- allows the Basic drive operations under microcomputer U6 control to proceed. The Basic drive outputs a SLD- (SELD) signal indicating the drive has been selected.

Track Selection is controlled by automatically repositioning the head to Track 0 reference position on tape drive reset (RST-). Track selects bits TR0- and TR1- are used to select one track from Tracks 0 thru 3 in four track drives. Track select bits TR0, TR1, TR2-, and TR3- are used to select one track from Tracks 0 thru 8 in nine track drives. The code combinations necessary to select the required track are shown in Table 5-1.

Table 5-1 Code Combinations For Track Selection

TRACK SELECT BIT	BINARY INPUT CODE								
	Track 0	Track 1	Track 2	Track 3	Track 4	Track 5	Track 6	Track 7	Track 8
(LSB) TR0 -	0	1	0	1	0	1	0	1	0
TR1 -	0	0	1	1	0	0	1	1	0
TR2 -	0	0	0	0	1	1	1	1	0
(MSB) TR3 -	0	0	0	0	0	0	0	0	1

5.3.3 Capstan Motor Control Circuits

The capstan motor control circuits are shown at the bottom of Figure A3-1, sheet 2, including U5 and the microcomputer U6. These circuits include the inverter/buffer for the REV- and GO- signals, the tachometer circuits, the hole detector circuits, and the circuits associated with the Write Protect switch, and Cartridge-In-Place switch. REV-(reverse) and GO- (move tape) are routed to the microcomputer. When REV- is HIGH at J1, the tape moves forward; when GO- is HIGH the tape stops. P20, P21, P22, P23, and PROG lines are used to send and receive commands and status between U5 and U6. The state of the REV- signal, therefore, determines the sequence of P and N signals from U5 that will be used to cause forward or reverse motor rotation. The tach signal (U5, T1) is used to determine the change in pulse width which must be applied to the N1-, N2-, and N3- inputs for control of motor speed. The pulse width in the pulse train determines the energy delivered to the capstan motor. As the pulse train becomes wider, more energy is applied to the motor, which then accelerates. As the motor approaches the correct speed, the width of the pulse becomes narrower until the motor stabilizes at the correct speed. As the capstan motor turns, a tachometer signal is generated by the motor. This provides feedback information to 'close' the servo loop.

The upper hole and lower hole photo-transistors, shown in the lower right of sheet 2, Figure A3-1, generate signals UTH and LTH that are used by U5 and microcomputer U6 to identify which portion of the tape is passing the Read/Write heads. The signals from these photo-transistors are input to U5.

U5 contains the control and monitoring circuits for the capstan motor control. Inputs UTH and LTH, TACH, H1, H2, H3, and microcomputer U6 (when processed by U5), produce output signals to the motor driver board. P and N channel motor driver circuits apply current to the brushless motor windings.

5.3.4 Motor Driver Circuits

The motor driver circuits are shown in Figure A3-2. Motor drive power + 12 VDC is supplied through J2-1 and 2. Logic voltage +5 VDC is supplied through J2-3 and 4. Signals for control of the three phase brushless DC motor are fed from the main board LSI controller U5 through J3. These signals are P1, P2, P3, N1, N2, and N3. These signals control the speed and direction of the capstan motor. These signals are turned 'on' in combination and sequence that produce the proper current phase to control the direction of motor rotation. A 14 KHz pulse width modulated signal on N1-, or N2-, or N3- controls the speed of motor rotation. U1, U2, and U3, which drive Q1, Q2, Q3, Q4, Q5, and Q6, are turned on by combinations of P1, P2, P3, N1-, N2-, and N3- to produce current in the motor windings.

5.3.5 Control Circuits

The drive control circuits are shown in Figure A3-1, sheet 2. On power up or assertion of a 70 microsecond or longer pulse on the RST- input signal line, the drive performs a 3 second power-up initialization and recalibration of the stepper motor positioner to recalibrate reference position.

Signals SLD-, TR0-, TR1-, TR2-, TR3-, REV-, GO-, CIN-, UTH-, LTH- are scanned at 1.7 msec intervals. When found by the scan, control functions are performed in the following priority:

1. Track position
2. Tape hole responses
3. Motion control

Signals are scanned by microcomputer U6 at the above rate except while the drive is performing any of the following:

1. Track positioning (500 msec/track)
2. Tape start (300 msec max)
3. Tape stop (300 msec max)

Drive control signals are not responded to unless DS0- is asserted for the drive. De-assertion of DS0- causes a tape stop sequence to occur. When found by the scan, a change in state of TR1, TR2, or TR3- causes a track position sequence to be performed to locate the recording head on the required track. Typical tape motion timing is shown in Figure 5-1. Assertion of GO-, when found by the scan, causes a tape start sequence in the direction specified by the state of REV-. It is permissible to change the state of TR1-, TR2-, or TR3- and REV- while GO- is asserted. Changing the state of TR1-, TR2-, or TR3- while GO- is asserted causes a stop sequence followed by a track position sequence and a start sequence if GO- is still asserted. Changing the state of REV- always causes a stop sequence followed by a start sequence in the opposite direction if GO- is left active. Removal of the cartridge causes a stop sequence to occur. Insertion and loading of the cartridge causes tape motion functions to be performed. Start sequences include protection against over-dissipation of the capstan motor caused by a defective cartridge via limiting the motor duty cycle to 50 msec 'on', 1 second 'off' when stalled.

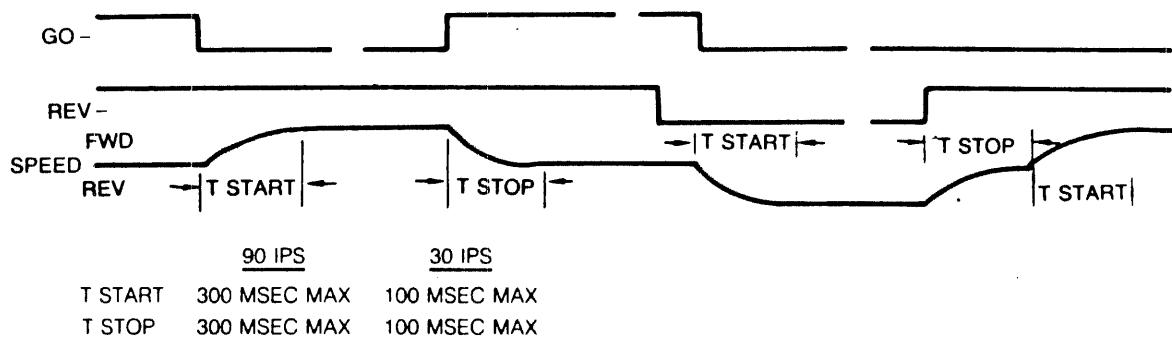


Figure 5-1 Motion Control Timing

Table 5-2 Code Combinations for Tape Hole Detection

UTH-	LTH-	TAPE POSITION
1	1	Beginning of Tape position (BOT holes nearest recording area just right of tape hole sensor).
0	1	End of Tape position (EOT hole nearest recording area just left of tape hole sensor).
1	0	Warning Zone (between BOT tape holes and load point hole or between early warning hole and EOT tape hole).
0	0	Recording Zone (between load point hole and early warning hole providing that a beginning of tape position or end of tape position has occurred since the last cartridge insertion (CIN-), otherwise this code means "tape position unknown").

When a cartridge insertion occurs, the position of the tape within the cartridge is unknown until the tape has been moved to BOT or EOT. It is, therefore, appropriate for the drive to cause a move to one or the other in order to place the tape at a known position. The drive can cause the tape to move to BOT by asserting REV- and GO-. When the BOT holes are seen by the drive, UTH- and LTH- are both asserted (refer to Table 5-2), a tape stop sequence occurs, the drive control lines are scanned for REV (inverse of REV-) and GO-, and, if not found, the tape is moved forward until the BOT holes are again seen and then immediately stopped. UTH- and LTH- will continue to be asserted as long as the drive commands Reverse or there is no tape movement). When FWD- and GO- are found by the scan, the drive asserts the Warning Zone indication prior to initializing the tape start sequence. When the Load Point hole is seen by the drive, Recording Zone is asserted. As forward motion continues, the Early Warning hole crosses the sensors and Warning Zone is asserted.

When the EOT hole is seen by the drive, end of tape position code is asserted, a tape stop sequence occurs, the drive control lines are scanned for REV- and GO-, and, if not found, the tape is moved reverse until the EOT hole is again seen and then immediately stopped. End of tape position code will continue to be asserted as long as the drive commands forward or no tape movement. When REV- and GO- are asserted, the drive asserts the Warning Zone indication prior to initializing the tape start sequence. Further events in the reverse direction are analogous to the description of forward events.

5.3.6 Write and Erase Circuits

The Basic drive Write and Erase channel is shown at the bottom of sheet 1 of Figure A3-1.

The Scorpion write and erase drivers are as shown in Figure 4-4. When enabled (DS0- and WEN- asserted), the write drivers supply current to the selected Write Head. When WDA+ is TRUE and WDA- is FALSE, negative current is supplied. The other two combinations of WDA+ and WDA- are disallowed when writing is enabled. Head selection is controlled by the low order track bit TR0-. Head 0 is connected to +12 V when TR0- is FALSE. Current appropriate for DC600 tape operation is enabled if HC- (High Current) is TRUE, otherwise current appropriate for DC300XL operation is allowed. Head 1 is connected to +12 V when TR0- is TRUE. The write driver is disconnected when the SAFE switch is open or during power up and down of the +5 V. For full protection of written tapes during power up and down, the drive does not activate WEN- or EEN-. The erase head is also connected to +12 V when TR0- is FALSE. The erase driver is enabled when the drive is selected and EEN- is asserted. The 2.7 MHz AC erase signal is internally generated by the drive.

The write hybrid microcircuit U1 contains the circuitry for the write head selection, erase circuit control, and the write function control.

The head select function is implemented by saturated transistors pulling the center-taps of the write/erase or write windings of the head up to the high voltage level. The center-taps of the Head 0 write winding and the Erase winding are tied together and are selected simultaneously. The Head 1 write winding is selected singly. The circuit has as inputs 3 TTL compatible signals to utilize in deciding which head should be selected. The inputs are LOW TRUE. USF and SELD must both be LOW in order to select either head. When TR0 is LOW, Head 1 is selected. When TR0 is HIGH, Head 0 is selected.

The erase circuit is controlled by 3 TTL compatible signals. All are LOW TRUE to command the active state. EEN is the Erase Enable input, it must be LOW or no erasing will occur. ER+ and ER- are the dynamic control inputs, they control the erase current flow. They are 2.7 MHz, 25% duty cycle and 180 degrees out of phase with one another. Assuming that the proper head is selected for erasing through the head select circuit and EEN is LOW, during the time that ER+ is LOW, erase current will sink into 'ERASE a' output through the Erase Head winding and during the time that ER- is LOW the erase current will sink into 'ERASE b' output through the other half of the erase head winding.

The write function is accomplished by two emitter controlled current sources, sinking current from each half of the write winding. The write windings are ORed so that the head-select function can control which head winding is receiving current. The current sources are driven 180 degrees out of phase with one another in a push-pull configuration. The control is done by 4 TTL compatible inputs. The static control is WEN (Write Enable), a LOW TRUE signal to allow the write function. There is a current control input, HC- (High Current), that when LOW, causes the output current sources to go into a HIGH (double the current) mode. When HC- is HIGH, the current source supplies a lower applied current.

5.3.7 Read Circuits

The read hybrid microcircuit U3 contains circuitry for the read head selection, tape head signal amplification, and detection functions. The head select is done by transistor switches, the amplification is done by two amplifiers, and the detection by a dual comparator (see Figure A3-1).

Selection of the Read Head is controlled by TRO-. Read Head 0 is selected when TRO- is not asserted, while Read Head 1 is selected when TRO- is asserted. For READ ONLY operations, the signal from the selected Read Head is amplified, differentiated and filtered, amplified again, and converted to logic level by a comparator and limiter. Transitions occurring less than half a data transition after the previous transition shall be removed by the time domain filter from the read signal. Read pulses (RDP-) are generated at each transition as shown in Figure 5-2. When THD- is TRUE, a 35% of nominal signal amplitude threshold is invoked to eliminate marginal recording areas from the magnetic media. This is used during a READ-AFTER-WRITE operation.

TR0 on U3 is a TTL level compatible input that directs the head selection process to the proper head. A low input allows RD1 CT output to go HIGH to approximately 12 volts, which allows the head isolation which corresponds to RD1 to forward bias and allows the signal from Head 1 to enter the input pins via the head isolation diodes (CR1 and CR2) for the first amplifier RD+ and RD- pins 1 and 2. When TR0 goes HIGH, RD1 CT goes LOW to about 1 volt, RD0 CT goes HIGH, and the signal from Head 0 is directed into the input RD+ and RD-pins of the hybrid. The second amplifier inputs are 12A and 12B. These are available to receive the output of the filter placed between the output of the first amplifier and the input of the second.

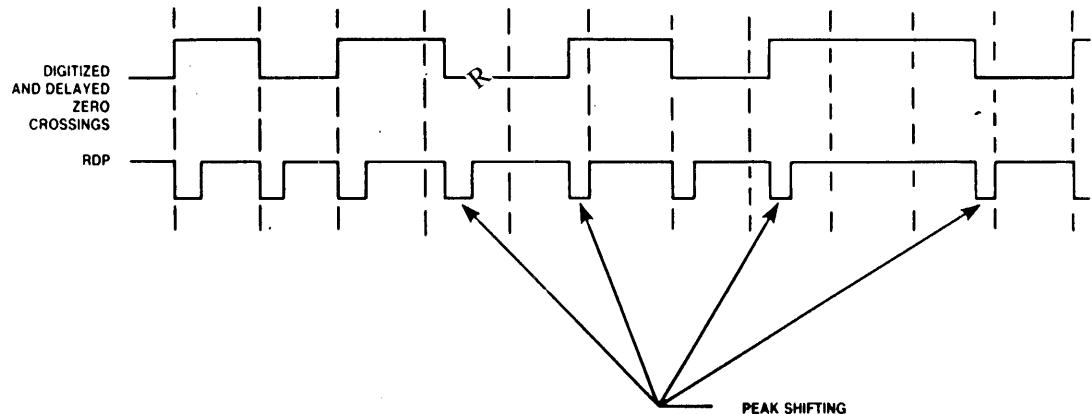


Figure 5-2 Read Signals

The output of the first amplifier is available at O1A and O1B. The gain of this amplifier is controlled by the impedance placed across G1A and G1B, with no additional impedance added between G1A and G1B and at frequencies more than ten times higher than 49 KHz, the gain from the input pins RD+ and RD- to the differential output between pins O1A and O1B. The output O1A and O1B are loaded by an interstage filter used to shape the response off the tape. The outputs are loaded with approximately 2K to ground. The second amplifier has no impedance between its gain inputs G2A and G2B, therefore, gain adjustment is provided by R4 and R5.

Outputs for the head select function are: RD0CT and RD1CT. The voltage levels at these outputs are approximately 12 volts through 4.42K, and approximately 1 volt.

Output RT0 is the output of a voltage comparator that responds to a signal on O2A and O2B with a digital square wave equivalent. There is no threshold, so virtually any signal present will cause switching at RT0. Output RT1 is the output of a voltage comparator that has a threshold of +0.5V or 1V p-p differential measured at outputs O2A and O2B.

5.4 SCORPION INTELLIGENT DRIVE CIRCUIT DESCRIPTION

5.4.1 Stand-Alone Controller Circuits

The controller allows eight-bit parallel transfer of data (Write and Read) from and to the host via the HB0 thru HB7 interface data bus. In addition to the data bus, there are four control signals sent to the host and four control signals required from the host. The host supplies Online (ONL-), Transfer (XFER-), Request (REQ-), and Reset (RESET-) to the controller. The controller supplies Ready (READY-), Acknowledge (ACK-), Direction (DIRC-), and Exception (EXCPT-) to the host. The data bus and the input and output control interface are shown and described in Chapter 3.

All commands from the host, write data from the host, and read data to the host are transferred by the data bus circuits. The data bus circuits are shown on sheet 2 of Figure A3-3. The eight data bits for each byte pass through the input data buffer 3E to the data bus in the LSI controller when DIRC- is LOW enabling 3E. When DIRC- is HIGH, the input data buffer is disconnected from the data bus. When the incoming byte is a command, it is sent to the microcomputer through the LSI controller internal data bus. The microprocessor, using an external crystal oscillator 7A, B, C, acts as the controlling and coordinating device to direct the operations in the LSI controller, and 7D I/O chip. Also, the Phase Locked Loop (PLL) VCO 4B and 16K RAM buffer 1D are used in the read and write process.

5.4.1.1 Microcomputer, 8K PROM, and Static Input/Output Ports Programmable Chip

The microcomputer circuits, Figure A3-3, sheet 1, require a 10.74 MHz crystal clock input at XTAL 2 on the microcomputer. Upon RESET, the microcomputer is initialized and proceeds to address the PROM 4D program. Under program control of the firmware in the PROM, it enables the LSI controller read/write operations, and the output ports (PA1-PA7, PC0-PC3) of 7D to control the Basic tape drive.

5.4.1.2 LSI Controller

The block diagram of the LSI controller is shown in Figure 5-3. The uP interface control block controls the interface signals between the microprocessor and the LSI controller chip. The status and control block controls internal functions and stores status regarding those functions. When the data bus input to the LSI controller is write data, it is sent to the host sequencer. Data flows from the host sequencer to the RAM buffer control in serial form. Under direction of the RAM buffer control, this serial data proceeds out of the LSI controller as a RAMIN data.

The RAMIN data is then stored in the 16K RAM buffer. From the RAM buffer, data goes back to the LSI controller as RAMOUT data where it is processed by the write sequencer. From the write sequencer (WDA, WDA-), it is sent to be written on tape.

During the read mode, read data is taken from the tape and sent to the read sequencer in the LSI controller where it is retrieved from the formatted data stream and stored in the 16K RAM buffer in blocks of 512 bytes of data. From the 16K RAM buffer, the data RAMOUT goes to the host sequencer where it is converted from serial to parallel bytes of data and placed on the 8-bit bi-directional host bus HB0-HB7.

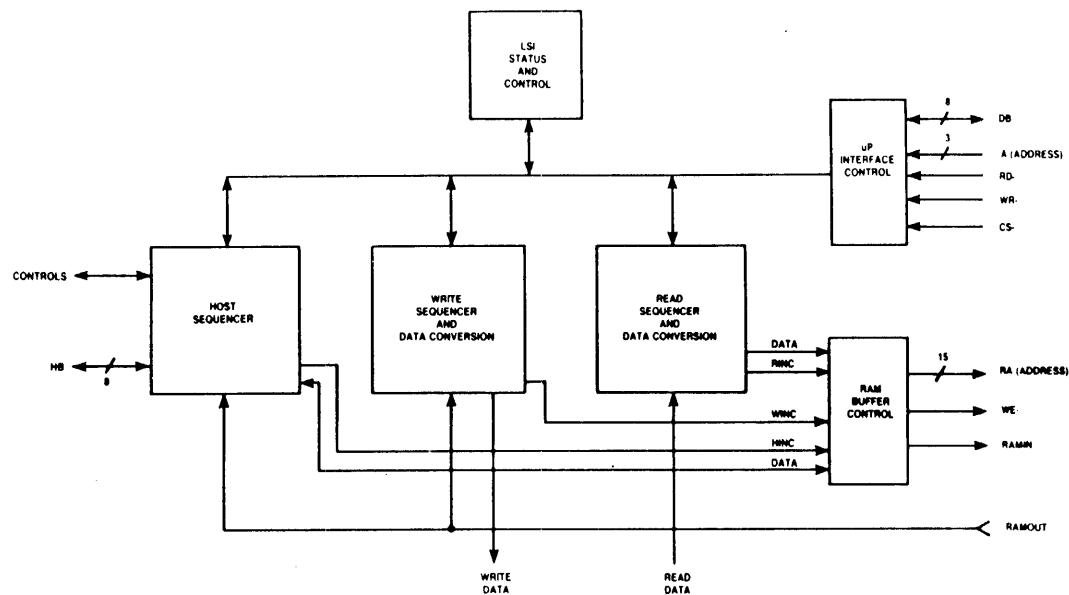


Figure 5-3 LSI Controller Block Diagram

5.4.1.2.1 Host Sequencer Circuits

The host sequencer controls the flow of read or write data to and from the host. The direction of data flow in the sequencer is dictated by control signal CIR. CIR is FALSE when the sequencer is processing write data and TRUE when the sequencer is processing read data. In the write data mode, the sequencer converts parallel bytes of write data into a bit serial stream which it sends to the RAM buffer control. In the read data mode, the sequencer converts a bit serial stream of data from the 16K RAM buffer to parallel bytes of data. This data is placed on the host bus as read data to the host computer. The sequencer is started by a control byte in the LSI controller that comes from the microcomputer on the data bus DB0-DB7. Once directed to start by the computer, the host sequencer will independently process a 512-byte block of data. During a read or write transfer, the host sequencer cycles through logic states until all 512 bytes have been transferred.

5.4.1.2.2 Read Sequencer Circuits

Key circuits which contribute to the operation of the read sequencer are the gap detect and no data detected circuits in the LSI controller, and the phase locked loop circuits outside the LSI controller.

The gap detect and no data detected circuits monitor all read data entering the LSI controller for all ones data pattern (gap), or no data. When a gap is detected, a logic signal is generated and sent to the read sequencer which starts the read sequencer. If twelve-bit cell times occur with no data transition, the no data detected circuit returns the read sequencer to an idle state.

The read sequencer controls the read data from the tape. The clock supplied to the LSI controller sequencer follows the actual frequency of data as it is read from the tape. The source of this clock is the phase lock loop. The read sequencer remains in the idle state until a gap is detected. When the read sequencer is at idle, the phase lock loop will be synchronized in phase and frequency to the write clock. The write clock is the normal frequency at which the read logic expects to see the data. By synchronizing to this frequency, the phase locked loop will be close to the correct frequency when the actual data enters the circuit. When gap is detected, the sequencer goes to read lock state, causing the phase locked loop to synchronize to the all ones gap signal off tape for frequency and phase. Now that the read sequencer has detected gap, and the VCO has locked to the read data, the read sequencer looks for a data block marker (sync byte). Once the data block has been found, the read sequencer will count the 512-byte record. Once 512 bytes have been counted, the read sequencer allows the block address to be checked by the microcomputer. During the processing of data by the read sequencer, the data is converted from 5-bit run length limited (RLL) code to 4-bit HEX code. The decoded data then will be loaded into the shift register, converted to bit-serial form, and sent to the RAM buffers through the RAM buffer control. A Cyclic Redundancy Check (CRC) is performed on all data being read, to determine if any errors are in the data.

5.4.1.2.3 Write Sequencer Circuits

The write sequencer is controlled by the microcomputer and takes data out of the RAM buffers 1D. The write sequencer data is handled in a bit-serial stream and the write sequencer converts 4-bit nibbles to 5-bit encoded data. The controller uses a 4-to-5 code to limit the number of consecutive zeroes in a data stream. In the encoded form, bytes are 10 bits long and nibbles are 5 bits long. Both forms of data must be handled in synchronization with each other. When gap write is enabled by the microcomputer, gap is written from BOT to the Load Point. The write sequencer is also in the gap write state when Write is not enabled. The write sequencer is started by a command from the microprocessor. When the tape comes to speed, the microcomputer begins looking for the Load Point. When the Load Point is detected, the write sequencer goes to the sync write state. Data then begins to flow from the buffers. The write sequencer will stay in the data write state or file mark write state until 512 bytes of data is moved out of the buffers. The block address is then supplied by the microcomputer and placed after the 512-byte block of data.

A CRC character is generated on the data and the block address as the data leaves the buffers and is written at the end of the block address. The data is converted from a four-bit code to a five-bit code by the data conversion (shift register) circuit before it is written to tape. Also, gap is written between blocks of data and between the Early Warning hole and EOT.

5.4.1.2.4 RAM Buffer Control

Each buffer stores 512 bytes (4096 bits) of data which can become a block of data on the tape or a block of data sent to the host. At the beginning of each block transfer, either into or out of a buffer, the buffer address counter is zeroed. The counter is incremented during loading of data from the host, on a write operation, and during the loading of data from the tape on a read operation.

During the write operation, the serial write data is shifted out by the host sequencer, and routed to the RAM buffer control. The RAM buffer control for the block of data being loaded is enabled by the microcomputer. The data is strobed into the selected RAM, advances the address counter, and each bit is loaded sequentially. When one buffer is full, the next buffer is enabled and loaded. After a buffer memory is filled, it is ready to be written to tape. The buffer is unloaded by resetting its address counter and enabling the appropriate RAM buffer control. As the counter counts up from zero, the output bit from each memory location is transferred out as write data into the write sequencer.

During the read operations, the serial read data is routed from the read sequencer to the appropriate buffer. The buffer memory address counters are advanced after each bit is input to the RAM. Each block on the tape fills a buffer. After a buffer is filled, the CRC check is made and the filling of the next buffer is started. A successful CRC check permits transferring the buffer contents to the host. The next buffer is enabled and that buffer's address counter is reset allowing the next block of data to be incrementally transferred.

5.4.1.3 Buffer Memory Circuits

The 16K RAM 1D is divided into four buffer memories and is used in both read and write operations. The input (RAMIN) and output (RAMOUT) data used during these operations is controlled by RA00 thru RA13 and WE- from the RAM buffer control in the LSI chip.

5.4.1.4 Phase Locked Loop and Data Separator (SAC)

When data is read from magnetic tape moving across a read head, even a signal which was written at constant frequency will vary in frequency as it is read. This is due primarily to tape motor speed instantaneous velocity changes. When NRZ data is read from tape, it is necessary to identify where data bits should be. To do this, a bit cell window is needed. This window must be able to shift to some degree to follow the variation in tape speed and data frequency. The circuit which will produce a clock to define a bit cell window is the Phase Locked Loop (PLL). The PLL will track the frequency of data as it is read from the tape and identify where the next bit should be. In the PLL, two different comparison circuits are used.

The first comparison circuit, Figure A3-3, sheet 3, is for synchronization to the write clock so that the read clock will be near the frequency of read data gap when the drive is switched to the Read mode. When synchronizing to the write clock, a phase and frequency comparison is made. The REF- signal (write clock) is compared (phase and frequency) at 6B to the phase and frequency of the read signal clock that the PLL produces. If the PLL signal is faster than the input data (REF-), a signal from 6B controlled by phase and frequency of the data will go into filter 3C through the ladder circuit. The output of filter 3C will cause the control voltage FRQ CONT of the voltage controlled oscillator (VCO) 4B to be lowered. The VCO produces a VCO1- or VCO2- signal whose frequency can be increased or decreased by increasing or decreasing the FRQ CONT voltage. The VCO1- signal is used with a 30 ips drive and the VCO2- signal is used with a 90 ips drive.

The VCO signal is divided by 3B and becomes the READ CLOCK produced by the PLL. The clock is constantly compared to the write clock and is adjusted to match it. If the PLL is slower than the input REF- (write clock), a signal is generated to speed up the VCO.

The second comparison circuit synchronizes to the read data stream with a circuit that is used to track where the ones are in relation to where they should be. If they are early, the VCO speeds up, if they are late, the VCO slows down. The REF- line to 6B consists of write clock until gap is detected. Once gap is detected, the LSI controller switches the read data stream onto the REF- line. After the VCO has been adjusted to the correct frequency during gap, the read sequencer causes lock to turn off the output of the first comparison circuit and turns 'on' the output of the second comparison circuit. The second comparison circuit, Figure A3- 3, sheet 2, generates a digital signal (using counter 3B and latch 2B) which is converted to a voltage across ladder circuit LADO-LAD4 and applied to filter 3C.

The data separator, Figure A3-3, sheet 3, consists of 7A, 2A, 5B, and 3A. The data separator separates ones and zeroes from the data stream and sends them to the LSI controller. The pulses from the output of 4A are gated through 5B where they preset the first 3A latch. Each data one pulse will set the latch for one bit-cell time. The bit-cell time is defined by the read clock pulse. The clock is delayed by 7A and input to the first 3A latch. If a data pulse does not occur during a bit-cell time (data zero), the low input at the 3A latch will be clocked through. The output of the first 3A latch is shifted to the second 3A latch on the next READ CLOCK. When MARGIN (the set input to 2A) is HIGH, inputs from the counter circuit are allowed to control the output of 2A, producing an input to 5B which limits the bit-cell window to the center 75 percent.

CHAPTER 6

REPAIR PROCEDURES

6.1 SCOPE

The repair procedures in this section include general precautions, removal and replacement procedures, and retest requirements.

6.2 GENERAL PRECAUTIONS

Before any procedure is performed, ensure power is removed from the drive. Dirt within the drive mechanism, particularly oxide dust from the tape, degrades the operation of the Basic drive. In all cases, when a Basic drive has been removed from service for repair, the read/write head should be thoroughly cleaned using a lintless cotton swab saturated with 95% isopropyl alcohol. The holes in the hole sensor block should be carefully cleaned. All foreign material in the drive should be removed using a vacuum and a soft bristle brush.

6.3 REQUIRED TOOLS

Required hand tools are listed in Chapter 1, paragraph 1.5. These tools are also called out where used.

6.4 REMOVAL AND REPLACEMENT

It is recommended that repair of the Scorpion Basic tape drive be limited to replacement of the main PCB, motor driver PCB, and the drive belt. Repair of the Scorpion Intelligent tape drive will include SAC PCB replacement. Repairs beyond this level should be referred to factory service representatives. Refer to Appendix II for part locations described in the following procedures.

6.4.1 Main PCB Removal (Figure A2-1)

1. Remove two Allen head screws (using 2 1/2-mm Allen wrench) and two Phillips head screws securing main PCB to frame.
2. Carefully disengage pins of J3 from motor driver PCB.
3. Disconnect all cables.
4. Carefully remove main PCB and place it in a protective bag or box.
5. Retain the securing hardware.

6.4.2 Main PCB Replacement (Figure A2-1)

1. Ensure that cables are routed for easy reconnection.
2. Reconnect cables to board.
3. Gently lay replacement main PCB on frame, being sure to carefully mate pins J3 to holes in motor driver PCB.
4. Attach main PCB with two Allen head screws (using 2 1/2-mm Allen wrench) and two Phillips head screws.
5. See retest chart Table 6-1.

6.4.3 Motor Driver PCB Removal (Figure A2-1)

1. Remove main PCB (paragraph 6.4.1).
2. Remove two Phillips head screws securing motor driver PCB to the top of the frame.
3. Carefully remove PCB and place it in a protective bag or box.
4. Retain the securing hardware.

6.4.4 Motor Driver PCB Replacement (Figure A2-1)

1. Gently lay motor driver PCB on frame.
2. Attach PCB with two Phillips screws and four HEX spacers.
3. Replace main PCB (paragraph 6.4.2).
4. See retest chart, Table 6-1.

6.4.5 Filter PCB Removal (Figure A2-2)

1. Remove main PCB (paragraph 6.4.1) from mounting; cable removal not necessary.
2. Carefully remove filter PCB from pins on main PCB and place it in protective bag or box.

6.4.6 Filter PCB Replacement (Figure A2-2)

1. Gently lay filter PCB on mating filter pins of main PCB.
2. Replace main PCB (paragraph 6.4.2)
3. See retest chart, Table 6-1.

6.4.7 SAC PCB Removal (Figure A2-1)

1. Four Allen head screws secure the controller chassis to the drive chassis, and are accessible via cutouts at the chassis seams. Remove two screws on one side of the chassis and loosen the two remaining screws.
2. Disconnect the cable between the Basic drive and the SAC.
3. Slide controller chassis to the side to separate it from the drive chassis.
4. Remove four Phillips head screws securing SAC PCB to frame.
5. Carefully remove SAC PCB and place it in a protective bag or box.
6. Retain the securing hardware.

6.4.8 SAC PCB Replacement (Figure A2-1)

1. Gently lay SAC PCB in frame.
2. Attach PCB with four Phillips head screws.
3. Slide controller chassis into two loosened screws on drive chassis to mate chassis.
4. Connect interface cable.
5. Replace the other two securing screws and tighten all four screws.
6. See retest chart, Table 6-1.

6.5 RETEST PROCEDURE

The retest chart in Table 6-1 provides a means of verifying the operational readiness of a repaired drive or Intelligent controller.

Table 6-1 Retest Chart

REPLACED PART DESCRIPTION	RETEST PROCEDURE
Main PCB	All performance test paragraphs 7.2.1 to 7.2.4.
Motor Driver PCB	Read test paragraph 7.2.3.
Filter PCB	Read test paragraph 7.2.3. Write test paragraph 7.2.4
SAC PCB	All performance test paragraphs 7.2.1 to 7.2.4

CHAPTER 7

PERFORMANCE TESTING, CHECKS, AND ADJUSTMENTS

7.1 PERFORMANCE TESTING

Performance testing is of two types: a) performance testing of suspected Basic drive, b) Intelligent controller and performance testing of repaired Basic drives or Intelligent controller. In either type of performance testing, the Basic Drive should be mated with a known good Intelligent controller and the Intelligent controller should be mated with a known good Basic drive. A known good tape should be used in all cases.

7.2 TESTING SUSPECTED OR REPAIRED BASIC DRIVE AND INTELLIGENT CONTROLLER

Always clean the read/write heads and verify that the sensor block is secure and UTH and LTH holes are not obstructed before testing the tape drive. It is useful to establish a data pattern for writing to and reading from tapes. The following data patterns result in a specific number of flux reversals per inch (frpi), A5, 29, and CF. The optimum write data buffer would be 170 bytes of A5, 170 bytes of 29, and 172 bytes of CF (512 bytes total). Establish the optimum pattern. A5 represents a one-half frequency (5000 frpi) whose amplitude when divided into the full-frequency amplitude of all the ones (at 10000 frpi) written by the drive during GAP time, provides a resolution ratio. CF is a worst case data pattern that, combined with a 29 pattern, exercises the units ability to accommodate peak shift.

7.2.1 Power-On Confidence Test

The Power-On Confidence (POC) test runs diagnostic checks in the controller/formatter portion of the SAC PCB. POC is executed upon power-on or RST- (Jumper KK must be present). The following tests are performed:

1. 8031 internal RAM and basic microcomputer instructions.
2. LSI controller chip.
3. 16K RAM chip.
4. Data separator logic.
5. 8155 PIA chip.

Failures detected by POC are reported to the host by the absence of EXC- for more than 5 seconds, which then are detected and displayed by the diagnostic LEDs (DS1 through DS5).

A successful completion of all POC tests is reported via the diagnostic LEDs by a single blink of all five LEDs following the off period during which the POC tests are performed. Successful completion of all POC tests is reported to the host by the assertion of EXC-within 5 seconds.

Each non-8031 test shall have an associated diagnostic LED as follows:

Table 7-1 Diagnostic LEDs

LED	ERROR STATUS
DS1	LSI controller chip error
DS2	16K RAM buffer chip error
DS3	Data separator logic error
DS4	8155 PIA error
DS5	not used

Each time a test fails, the associated diagnostic LED blinks and the test is repeated. Continued failure of a given test is indicated by continued blinking of its associated LED. Failure of the 8031 is indicated by unpredictable results.

Refer to the trouble-shooting chart under POC test failure at the end of this chapter, if a failure of POC test is indicated.

7.2.2 Basic Operations

The following tests address the basic operations of the drive. They require that the drive respond to and execute computer issued commands.

1. Execute a Read Status command without a tape cartridge installed. The unit should respond with No Cartridge and Write Protected.
2. Install an Archive Model 09C Tape Cartridge with Safe indicator positioned to inhibit writing (SAFE).
3. Execute a Read Status command. The unit should respond with Cartridge In and Write Protected.
4. Remove the Archive Model 09C Tape Cartridge and rotate the Safe indicator to enable writing.
5. Execute a Read Status command. The unit should respond with Cartridge In and Write Enabled.
6. Execute a Rewind command to position the tape at BOT (Beginning of Tape).
7. Execute an Initialize Cartridge command. The unit will respond by moving tape from BOT to EOT (End of Tape) and a Rewind from EOT to BOT (approximately two minutes with 600 ft. tape).

If the drive will not operate as indicated in steps 1 through 5, refer to problems with Cartridge Not In Place (CNI) or Write Protected (WRP) in the trouble-shooting chart in this chapter. For tape positioning problems encountered in steps 6 and 7 see tape unloads in the trouble-shooting chart in this chapter.

7.2.3 Read Test

The read test can be used to detect read problems in suspected drives or evaluate the read performance of repaired drives.

Using a known good tape generated by a Master Drive, read at least one pass of the entire tape and compare the soft error status to the following limits:

For 1 error in 1×10^8 bits, the tables are as follows:

20 MB DRIVE		CUMULATIVE NUMBER OF ERRORS					
<u>Number of Passes</u>		0	1	2	3	4	5
1		A	A	T	T	F	F
2			A	A	T	F	
3				A	F		

45 MB DRIVE		CUMULATIVE NUMBER OF ERRORS						
<u>Number of Passes</u>		0	2	4	6	8	10	12
1		A	A	A	T	F	F	F
2				A	T	F	F	
3				A	A	F		

A = Accept, T = Test, F = Fail

If the tape can be read but has an unacceptable number of retries, then perform the alignment check in this chapter. If the tape cannot be read, refer to read problems in the troubleshooting chart in this chapter.

7.2.4 Write Test

The write test can be used to detect write problems in suspected drives or evaluate the write performance of repaired drives. The rate of rewrites should be within those noted.

NOTE

Due to imperfections in tape oxide coating, it is not uncommon to encounter soft errors during writing of data to tape. With a known good qualified cartridge, this soft error rate could approach 400 rewrites for a 20 Mbyte transfer and 900 for a 45 Mbyte transfer.

Using a known good tape, attempt to write to the tape.

NOTE

Ensure that the write protect cam on the cartridge is in the write position before inserting the cartridge in the tape drive.

If the tape is written on, but has an unacceptable number of rewrites, then perform the alignment check in this chapter. If the tape drive cannot write on the tape, recheck the position of the write protect cam and the condition of the tape. If the problem is not with the tape cartridge, refer to the trouble-shooting chart under Write Problems.

7.3 TAPE DRIVE CHECKS

Particular checks of the tape drive are recommended in the course of drive performance testing referenced by the trouble-shooting chart, or may simply be used as an aid in determining the cause of a problem.

Tape drive checks require the use of test equipment listed in Chapter 1, paragraph 1.5. The test equipment is also called out where used in this chapter.

7.3.1 Alignment Checks

There are three mechanical checks: zenith alignment check, vertical track position, and azimuth alignment check. Zenith is checked with a tool. Vertical track and azimuth alignment checks require a special reference tape cartridge.

CAUTION

Proper care of alignment tapes is an important factor in ensuring reliable alignment checks. The following precautions are essential:

1. Alignment tapes are precision tools and must be handled carefully. Ensure proper personnel training and control procedures prior to use.
2. Always keep the alignment tape in a clean container in an area free from magnetic fields (electric motors, transformers, tools, etc.) when not in use.
3. Always cycle alignment tapes from BOT to EOT without stops.
4. Use alignment tapes under controlled temperature conditions ($25^{\circ}\text{C} \pm 3^{\circ}$).

7.3.1.1 Zenith Alignment Check

The zenith alignment check verifies that the forward (front) face of the read/write head is parallel to the vertical tape path. In other words, zenith is the slope or lean of the read/write head as it addresses the tape. Positive zenith would indicate that the head is sloped backwards from the vertical tape while negative zenith would indicate that the head is leaning forward into the vertical tape.

1. Insert the Cartridge Base and Zenith Tool (90098-XXX).
2. Place the face of the tool between the two read/write heads
3. Apply a light pressure to maintain the face of the tool on the face of the head.
4. Verify that the zenith of the read/write head is within \pm 7.5 minutes (1/2 division on the zenith check tool).

CAUTION

Both of the reference tape cartridges required for the following procedures are manufactured by Archive under stringently controlled conditions and are intended for use by Archive trained and qualified personnel under the auspices of a constant calibration and correlation program. The program assures that the integrity of the reference tapes are maintained since indiscriminate use of these tapes may result in erroneous conclusions regarding the integrity of the alignment checks.

7.3.1.2 Vertical Track Position (Figure 7-1)

The objective of the vertical track position check is to verify that the read/write head is properly positioned during the read/write operations.

A Vertical Track Position Reference Tape Cartridge is required. This tape has been written full width with an erase head at 5000 frpi. The Track Zero position on the tape, with the exception of the first 75 feet, has been erased with a read head. The result is a Track Zero null.

1. Oscilloscope Settings:
 SYNC: INT POS 5us CH 1
 CHAN 1: AC 500mV
 MODE: Channel One Only
 CHAN 1 PROBE: TP4 (on Basic drive). (Signal is DIFFOUT).
2. Set ground on the center graticule line. The voltage base is selectable as it will be necessary to adjust the playback observed to full scale.
3. Execute a Cartridge Initialization (Retension) command.

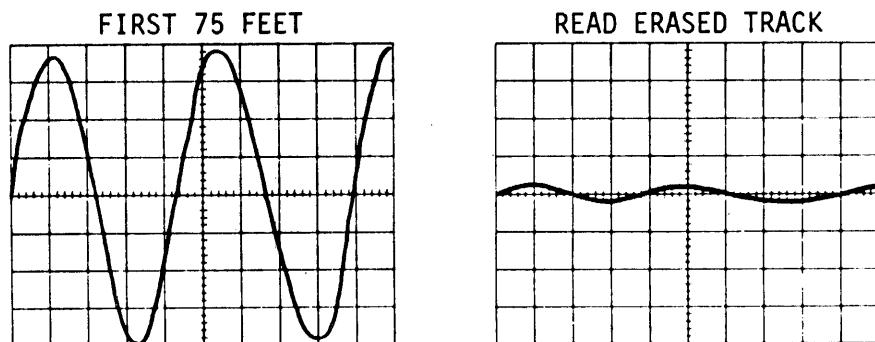


Figure 7-1 Vertical Track Position

4. Set amplitude of playback observed for the first 75 feet (10 seconds for 90 ips) to eight divisions (maximum vertical deflection).
5. Verify that the output for reading the erased Track Zero is less than 0.6 division for both the forward and reverse directions in both horizontal and vertical mounting positions.

7.3.1.3 Azimuth Alignment Check (Figure 7-2)

The azimuth check verifies that the read/write head is perpendicular to the tape path.

An Azimuth Reference Tape is required. This tape has a 15000 frpi signal recorded on Track Zero only. The rest of the tape has been erased.

The objective of this check is to verify that the read/write head does not have excessive azimuthal arc. This is done by verifying that the read head playback amplitude is at, or near, its peak (maximum) and that any movement of the head will result in a decrease in amplitude while reading the azimuth reference tape.

1. Oscilloscope Setting:
 SYNC: INT POS 5us
 CHAN 1: AC 100-200mV
 MODE: Channel One Only
 CHAN 1 PROBE: TP4 (on Basic drive). (Signal is DIFFOUT)
2. Set ground on the center graticule line. The voltage base is selectable as it will be required to adjust the observed playback for six divisions.
3. Execute a Cartridge Initialization (Retention) Command.

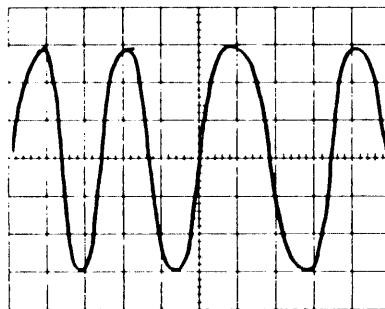


Figure 7-2 Azimuth Alignment Check

4. Apply finger point pressure to the top of the head assembly at two points, on each side.
5. Verify that the playback amplitude decreases in all cases.
6. Should the amplitude increase, note and record the point at which pressure on the head assembly resulted in the increase, i.e. inside or outside, and how much the signal increased.
7. Verify that the increase in amplitude was less than one-half minor division, zero to peak (not peak-to-peak).

7.3.2 Read Playback Verification Check (Figure 7-3)

Read playback confirms that both read heads (one head for forward track and one head for reverse track) and the first stage of the read channel respond within specified limits to a particular test signal off tape. The all ones pattern is the highest frequency signal placed on tape as part of a normal format between blocks of data. This test is performed while monitoring the playback amplitude of the all one's frequency that occurs during the LOCK time between the actual blocks of user data. The frequency of this all one's area is 10000 frpi. Its amplitude is, therefore, the lowest peak-to-peak value of all the possible data patterns/frequencies.

1. Oscilloscope Settings:

SYNC: INT POS 50us CH 1

CHAN 1: DC 2V

CHAN 2: AC 200mV

MODE: Alternate

CHAN 1 PROBE: TPE (on Intelligent controller). (Signal is LOCK)

CHAN 2 PROBE: TPL (on Basic drive). (Signal is DAC)

2. Execute a Read command. Read on adequate number of blocks/bytes to take readings/measurements of the playback amplitude in both directions, i.e. read from both the forward head and the reverse head.

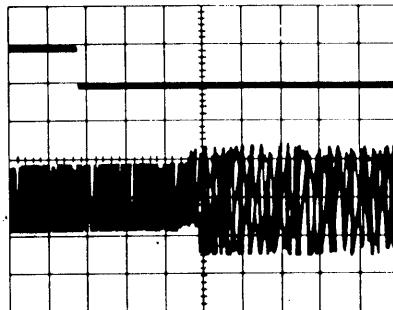


Figure 7-3 Read Playback Verification Signal

3. Verify that the read playback during LOCK is within 400 millivolts in both directions.
4. Note and record the values of the playback amplitudes in both directions.
5. Verify that the amplitudes of each head are within 20 percent of each other, i.e. divide the differences between them by the lesser of the two values and multiply by 100.

If the drive fails to meet these requirements, refer to Read Problems in the trouble-shooting chart at the end of this chapter. Electrical adjustments cannot be used to correct this problem.

7.3.3 Read Data Pulse Check (Figure 7-4)

Read Data Pulse (RDP) check can be used to roughly verify that the read circuits about 1/3 through the read process are producing properly formed read pulses. RDP proceeds from this point to pin 27 on the LSI controller chip on the SAC board.

1. Oscilloscope Settings:
SYNC: INT POS 100ns CH 1
CHAN 1: AC 1V
MODE: Channel One Only
CHAN 1 PROBE: TP7 (on Basic drive). (Signal is RDP)
2. Verify that the timing of the pulse is within 280-440ns.

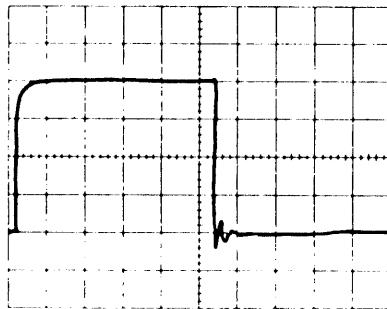


Figure 7-4 Read Data Pulse

7.3.4 Peak Shift Check (Figure 7-5)

This procedure verifies that the PLL accommodates peak shift. In order to perform properly, the PLL must receive a good quality read signal and be properly adjusted. The test is performed by monitoring the output of the PLL's DAC. The objective is to verify that the error signals from the DAC do not exceed the requirements while reading a worst case peak shift pattern.

1. Oscilloscope Settings:
SYNC: INT POS 500us CH 1
CHAN 1: DC 5V
CHAN 2: AC 100mV
MODE: Alternate
CHAN 1 PROBE: TPE (on Intelligent controller). (Signal is LOCK)
CHAN 2 PROBE: TPF (on Intelligent controller). (Signal is DAC)
2. Uncalibrate the time base. Vary the time base to display a LOCK pulse at each end of the screen. The Channel 2 display will then depict one entire 528.5-byte block.
3. If required, execute a Write command with the write buffer set to the combination of 29 and CF, i.e. 50 bytes of 29, 50 bytes of CF, etc., throughout the buffer, Figure 7-5 is based on A5, 29, CF buffer of approximately 170 bytes each.
4. Execute a Read command of adequate block/byte length to facilitate a reading in both directions.

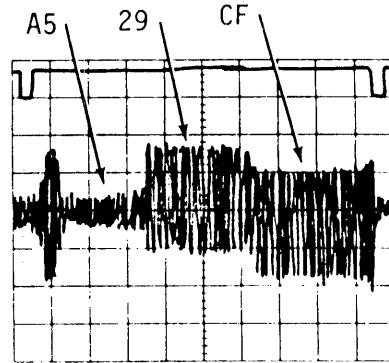


Figure 7-5 Peak Shift Check

5. Verify that the maximum peak-to-peak amplitudes achieved by the combination of 29 and CF does not exceed 1700 millivolts (1.7V) in both directions. The measurement is taken from the top of the 29 pattern to the bottom of the CF pattern and excludes or discounts the minute spikes exceeding the body of the waveform.

If required parameter cannot be met, refer to Read Problems in the trouble-shooting chart at the end of this chapter.

7.3.5 Resolution Check (Figure 7-6)

This procedure verifies the resolution of the read/write heads and is provided as a trouble-shooting aid, not a specification check.

The resolution check provides a check of the ability of the read heads to respond to basic rates of data read from tape. Failure of this test may indicate a worn or faulty head assembly. Refer to Read Problems in the trouble-shooting chart at the end of this chapter to eliminate any other read problems that may interfere with a proper resolution check.

The objective is to measure the playback amplitudes of three basic frequencies, i.e. 10000 frpi, 5000 frpi, and 3300 frpi.

The 10000 frpi gap pattern is available under the LOCK signal. The 5000 frpi is created by writing a data pattern of A5. The 3300 frpi is created by writing a data pattern of 29.

1. Oscilloscope Settings:

- SYNCH: INT POS 50us CH1
- CHAN 1: DC 5V
- CHAN 2: AC 100mV
- MODE: Alternate
- CHAN 1 PROBE: TPE (on Intelligent controller). (Signal is LOCK)
- CHAN 2 PROBE: TP1 (on Basic drive). (Signal is RDAMP)

2. If required, execute a Write command writing blocks of data consisting of A5.
3. Execute a Read Command. Read and record the amplitude of the data gap pattern under the LOCK signal. Locate the A5 pattern written after the gap all ones pattern. Record the amplitude.

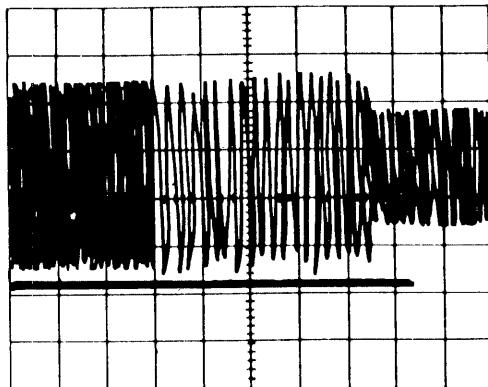


Figure 7-6 Resolution Check

4. Perform the measurement in both directions.
5. Repeat the last three steps with a data pattern of 29.
6. Develop the resolution by taking the ratio of each of the lower frequency, higher signals and dividing them into the high frequency, low amplitude signal. Then multiply by 100 to convert to percentages.
7. Verify that the difference between the heads is less than 20 percent. A typical example is shown as follows:

<u>Amplitude</u>	<u>GAP</u>	<u>A5</u>	<u>29</u>	<u>GAP/A5</u>	<u>GAP/29</u>
Forward	800mv	1300mv	1400	61%	57%
Reverse	750mv	1200mv	1300	63%	58%
Delta	50/750	100/1200	100/1300		
	=7%	=8%	=9%		

8. Verify that the amplitude measured and resolutions developed are within the following tolerances:

Amplitudes:	GAP	400-1200 mv
	A5	725-1570 mv
	29	850-1715 mv
Resolutions:	GAP/	55 to 77%
	A5	47 to 70%

7.3.6 Capstan Motor Noise Check (Figure 7-7)

This procedure verifies that the tape is being erased and that the capstan motor does not create excessive noise. The test is performed by reading an erased tape and monitoring the output of the differentiator for excessive noise spikes.

1. Execute and Erase command. The unit will move tape from BOT to EOT while it performs a full tape width erase. The unit will then move tape back to BOT (about two minutes).
2. Oscilloscope Settings:
SYNC: INT NEG 1ms CH 1
CHAN 1: DC 5V
CHAN 2: AC 200mV
MODE: Alternate
CHAN 1 PROBE: U7 PIN 6 (on Basic drive). (Signal is TACH)
CHAN 2 PROBE: TP4 (on Basic drive). (Signal is DIFFOUT)
3. Execute Initialize Cartridge command. The unit will move from BOT to EOT and back to BOT (approximately two minutes).

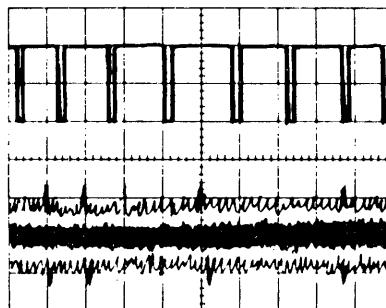


Figure 7-7 Capstan Motor Noise Check

4. Uncalibrate the time base. Vary the time base to display six or eight pulses across screen, i.e. one revolution of the capstan motor.
5. Verify that the noise spikes do not exceed ± 250 millivolts peak (500mV peak-to-peak). The noise spikes will be asynchronous with the tachometer pulses.
6. Failure of the test may indicate a faulty erase circuit on SAC board or a noisy capstan motor.

7.3.7 Capstan Motor Speed Variation (Figure 7-8)

This procedure verifies that the capstan motor is under the control of the microcomputer and does not exhibit excessive speed variation. This test is performed by monitoring the tachometer pulses to the microcomputer during the execution of a Motion command (Erase, Retension, Write, Read, or Rewind).

1. Oscilloscope Settings:

SYNC: INT NEG 500us CH 1

CHAN 1: DC 2V

MODE: Channel One Only

CHAN 1 PROBE: U5 PIN 6(on Basic drive). (Signal is TACH)

2. Execute a Write command. Write from Beginning Of Media (BOM) to End Of Media (EOM). At the conclusion of the Write, ensure that a File Mark is written.

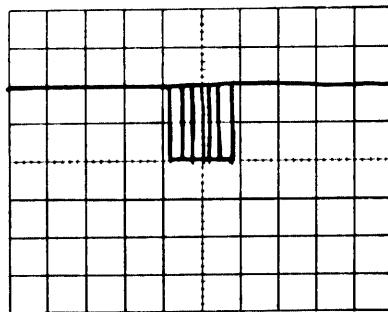


Figure 7-8 Capstan Motor Speed Variation

3. Spread seven or nine negative pulses (see note that follows) across the screen. Using the horizontal position knob, place the leading edge of the first pulse on the first vertical graticule line. Using the variable time base knob, place the reading of the last pulse at the tenth graticule line.

NOTE

If this is a six tach pulse per revolution drive, the seventh pulse will appear to be stable and will be used as 'the last pulse' referred to in this procedure.

If this is an eight tach pulse per revolution drive, the ninth pulse will appear to be stable and will be used as 'the last pulse' referred to in this procedure.

4. Horizontally position the last pulse on the center vertical graticule line and magnify the display times ten (10X).
5. Verify the total 'jitter' does not exceed six vertical graticule lines ± 3 major divisions for the entire length of the tape in both directions.
6. At the conclusion of the Write sequence, note and record the following:
Total number of Blocks/Bytes Written
Total number of Blocks/Bytes Rewritten

NOTE

The number of blocks rewritten is provided via the read status data. The number of blocks rewritten divided by two equals the actual number of rewrites that occurred. Verify that the number of rewrites do not exceed 100.

CAUTION

If a motor speed problem is indicated, it could be due to using a faulty tape cartridge.

If the tape cartridge is good, failure of this check may indicate faulty motor control and drive circuits on the Main PCB or a faulty capstan motor.

7.4 ELECTRICAL ADJUSTMENTS

The electrical adjustments ensure the proper set up of the read system of the main PCB. Read alignment check is not necessary before performing these procedures. Because these adjustments are interactive, all adjustments in the procedure must be checked and in the order given. The first adjustment requires that; power is applied to the drive, a good tape cartridge is installed, and that the drive respond to a Write command from the host computer. All other adjustments require only that power be applied to the drive. The following adjustment procedures verify four potentiometer settings.

7.4.1 Read Amplifier Gain Adjust (R4) (Figure 7-9)

This procedure is a verification of the Write and Read operation of the tape drive. This test is performed by monitoring the waveform output at TP4 on the main PCB. This test may require adjusting potentiometer R4 to bring the signal within tolerance.

1. Oscilloscope Settings:
SWEEP TIME: 2msec
CHAN 1: 1 VOLT/DIV
CHAN 1 PROBE: TP4 (on Basic drive) and GND
2. Input pattern (Hex 29) to tape drive from host and write forward on track 0.
3. Verify that waveform is $1.4 \pm .1$ Volts above and below centerline as shown in Figure 7-9.
4. Adjust potentiometer R4 as required. Verify waveform adjusts to $1.4 \pm .1$ Volts above and below centerline on oscilloscope.
5. Select track 1 and write reverse.
6. Observe waveform and adjust R4 as required for $1.4 \pm .1$ Volts above and below centerline on oscilloscope.

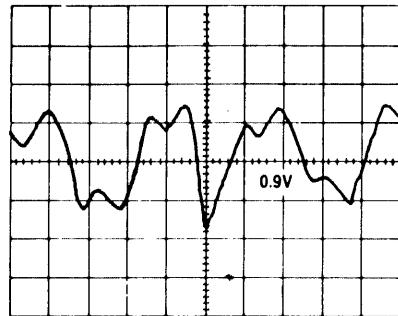


Figure 7-9 Read Amplifier Gain Adjustment

7.4.2 Differentiator Symmetry/Balance (R5) (Figure 7-10)

This procedure is a verification of the symmetrical balance of the differentiator. The test is performed by monitoring the Read Data Pulse (RDP) at TP7 on the Basic drive main board. This test requires turning potentiometer R5 in both directions to verify the adjustment.

**NOTE
DO NOT MOVE TAPE.**

1. Oscilloscope Settings:
SYNC: INT POS 200ns CH 1
CHAN 1: AC 1V
MODE: Channel One Only
CHAN 1 PROBE: TP7 (on Basic drive). (Signal is RDP)
2. Set ground on the center horizontal graticule line.
3. Adjust potentiometer R5 in both directions, and verify that the signal waveform is at its maximum positive position/level.

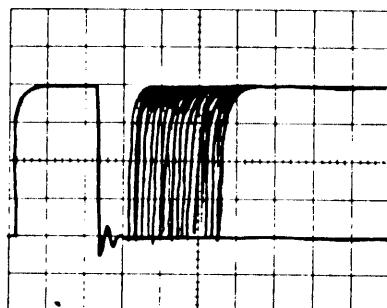


Figure 7-10 Differentiator Symmetry/Balance

7.4.3 Phase Locked Loop Gain (R12) (Figure 7-11)

This procedure verifies the gain setting of the Phase Locked Loop (PLL). The test is performed by monitoring the Read Clock at TPD and injecting a calibration signal into the PLL. The adjustment is made via the R12 potentiometer located on the front of the controller PCB.

1. Select the Basic drive.
2. Jumper the pins together on jumper block C.
3. Oscilloscope Settings:
 - SYNC: INT POS 100ns CH 1
 - CHAN 1: DC 1V
 - MODE: Channel One Only
 - CHAN 1 PROBE: TPD (on Intelligent controller). (Signal is RDCLK)
4. Uncalibrate the time base. Vary the time base to display the entire signal, including all the ‘jitter’, over 9 major divisions on the scope (Figure 7-11).
5. Horizontally position the leading edge on the first left hand graticule line and verify that the entire signal with all of its ‘jitter’ is displayed (Figure 7-11).
6. Verify that the leading edge of the second pulse is within $1.3 \pm .1$ divisions total jitter.
7. Adjust R12 as required. Verify that the entire signal is displayed by manipulating the horizontal position to locate the leading edge and the time base for the last of the second set of leading (rising) edges.
8. Remove the jumper from jumper block C after the check/adjustment.

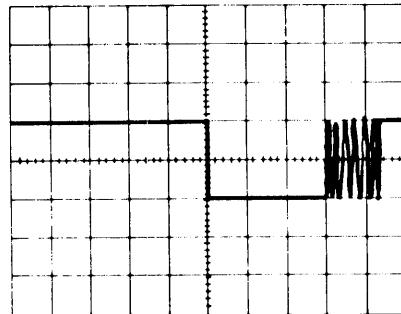


Figure 7-11 Phase Locked Loop Gain

7.4.4 Phase Locked Loop (PLL) Balance (R11) (Figure 7-12)

This procedure is a verification of the Phase Locked Loop (PLL) Balance. The test is performed by monitoring the output of the digital to analog converter (DAC) at TPF while the drive is either reading or writing. TPF is located on the controller PCB.

The adjustment is made via the R11 potentiometer.

1. Oscilloscope Settings:

SYNC: INT POS 50us CH 1

CHAN 1: DC 1V

CHAN 2: AC 100mV

MODE: Alternate

CHAN 1 PROBE: TPE (on Intelligent controller). Signal is LOCK.

CHAN 2 PROBE: TPF (on Intelligent controller). Signal is DAC.

2. Jumper block FF and block C.

3. Execute a Read command. Read an adequate number of blocks to ensure readings/measurements in both directions, i.e. read from both the forward head and reverse head.

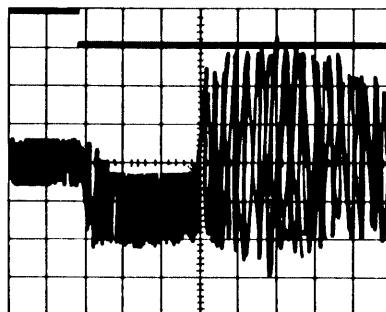


Figure 7-12 Phase Locked Loop Balance

4. Verify that the second level is negative in respect to the first level and that the difference between them is 100 millivolts (0.1V) as measured through the center of the 'fuzz'.
5. Adjust R11 as required to set the difference between the two levels at 100 millivolts (0.1V).
6. Switch the oscilloscope coupling to DC and verify that the second level is at 2.4 VDC.
7. Remove jumpers FF and C.

7.5 TROUBLE-SHOOTING CHART

The trouble-shooting chart is based upon discrepancies in performance and probable causes limited to identifying possible difficulties at the major subassembly level. All internal sockets and plug-in chips should be checked for security. The drive should also be checked for any visible damage.

Table 7-2 Trouble-Shooting Chart

SYMPTOM	CHECK	PROBABLE CAUSE
Drive will not respond	+5 VDC and +12 VDC on SAC board	1. No power from host, or 2. Power to J2 disconnected, or 3. Short in SAC board
POC test failure	POC test, paragraph 7.2.1 SAC board	
<u>Basic Operations Problems</u>	Basic operations tests, paragraph 7.2.2.	
1. Problems with Cartridge Not In Place (CNI) or Write Protected (WRP)	Check by substituting a known good main PCB 1. Drive test passes 2. Drive test fails	1. Main PCB 2. Sensor assembly
2. Tape positioning Problems	Basic Operations test, paragraph 7.2.2.	
a. No tape motion	With power applied, short test point T and push the cartridge-in switch. 1. Motor drives 2. Motor does not drive (remove short from test point T after check) Disconnect the existing motor and externally connect a good motor. Short test point T and push the cartridge-in switch.	1. Replace main PCB 2. Go to next check.

Table 7-2 Trouble-Shooting Chart (Continued)

SYMPTOM	CHECK	PROBABLE CAUSE
b. Tape winds off the reel or tape sheers	1. Motor drives 2. Motor does not drive (remove short from test point T after check) Check for obstructed tape holes Check by substituting a known good main PCB. 1. Test at paragraph 7.2.2, steps 6 & 7, passes 2. Test at paragraph 7.2.2, steps 6 & 7, fails	1. Replace capstan motor 2. Replace main PCB Dirty tape holes 1. Main PCB 2. Sensor assembly
<u>Read Problems</u>	Read Test, paragraph 7.2.3	
1. Will not read	Check by substituting a known good main PCB 1. Drive test passes 2. Drive test fails	1. Main PCB 2. See other checks
2. Will not read due to improper head position	Remove cartridge and watch head calibration movement on RESET or power up Head does not move	Carriage assembly
3. Will read, but with an unacceptable number of retries	Double check the quality of the tape in use Check head alignment, if not already done, paragraph 7.3.1 Check read system adjustments	Faulty tape cartridge Head alignment Read system needs adjustment paragraph 7.4

Table 7-2 Trouble-Shooting Chart (Continued)

SYMPTOM	CHECK	PROBABLE CAUSE
<p><u>Write Problems</u></p> <p>Does not write or has an unacceptable number of rewrites</p>	<p>If all other read checks fail to identify the read problem, perform Resolution Check, paragraph 7.3.5. Check Fails</p> <p>Write Test, paragraph 7.2.4</p> <p>Substitute a good main PCB</p> <p>1. Drive test passes 2. Drive test fails</p> <p>Verify that head alignment is correct</p> <p>Double check the quality of the tape cartridge used for the write test</p> <p>Failure of the above checks to identify the problem indicate a possible carriage assembly problem (write head failure)</p>	<p>Replace carriage assembly</p> <p>1. Main PCB 2. See next checks</p> <p>Head alignment</p> <p>Faulty cartridge</p> <p>Carriage assembly</p>

APPENDIX I

MASTER DRIVE

A1.1 MASTER DRIVE

A Master Drive is frequently maintained by users and distributors as a secondary standard. This Master Drive is used to check the quality of tapes written by drives which are in daily use in the field. Specifically, this drive may be used to create software distribution tapes or to create test tapes used for product verification. This appendix contains information to be used by a trained maintenance person and is intended to ensure the viability of the Master Drive as a standard.

A1.2 MASTER DRIVE CLEANING

Perform the following cleaning procedures on the Master Drive after each 10 hours of use. Clean the drive after each new tape is used, or after every two hours if all new tapes are being used.

1. Clean the read/write head using a clean, lintless cotton swab saturated with 95% isopropyl alcohol.

NOTE

Q-tips will leave cotton on the head, which could lead to data errors.
Be sure to remove all visible oxide.

2. Using alcohol dampened swab, clean the tape hole detector opening.
3. Using alcohol dampened swab, wipe all dust and debris out of the tape cartridge cavity.

A1.3 MASTER DRIVE VERIFICATION

On a scheduled basis, perform the alignment and adjustment procedures in Chapter 7 using the special tools listed to verify the quality of the Master Drive. Archive Corporation will train personnel to effectively use these procedures.

CAUTION

Extreme caution should be exercised when performing the procedures in Chapter 7 on the Master Drive. Insure all personnel are properly trained and that adequate controls are in place prior to using the alignment and adjustment procedures.s in the controller/formatter portion of the SAC PCB. POC is executed upon power-on or RST- (Jumper KK must be present). The following tests are performed.

APPENDIX II

PARTS LISTS

A2.1 SCOPE

This Appendix contains the parts lists and parts location diagrams for the Scorpion Drive.

Table A2-1 Scorpion Parts List

Item (Fig. A2-1)	Part Number	Description	Qty	Usage Code (1)
1	80061-903	Main PCB	1	
2	80017-003	Motor Driver PCB	1	
3	80153-XXX	SAC PCB	1	A
3	80153-XXX	SAC PCB	1	B
3	80154-XXX	SAC PCB	1	C
3	80154-XXX	SAC PCB	1	D
4	80173-XXX	EPROM QIC-11	1	A,C (2)
4	80181-XXX	EPROM QIC-24/11	1	B,D (2)
5	20405-001	Filter PCB	1	(3)
6	20251-00X	Belt	1	E
7	40178-002	Bezel, Controller	1	E
8	40194-001	Bezel, Basic Drive	1	E
9	30167-001	Knob	1	E
9	30188-001	Spring Clip	1	E
10	50202-001	Chassis, Controller	1	E

Notes:

1. Usage Code column contains codes which indicate that a part or assembly is used with a particular model of tape drive. See list below:
 A-Model 5920L-1
 B-Model 5920L-2
 C-Model 5945L-1
 D-Model 5945L-2
 E-All Models
2. The EPROM is a separately ordered part and is required to complete a SAC PCB assembly.
3. The filter board is a separately ordered part and is required to complete a Main PCB assembly.

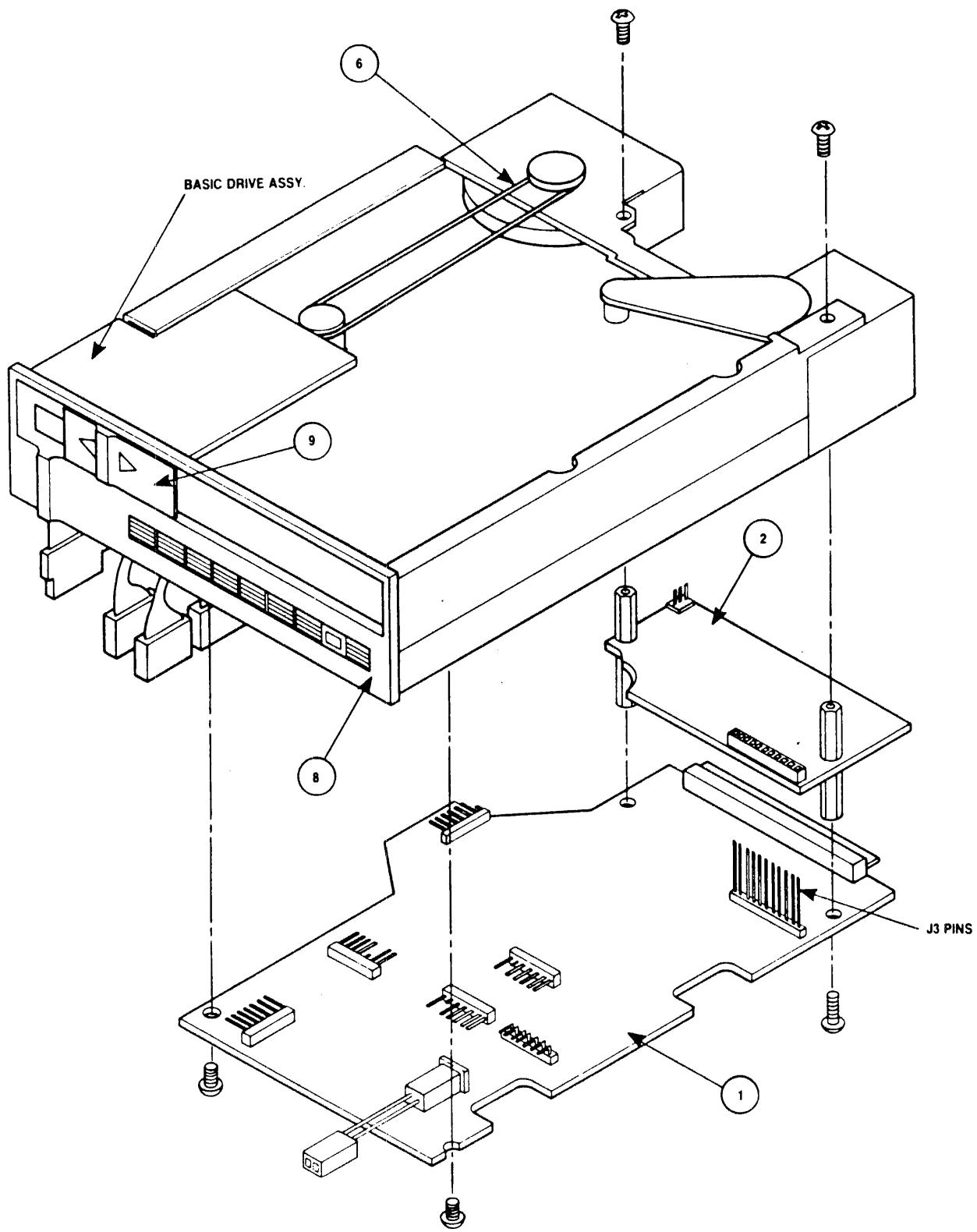


Figure A2-1 Scorpion Parts Location (Sheet 1 of 2)

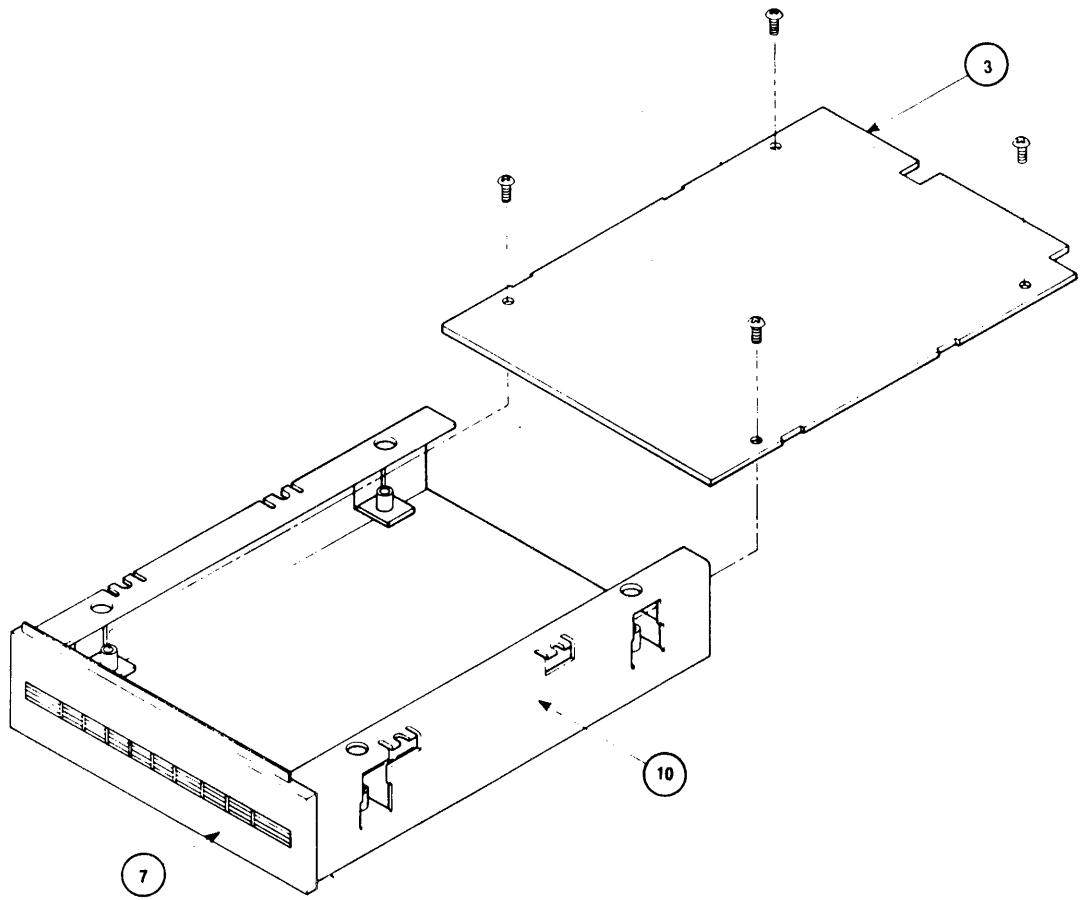


Figure A2-1 Scorpion Parts Location (Sheet 2 of 2)

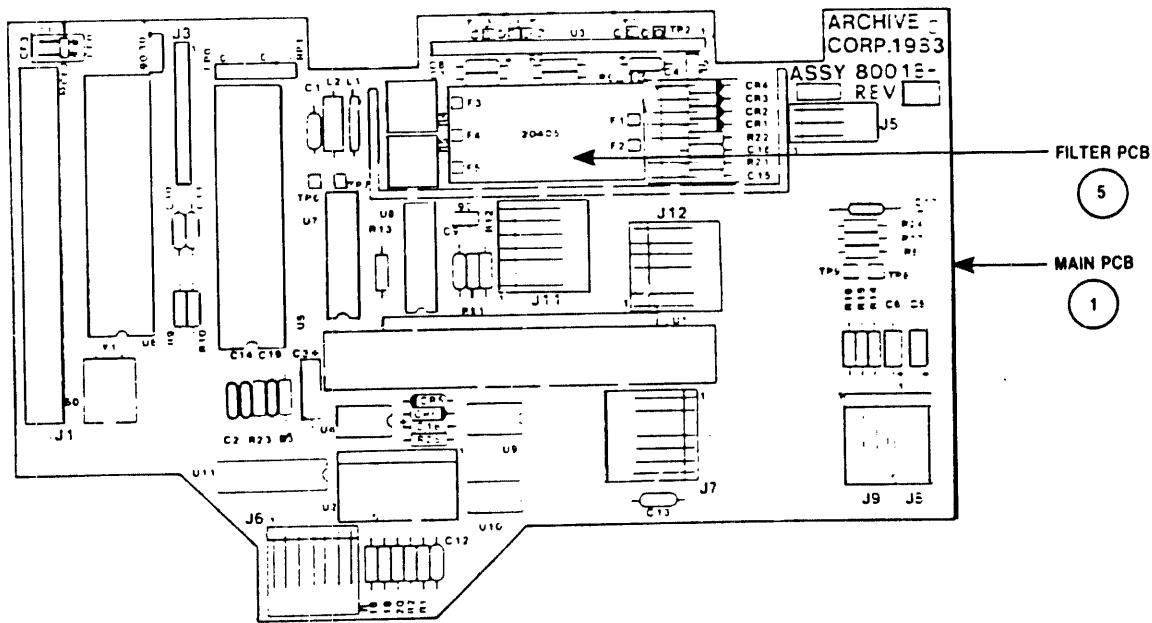


Figure A2-2 Main PCB Parts Location

Table A2-2 Main PCB Parts List

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	REFERENCE DESIGNATOR
80061-903	ASSY., MAIN PCB, SCORPION (FIG A2-2)	1 EA	(3)
20254-001	LSI, BASIC DRIVE	1 EA	(1)U5
20260-002	UCOMPUTER VER 3.00 W/PROM	1 EA	(2)U6
80018-903	S/A SCORP MAIN PCB	1 EA	
14403-001	TAPE, DOUBLE COATED	3 EA	(1)U1 U2,Y1
15500-047	CAP., CER. 5% 50V 4.7PF	1 EA	(1)C10
15500-200	CAP., CER. NPO 5% 50V 20PF	1 EA	(1)C11
15500-221	CAP., CER. NPO 5% 50V 220PF	1 EA	(1)C9
15500-301	CAP., CER. NPO 5% 50V 300PF	1 EA	(1)C16
15501-226	CAP., TANT. 20% 10V 22UF	2 EA	(1)C5,6
15502-685	CAP., TANT. 20% 4V 6.8UF	2 EA	(1)C4,8
15503-225	CAP.TANT.20% 35V 2.2UF	1 EA	(1)C18
15503-334	CAP. TANTALUM, 20% 35V .33UF	1 EA	(1)C14
15504-156	CAP, TANTALUM 20% 20V 15UF	2 EA	(1)C3,17
15505-104	CAP., CER. Z5U 50V .1UF	6 EA	(1)C1,2,7, 12,13,19
15506-272	CAP.,CER. 10% 2700PF	1 EA	(1)C15
15809-003	CONN. 3 PIN AMP 640099-3	1 EA	(1)J-5
15810-006	PIN, .025 SQUARE TIN	9 EA	(1)TP1-TP9
15810-007	PIN, .025 SQUARE SEL GOLD	11 EA	(1)F1-5 RP0,RP1
15815-040	SOCKET, I.C. 40 PIN DIP	2 EA	(1)U5,U6
15816-001	CLIP, JUMPER #DC25-100-2-T	2 EA	(1)RP0,1
15817-008	WAFER, RGT ANG #22-12-2081	1 EA	(1)J13
15837-011	CONN, MOLEX(4030-NBA-11 POS)	1 EA	(1)J3
15843-002	WAFER, RGT ANG, BERG 65521-402	1 EA	(1)CF0
15845-050	CONN, RGT ANGLE, 50 PIN EDGE	1 EA	(1)J1
15849-007	HEADER	5 EA	(1)J6,7,8, 9,11,12
16000-005	CRYSTAL, 10.7386 MHZ, HC-18	1 EA	(1)Y1

Table A2-2 Main PCB Parts List (Cont.)

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	REFERENCE DESIGNATOR
16100-001	DIODE, 1N4150	4 EA	(1)CR1-4
16401-106	INDUCTOR, MOLDED 10% 10UH	1 EA	(1)L2
16513-001	I.C., 9602	1 EA	(1)U8
16567-001	I.C., 74LS244	1 EA	(1)U7
16575-001	I.C., 75478	2 EA	(1)U9,10
17801-104	POT, TRIMMER 10% 100K	1 EA	(1)R5
17801-502	POT, TRIMMER 10% 5K	1 EA	(1)R4
18200-020	RESIS, CAR., 1/4W 5% 2 OHMS	1 EA	(1)R25
18200-102	RESIS, CAR. 1/4W 5% 1K	4 EA	(1)R10,18 R19,20
18200-104	RESIS, CAR. 1/4W 5% 100K	2 EA	(1)R15,16
18200-105	RESIS, CAR. 1/4W 5% 1 MEG	1 EA	(1)R9
18200-150	RESIS, CARBON 1/4W 5% 15	2 EA	(1)R3,R24
18200-152	RESIS, CAR. 1/4W 5% 1.5K	1 EA	(1)R23
18200-181	RESIS, CAR, 1/4W 5% 180	1 EA	(1)R17
18200-221	RESIS, CAR. 1/4W 5% 220	1 EA	(1)R2
18200-331	RESIS, CAR. 1/4W 5% 330	1 EA	(1)R1
18200-333	RESIS, CAR. 1/4W 5% 33K	2 EA	(1)R6,7
18200-472	RESIS, CAR. 1/4W 5% 4.7K	2 EA	(1)R8,13
18201-101	RESIS, CARBON, 1/2W 5% 100	1 EA	(1)R14
18203-381	RES, MET FILM 1/4W 1% 9.09K	1 EA	(1)R12
18203-413	RESIS, MET.FLM. 1/4W 1% 19.6K	1 EA	(1)R11
18205-001	TERMINATOR, 16 PIN DIP	1 EA	(1)U11
18216-306	RES. MTL. FLM 1/8W 1% 1.5K	1 EA	(1)R21
18216-335	RES. MTL. FLM 1/8W 1% 3.01K	1 EA	(1)R22
19402-001	WIRE, SOLID JUMPER, 26 AWG	3 FT	(1)90IPS (2 PLC)L1
19500-008	BUS BAR 8 TAB .25	1 EA	(1)
20244-002	READ CHAIN HYBRID	1 EA	(1)U3
20244-001	READ CHAIN HYBRID	1 EA	
20424-001	RESET LOW VOL DETECT HYBRID	1 EA	(1)U2
20473-001	WRITE/ERASE HYBRID III	1 EA	(2)U1
50188-003	MAIN PCB, DETAIL, SCORPION 2	1 EA	(2)

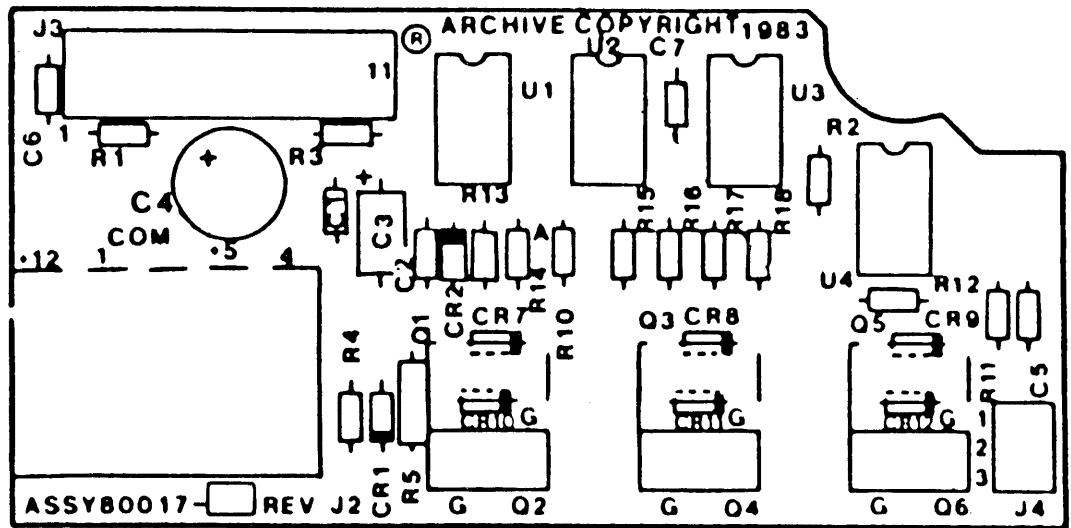


Figure A2-3 Motor Driver PCB Parts Location

Table A2-3 Motor Driver PCB Parts List

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	REFERENCE DESIGNATOR
80017-003	ASSY, MTR DRIVER PCB #3, SCORP 2 (FIG A2-3)	1 EA	(4)
12653-001	HEAT SINK	3 EA	(2)
12900-004	NUT, HEX 4-40	3 EA	(2)
13602-406	SCREW, PAN HEAD, PHILLIPS	3 EA	(2)
15501-226	CAP., TANT. 20% 10V 22UF	1 EA	(2)C3
15506-103	CAP, CER X7R 10% 50V .01UF	2 EA	(2)C5,7
15511-104	CAP, CERAMIC, 50V, 0.1UF	3 EA	(2)C1,2,6
15512-107	CAP, ELECTROLYIC, 35V, 100UF	1 EA	(2)C4
15808-003	HEADER, .100 CENTERS	1 EA	(2)J4
15833-001	CONNECTOR, AMP 641737-1	1 EA	(2)J2
15836-011	CONNECTOR, 11 PIN MOLEX	1 EA	(2)J3
16100-001	DIODE, 1N4150	2 EA	(2)CR1,2
16106-103	DIODE, 11DQ0D(IRF)	6 EA	(2)CR7-12
16590-001	I.C. VOLTAGE COMPARATOR	1 EA	(1)U4
16596-001	I.C., 75361	3 EA	(2)U1-U3
18208-001	RESIS, WIREWOUND 1W 1% .1	1 EA	(2)R5
18216-289	RES. MTL. FLM 1/8W, 1% 1.00K	1 EA	(1)R3
18216-290	RES. MTL. FKM 1/8W, 1% 1.02K	1 EA	(1)R12
18216-397	RES. MTL. FLM 1/8W 1% 13.3K	1 EA	(1)R11
18216-467	RES. MTL. FLM 1/8W 1% 71.5K	1 EA	(1)R2
18216-477	RES. MTL. FLM 1/8W 1% 90.9K	1 EA	(1)R4
18218-101	RESIS, CARBON 1/8W 5% 100 OHMS	6 EA	(2)R13-R18
19114-001	HEX FET, IRF9531, "P" CHANNEL	3 EA	(2)Q2,4,6
19118-001	HEX FET, IRF531, "N" CHANNEL	3 EA	(2)Q1,3,5
30187-001	HEAT SINK	3 EA	(2)
40197-003	PCB DETAIL, MOTOR DRIVER PCB 3	1 EA	(2)
80186-001	SUB-ASSY RESISTOR	1 EA	(1)R1
18216-351	RES.FXD.MTL FILM 1/8W 1% 4.42K	1 EA	
18216-353	RES.FXD.MTL FILM, 1/8W,1% 4.64K	1 EA	
18216-355	RES.FXD.MTL FILM, 1/8W 1% 4.87K	1 EA	
18216-357	RES.FXD.MTL FILM, 1/8W 1% 5.11K	1 EA	
18216-359	RES.FXD.MTL FILM, 1/8W 1% 5.36K	1 EA	
18216-361	RES.FXD.MTL FILM, 1/8W 1% 5.62K	1 EA	
18216-363	RES.FXD.MTL FILM, 1/8W 1% 5.90K	1 EA	
18216-365	RES.FXD.MTL FILM, 1/8W 1% 6.19K	1 EA	
18216-367	RES.FXD.MTL FILM, 1/8W 1% 6.49K	1 EA	
18216-369	RES.FXD.MTL FILM, 1/8W 1% 6.81K	1 EA	
18216-371	RES.FXD.MTL FILM, 1/8W 1% 7.15K	1 EA	
18216-373	RES.FXD.MTL FILM, 1/8W 1% 7.50K	1 EA	
18216-375	RES.FXD.MTL FILM, 1/8W 1% 7.87K	1 EA	
18216-377	RES.FXD.MTL FILM, 1/8W 1% 8.25K	1 EA	
18216-379	RES.FXD.MTL FILM, 1/8W 1% 8.66K	1 EA	
18216-381	RES.FXD.MTL FILM, 1/8W 1% 9.09K	1 EA	
18216-383	RES.FXD.MTL FILM, 1/8W 1% 9.53K	1 EA	
18216-385	RES.FXD.MTL FILM, 1/8W 1% 10.0K	1 EA	

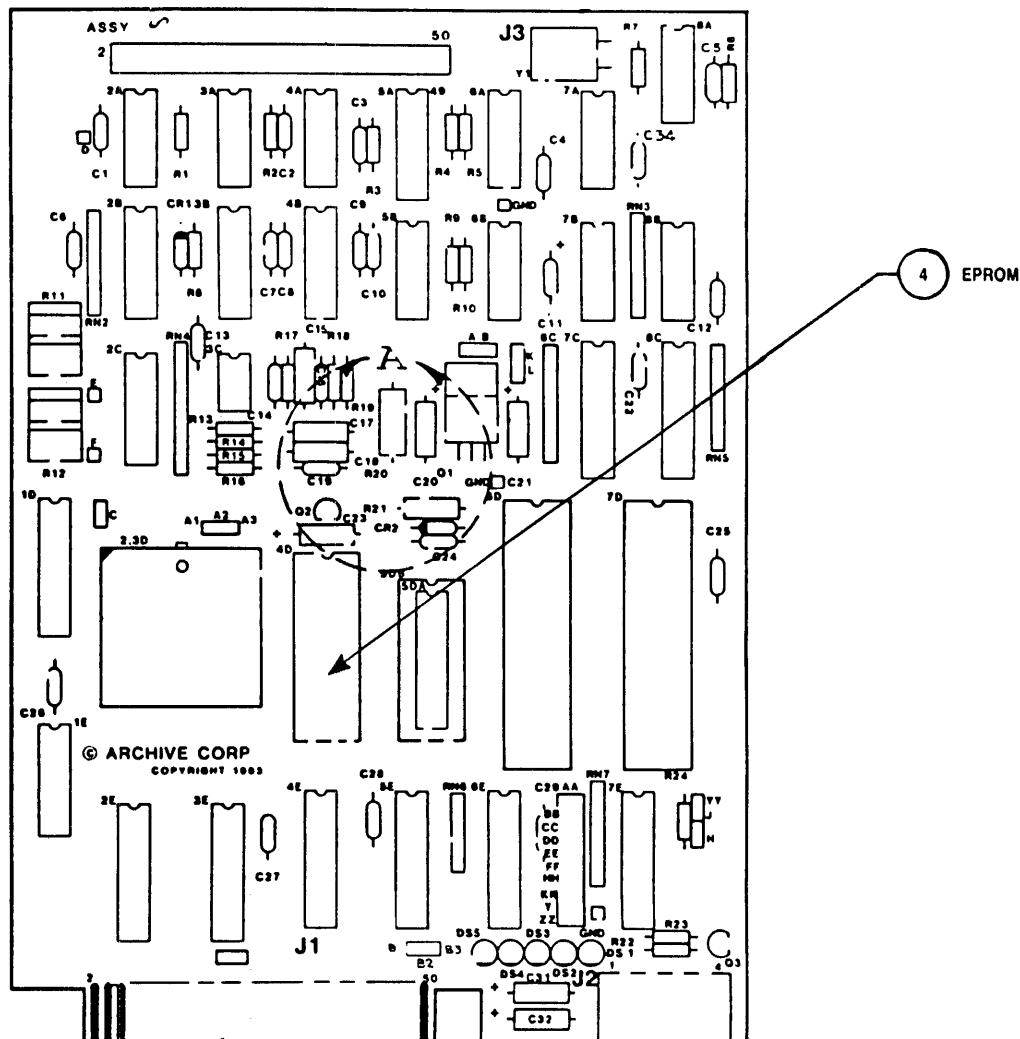


Figure A2-4 SAC PCB Parts Location

Table A2-4 SAC PCB Parts List

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	REFERENCE DESIGNATOR	USAGE CODE
80153-001	ASSY PCB SC149-1 (FIG A2-4)	1 EA		A
80153-002	ASSY PCB SC149-2 (FIG A2-4)	1 EA	B	C
80154-001	ASSY PCB SC199-1 (FIG A2-4)	1 EA		D
80154-002	ASSY PCB SC199-2 (FIG A2-4)	1 EA		
15816-001	CLIP, JUMPER #DC25-100-2-T	6 EA	(1)	
17308-001	MICROCOMPUTER, 8031	1 EA	(1)6D	
20200-102	LSI, CONTROLLER	1 EA	(2)2D	A,C
20461-002	LSI, CONTROLLER, QIC-24	1 EA	(1)2D	B,D
80158-001	S/A SAC 12V SUPSD BY -002	1 EA	(4)	
19402-001	WIRE, SOLID JUMPER, 26 AWG	.170 FT		
80160-001	S/A PCB SAC SUPSD BY -002	1 EA	(2)	
14400-001	TAPE, DBL COATED POLYURETHANE	1 FT	(1)Y1	
15500-068	CAP., CER. 5% 50V 6.8PF	2 EA	(1)C5,C8	
15500-152	CAP. CER.5% 50V 1500PF	1 EA	(1)C18	
15500-240	CAP., CER. 5% 50V 24PF	2 EA	(1)C9,34	
15500-301	CAP., CER. NPO 5% 50V 300PF	1 EA	(1)C19	
15500-822	CAP., CER. 5% 50V 8200PF	1 EA	(1)C17	
15501-225	CAP., TANT. 20% 10V 2.2UF	1 EA	(1)C11	
15501-226	CAP., TANT. 20% 10V 22UF	1 EA	(1)C32	
15501-475	CAP., TANT. 20% 10V 4.7UF	1 EA	(1)C20	
15503-475	CAP., TANT. 20% 35V 4.7UF	2 EA	(1)C21,31	
15505-104	CAP., CER. Z5U 50V .1UF	13 EA	(1)C1,2,4 C6,C12-14 C22,C25-30	
15506-103	CAP, CER X7R 10% 50V .01UF	4 EA	(1)C3,7 C10,13	
15810-006	PIN, .025 SQUARE TIN	23 EA	(1)A(2)A1, A2,A3,B B1,B2,B3 C(2),D,E, F,H,J K(2),L,YY GND(3)	
15815-016	SOCKET, I.C. 16 PIN DIP	1 EA	(1)1E (TERM)	
15815-028	SOCKET, I.C., 28 PIN	1 EA	(1)4D,PROM	
15815-040	SOCKET, I.C. 40 PIN DIP	2 EA	(1)6D,7D UPS	
15818-020	HEADER, DOUBLE ROW, STRAIGHT	1 EA	(1)CONFIG	
15833-001	CONNECTOR, AMP 641737-1	1 EA	(1)J2 (POWER)	
15842-001	I.C. SOCKET, 68 PIN	1 EA	2D	
15846-024	SOCKET, 24 PIN	1 EA	(2)5D-B	
15854-050	HEADER, DOUBLE ROW	1 EA	(1)J3	
16000-004	CRYSTAL, 10.7386 MHZ	1 EA	(1)Y1	
16100-001	DIODE, 1N4150	1 EA	(1)CR1	
16103-001	DIODE, IN4001	1 EA	(1)CR2	
16500-001	I.C., 74S240	2 EA	(1)3E,6E	
16521-001	I.C., 74LS14	1 EA	(1)8B	
16539-001	I.C., 4044	1 EA	(1)6B	
16548-001	I.C., 74LS240	4 EA	(1)2E4E 5E,7C	
16551-001	I.C., 74LS373	1 EA	(1)5D	
16555-001	I.C., 74S74	4 EA	(1)2A,3A 4A,7B	

Table A2-4 SAC PCB Parts List (Cont.)

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	REFERENCE DESIGNATOR
16556-001	I.C., 74S00	1 EA	(1)5B
16557-001	I.C., 74S04	1 EA	(1)6A
16559-001	I.C., 74S174	1 EA	(1)2B
16560-001	I.C., 74S124	1 EA	(1)4B (VC0)
16561-001	I.C., LF353	1 EA	(1)3C
16562-001	I.C., CD4502	2 EA	(1)2C,5A
16567-001	I.C., 74LS244	1 EA	(1)8C
16572-001	I.C., 2167-3	1 EA	(1)1D (RAM 16KX1)
16573-001	I.C., TL78005	1 EA	(1)Q1
16577-001	I.C., 74HC04	1 EA	(1)8A
16579-001	I.C., 74S86	1 EA	(1)7A
16594-001	I.C., 8155	1 EA	(1)7D
16606-001	IC 74F163 4 BIT BINARY COUNTER	1 EA	(1)3B
17202-001	INDICATOR, LED (RED) T1	5 EA	(1)DS1-5
17801-502	POT, TRIMMER 10% 5K	1 EA	(1)R12
17801-503	POT, TRIMMER 10% 50K	1 EA	(1)R11
18200-101	RESIS, CAR. 1/4W 5% 100	1 EA	(1)R3
18200-102	RESIS, CAR. 1/4W 5% 1K	2 EA	(1)R1,2
18200-103	RESIS, CAR. 1/4W 5% 10K	3 EA	(1)R4,5,16
18200-104	RESIS, CAR. 1/4W 5% 100K	1 EA	(1)R15
18200-105	RESIS, CAR. 1/4W 5% 1 MEG	1 EA	(1)R6
18200-272	RESIS, CAR. 1/4W 5% 2.7K	1 EA	(1)R24
18200-332	RESIS, CAR. 1/4W 5% 3.3K	1 EA	(1)R25
18200-333	RESIS, CAR. 1/4W 5% 33K	2 EA	(1)R9,10
18200-362	RESIS, CAR. 1/4W 5% 3.6K	1 EA	(1)R17
18200-472	RESIS, 1/4W 5% 4.7K	4 EA	(1)R7,R19 R22,R23
18200-511	RESIS, CAR. 1/4W 5% 510	1 EA	(1)R8
18203-335	RESIS, MET.FLM. 1/4W 1% 3.01K	1 EA	(1)R13
18203-361	RESIS, MET.FLM. 1/4W 1% 5.62K	2 EA	(1)R14,18
18205-001	TERMINATOR, 16 PIN DIP	1 EA	(1)1E
18211-471	NETWORK, RES 470 6 PIN	1 EA	(1)RN6 LED PULLUP
18212-103	NETWORK, RES 10K 8 PIN	3 EA	(1)RN2 RN5,7 PULLUPS
18219-001	TERMINATOR, 8 PIN SIP 220/330	1 EA	(1)RN3
19107-001	TRANSISTOR, NPN 2N3904	1 EA	(1)Q3
20215-001	NETWORK, RESISTOR	1 EA	(1)RN4 LADDER (CTS)
20425-001	HYBRID, RESET CKT	1 EA	(1)6C
20467-001	IC PAL10H8 PROGRAMMED	1 EA	(1)7E
50107-003	DET SAC	1 EA	(1)

Table A2-5 Filter Board Parts List

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	REFERENCE DESIGNATOR
20405-001	ASSY, FILTER PCB, 90 IPS	1 EA	(3)
15500-101	CAP., CER. NPO 5% 50V 100PF	1 EA	(1)C3
15500-200	CAP., CER. NPO 5% 50V 20PF	1 EA	(1)C4
15500-391	CAP., CER. NPO 5% 50V 39OPF	2 EA	9)C1,2
5838-001	RECEPTACLE CONTACT	5 EA	(1)AMP
16401-127	INDUCTOR, MOLDED 5% 120UH	2 EA	(1)L3,4
16401-277	INDUCTOR, MOLDED 5% 270UH	2 EA	(1)L1,2
50104-001	BOARD, PN-FILTER (LSI)	1 EA	

APPENDIX III

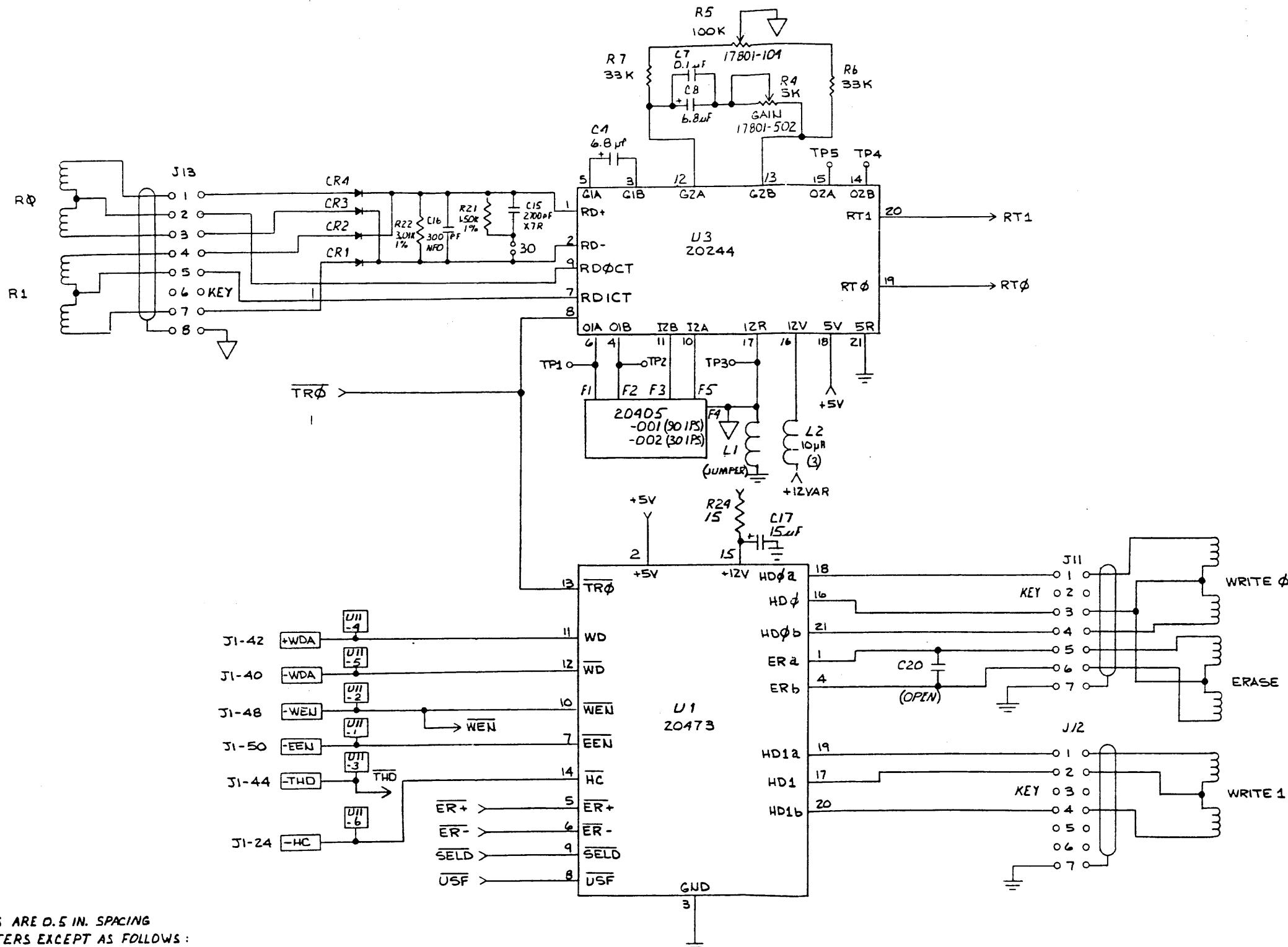
SCHEMATIC DIAGRAMS

A3.1 SCOPE

This appendix contains the schematic diagrams for the Scorpion Intelligent tape drive.

Table A3-1 Schematic Diagrams

FIGURE	TITLE
A3-1	Main PCB, Schematic Diagram (2 sheets)
A3-2	Motor Driver, Schematic Diagram (1 sheet)
A3-3	Stand-Alone Controller Schematic Diagram (3 sheets)



<u>LAST USED</u>	<u>NOT USED</u>
R 25	U 4
C 20	J 2, 4, 10
CR 6	C 19
U 11	L 2
L 2	TP 9
TP 9	J 12
J 12	

Figure A3-1 Main PCB Schematic Diagram
(Sheet 1 of 2)

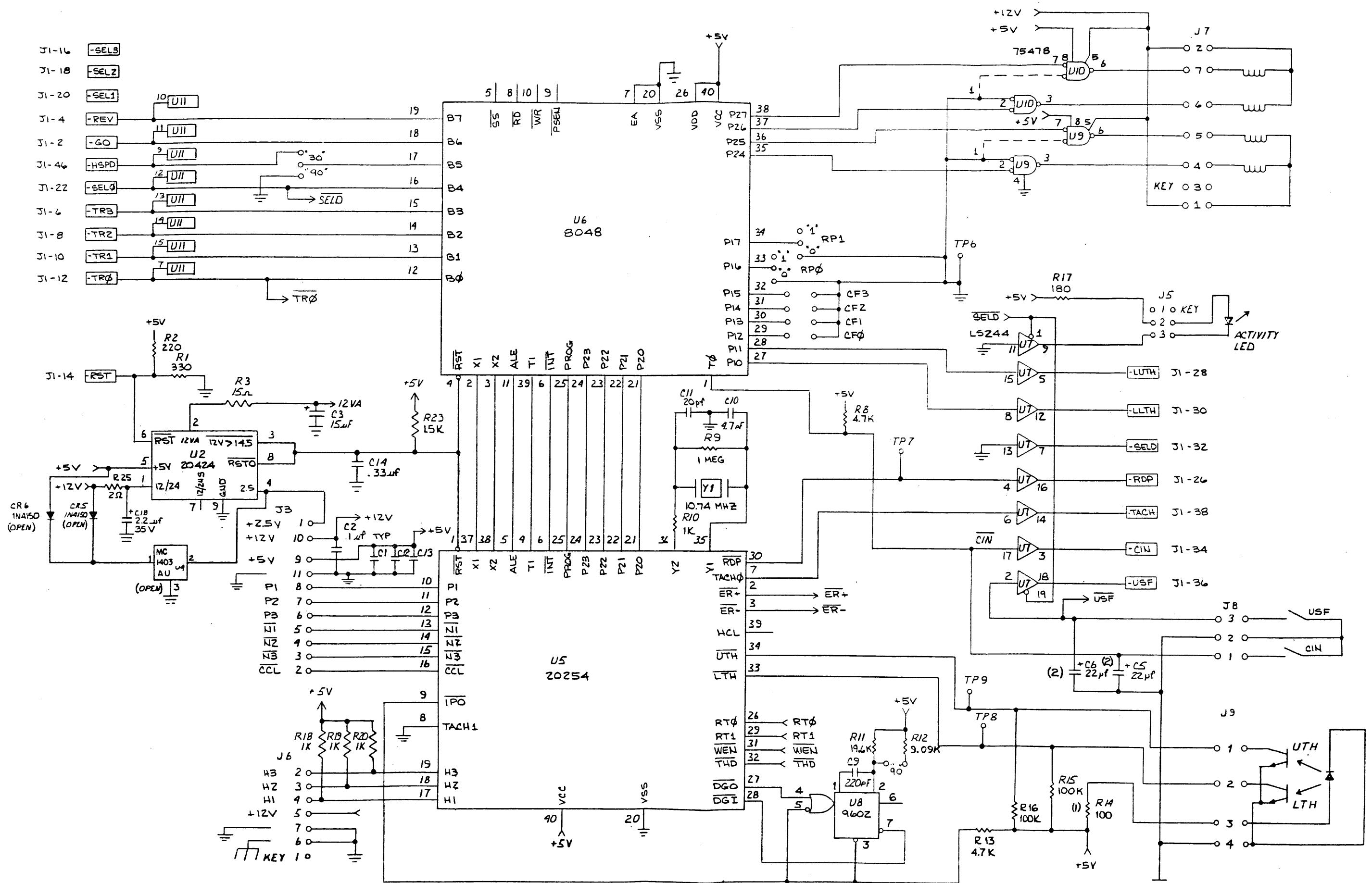


Figure A3-1 Main PCB Schematic Diagram
(Sheet 2 of 2)

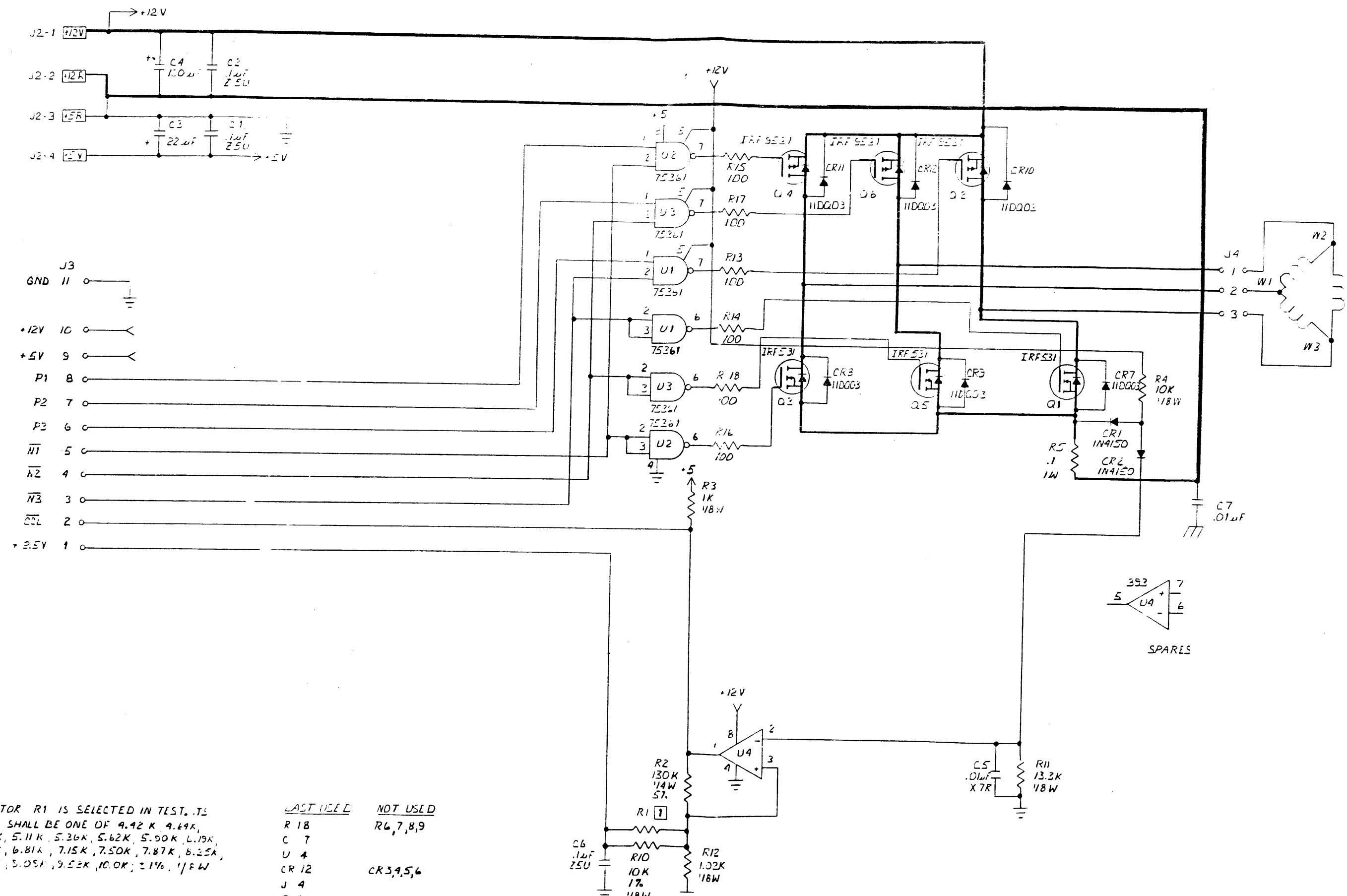


Figure A3-2 Motor Driver Schematic Diagram

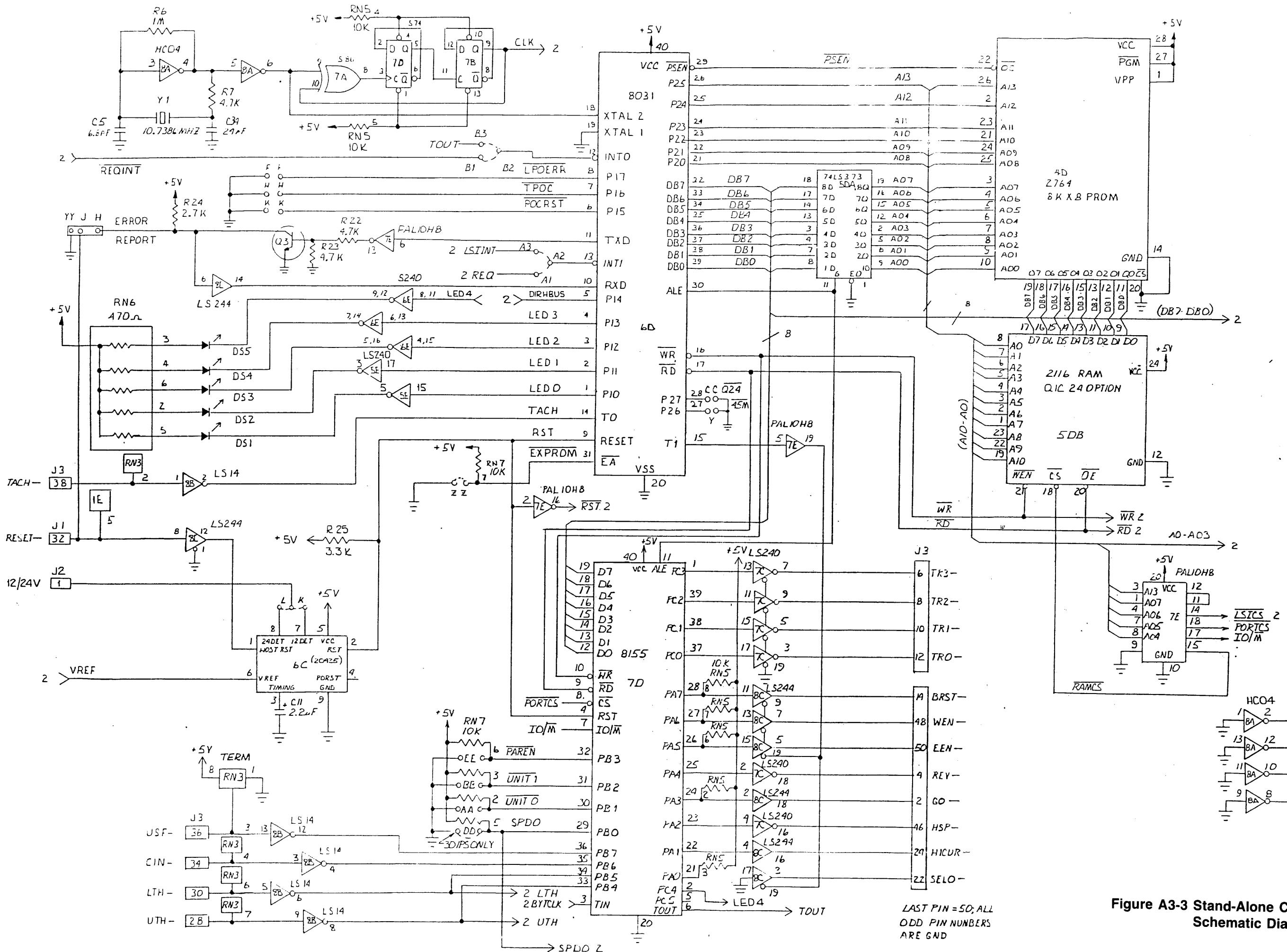


Figure A3-3 Stand-Alone Controller Schematic Diagram (Sheet 1 of 3)

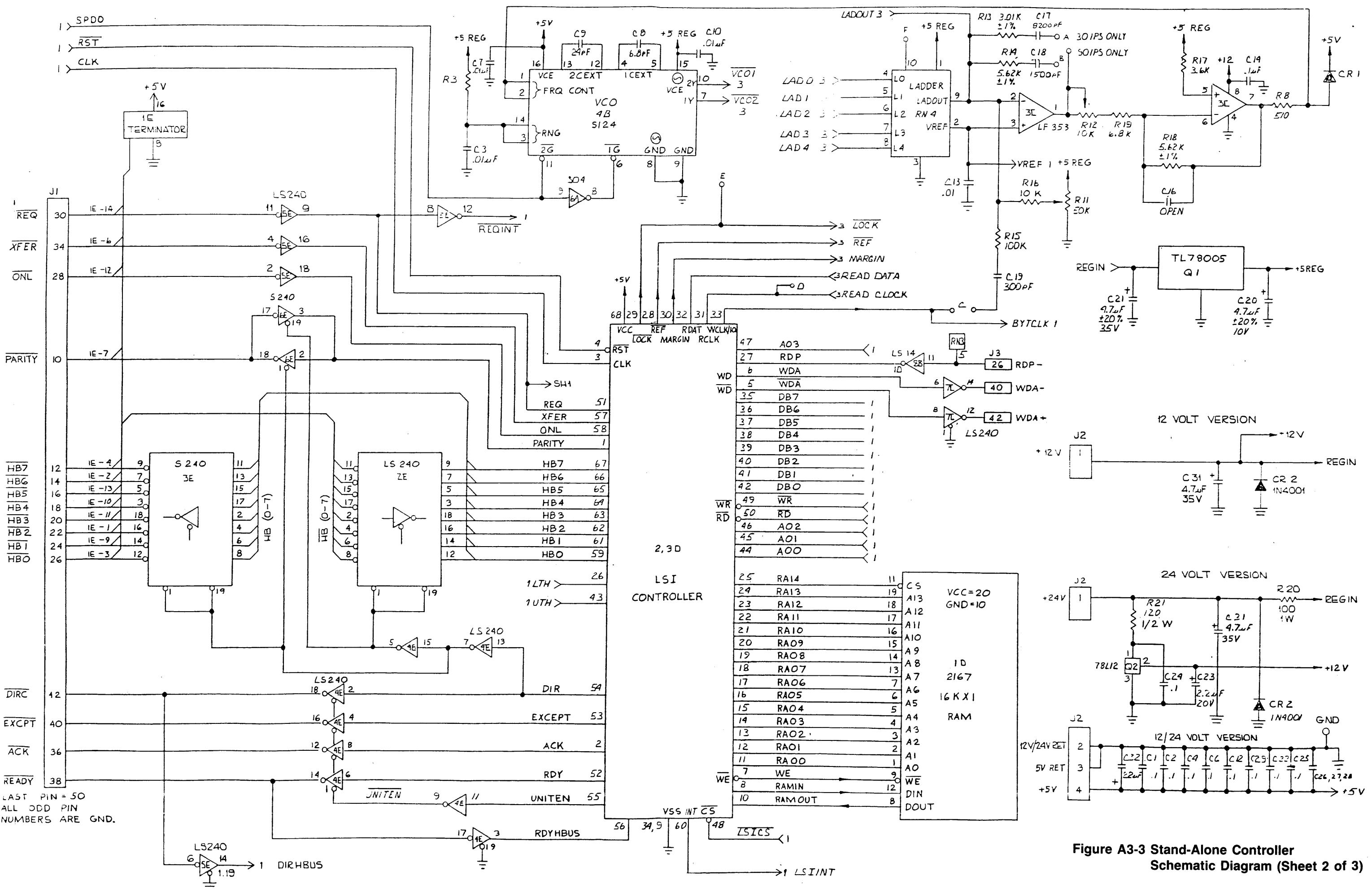


Figure A3-3 Stand-Alone Controller
Schematic Diagram (Sheet 2 of 3)

