

Block diagram

A

A

B

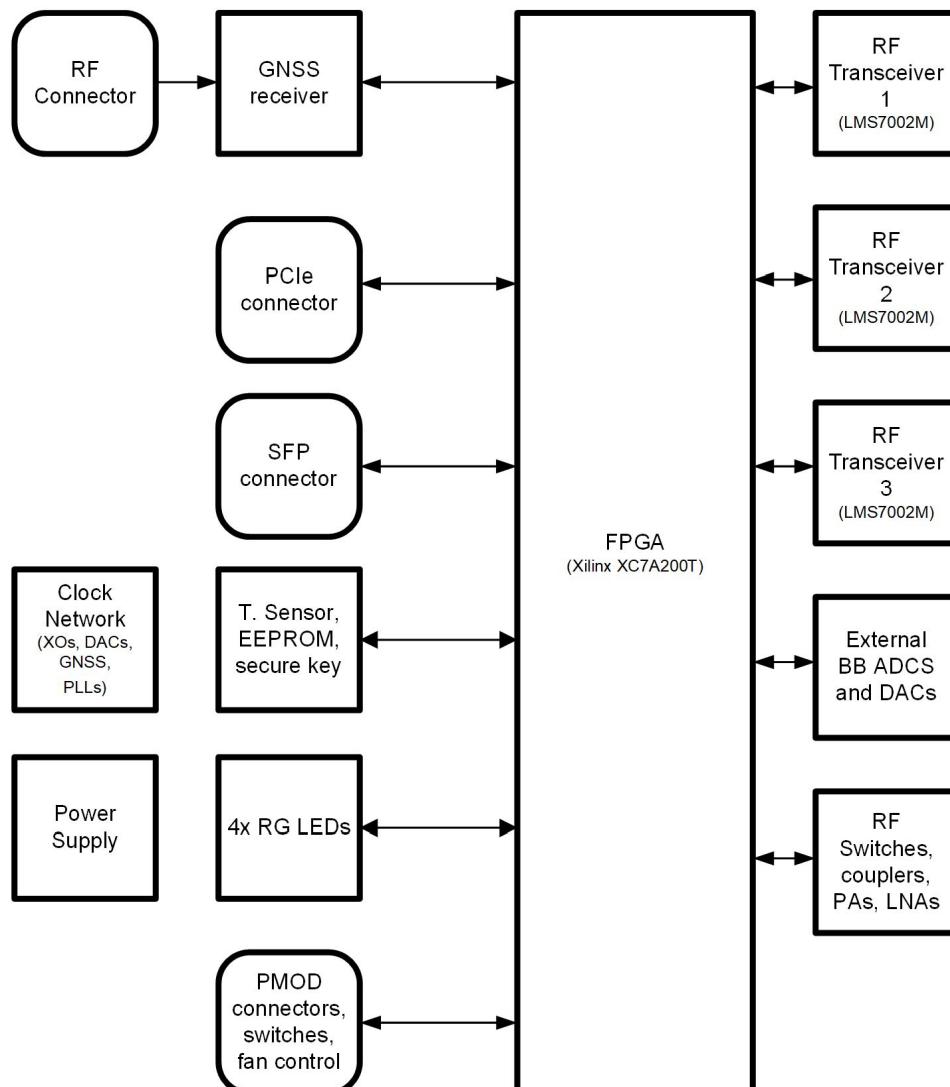
B

C

C

D

D



Project name: **LimeSDR-X3_1v0.PnjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.0**

Date: **2022-12-19** Time: **12:43:46** Sheet **1** of **31**

File: **01_BlockDiagram.SchDoc**

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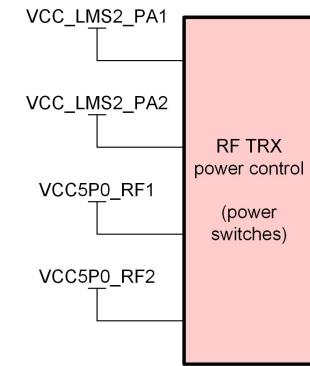
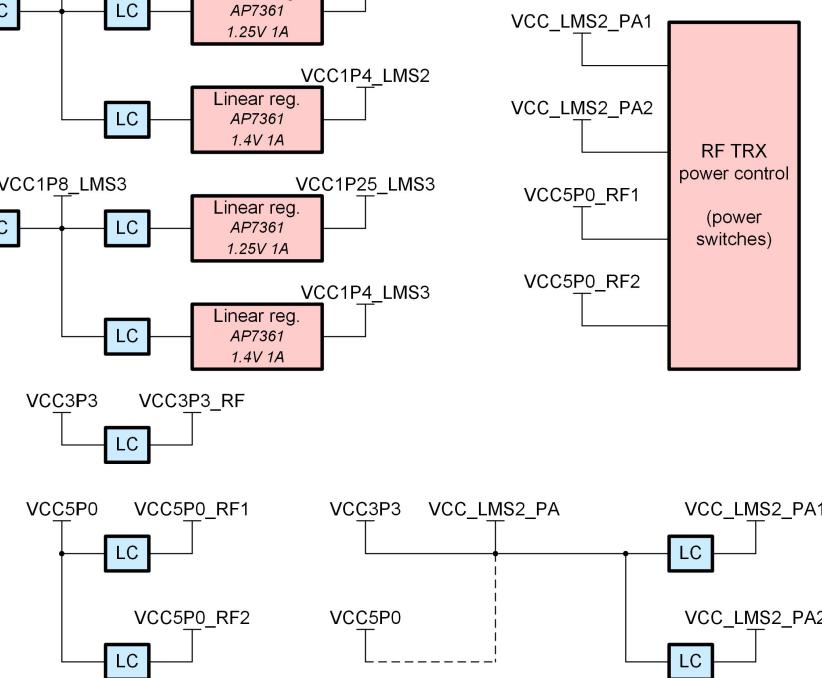
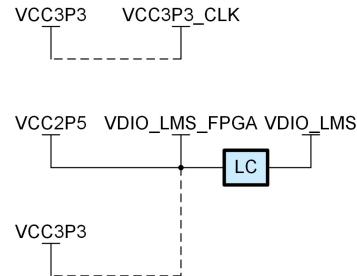
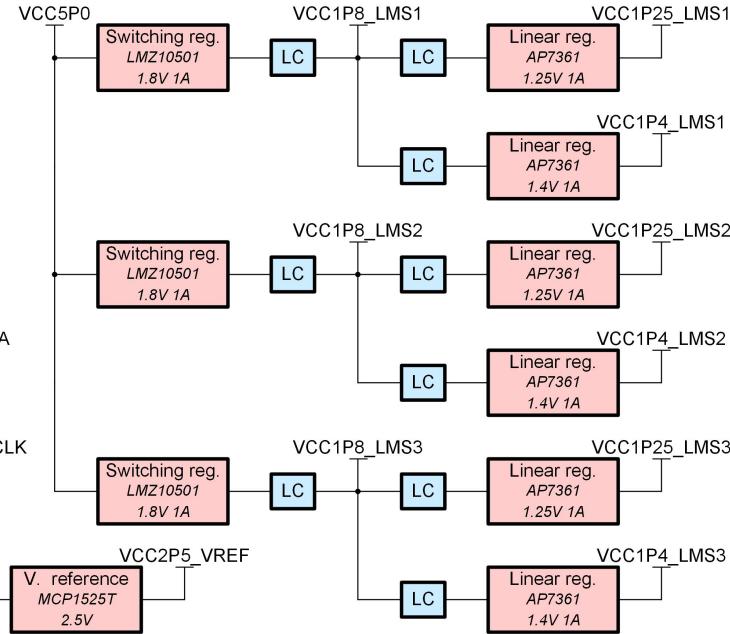
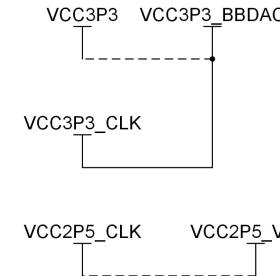
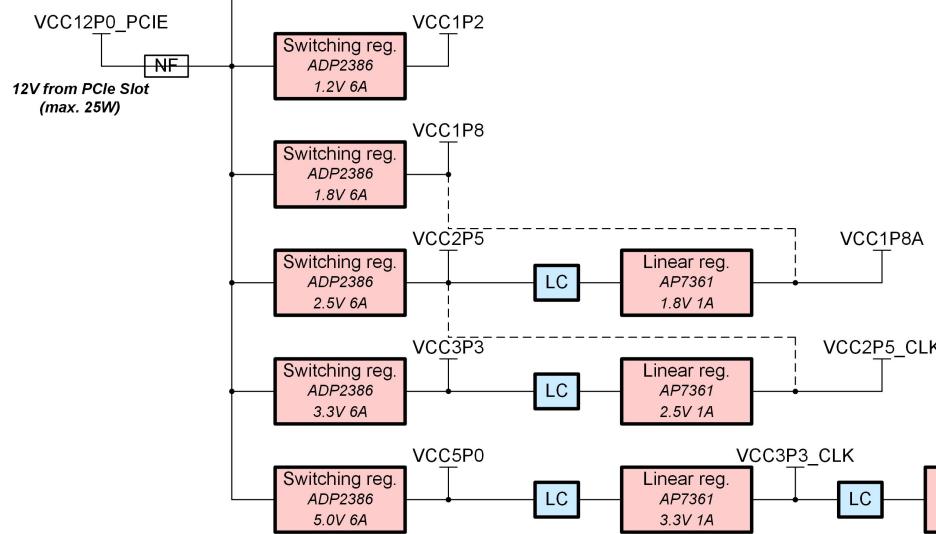
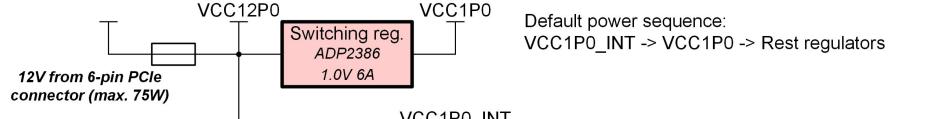
Power diagram

1

2

3

4



Project name: *LimeSDR-X3_1v0.PnjPcb*

Title: *Power diagram*

Size: **A4** Revision: **v1.0**

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File: 02_PowerDiagram.SchDoc United Kingdom



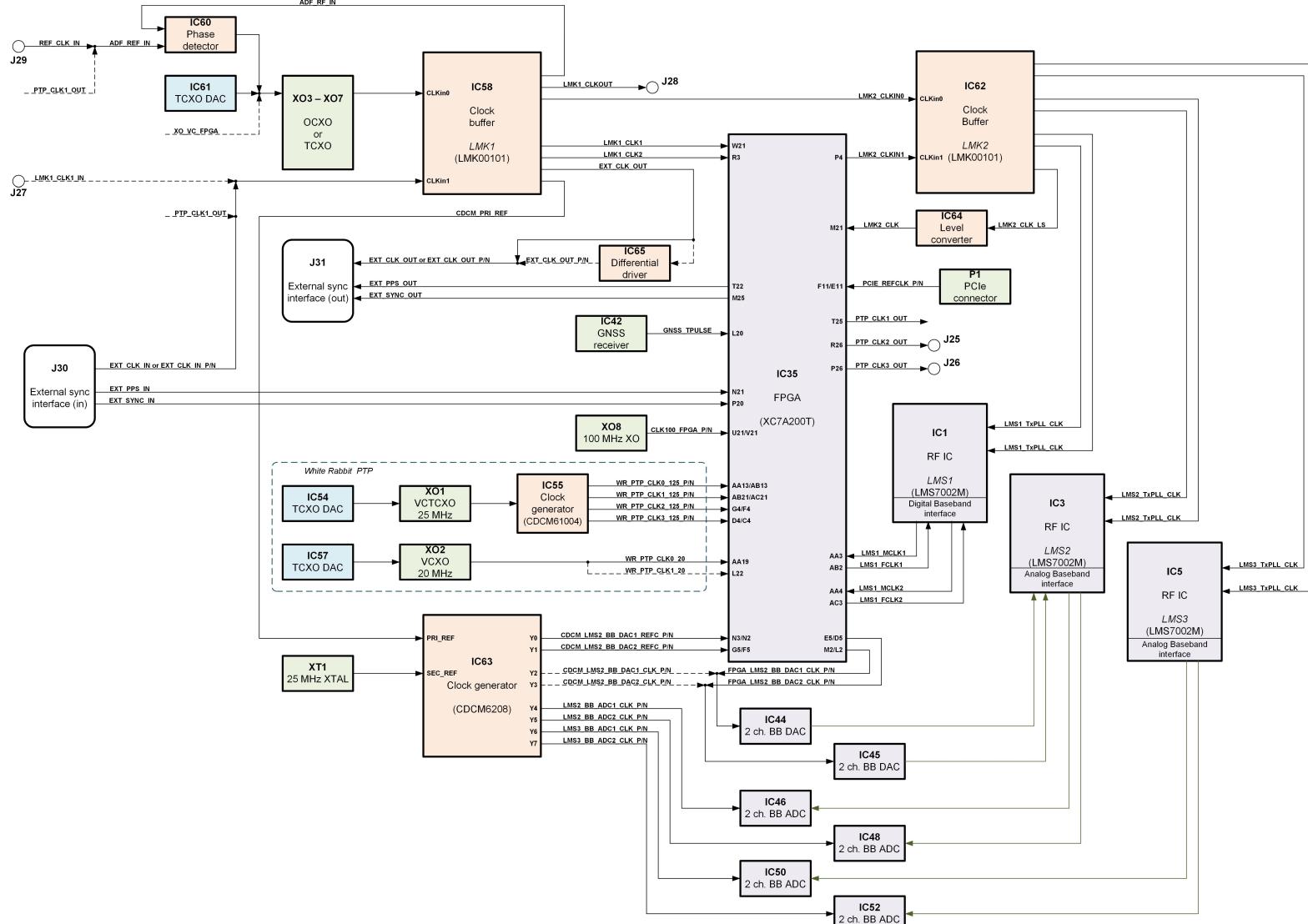
1

2

3

4

Clock diagram



Project name: **LimeSDR-X3_1v0.PnjPcb**

Title: **Clock diagram**

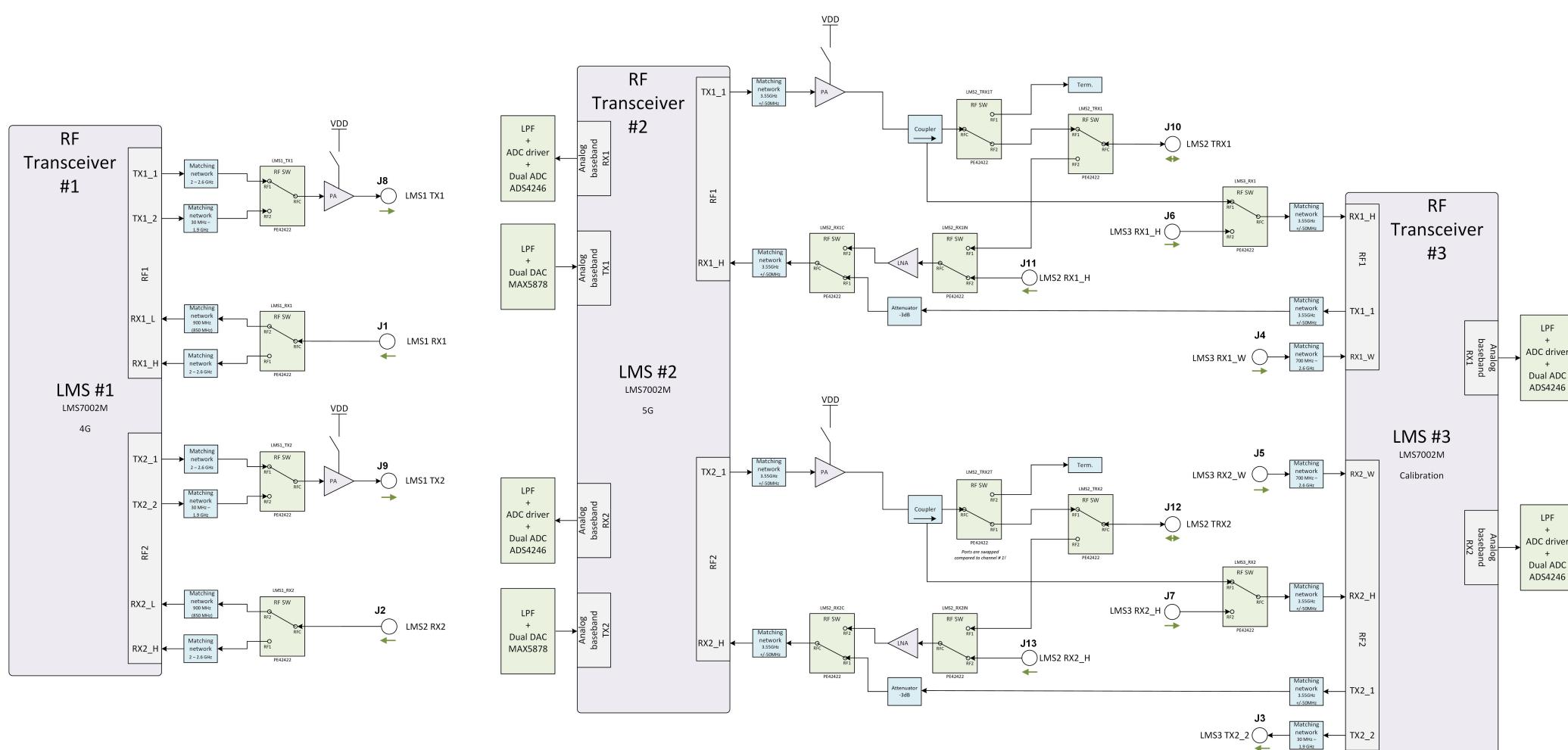
Size: **A4** Revision: **v1.0**

Date: **2022-12-19** Time: **12:44:07** Sheet**3** of **31**

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RF diagram



Project name: LimeSDR-X3 Rev0.PriPcb

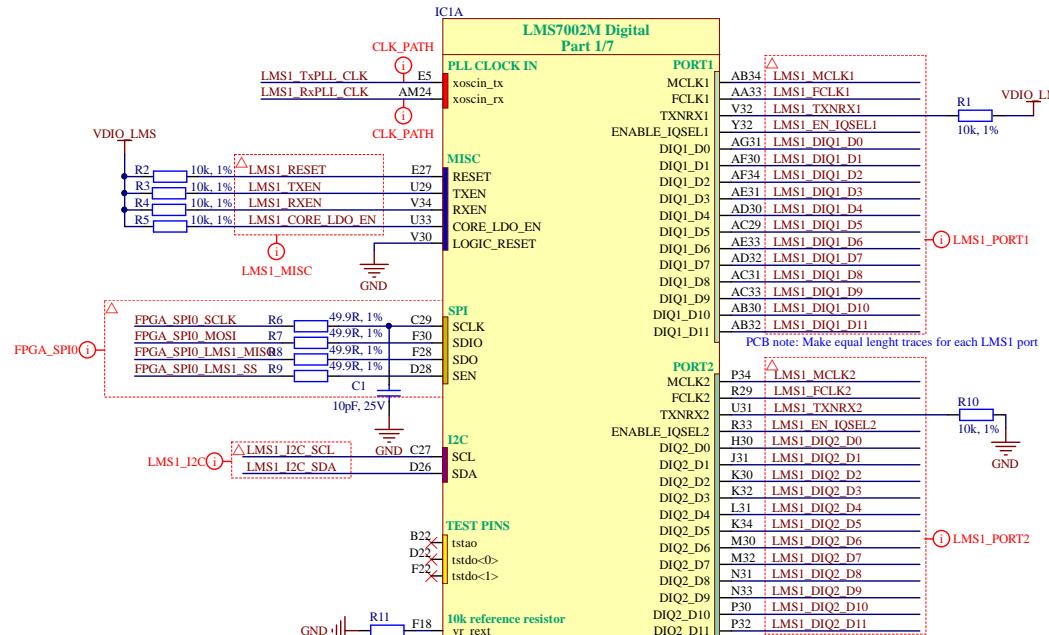
Title: RF diagram		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom	 Lime microsystems
Size: A4	Revision: v1.0		
Date: 2022-12-19	Time: 12:44:22	Sheet 4 of 31	
File: 04_RFDIagram.SchDoc			

NF elements on sheet: MECH15, MECH16, MECH17, MECH18
Number of NF elements on sheet: 4

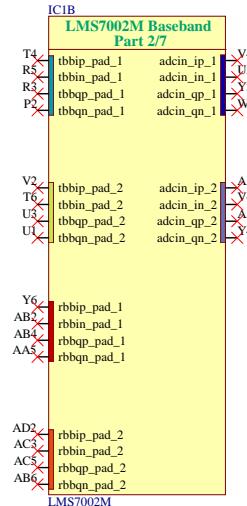
LMS7002M misc

LMS1_ (4G)

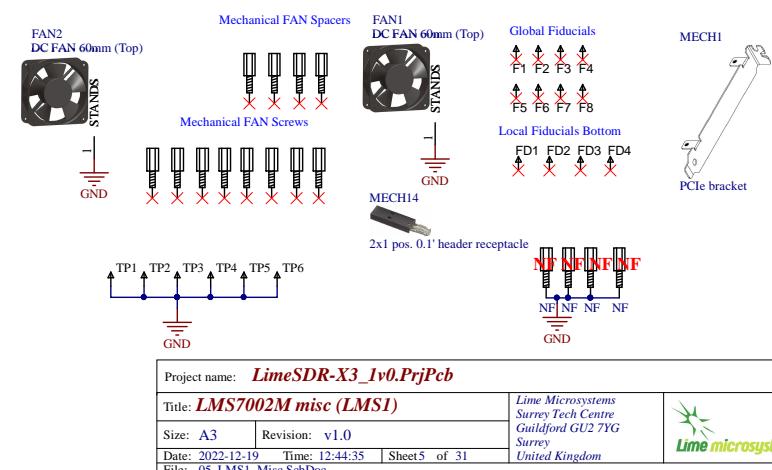
Digital interfaces



Baseband external IO



Mechanical

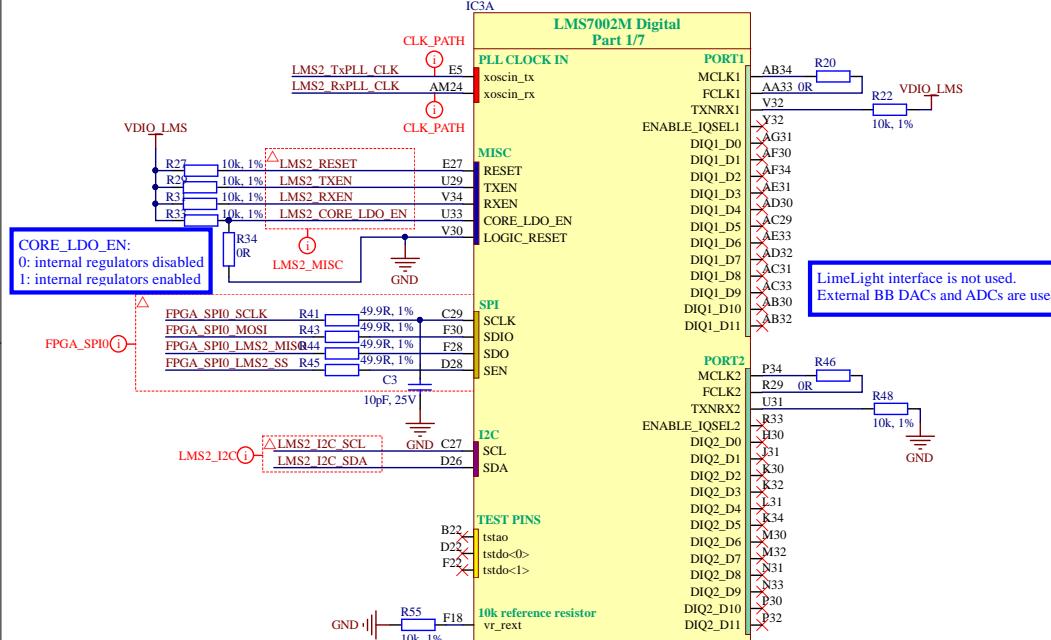


NF elements on sheet: -
Number of NF elements on sheet: 0

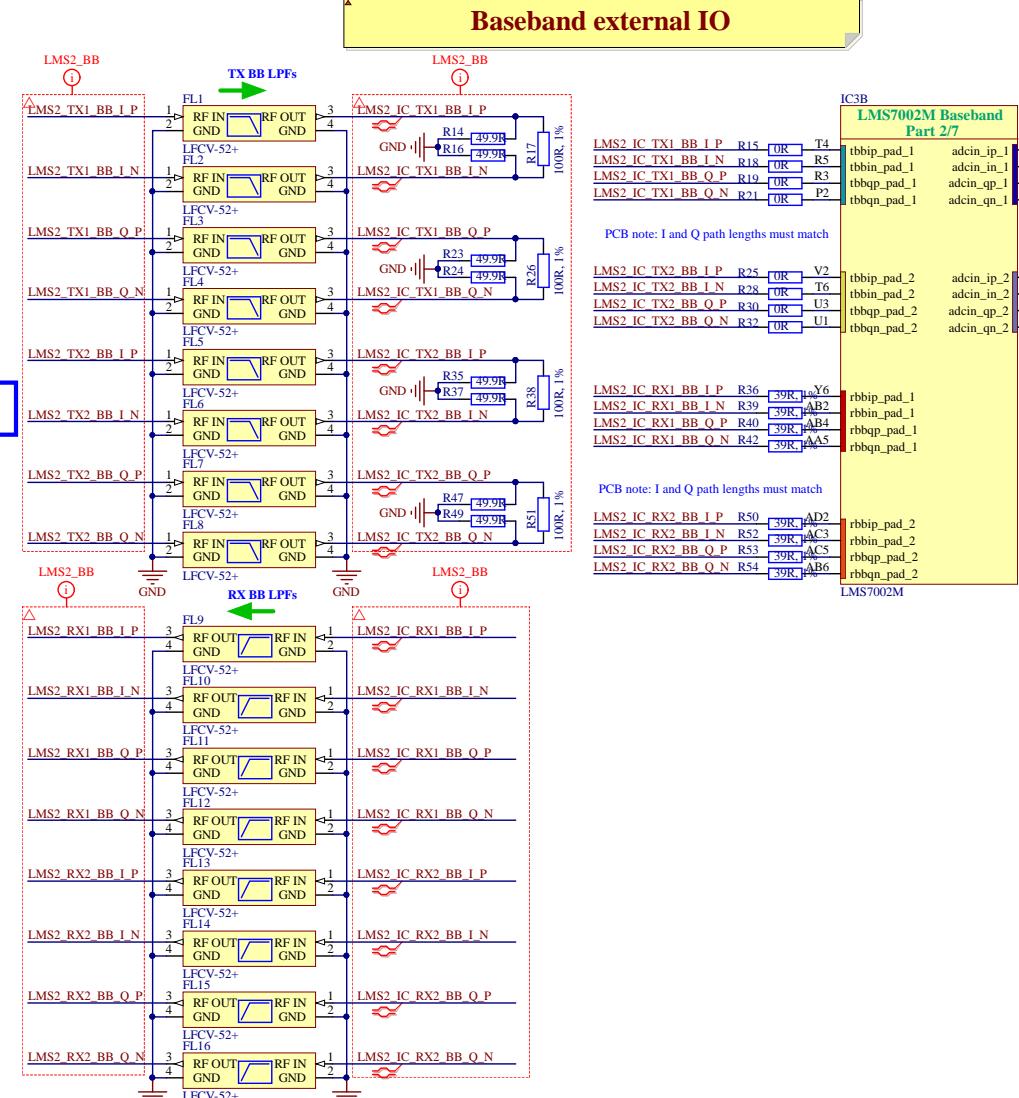
LMS7002M misc

LMS2_ (5G)

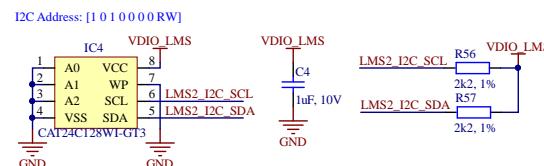
Digital interfaces



Baseband external IO



LMS2 EEPROM



Project name: LimeSDR-X3_Inv0.PrfPcb

Title: LMS7002M misc (LMS2)

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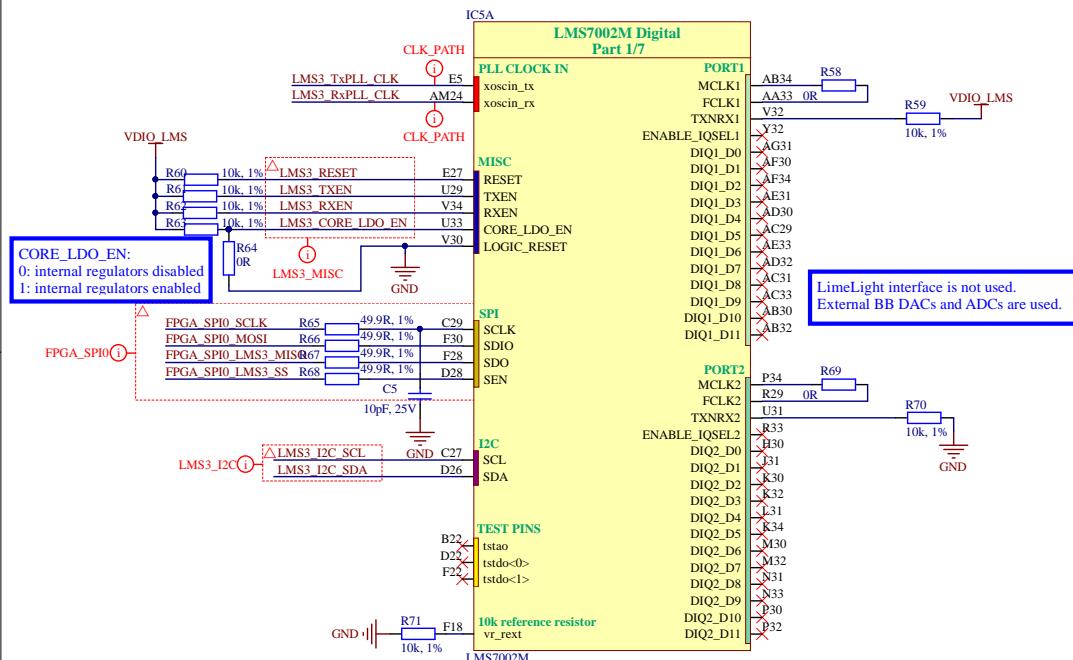
Size: A3 Revision: v1.0
Date: 2022-12-19 Time: 12:44:43 Sheet 6 of 31
File: 06 LMS2_Misc.SchDoc

NF elements on sheet: -
Number of NF elements on sheet: 0

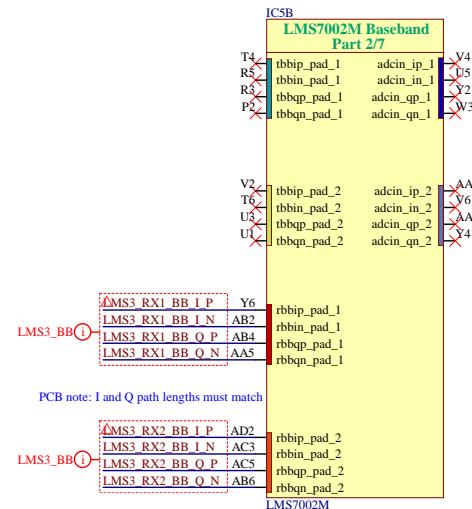
LMS7002M misc

LMS3_ (Calibration)

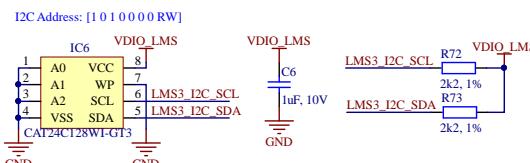
Digital interfaces



Baseband external IO



LMS3 EEPROM



Project name: LimeSDR-X3_Inv0.PrfPcb

Title: LMS7002M misc (LMS1)

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Size: A3 Revision: v1.0

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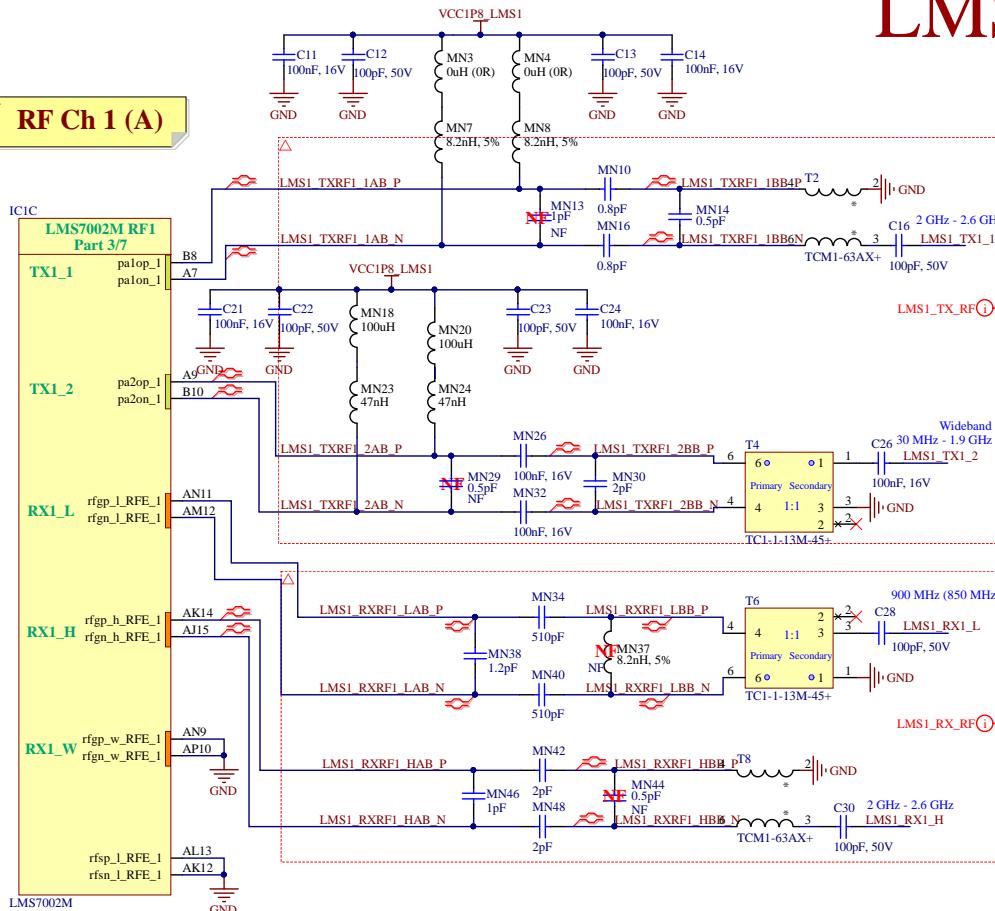
File: 07_LMS3_Misc.SchDoc

NF elements on sheet: MN11, MN13, MN27, MN29, MN35, MN37, MN43, MN44, ESD1, ESD2
Number of NF elements on sheet: 10

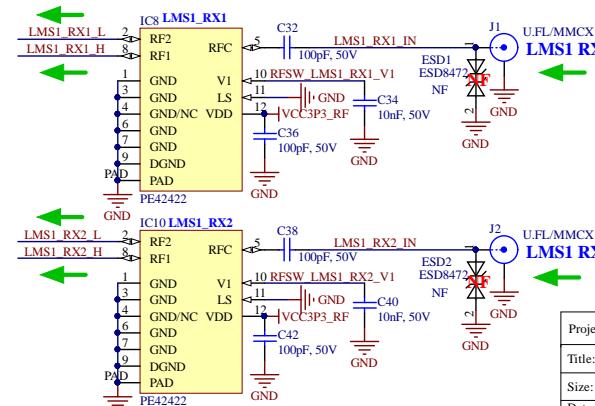
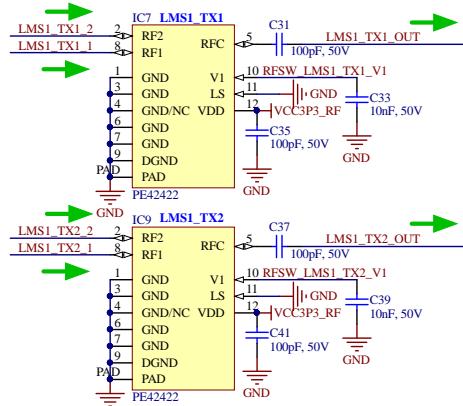
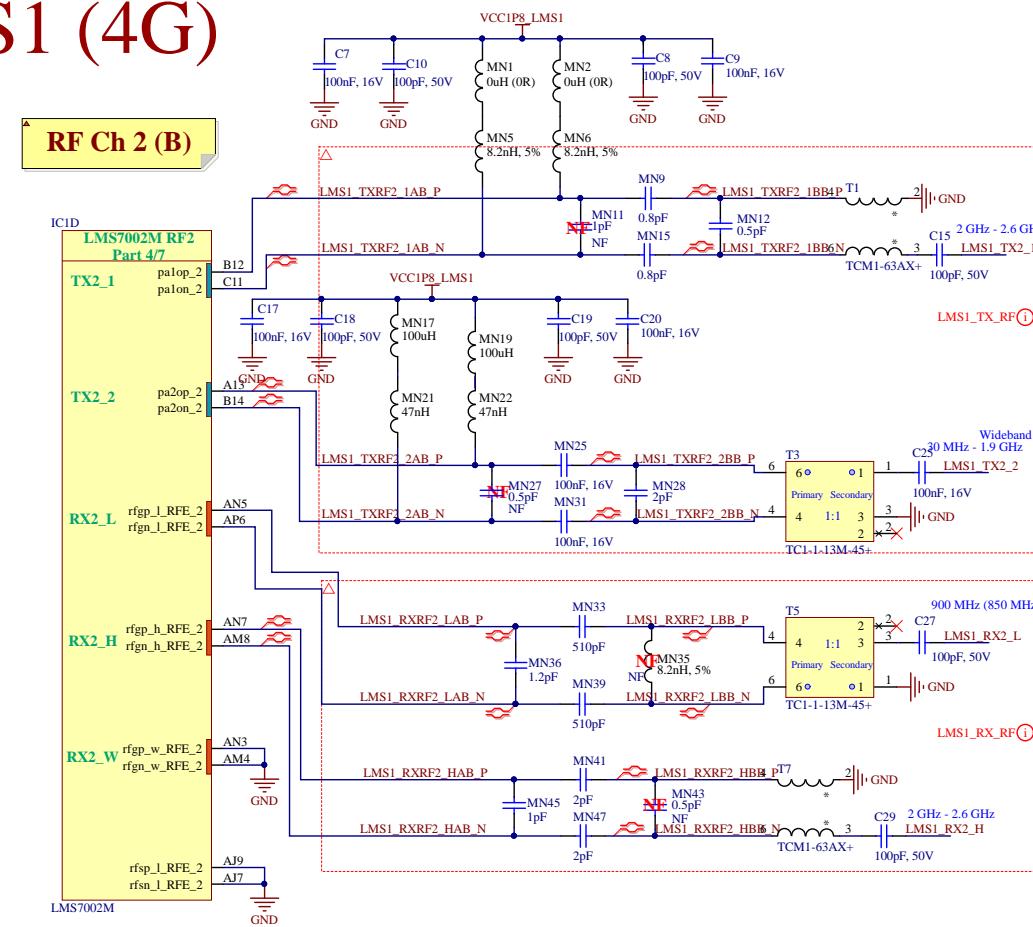
LMS7002M RF circuits (LMS1)

LMS1 (4G)

RF Ch 1 (A)



RF Ch 2 (B)



Project name: LimeSDR-X3_Iv0.PnjPcb

Title: LMS7002M RF (LMS1)

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Size: A3 Revision: v1.0

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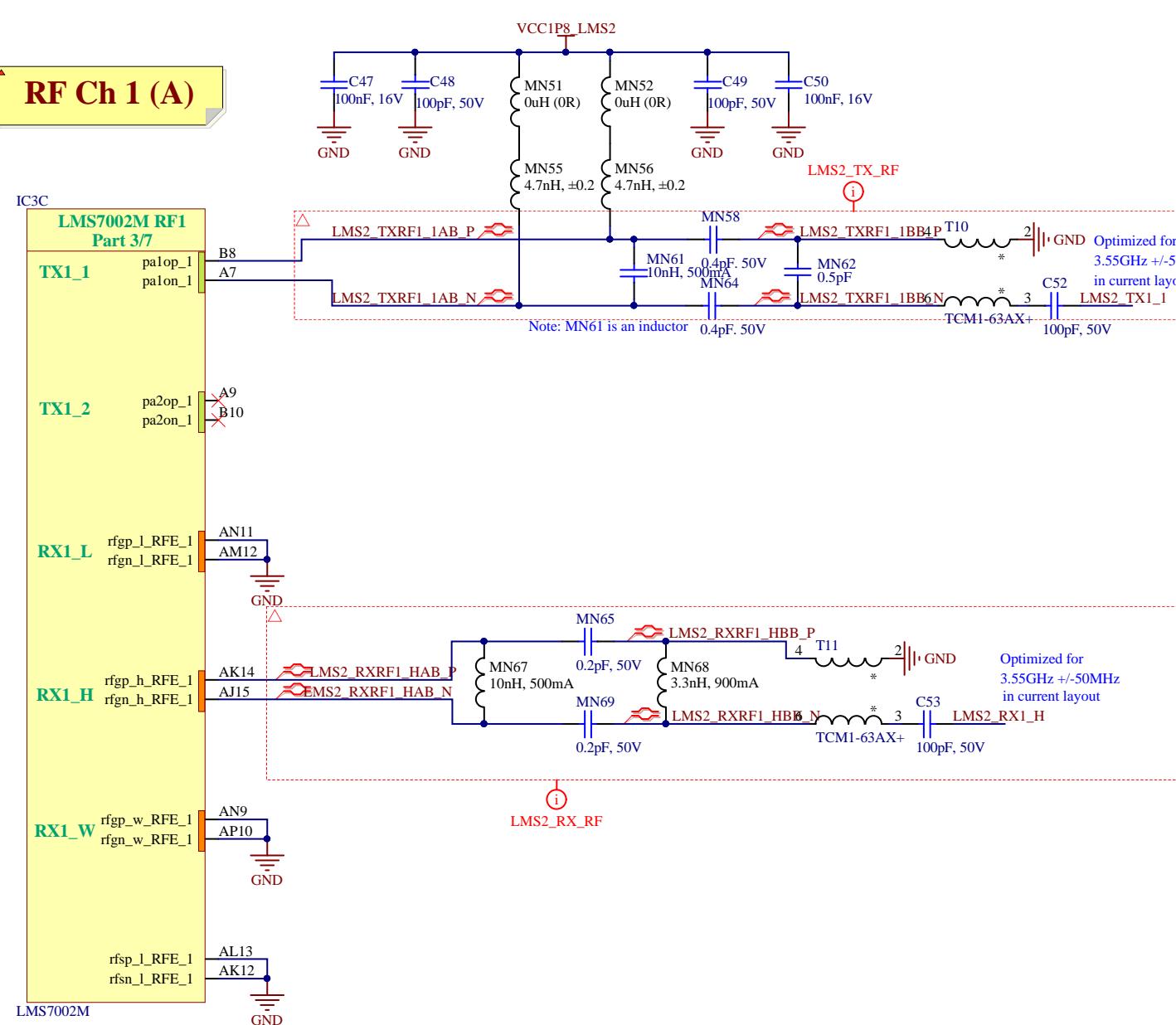
File: 08 LMS1_RF.SchDoc

NF elements on sheet: -
Number of NF elements on sheet: 0

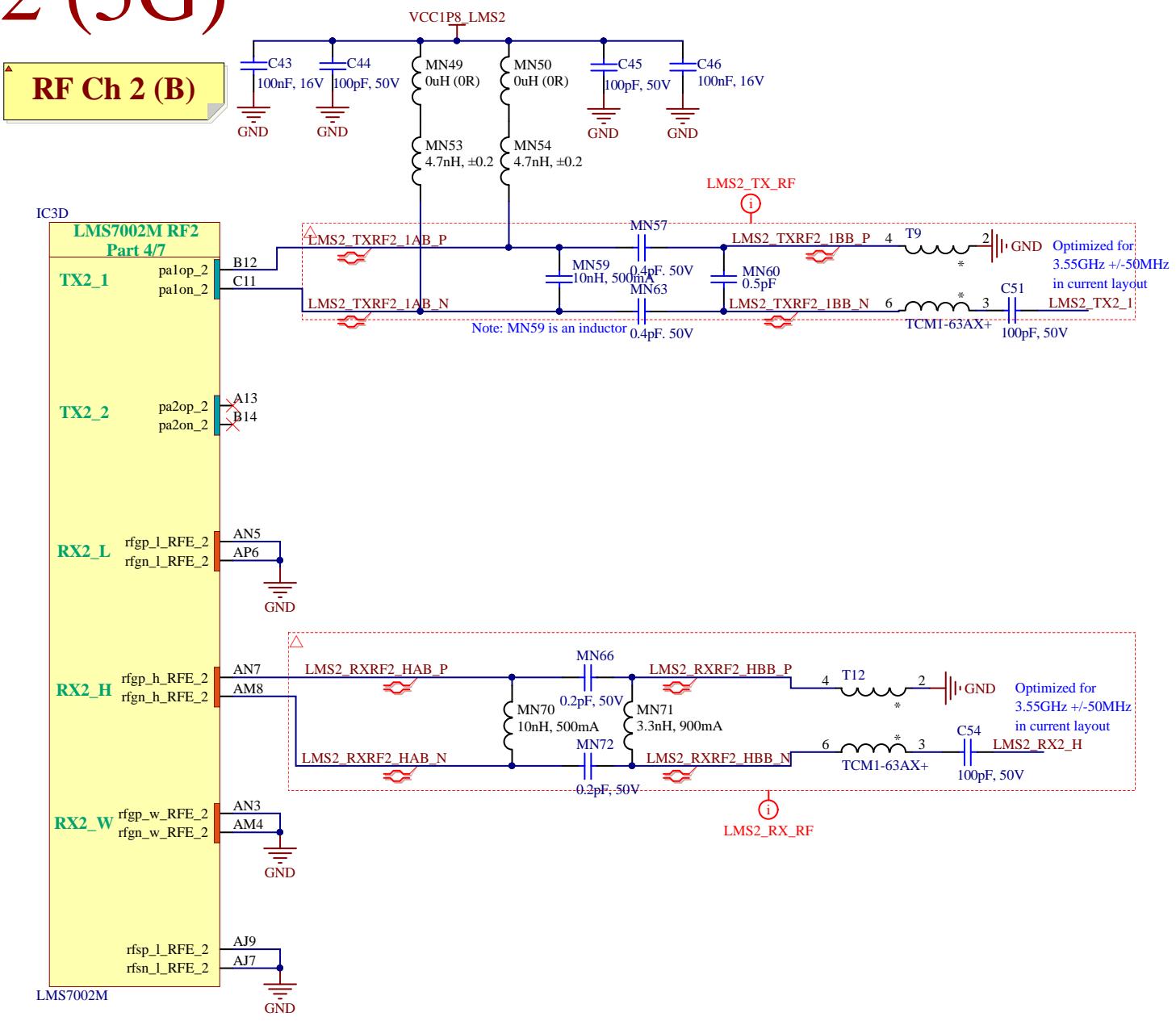
LMS7002M RF circuits (LMS2)

LMS2 (5G)

RF Ch 1 (A)



RF Ch 2 (B)



Project name: LimeSDR-X3_1v0.PrjPcb

Title: LMS7002M RF (LMS2)

Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:45:07 Sheet 9 of 31

File: 09_LMS2_RF.SchDoc

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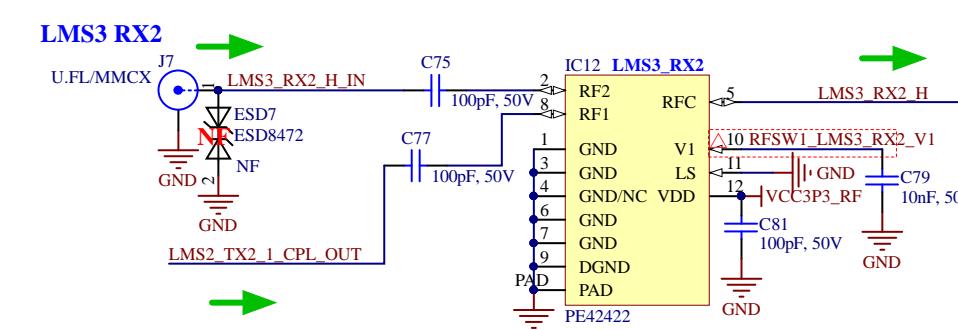
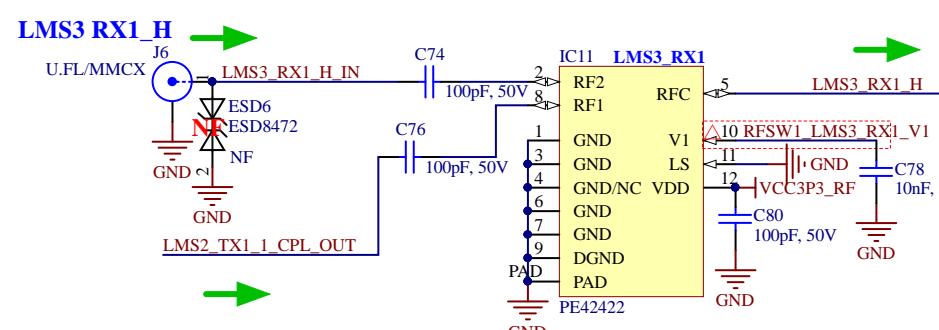
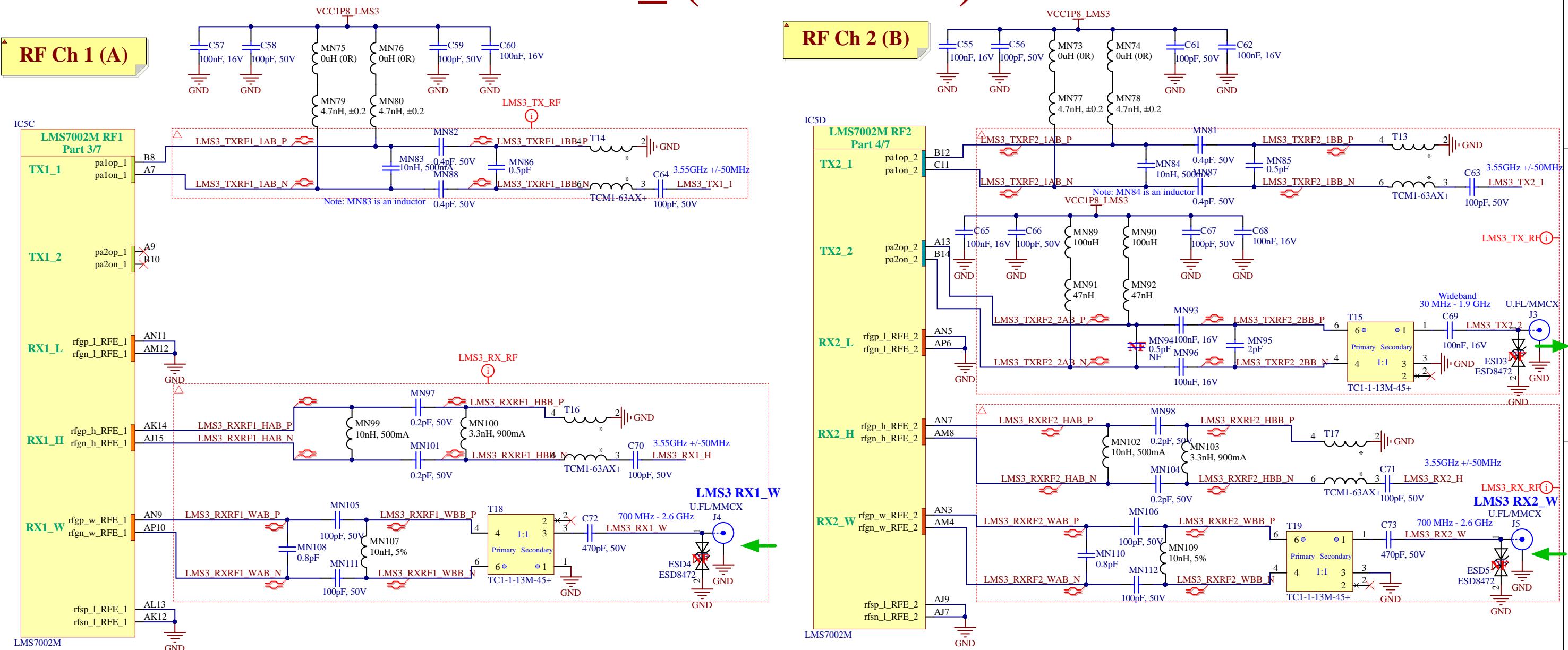


NF elements on sheet: MN94, ESD3, ESD4, ESD5, ESD6, ESD7

Number of NF elements on sheet: 6

LMS7002M RF circuits (LMS3)

LMS3_ (Calibration)



Project name: LimeSDR-X3_1v0.PrjPcb

Title: LMS7002M RF (LMS3)

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Size: A3 Revision: v1.0

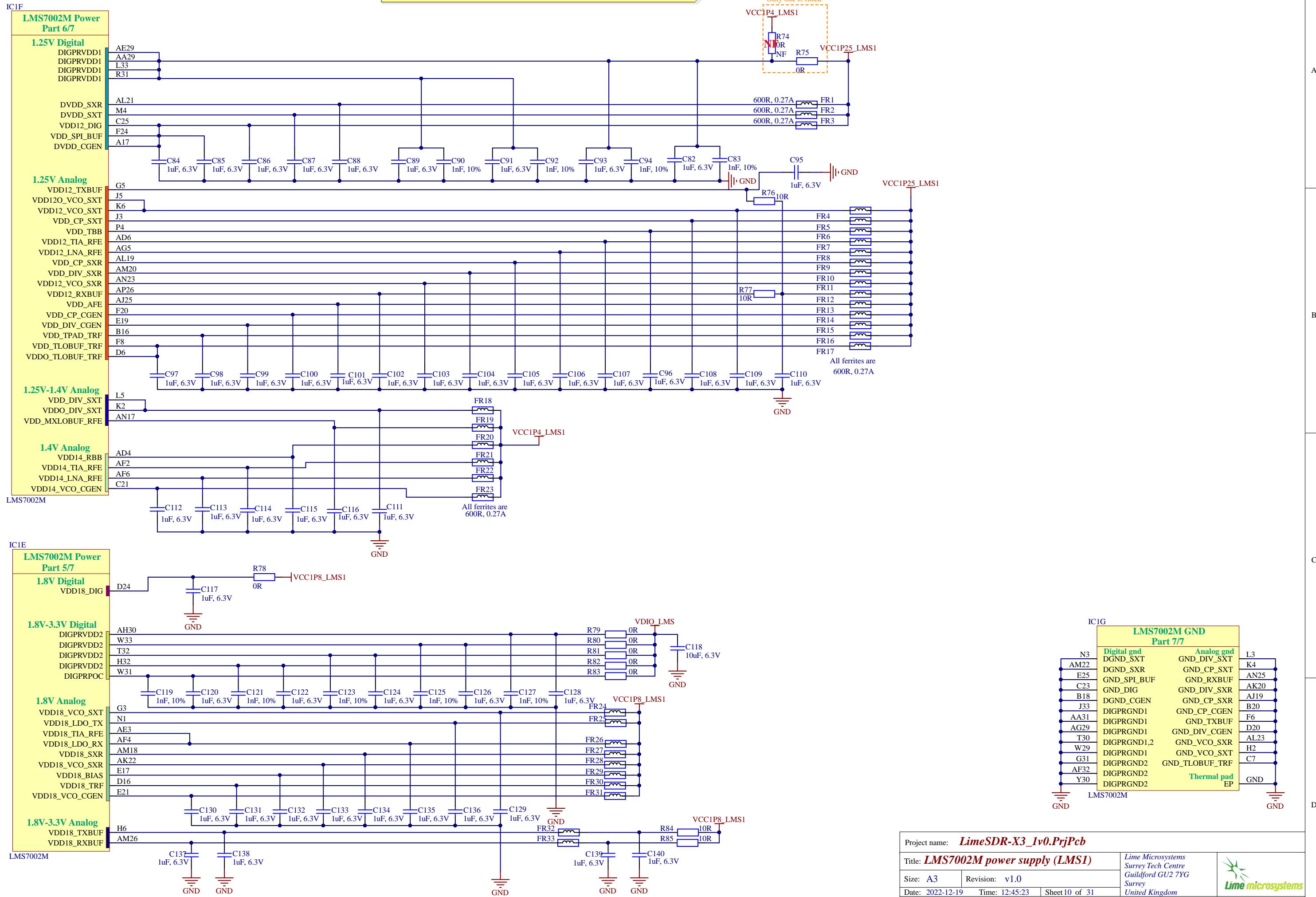
Date: 2022-12-19 Time: 12:45:15 Sheet 10 of 31

File: 10_LMS3_RF.SchDoc



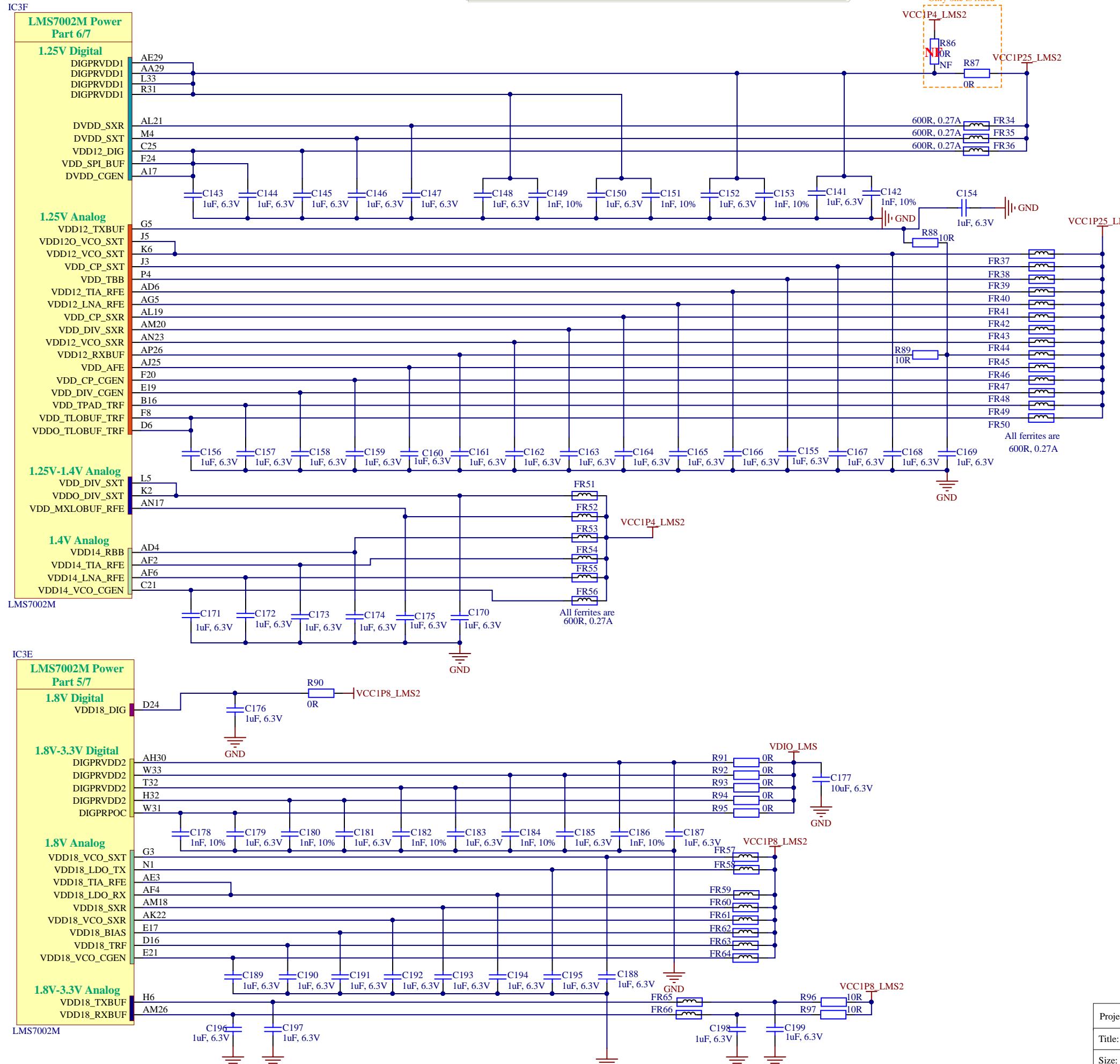
NF elements on sheet: R74
Number of NF elements on sheet: 1

LMS7002M power supply circuit (LMS1)



NF elements on sheet: R86
Number of NF elements on sheet: 1

LMS7002M power supply circuit (LMS2)



Project name: LimeSDR-X3_1v0.PrbPcb

Title: LMS7002M power supply (LMS2)

Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:45:31 Sheet 10 of 31

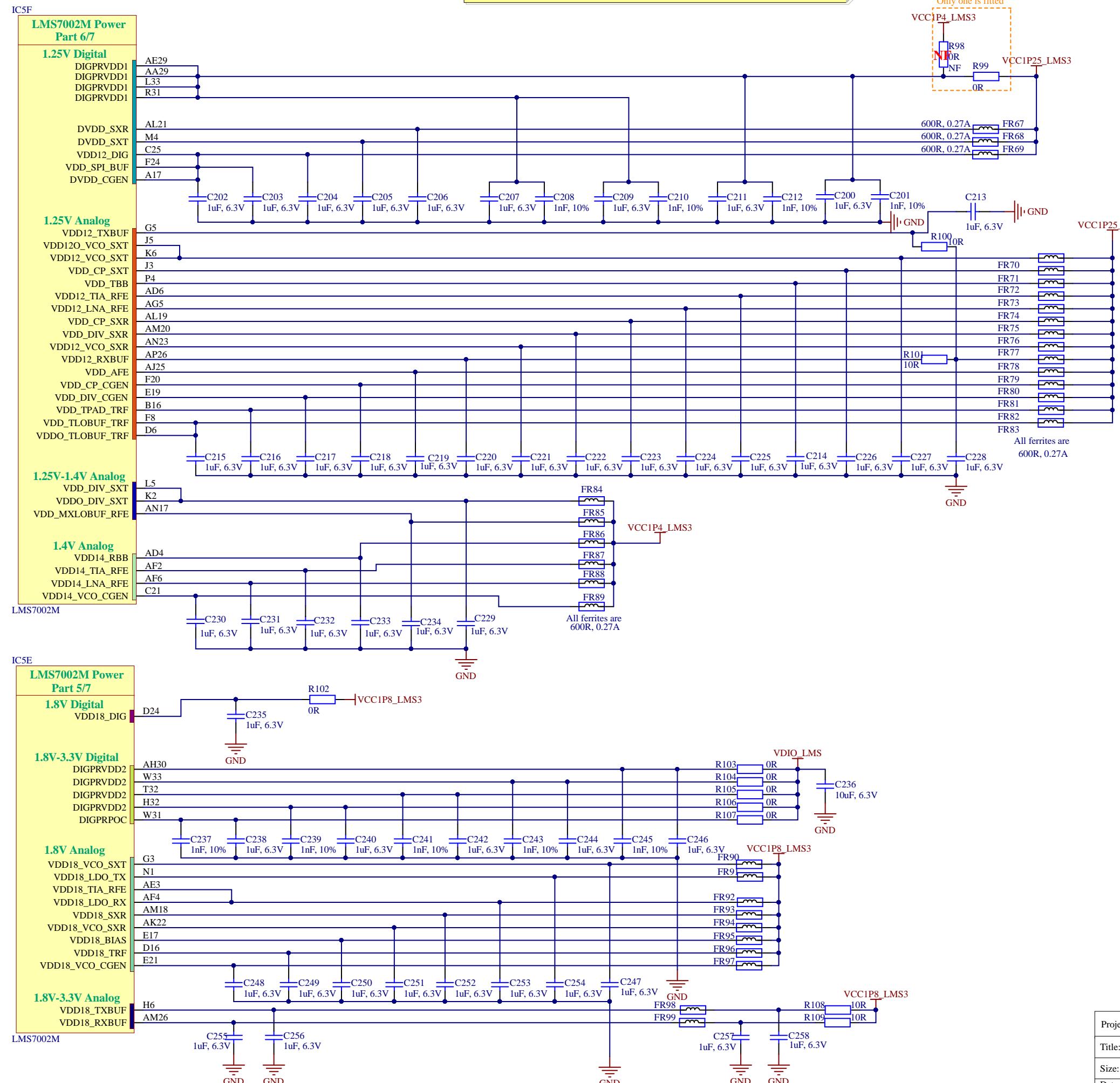
File: 12_LMS2_Power.SchDoc

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NF elements on sheet: R98
Number of NF elements on sheet: 1

LMS7002M power supply circuit (LMS3)



Project name: LimeSDR-X3_1v0.PrbPcb

Title: LMS7002M power supply (LMS3)

Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:45:39 Sheet 10 of 31

File: 13_LMS3_Power.SchDoc

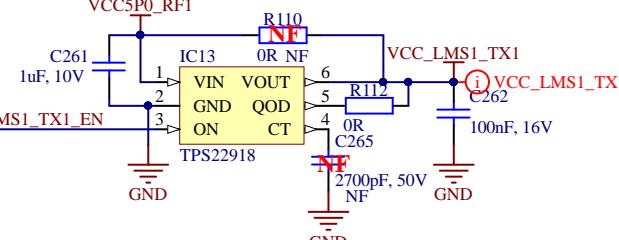
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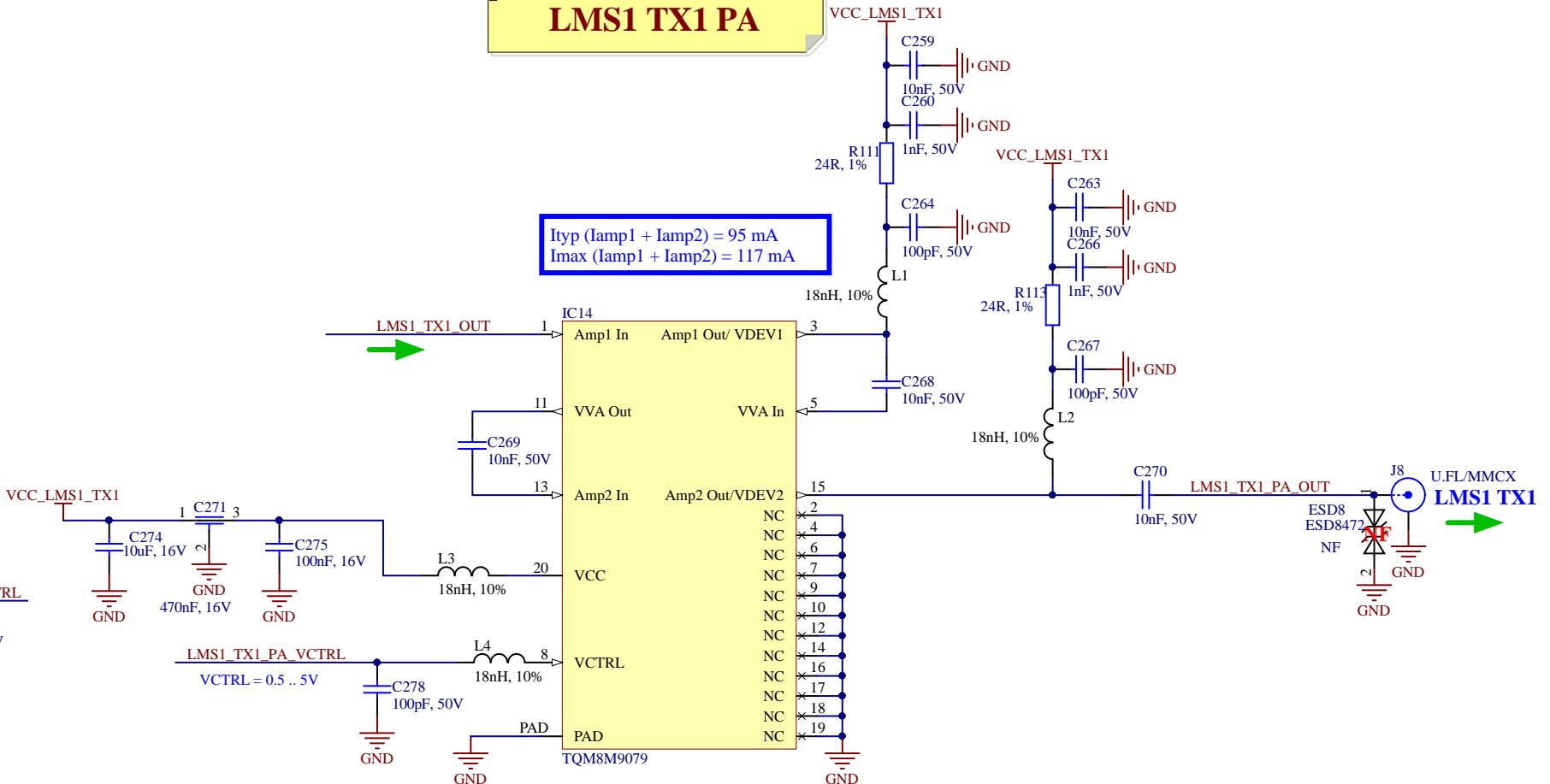
NF elements on sheet: R110, C265, R114, R118, C276, ESD8, R122, C286, R126, R130, C297, ESD9
Number of NF elements on sheet: 12

LMS1 RF PA

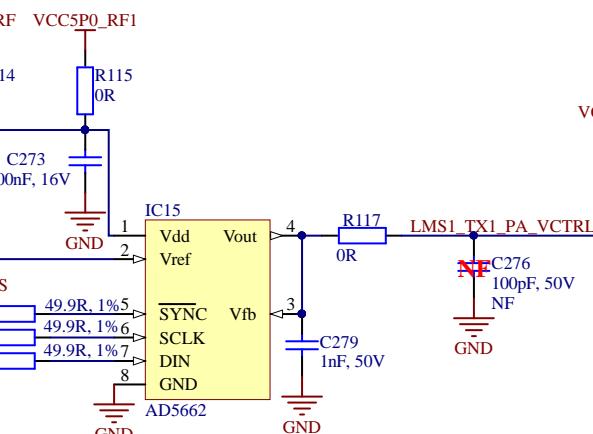
PA power control



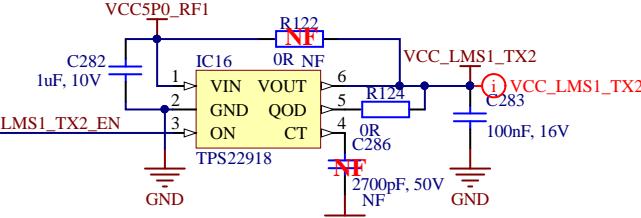
LMS1 TX1 PA



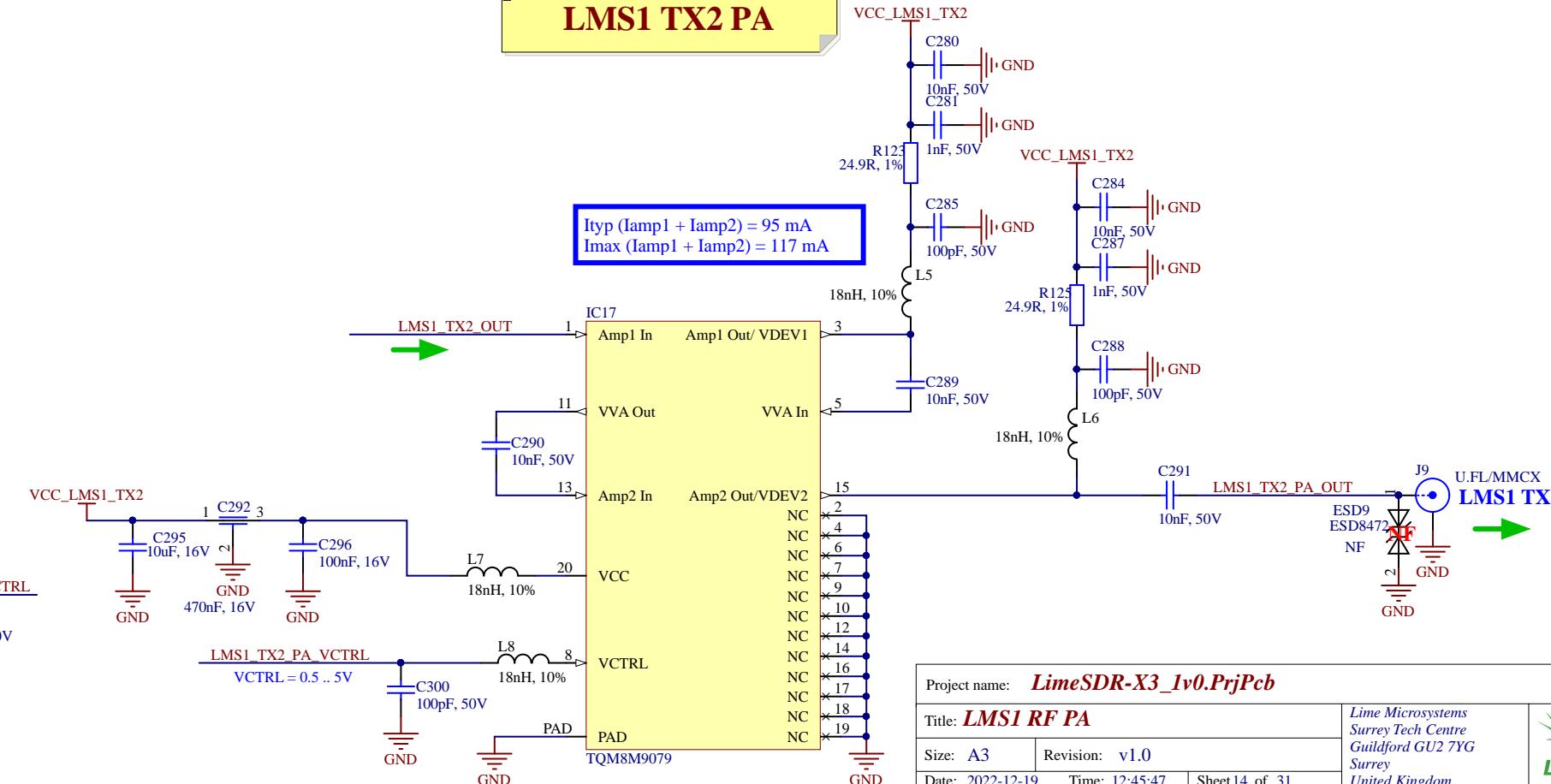
Voltage variable attenuator (VVA) DAC



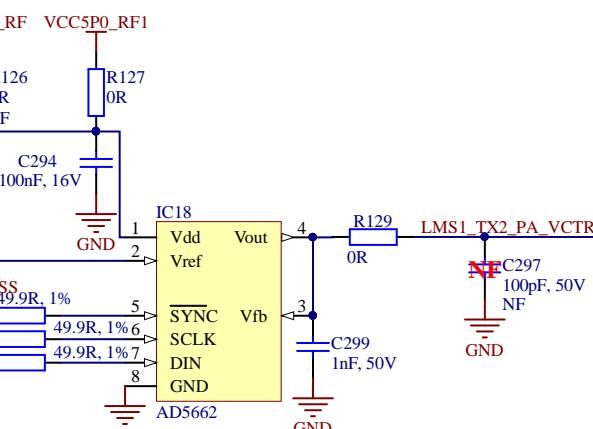
PA power control



LMS1 TX2 PA



Voltage variable attenuator (VVA) DAC



Project name: LimeSDR-X3_1v0.PrbPcb

Title: LMS1 RF PA

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Size: A3

Revision: v1.0

Date: 2022-12-19 Time: 12:45:47 Sheet 14 of 31

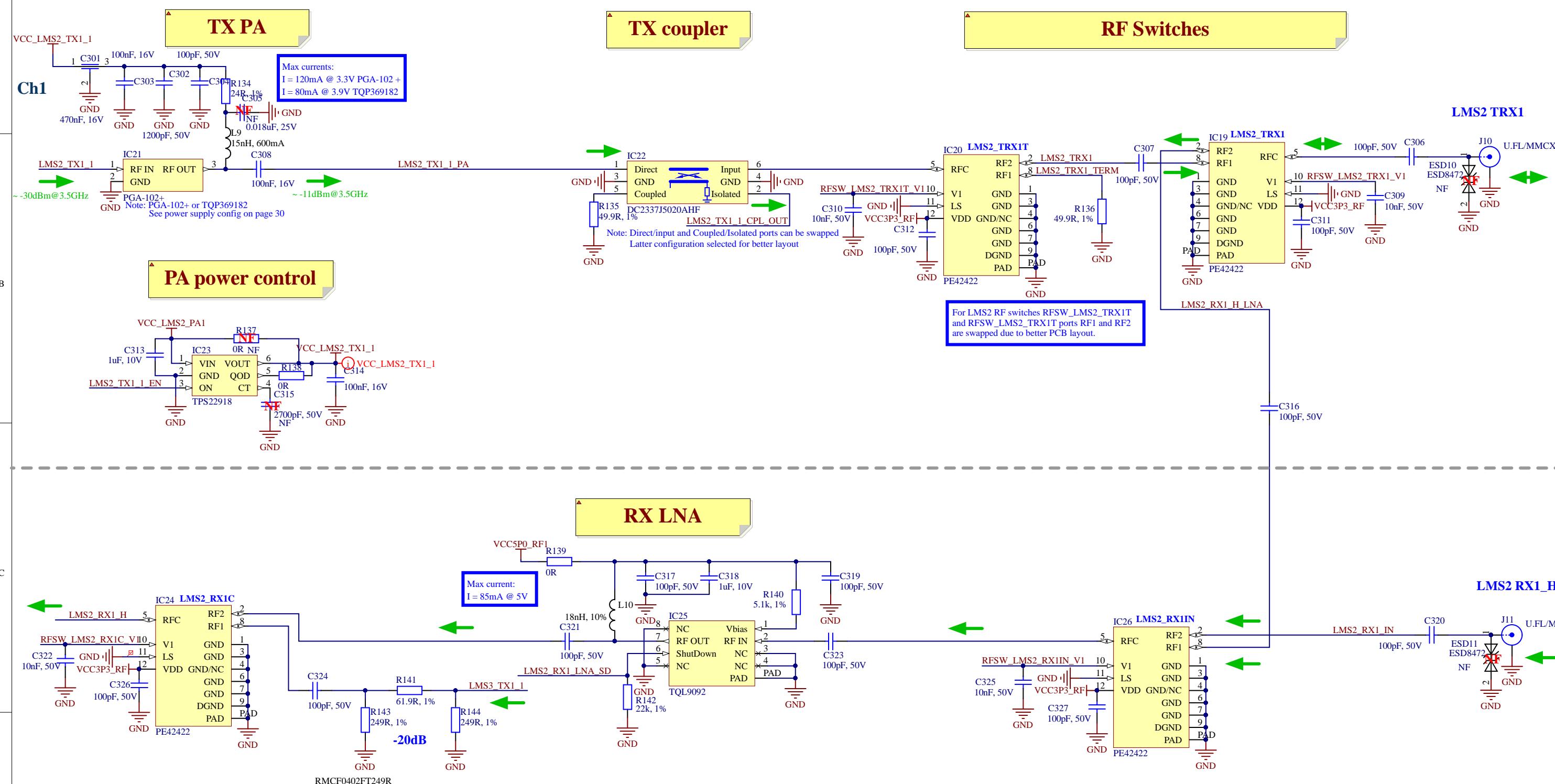
File: 14 LMS1_RF_PA.SchDoc



NF elements on sheet: C305, ESD10, R137, C315, ESD11

Number of NF elements on sheet: 3

LMS2 RF1 Mis



Lj - SDR V2.1.0.B.1B.1

The LMS2 RE1 Miss

Sign: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:45:54 Sheet 15 of 31

Date: 2022-12-15 Time: 12:45:54 Sheet 15 of 31
File: 15_LMS2_RF1_Misc.SchDoc

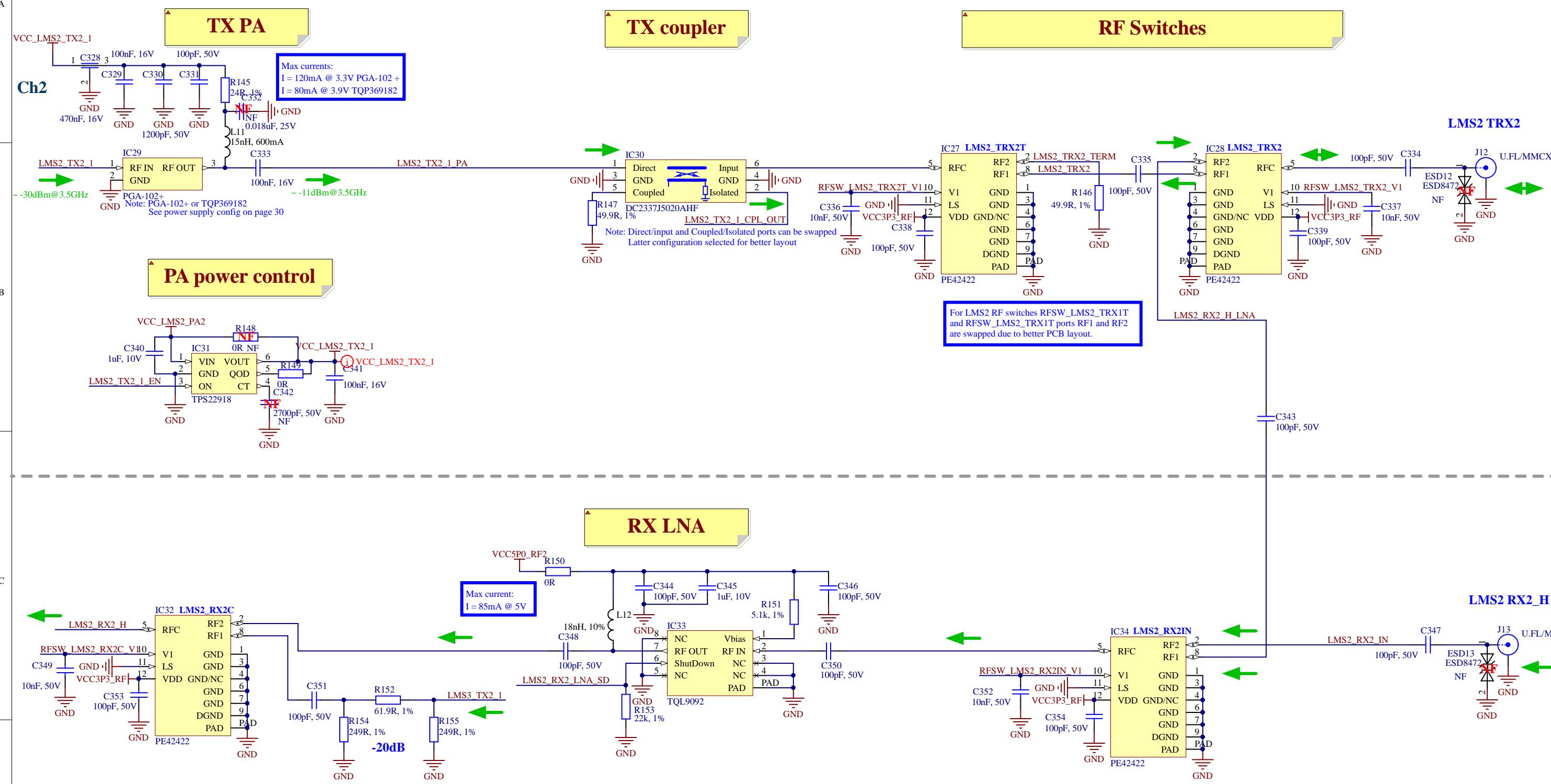
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NF elements on sheet: C332, ESD12, R148, C342, ESD13

Number of NF elements on sheet: 5

LMS2 RF2 Mis



NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA Banks 12, 13, 14, 15

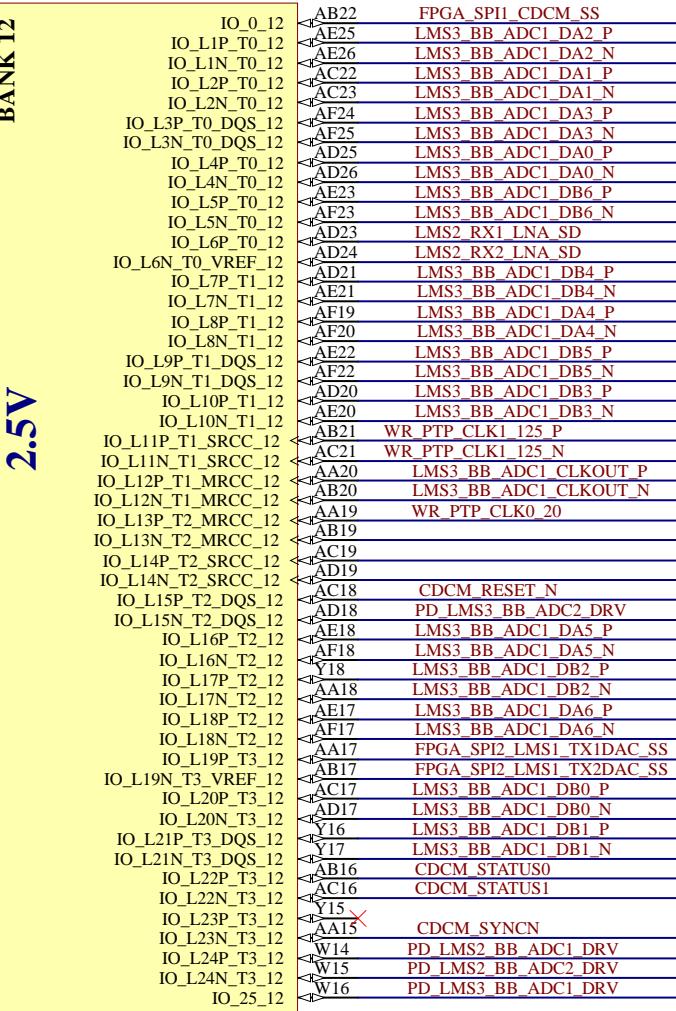
Board SPI interfaces:

FPGA_SPI0 (VDIO_LMS (default 2.5V)): LMS1, LMS2, LMS3

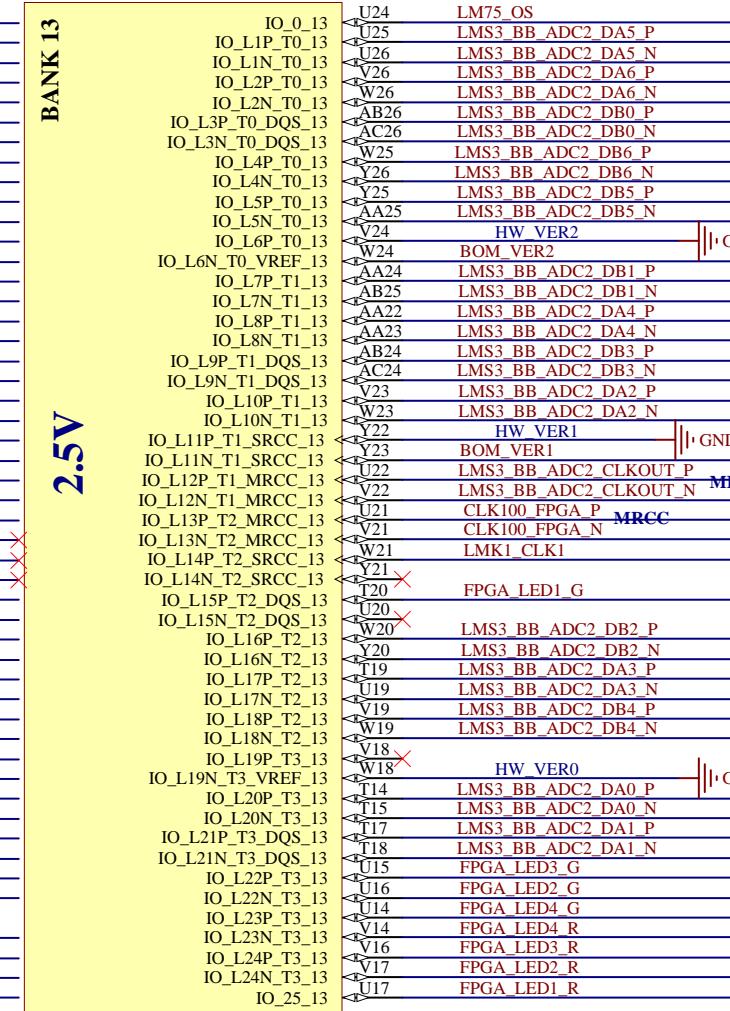
FPGA_SPI1 (2.5V): BB_ADC1, BB_ADC2, BB_ADC3, BB_ADC4, CDCM1, CDCM2

FPGA_SPI2 (2.5V): XO_DAC, XO_20_DAC, LMS1_TX1DAC, LMS1_TX2DAC, ADF

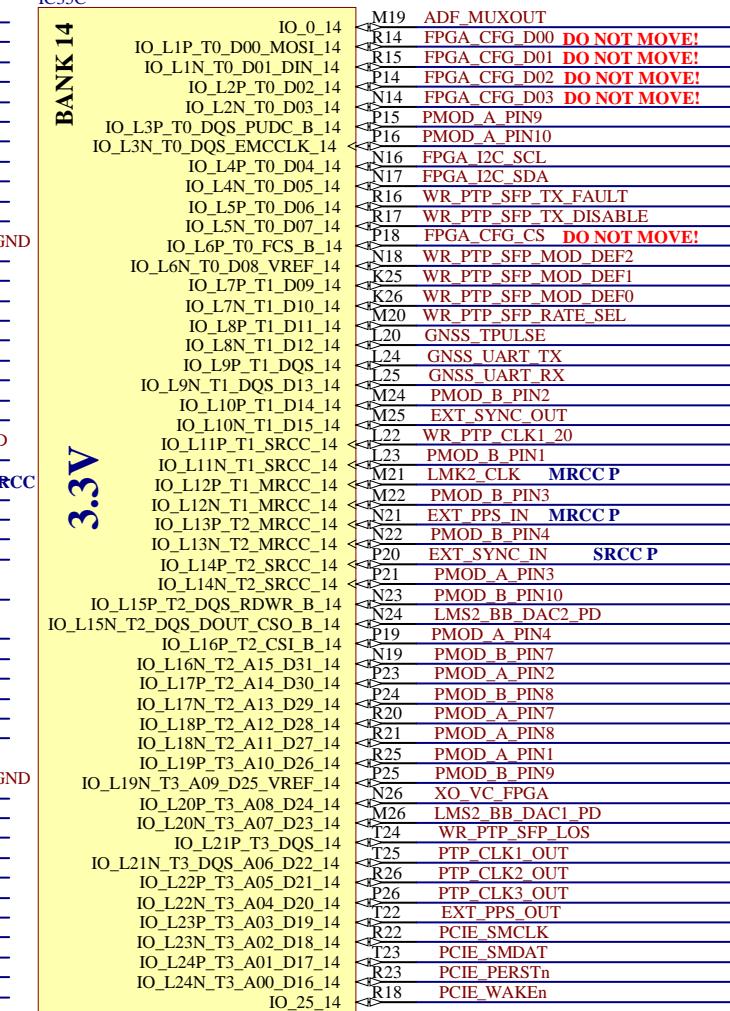
BANK 12



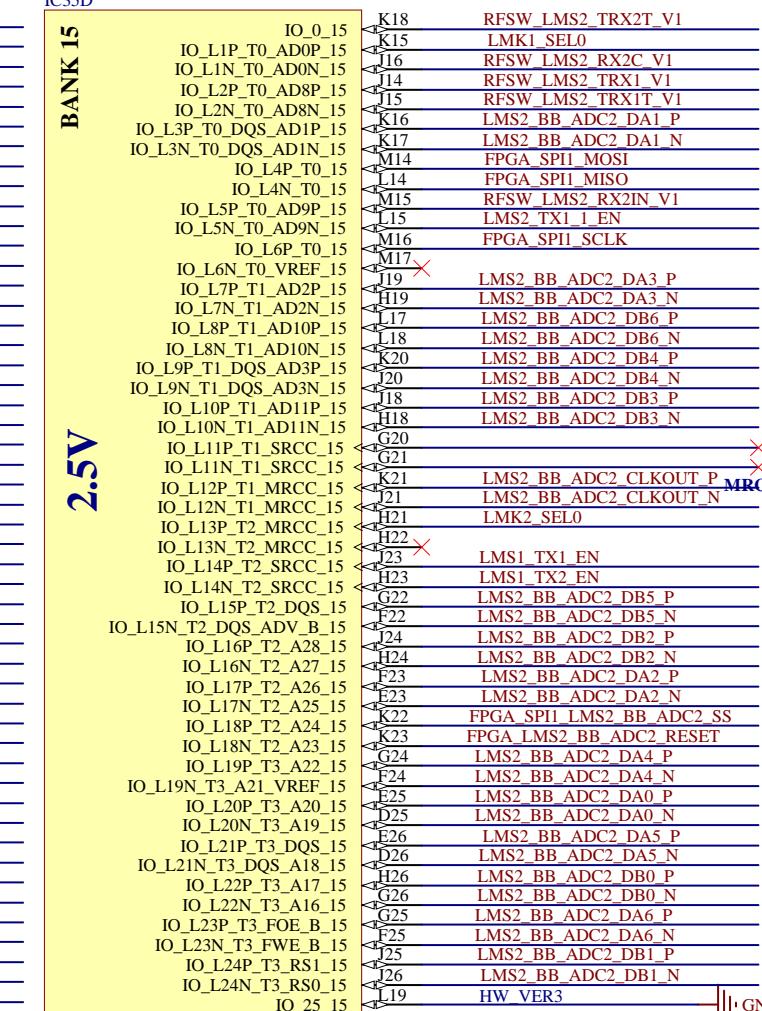
BANK 13



BANK 14



BANK 15



XC7A200T-2FBG676C

XC7A200T-2FBG676C

XC7A200T-2FBG676C

XC7A200T-2FBG676C

Project name: LimeSDR-X3_1v0.PrjPcb

Title: **FPGA Banks 12, 13, 14, 15**

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Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:46:10 Sheet 17 of 31

File: 17_FPGA_B12_B13_B14_B15.SchDoc

NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA Banks 16, 33, 34, 35

A

A

B

B

C

C

2.5V

C

XC7A200T-2FBG676C

BANK 16

IO_0_16	H17	RFSW_LMS2_TRX2_V1
IO_L1P_T0_16	H14	LMS2_TX2_1_EN
IO_L1N_T0_16	H15	RFSW_LMS2_RX1C_V1
IO_L2P_T0_16	G17	LMS2_BB_ADC1_DA2_P
IO_L2N_T0_16	F17	LMS2_BB_ADC1_DA2_N
IO_L3P_T0_DQS_16	F18	LMS2_BB_ADC1_DB2_P
IO_L3N_T0_DQS_16	F19	LMS2_BB_ADC1_DB2_N
IO_L4P_T0_16	G15	RFSW_LMS1_RX2_V1
IO_L4N_T0_16	F15	RFSW_LMS1_RX1_V1
IO_L5P_T0_16	G19	RFSW_LMS1_TX1_V1
IO_L5N_T0_16	F20	FPGA_SPII_LMS3_BB_ADC1_SS
IO_L6P_T0_16	H16	RFSW_LMS1_TX2_V1
IO_L6N_T0_VREF_16	G16	
IO_L7P_T1_16	C17	LMS2_BB_ADC1_DA4_P
IO_L7N_T1_16	B17	LMS2_BB_ADC1_DA4_N
IO_L8P_T1_16	E16	LMS2_BB_ADC1_DA5_P
IO_L8N_T1_16	D16	LMS2_BB_ADC1_DA5_N
IO_L9P_T1_DQS_16	A17	LMS2_BB_ADC1_DA1_P
IO_L9N_T1_DQS_16	A18	LMS2_BB_ADC1_DA1_N
IO_L10P_T1_16	B19	LMS2_BB_ADC1_DA3_P
IO_L10N_T1_16	A19	LMS2_BB_ADC1_DA3_N
IO_L11P_T1_SRCC_16	E17	RFSW1_LMS3_RX1_V1
IO_L11N_T1_SRCC_16	E18	RFSW1_LMS3_RX2_V1
IO_L12P_T1_MRCC_16	D18	LMS2_BB_ADC1_CLKOUT_P_MRCC
IO_L12N_T1_MRCC_16	C18	LMS2_BB_ADC1_CLKOUT_N
IO_L13P_T1_MRCC_16	D19	RFSW_LMS2_RX1IN_V1
IO_L13N_T2_MRCC_16	C19	
IO_L14P_T2_SRCC_16	E20	FPGA_SPII_LMS3_BB_ADC2_SS
IO_L14N_T2_SRCC_16	D20	FPGA_LMS3_BB_ADC2_RESET
IO_L15P_T2_DQS_16	B20	LMS2_BB_ADC1_DA0_P
IO_L15N_T2_DQS_16	A20	LMS2_BB_ADC1_DA0_N
IO_L16P_T2_16	C21	LMS2_BB_ADC1_DB3_P
IO_L16N_T2_16	B21	LMS2_BB_ADC1_DB3_N
IO_L17P_T2_16	B22	LMS2_BB_ADC1_DA6_P
IO_L17N_T2_16	A22	LMS2_BB_ADC1_DA6_N
IO_L18P_T2_16	E21	LMS2_BB_ADC1_DB4_P
IO_L18N_T2_16	D21	LMS2_BB_ADC1_DB4_N
IO_L19P_T3_16	C22	FPGA_SPII_LMS2_BB_ADC1_SS
IO_L19N_T3_VREF_16	C23	
IO_L20P_T3_16	B25	LMS2_BB_ADC1_DB6_P
IO_L20N_T3_16	A25	LMS2_BB_ADC1_DB6_N
IO_L21P_T3_DQS_16	A23	LMS2_BB_ADC1_DB0_P
IO_L21N_T3_DQS_16	C24	LMS2_BB_ADC1_DB0_N
IO_L22P_T3_16	B26	LMS2_BB_ADC1_DB1_P
IO_L22N_T3_16	C24	LMS2_BB_ADC1_DB1_N
IO_L23P_T3_16	B24	LMS2_BB_ADC1_DB5_P
IO_L23N_T3_16	D23	LMS2_BB_ADC1_DB5_N
IO_L24P_T3_16	D24	FPGA_LMS2_BB_ADC1_RESET
IO_L24N_T3_16	E22	FPGA_LMS3_BB_ADC1_RESET
IO_25_16		FPGA_SPII_MISO_BB_ADC

BANK 33

IO_0_33	V4	LMS1_DIQ1_D0
IO_L1P_T0_33	V1	LMS1_RESET
IO_L1N_T0_33	V2	LMS1_DIQ2_D2
IO_L2P_T0_33	W5	LMS1_DIQ1_D1
IO_L2N_T0_33	W4	LMS1_DIQ1_D4
IO_L3P_T0_DQS_33	V3	LMS1_DIQ2_D1
IO_L3N_T0_DQS_33	V2	LMS1_DIQ2_D0
IO_L4P_T0_33	V6	LMS1_TXEN
IO_L4N_T0_33	V5	LMS3_RESET
IO_L5P_T0_33	W3	LMS1_DIQ2_D9
IO_L5N_T0_33	Y3	LMS1_DIQ2_D5
IO_L6P_T0_33	V7	LMS3_RXEN
IO_L6N_T0_VREF_33	V7	LMS2_RESET
IO_L7P_T1_33	AB1	LMS1_DIQ2_D6
IO_L7N_T1_33	AC1	LMS1_DIQ2_D8
IO_L8P_T1_33	Y2	LMS1_DIQ2_D7
IO_L8N_T1_33	Y1	LMS1_DIQ2_D3
IO_L9P_T1_DQS_33	AD1	LMS1_DIQ2_D11
IO_L9N_T1_DQS_33	AE1	LMS1_DIQ2_D10
IO_L10P_T1_33	AE2	LMS1_EN_IQSEL2
IO_L10N_T1_33	AF2	LMS1_DIQ2_D4
IO_L11P_T1_SRCC_33	AB2	LMS1_FCLK1_SRCC_P
IO_L11N_T1_SRCC_33	AC2	FPGA_SPI0_LMS3_SS
IO_L12P_T1_MRCC_33	AA3	LMS1_MCLK1_MRCC_P
IO_L12N_T1_MRCC_33	AA2	FPGA_SPI0_LMS2_SS
IO_L13P_T1_MRCC_33	AA4	LMS1_MCLK2_MRCC_P
IO_L13N_T2_MRCC_33	AB4	FPGA_SPI0_LMS2_MISO
IO_L14P_T2_SRCC_33	AC3	LMS1_FCLK2_SRCC_P
IO_L14N_T2_SRCC_33	AD3	FPGA_SPI0_LMS3_MISO
IO_L15P_T2_DQS_33	AD5	LMS1_DIQ1_D9
IO_L15N_T2_DQS_33	AE5	LMS1_DIQ1_D8
IO_L16P_T2_16	AE3	LMS1_RXEN
IO_L16N_T2_16	AF3	LMS1_TXNRX2
IO_L17P_T2_16	AF5	LMS1_DIQ1_D11
IO_L17N_T2_16	AF4	LMS1_TXNRX1
IO_L18P_T2_16	AC4	LMS1_DIQ1_D10
IO_L18N_T2_16	AD4	LMS1_EN_IQSEL1
IO_L19P_T3_16	Y7	LMS3_RXEN
IO_L19N_T3_VREF_33	AA7	LMS1_DIQ1_D5
IO_L20P_T3_16	Y6	FPGA_SPI0_SCLK
IO_L20N_T3_16	Y5	FPGA_SPI0_MOSI
IO_L21P_T3_DQS_33	Y8	FPGA_SPI0_LMS1_SS
IO_L21N_T3_DQS_33	AA5	LMS1_DIQ1_D6
IO_L22P_T3_16	AB5	LMS1_DIQ1_D7
IO_L22N_T3_16	Y8	LMS2_RXEN
IO_L23P_T3_16	AA6	LMS2_TXEN
IO_L23N_T3_16	AB6	LMS1_DIQ1_D3
IO_L24P_T3_16	AC6	LMS1_DIQ1_D2
IO_25_33	V9	

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BANK 34

IO_0_34	N8	BOM_VER3
IO_L1P_T0_34	K3	LMS2_BB_DAC1_B13_P
IO_L1N_T0_34	I3	LMS2_BB_DAC1_B13_N
IO_L2P_T0_34	M7	LMS2_BB_DAC1_B2_P
IO_L2N_T0_34	L7	LMS2_BB_DAC1_B2_N
IO_L3P_T0_DQS_34	M4	LMS2_BB_DAC1_B12_P
IO_L3N_T0_DQS_34	L4	LMS2_BB_DAC1_B12_N
IO_L4P_T0_34	L5	FPGA_SW1
IO_L4N_T0_34	K5	FPGA_SW0
IO_L5P_T0_34	N7	FPGA_SPI2_XO_20_DAC_SS
IO_L5N_T0_34	N6	FPGA_SPI2_XO_25_DAC_SS
IO_L6P_T0_34	M6	LMS2_BB_DAC1_SELIQ_P
IO_L6N_T0_VREF_34	M5	LMS2_BB_DAC1_SELIQ_N
IO_L7P_T1_34	K1	LMS2_BB_DAC1_B14_P
IO_L7N_T1_34	I1	LMS2_BB_DAC1_B14_N
IO_L8P_T1_34	L3	
IO_L8N_T1_34	K2	BOM_VERO
IO_L9P_T1_DQS_34	N1	LMS2_BB_DAC1_B0_P
IO_L9N_T1_DQS_34	M1	LMS2_BB_DAC1_B0_N
IO_L10P_T1_34	H2	LMS2_BB_DAC1_B15_P
IO_L10N_T1_34	H1	LMS2_BB_DAC1_B15_N
IO_L11P_T1_SRCC_34	M2	FPGA_LMS2_BB_DAC1_CLK_P
IO_L11N_T1_SRCC_34	N3	MRCC_CDCM_LMS2_BB_DAC1_REFPC_P
IO_L12P_T1_MRCC_34	AA3	CDCM_LMS2_BB_DAC1_REFPC_N
IO_L12N_T1_MRCC_34	AA2	FPGA_LMS2_BB_DAC1_CLK_P
IO_L13P_T2_MRCC_34	AA4	CDCM_LMS2_BB_DAC1_REFPC_N
IO_L13N_T2_MRCC_34	R3	LMK1_CLK2_MRCC/SRCC_P
IO_L14P_T2_SRCC_34	P3	
IO_L14N_T2_SRCC_34	P4	LMK2_CLK1NI
IO_L14P_T2_DQS_34	N4	
IO_L15P_T2_SRCC_34	P1	LMS2_BB_DAC1_B10_P
IO_L15P_T2_DQS_34	P2	LMS2_BB_DAC1_B10_N
IO_L15N_T2_DQS_34	T4	LMS2_BB_DAC1_B11_P
IO_L16P_T2_34	T3	LMS2_BB_DAC1_B11_N
IO_L16N_T2_34	T2	LMS2_BB_DAC1_B9_P
IO_L17P_T2_34	R2	LMS2_BB_DAC1_B9_N
IO_L17N_T2_34	J2	LMS2_BB_DAC1_B8_P
IO_L18P_T2_34	I1	LMS2_BB_DAC1_B8_N
IO_L18N_T2_34	P6	LMS2_BB_DAC1_B6_P
IO_L19P_T3_34	P5	LMS2_BB_DAC1_B6_N
IO_L19N_T3_VREF_34	T5	LMS2_BB_DAC1_B7_P
IO_L20P_T3_34	R5	LMS2_BB_DAC1_B7_N
IO_L20N_T3_34	U6	LMS2_BB_DAC1_B5_P
IO_L21P_T3_DQS_34	U5	LMS2_BB_DAC1_B5_N
IO_L21N_T3_DQS_34	R8	LMS2_BB_DAC1_B4_P
IO_L22P_T3_34	P8	LMS2_BB_DAC1_B4_N
IO_L22N_T3_34	R7	LMS2_BB_DAC1_B1_P
IO_L23P_T3_34	R6	LMS2_BB_DAC1_B1_N
IO_L23N_T3_34	T8	LMS2_BB_DAC1_B3_P
IO_L24P_T3_34	J7	LMS2_BB_DAC1_B3_N
IO_L24N_T3_34	U4	FAN_CTRL
IO_25_34		

XC7A200T-2FBG676C

2.5V

BANK 35

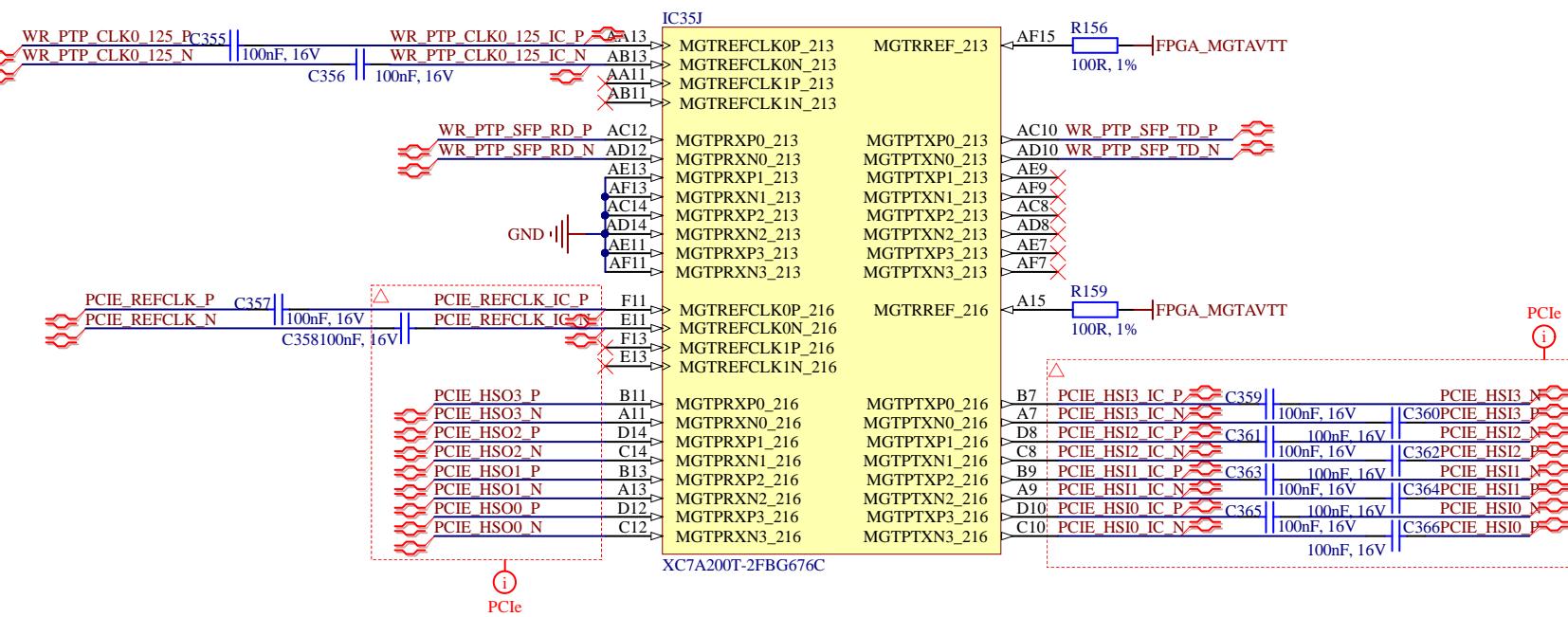
IO_0_35	J8	LMS2_BB_DAC2_B0_P
IO_L1P_T0_AD4P_35	E6	LMS2_BB_DAC2_B0_N
IO_L1N_T0_AD4N_35	D6	LMS2_BB_DAC2_B13_P
IO_L2P_T0_AD12P_35	H8	LMS2_BB_DAC2_B13_N

NF elements on sheet: R162, R163, R164, IC36, R167, R168, R179, R181

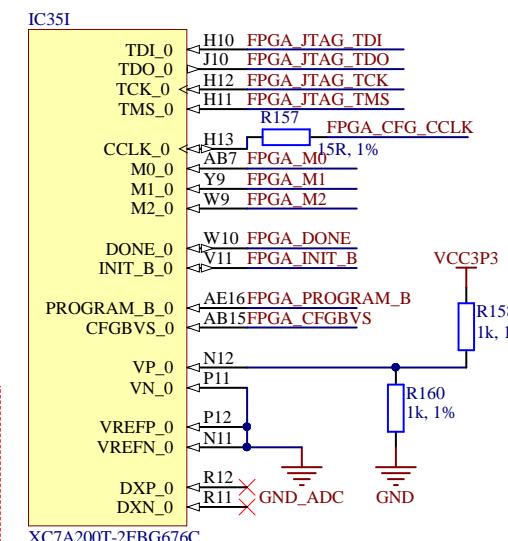
Number of NF elements on sheet: 8

FPGA misc (PCIe, config)

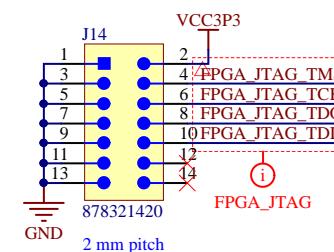
PCI Express x4



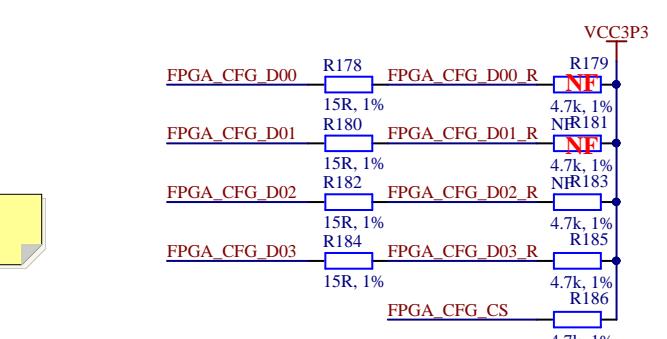
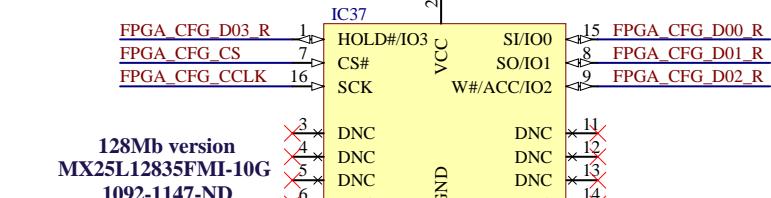
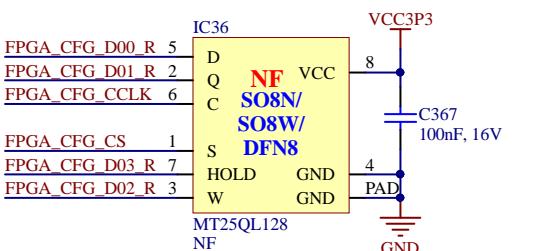
FPGA Configuration



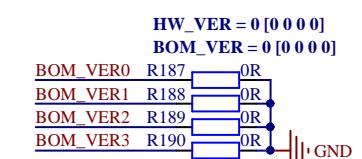
FPGA JTAG



FPGA Configuration Flash



HW_VER, BOM_VER



Project name: LimeSDR-X3_1v0.PrbPcb

Title: FPGA misc (PCIe, config)

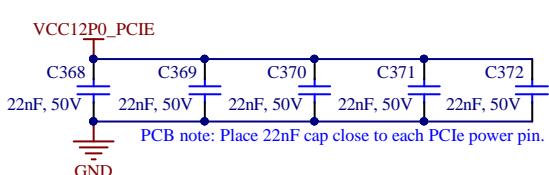
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Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:46:26 Sheet 19 of 31

File: 19_FPGA_mis.SchDoc

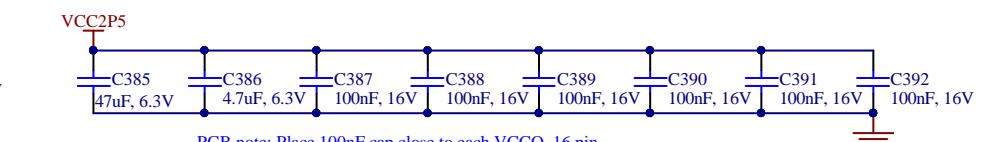
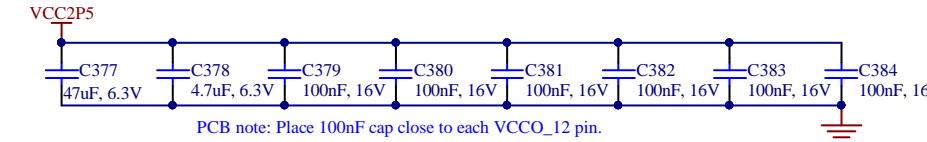
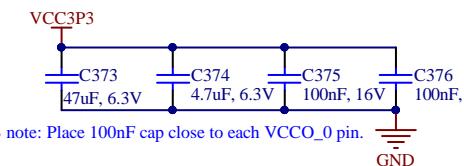
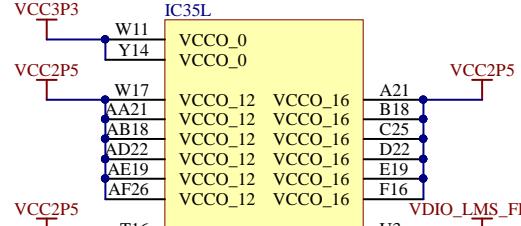


NF elements on sheet: BATTH1, BATT1, R192

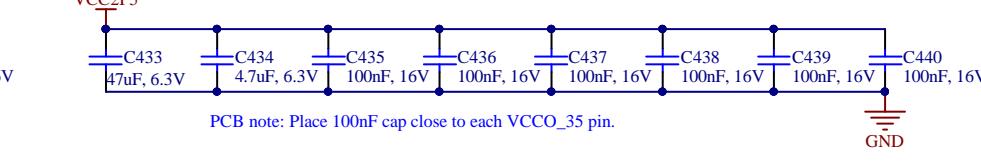
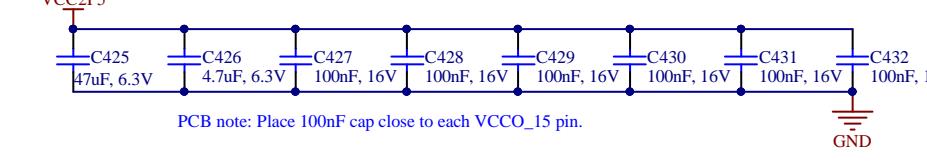
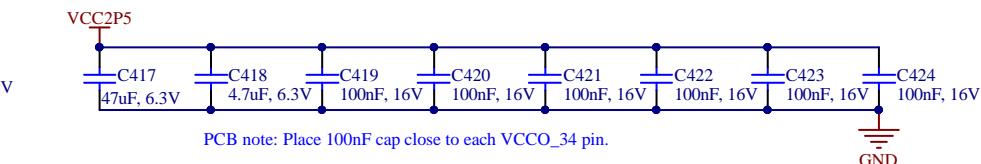
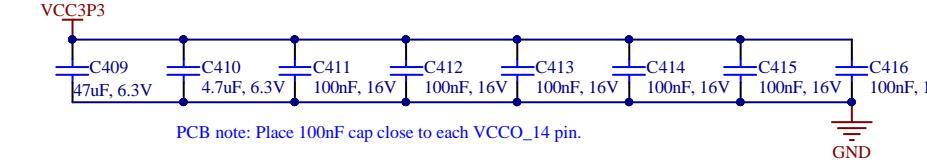
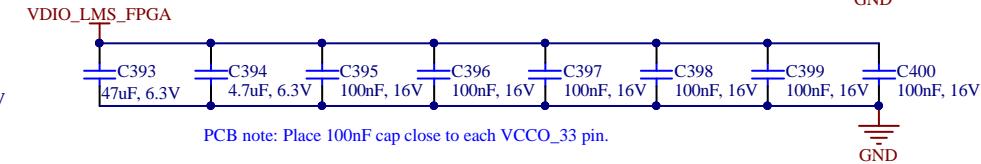
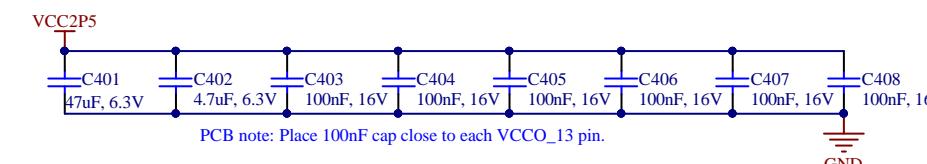
Number of NF elements on sheet: 3

FPGA power

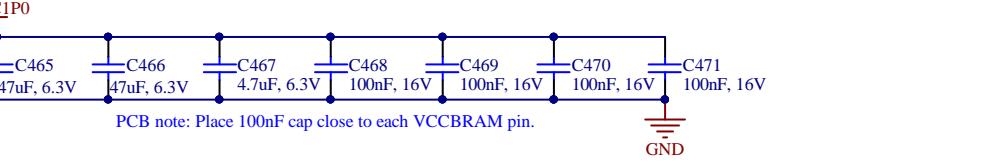
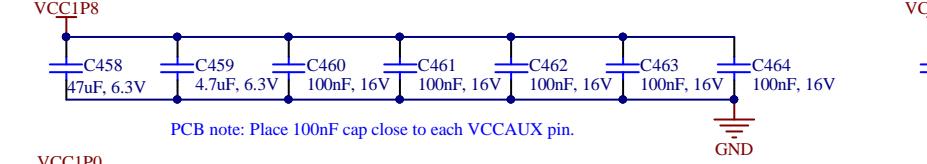
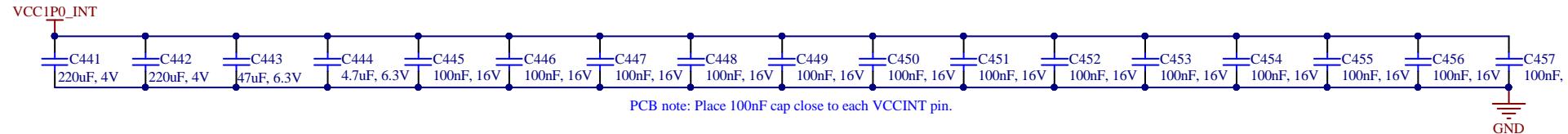
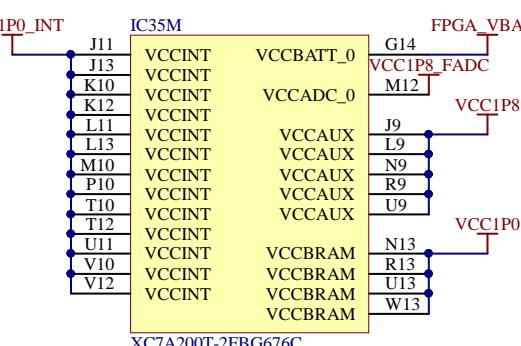
A



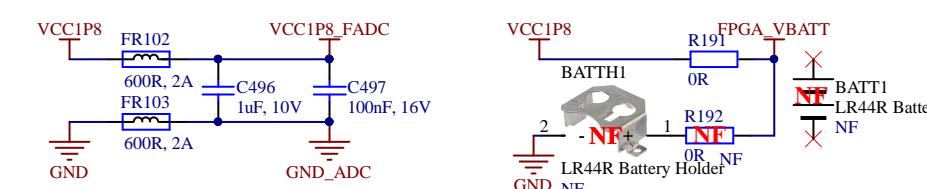
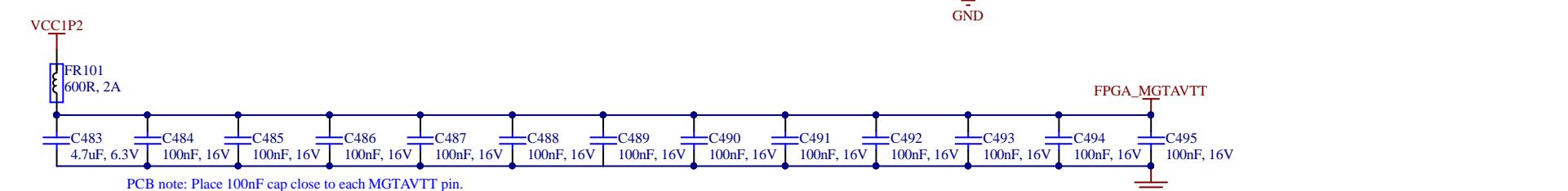
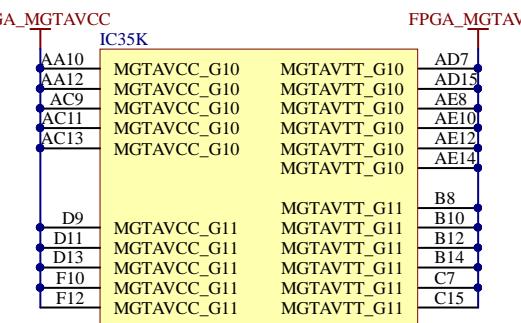
B



C



D



Project name: LimeSDR-X3_1v0.PrbPcb

Title: **FPGA power**

Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:46:34 Sheet 20 of 31

File: 20 FPGA Power.SchDoc

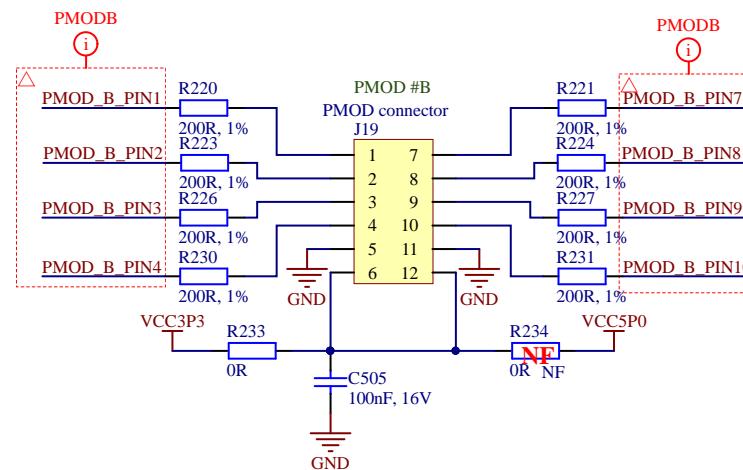
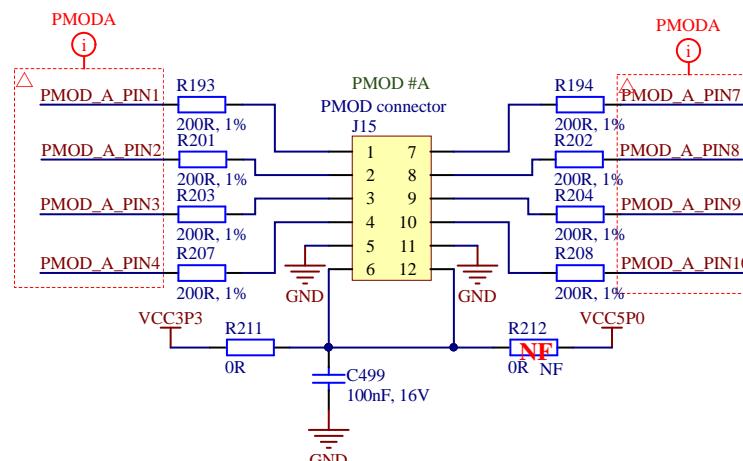
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Surrey
United Kingdom



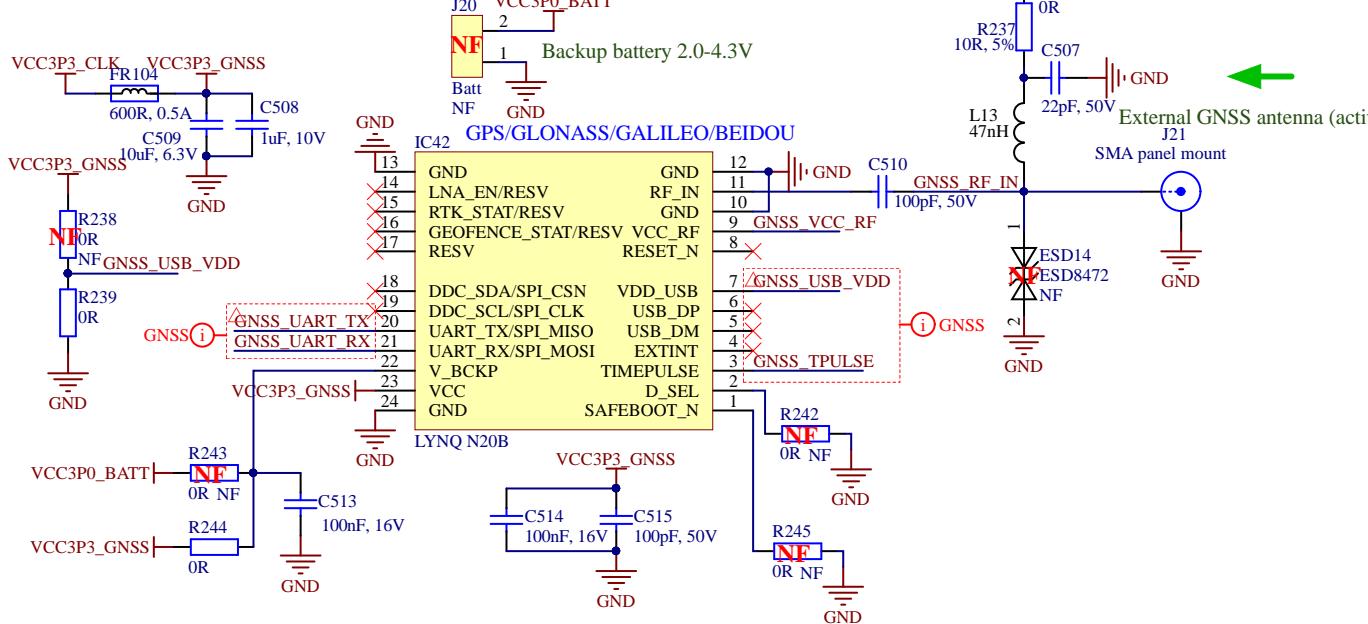
NF elements on sheet: C498, R212, R216, R218, R225, R228, R234, R235, J20, R238, ESD14, R242, R243, R245, R241, IC41
Number of NF elements on sheet: 16

Peripherals

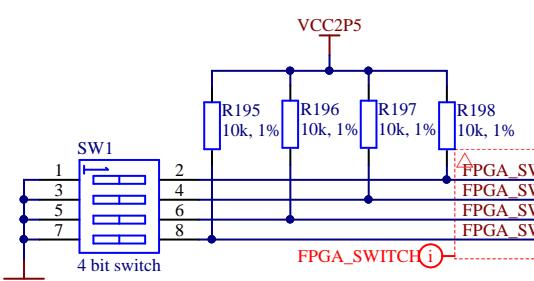
PMOD 12-pin connectors



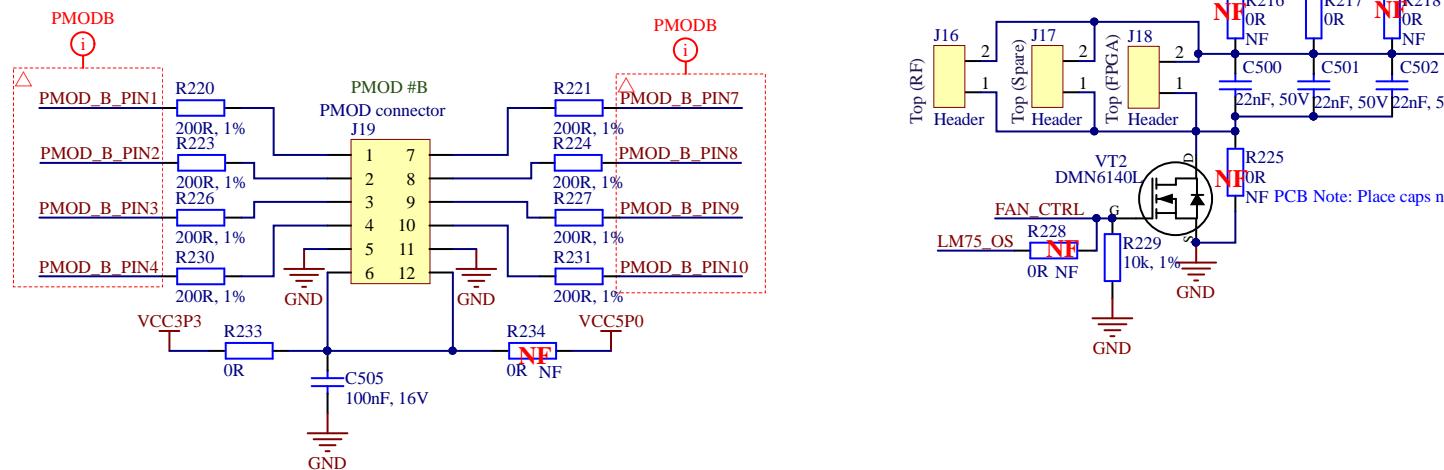
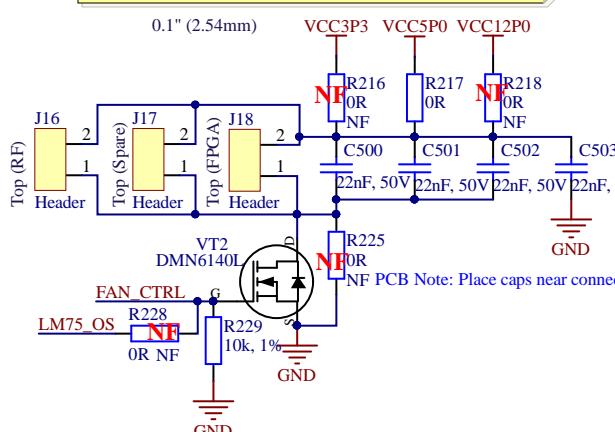
GNSS receiver



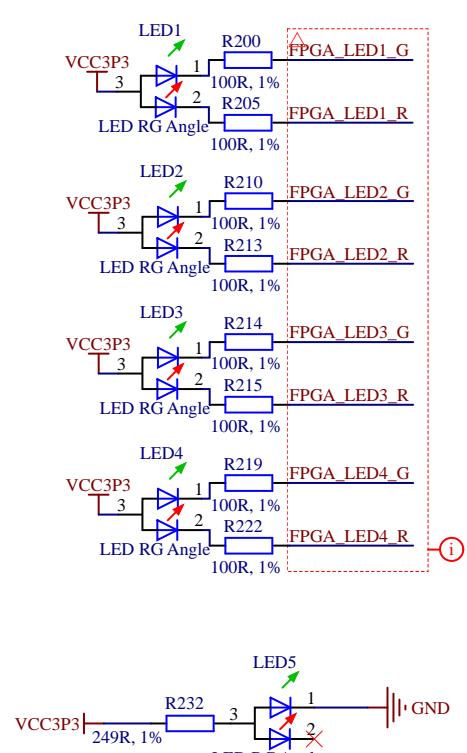
FPGA_SW



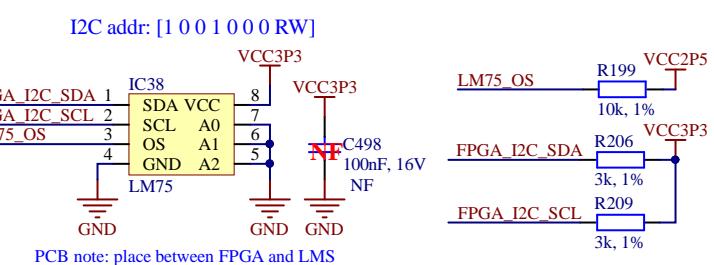
FAN control



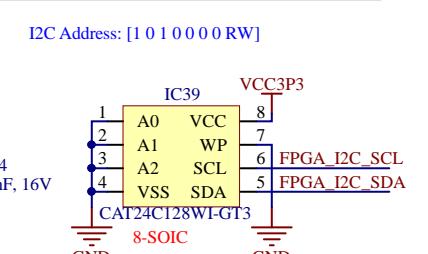
FPGA LEDs



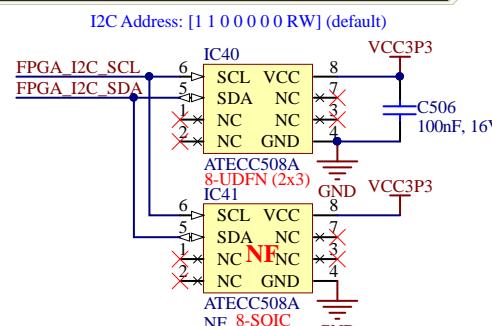
I2C Temperature sensor



I2C EEPROM



I2C secure key storage

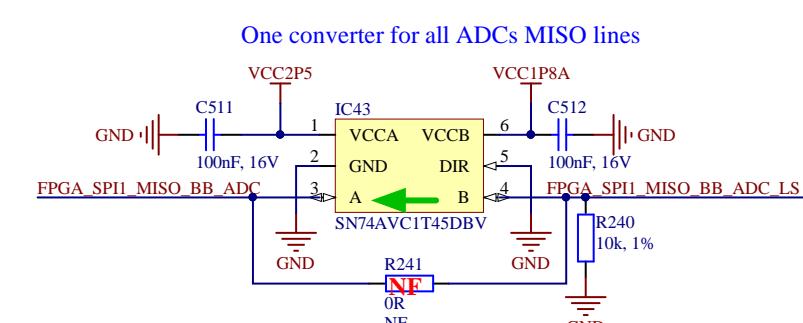


External SMA to internal U.FL



Can be connected internal U.FL connector via pigtail

SPI1 MISO BB ADCs level converter



Project name: LimeSDR-X3_1v0.PrbPcb

Title: Peripherals

Size: A3

Revision: v1.0

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Date: 2022-12-19 Time: 12:46:42

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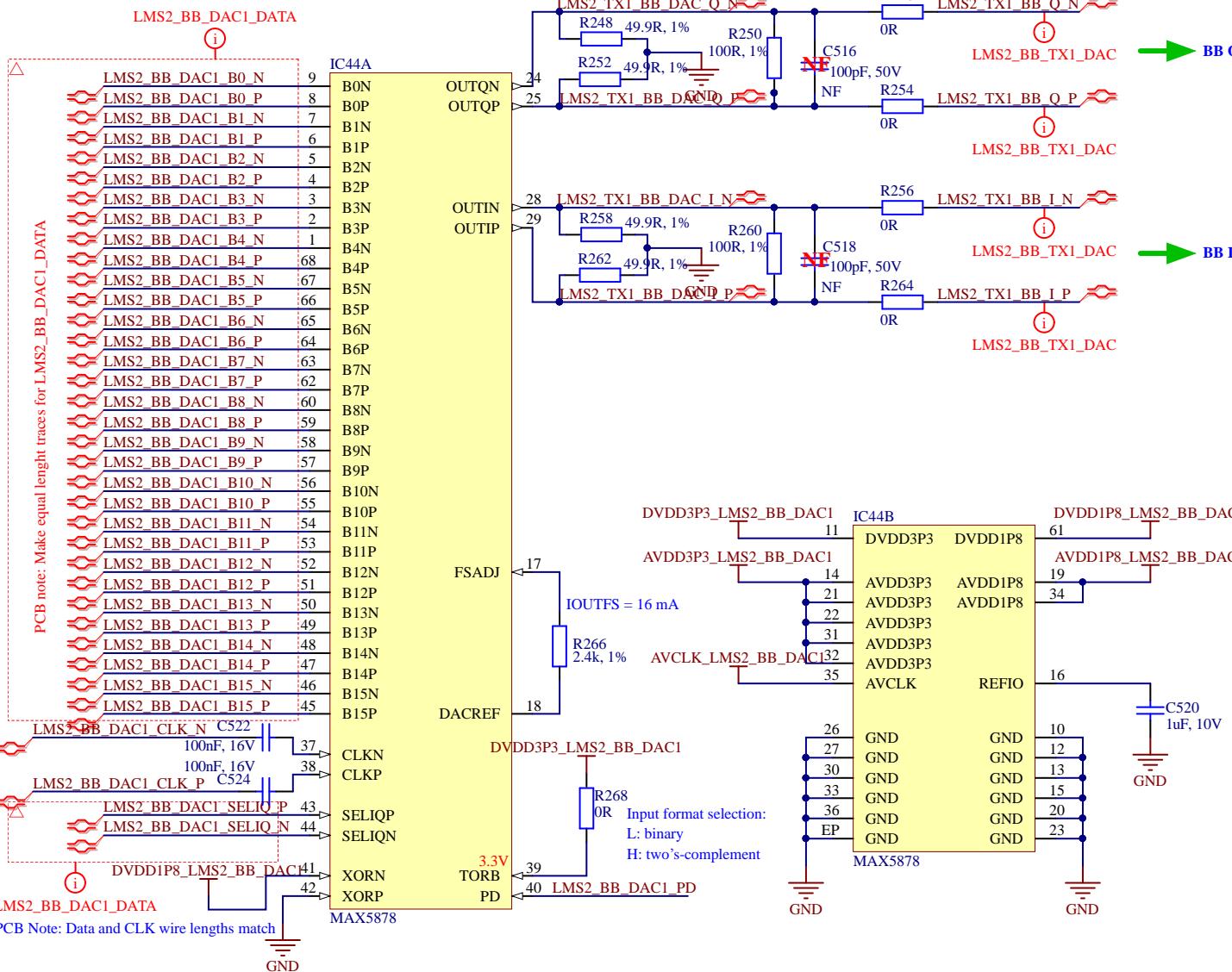
File: 21_Peripherals.SchDoc

NF elements on sheet: R516, C518, C517, C519

Number of NF elements on sheet: 4

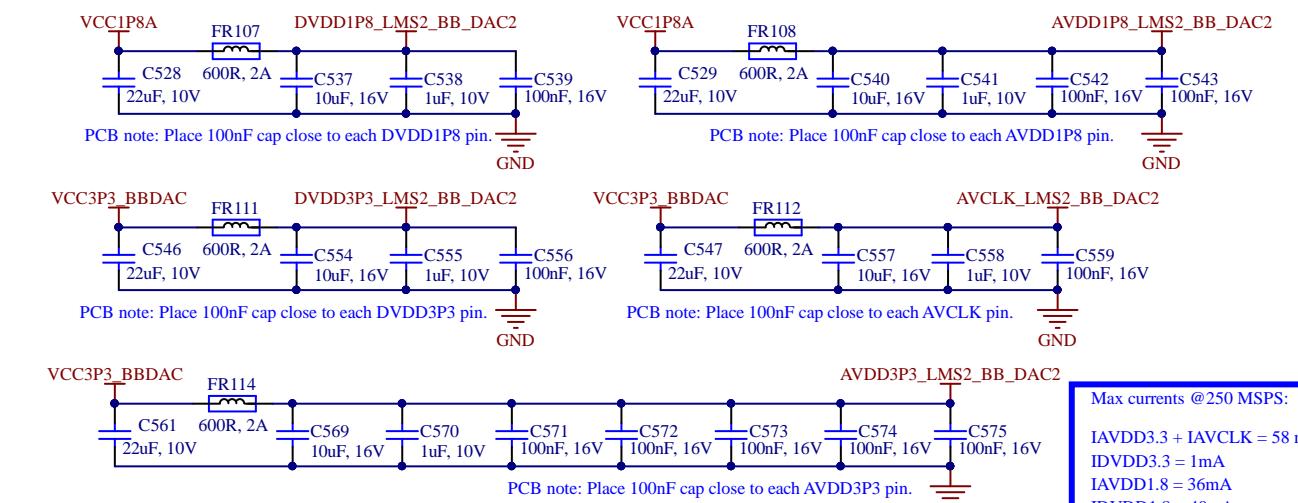
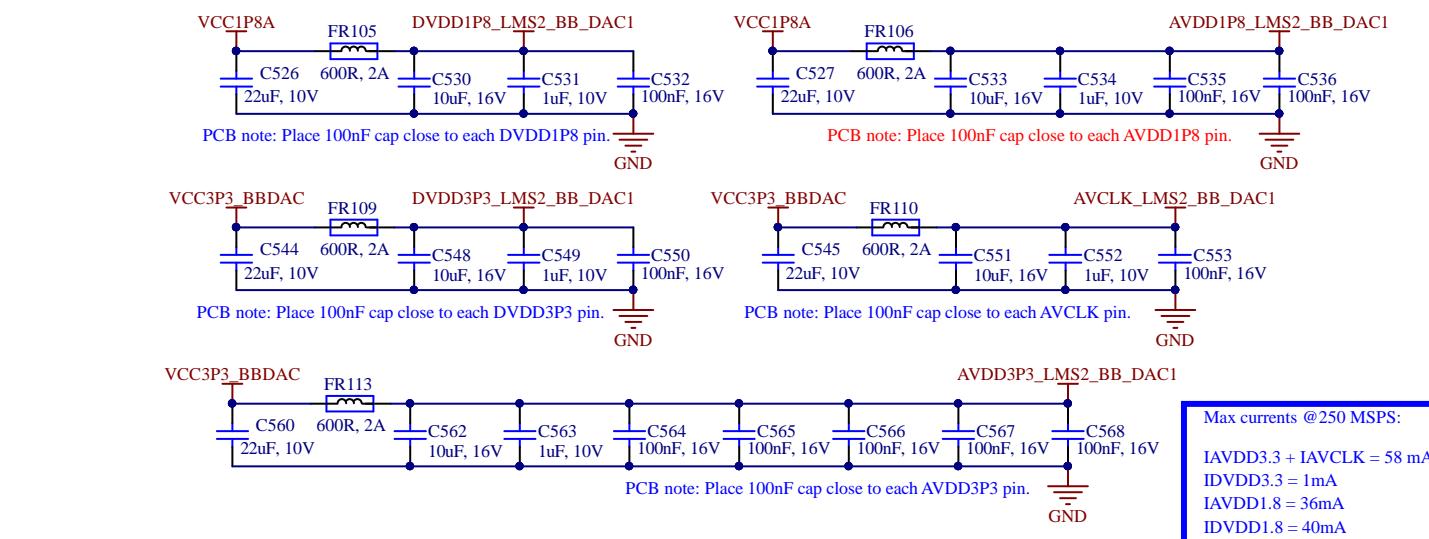
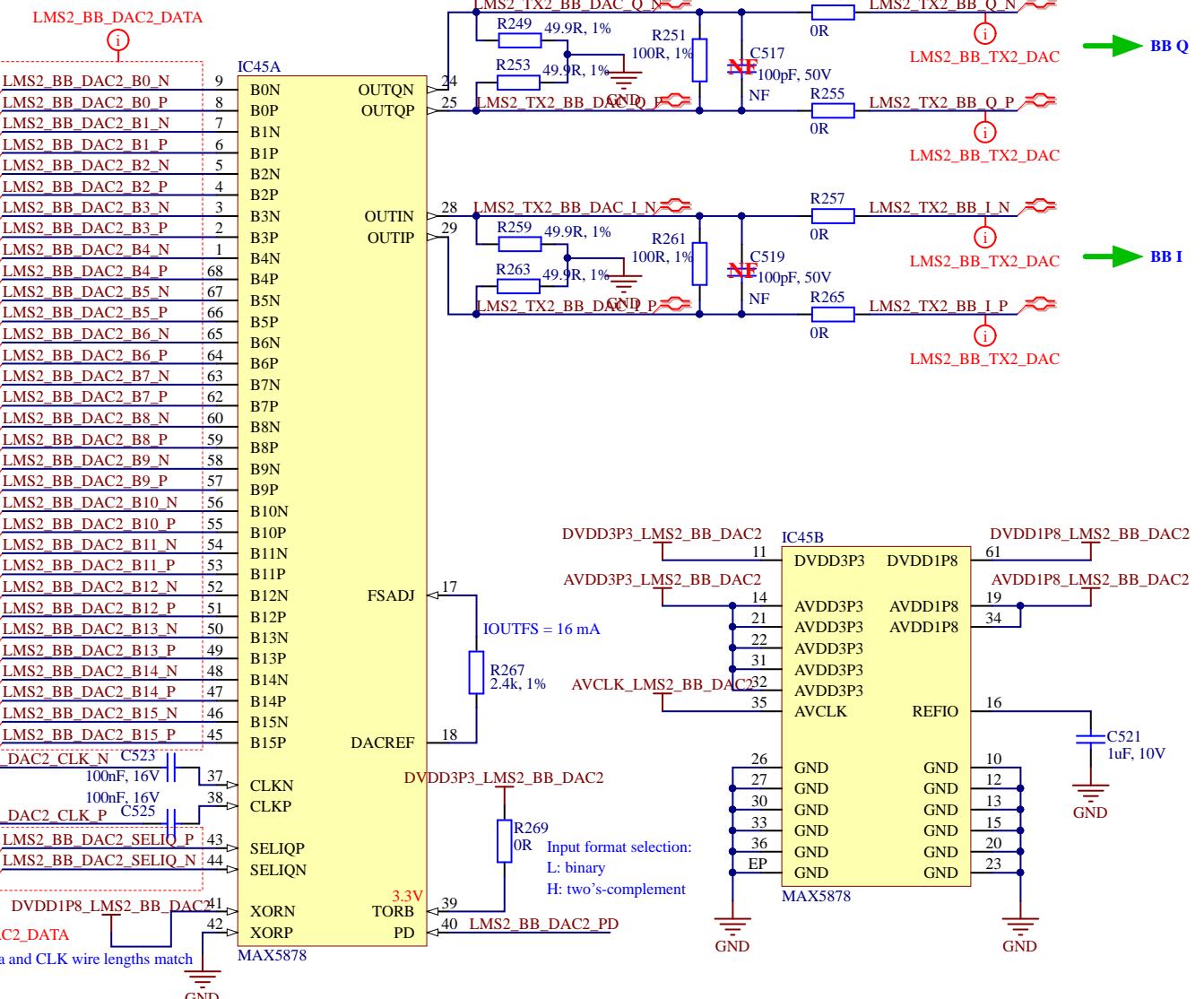
LMS2_TX1_BB DAC

2 ch., 16-bit, 250MSPS



LMS2_TX2_BB DAC

2 ch., 16-bit, 250MSPS



Project name: LimeSDR-X3_1v0.PrbPcb

Title: LMS2 TX BB DACs

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United Kingdom



Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:46:49 Sheet 22 of 31

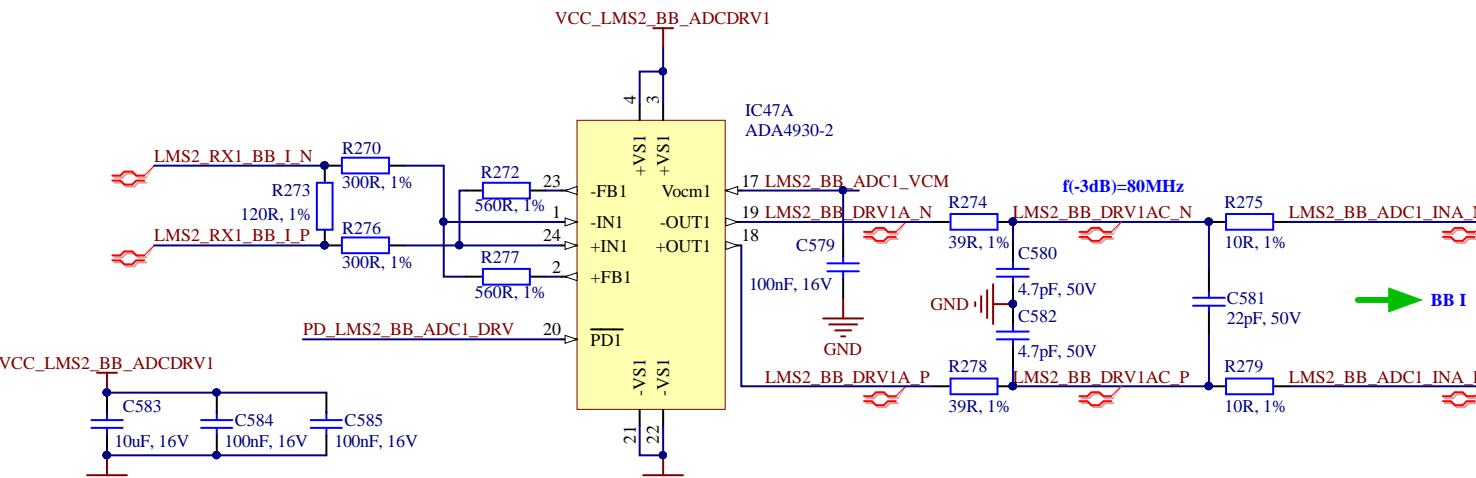
File: 22_LMS2 TX_BB DACs.SchDoc

NF elements on sheet: R297
Number of NF elements on sheet: 1

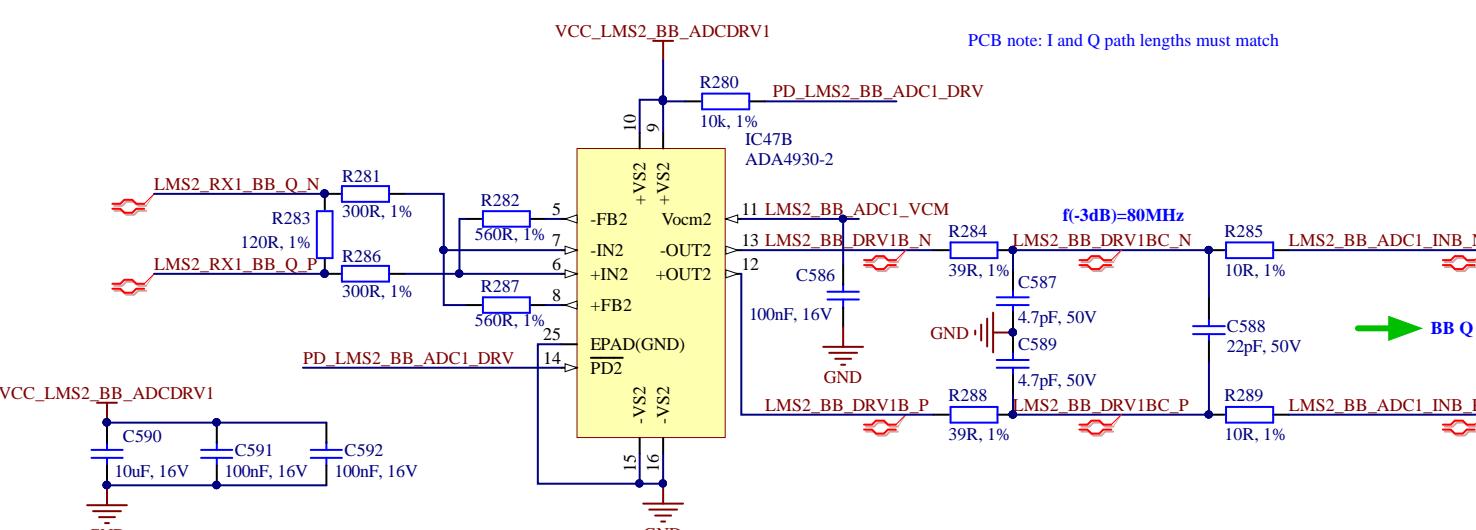
LMS2 RX1 BB ADC

A

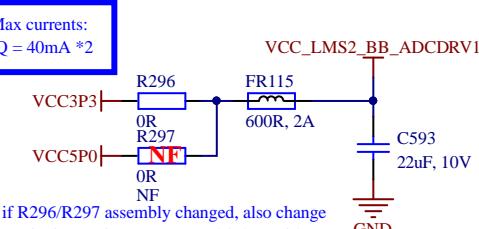
ADC Drivers



B



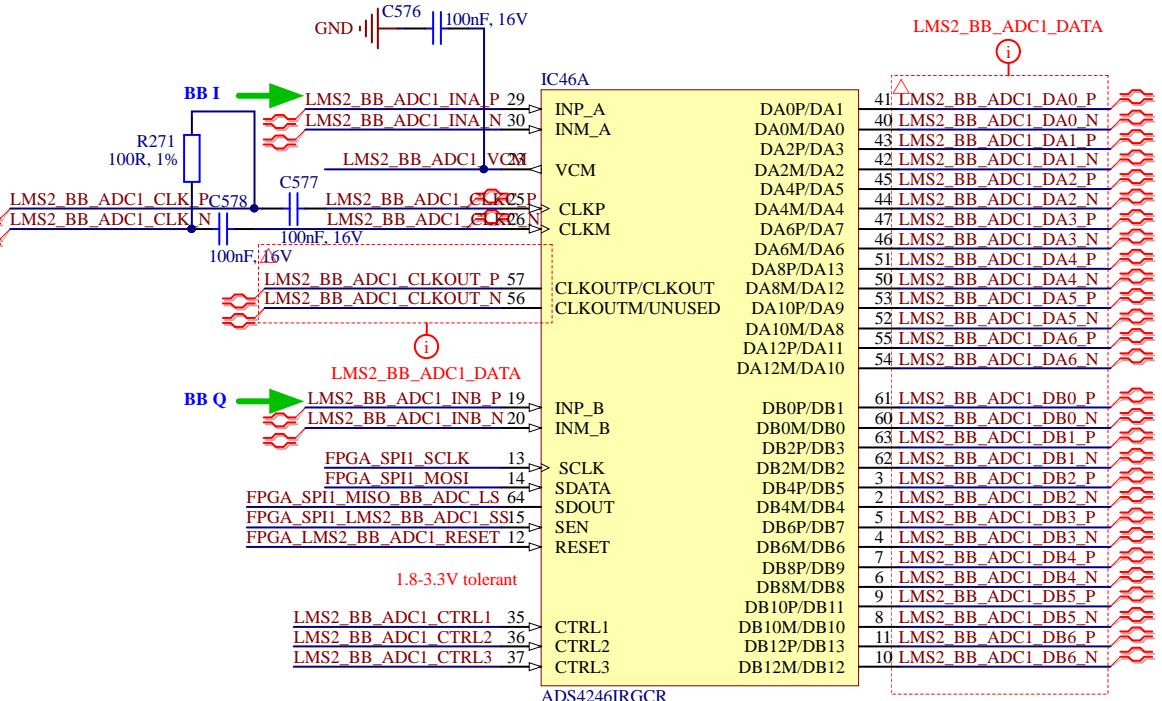
C



D

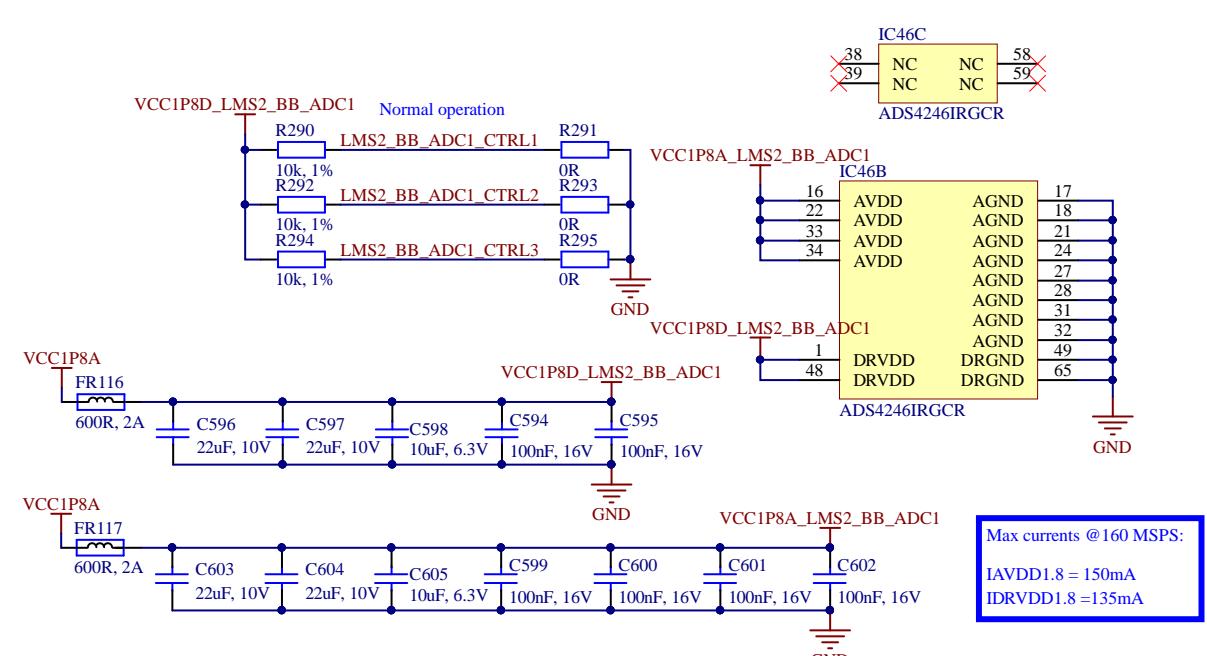
ADC

2 ch., 14-bit, 160MSPS



PCB note: Make equal length traces for LMS2_BB_ADC1_DATA

ADC Control & Power



Local ADC and DAC fiducial Top

FL17

Project name: LimeSDR-X3_1v0.PrfPcb

Title: LMS2 RX1 BB ADC

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Surrey
United Kingdom



Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:46:57 Sheet 23 of 31

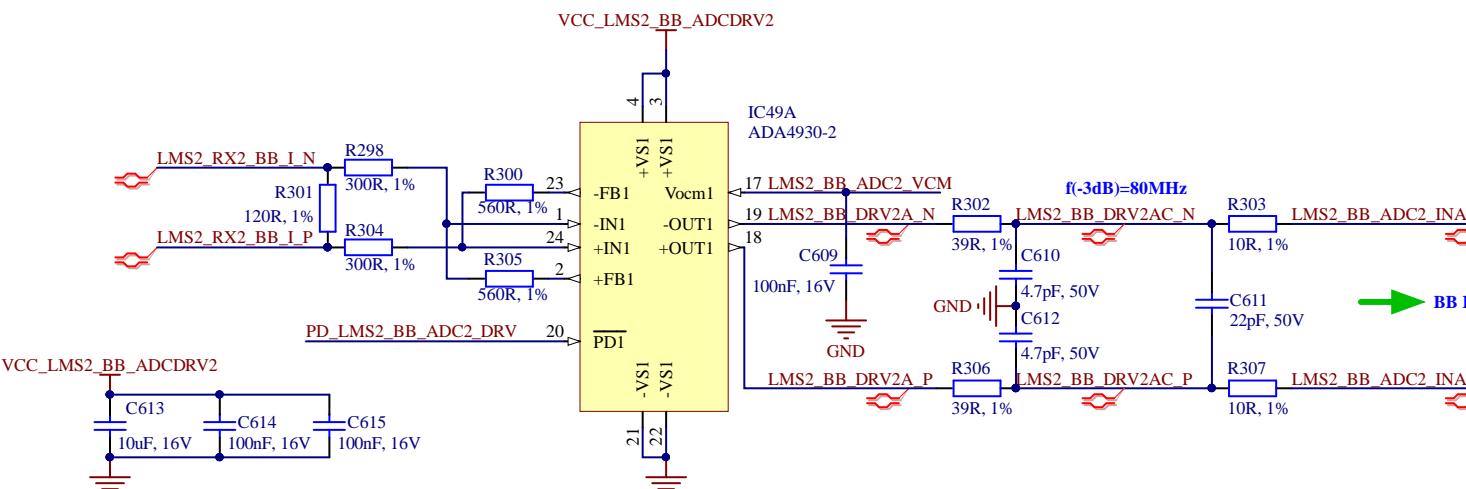
File: 23_LMS2_RX1_BB_ADC.SchDoc

NF elements on sheet: R325
Number of NF elements on sheet: 1

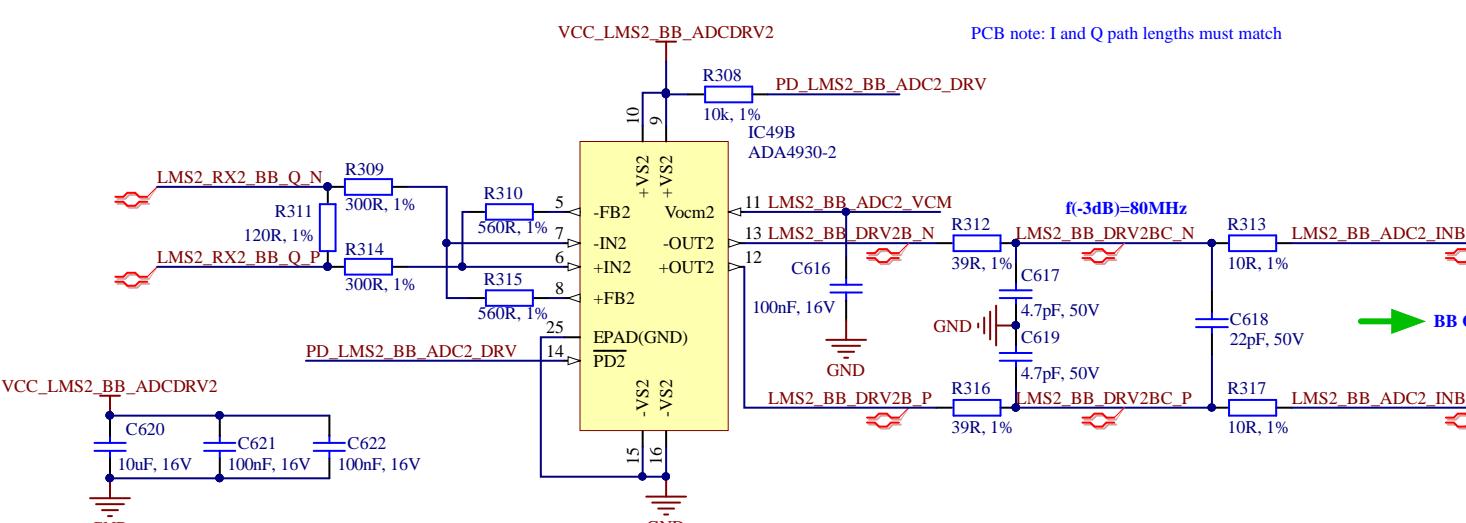
LMS2 RX2 BB ADC

A

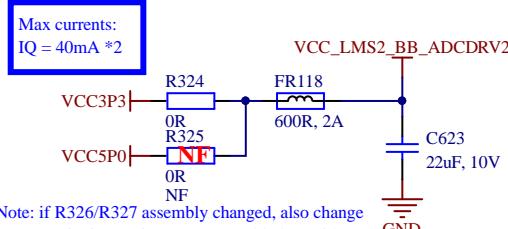
ADC Drivers



B



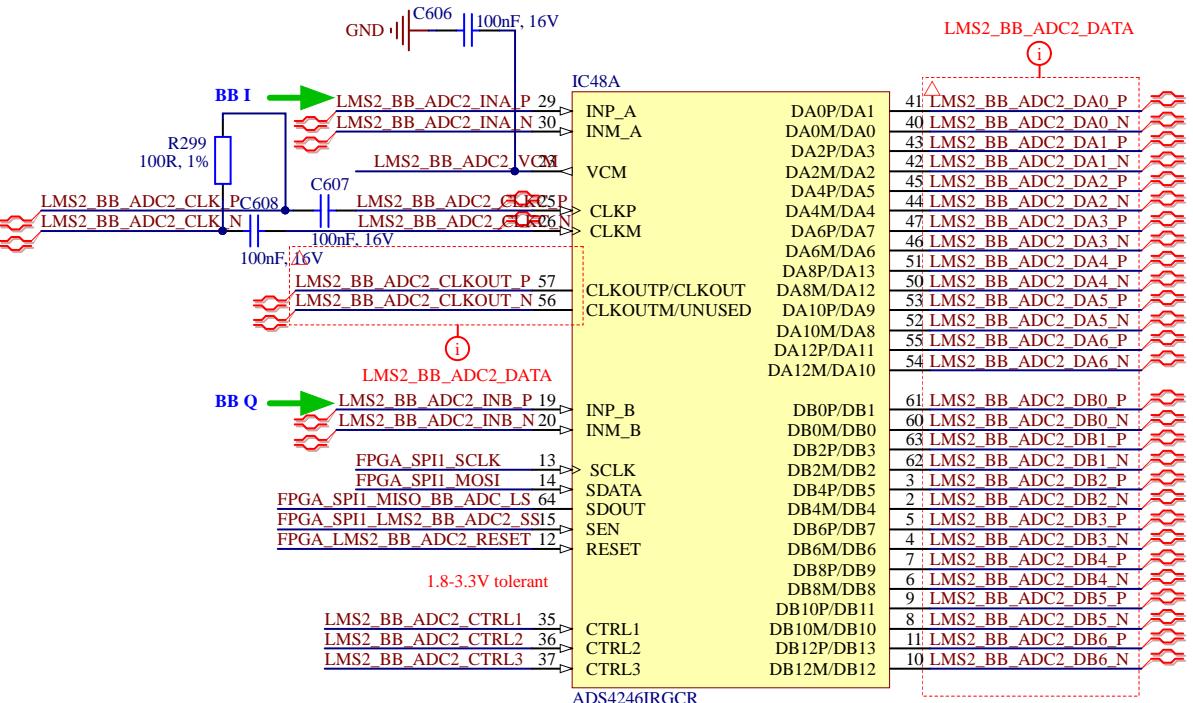
C



Note: if R326/R327 assembly changed, also change equivalent resistors on pages 23, 25 and 26.

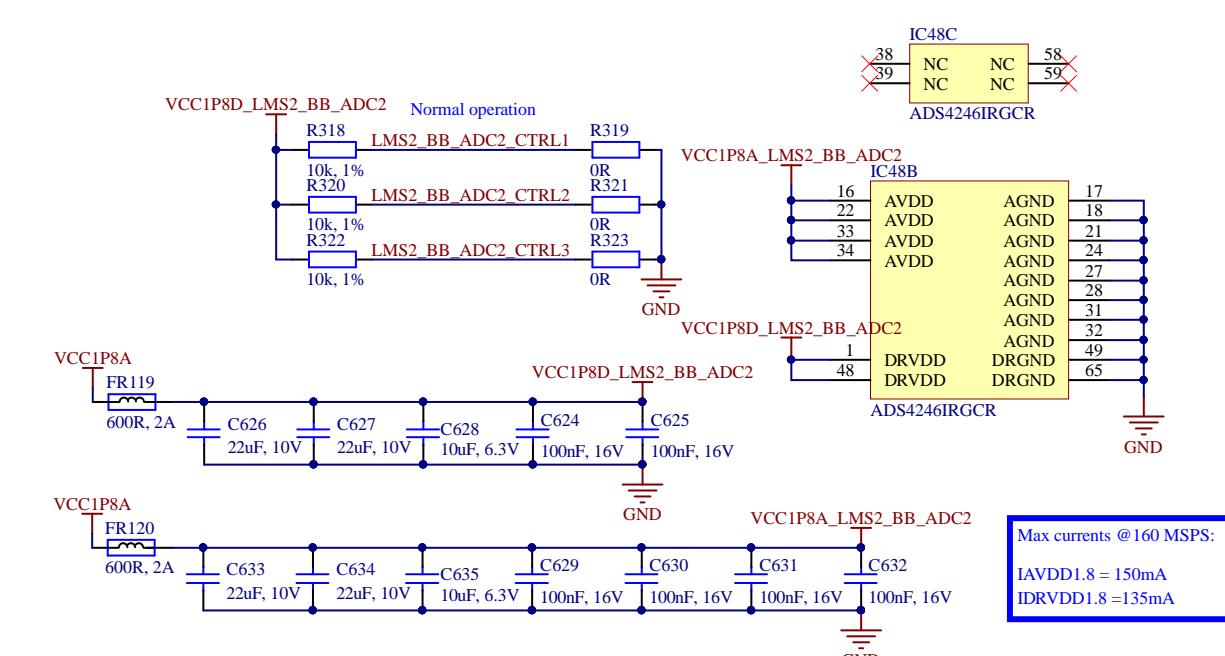
ADC

2 ch., 14-bit, 160MSPS



PCB note: Make equal length traces for LMS2_BB_ADC2_DATA

ADC Control & Power



Project name: LimeSDR-X3_1v0.PrbPcb

Local ADC and DAC fiducial Top

FL18

Title: LMS2 RX2 BB ADC	Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Revision: v1.0
Date: 2022-12-19	Time: 12:47:05
File: 24 LMS2 RX2 BB ADC.SchDoc	

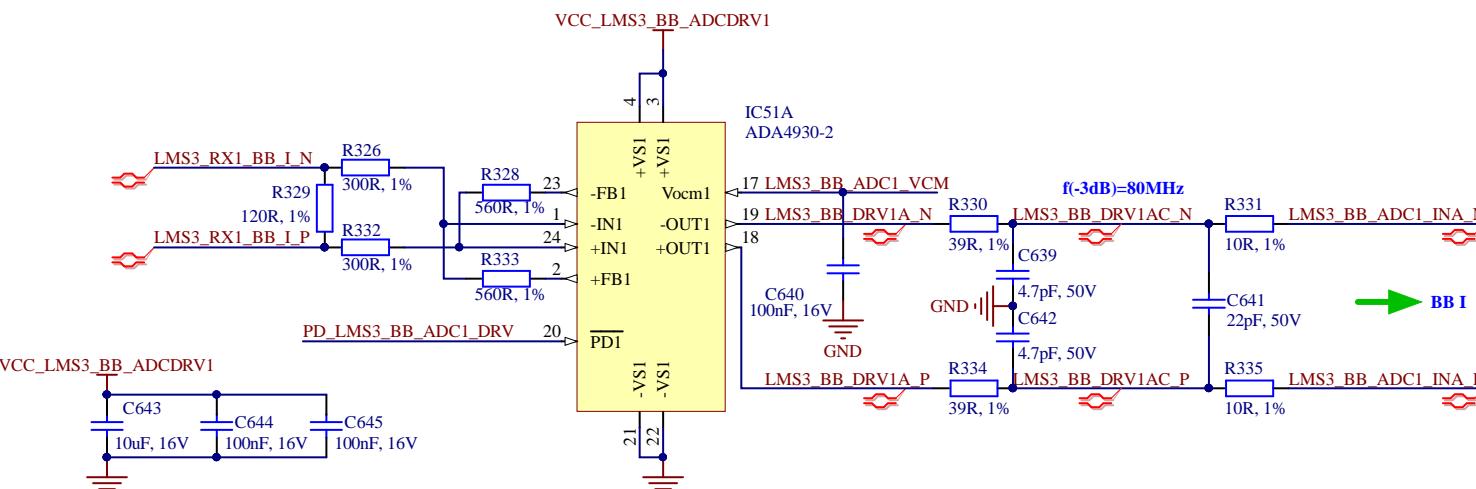


NF elements on sheet: R353
Number of NF elements on sheet: 1

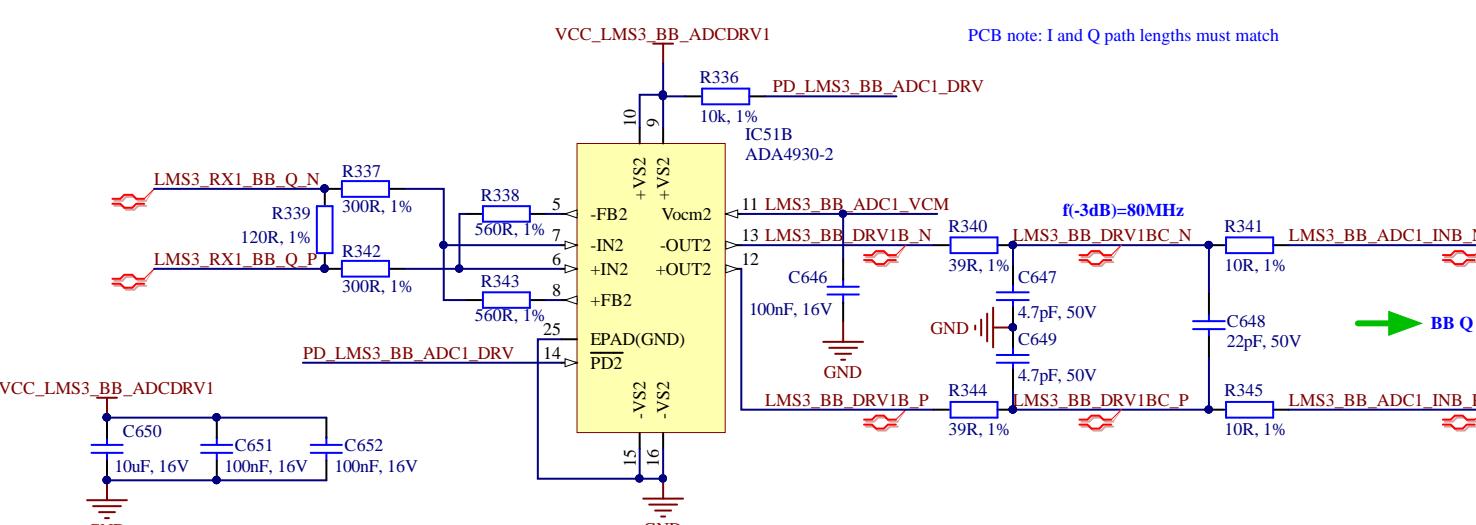
LMS3 RX1 BB ADC

A

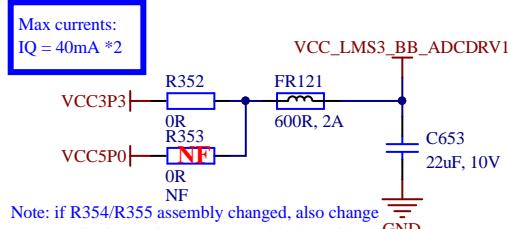
ADC Drivers



B



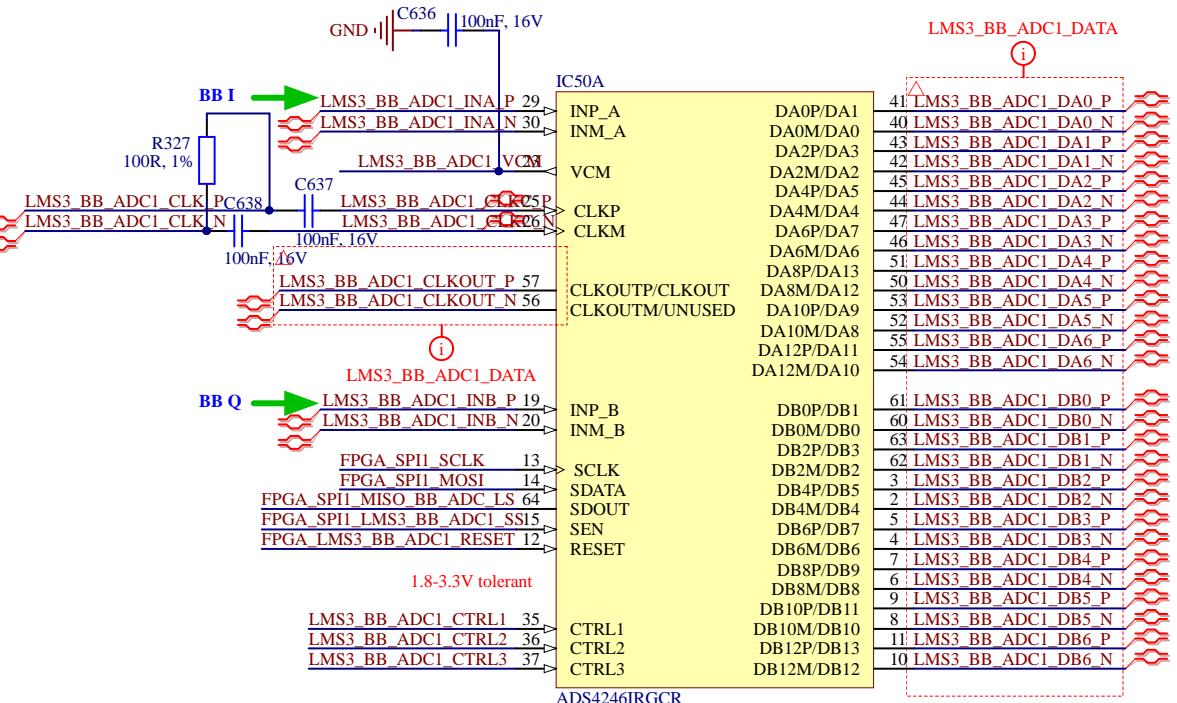
C



D

ADC

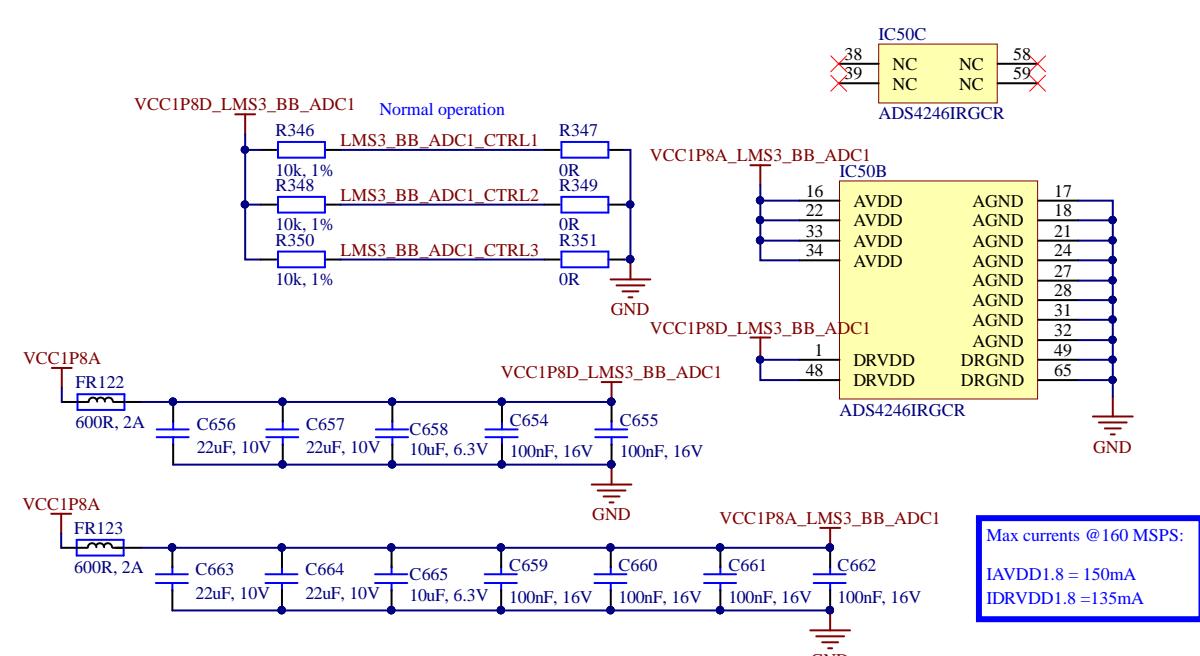
2 ch., 14-bit, 160MSPS



PCB note: Make equal length traces for LMS3_BB_ADC1_DATA

PCB note: Make equal length traces for LMS3_BB_ADC1_CLKOUT

ADC Control & Power



Project name: LimeSDR-X3_1v0.PrbPcb

Local ADC and DAC fiducial Top

FL19

Title: LMS3 RX1 BB ADC

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Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:47:12 Sheet 25 of 31

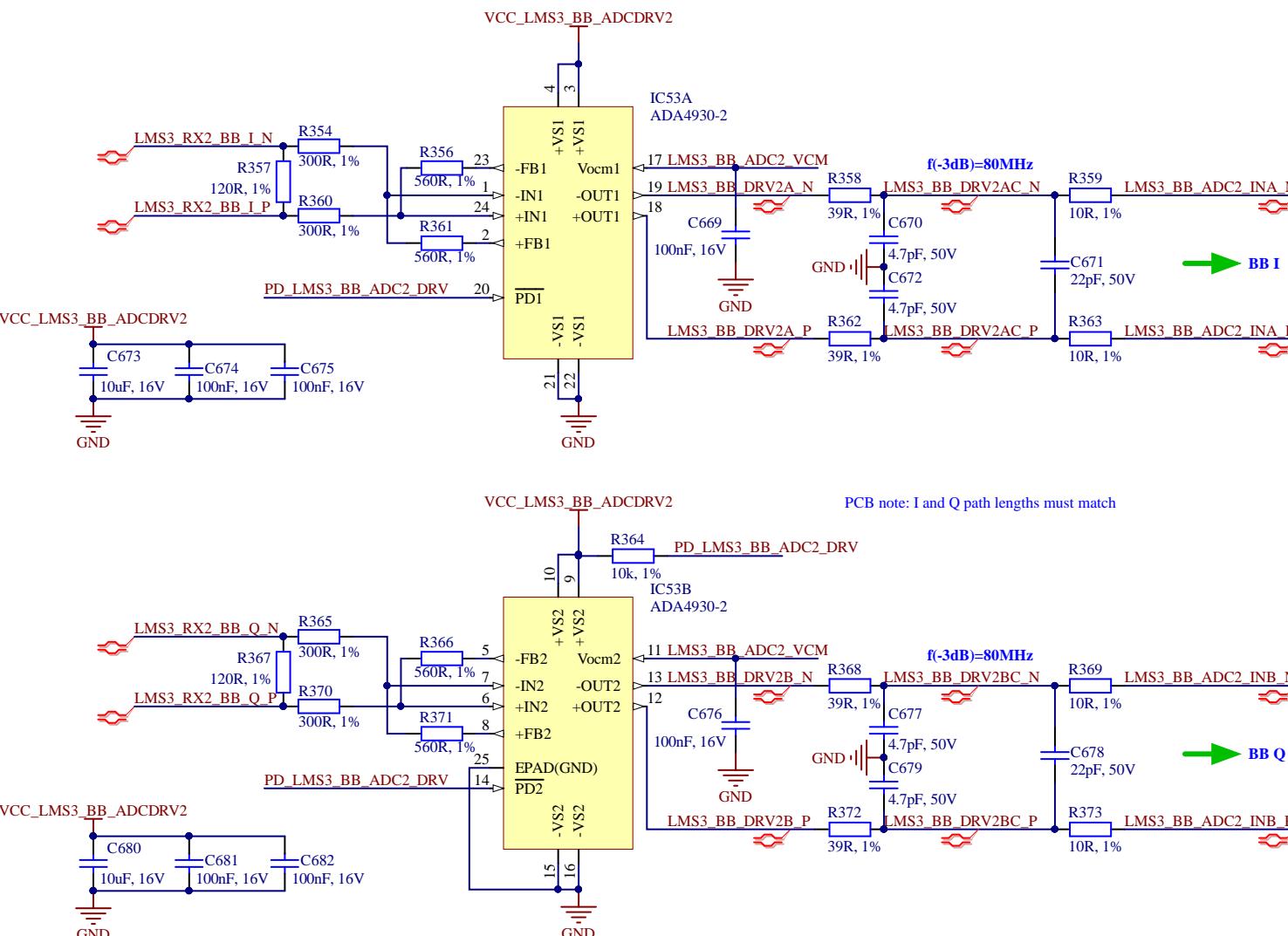
File: 25_LMS3_RX1_BB_ADC.SchDoc

NF elements on sheet: R381
Number of NF elements on sheet: 1

LMS3 RX2 BB ADC

A

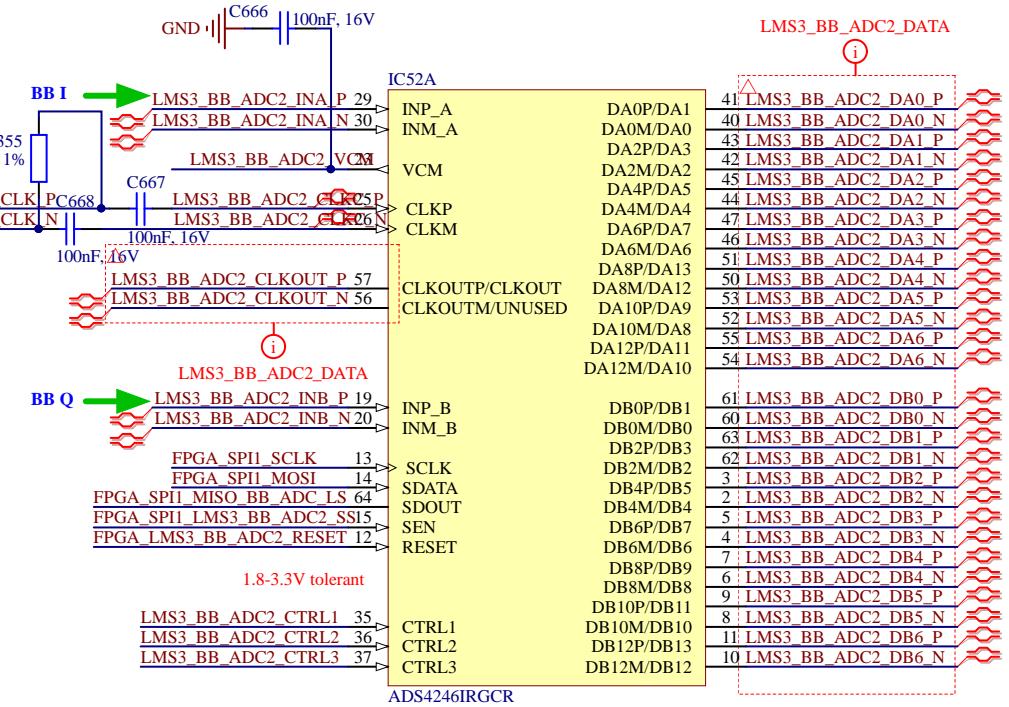
ADC Drivers



B

ADC

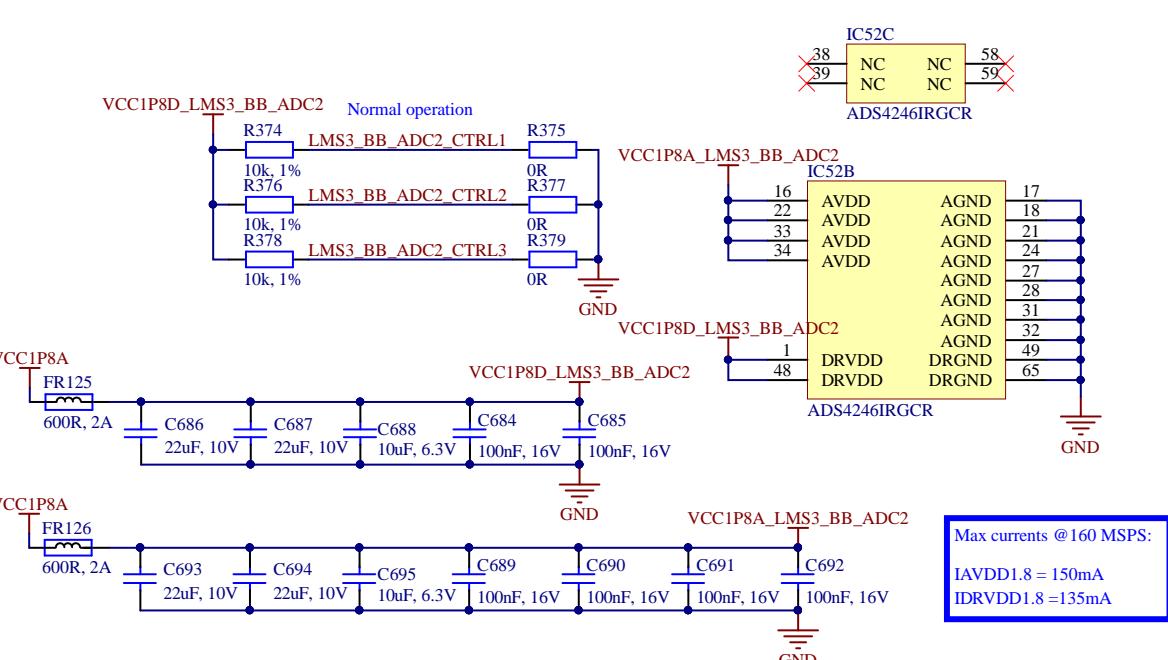
2 ch., 14-bit, 160MSPS



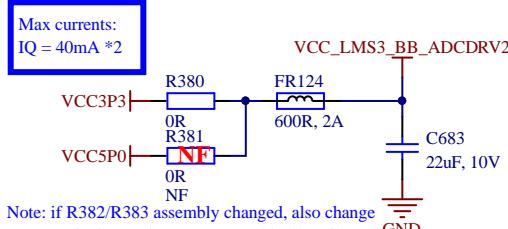
PCB note: Make equal length traces for LMS3_BB_ADC2_DATA

C

ADC Control & Power



D



D

Local ADC and DAC fiducial Top

FL20

Project name: LimeSDR-X3_1v0.PrfPcb

Title: LMS3 RX2 BB ADC

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United Kingdom



Size: A3 Revision: v1.0

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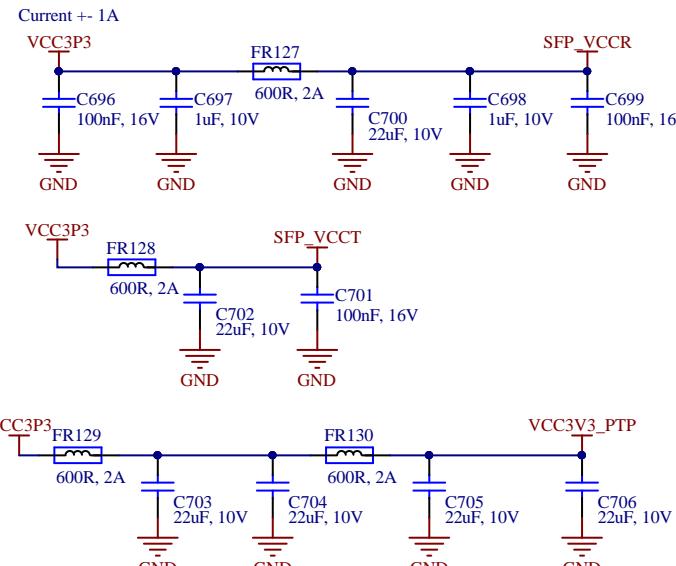
File: 26_LMS3_RX2_BB_ADC.SchDoc

1 2 3 4 5 6 7 8

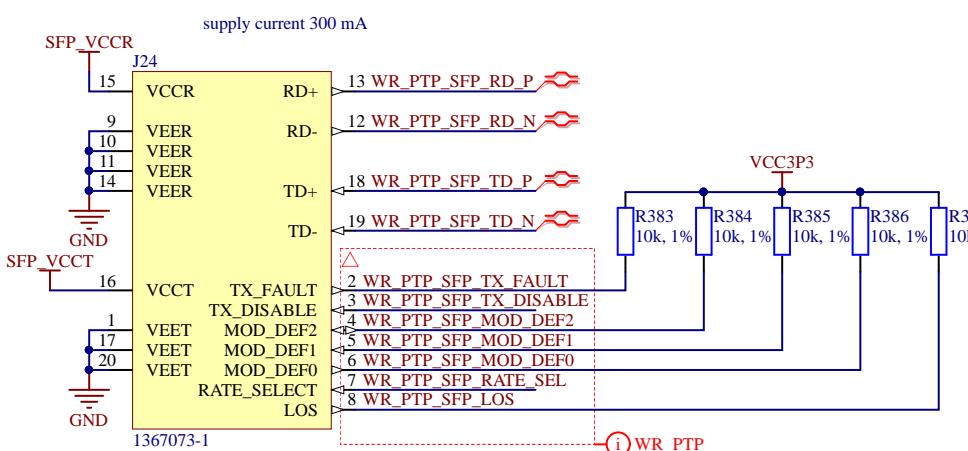
NF elements on sheet: R389, R394, C721, IC56, R395, R397, R398, R399, R400, R401, R402, R405, R408
Number of NF elements on sheet: 13

White Rabbit PTP

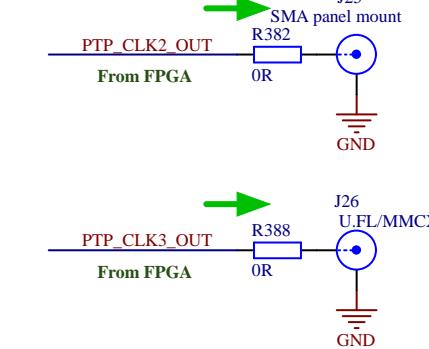
Power filters



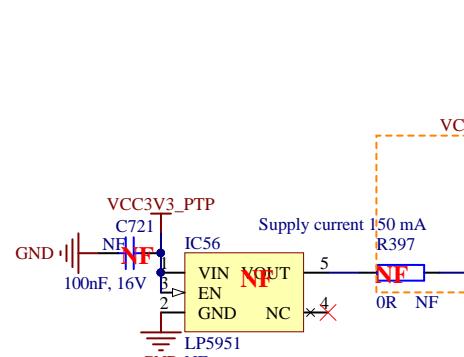
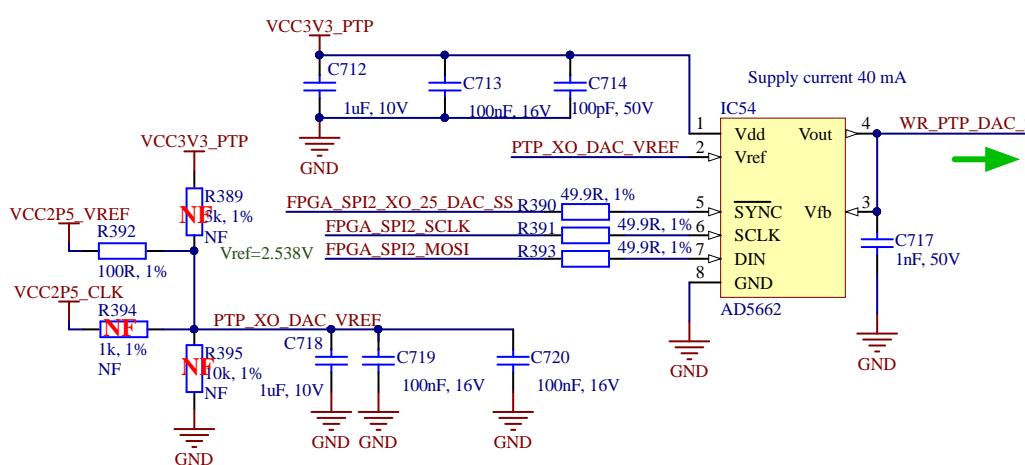
SFP connector



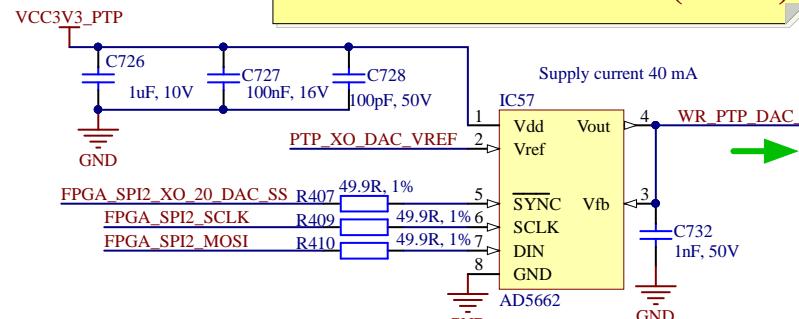
PTP CLK OUT



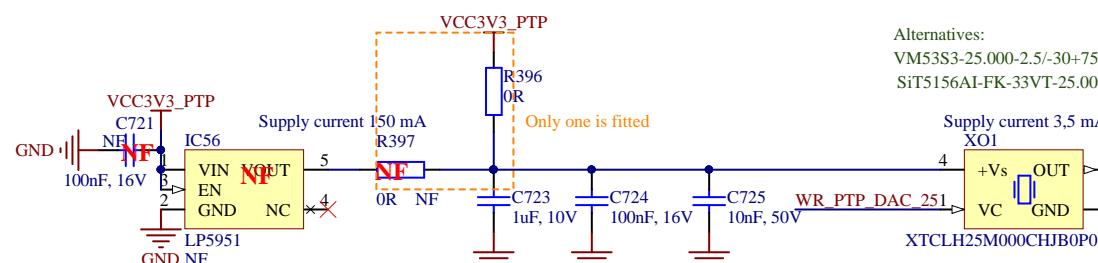
XO 25 MHz VC DAC (16 bit)



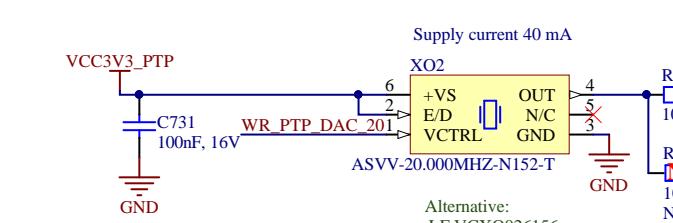
XO 20 MHz VC DAC (16 bit)



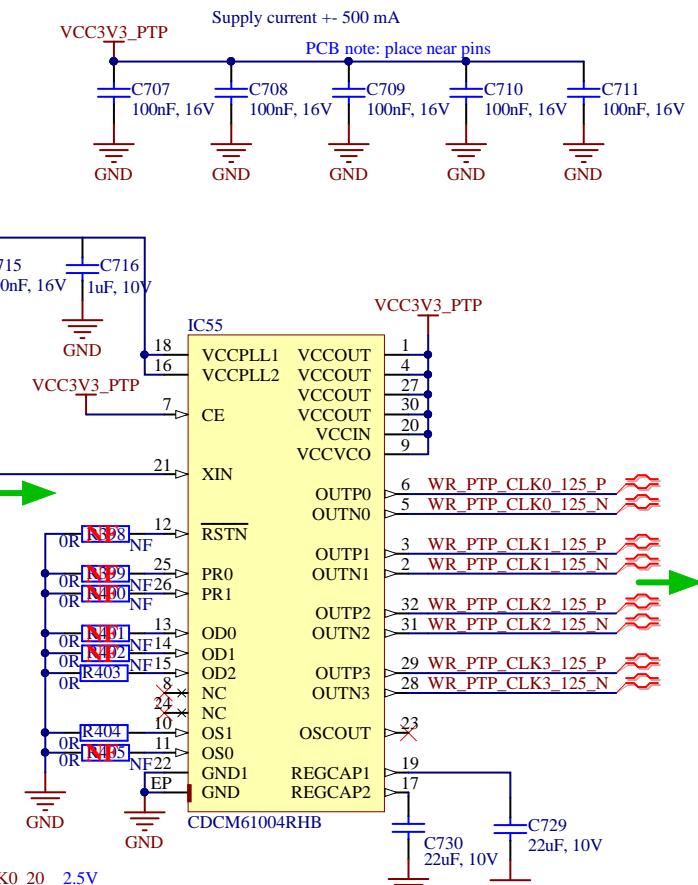
VCTCXO (25 MHz)



VCXO (20 MHz)



Frequency synthesizer



Config (pins have internal pull-ups):
Presc. div. = 4, feedback div. = 20 (PR [1 1])
Output divider = 4 (OD [0 1 1])
Output Type: LVDS, OSC_OUT Off (OS [0 1])

Project name: LimeSDR-X3_Inv0.PjrPcb

Title: White Rabbit PTP

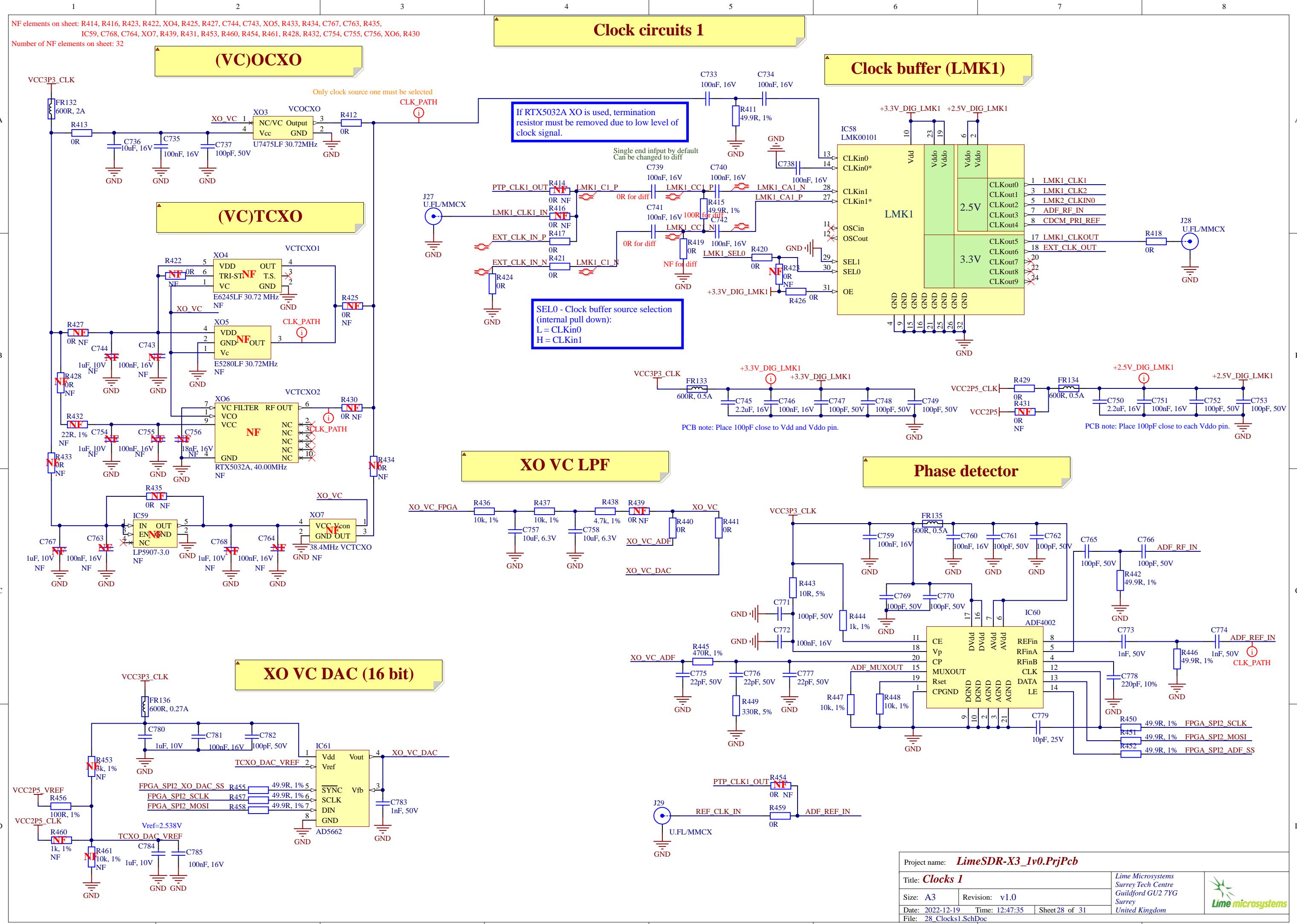
Size: A3 Revision: v1.0

Date: 2022-12-19 Time: 12:47:28 Sheet 27 of 31

File: 27_WR_PTP.SchDoc

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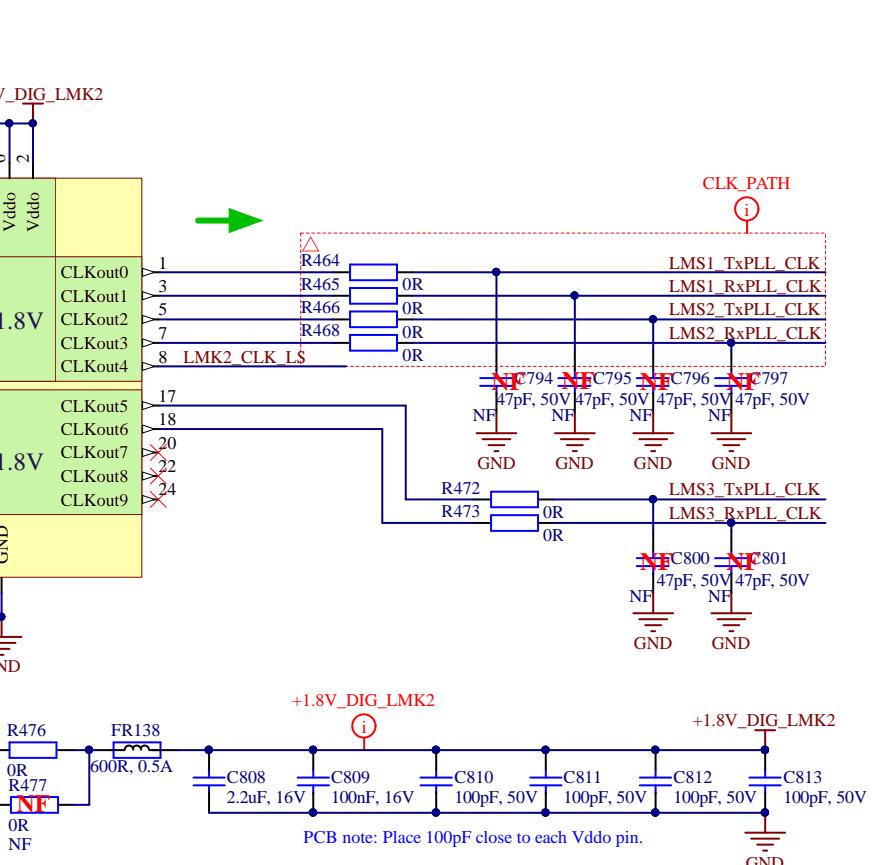
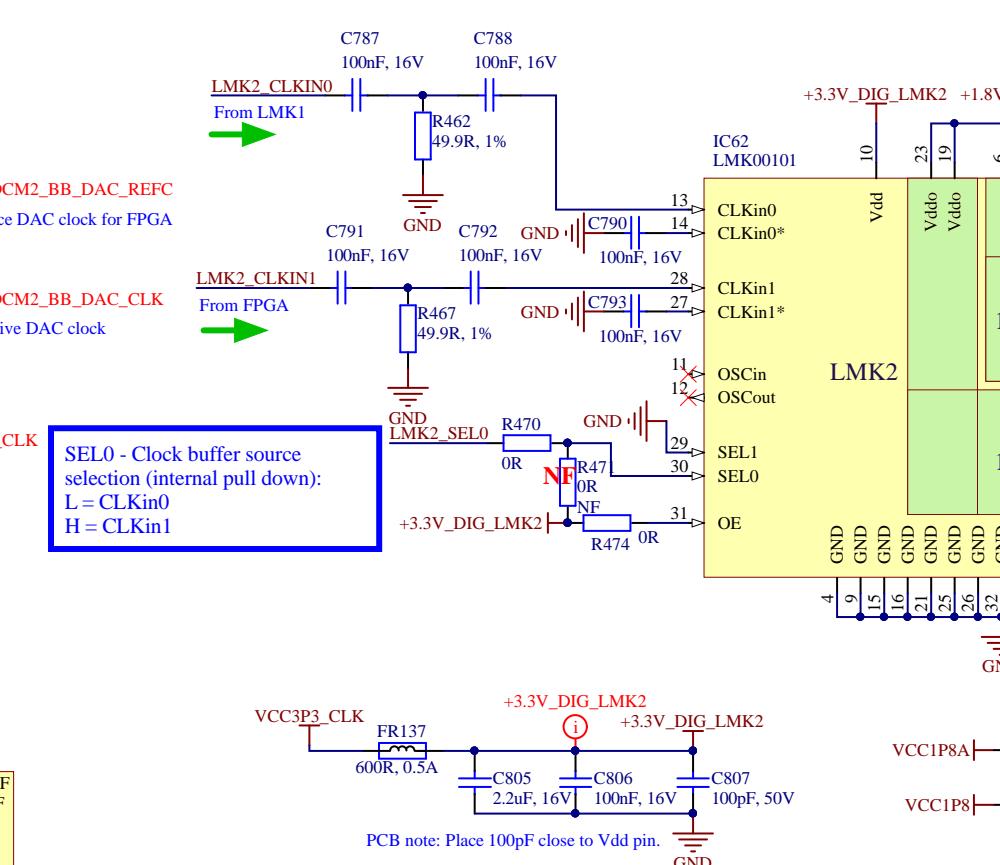
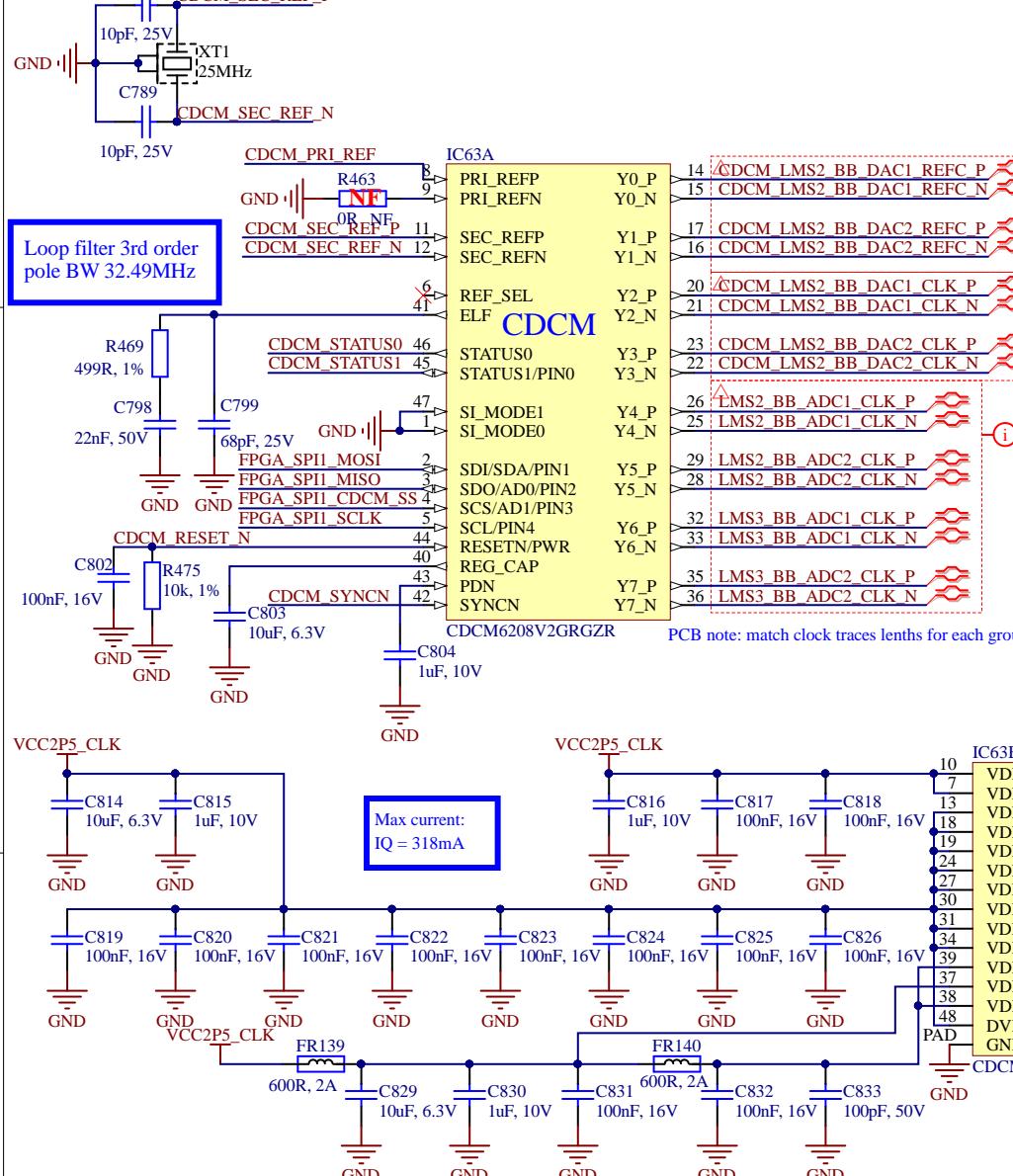




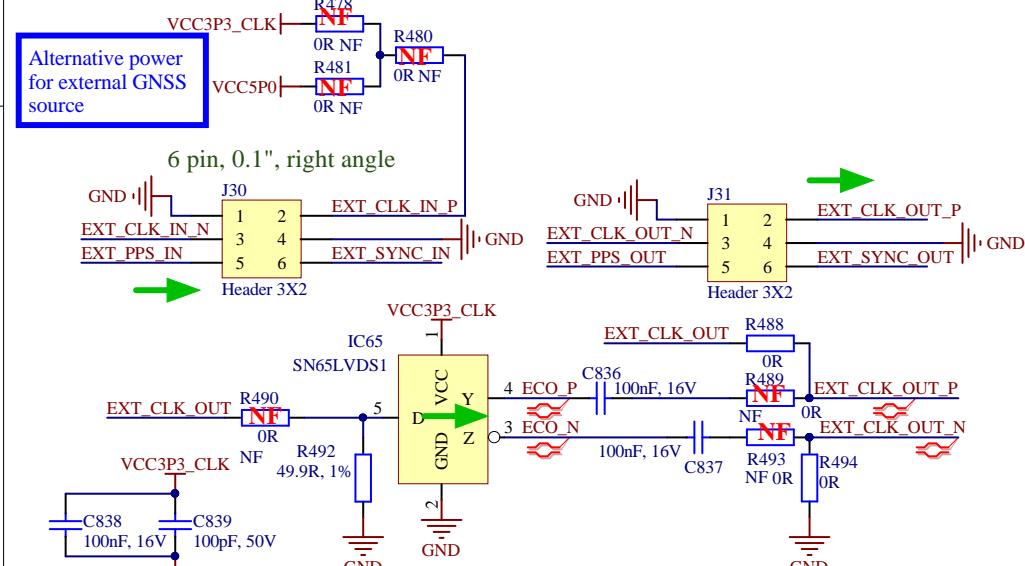
NF elements on sheet: R463, R471, C794, C795, C796, C797, C800, C801, R477, R478, R480, R481, R490, R489, R493, R482, R484, R491, R496, R486
Number of NF elements on sheet: 20

Clock circuits 3

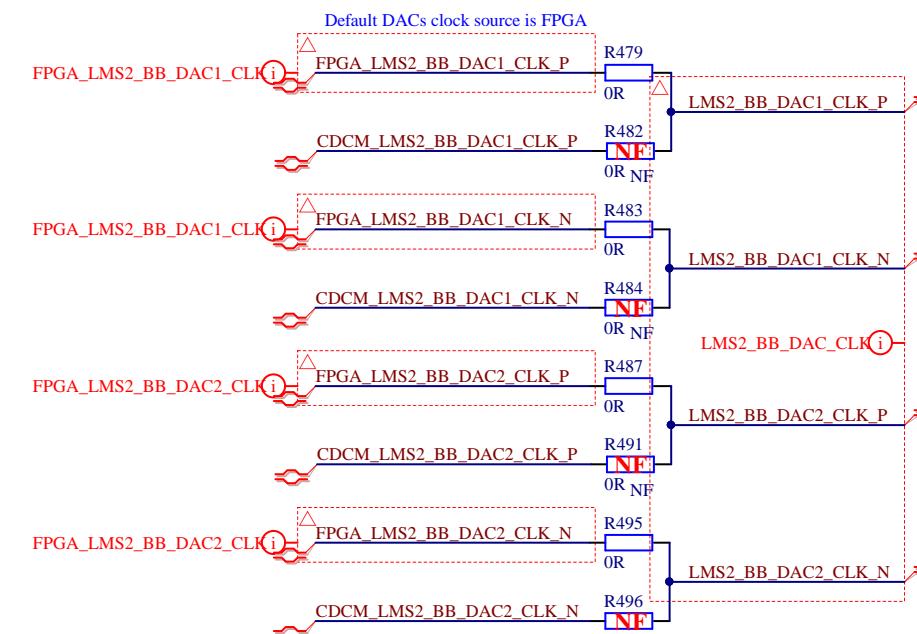
Clock generator for BB DACs, ADCs



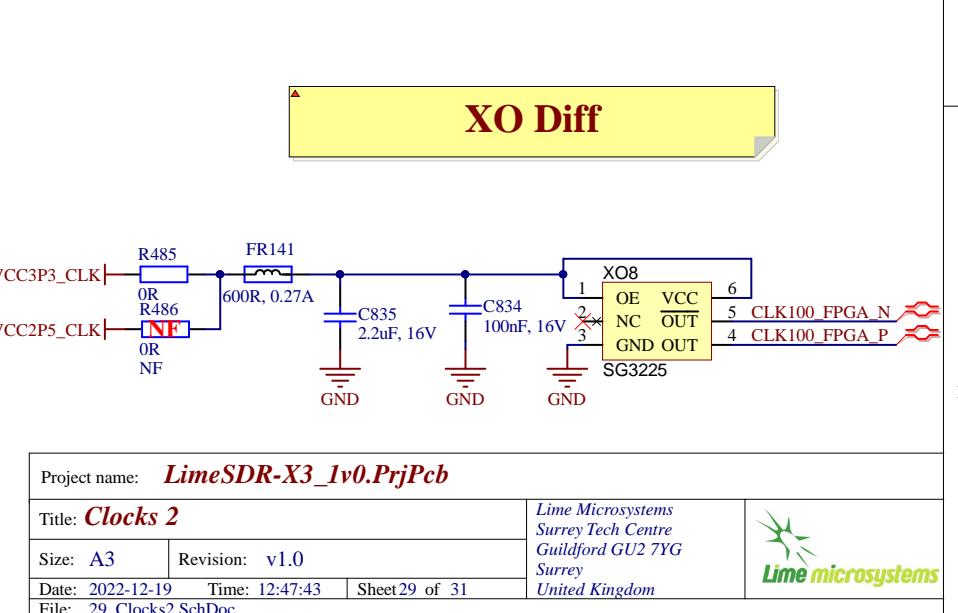
External sync In/Out



DACs clock source selection



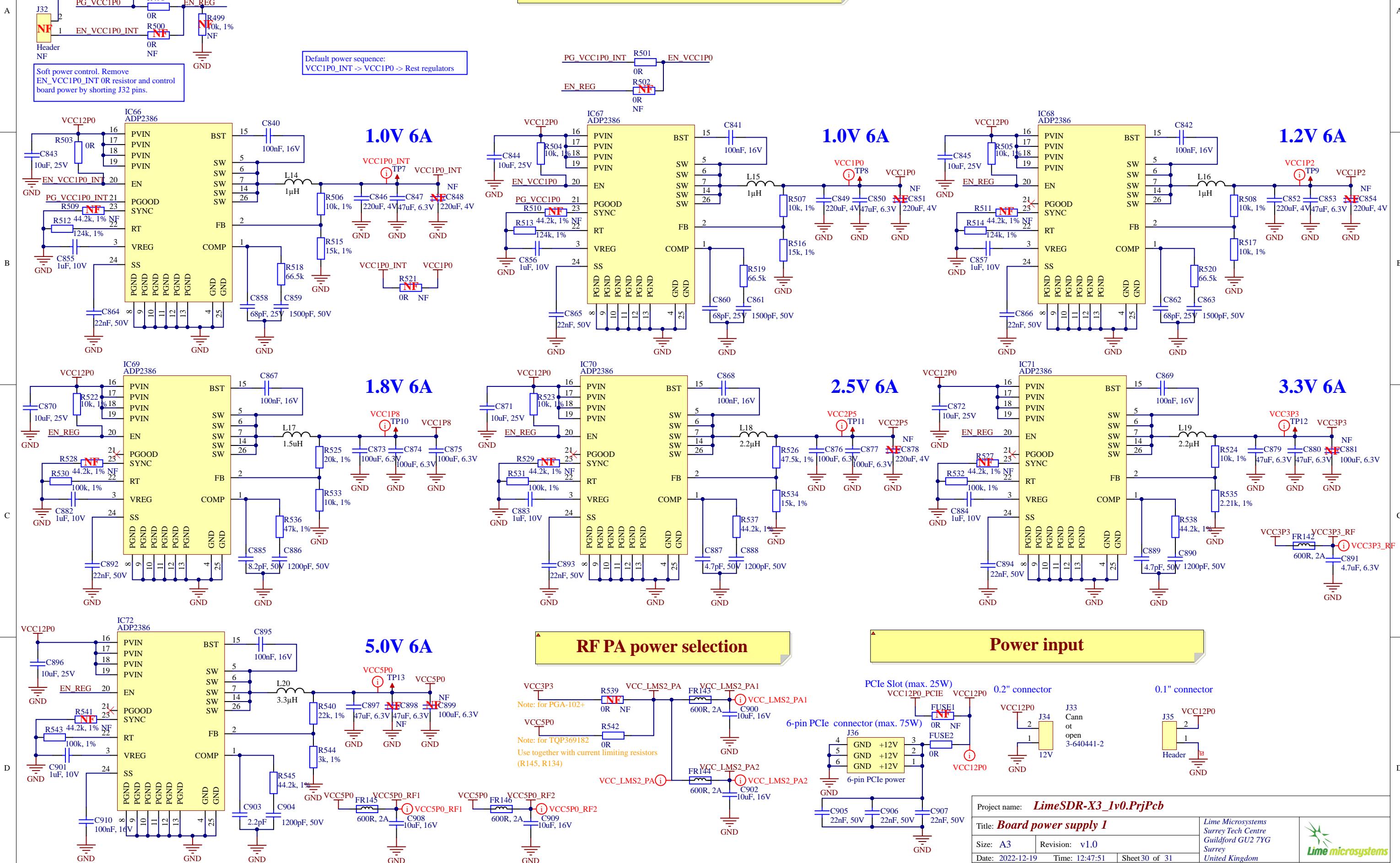
XO Diff



NF elements on sheet: J32, R500, R499, R509, C848, R521, R502, R510, C851, R511, C854, R528, R529, C878, R527, C881, R541, C898, C899, R539, FUSE1
Number of NF elements on sheet: 21

Board power circuits 1

Main switching regulators

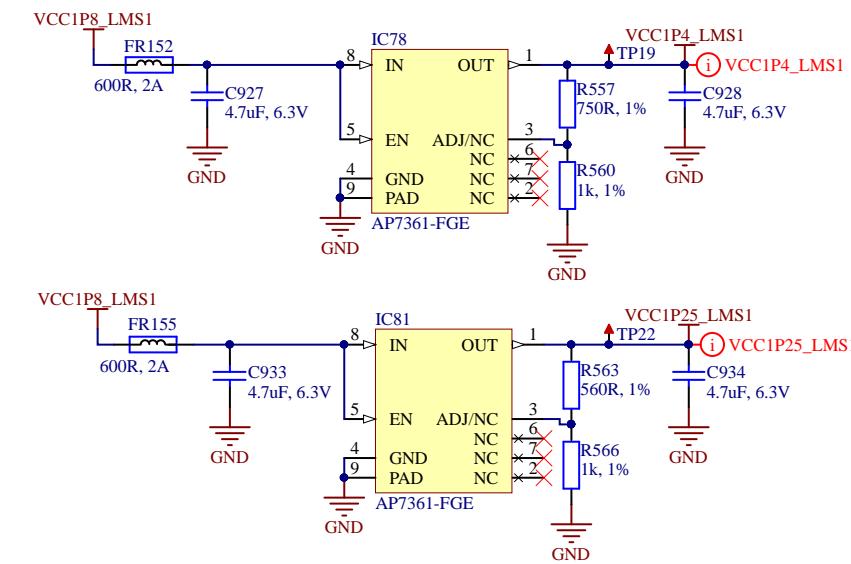
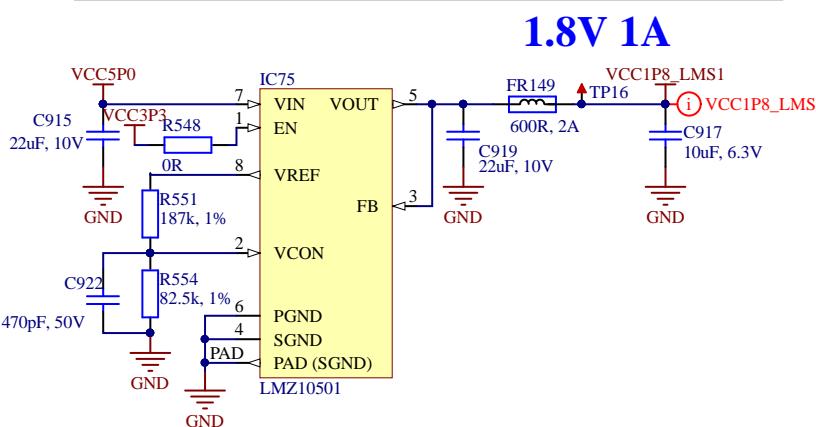


NF elements on sheet: FR156, FR157, R567, FR163, FR161, R573

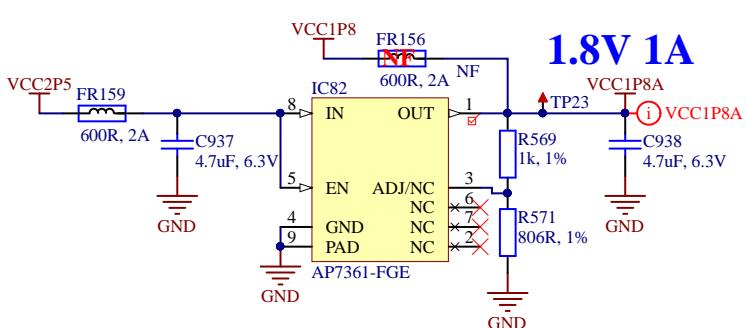
Number of NF elements on sheet: 6

Total number of NF elements on all sheets: 172

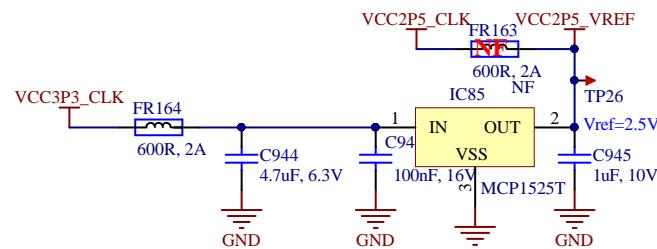
LMS 1



Misc power

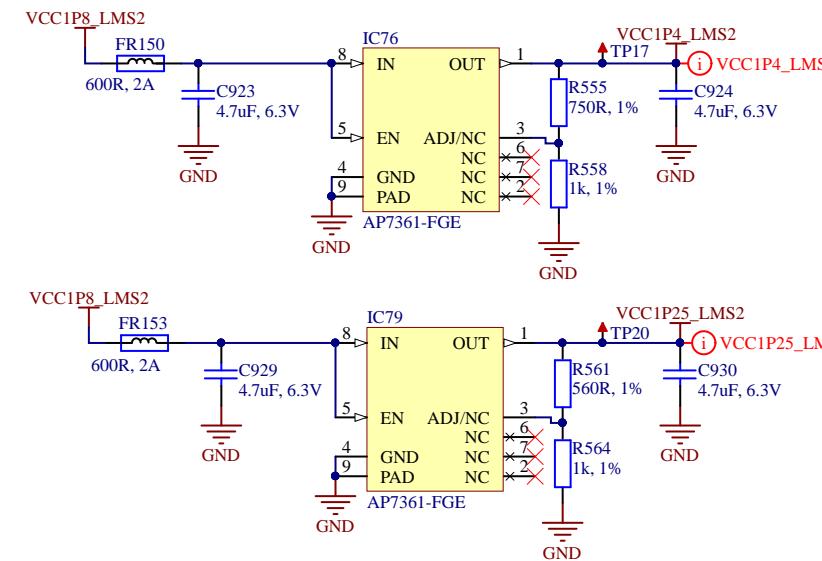
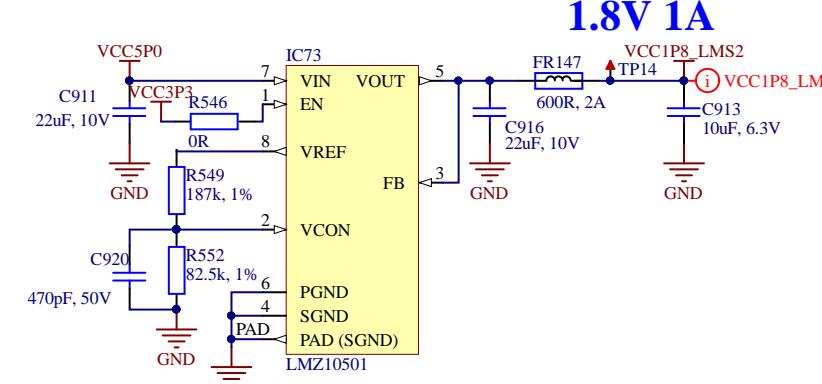


Voltage reference (2.5V)

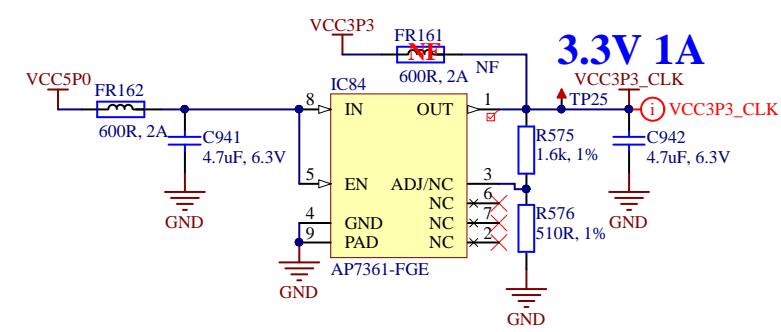
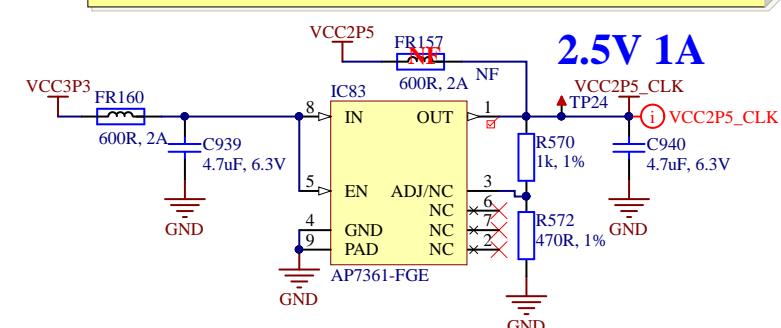


Board power circuits 2

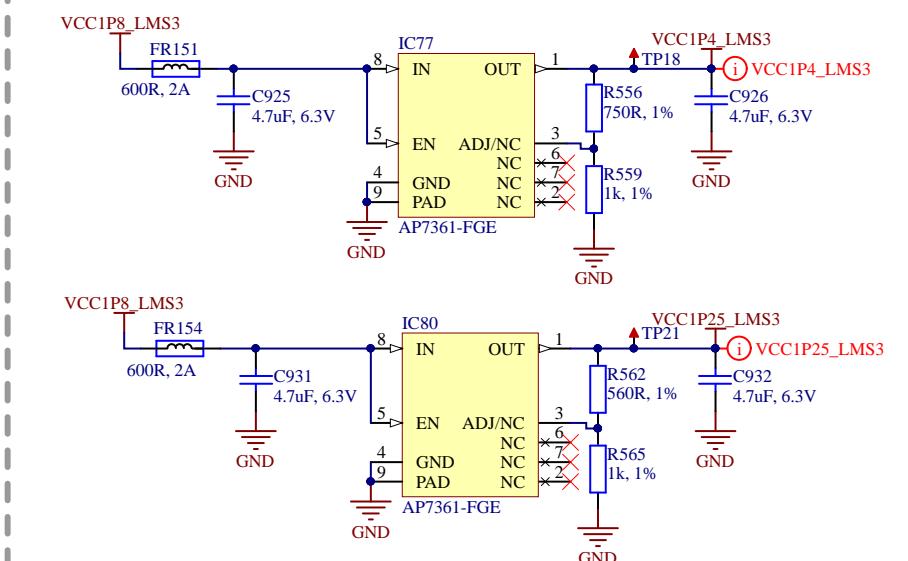
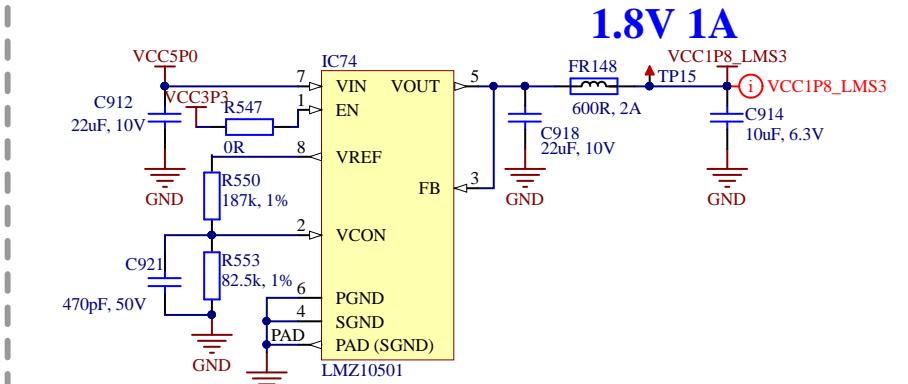
LMS 2



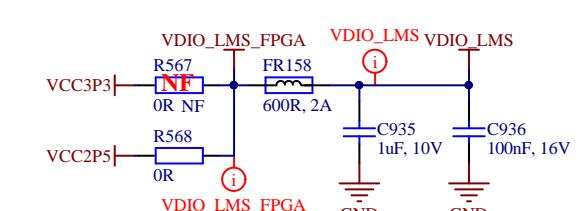
Clock network power



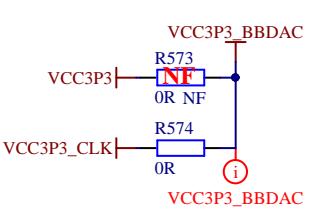
LMS 3



LMS VDIO power selection



VCC3P3_BBDAC power selection



Project name: LimeSDR-X3_1v0.PrbPcb

Title: Board power supply 2

Size: A3 Revision: v1.0

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File: 31_Power2.SchDoc

