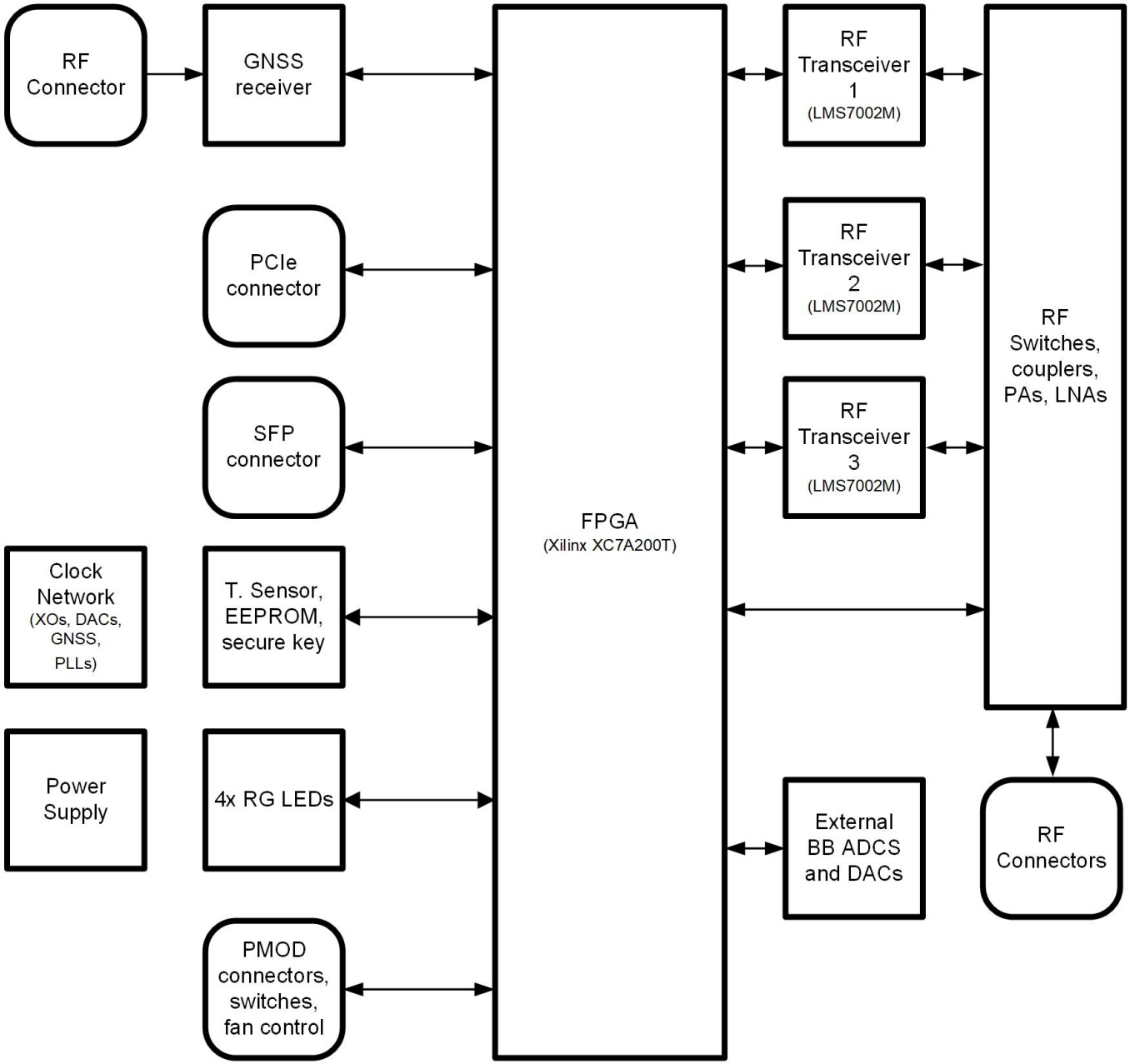
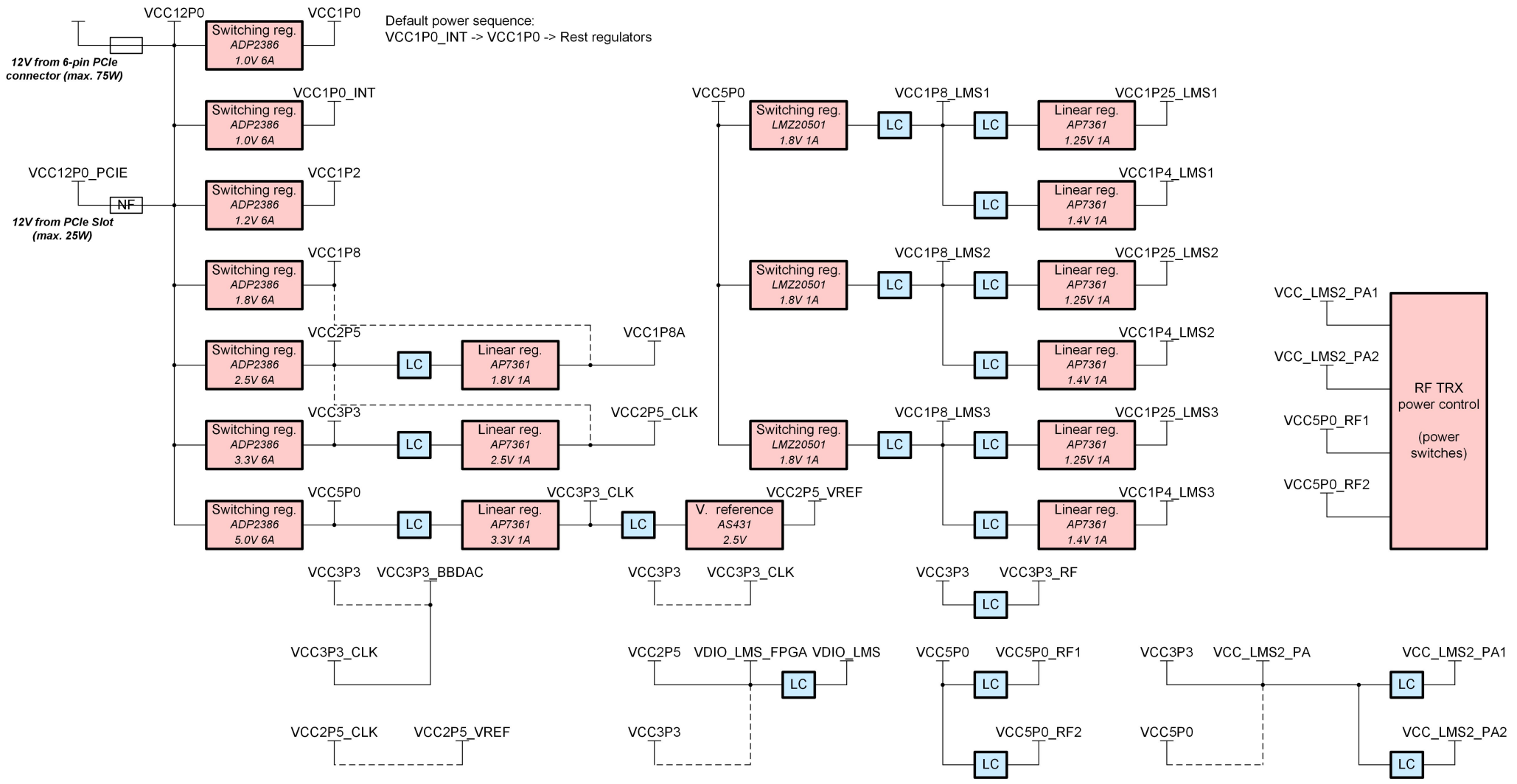
Block diagram



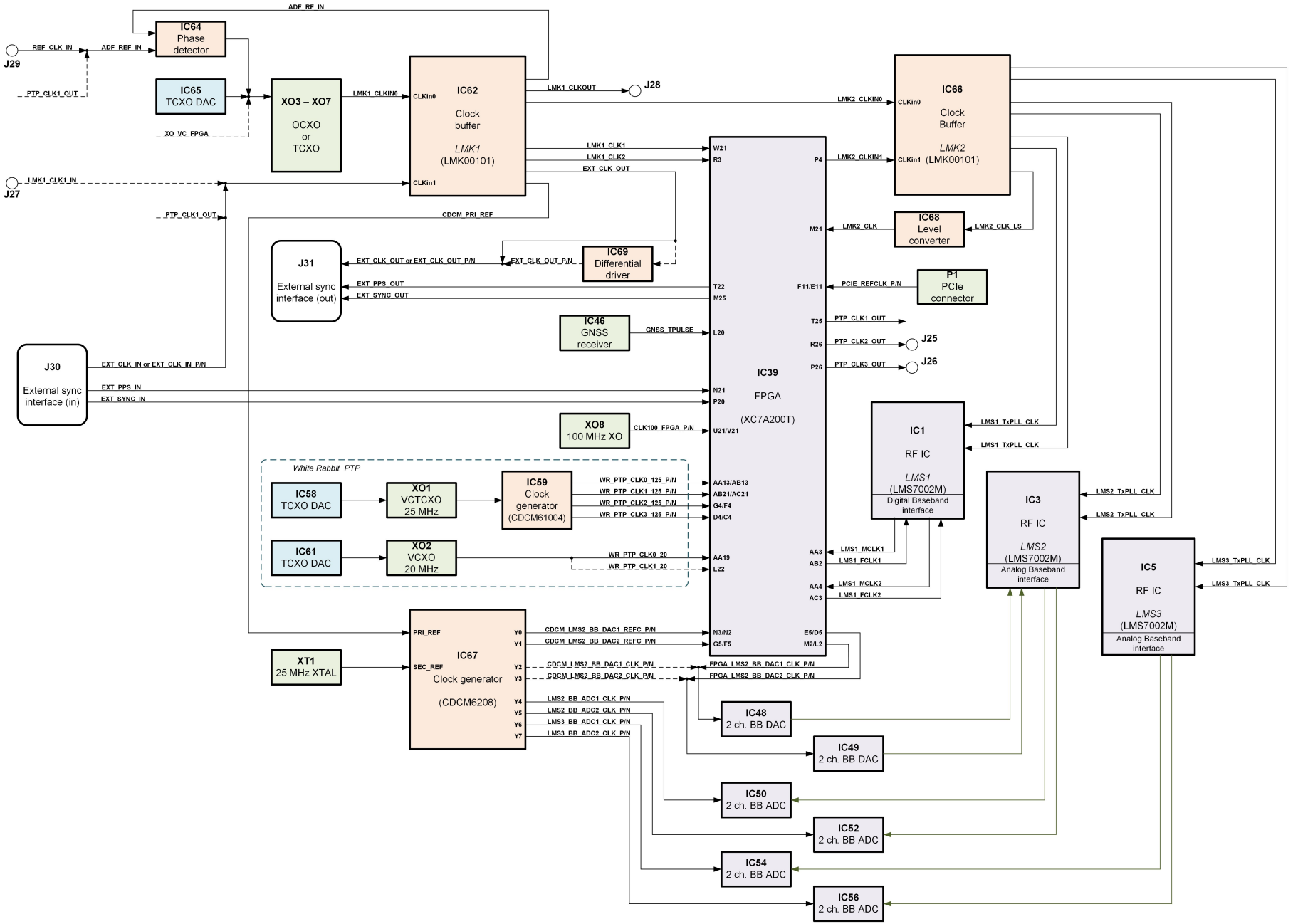
Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*Block diagram*		*Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom*
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:26:30	Sheet 1 of 11	
File: 01_BlockDiagram.SchDoc			

Power diagram



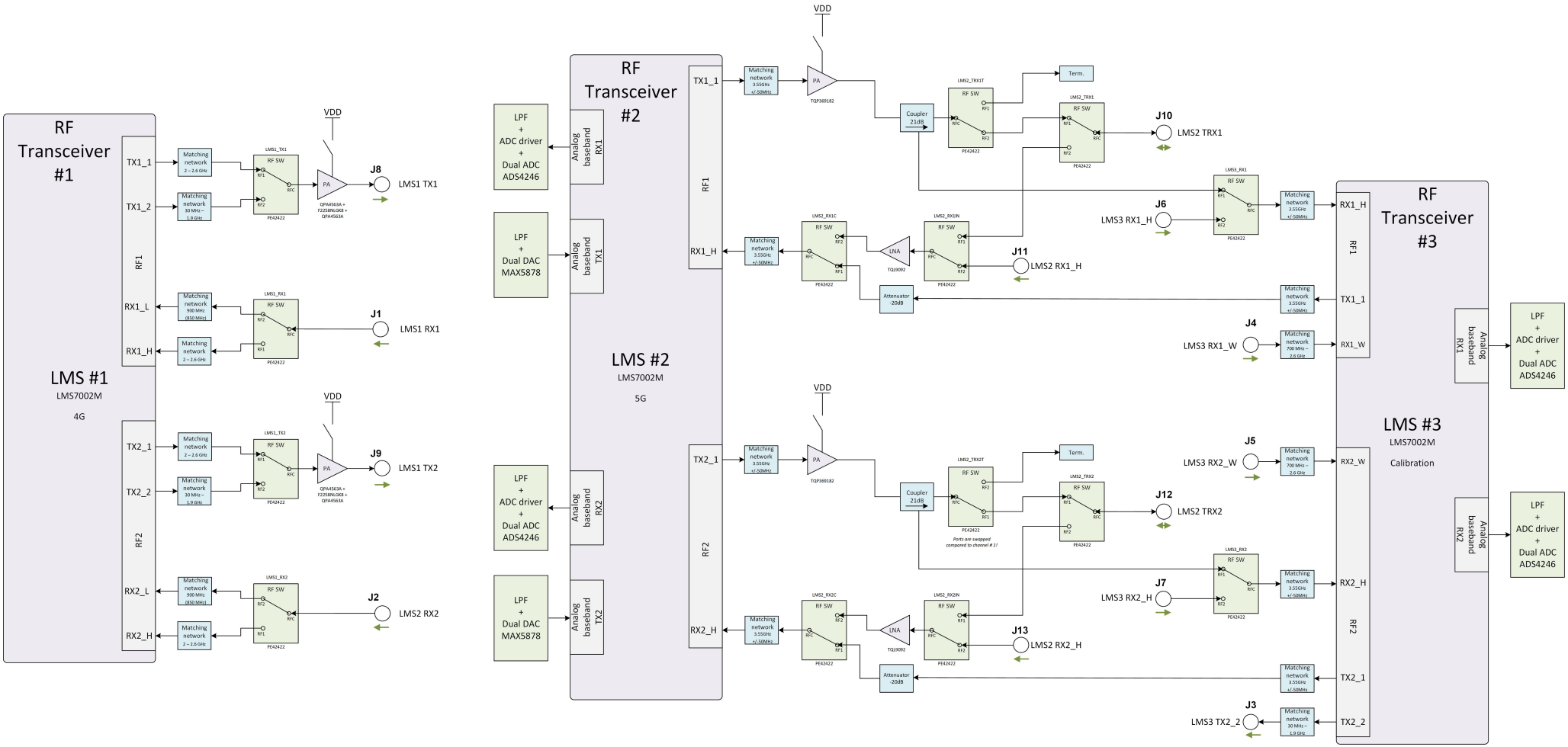
Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	***Power diagram***		*Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom*
Size: A3	Revision: v1.1		Lime microsystems
Date: 2024-06-11	Time: 10:26:33	Sheet 2 of 11	
File: 02_PowerDiagram.SchDoc			

Clock diagram



Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*Clock diagram*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:26:39	Sheet 3 of 11	
File: 03_ClockDiagram.SchDoc			

RF diagram



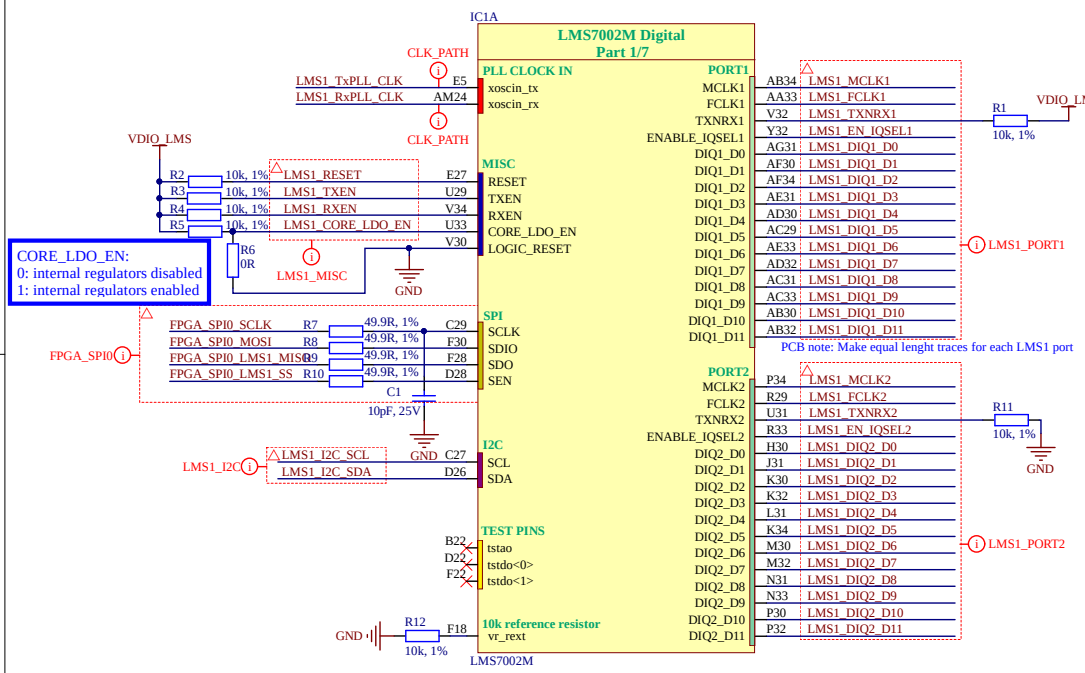
Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*RF diagram*	*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*	Lime microsystems
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:26:47	Sheet 1 of 11	
File: 04_RFDiagram.SchDoc			

NF elements on sheet: MECH15, MECH16, MECH17, MECH18
Number of NF elements on sheet: 4

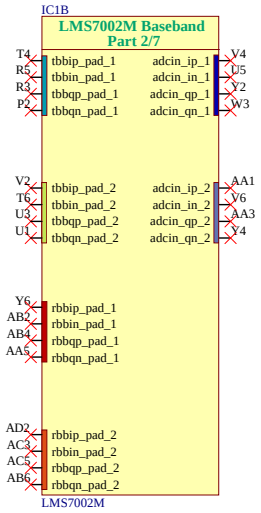
LMS7002M misc

LMS1_ (4G)

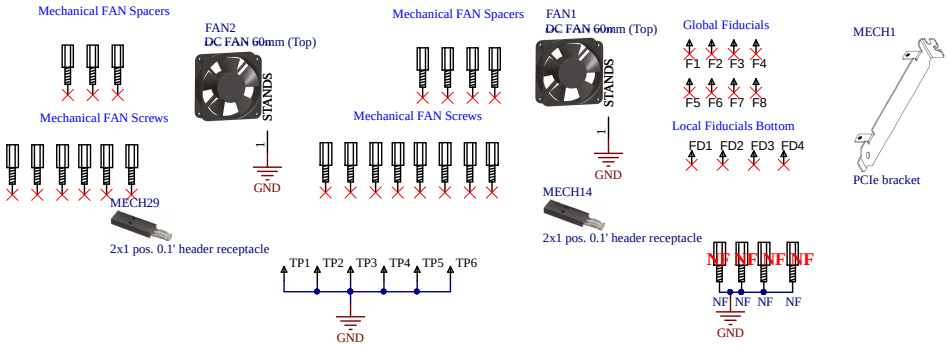
Digital interfaces



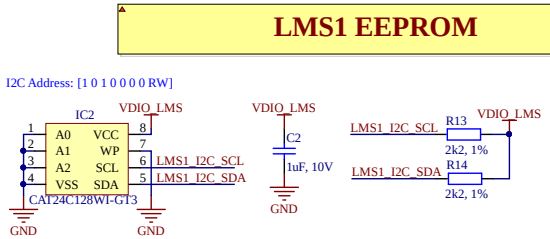
Baseband external IO



Mechanical



LMS1 EEPROM



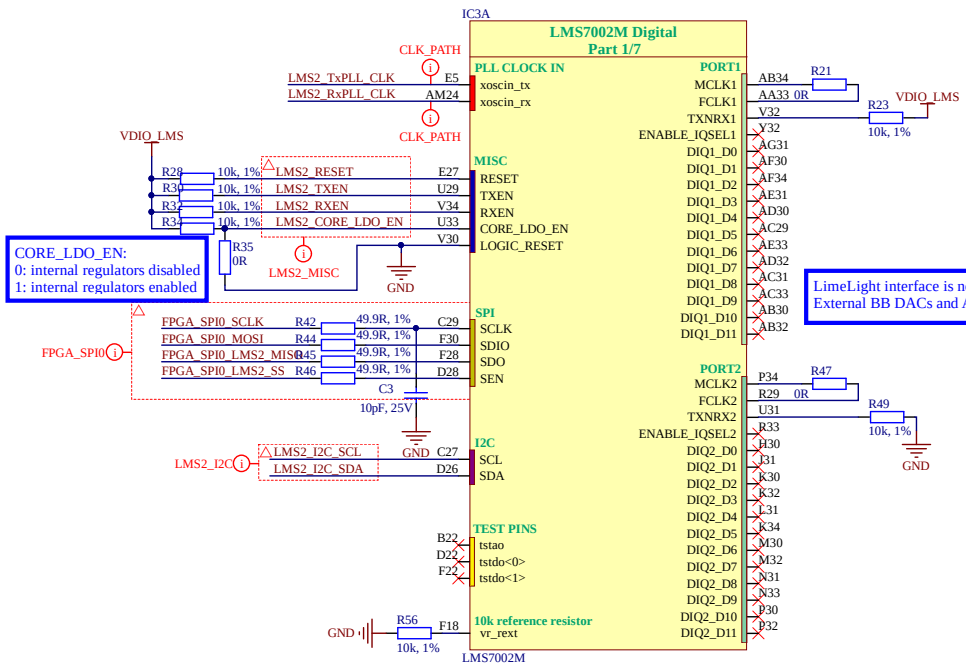
Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*LMS7002M misc (LMS1)*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		Lime microsystems
Date: 2024-06-11	Time: 10:26:56	Sheet 5 of 31	
File: 05_LMS1_Misc.SchDoc			

NF elements on sheet: -
Number of NF elements on sheet: 0

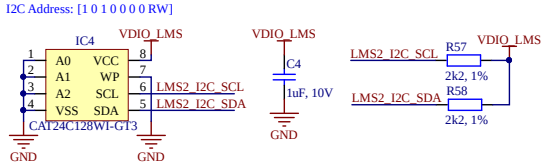
LMS7002M misc

LMS2_ (5G)

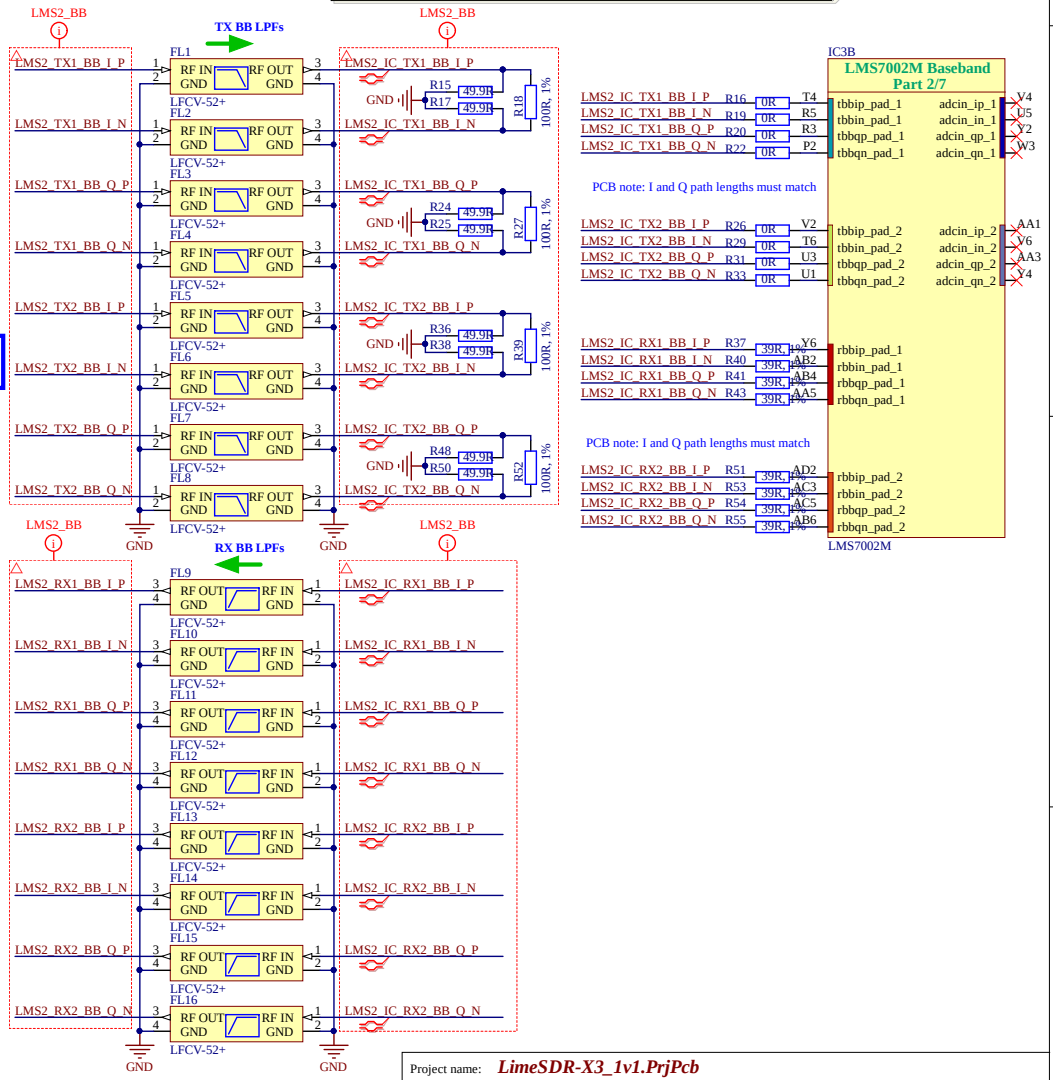
Digital interfaces



LMS2 EEPROM



Baseband external IO



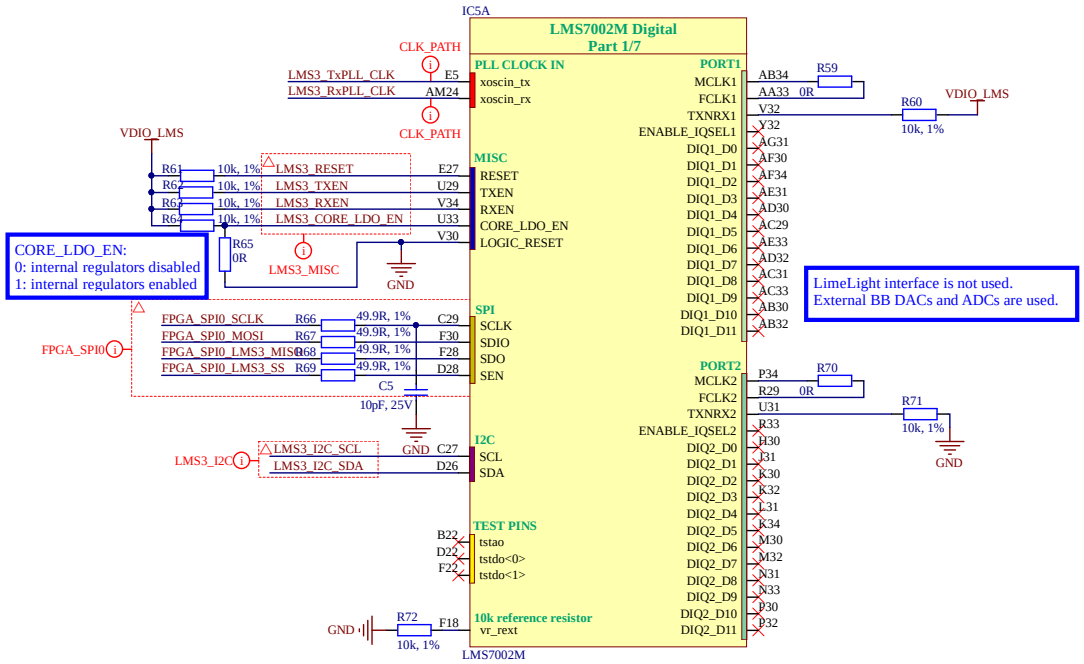
Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*LMS7002M misc (LMS2)*		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Revision: v1.1		Lime microsystems
Date: 2024-06-11	Time: 10:26:58	Sheet 6 of 31	
File: 06_LMS2_Misc.SchDoc			

NF elements on sheet: -
Number of NF elements on sheet: 0

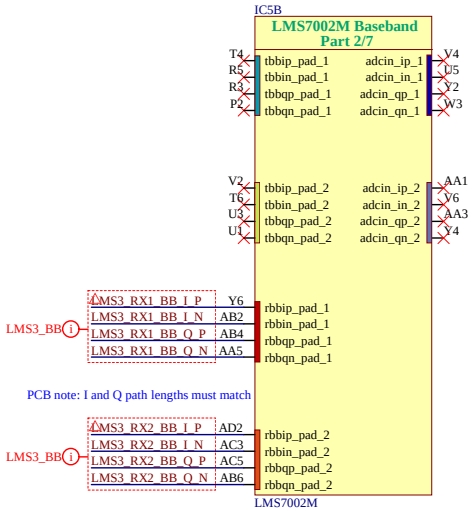
LMS7002M misc

LMS3_ (Calibration)

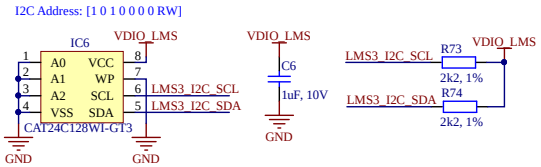
Digital interfaces



Baseband external IO



LMS3 EEPROM



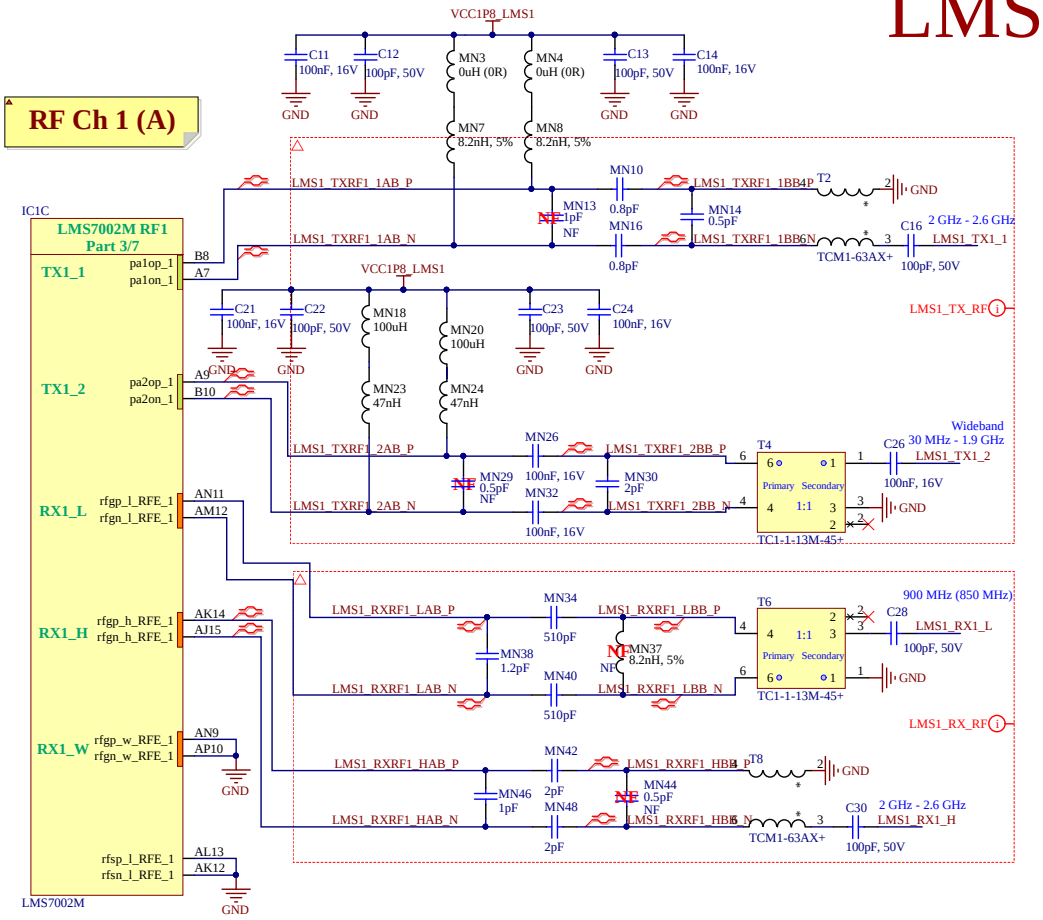
Project name: *LimeSDR-X3_1v1.PrjPcb*			
Title: *LMS7002M misc (LMS1)*			Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:27:00	Sheet 7 of 31	
File: 07_LMS3_Misc.SchDoc			

NF elements on sheet: MN11, MN13, MN27, MN29, MN35, MN37, MN43, MN44, ESD1, ESD2
Number of NF elements on sheet: 10

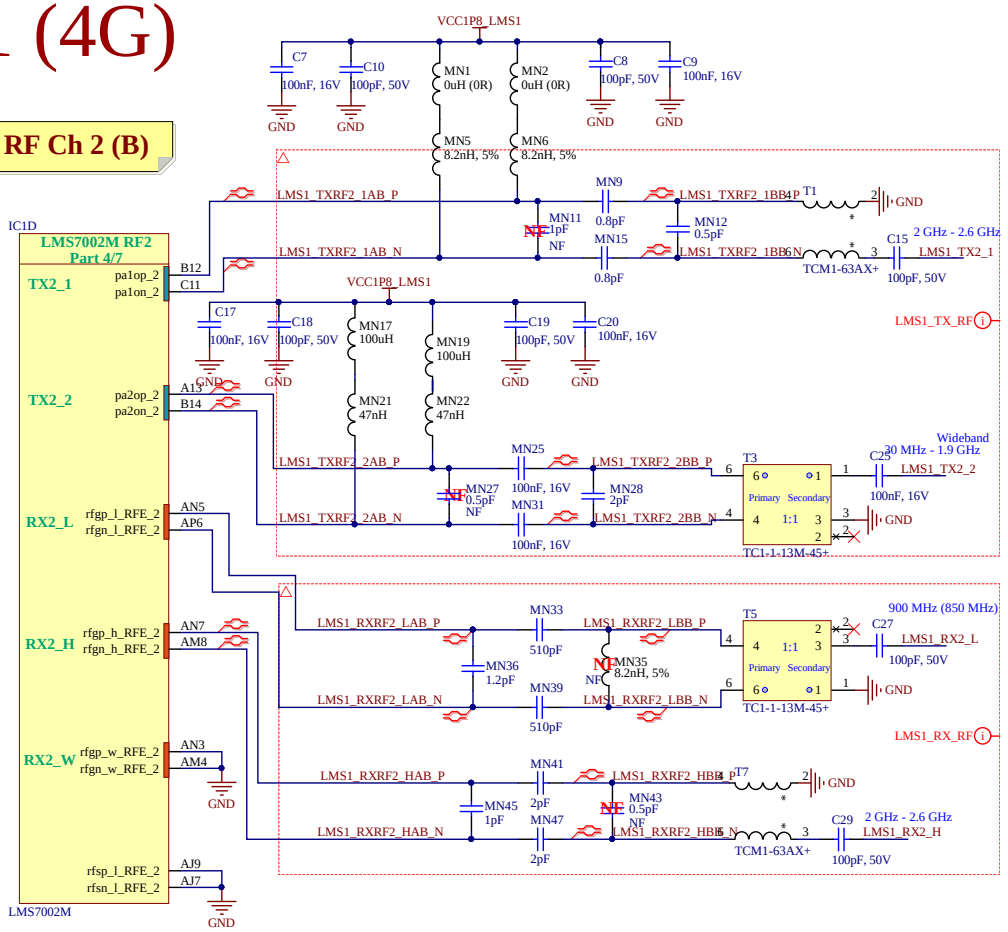
LMS7002M RF circuits (LMS1)

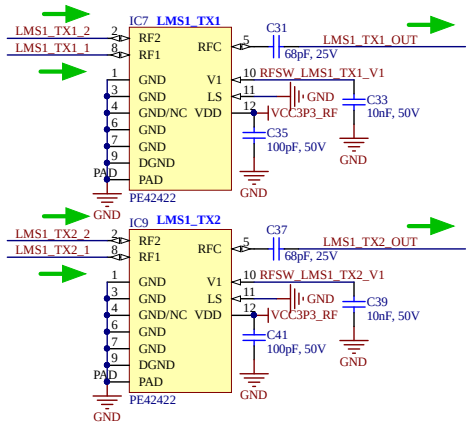
LMS1 (4G)

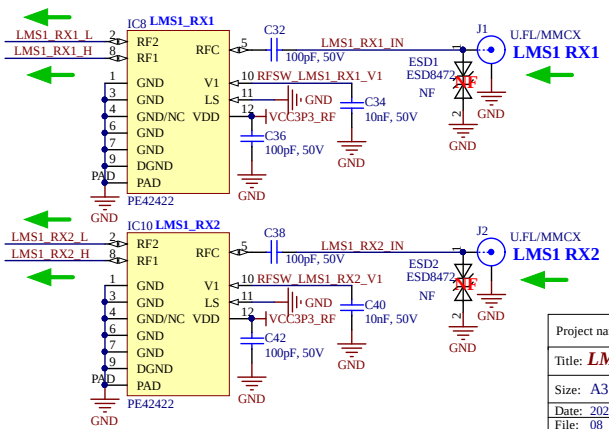
RF Ch 1 (A)



RF Ch 2 (B)







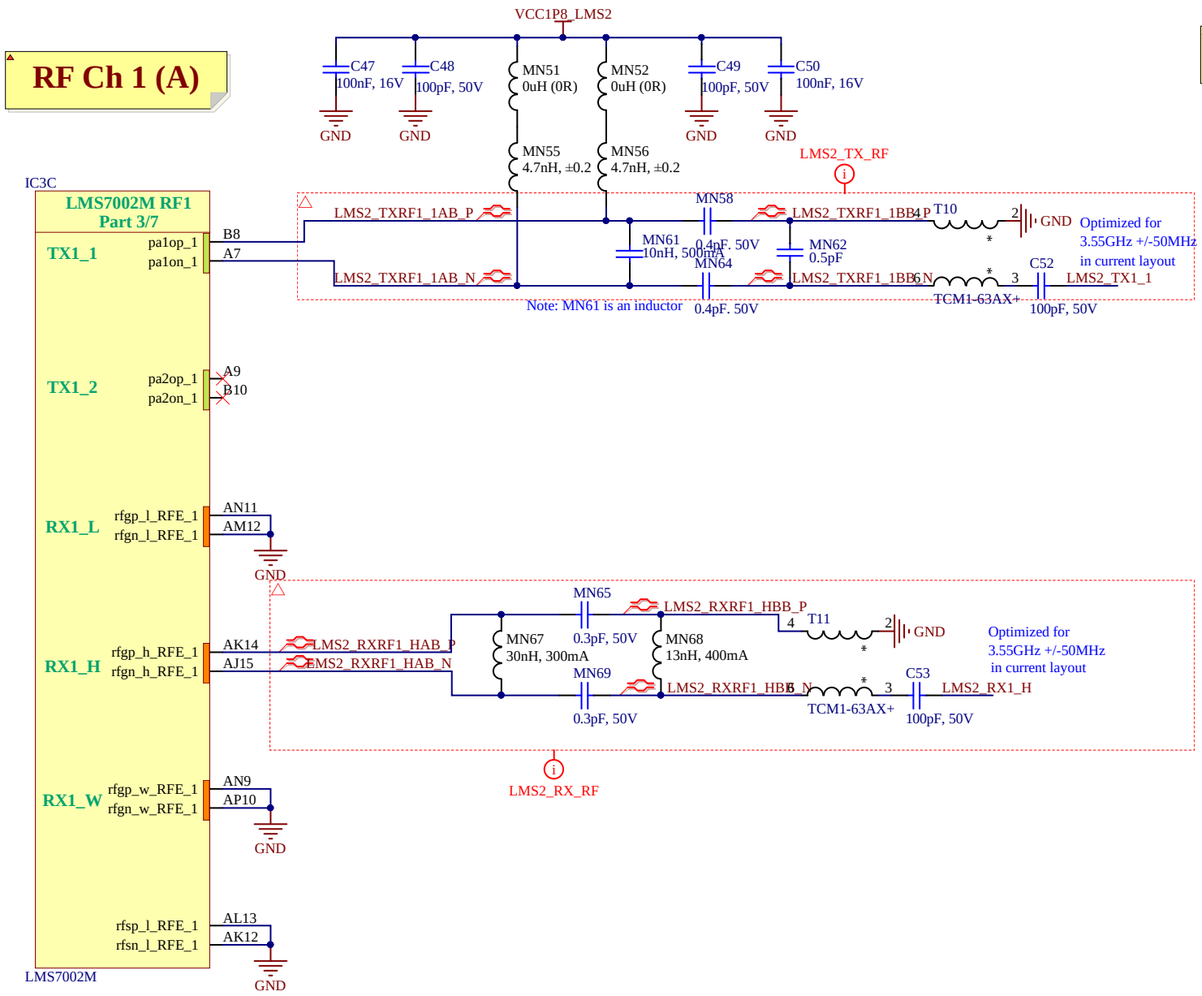
Project name:	LimeSDR-X3_1v1.PrjPcb		
Title:	LMS7002M RF (LMS1)	Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom	Lime microsystems
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:27:03	Sheet 8 of 31	
File: 08_LMS1_RF.SchDoc			

NF elements on sheet: -
Number of NF elements on sheet: 0

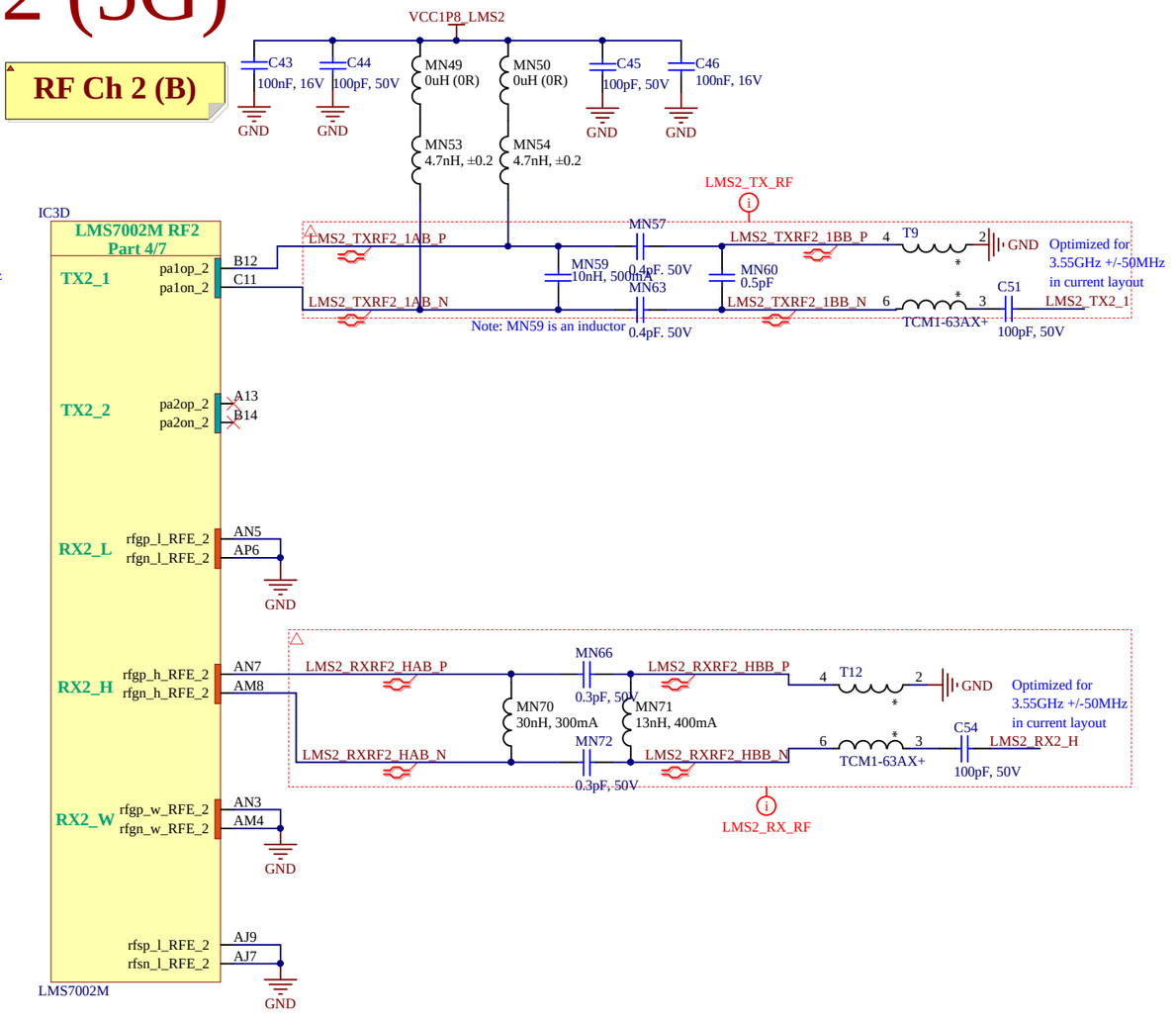
LMS7002M RF circuits (LMS2)

LMS2 (5G)

RF Ch 1 (A)



RF Ch 2 (B)



Project name:	*LimeSDR-X3_1v1.PrjPcb*
Title:	*LMS7002M RF (LMS2)*
Size:	A3
Revision:	v1.1
Date:	2024-06-11
Time:	10:27:06
Sheet	9 of 31
File:	09_LMS2_RF.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

Lime microsystems

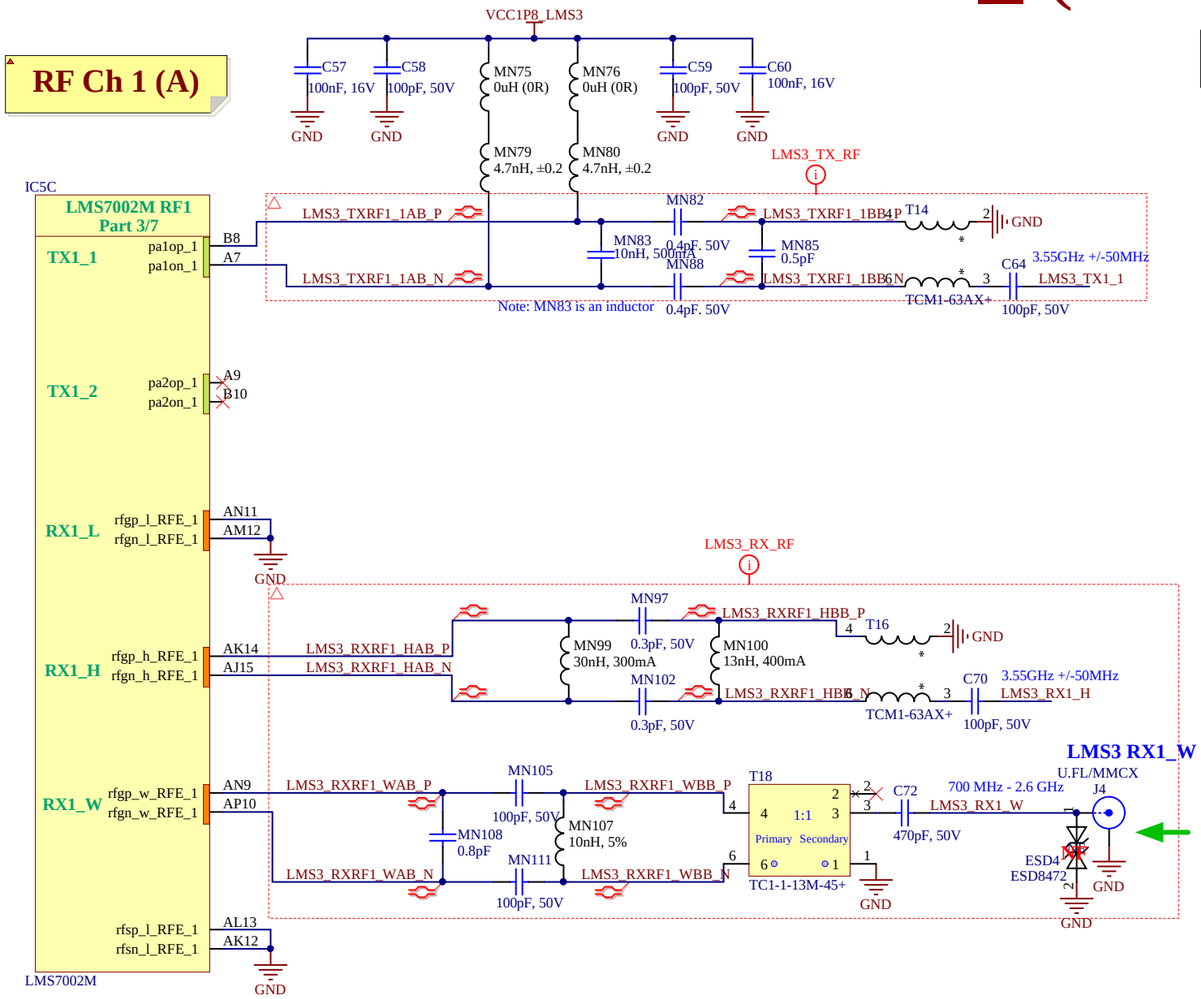
NF elements on sheet: MN94, ESD3, ESD4, ESD5, ESD6, ESD7

Number of NF elements on sheet: 6

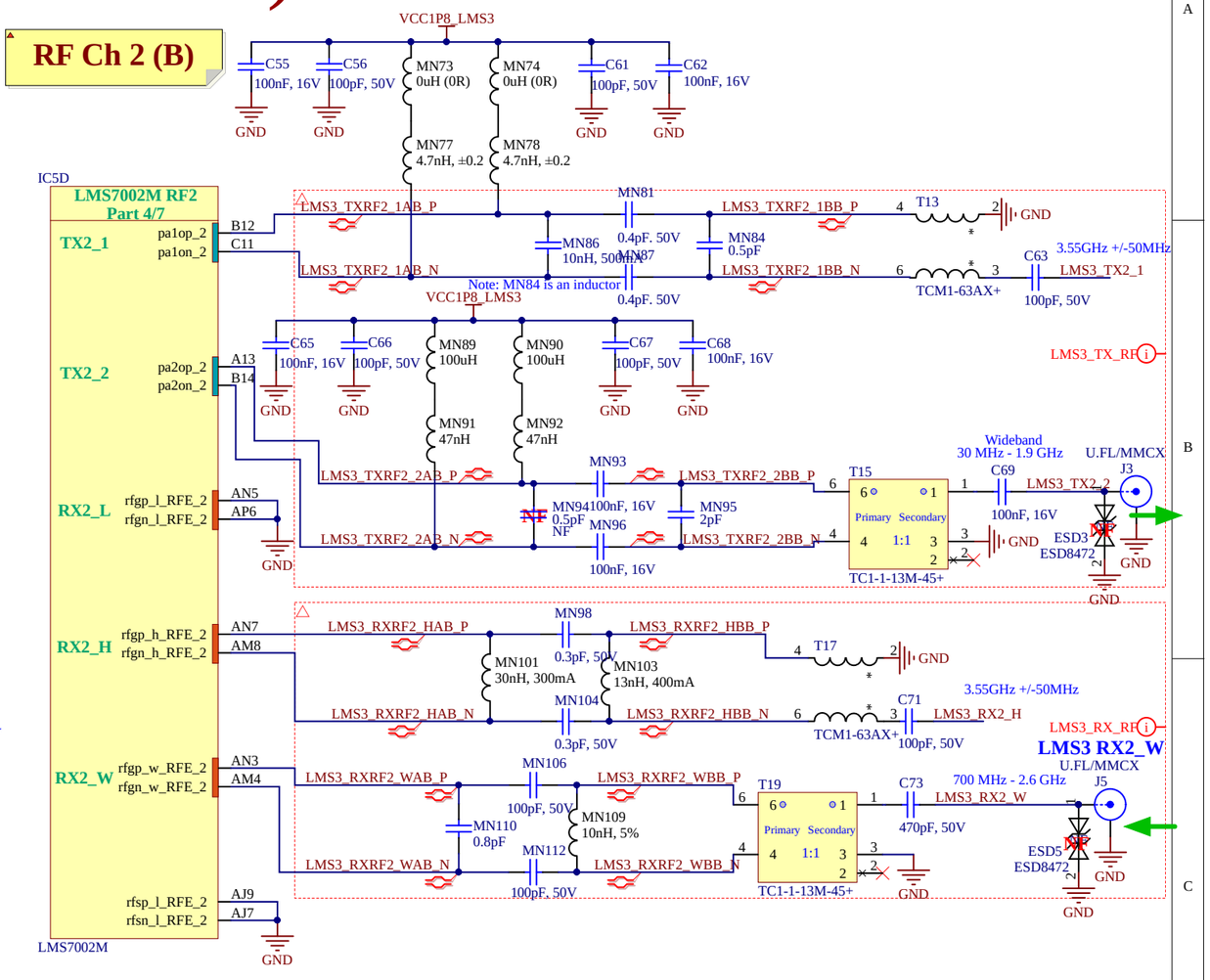
LMS7002M RF circuits (LMS3)

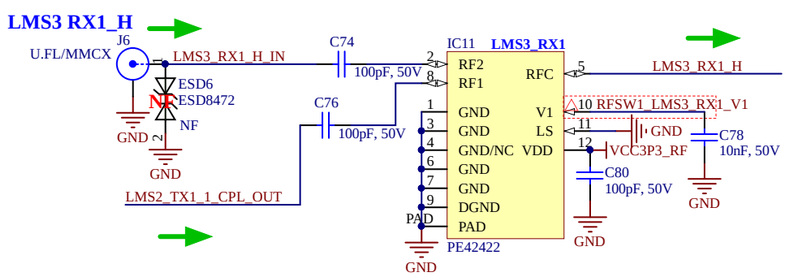
LMS3_ (Calibration)

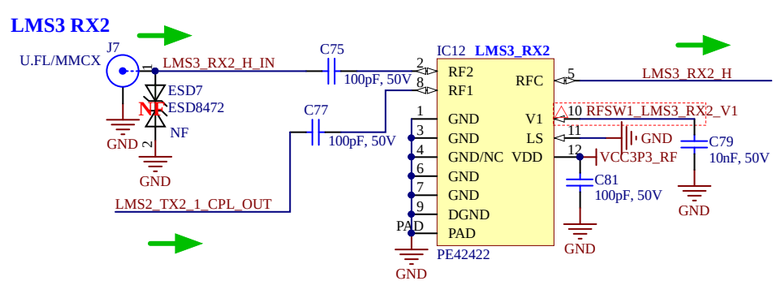
RF Ch 1 (A)



RF Ch 2 (B)







Project name:	*LimeSDR-X3_1v1.PrjPcb*
Title:	*LMS7002M RF (LMS3)*
Size:	A3
Revision:	v1.1
Date:	2024-06-11
Time:	10:27:09
Sheet	10 of 31
File:	10_LMS3_RF.SchDoc

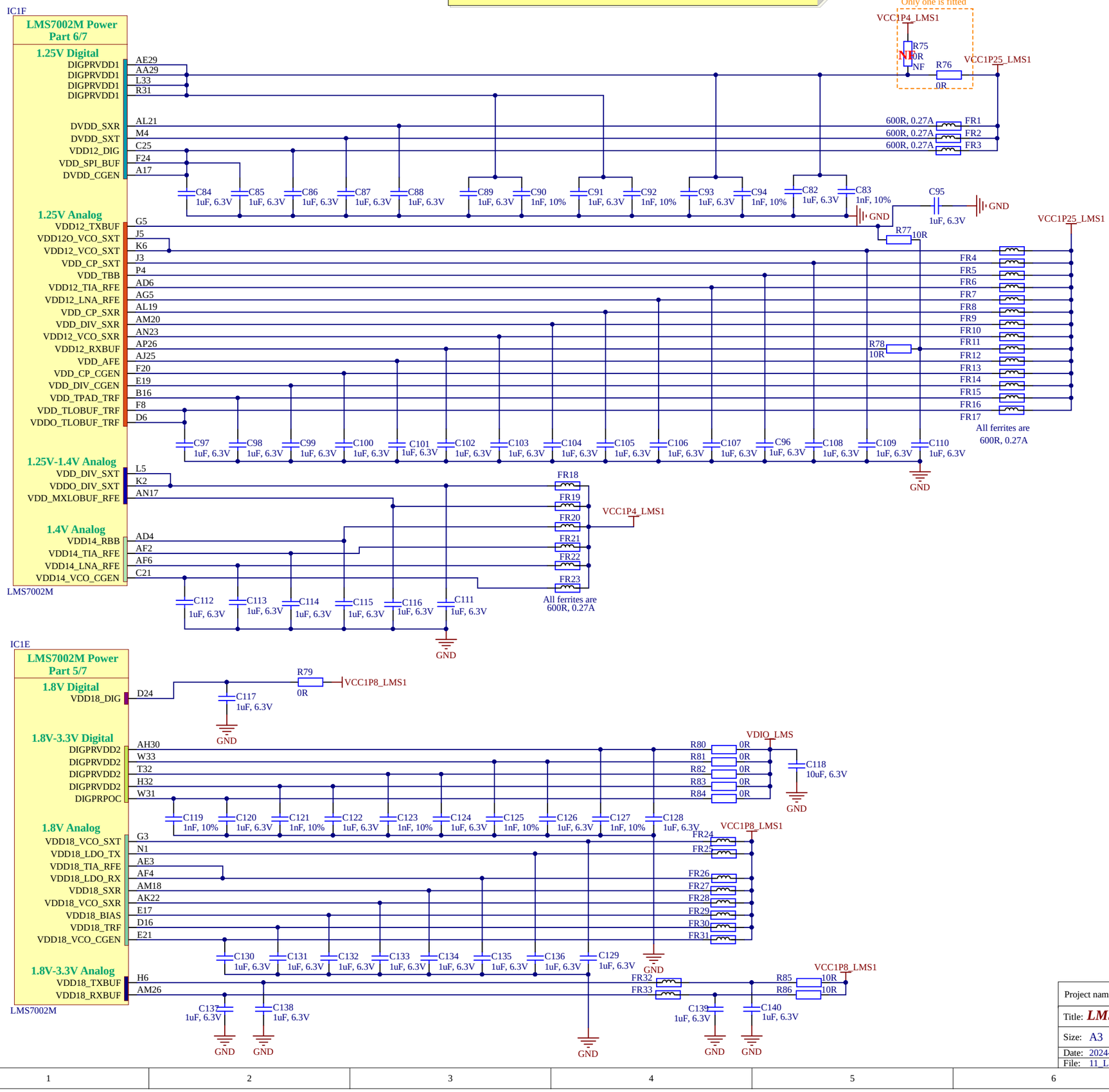
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

Lime microsystems

NF elements on sheet: R75

Number of NF elements on sheet: 1

LMS7002M power supply circuit (LMS1)



Project name:	***LimeSDR-X3_1v1.PrjPcb***		
Title:	***LMS7002M power supply (LMS1)***		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:27:12	Sheet 10 of 31	
File: 11_LMS1_Power.SchDoc			

NF elements on sheet: R87

Number of NF elements on sheet: 1

LMS7002M power supply circuit (LMS2)

IC3F

LMS7002M Power Part 6/7

1.25V Digital

DIGPRVDD1 — AE29, AA29, L33, R31

DVDD_SXR — AL21

DVDD_SXT — M4

VDD12_DIG — C25

VDD_SPI_BUF — F24

DVDD_CGEN — A17

Only one is fitted

VCC1P4_LMS2 — R87 NF / NF 0R — R88 0R — VCC1P25_LMS2

600R, 0.27A — FR34

600R, 0.27A — FR35

600R, 0.27A — FR36

C143 1uF, 6.3V; C144 1uF, 6.3V; C145 1uF, 6.3V; C146 1uF, 6.3V; C147 1uF, 6.3V; C148 1uF, 6.3V; C149 1nF, 10%; C150 1uF, 6.3V; C151 1nF, 10%; C152 1uF, 6.3V; C153 1nF, 10%; C141 1uF, 6.3V; C142 1nF, 10%; C154 1uF, 6.3V

GND

1.25V Analog

VDD12_TXBUF — G5

VDD12O_VCO_SXT — J5

VDD12_VCO_SXT — K6

VDD_CP_SXT — J3

VDD_TBB — P4

VDD12_TIA_RFE — AD6

VDD12_LNA_RFE — AG5

VDD_CP_SXR — AL19

VDD_DIV_SXR — AM20

VDD12_VCO_SXR — AN23

VDD12_RXBUF — AP26

VDD_AFE — AJ25

VDD_CP_CGEN — F20

VDD_DIV_CGEN — E19

VDD_TPAD_TRF — B16

VDD_TLOBUF_TRF — F8

VDDO_TLOBUF_TRF — D6

VCC1P25_LMS2 — R89 10R — R90 10R

FR37; FR38; FR39; FR40; FR41; FR42; FR43; FR44; FR45; FR46; FR47; FR48; FR49; FR50

All ferrites are 600R, 0.27A

C156 1uF, 6.3V; C157 1uF, 6.3V; C158 1uF, 6.3V; C159 1uF, 6.3V; C160 1uF, 6.3V; C161 1uF, 6.3V; C162 1uF, 6.3V; C163 1uF, 6.3V; C164 1uF, 6.3V; C165 1uF, 6.3V; C166 1uF, 6.3V; C155 1uF, 6.3V; C167 1uF, 6.3V; C168 1uF, 6.3V; C169 1uF, 6.3V

GND

1.25V-1.4V Analog

VDD_DIV_SXT — L5

VDDO_DIV_SXT — K2

VDD_MXLOBUF_RFE — AN17

FR51; FR52; FR53; FR54; FR55; FR56 — VCC1P4_LMS2

All ferrites are 600R, 0.27A

1.4V Analog

VDD14_RBB — AD4

VDD14_TIA_RFE — AF2

VDD14_LNA_RFE — AF6

VDD14_VCO_CGEN — C21

C171 1uF, 6.3V; C172 1uF, 6.3V; C173 1uF, 6.3V; C174 1uF, 6.3V; C175 1uF, 6.3V; C170 1uF, 6.3V

GND

LMS7002M

IC3E

LMS7002M Power Part 5/7

1.8V Digital

VDD18_DIG — D24 — R91 0R — VCC1P8_LMS2

C176 1uF, 6.3V

GND

1.8V-3.3V Digital

DIGPRVDD2 — AH30, W33, T32, H32

DIGPRPOC — W31

R92 0R; R93 0R; R94 0R; R95 0R; R96 0R — VDIO_LMS

C177 10uF, 6.3V

GND

C178 1nF, 10%; C179 1uF, 6.3V; C180 1nF, 10%; C181 1uF, 6.3V; C182 1nF, 10%; C183 1uF, 6.3V; C184 1nF, 10%; C185 1uF, 6.3V; C186 1nF, 10%; C187 1uF, 6.3V

1.8V Analog

VDD18_VCO_SXT — G3

VDD18_LDO_TX — N1

VDD18_TIA_RFE — AE3

VDD18_LDO_RX — AF4

VDD18_SXR — AM18

VDD18_VCO_SXR — AK22

VDD18_BIAS — E17

VDD18_TRF — D16

VDD18_VCO_CGEN — E21

FR57; FR58; FR59; FR60; FR61; FR62; FR63; FR64 — VCC1P8_LMS2

GND

C189 1uF, 6.3V; C190 1uF, 6.3V; C191 1uF, 6.3V; C192 1uF, 6.3V; C193 1uF, 6.3V; C194 1uF, 6.3V; C195 1uF, 6.3V; C188 1uF, 6.3V

1.8V-3.3V Analog

VDD18_TXBUF — H6

VDD18_RXBUF — AM26

FR65; FR66 — VCC1P8_LMS2 — R97 10R; R98 10R

C196 1uF, 6.3V; C197 1uF, 6.3V; C198 1uF, 6.3V; C199 1uF, 6.3V

GND

LMS7002M

IC3G

LMS7002M GND Part 7/7

Digital gnd		Analog gnd	
N3	DGND_SXT	GND_DIV_SXT	L3
AM22	DGND_SXR	GND_CP_SXT	K4
E25	GND_SPI_BUF	GND_RXBUF	AN25
C23	GND_DIG	GND_DIV_SXR	AK20
B18	DGND_CGEN	GND_CP_SXR	AJ19
J33	DIGPRGND1	GND_CP_CGEN	B20
AA31	DIGPRGND1	GND_TXBUF	F6
AG29	DIGPRGND1	GND_DIV_CGEN	D20
T30	DIGPRGND1,2	GND_VCO_SXR	AL23
W29	DIGPRGND1	GND_VCO_SXT	H2
G31	DIGPRGND2	GND_TLOBUF_TRF	C7
AF32	DIGPRGND2	Thermal pad EP	GND
Y30	DIGPRGND2		

GND — LMS7002M — GND

Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*LMS7002M power supply (LMS2)*		
Size:	A3	Revision:	v1.1
Date:	2024-06-11	Time: 10:27:14	Sheet 10 of 31
File:	12_LMS2_Power.SchDoc		

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

Lime microsystems

NF elements on sheet: R99

Number of NF elements on sheet: 1

LMS7002M power supply circuit (LMS3)

IC5F

LMS7002M Power Part 6/7

1.25V Digital

DIGPRVDD1 AE29
DIGPRVDD1 AA29
DIGPRVDD1 L33
DIGPRVDD1 R31
DVDD_SXR AL21
DVDD_SXT M4
VDD12_DIG C25
VDD_SPI_BUF F24
DVDD_CGEN A17

1.25V Analog

VDD12_TXBUF G5
VDD12O_VCO_SXT J5
VDD12_VCO_SXT K6
VDD_CP_SXT J3
VDD_TBB P4
VDD12_TIA_RFE AD6
VDD12_LNA_RFE AG5
VDD_CP_SXR AL19
VDD_DIV_SXR AM20
VDD12_VCO_SXR AN23
VDD12_RXBUF AP26
VDD_AFE AJ25
VDD_CP_CGEN F20
VDD_DIV_CGEN E19
VDD_TPAD_TRF B16
VDD_TLOBUF_TRF F8
VDDO_TLOBUF_TRF D6

1.25V-1.4V Analog

VDD_DIV_SXT L5
VDDO_DIV_SXT K2
VDD_MXLOBUF_RFE AN17

1.4V Analog

VDD14_RBB AD4
VDD14_TIA_RFE AF2
VDD14_LNA_RFE AF6
VDD14_VCO_CGEN C21

LMS7002M

Only one is fitted

VCC1P4_LMS3 — R99 NF / 0R NF — VCC1P25_LMS3

R100 0R

600R, 0.27A FR67
600R, 0.27A FR68
600R, 0.27A FR69

C202 1uF, 6.3V; C203 1uF, 6.3V; C204 1uF, 6.3V; C205 1uF, 6.3V; C206 1uF, 6.3V; C207 1uF, 6.3V; C208 1nF, 10%; C209 1uF, 6.3V; C210 1nF, 10%; C211 1uF, 6.3V; C212 1nF, 10%; C200 1uF, 6.3V; C201 1nF, 10%

C213 1uF, 6.3V — GND

R101 10R

FR70 FR71 FR72 FR73 FR74 FR75 FR76 FR77 FR78 FR79 FR80 FR81 FR82 FR83 — All ferrites are 600R, 0.27A

R102 10R

C215 1uF, 6.3V; C216 1uF, 6.3V; C217 1uF, 6.3V; C218 1uF, 6.3V; C219 1uF, 6.3V; C220 1uF, 6.3V; C221 1uF, 6.3V; C222 1uF, 6.3V; C223 1uF, 6.3V; C224 1uF, 6.3V; C225 1uF, 6.3V; C214 1uF, 6.3V; C226 1uF, 6.3V; C227 1uF, 6.3V; C228 1uF, 6.3V

GND

FR84 FR85 FR86 FR87 FR88 FR89 — All ferrites are 600R, 0.27A

VCC1P4_LMS3

C230 1uF, 6.3V; C231 1uF, 6.3V; C232 1uF, 6.3V; C233 1uF, 6.3V; C234 1uF, 6.3V; C229 1uF, 6.3V

GND

IC5E

LMS7002M Power Part 5/7

1.8V Digital

VDD18_DIG D24

R103 0R — VCC1P8_LMS3

C235 1uF, 6.3V — GND

1.8V-3.3V Digital

DIGPRVDD2 AH30
DIGPRVDD2 W33
DIGPRVDD2 T32
DIGPRVDD2 H32
DIGPRVDD2 W31
DIGPRPOC

R104 0R; R105 0R; R106 0R; R107 0R; R108 0R — VDIO_LMS

C236 10uF, 6.3V — GND

C237 1nF, 10%; C238 1uF, 6.3V; C239 1nF, 10%; C240 1uF, 6.3V; C241 1nF, 10%; C242 1uF, 6.3V; C243 1nF, 10%; C244 1uF, 6.3V; C245 1nF, 10%; C246 1uF, 6.3V

1.8V Analog

VDD18_VCO_SXT G3
VDD18_LDO_TX N1
VDD18_TIA_RFE AE3
VDD18_LDO_RX AF4
VDD18_SXR AM18
VDD18_VCO_SXR AK22
VDD18_BIAS E17
VDD18_TRF D16
VDD18_VCO_CGEN E21

FR90 FR91 FR92 FR93 FR94 FR95 FR96 FR97 — VCC1P8_LMS3

C248 1uF, 6.3V; C249 1uF, 6.3V; C250 1uF, 6.3V; C251 1uF, 6.3V; C252 1uF, 6.3V; C253 1uF, 6.3V; C254 1uF, 6.3V; C247 1uF, 6.3V

GND

1.8V-3.3V Analog

VDD18_TXBUF H6
VDD18_RXBUF AM26

FR98 FR99 — R109 10R; R110 10R — VCC1P8_LMS3

C255 1uF, 6.3V; C256 1uF, 6.3V; C257 1uF, 6.3V; C258 1uF, 6.3V

GND

LMS7002M

IC5G

LMS7002M GND Part 7/7

Digital gnd		Analog gnd	
N3	DGND_SXT	GND_DIV_SXT	L3
AM22	DGND_SXR	GND_CP_SXT	K4
E25	GND_SPI_BUF	GND_RXBUF	AN25
C23	GND_DIG	GND_DIV_SXR	AK20
B18	DGND_CGEN	GND_CP_SXR	AJ19
J33	DIGPRGND1	GND_CP_CGEN	B20
AA31	DIGPRGND1	GND_TXBUF	F6
AG29	DIGPRGND1	GND_DIV_CGEN	D20
T30	DIGPRGND1,2	GND_VCO_SXR	AL23
W29	DIGPRGND1	GND_VCO_SXT	H2
G31	DIGPRGND2	GND_TLOBUF_TRF	C7
AF32	DIGPRGND2	Thermal pad	
Y30	DIGPRGND2	EP	GND

GND GND

Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*LMS7002M power supply (LMS3)*		
Size:	A3	Revision:	v1.1
Date:	2024-06-11	Time: 10:27:17	Sheet 10 of 31
File:	13_LMS3_Power.SchDoc		

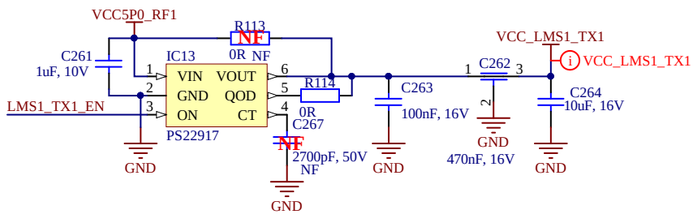
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

Lime microsystems

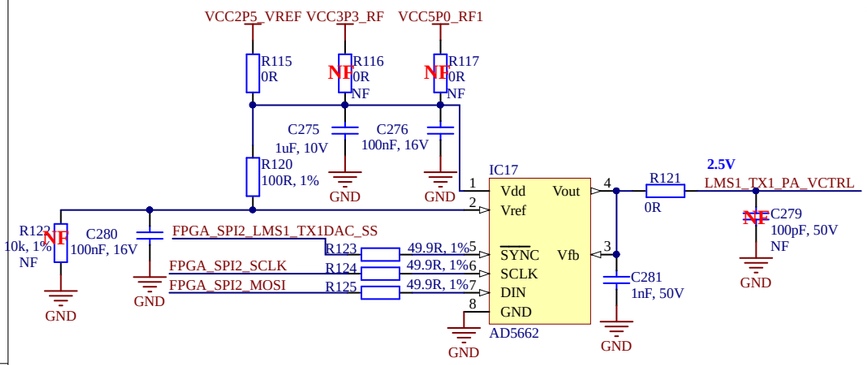
NF elements on sheet: R113, C267, R116, R117, R122, C279, ESD8, R128, C290, ESD9, R131, R132, R137, C302
Number of NF elements on sheet: 14

LMS1 RF PA

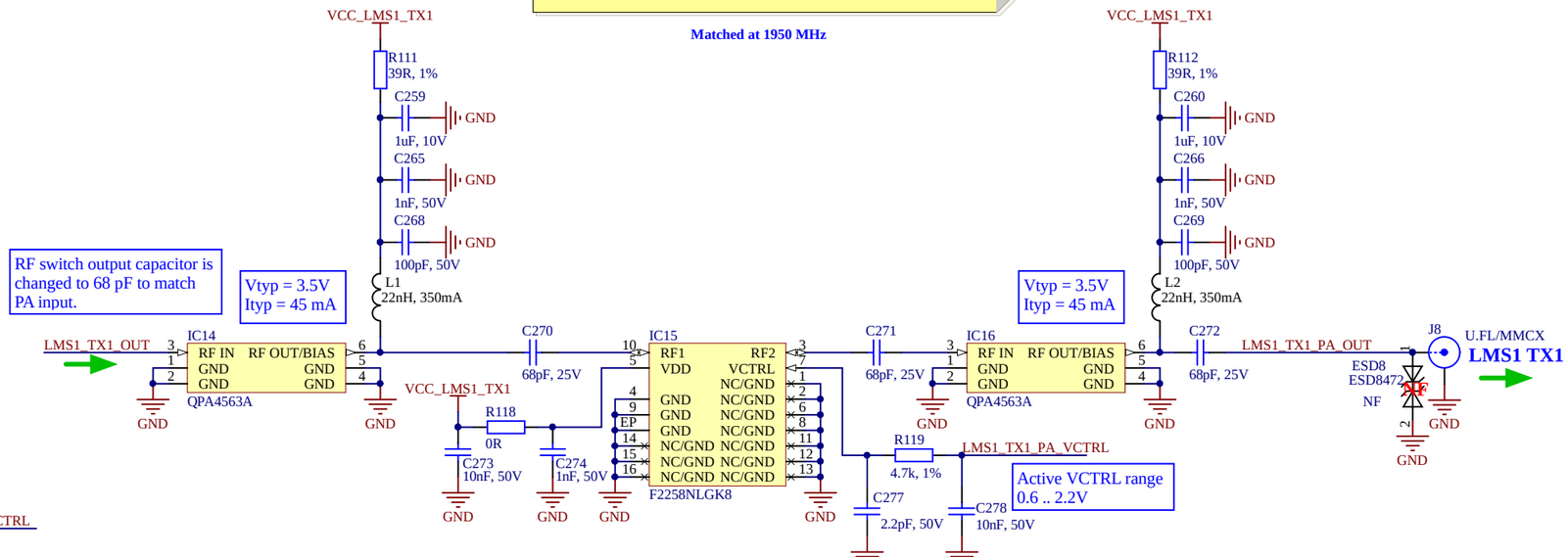
PA power control



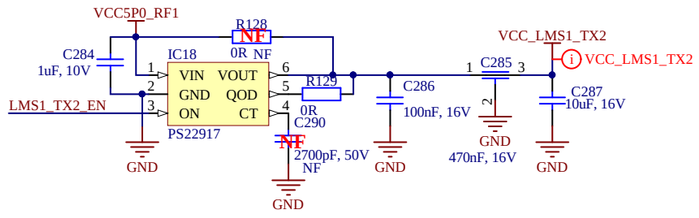
Voltage variable attenuator (VVA) DAC



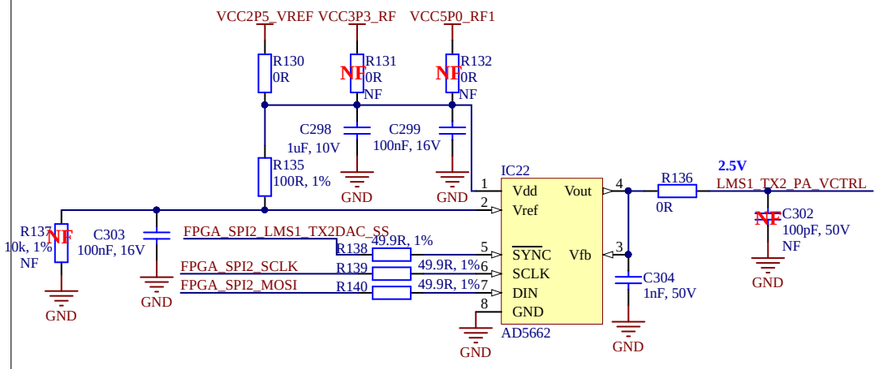
LMS1 TX1 PAs and Attenuator



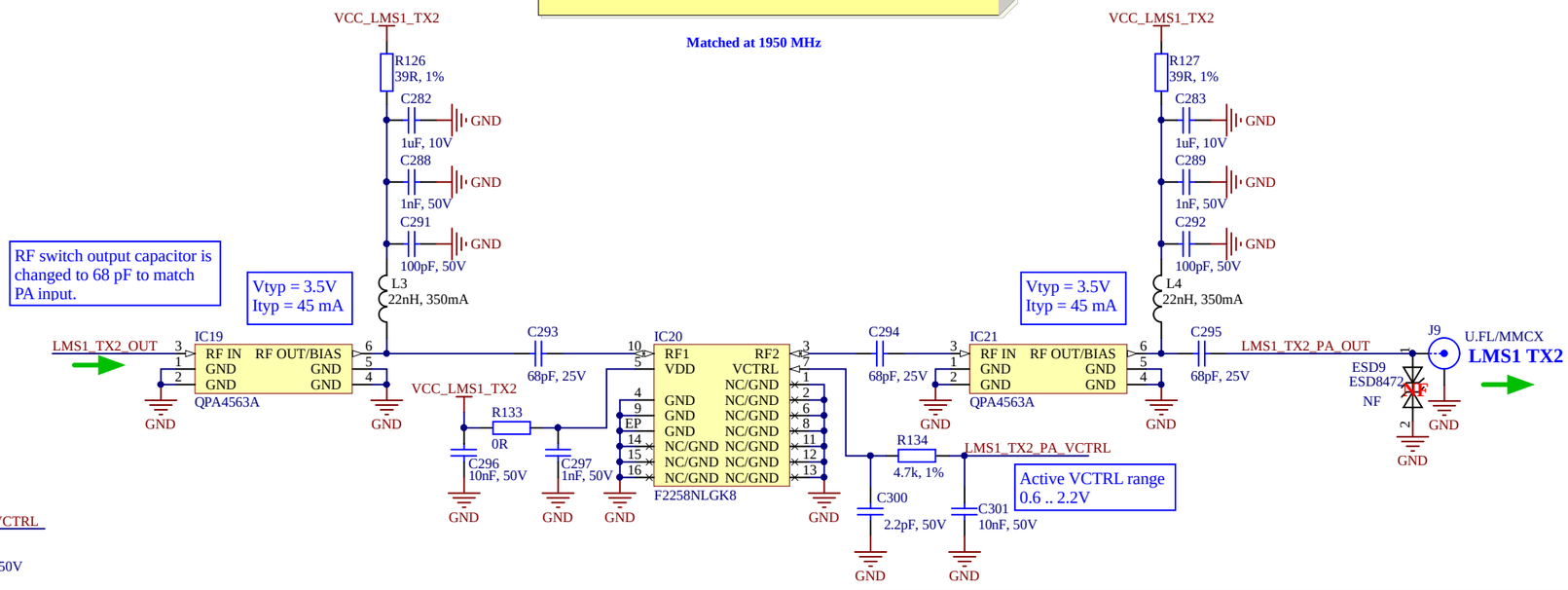
PA power control



Voltage variable attenuator (VVA) DAC



LMS1 TX2 PAs and Attenuator

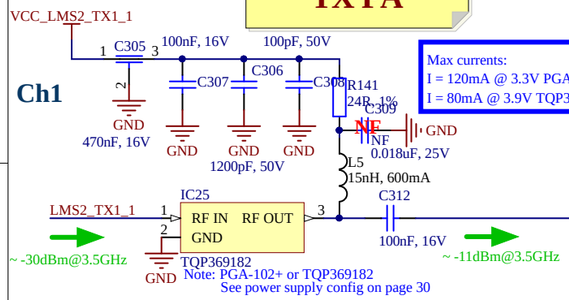


Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*LMS1 RF PA*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:27:21	Sheet 14 of 31	
File: 14_LMS1_RF_PA.SchDoc			

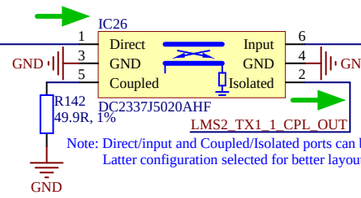
NF elements on sheet: C309, ESD10, R144, C319, ESD11
Number of NF elements on sheet: 5

LMS2 RF1 Misc

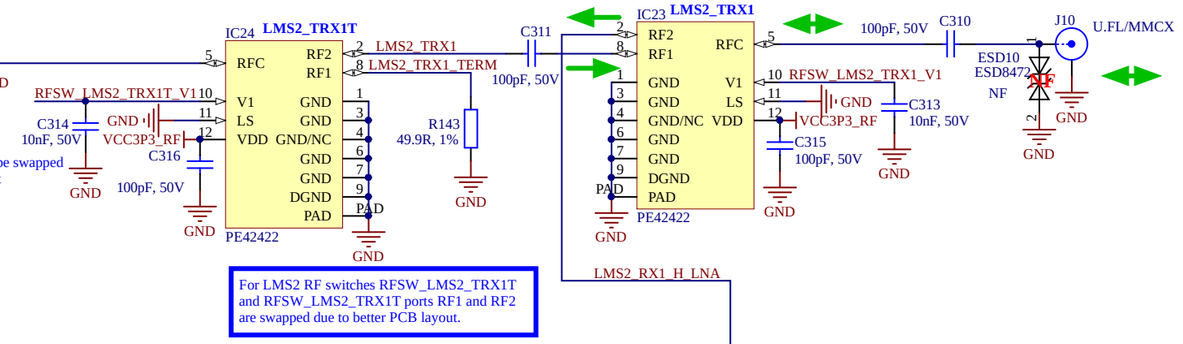
TX PA



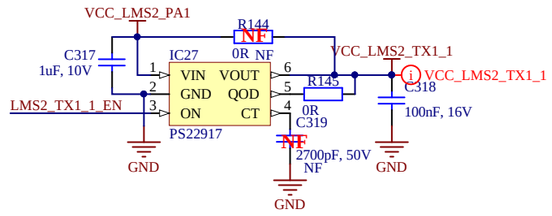
TX coupler



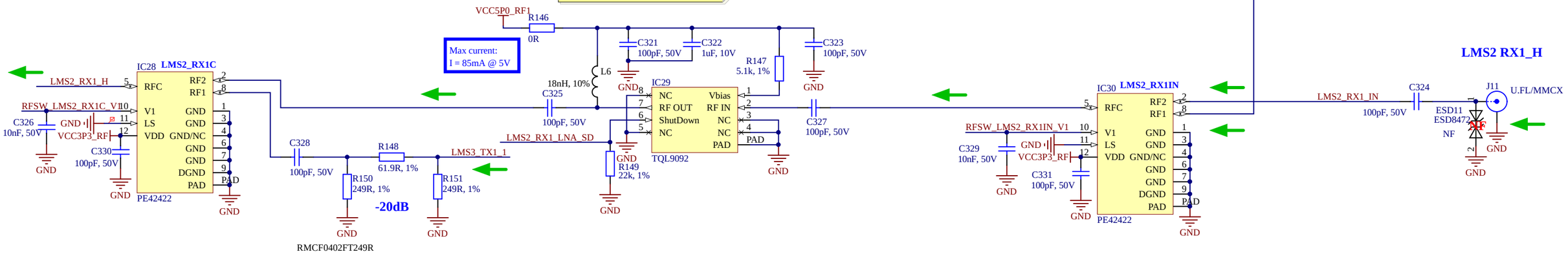
RF Switches



PA power control



RX LNA



Project name:	*LimeSDR-X3_1v1.PrjPcb*
Title:	*LMS2 RF1 Misc*
Size: A3	Revision: v1.1
Date: 2024-06-11	Time: 10:27:25 Sheet 15 of 31
File:	15_LMS2_RF1_Misc.SchDoc

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Surrey
United Kingdom

Lime microsystems

NF elements on sheet: C336, ESD12, R155, C346, ESD13
Number of NF elements on sheet: 5

LMS2 RF2 Misc

TX PA

Ch2

VCC_LMS2_TX2_1
C332 100nF, 16V
C333 100pF, 50V
C334
C335
R152 24R, 1%
C336 NF 0.018uF, 25V
L7 15nH, 600mA
C337 100nF, 16V
IC33 RF IN RF OUT GND
TQP369182
LMS2_TX2_1
~ -30dBm@3.5GHz
~ -11dBm@3.5GHz
LMS2_TX2_1_PA
Note: PGA-102+ or TQP369182
See power supply config on page 30

Max currents:
I = 120mA @ 3.3V PGA-102 +
I = 80mA @ 3.9V TQP369182

TX coupler

IC34 Direct Input GND GND Coupled Isolated
DC2337J5020AHF
R154 49.9R, 1%
LMS2_TX2_1_CPL_OUT
Note: Direct/input and Coupled/Isolated ports can be swapped
Latter configuration selected for better layout

RF Switches

IC31 LMS2_TRX2T
RFSW_LMS2_TRX2T_V1
C340 10nF, 50V
VCC3P3_RF
C342 100pF, 50V
LMS2_TRX2_TERM
LMS2_TRX2
R153 49.9R, 1%
C339 100pF, 50V
PE42422

For LMS2 RF switches RFSW_LMS2_TRX1T and RFSW_LMS2_TRX1T ports RF1 and RF2 are swapped due to better PCB layout.

IC32 LMS2_TRX2
RFSW_LMS2_TRX2_V1
C341 10nF, 50V
C343 100pF, 50V
C338 100pF, 50V
J12 U.FL/MMCX
ESD12 ESD8472 NF
PE42422

LMS2 TRX2

LMS2_RX2_H_LNA
C347 100pF, 50V

PA power control

VCC_LMS2_PA2
R155 NF 0R
C344 1uF, 10V
IC35 VIN VOUT GND QOD ON CT
PS22917
LMS2_TX2_1_EN
R156 0R
C345 100nF, 16V
C346 NF 2700pF, 50V
VCC_LMS2_TX2_1

RX LNA

VCC5P0_RF2
R157 0R
C348 100pF, 50V
C349 1uF, 10V
C350 100pF, 50V
L8 18nH, 10%
C352 100pF, 50V
IC37 NC RF OUT ShutDown NC Vbias RF IN NC NC PAD
TQL9092
R158 5.1k, 1%
C354 100pF, 50V
LMS2_RX2_LNA_SD
R160 22k, 1%

Max current:
I = 85mA @ 5V

IC36 LMS2_RX2C
LMS2_RX2_H
RFSW_LMS2_RX2C_V1
C353 10nF, 50V
C357 100pF, 50V
PE42422
C355 100pF, 50V
R159 61.9R, 1%
R161 249R, 1%
R162 249R, 1%
-20dB
LMS3_TX2_1

IC38 LMS2_RX2IN
RFSW_LMS2_RX2IN_V1
C356 10nF, 50V
C358 100pF, 50V
PE42422
LMS2_RX2_IN
C351 100pF, 50V
J13 U.FL/MMCX
ESD13 ESD8472 NF

LMS2 RX2_H

Project name:	LimeSDR-X3_1v1.PrjPcb		
Title:	LMS2 RF2 Misc	Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom	Lime microsystems
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:27:28	Sheet 16 of 31	
File: 16_LMS2_RF2_Misc.SchDoc			

NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA Banks 12, 13, 14, 15

Board SPI interfaces:

FPGA_SPI0 (VDIO_LMS (default 2.5V)): LMS1, LMS2, LMS3
FPGA_SPI1 (2.5V): BB_ADC1, BB_ADC2, BB_ADC3, BB_ADC4, CDCM1, CDCM2
FPGA_SPI2 (2.5V): XO_DAC, XO_20_DAC, LMS1_TX1DAC, LMS1_TX2DAC, ADF

IC39A

BANK 12 — 2.5V

IO_0_12	AB22	FPGA_SPI1_CDCM_SS
IO_L1P_T0_12	AE25	LMS3_BB_ADC1_DA2_P
IO_L1N_T0_12	AE26	LMS3_BB_ADC1_DA2_N
IO_L2P_T0_12	AC22	LMS3_BB_ADC1_DA1_P
IO_L2N_T0_12	AC23	LMS3_BB_ADC1_DA1_N
IO_L3P_T0_DQS_12	AF24	LMS3_BB_ADC1_DA3_P
IO_L3N_T0_DQS_12	AF25	LMS3_BB_ADC1_DA3_N
IO_L4P_T0_12	AD25	LMS3_BB_ADC1_DA0_P
IO_L4N_T0_12	AD26	LMS3_BB_ADC1_DA0_N
IO_L5P_T0_12	AE23	LMS3_BB_ADC1_DB6_P
IO_L5N_T0_12	AF23	LMS3_BB_ADC1_DB6_N
IO_L6P_T0_12	AD23	LMS2_RX1_LNA_SD
IO_L6N_T0_VREF_12	AD24	LMS2_RX2_LNA_SD
IO_L7P_T1_12	AD21	LMS3_BB_ADC1_DB4_P
IO_L7N_T1_12	AE21	LMS3_BB_ADC1_DB4_N
IO_L8P_T1_12	AF19	LMS3_BB_ADC1_DA4_P
IO_L8N_T1_12	AF20	LMS3_BB_ADC1_DA4_N
IO_L9P_T1_DQS_12	AE22	LMS3_BB_ADC1_DB5_P
IO_L9N_T1_DQS_12	AF22	LMS3_BB_ADC1_DB5_N
IO_L10P_T1_12	AD20	LMS3_BB_ADC1_DB3_P
IO_L10N_T1_12	AE20	LMS3_BB_ADC1_DB3_N
IO_L11P_T1_SRCC_12	AB21	WR_PTP_CLK1_125_P
IO_L11N_T1_SRCC_12	AC21	WR_PTP_CLK1_125_N
IO_L12P_T1_MRCC_12	AA20	LMS3_BB_ADC1_CLKOUT_P
IO_L12N_T1_MRCC_12	AB20	LMS3_BB_ADC1_CLKOUT_N
IO_L13P_T2_MRCC_12	AA19	WR_PTP_CLK0_20
IO_L13N_T2_MRCC_12	AB19	
IO_L14P_T2_SRCC_12	AC19	
IO_L14N_T2_SRCC_12	AD19	
IO_L15P_T2_DQS_12	AC18	CDCM_RESET_N
IO_L15N_T2_DQS_12	AD18	PD_LMS3_BB_ADC2_DRV
IO_L16P_T2_12	AE18	LMS3_BB_ADC1_DA5_P
IO_L16N_T2_12	AF18	LMS3_BB_ADC1_DA5_N
IO_L17P_T2_12	Y18	LMS3_BB_ADC1_DB2_P
IO_L17N_T2_12	AA18	LMS3_BB_ADC1_DB2_N
IO_L18P_T2_12	AE17	LMS3_BB_ADC1_DA6_P
IO_L18N_T2_12	AF17	LMS3_BB_ADC1_DA6_N
IO_L19P_T3_12	AA17	FPGA_SPI2_LMS1_TX1DAC_SS
IO_L19N_T3_VREF_12	AB17	FPGA_SPI2_LMS1_TX2DAC_SS
IO_L20P_T3_12	AC17	LMS3_BB_ADC1_DB0_P
IO_L20N_T3_12	AD17	LMS3_BB_ADC1_DB0_N
IO_L21P_T3_DQS_12	Y16	LMS3_BB_ADC1_DB1_P
IO_L21N_T3_DQS_12	Y17	LMS3_BB_ADC1_DB1_N
IO_L22P_T3_12	AB16	CDCM_STATUS0
IO_L22N_T3_12	AC16	CDCM_STATUS1
IO_L23P_T3_12	Y15	
IO_L23N_T3_12	AA15	CDCM_SYNCN
IO_L24P_T3_12	W14	PD_LMS2_BB_ADC1_DRV
IO_L24N_T3_12	W15	PD_LMS2_BB_ADC2_DRV
IO_25_12	W16	PD_LMS3_BB_ADC1_DRV

XC7A200T-2FBG676C

IC39B

BANK 13 — 2.5V

IO_0_13	U24	LM75_OS
IO_L1P_T0_13	U25	LMS3_BB_ADC2_DA5_P
IO_L1N_T0_13	U26	LMS3_BB_ADC2_DA5_N
IO_L2P_T0_13	V26	LMS3_BB_ADC2_DA6_P
IO_L2N_T0_13	W26	LMS3_BB_ADC2_DA6_N
IO_L3P_T0_DQS_13	AB26	LMS3_BB_ADC2_DB0_P
IO_L3N_T0_DQS_13	AC26	LMS3_BB_ADC2_DB0_N
IO_L4P_T0_13	W25	LMS3_BB_ADC2_DB6_P
IO_L4N_T0_13	Y26	LMS3_BB_ADC2_DB6_N
IO_L5P_T0_13	Y25	LMS3_BB_ADC2_DB5_P
IO_L5N_T0_13	AA25	LMS3_BB_ADC2_DB5_N
IO_L6P_T0_13	V24	HW_VER2
IO_L6N_T0_VREF_13	W24	BOM_VER2
IO_L7P_T1_13	AA24	LMS3_BB_ADC2_DB1_P
IO_L7N_T1_13	AB25	LMS3_BB_ADC2_DB1_N
IO_L8P_T1_13	AA22	LMS3_BB_ADC2_DA4_P
IO_L8N_T1_13	AA23	LMS3_BB_ADC2_DA4_N
IO_L9P_T1_DQS_13	AB24	LMS3_BB_ADC2_DB3_P
IO_L9N_T1_DQS_13	AC24	LMS3_BB_ADC2_DB3_N
IO_L10P_T1_13	V23	LMS3_BB_ADC2_DA2_P
IO_L10N_T1_13	W23	LMS3_BB_ADC2_DA2_N
IO_L11P_T1_SRCC_13	Y22	HW_VER1
IO_L11N_T1_SRCC_13	Y23	BOM_VER1
IO_L12P_T1_MRCC_13	U22	LMS3_BB_ADC2_CLKOUT_P
IO_L12N_T1_MRCC_13	V22	LMS3_BB_ADC2_CLKOUT_N
IO_L13P_T2_MRCC_13	U21	CLK100_FPGA_P
IO_L13N_T2_MRCC_13	V21	CLK100_FPGA_N
IO_L14P_T2_SRCC_13	W21	LMK1_CLK1
IO_L14N_T2_SRCC_13	Y21	
IO_L15P_T2_DQS_13	T20	FPGA_LED1_G
IO_L15N_T2_DQS_13	U20	
IO_L16P_T2_13	W20	LMS3_BB_ADC2_DB2_P
IO_L16N_T2_13	Y20	LMS3_BB_ADC2_DB2_N
IO_L17P_T2_13	T19	LMS3_BB_ADC2_DA3_P
IO_L17N_T2_13	U19	LMS3_BB_ADC2_DA3_N
IO_L18P_T2_13	V19	LMS3_BB_ADC2_DB4_P
IO_L18N_T2_13	W19	LMS3_BB_ADC2_DB4_N
IO_L19P_T3_13	V18	
IO_L19N_T3_VREF_13	W18	HW_VER0
IO_L20P_T3_13	T14	LMS3_BB_ADC2_DA0_P
IO_L20N_T3_13	T15	LMS3_BB_ADC2_DA0_N
IO_L21P_T3_DQS_13	T17	LMS3_BB_ADC2_DA1_P
IO_L21N_T3_DQS_13	T18	LMS3_BB_ADC2_DA1_N
IO_L22P_T3_13	U15	FPGA_LED3_G
IO_L22N_T3_13	U16	FPGA_LED2_G
IO_L23P_T3_13	U14	FPGA_LED4_G
IO_L23N_T3_13	V14	FPGA_LED4_R
IO_L24P_T3_13	V16	FPGA_LED3_R
IO_L24N_T3_13	V17	FPGA_LED2_R
IO_25_13	U17	FPGA_LED1_R

GND, MRCC, MRCC

XC7A200T-2FBG676C

IC39C

BANK 14 — 3.3V

IO_0_14	M19	ADF_MUXOUT
IO_L1P_T0_D00_MOSI_14	R14	FPGA_CFG_D00 DO NOT MOVE!
IO_L1N_T0_D01_DIN_14	R15	FPGA_CFG_D01 DO NOT MOVE!
IO_L2P_T0_D02_14	P14	FPGA_CFG_D02 DO NOT MOVE!
IO_L2N_T0_D03_14	N14	FPGA_CFG_D03 DO NOT MOVE!
IO_L3P_T0_DQS_PUDC_B_14	P15	PMOD_A_PIN9
IO_L3N_T0_DQS_EMCCLK_14	P16	PMOD_A_PIN10
IO_L4P_T0_D04_14	N16	FPGA_I2C_SCL
IO_L4N_T0_D05_14	N17	FPGA_I2C_SDA
IO_L5P_T0_D06_14	R16	WR_PTP_SFP_TX_FAULT
IO_L5N_T0_D07_14	R17	WR_PTP_SFP_TX_DISABLE
IO_L6P_T0_FCS_B_14	P18	FPGA_CFG_CS DO NOT MOVE!
IO_L6N_T0_D08_VREF_14	N18	WR_PTP_SFP_MOD_DEF2
IO_L7P_T1_D09_14	K25	WR_PTP_SFP_MOD_DEF1
IO_L7N_T1_D10_14	K26	WR_PTP_SFP_MOD_DEF0
IO_L8P_T1_D11_14	M20	WR_PTP_SFP_RATE_SEL
IO_L8N_T1_D12_14	L20	GNSS_TPULSE
IO_L9P_T1_DQS_14	L24	GNSS_UART_TX
IO_L9N_T1_DQS_D13_14	L25	GNSS_UART_RX
IO_L10P_T1_D14_14	M24	PMOD_B_PIN2
IO_L10N_T1_D15_14	M25	EXT_SYNC_OUT
IO_L11P_T1_SRCC_14	L22	WR_PTP_CLK1_20
IO_L11N_T1_SRCC_14	L23	PMOD_B_PIN1
IO_L12P_T1_MRCC_14	M21	LMK2_CLK MRCC P
IO_L12N_T1_MRCC_14	M22	PMOD_B_PIN3
IO_L13P_T2_MRCC_14	N21	EXT_PPS_IN MRCC P
IO_L13N_T2_MRCC_14	N22	PMOD_B_PIN4
IO_L14P_T2_SRCC_14	P20	EXT_SYNC_IN SRCC P
IO_L14N_T2_SRCC_14	P21	PMOD_A_PIN3
IO_L15P_T2_DQS_RDWR_B_14	N23	PMOD_B_PIN10
IO_L15N_T2_DQS_DOUT_CSO_B_14	N24	LMS2_BB_DAC2_PD
IO_L16P_T2_CSI_B_14	P19	PMOD_A_PIN4
IO_L16N_T2_A15_D31_14	N19	PMOD_B_PIN7
IO_L17P_T2_A14_D30_14	P23	PMOD_A_PIN2
IO_L17N_T2_A13_D29_14	P24	PMOD_B_PIN8
IO_L18P_T2_A12_D28_14	R20	PMOD_A_PIN7
IO_L18N_T2_A11_D27_14	R21	PMOD_A_PIN8
IO_L19P_T3_A10_D26_14	R25	PMOD_A_PIN1
IO_L19N_T3_A09_D25_VREF_14	P25	PMOD_B_PIN9
IO_L20P_T3_A08_D24_14	N26	XO_VC_FPGA
IO_L20N_T3_A07_D23_14	M26	LMS2_BB_DAC1_PD
IO_L21P_T3_DQS_14	T24	WR_PTP_SFP_LOS
IO_L21N_T3_DQS_A06_D22_14	T25	PTP_CLK1_OUT
IO_L22P_T3_A05_D21_14	R26	PTP_CLK2_OUT
IO_L22N_T3_A04_D20_14	P26	PTP_CLK3_OUT
IO_L23P_T3_A03_D19_14	T22	EXT_PPS_OUT
IO_L23N_T3_A02_D18_14	R22	PCIE_SMCLK
IO_L24P_T3_A01_D17_14	T23	PCIE_SMDAT
IO_L24N_T3_A00_D16_14	R23	PCIE_PERSTn
IO_25_14	R18	PCIE_WAKEn

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IC39D

BANK 15 — 2.5V

IO_0_15	K18	RFSW_LMS2_TRX2T_V1
IO_L1P_T0_AD0P_15	K15	LMK1_SEL0
IO_L1N_T0_AD0N_15	J16	RFSW_LMS2_RX2C_V1
IO_L2P_T0_AD8P_15	J14	RFSW_LMS2_TRX1_V1
IO_L2N_T0_AD8N_15	J15	RFSW_LMS2_TRX1T_V1
IO_L3P_T0_DQS_AD1P_15	K16	LMS2_BB_ADC2_DA1_P
IO_L3N_T0_DQS_AD1N_15	K17	LMS2_BB_ADC2_DA1_N
IO_L4P_T0_15	M14	FPGA_SPI1_MOSI
IO_L4N_T0_15	L14	FPGA_SPI1_MISO
IO_L5P_T0_AD9P_15	M15	RFSW_LMS2_RX2IN_V1
IO_L5N_T0_AD9N_15	L15	LMS2_TX1_1_EN
IO_L6P_T0_15	M16	FPGA_SPI1_SCLK
IO_L6N_T0_VREF_15	M17	
IO_L7P_T1_AD2P_15	J19	LMS2_BB_ADC2_DA3_P
IO_L7N_T1_AD2N_15	H19	LMS2_BB_ADC2_DA3_N
IO_L8P_T1_AD10P_15	L17	LMS2_BB_ADC2_DB6_P
IO_L8N_T1_AD10N_15	L18	LMS2_BB_ADC2_DB6_N
IO_L9P_T1_DQS_AD3P_15	K20	LMS2_BB_ADC2_DB4_P
IO_L9N_T1_DQS_AD3N_15	J20	LMS2_BB_ADC2_DB4_N
IO_L10P_T1_AD11P_15	J18	LMS2_BB_ADC2_DB3_P
IO_L10N_T1_AD11N_15	H18	LMS2_BB_ADC2_DB3_N
IO_L11P_T1_SRCC_15	G20	
IO_L11N_T1_SRCC_15	G21	
IO_L12P_T1_MRCC_15	K21	LMS2_BB_ADC2_CLKOUT_P MRCC
IO_L12N_T1_MRCC_15	J21	LMS2_BB_ADC2_CLKOUT_N
IO_L13P_T2_MRCC_15	H21	LMK2_SEL0
IO_L13N_T2_MRCC_15	H22	
IO_L14P_T2_SRCC_15	J23	LMS1_TX1_EN
IO_L14N_T2_SRCC_15	H23	LMS1_TX2_EN
IO_L15P_T2_DQS_15	G22	LMS2_BB_ADC2_DB5_P
IO_L15N_T2_DQS_ADV_B_15	F22	LMS2_BB_ADC2_DB5_N
IO_L16P_T2_A28_15	J24	LMS2_BB_ADC2_DB2_P
IO_L16N_T2_A27_15	H24	LMS2_BB_ADC2_DB2_N
IO_L17P_T2_A26_15	F23	LMS2_BB_ADC2_DA2_P
IO_L17N_T2_A25_15	E23	LMS2_BB_ADC2_DA2_N
IO_L18P_T2_A24_15	K22	FPGA_SPI1_LMS2_BB_ADC2_SS
IO_L18N_T2_A23_15	K23	FPGA_LMS2_BB_ADC2_RESET
IO_L19P_T3_A22_15	G24	LMS2_BB_ADC2_DA4_P
IO_L19N_T3_A21_VREF_15	F24	LMS2_BB_ADC2_DA4_N
IO_L20P_T3_A20_15	E25	LMS2_BB_ADC2_DA0_P
IO_L20N_T3_A19_15	D25	LMS2_BB_ADC2_DA0_N
IO_L21P_T3_DQS_15	E26	LMS2_BB_ADC2_DA5_P
IO_L21N_T3_DQS_A18_15	D26	LMS2_BB_ADC2_DA5_N
IO_L22P_T3_A17_15	H26	LMS2_BB_ADC2_DB0_P
IO_L22N_T3_A16_15	G26	LMS2_BB_ADC2_DB0_N
IO_L23P_T3_FOE_B_15	G25	LMS2_BB_ADC2_DA6_P
IO_L23N_T3_FWE_B_15	F25	LMS2_BB_ADC2_DA6_N
IO_L24P_T3_RS1_15	J25	LMS2_BB_ADC2_DB1_P
IO_L24N_T3_RS0_15	J26	LMS2_BB_ADC2_DB1_N
IO_25_15	L19	HW_VER3

GND, MRCC

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Project name:	LimeSDR-X3_1v1.PrjPcb
Title:	FPGA Banks 12, 13, 14, 15
Size: A3	Revision: v1.1
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File:	17_FPGA_B12_B13_B14_B15.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

Lime microsystems

NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA Banks 16, 33, 34, 35

IC39E

BANK 16

IO_0_16	H17	RFSW_LMS2_TRX2_V1
IO_L1P_T0_16	H14	LMS2_TX2_1_EN
IO_L1N_T0_16	H15	RFSW_LMS2_RX1C_V1
IO_L2P_T0_16	G17	LMS2_BB_ADC1_DA2_P
IO_L2N_T0_16	F17	LMS2_BB_ADC1_DA2_N
IO_L3P_T0_DQS_16	F18	LMS2_BB_ADC1_DB2_P
IO_L3N_T0_DQS_16	F19	LMS2_BB_ADC1_DB2_N
IO_L4P_T0_16	G15	RFSW_LMS1_RX2_V1
IO_L4N_T0_16	F15	RFSW_LMS1_RX1_V1
IO_L5P_T0_16	G19	RFSW_LMS1_TX1_V1
IO_L5N_T0_16	F20	FPGA_SPI1_LMS3_BB_ADC1_SS
IO_L6P_T0_16	H16	RFSW_LMS1_TX2_V1
IO_L6N_T0_VREF_16	G16	
IO_L7P_T1_16	J17	LMS2_BB_ADC1_DA4_P
IO_L7N_T1_16	J17	LMS2_BB_ADC1_DA4_N
IO_L8P_T1_16	E16	LMS2_BB_ADC1_DA5_P
IO_L8N_T1_16	D16	LMS2_BB_ADC1_DA5_N
IO_L9P_T1_DQS_16	A17	LMS2_BB_ADC1_DA1_P
IO_L9N_T1_DQS_16	A18	LMS2_BB_ADC1_DA1_N
IO_L10P_T1_16	B19	LMS2_BB_ADC1_DA3_P
IO_L10N_T1_16	A19	LMS2_BB_ADC1_DA3_N
IO_L11P_T1_SRCC_16	E17	RFSW1_LMS3_RX1_V1
IO_L11N_T1_SRCC_16	E18	RFSW1_LMS3_RX2_V1
IO_L12P_T1_MRCC_16	D18	LMS2_BB_ADC1_CLKOUT_P **MRCC**
IO_L12N_T1_MRCC_16	C18	LMS2_BB_ADC1_CLKOUT_N
IO_L13P_T2_MRCC_16	D19	RFSW_LMS2_RX1IN_V1
IO_L13N_T2_MRCC_16	C19	
IO_L14P_T2_SRCC_16	E20	FPGA_SPI1_LMS3_BB_ADC2_SS
IO_L14N_T2_SRCC_16	D20	FPGA_LMS3_BB_ADC2_RESET
IO_L15P_T2_DQS_16	B20	LMS2_BB_ADC1_DA0_P
IO_L15N_T2_DQS_16	A20	LMS2_BB_ADC1_DA0_N
IO_L16P_T2_16	C21	LMS2_BB_ADC1_DB3_P
IO_L16N_T2_16	B21	LMS2_BB_ADC1_DB3_N
IO_L17P_T2_16	B22	LMS2_BB_ADC1_DA6_P
IO_L17N_T2_16	A22	LMS2_BB_ADC1_DA6_N
IO_L18P_T2_16	E21	LMS2_BB_ADC1_DB4_P
IO_L18N_T2_16	D21	LMS2_BB_ADC1_DB4_N
IO_L19P_T3_16	C22	FPGA_SPI1_LMS2_BB_ADC1_SS
IO_L19N_T3_VREF_16	C23	
IO_L20P_T3_16	B25	LMS2_BB_ADC1_DB6_P
IO_L20N_T3_16	A25	LMS2_BB_ADC1_DB6_N
IO_L21P_T3_DQS_16	A23	LMS2_BB_ADC1_DB0_P
IO_L21N_T3_DQS_16	A24	LMS2_BB_ADC1_DB0_N
IO_L22P_T3_16	C26	LMS2_BB_ADC1_DB1_P
IO_L22N_T3_16	B26	LMS2_BB_ADC1_DB1_N
IO_L23P_T3_16	C24	LMS2_BB_ADC1_DB5_P
IO_L23N_T3_16	B24	LMS2_BB_ADC1_DB5_N
IO_L24P_T3_16	D23	FPGA_LMS2_BB_ADC1_RESET
IO_L24N_T3_16	D24	FPGA_LMS3_BB_ADC1_RESET
IO_25_16	E22	FPGA_SPI1_MISO_BB_ADC

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IC39F

BANK 33

IO_0_33	V4	LMS1_DIQ1_D0
IO_L1P_T0_33	V1	LMS1_RESET
IO_L1N_T0_33	W1	LMS1_DIQ2_D2
IO_L2P_T0_33	W5	LMS1_DIQ1_D1
IO_L2N_T0_33	W4	LMS1_DIQ1_D4
IO_L3P_T0_DQS_33	V3	LMS1_DIQ2_D1
IO_L3N_T0_DQS_33	V2	LMS1_DIQ2_D0
IO_L4P_T0_33	V6	LMS1_TXEN
IO_L4N_T0_33	W6	LMS3_RESET
IO_L5P_T0_33	W3	LMS1_DIQ2_D9
IO_L5N_T0_33	Y3	LMS1_DIQ2_D5
IO_L6P_T0_33	U7	LMS3_RXEN
IO_L6N_T0_VREF_33	V7	LMS2_RESET
IO_L7P_T1_33	AB1	LMS1_DIQ2_D6
IO_L7N_T1_33	AC1	LMS1_DIQ2_D8
IO_L8P_T1_33	Y2	LMS1_DIQ2_D7
IO_L8N_T1_33	Y1	LMS1_DIQ2_D3
IO_L9P_T1_DQS_33	AD1	LMS1_DIQ2_D11
IO_L9N_T1_DQS_33	AE1	LMS1_DIQ2_D10
IO_L10P_T1_33	AE2	LMS1_EN_IQSEL2
IO_L10N_T1_33	AF2	LMS1_DIQ2_D4
IO_L11P_T1_SRCC_33	AB2	LMS1_FCLK1 **SRCC_P**
IO_L11N_T1_SRCC_33	AC2	FPGA_SPI0_LMS3_SS
IO_L12P_T1_MRCC_33	AA3	LMS1_MCLK1 **MRCC_P**
IO_L12N_T1_MRCC_33	AA2	FPGA_SPI0_LMS2_SS
IO_L13P_T2_MRCC_33	AA4	LMS1_MCLK2 **MRCC_P**
IO_L13N_T2_MRCC_33	AB4	FPGA_SPI0_LMS2_MISO
IO_L14P_T2_SRCC_33	AC3	LMS1_FCLK2 **SRCC_P**
IO_L14N_T2_SRCC_33	AD3	FPGA_SPI0_LMS3_MISO
IO_L15P_T2_DQS_33	AD5	LMS1_DIQ1_D9
IO_L15N_T2_DQS_33	AE5	LMS1_DIQ1_D8
IO_L16P_T2_33	AE3	LMS1_RXEN
IO_L16N_T2_33	AF3	LMS1_TXNRX2
IO_L17P_T2_33	AF5	LMS1_DIQ1_D11
IO_L17N_T2_33	AF4	LMS1_TXNRX1
IO_L18P_T2_33	AC4	LMS1_DIQ1_D10
IO_L18N_T2_33	AD4	LMS1_EN_IQSEL1
IO_L19P_T3_33	Y7	LMS3_TXEN
IO_L19N_T3_VREF_33	AA7	LMS1_DIQ1_D5
IO_L20P_T3_33	Y6	FPGA_SPI0_SCLK
IO_L20N_T3_33	Y5	FPGA_SPI0_MOSI
IO_L21P_T3_DQS_33	V8	FPGA_SPI0_LMS1_MISO
IO_L21N_T3_DQS_33	W8	FPGA_SPI0_LMS1_SS
IO_L22P_T3_33	AA5	LMS1_DIQ1_D6
IO_L22N_T3_33	AB5	LMS1_DIQ1_D7
IO_L23P_T3_33	Y8	LMS2_RXEN
IO_L23N_T3_33	AA8	LMS2_TXEN
IO_L24P_T3_33	AB6	LMS1_DIQ1_D3
IO_L24N_T3_33	AC6	LMS1_DIQ1_D2
IO_25_33	V9	

VDIO_LMS

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IC39G

BANK 34

IO_0_34	N8	BOM_VER3
IO_L1P_T0_34	K3	LMS2_BB_DAC1_B13_P
IO_L1N_T0_34	J3	LMS2_BB_DAC1_B13_N
IO_L2P_T0_34	M7	LMS2_BB_DAC1_B2_P
IO_L2N_T0_34	L7	LMS2_BB_DAC1_B2_N
IO_L3P_T0_DQS_34	M4	LMS2_BB_DAC1_B12_P
IO_L3N_T0_DQS_34	L4	LMS2_BB_DAC1_B12_N
IO_L4P_T0_34	L5	FPGA_SW1
IO_L4N_T0_34	K5	FPGA_SW0
IO_L5P_T0_34	N7	FPGA_SPI2_XO_20_DAC_SS
IO_L5N_T0_34	N6	FPGA_SPI2_XO_25_DAC_SS
IO_L6P_T0_34	M6	LMS2_BB_DAC1_SELIQ_P
IO_L6N_T0_VREF_34	M5	LMS2_BB_DAC1_SELIQ_N
IO_L7P_T1_34	K1	LMS2_BB_DAC1_B14_P
IO_L7N_T1_34	J1	LMS2_BB_DAC1_B14_N
IO_L8P_T1_34	J3	
IO_L8N_T1_34	K2	BOM_VER0
IO_L9P_T1_DQS_34	N1	LMS2_BB_DAC1_B0_P
IO_L9N_T1_DQS_34	M1	LMS2_BB_DAC1_B0_N
IO_L10P_T1_34	H2	LMS2_BB_DAC1_B15_P
IO_L10N_T1_34	H1	LMS2_BB_DAC1_B15_N
IO_L11P_T1_SRCC_34	M2	FPGA_LMS2_BB_DAC1_CLK_P
IO_L11N_T1_SRCC_34	L2	FPGA_LMS2_BB_DAC1_CLK_N
IO_L12P_T1_MRCC_34	N3	**MRCC** CDCM_LMS2_BB_DAC1_REFC_P
IO_L12N_T1_MRCC_34	N2	CDCM_LMS2_BB_DAC1_REFC_N
IO_L13P_T2_MRCC_34	R3	LMK1_CLK2 **MRCC/SRCC P**
IO_L13N_T2_MRCC_34	P3	
IO_L14P_T2_SRCC_34	P4	LMK2_CLKIN1
IO_L14N_T2_SRCC_34	N4	
IO_L15P_T2_DQS_34	R1	LMS2_BB_DAC1_B10_P
IO_L15N_T2_DQS_34	P1	LMS2_BB_DAC1_B10_N
IO_L16P_T2_34	T4	LMS2_BB_DAC1_B11_P
IO_L16N_T2_34	T3	LMS2_BB_DAC1_B11_N
IO_L17P_T2_34	T2	LMS2_BB_DAC1_B9_P
IO_L17N_T2_34	R2	LMS2_BB_DAC1_B9_N
IO_L18P_T2_34	U2	LMS2_BB_DAC1_B8_P
IO_L18N_T2_34	U1	LMS2_BB_DAC1_B8_N
IO_L19P_T3_34	P6	LMS2_BB_DAC1_B6_P
IO_L19N_T3_VREF_34	P5	LMS2_BB_DAC1_B6_N
IO_L20P_T3_34	T5	LMS2_BB_DAC1_B7_P
IO_L20N_T3_34	R5	LMS2_BB_DAC1_B7_N
IO_L21P_T3_DQS_34	U6	LMS2_BB_DAC1_B5_P
IO_L21N_T3_DQS_34	U5	LMS2_BB_DAC1_B5_N
IO_L22P_T3_34	R8	LMS2_BB_DAC1_B4_P
IO_L22N_T3_34	P8	LMS2_BB_DAC1_B4_N
IO_L23P_T3_34	R7	LMS2_BB_DAC1_B1_P
IO_L23N_T3_34	R6	LMS2_BB_DAC1_B1_N
IO_L24P_T3_34	T8	LMS2_BB_DAC1_B3_P
IO_L24N_T3_34	T7	LMS2_BB_DAC1_B3_N
IO_25_34	U4	FAN_CTRL

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IC39H

BANK 35

IO_0_35	I8	
IO_L1P_T0_AD4P_35	E6	LMS2_BB_DAC2_B0_P
IO_L1N_T0_AD4N_35	D6	LMS2_BB_DAC2_B0_N
IO_L2P_T0_AD12P_35	H8	LMS2_BB_DAC2_B15_P
IO_L2N_T0_AD12N_35	G8	LMS2_BB_DAC2_B15_N
IO_L3P_T0_DQS_AD5P_35	H7	LMS2_BB_DAC2_B1_P
IO_L3N_T0_DQS_AD5N_35	G7	LMS2_BB_DAC2_B1_N
IO_L4P_T0_35	F8	LMS2_BB_DAC2_B13_P
IO_L4N_T0_35	F7	LMS2_BB_DAC2_B13_N
IO_L5P_T0_AD13P_35	H6	LMS2_BB_DAC2_B12_P
IO_L5N_T0_AD13N_35	G6	LMS2_BB_DAC2_B12_N
IO_L6P_T0_35	H9	LMS2_BB_DAC2_B14_P
IO_L6N_T0_VREF_35	G9	LMS2_BB_DAC2_B14_N
IO_L7P_T1_AD6P_35	J6	FPGA_SPI2_XO_DAC_SS
IO_L7N_T1_AD6N_35	J5	FPGA_SPI2_ADF_SS
IO_L8P_T1_AD14P_35	L8	LMS2_BB_DAC2_SELIQ_P
IO_L8N_T1_AD14N_35	K8	LMS2_BB_DAC2_SELIQ_N
IO_L9P_T1_DQS_AD7P_35	J4	LMS2_BB_DAC2_B4_P
IO_L9N_T1_DQS_AD7N_35	H4	LMS2_BB_DAC2_B4_N
IO_L10P_T1_AD15P_35	K7	LMS2_BB_DAC2_B3_P
IO_L10N_T1_AD15N_35	K6	LMS2_BB_DAC2_B3_N
IO_L11P_T1_SRCC_35	G4	WR_PTP_CLK2_125_P
IO_L11N_T1_SRCC_35	F4	WR_PTP_CLK2_125_N
IO_L12P_T1_MRCC_35	G5	**MRCC** CDCM_LMS2_BB_DAC2_REFC_P
IO_L12N_T1_MRCC_35	F5	CDCM_LMS2_BB_DAC2_REFC_N
IO_L13P_T2_MRCC_35	E5	FPGA_LMS2_BB_DAC2_CLK_P
IO_L13N_T2_MRCC_35	D5	FPGA_LMS2_BB_DAC2_CLK_N
IO_L14P_T2_SRCC_35	D4	WR_PTP_CLK3_125_P
IO_L14N_T2_SRCC_35	C4	WR_PTP_CLK3_125_N
IO_L15P_T2_DQS_35	B5	LMS2_BB_DAC2_B11_P
IO_L15N_T2_DQS_35	A5	LMS2_BB_DAC2_B11_N
IO_L16P_T2_35	B4	LMS2_BB_DAC2_B9_P
IO_L16N_T2_35	A4	LMS2_BB_DAC2_B9_N
IO_L17P_T2_35	D3	LMS2_BB_DAC2_B8_P
IO_L17N_T2_35	C3	LMS2_BB_DAC2_B8_N
IO_L18P_T2_35	F3	LMS2_BB_DAC2_B2_P
IO_L18N_T2_35	E3	LMS2_BB_DAC2_B2_N
IO_L19P_T3_35	C2	FPGA_SPI2_SCLK
IO_L19N_T3_VREF_35	B2	FPGA_SPI2_MOSI
IO_L20P_T3_35	A3	LMS2_BB_DAC2_B10_P
IO_L20N_T3_35	A2	LMS2_BB_DAC2_B10_N
IO_L21P_T3_DQS_35	C1	LMS2_BB_DAC2_B7_P
IO_L21N_T3_DQS_35	B1	LMS2_BB_DAC2_B7_N
IO_L22P_T3_35	F2	LMS2_BB_DAC2_B5_P
IO_L22N_T3_35	E2	LMS2_BB_DAC2_B5_N
IO_L23P_T3_35	E1	LMS2_BB_DAC2_B6_P
IO_L23N_T3_35	D1	LMS2_BB_DAC2_B6_N
IO_L24P_T3_35	G2	FPGA_SW3
IO_L24N_T3_35	G1	FPGA_SW2
IO_25_35	H3	

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Project name:	***LimeSDR-X3_1v1.PrjPcb***		
Title:	***FPGA Banks 16, 33, 34, 35***		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
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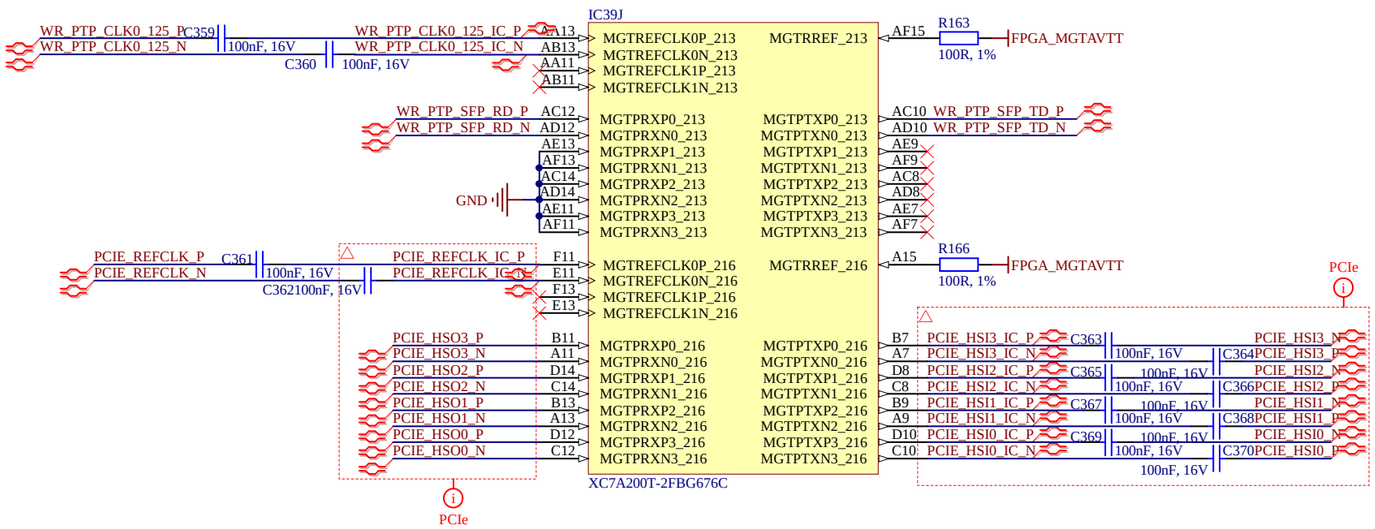
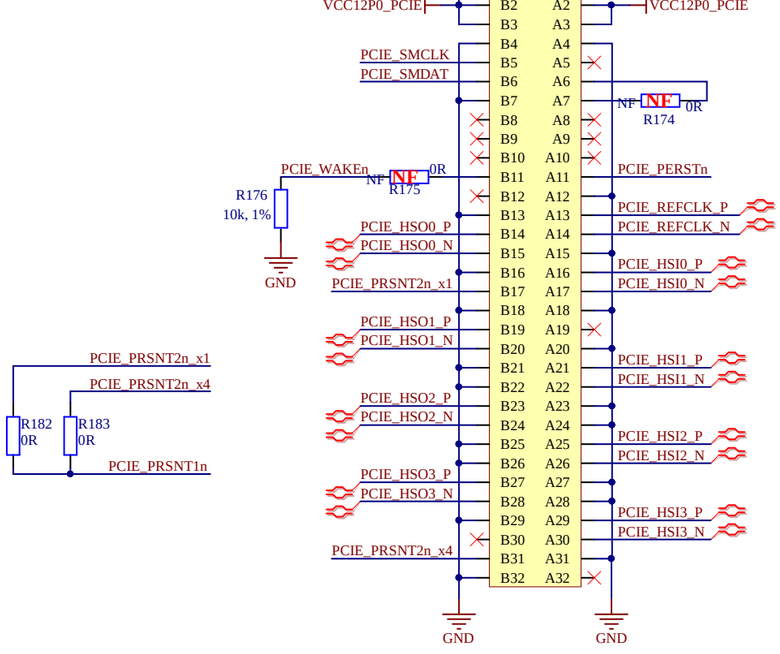
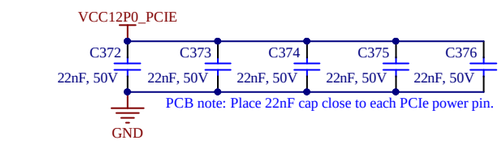
NF elements on sheet: R169, R170, R171, R174, R175, IC40, R186, R188
Number of NF elements on sheet: 8

FPGA misc (PCIe, config)

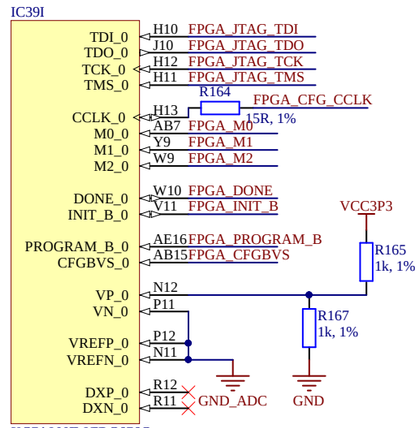
PCI Express x4

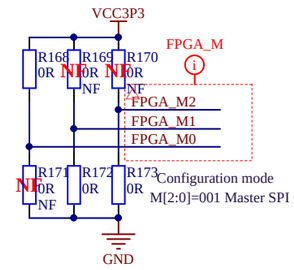


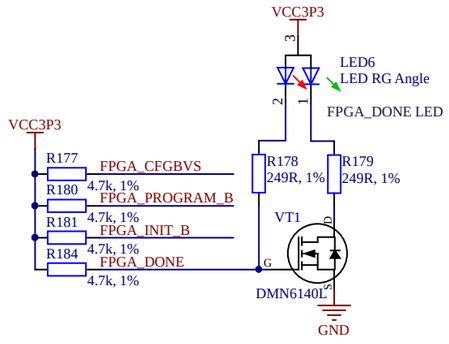




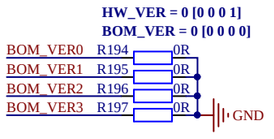
FPGA Configuration



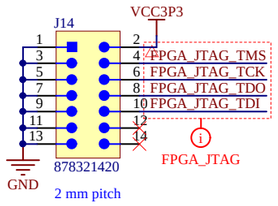




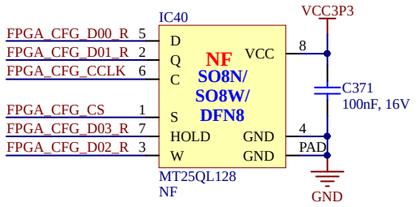
HW_VER, BOM_VER

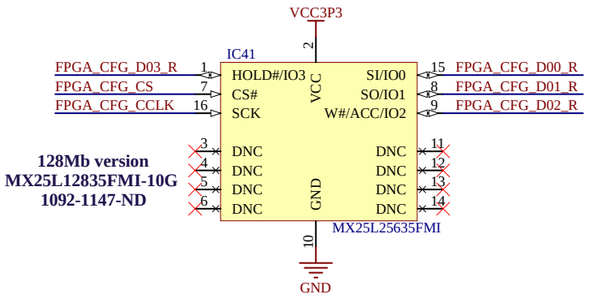


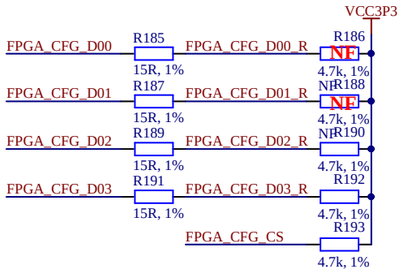
FPGA JTAG



FPGA Configuration Flash



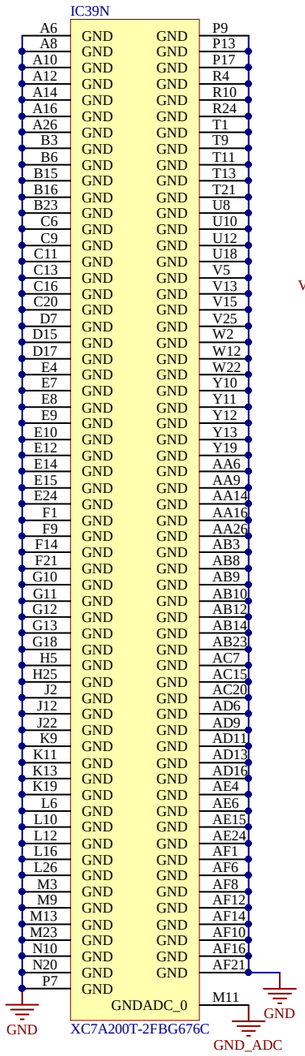


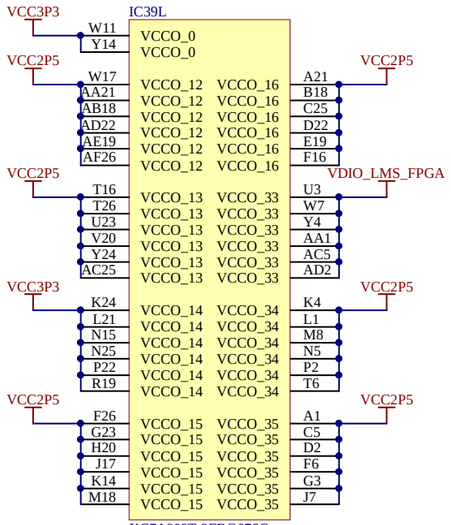


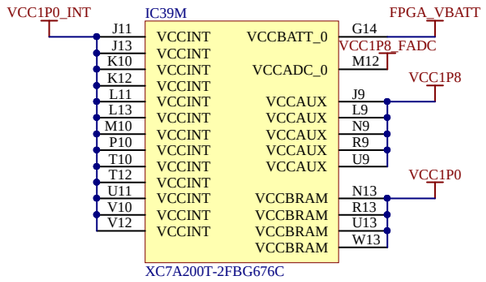
Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*FPGA misc (PCIe, config)*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:27:37	Sheet 19 of 31	
File: 19_FPGA_misc.SchDoc			

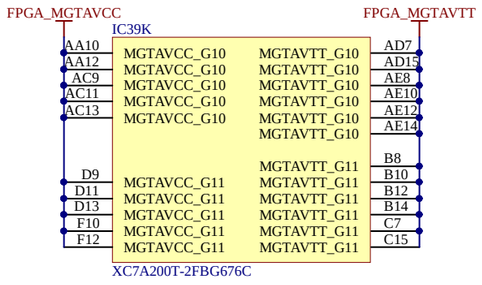
NF elements on sheet: BATTH1, BATT1, R199
Number of NF elements on sheet: 3

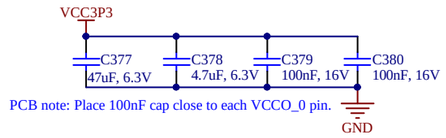
FPGA power

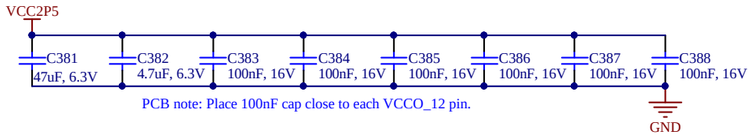


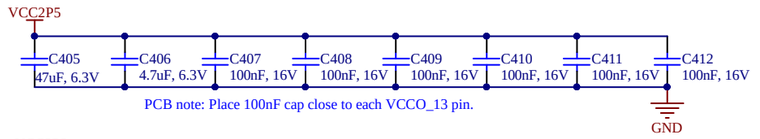


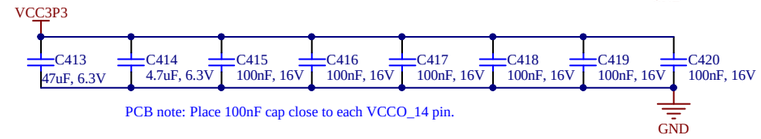


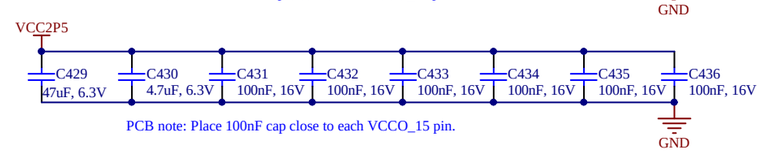


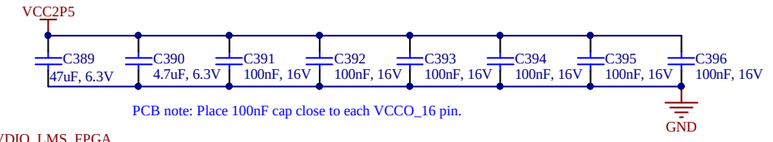


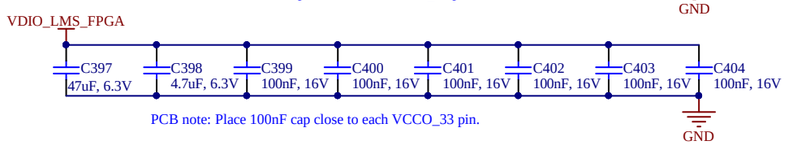


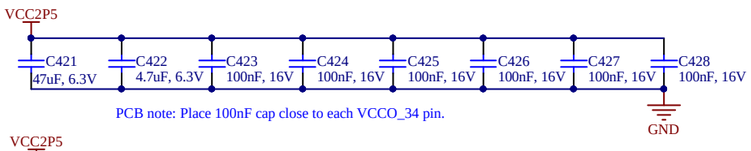


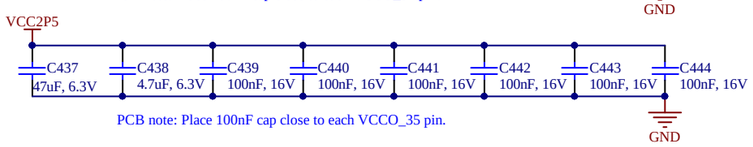


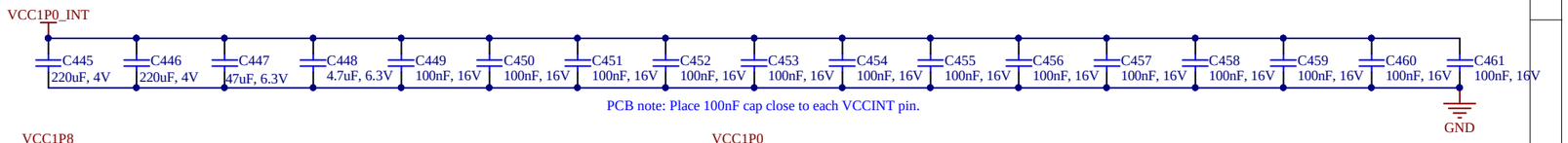


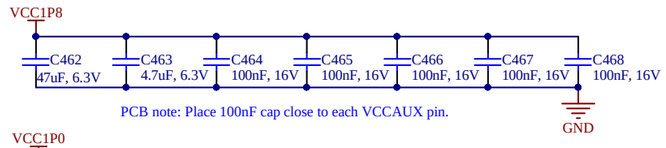


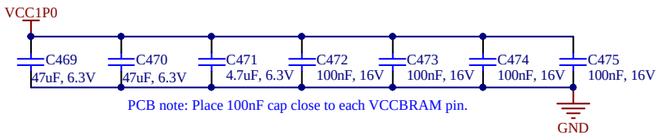


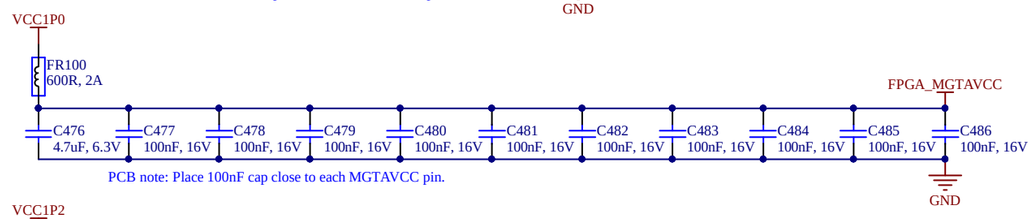


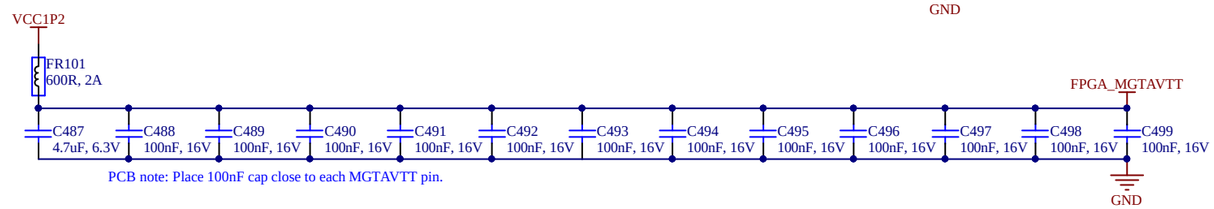


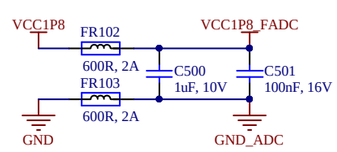


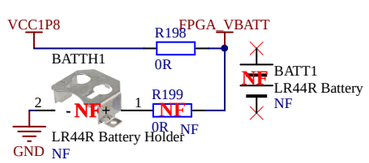










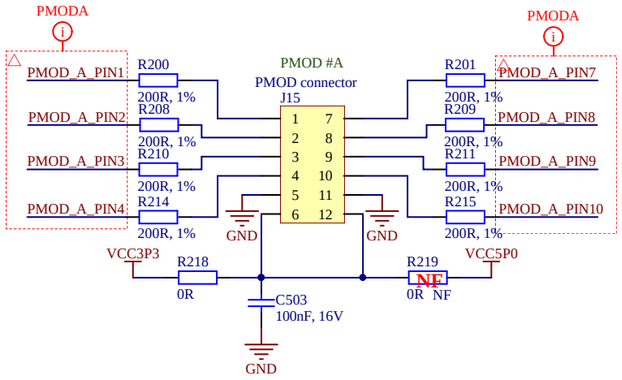


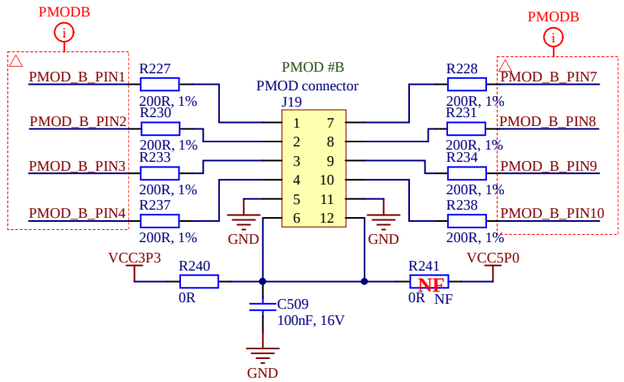
Project name:	***LimeSDR-X3_1v1.PrjPcb***	
Title:	***FPGA power***	*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1	
Date: 2024-06-11	Time: 10:27:40	Sheet 20 of 31
File: 20_FPGA_Power.SchDoc		

NF elements on sheet: R219, R223, R225, R232, R235, C502, IC45, R241, R242, ESD14, J20, R245, R248, R249, R252, R250
Number of NF elements on sheet: 16

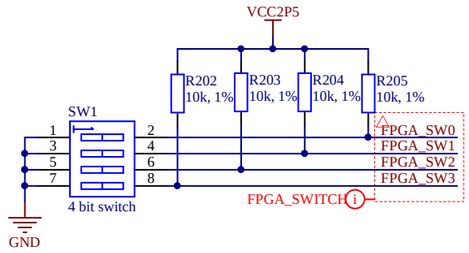
Peripherals

PMOD 12-pin connectors

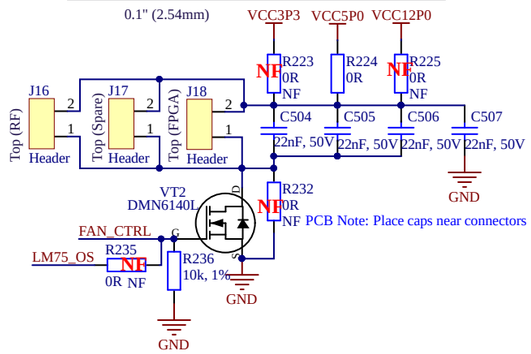




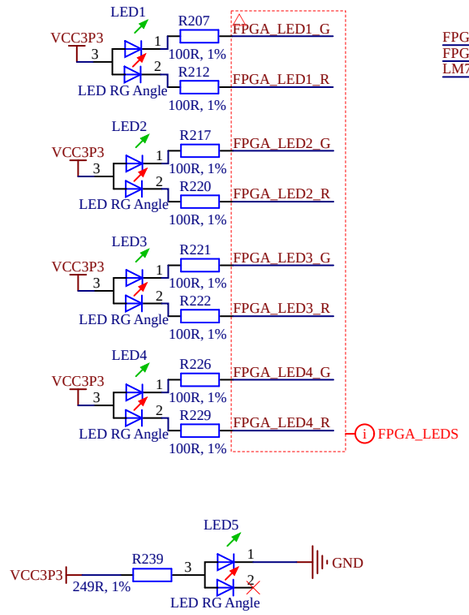
FPGA_SW



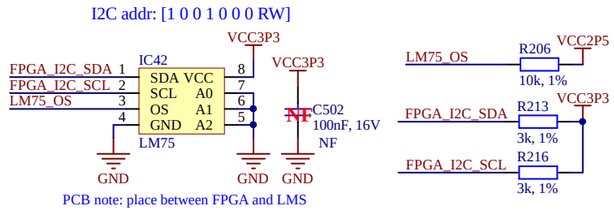
FAN control



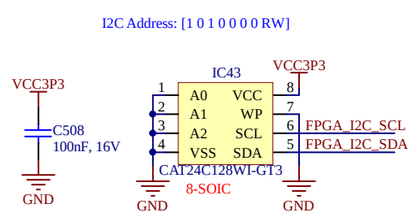
FPGA LEDs



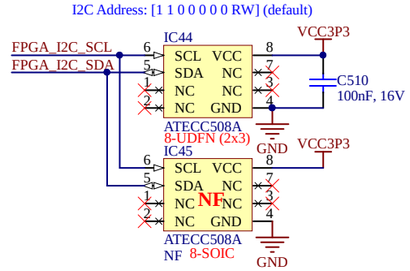
I2C Temperature sensor



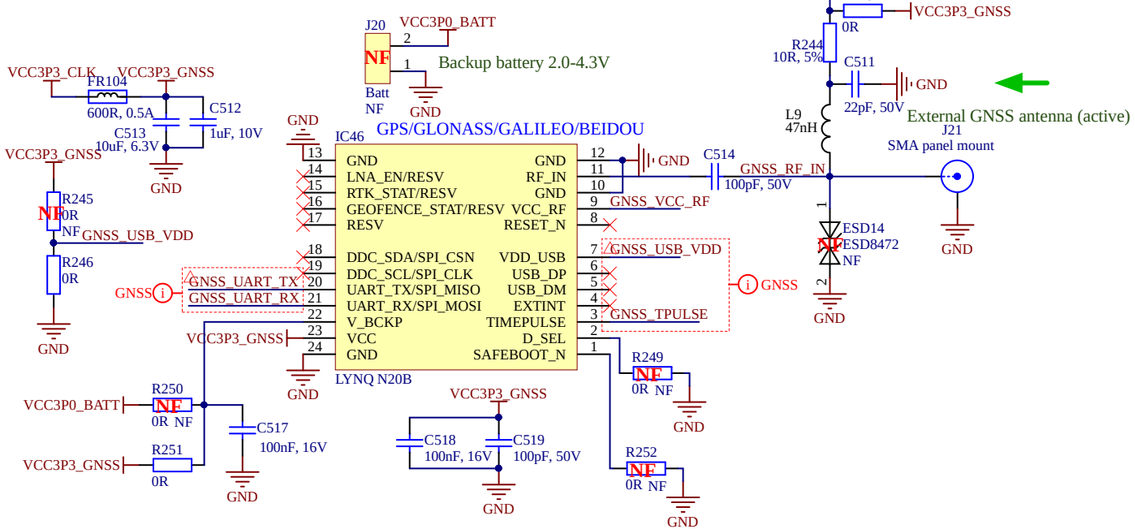
I2C EEPROM



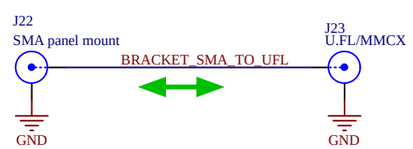
I2C secure key storage



GNSS receiver



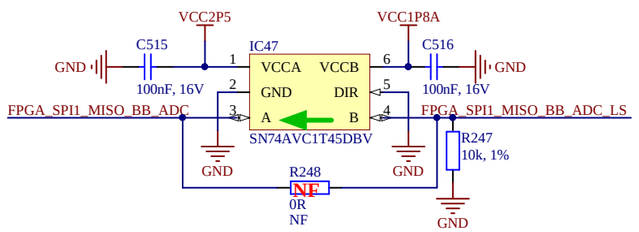
External SMA to internal U.FL



Can be connected internal U.FL connector via pigtail

SPI1 MISO BB ADCs level converter

One converter for all ADCs MISO lines



Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*Peripherals*		
Size:	A3	Revision:	v1.1
Date:	2024-06-11	Time: 10:27:44	Sheet 21 of 31
File:	21_Peripherals.SchDoc		

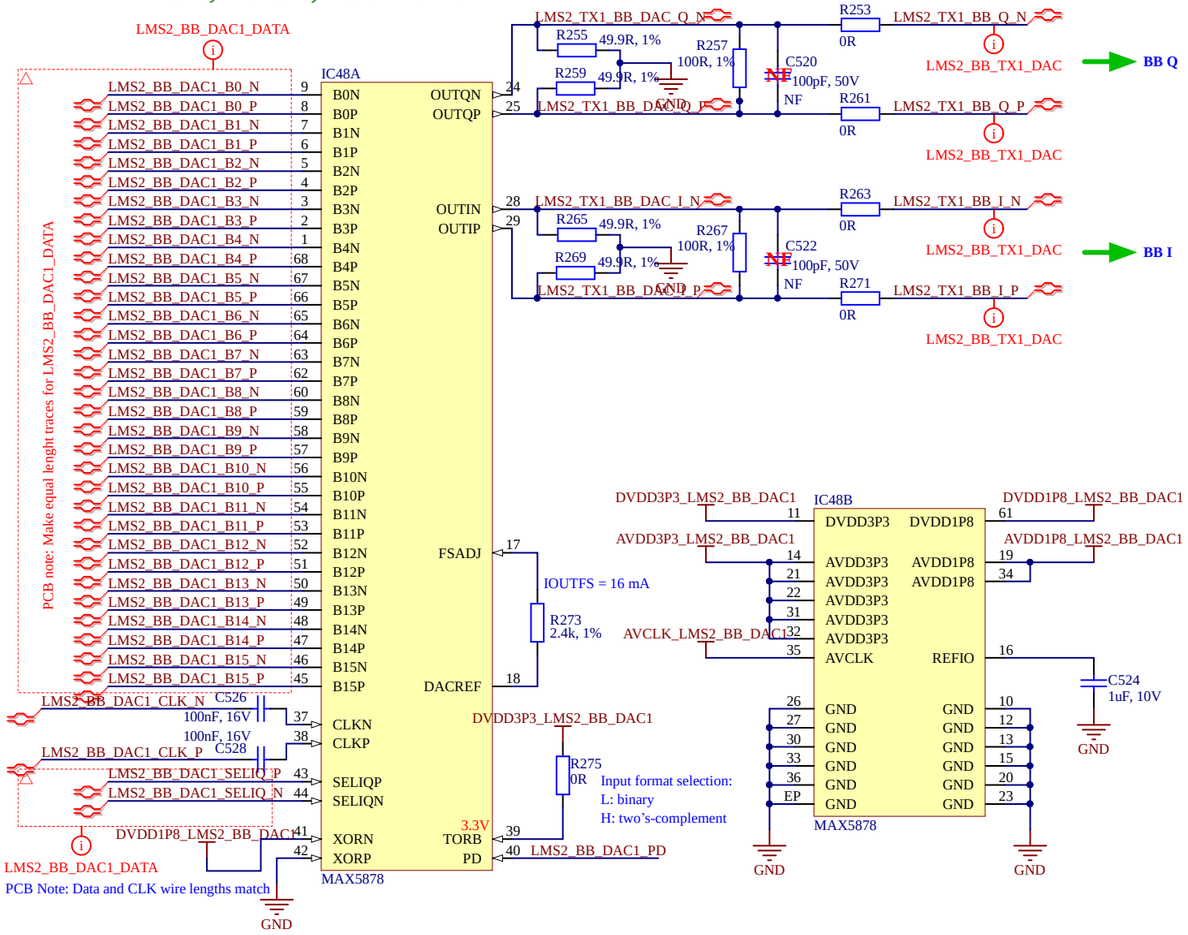
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surray
United Kingdom

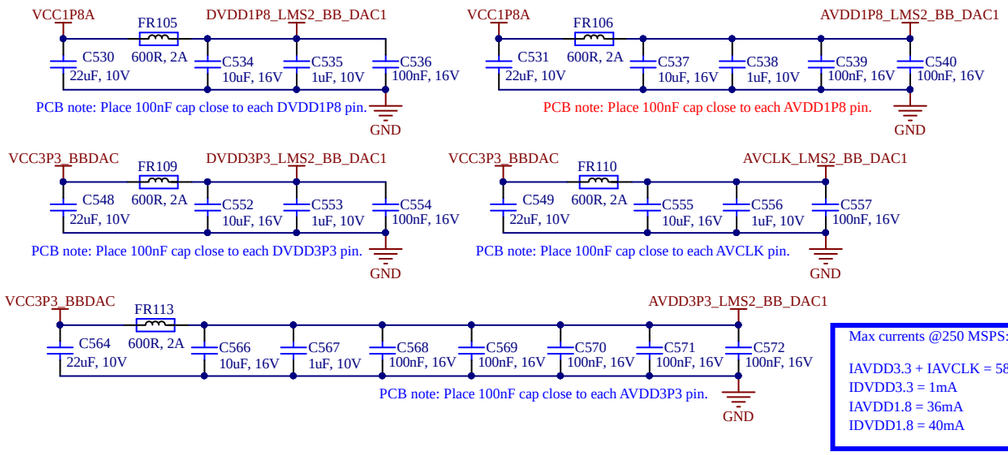
Lime microsystems

NF elements on sheet: R520, C522, C521, C523
Number of NF elements on sheet: 4

LMS2_TX1_BB DAC

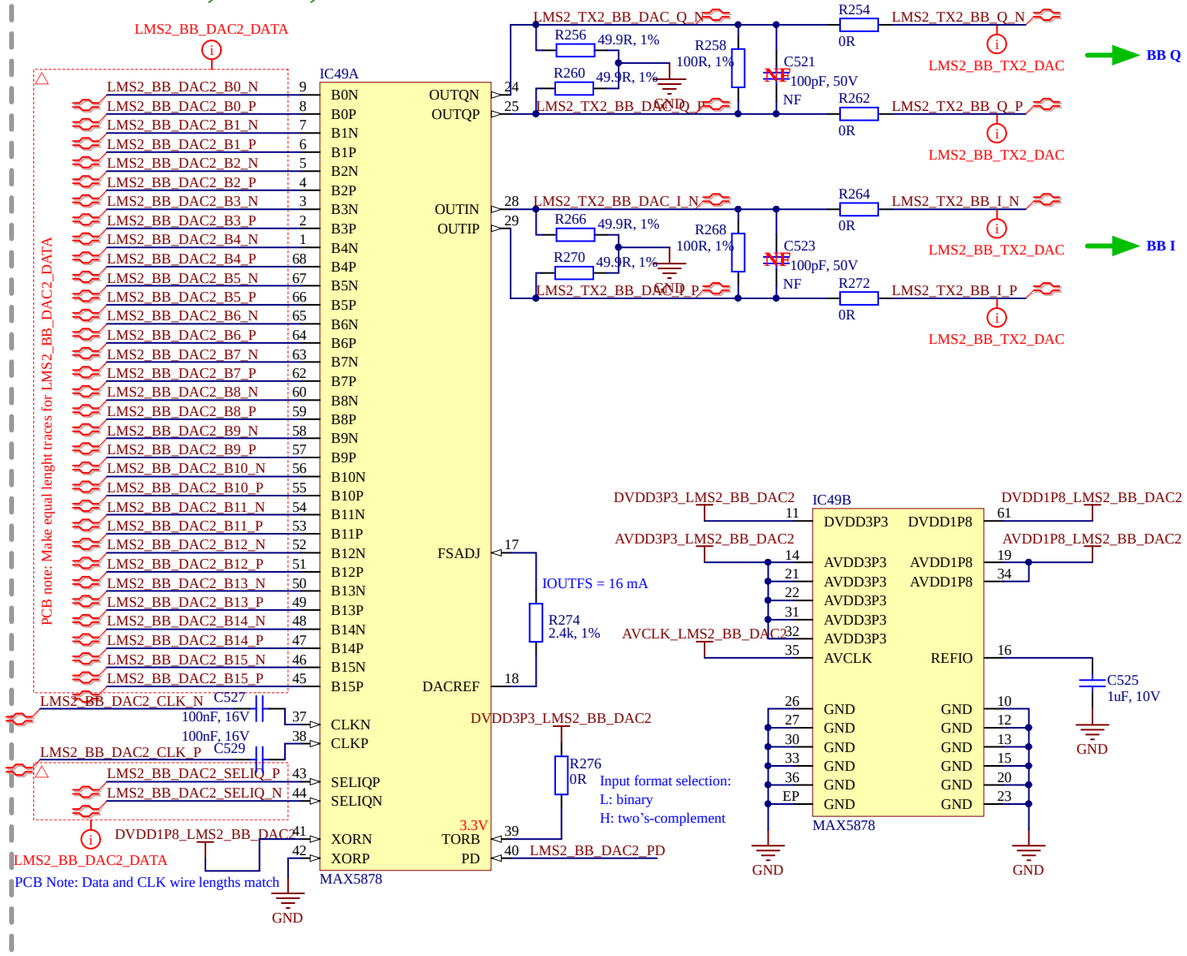
2 ch., 16-bit, 250MSPS





LMS2_TX2_BB DAC

2 ch., 16-bit, 250MSPS



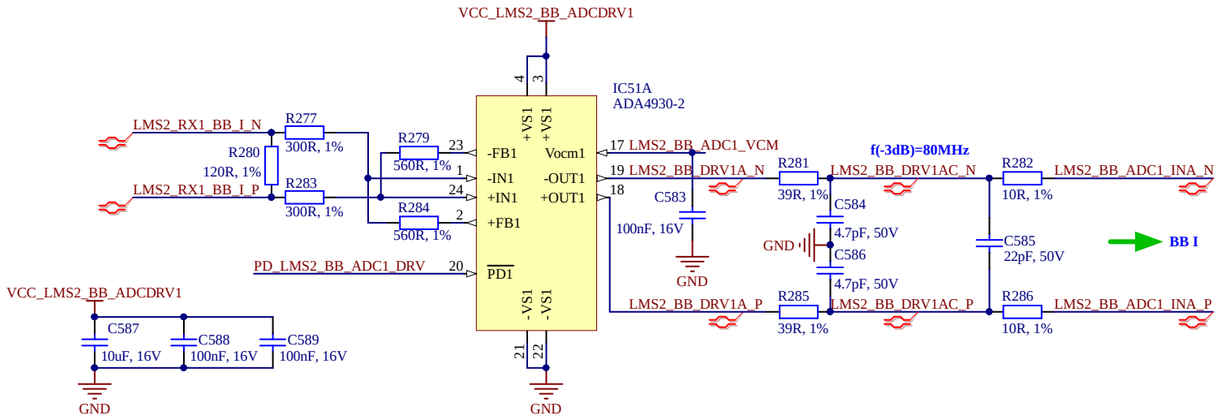
Project name:	*LimeSDR-X3_1v1.PrjPcb*
Title:	*LMS2 TX BB DACs*
Size:	A3
Revision:	v1.1
Date:	2024-06-11
Time:	10:27:47
Sheet	22 of 31
File:	22_LMS2_TX_BB_DACs.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

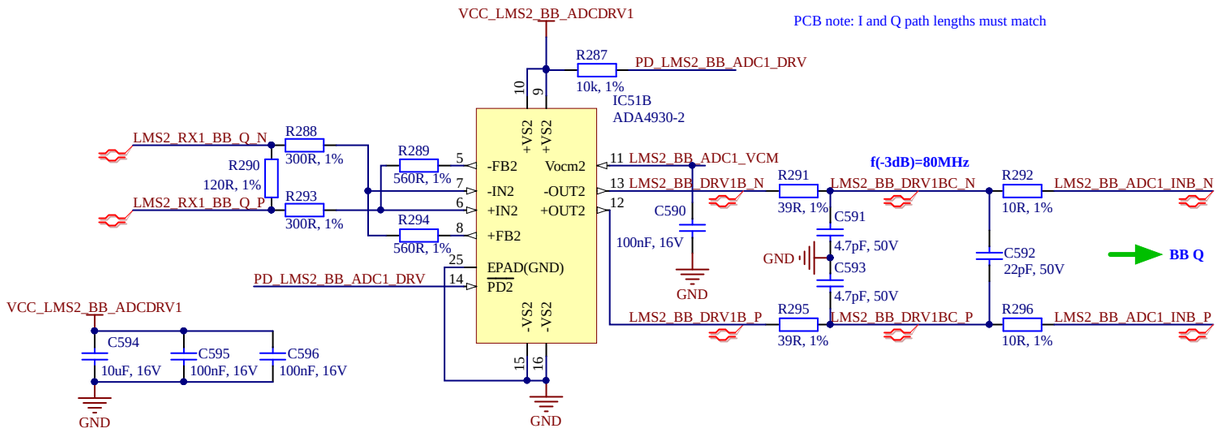
NF elements on sheet: R304
Number of NF elements on sheet: 1

LMS2 RX1 BB ADC

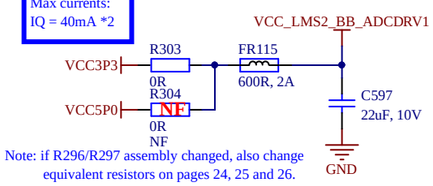
ADC Drivers



PCB note: I and Q path lengths must match



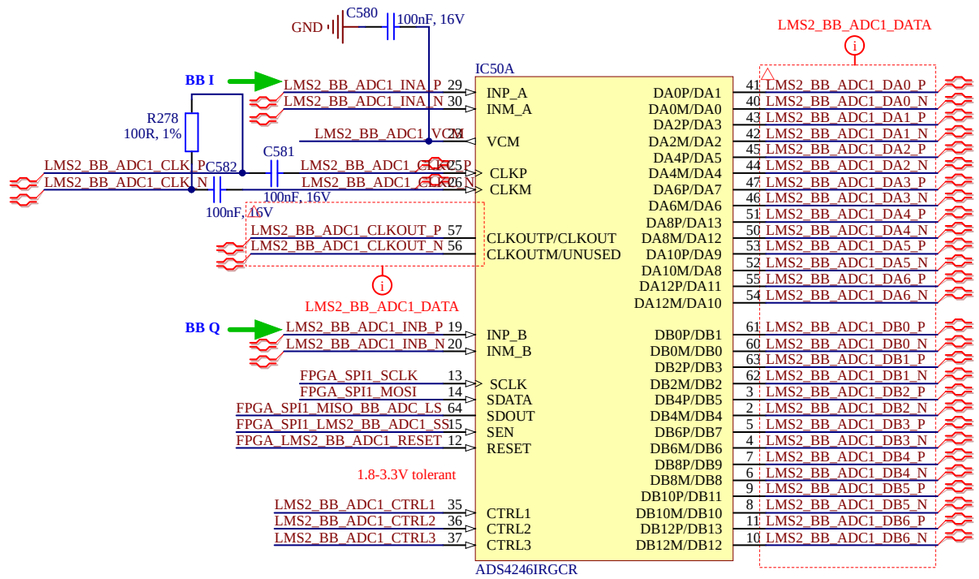
Max currents:
IQ = 40mA *2



Note: if R296/R297 assembly changed, also change equivalent resistors on pages 24, 25 and 26.

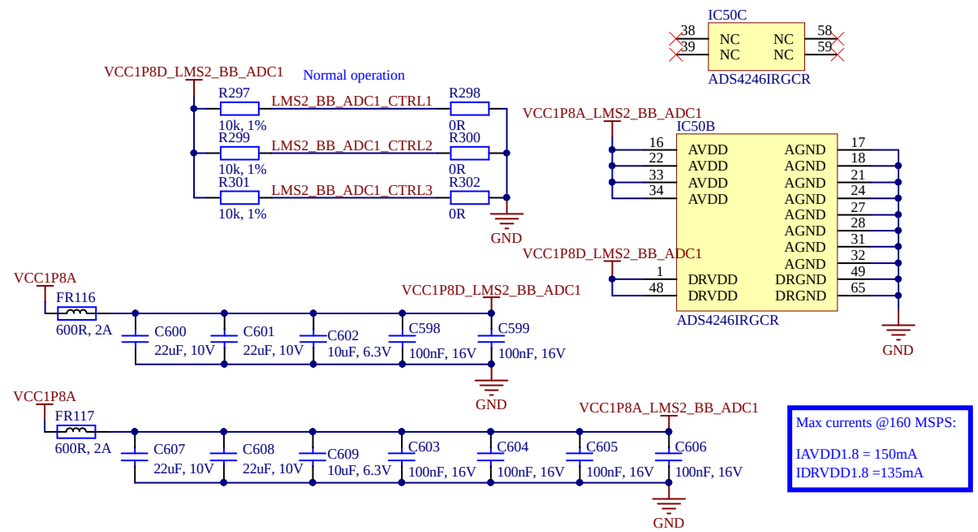
ADC

2 ch., 14-bit, 160MSPS



PCB note: Make equal lenght traces for LMS2_BB_ADC1_DATA

ADC Control & Power



Max currents @160 MSPS:

IAVDD1.8 = 150mA
IDRVDD1.8 =135mA

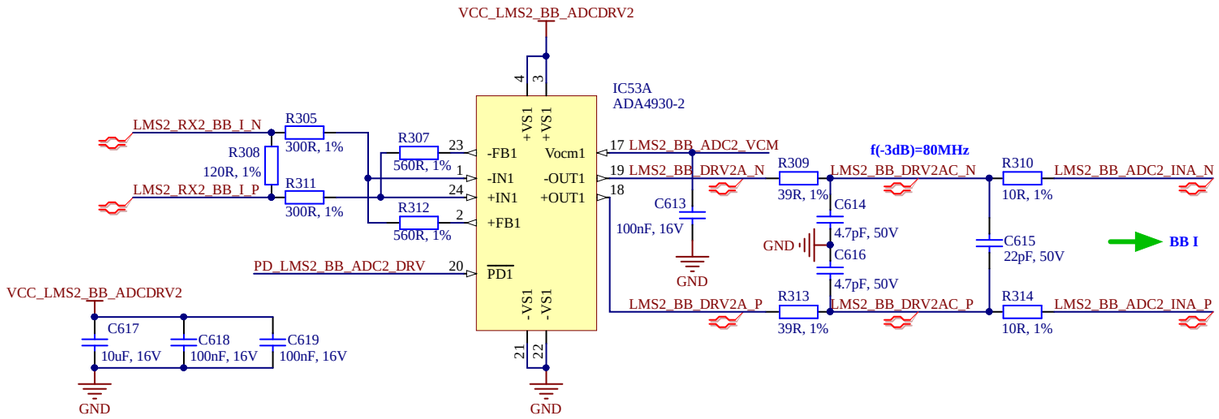
Local ADC and DAC fiducial Top
FL17

Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*LMS2 RX1 BB ADC*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:27:51	Sheet 23 of 31	
File: 23_LMS2_RX1_BB_ADC.SchDoc			

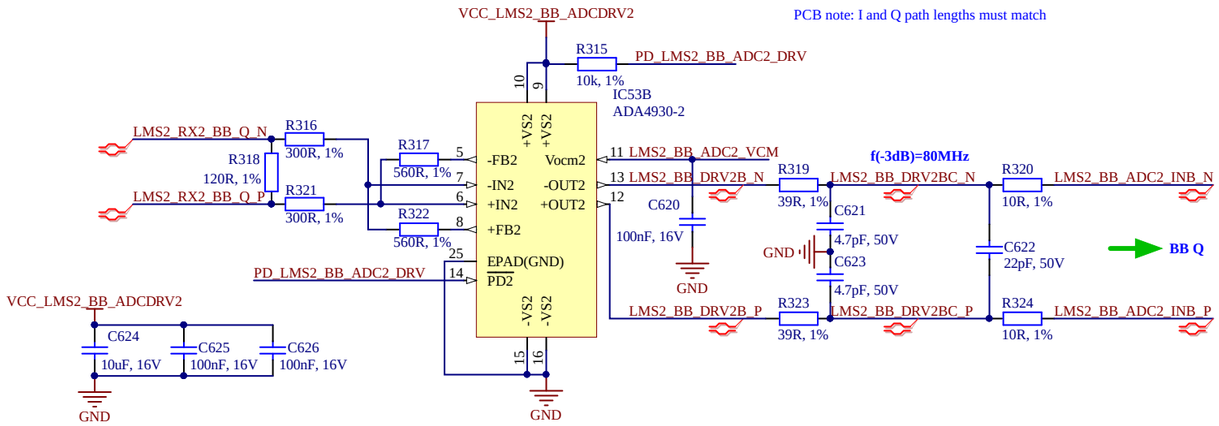
NF elements on sheet: R332
Number of NF elements on sheet: 1

LMS2 RX2 BB ADC

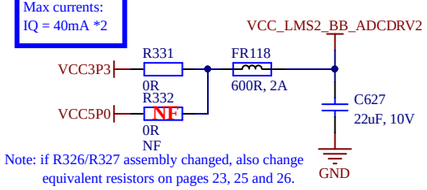
ADC Drivers



PCB note: I and Q path lengths must match



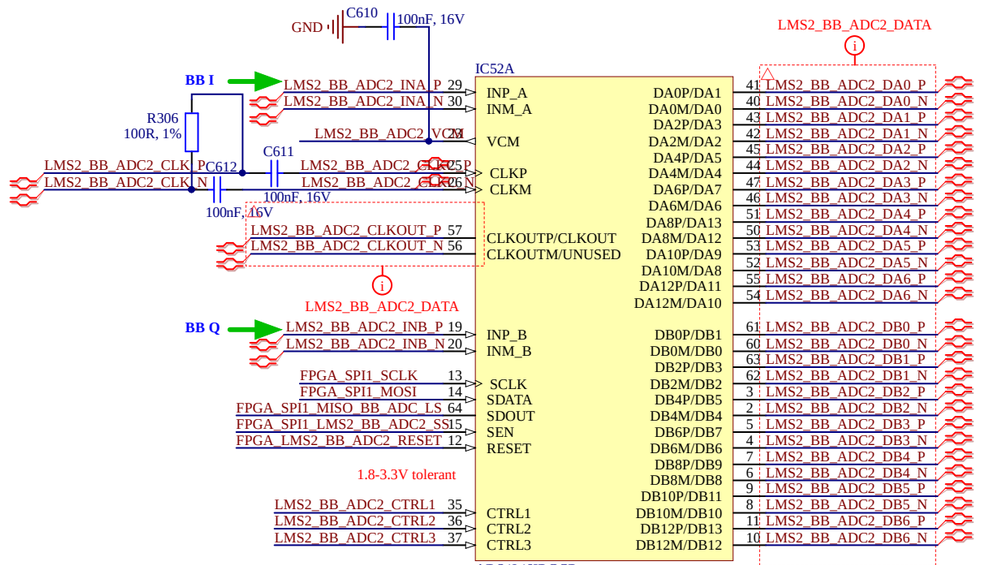
Max currents:
IQ = 40mA *2



Note: if R326/R327 assembly changed, also change equivalent resistors on pages 23, 25 and 26.

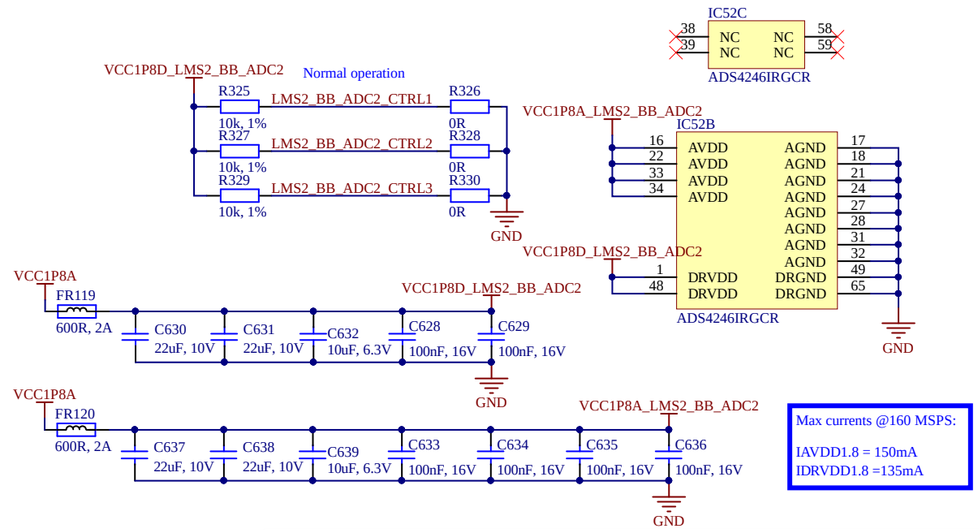
ADC

2 ch., 14-bit, 160MSPS



PCB note: Make equal lenght traces for LMS2_BB_ADC2_DATA

ADC Control & Power



Max currents @160 MSPS:

IAVDD1.8 = 150mA
IDRVDD1.8 =135mA

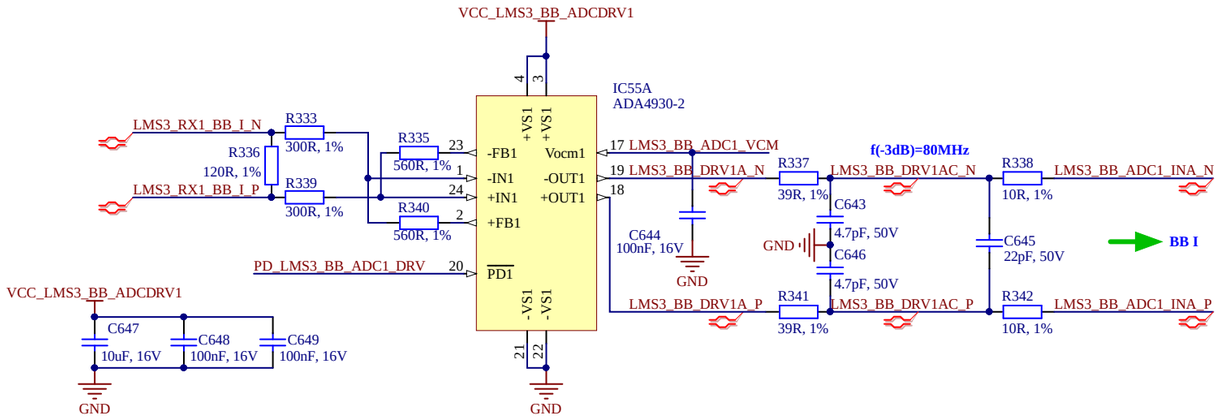
Local ADC and DAC fiducial Top
FL18

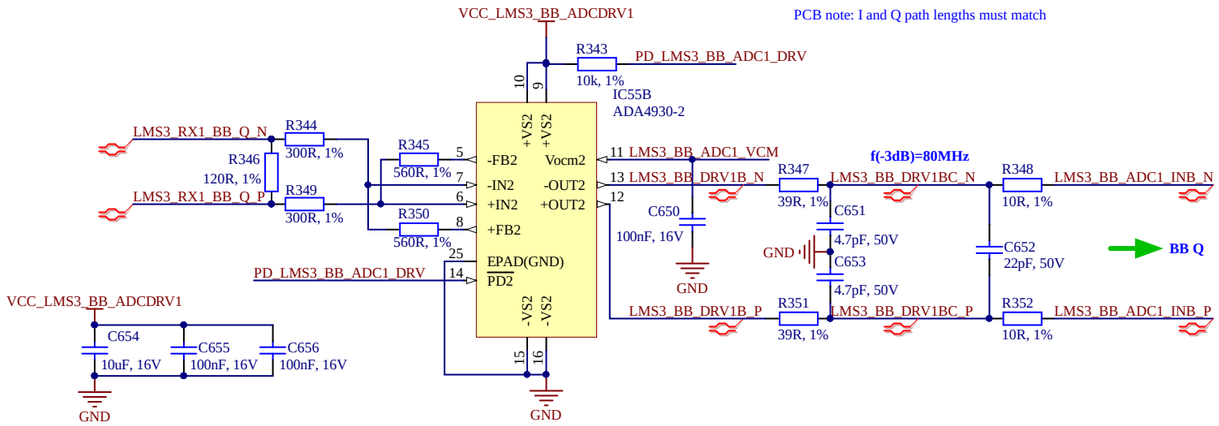
Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*LMS2 RX2 BB ADC*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:27:54	Sheet 24 of 31	
File: 24_LMS2_RX2_BB_ADC.SchDoc			

NF elements on sheet: R360
Number of NF elements on sheet: 1

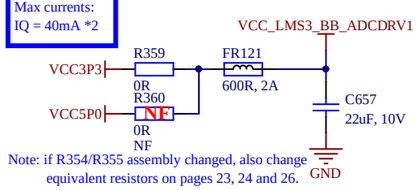
LMS3 RX1 BB ADC

ADC Drivers





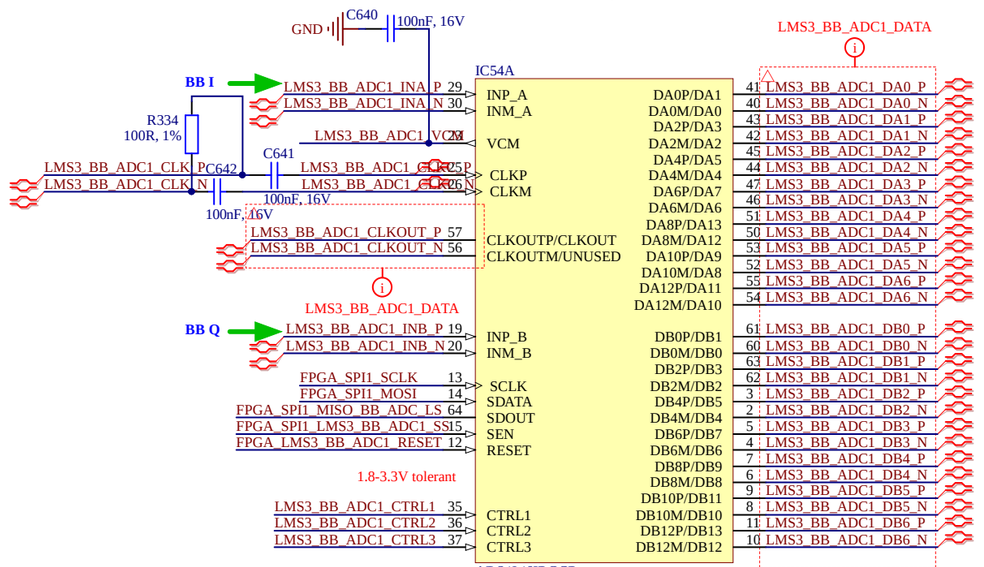
Max currents:
IQ = 40mA *2



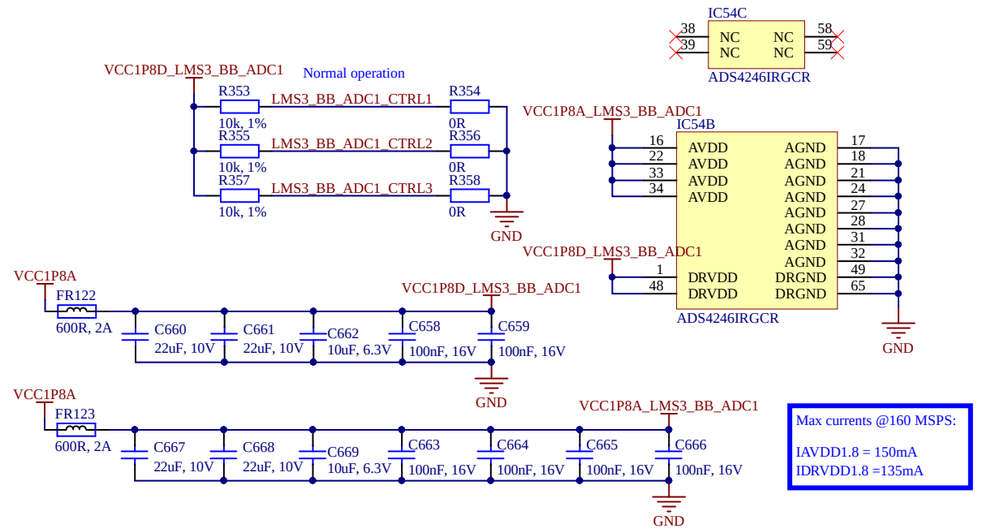
Note: if R354/R355 assembly changed, also change equivalent resistors on pages 23, 24 and 26.

ADC

2 ch., 14-bit, 160MSPS



ADC Control & Power



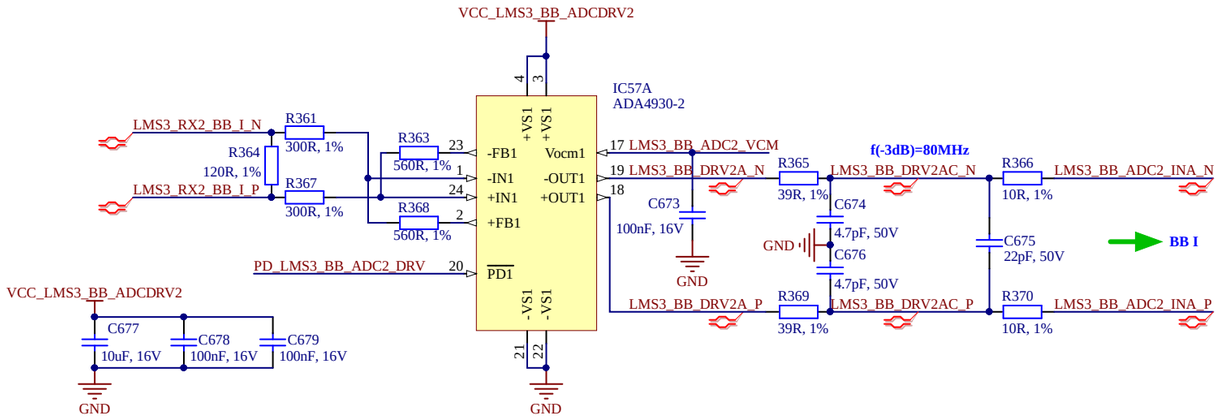
Local ADC and DAC fiducial Top
FL19

Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*LMS3 RX1 BB ADC*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.0		
Date: 2024-06-11	Time: 10:27:58	Sheet 25 of 31	
File: 25_LMS3_RX1_BB_ADC.SchDoc			

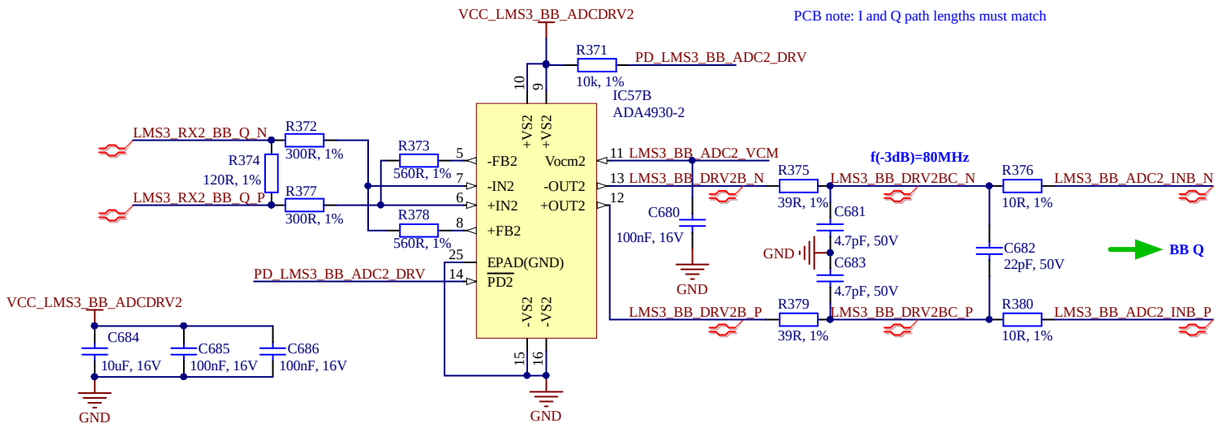
NF elements on sheet: R388
Number of NF elements on sheet: 1

LMS3 RX2 BB ADC

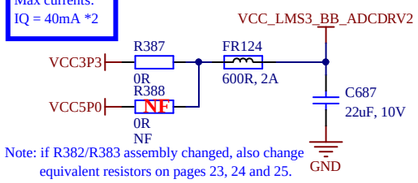
ADC Drivers



PCB note: I and Q path lengths must match



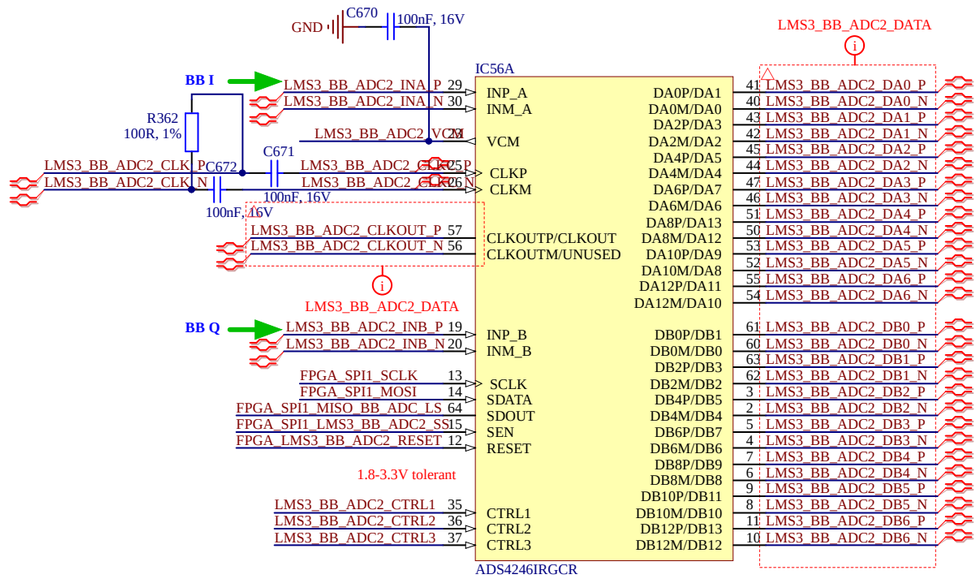
Max currents:
IQ = 40mA *2



Note: if R382/R383 assembly changed, also change equivalent resistors on pages 23, 24 and 25.

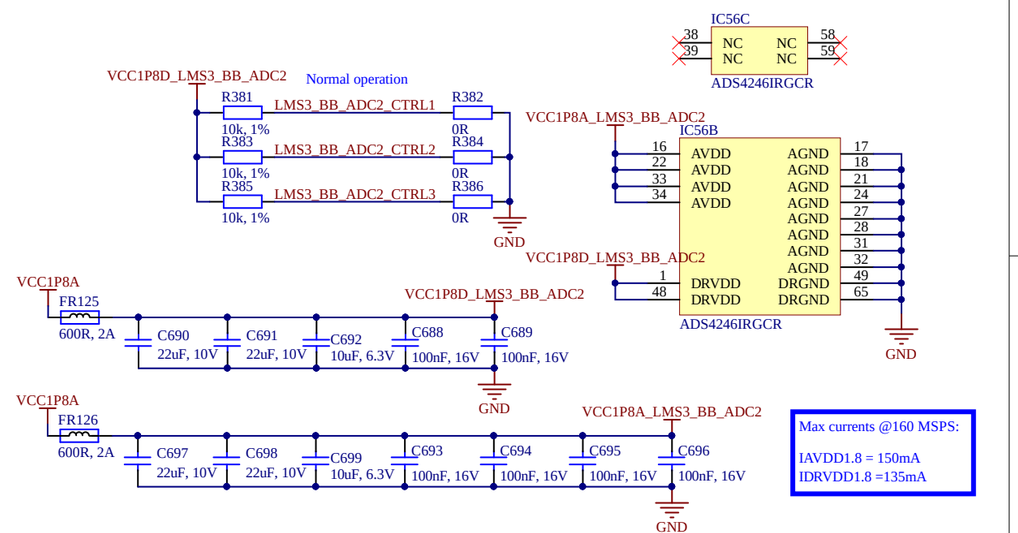
ADC

2 ch., 14-bit, 160MSPS



PCB note: Make equal lenght traces for LMS3_BB_ADC2_DATA

ADC Control & Power



Max currents @160 MSPS:

IAVDD1.8 = 150mA
IDRVDD1.8 =135mA

Local ADC and DAC fiducial Top

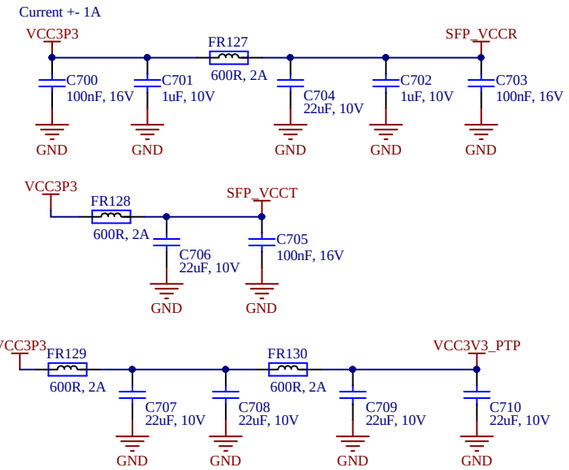
FL20

Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	*LMS3 RX2 BB ADC*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:28:01	Sheet 26 of 31	
File: 26_LMS3_RX2_BB_ADC.SchDoc			

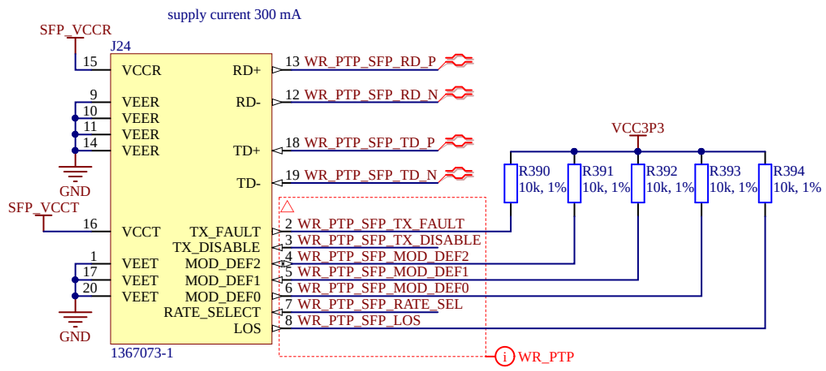
NF elements on sheet: R396, R401, R402, C725, IC60, R404, R405, R406, R407, R408, R409, R412, R415
Number of NF elements on sheet: 13

White Rabbit PTP

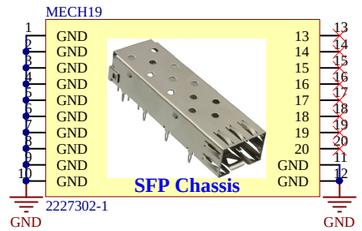
Power filters



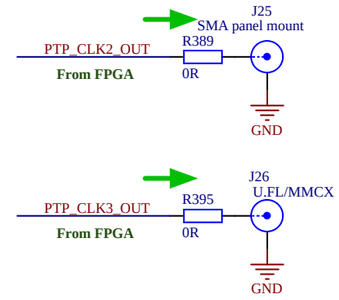
SFP connector



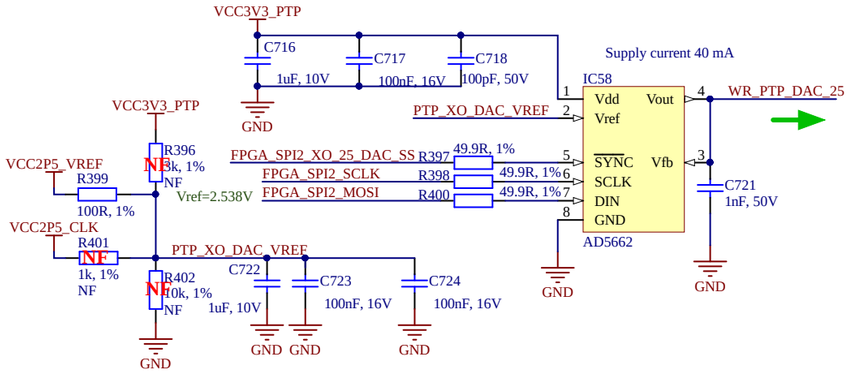
Compliant SFP devices see "http://www.ohwr.org/projects/white-rabbit/wiki/SFP"



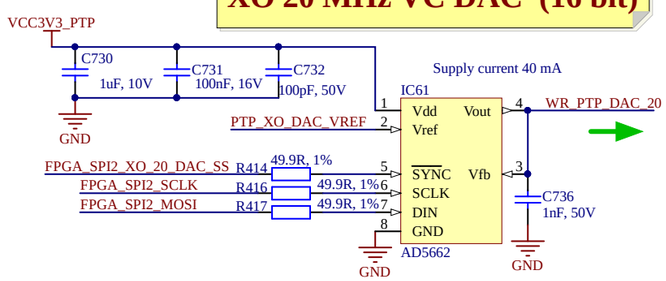
PTP CLK OUT



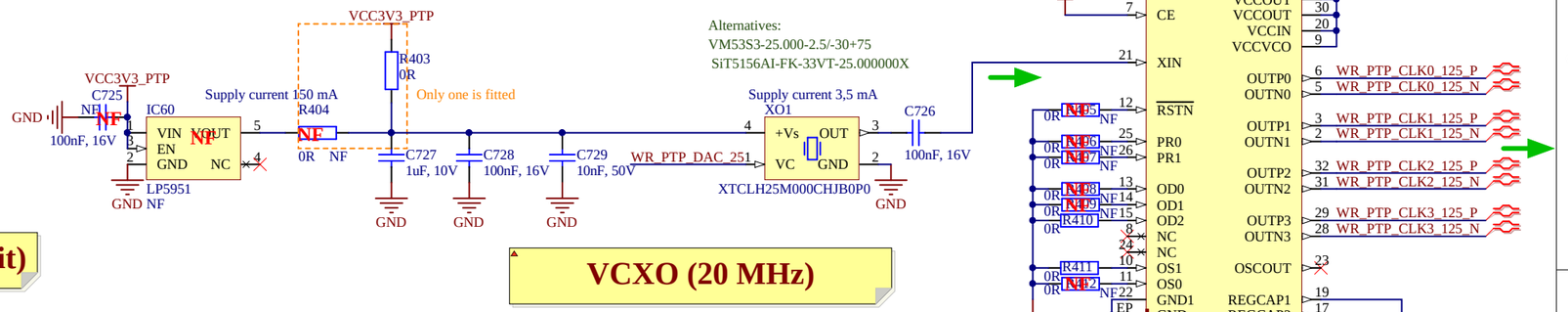
XO 25 MHz VC DAC (16 bit)



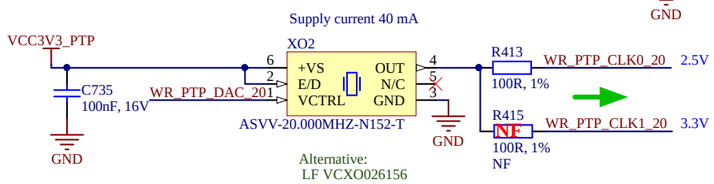
XO 20 MHz VC DAC (16 bit)



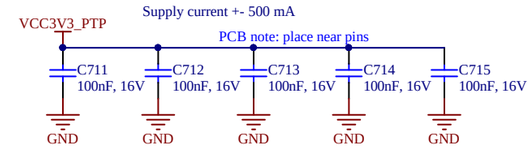
VCTCXO (25 MHz)



VCXO (20 MHz)

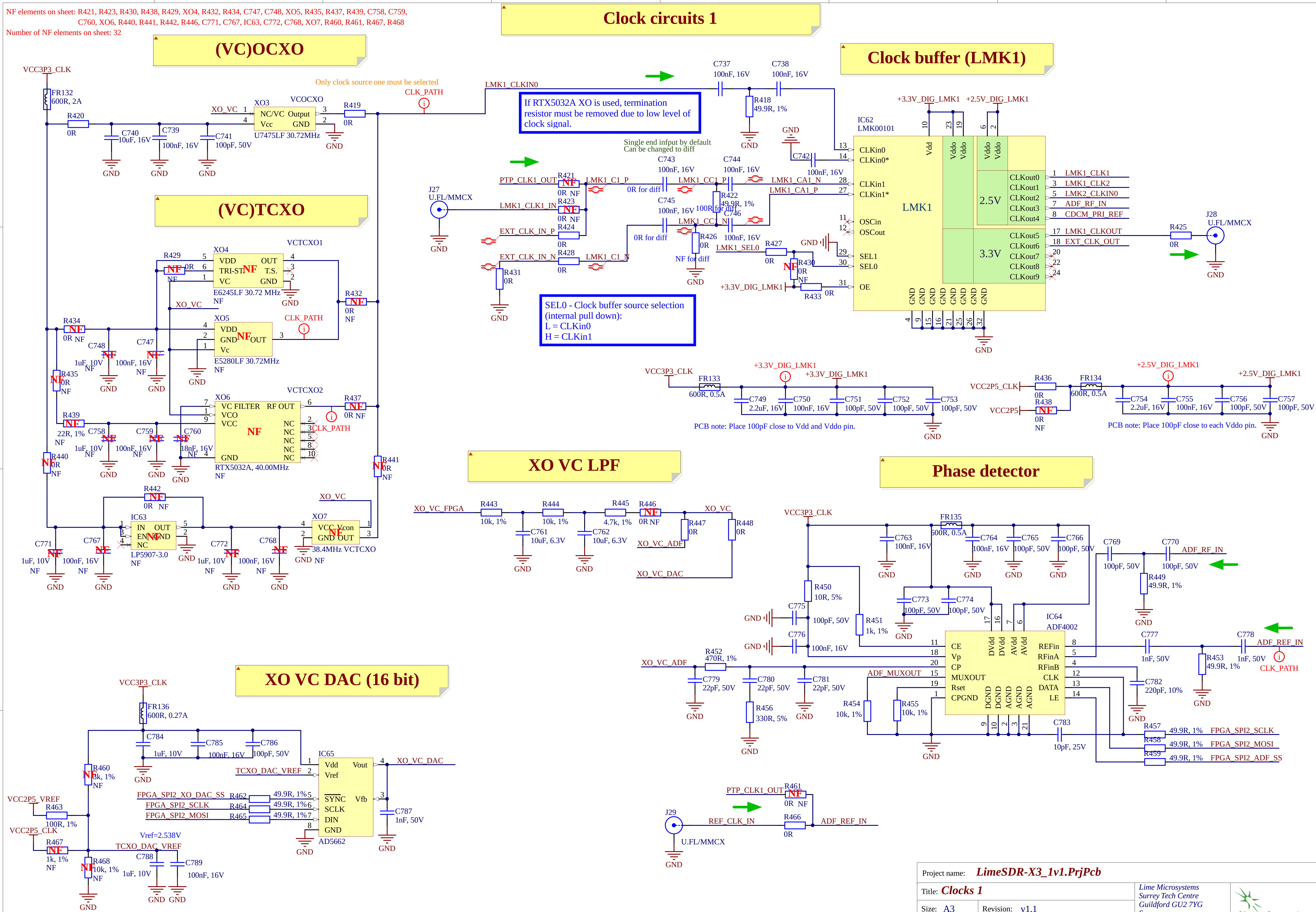


Frequency synthesizer



Config (pins have internal pull-ups):
Presc. div. = 4, feedbak div. = 20 (PR [1 1])
Output divider = 4 (OD [0 1 1])
Output Type: LVDS, OSC_OUT Off (OS [0 1])

Project name: *LimeSDR-X3_1v1.PrjPcb*			
Title: *White Rabbit PTP*			Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:28:06	Sheet 27 of 31	
File: 27_WR_PTP.SchDoc			



Project name: *LimeSDR-X3_1v1.PrjPcb*

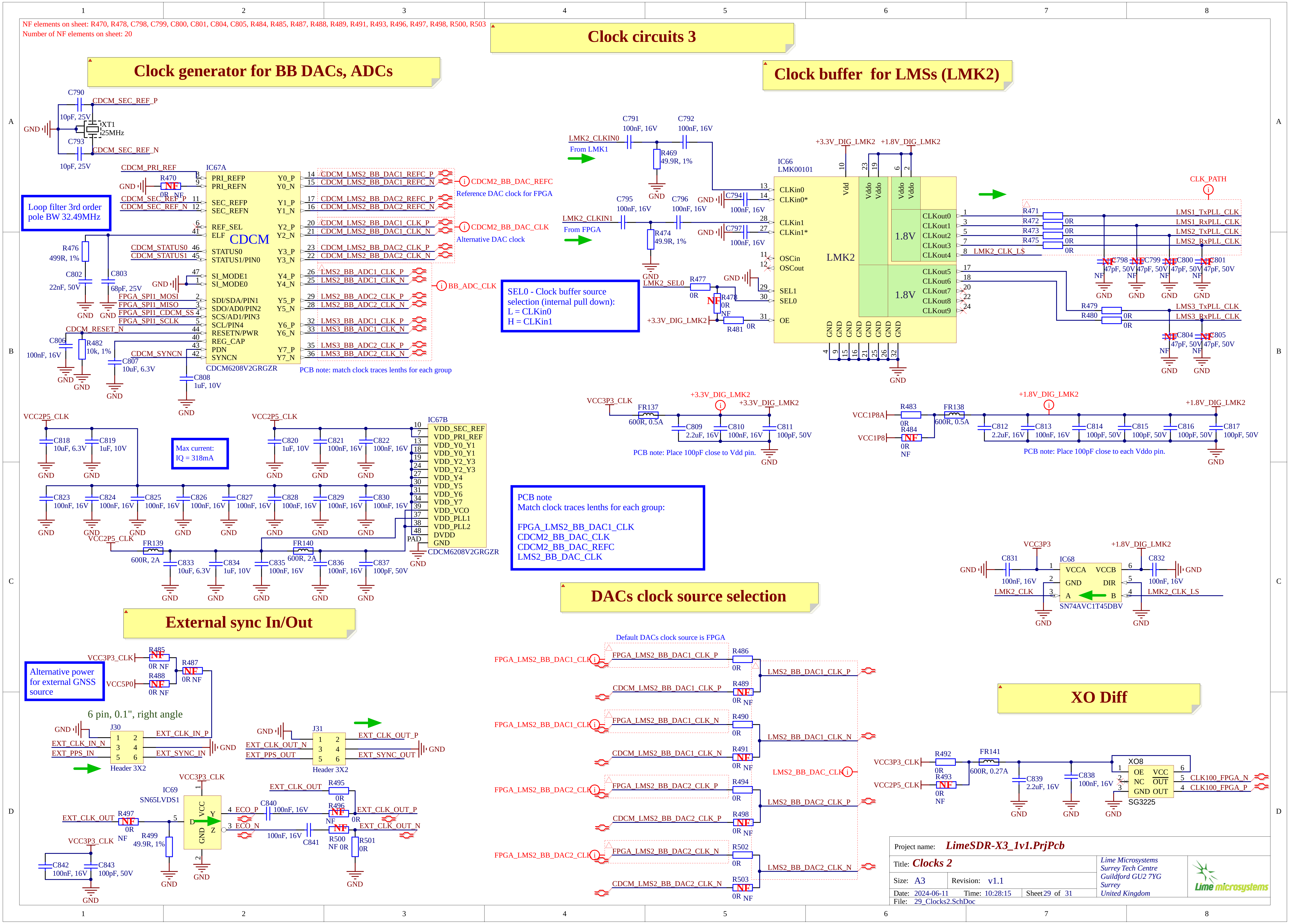
Title: **Clocks 1**

Size: A3 | Revision: v1.1

Date: 2024-06-11 Time: 10:28:10 Sheet 28 of 31

File: 28_Clocks1.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



NF elements on sheet: R470, R478, C798, C799, C800, C801, C804, C805, R484, R485, R487, R488, R489, R491, R493, R496, R497, R498, R500, R503
Number of NF elements on sheet: 20
Clock circuits 3
Clock generator for BB DACs, ADCs
Clock buffer for LMSs (LMK2)
C790
10pF, 25V
CDCM_SEC_REF_P
GND
XT1
25MHz
C793
10pF, 25V
CDCM_SEC_REF_N
CDCM_PRI_REF
IC67A
R470
0R NF
PRI_REFP
PRI_REFN
CDCM_SEC_REF_P
CDCM_SEC_REF_N
SEC_REFP
SEC_REFN
Loop filter 3rd order
pole BW 32.49MHz
REF_SEL
ELF
CDCM
R476
499R, 1%
C802
22nF, 50V
C803
68pF, 25V
CDCM_STATUS0
CDCM_STATUS1
STATUS0
STATUS1/PIN0
SI_MODE1
SI_MODE0
FPGA_SPI1_MOSI
FPGA_SPI1_MISO
FPGA_SPI1_CDCM_SS
FPGA_SPI1_SCLK
SDI/SDA/PIN1
SDO/AD0/PIN2
SCS/AD1/PIN3
SCL/PIN4
CDCM_RESET_N
RESETN/PWR
REG_CAP
PDN
SYNCN
C806
100nF, 16V
R482
10k, 1%
C807
10uF, 6.3V
CDCM_SYNCN
C808
1uF, 10V
CDCM6208V2GRGZR
Y0_P
Y0_N
Y1_P
Y1_N
Y2_P
Y2_N
Y3_P
Y3_N
Y4_P
Y4_N
Y5_P
Y5_N
Y6_P
Y6_N
Y7_P
Y7_N
CDCM_LMS2_BB_DAC1_REFC_P
CDCM_LMS2_BB_DAC1_REFC_N
CDCM_LMS2_BB_DAC2_REFC_P
CDCM_LMS2_BB_DAC2_REFC_N
CDCM_LMS2_BB_DAC1_CLK_P
CDCM_LMS2_BB_DAC1_CLK_N
CDCM_LMS2_BB_DAC2_CLK_P
CDCM_LMS2_BB_DAC2_CLK_N
LMS2_BB_ADC1_CLK_P
LMS2_BB_ADC1_CLK_N
LMS2_BB_ADC2_CLK_P
LMS2_BB_ADC2_CLK_N
LMS3_BB_ADC1_CLK_P
LMS3_BB_ADC1_CLK_N
LMS3_BB_ADC2_CLK_P
LMS3_BB_ADC2_CLK_N
CDCM2_BB_DAC_REFC
Reference DAC clock for FPGA
CDCM2_BB_DAC_CLK
Alternative DAC clock
BB_ADC_CLK
PCB note: match clock traces lenths for each group
LMK2_CLKIN0
From LMK1
C791
100nF, 16V
C792
100nF, 16V
R469
49.9R, 1%
C794
100nF, 16V
LMK2_CLKIN1
From FPGA
C795
100nF, 16V
C796
100nF, 16V
R474
49.9R, 1%
C797
100nF, 16V
LMK2_SEL0
R477
0R
R478
0R
NF
R481
0R
+3.3V_DIG_LMK2
+1.8V_DIG_LMK2
IC66
LMK00101
CLKin0
CLKin0*
CLKin1
CLKin1*
OSCin
OSCout
SEL1
SEL0
OE
Vdd
Vddo
LMK2
1.8V
CLKout0
CLKout1
CLKout2
CLKout3
CLKout4
CLKout5
CLKout6
CLKout7
CLKout8
CLKout9
SEL0 - Clock buffer source
selection (internal pull down):
L = CLKin0
H = CLKin1
CLK_PATH
R471
R472
R473
R475
0R
LMS1_TxPLL_CLK
LMS1_RxPLL_CLK
LMS2_TxPLL_CLK
LMS2_RxPLL_CLK
LMK2_CLK_LS
C798
C799
C800
C801
47pF, 50V
R479
R480
LMS3_TxPLL_CLK
LMS3_RxPLL_CLK
C804
C805
VCC3P3_CLK
FR137
600R, 0.5A
C809
2.2uF, 16V
C810
100nF, 16V
C811
100pF, 50V
PCB note: Place 100pF close to Vdd pin.
VCC1P8A
VCC1P8
R483
0R
R484
0R
NF
FR138
600R, 0.5A
C812
2.2uF, 16V
C813
100nF, 16V
C814
C815
C816
C817
100pF, 50V
PCB note: Place 100pF close to each Vddo pin.
VCC2P5_CLK
C818
10uF, 6.3V
C819
1uF, 10V
Max current:
IQ = 318mA
C820
1uF, 10V
C821
100nF, 16V
C822
100nF, 16V
IC67B
VDD_SEC_REF
VDD_PRI_REF
VDD_Y0_Y1
VDD_Y2_Y3
VDD_Y4
VDD_Y5
VDD_Y6
VDD_Y7
VDD_VCO
VDD_PLL1
VDD_PLL2
DVDD
GND
CDCM6208V2GRGZR
C823
C824
C825
C826
C827
C828
C829
C830
100nF, 16V
FR139
600R, 2A
C833
10uF, 6.3V
C834
1uF, 10V
C835
100nF, 16V
FR140
600R, 2A
C836
100nF, 16V
C837
100pF, 50V
PCB note
Match clock traces lenths for each group:
FPGA_LMS2_BB_DAC1_CLK
CDCM2_BB_DAC_CLK
CDCM2_BB_DAC_REFC
LMS2_BB_DAC_CLK
VCC3P3
C831
100nF, 16V
IC68
VCCA
VCCB
GND
DIR
A
B
C832
100nF, 16V
LMK2_CLK
LMK2_CLK_LS
SN74AVC1T45DBV
DACs clock source selection
External sync In/Out
Alternative power
for external GNSS
source
VCC3P3_CLK
VCC5P0
R485
0R NF
R487
0R NF
R488
0R NF
6 pin, 0.1", right angle
J30
EXT_CLK_IN_N
EXT_PPS_IN
EXT_CLK_IN_P
EXT_SYNC_IN
Header 3X2
J31
EXT_CLK_OUT_N
EXT_PPS_OUT
EXT_CLK_OUT_P
EXT_SYNC_OUT
Header 3X2
IC69
SN65LVDS1
EXT_CLK_OUT
R495
0R
R496
0R
NF
ECO_P
ECO_N
C840
100nF, 16V
C841
100nF, 16V
R497
0R
NF
R499
49.9R, 1%
R500
NF 0R
R501
0R
C842
100nF, 16V
C843
100pF, 50V
Default DACs clock source is FPGA
FPGA_LMS2_BB_DAC1_CLK
FPGA_LMS2_BB_DAC1_CLK_P
CDCM_LMS2_BB_DAC1_CLK_P
FPGA_LMS2_BB_DAC1_CLK_N
CDCM_LMS2_BB_DAC1_CLK_N
FPGA_LMS2_BB_DAC2_CLK
FPGA_LMS2_BB_DAC2_CLK_P
CDCM_LMS2_BB_DAC2_CLK_P
FPGA_LMS2_BB_DAC2_CLK_N
CDCM_LMS2_BB_DAC2_CLK_N
R486
R489
R490
R491
R494
R498
R502
R503
LMS2_BB_DAC1_CLK_P
LMS2_BB_DAC1_CLK_N
LMS2_BB_DAC_CLK
LMS2_BB_DAC2_CLK_P
LMS2_BB_DAC2_CLK_N
XO Diff
VCC3P3_CLK
VCC2P5_CLK
R492
0R
R493
0R
NF
FR141
600R, 0.27A
C839
2.2uF, 16V
C838
100nF, 16V
XO8
OE
NC
GND
VCC
OUT
OUT
SG3225
CLK100_FPGA_N
CLK100_FPGA_P
Project name: LimeSDR-X3_1v1.PrjPcb
Title: Clocks 2
Size: A3
Revision: v1.1
Date: 2024-06-11
Time: 10:28:15
Sheet29 of 31
File: 29_Clocks2.SchDoc
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

NF elements on sheet: J32, R506, R507, R509, R516, R528, C852, R517, C855, R518, C858, R535, R536, C882, R534, C885, R548, C902, C903, R546, FUSE1
Number of NF elements on sheet: 21

Board power circuits 1

Main switching regulators

Soft power control. Remove EN_VCC1P0_INT 0R resistor and control board power by shorting J32 pins.

Default power sequence:
VCC1P0_INT -> VCC1P0 -> Rest regulators

1.0V 6A

1.0V 6A

1.2V 6A

1.8V 6A

2.5V 6A

3.3V 6A

5.0V 6A

RF PA power selection

Note: for PGA-102+

Note: for TQP369182
Use together with current limiting resistors (R145, R134)

Power input

PCIe Slot (max. 25W)

6-pin PCIe connector (max. 75W)

0.2" connector

0.1" connector

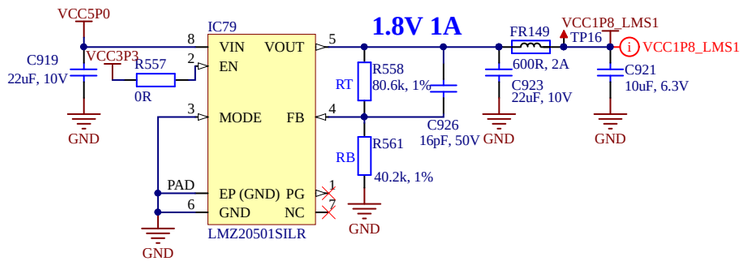
Project name:	LimeSDR-X3_1v1.PrjPcb
Title:	Board power supply 1
Size:	A3
Revision:	v1.1
Date:	2024-06-11
Time:	10:28:20
Sheet	30 of 31
File:	30_Power1.SchDoc

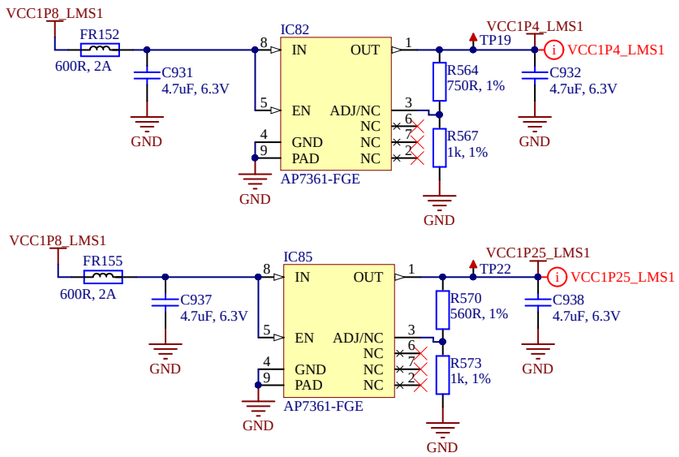
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

NF elements on sheet: FR156, FR157, R574,C947, R586, FR163, FR161, R580
Number of NF elements on sheet: 8
Total number of NF elements on all sheets: 176

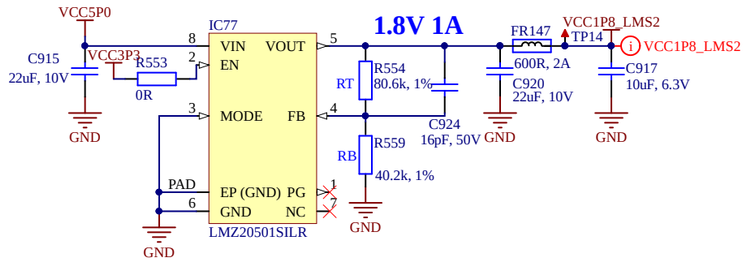
Board power circuits 2

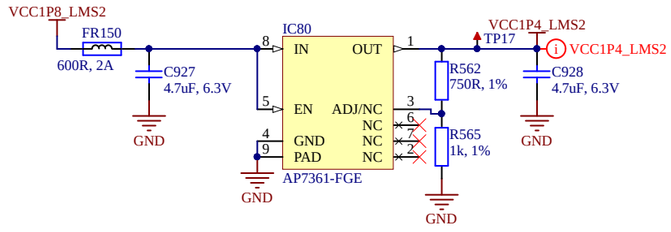
LMS 1

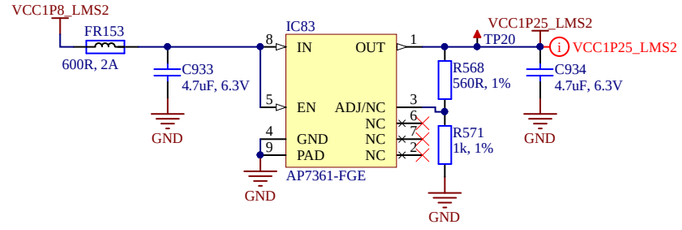




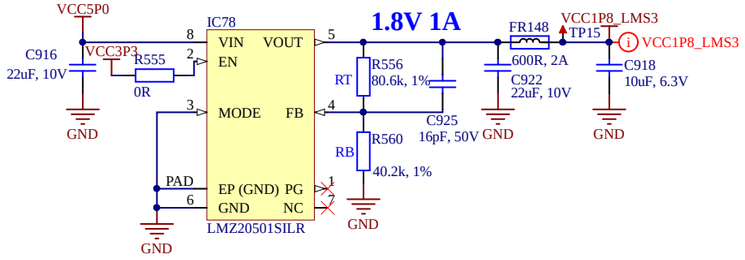
LMS 2

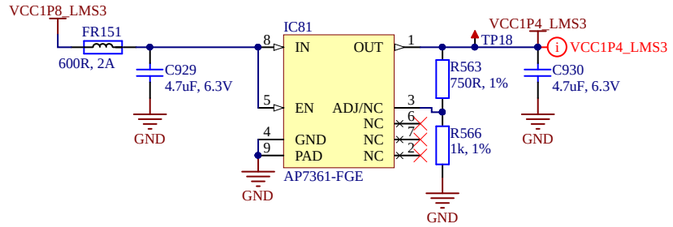


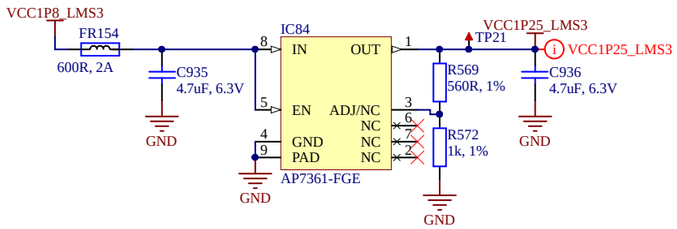




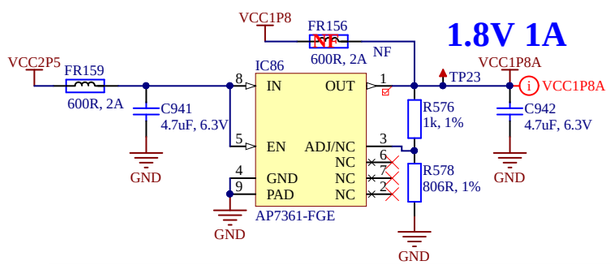
LMS 3



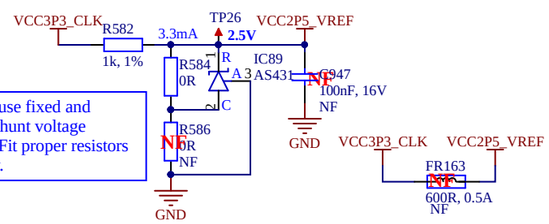




Misc power

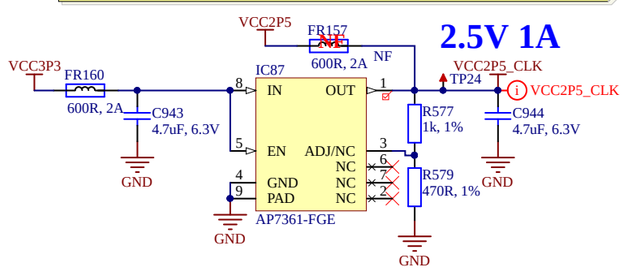


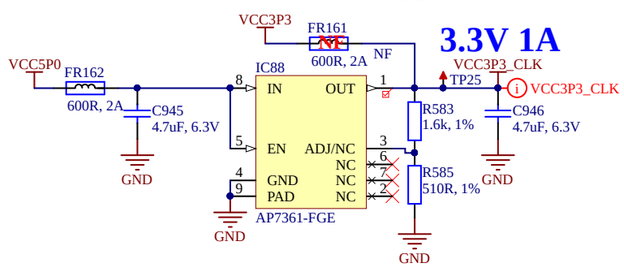
Voltage reference (2.5V)



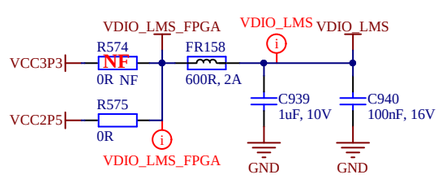
Possible to use fixed and adjustable shunt voltage references. Fit proper resistors accordingly.

Clock network power

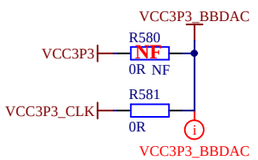




LMS VDIO power selection



VCC3P3_BBDAC power selection



Project name:	*LimeSDR-X3_1v1.PrjPcb*		
Title:	***Board power supply 2***		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2024-06-11	Time: 10:28:25	Sheet 31 of 31	
File: 31_Power2.SchDoc			