mBldcm Register Map ver. 2.00

1. Summary of Register Map

Offset	Register Name	R/W/H (*1)	Bit								Note
			31-28	27-17	16-12	11-6	5	4-2	1	0	
0x0	FREQTGT	R/W	FREQTGT								-
0x4	PWM_CMP	R/W	*RESERVED*		PWM_CMP						-
0x8	CTRL	R/W/H	*RESERVED*	PWM_MAXCNT		PWM_PRSC	W_PHASE	PHASE	BRK	EN	CTRL.BRK is not implemented now.
0xC	STAT	R	*RESERVED*						REFLECTEDFREQ	STOP	-

(*1) … ‘R’ means read-only. ‘W’ means write-only and invalid value is read when read. ‘R/W’ means readable and writable. ‘R/W/H’ means R/W and the value can be changed by hardware.

2. Descriptions of Bit Fields

2.1. FREQTGT

Bit Field	Initial Value	Description
FREQTGT	32’h00000000	Target frequency of rotation (Rotate per second)

2.2. PWM_CMP

Bit Field	Initial Value	Description
PWM_CMP	17’h00000	Comparison value used to determine PWM duty. The PWM signal is turned on when PWM_CMP is greater than PWM_MAXCNT. (Range: 17’h00000 to 17’h10000)

2.3. CTRL

Bit Field	Initial Value	Description
PWM_MAXCNT	16’hFFFF	Maximum value of PWM counter. (Range: 16’h0001 to 16’hFFFF)
PWM_PRSC	6’h00	Clock division of PWM counter in the format of “(1/2)^[PWM_PRSC]”. (Range: 0 to 32)
W_PHASE	1’h0	Write PHASE register. Only if this bit is set at writing, PHASE bit-field is accepted by hardware. Always return ‘1’b0’ at reading.
PHASE	3’h00	Phase of rotation. Only if W_PHASE bit is set at writing, this bit-field is accepted by hardware. Return current phase at reading. (Range: 0 to 6)
BRK	-	*RESERVED*
EN	1’h0	Enable signal output. This bit is set, then mBldcm outputs a signal to excite a motor. Cleared, not output.

2.4 STAT

Bit Field	Initial Value	Description
STOP	1’h1	Indicates that motor is stopped. (0: Not stopped, 1: Stopped)
REFLECTEDFREQ	1’h1	Indicates that the value of FREQTGT is reflected. (0: Not reflected, 1: Reflected)