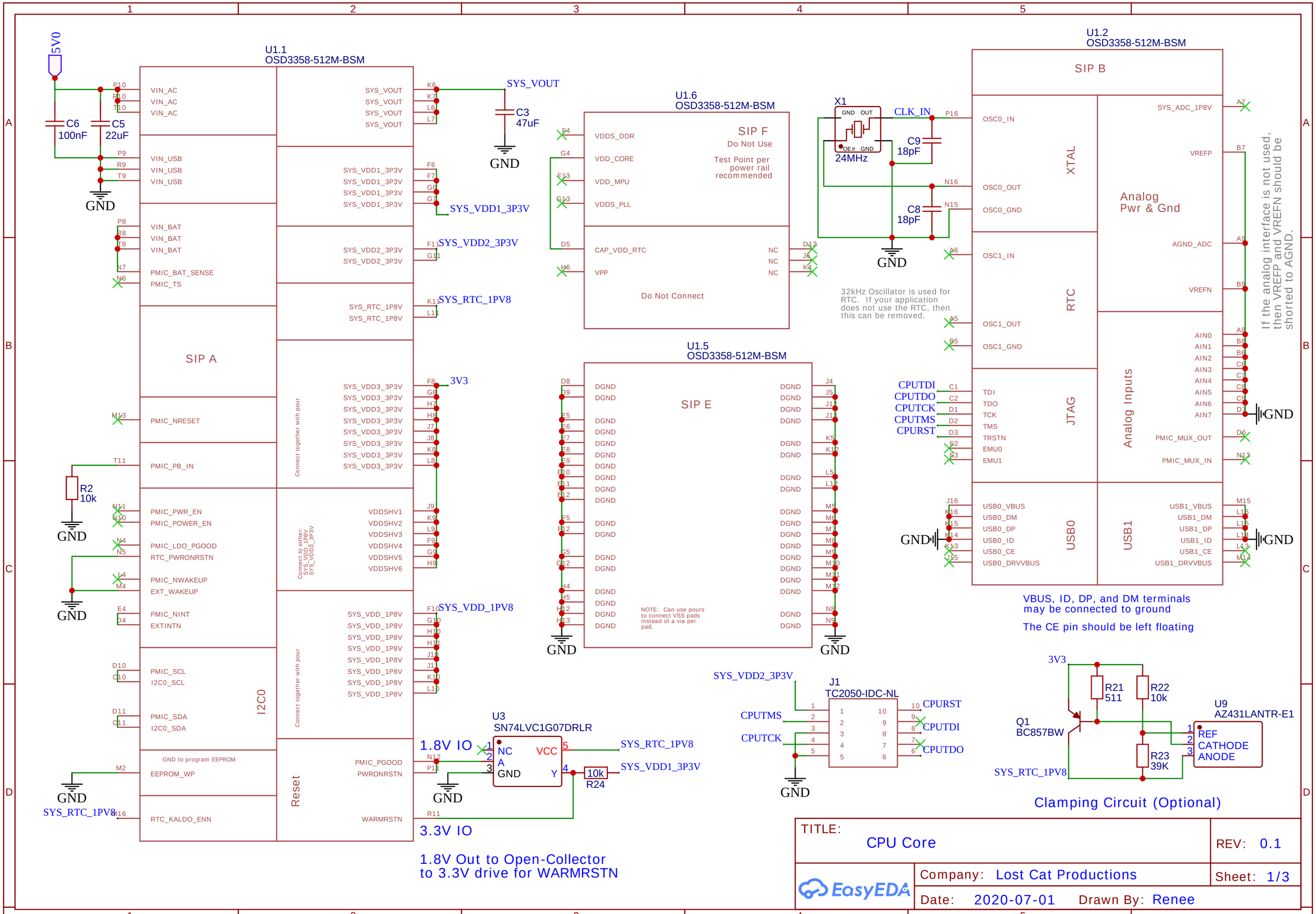
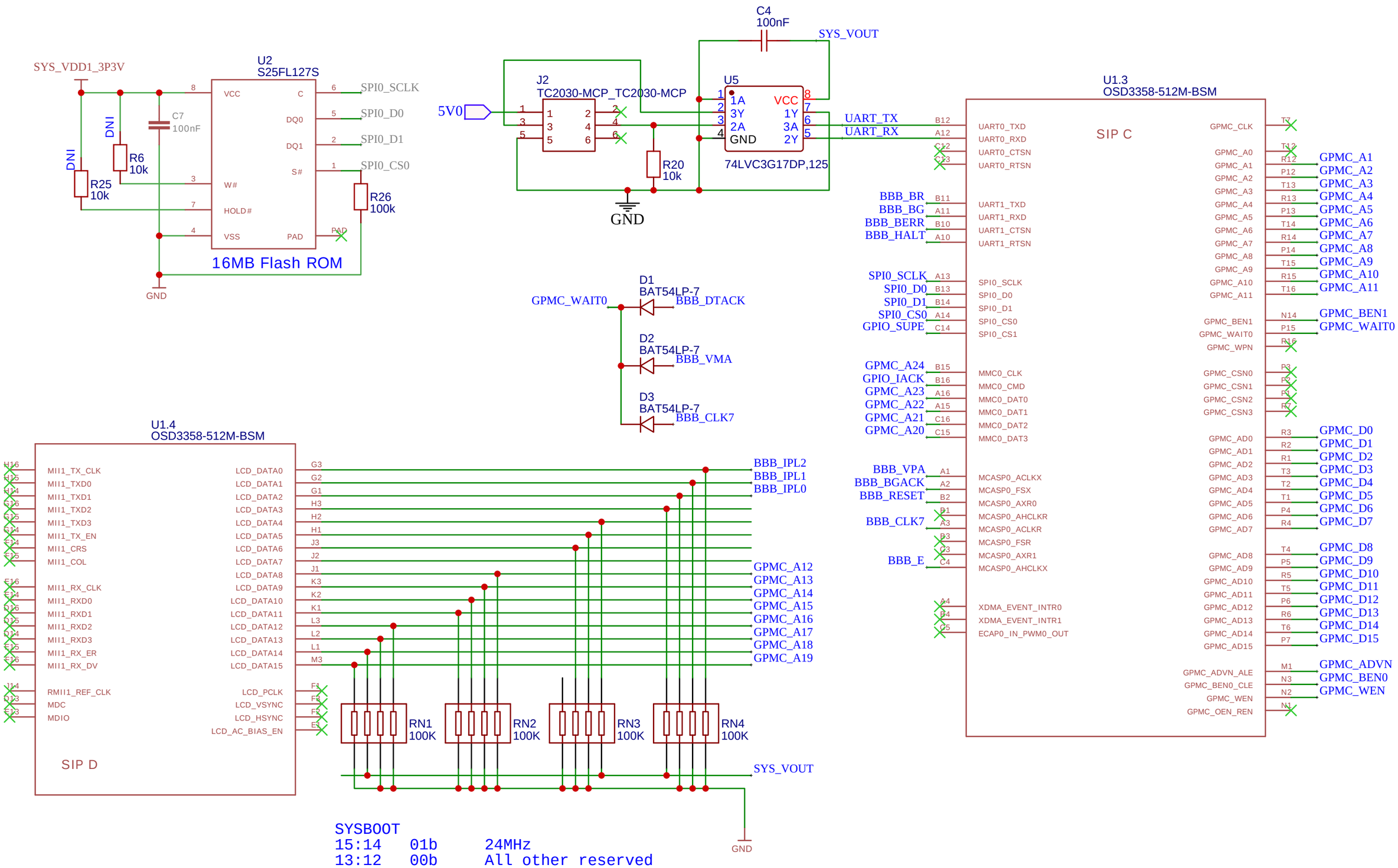

5V0
C6 100nF
C5 22uF
GND
U1.1 OSD3358-512M-BSM
VIN_AC
VIN_USB
VIN_BAT
PMIC_BAT_SENSE
PMIC_TS
SIP A
PMIC_NRESET
PMIC_PB_IN
R2 10k
PMIC_PWR_EN
PMIC_POWER_EN
PMIC_LDO_PGOOD
RTC_PWRONRSTN
PMIC_NWAKEUP
EXT_WAKEUP
PMIC_NINT
EXTINTN
PMIC_SCL
I2C0_SCL
PMIC_SDA
I2C0_SDA
I2C0
GND to program EEPROM
EEPROM_WP
SYS_RTC_1PV8
RTC_KALDO_ENN
SYS_VOUT
C3 47uF
SYS_VDD1_3P3V
SYS_VDD2_3P3V
SYS_RTC_1PV8
Connect together with pour
3V3
Connect to either: SYS_VDD_1P8V SYS_VDD3_3P3V
VDDSHV1
VDDSHV2
VDDSHV3
VDDSHV4
VDDSHV5
VDDSHV6
SYS_VDD_1PV8
Reset
PMIC_PGOOD
PWRONRSTN
WARMRSTN
U1.6 OSD3358-512M-BSM
SIP F
Do Not Use
Test Point per power rail recommended
VDDS_DDR
VDD_CORE
VDD_MPU
VDDS_PLL
CAP_VDD_RTC
VPP
NC
Do Not Connect
U1.5 OSD3358-512M-BSM
SIP E
DGND
NOTE: Can use pours to connect VSS pads instead of a via per pad.
X1
GND OUT
OE# GND
24MHz
CLK_IN
C9 18pF
C8 18pF
32kHz Oscillator is used for RTC. If your application does not use the RTC, then this can be removed.
U1.2 OSD3358-512M-BSM
SIP B
OSC0_IN
OSC0_OUT
OSC0_GND
XTAL
OSC1_IN
OSC1_OUT
OSC1_GND
RTC
TDI
TDO
TCK
TMS
TRSTN
EMU0
EMU1
JTAG
CPUTDI
CPUTDO
CPUTCK
CPUTMS
CPURST
USB0_VBUS
USB0_DM
USB0_DP
USB0_ID
USB0_CE
USB0_DRVVBUS
USB0
USB1_VBUS
USB1_DM
USB1_DP
USB1_ID
USB1_CE
USB1_DRVVBUS
USB1
SYS_ADC_1P8V
VREFP
Analog Pwr & Gnd
AGND_ADC
VREFN
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
Analog Inputs
PMIC_MUX_OUT
PMIC_MUX_IN
If the analog interface is not used, then VREFP and VREFN should be shorted to AGND.
VBUS, ID, DP, and DM terminals may be connected to ground
The CE pin should be left floating
U3 SN74LVC1G07DRLR
NC
A
GND
VCC
Y
1.8V IO
3.3V IO
10k R24
SYS_RTC_1PV8
SYS_VDD1_3P3V
1.8V Out to Open-Collector to 3.3V drive for WARMRSTN
J1 TC2050-IDC-NL
SYS_VDD2_3P3V
CPUTMS
CPUTCK
CPURST
CPUTDI
CPUTDO
3V3
R21 511
R22 10k
R23 39K
Q1 BC857BW
U9 AZ431LANTR-E1
REF
CATHODE
ANODE
Clamping Circuit (Optional)
TITLE:
CPU Core
REV: 0.1
Company: Lost Cat Productions
Sheet: 1/3
Date: 2020-07-01
Drawn By: Renee
EasyEDA

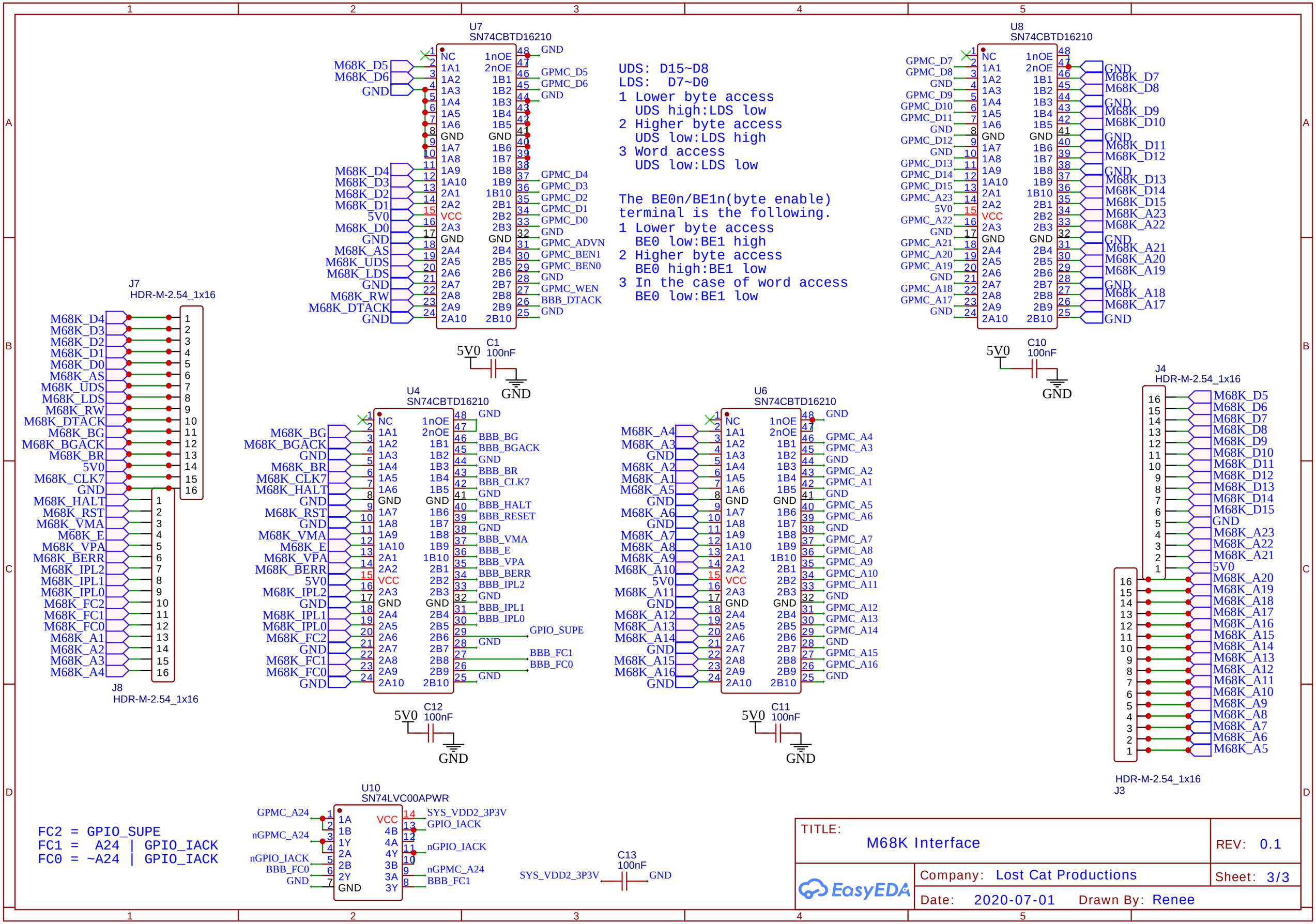


SYSBOOT

15:14	01b	24MHz
13:12	00b	All other reserved
11:10	00b	Don't care for ROM code
9	0	Don't care for ROM code
8	0	Don't care for ROM code
7:6	00	MII EMAC
5	0	CLKOUT1 disabled
4:0	11000b	Boot order: SPI0->MMC0->USB0->UART0

TITLE: CPU Interface	REV: 0.1
Company: Lost Cat Productions	Sheet: 2/3
Date: 2020-08-06 Drawn By: Renee	

EasyEDA


U7
SN74CBTD16210
U8
SN74CBTD16210
U4
SN74CBTD16210
U6
SN74CBTD16210
U10
SN74LVC00APWR
J7
HDR-M-2.54_1x16
J8
HDR-M-2.54_1x16
J4
HDR-M-2.54_1x16
J3
HDR-M-2.54_1x16
C1 100nF
C10 100nF
C12 100nF
C11 100nF
C13 100nF
5V0
GND
UDS: D15~D8
LDS: D7~D0
1 Lower byte access
UDS high:LDS low
2 Higher byte access
UDS low:LDS high
3 Word access
UDS low:LDS low
The BE0n/BE1n(byte enable)
terminal is the following.
1 Lower byte access
BE0 low:BE1 high
2 Higher byte access
BE0 high:BE1 low
3 In the case of word access
BE0 low:BE1 low
FC2 = GPIO_SUPE
FC1 = A24 | GPIO_IACK
FC0 = ~A24 | GPIO_IACK
TITLE:
M68K Interface
REV: 0.1
Company: Lost Cat Productions
Sheet: 3/3
Date: 2020-07-01
Drawn By: Renee
EasyEDA

GPMC_A24