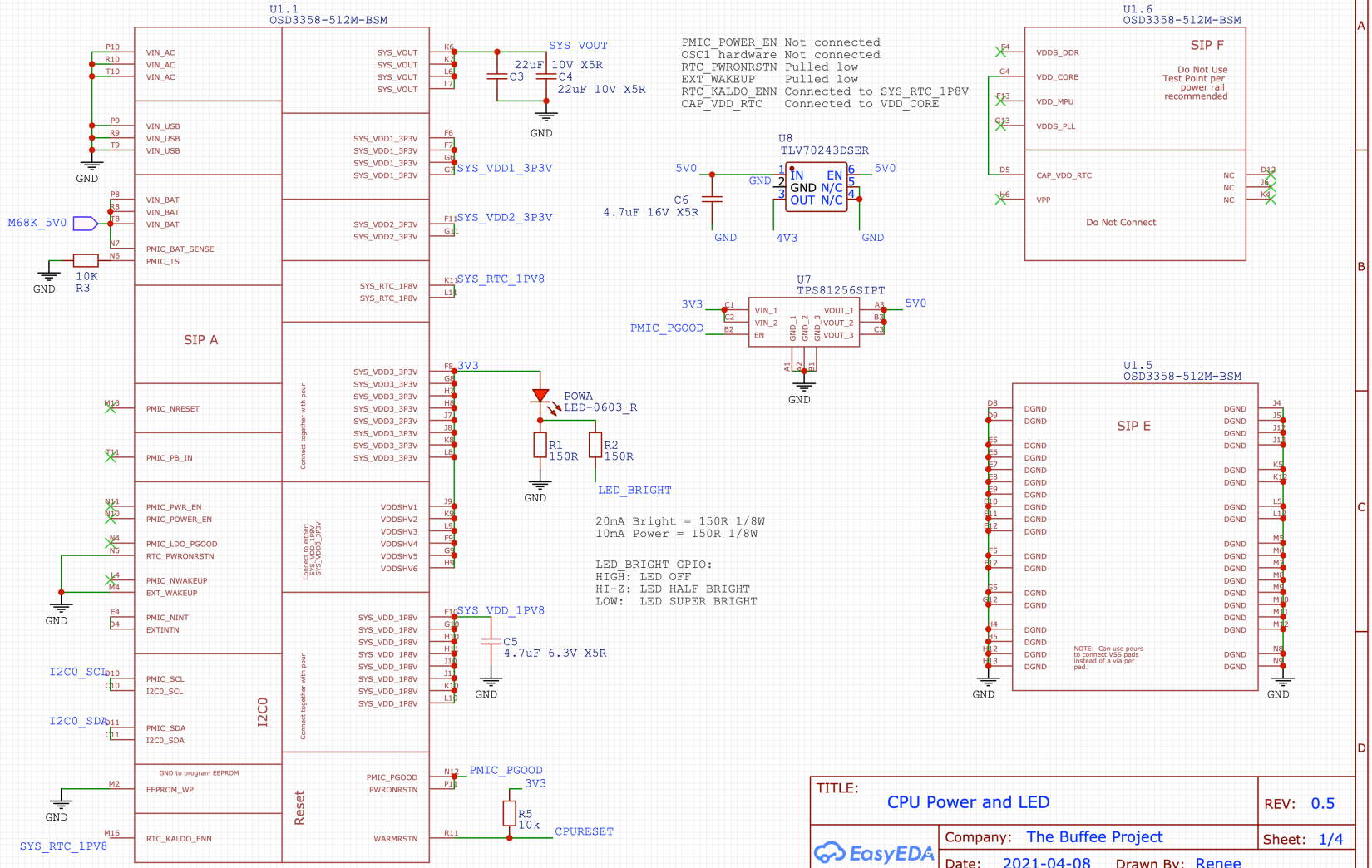
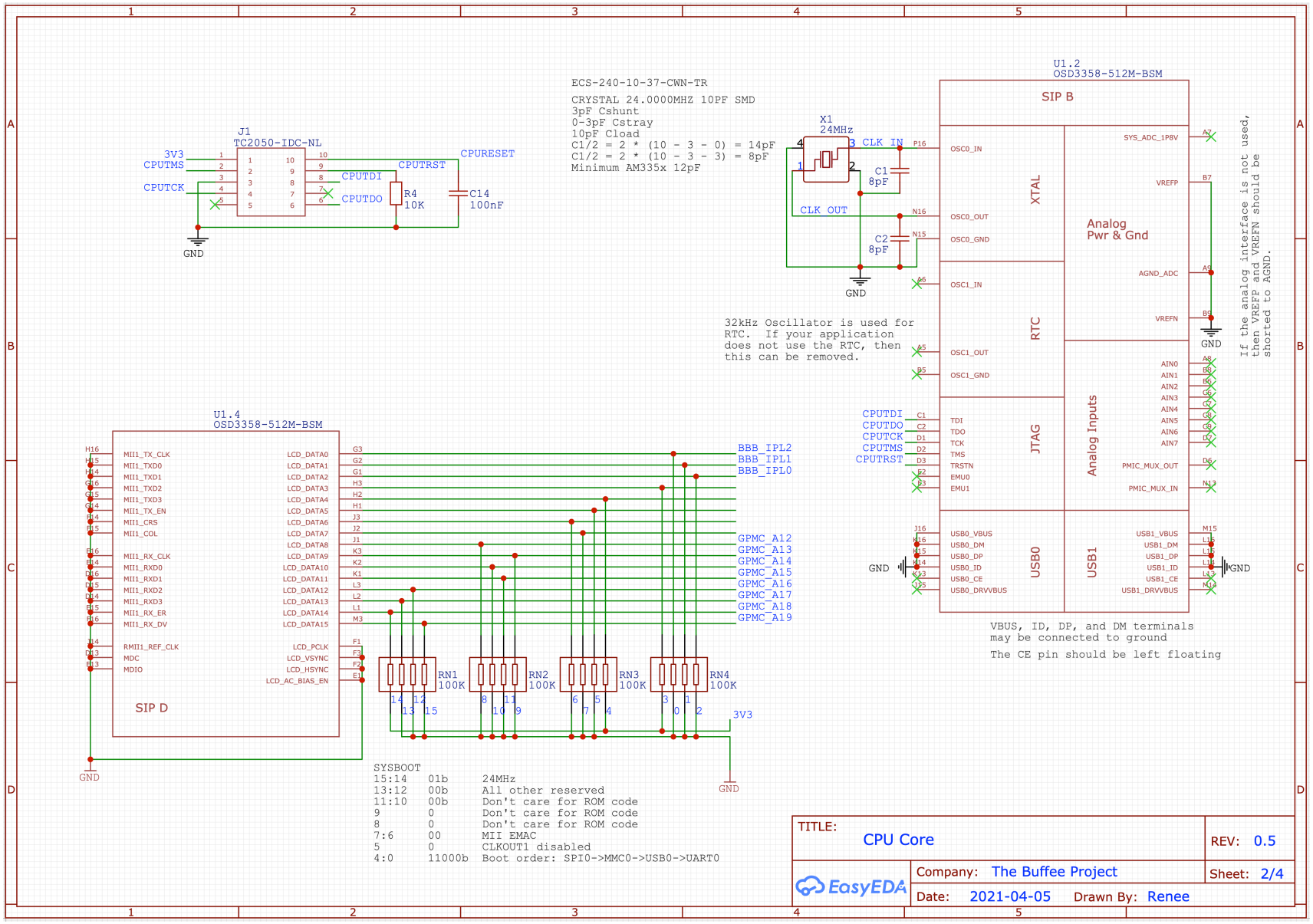
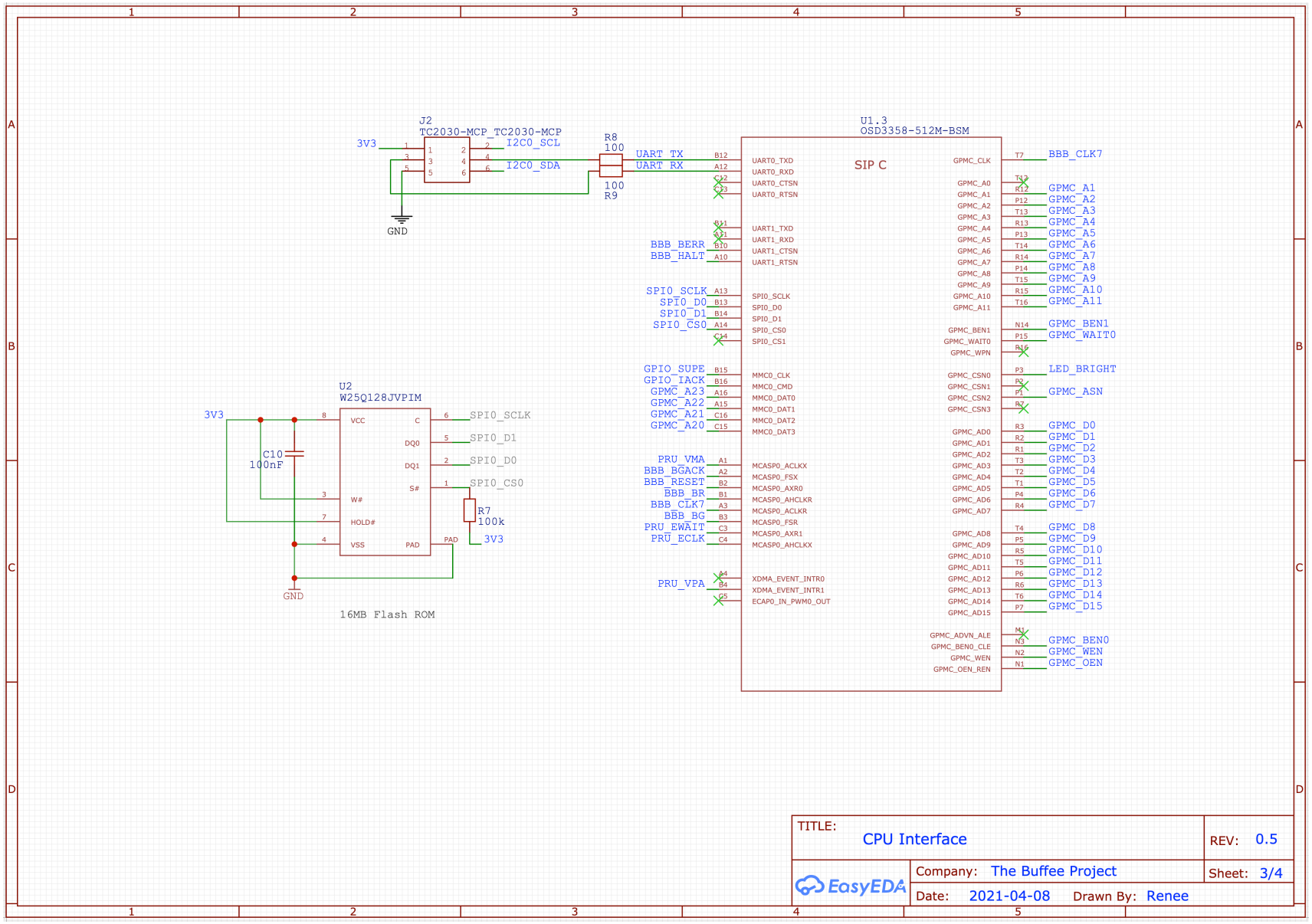
A nonportable system operates on a regulated 5-V supply that does not require input overvoltage protection. In this case, the 5-V power supply is connected through the BAT pins. The DC/DC converter inputs, WLED driver, LDO1, and LDO2 are connected directly to the 5-V supply. A standard, constant-value 10-kΩ resistor is connected from the TS pin to ground to simulate the NTC thermistor monitoring the battery. The load switches (or LDO3 and LDO4, depending on configuration) typically connect to one of the lower system rails, but can also be connected directly to the 5-V input supply.



TITLE: CPU Power and LED	REV: 0.5
Company: The Buffee Project	Sheet: 1/4
Date: 2021-04-08 Drawn By: Renee	

EasyEDA


J1
TC2050-IDC-NL
3V3
CPUTMS
CPUTCK
CPUTDI
CPUTDO
CPUTRST
CPURESET
R4
10K
C14
100nF
GND
ECS-240-10-37-CWN-TR
CRYSTAL 24.0000MHZ 10PF SMD
3pF Cshunt
0-3pF Cstray
10pF Cload
C1/2 = 2 * (10 - 3 - 0) = 14pF
C1/2 = 2 * (10 - 3 - 3) = 8pF
Minimum AM335x 12pF
X1
24MHz
CLK IN
CLK OUT
C1
8pF
C2
8pF
U1.2
OSD3358-512M-BSM
SIP B
XTAL
RTC
JTAG
USB0
Analog Pwr & Gnd
Analog Inputs
USB1
32kHz Oscillator is used for RTC. If your application does not use the RTC, then this can be removed.
If the analog interface is not used, then VREFP and VREFN should be shorted to AGND.
VBUS, ID, DP, and DM terminals may be connected to ground
The CE pin should be left floating
U1.4
OSD3358-512M-BSM
SIP D
BBB_IPL2
BBB_IPL1
BBB_IPL0
GPMC_A12
GPMC_A13
GPMC_A14
GPMC_A15
GPMC_A16
GPMC_A17
GPMC_A18
GPMC_A19
RN1
100K
RN2
100K
RN3
100K
RN4
100K
SYSBOOT
15:14 01b 24MHz
13:12 00b All other reserved
11:10 00b Don't care for ROM code
9 0 Don't care for ROM code
8 0 Don't care for ROM code
7:6 00 MII EMAC
5 0 CLKOUT1 disabled
4:0 11000b Boot order: SPI0->MMC0->USB0->UART0
TITLE:
CPU Core
REV: 0.5
Company: The Buffee Project
Sheet: 2/4
Date: 2021-04-05
Drawn By: Renee
EasyEDA



TITLE: CPU Interface		REV: 0.5
EasyEDA	Company: The Buffee Project	Sheet: 3/4
	Date: 2021-04-08 Drawn By: Renee	

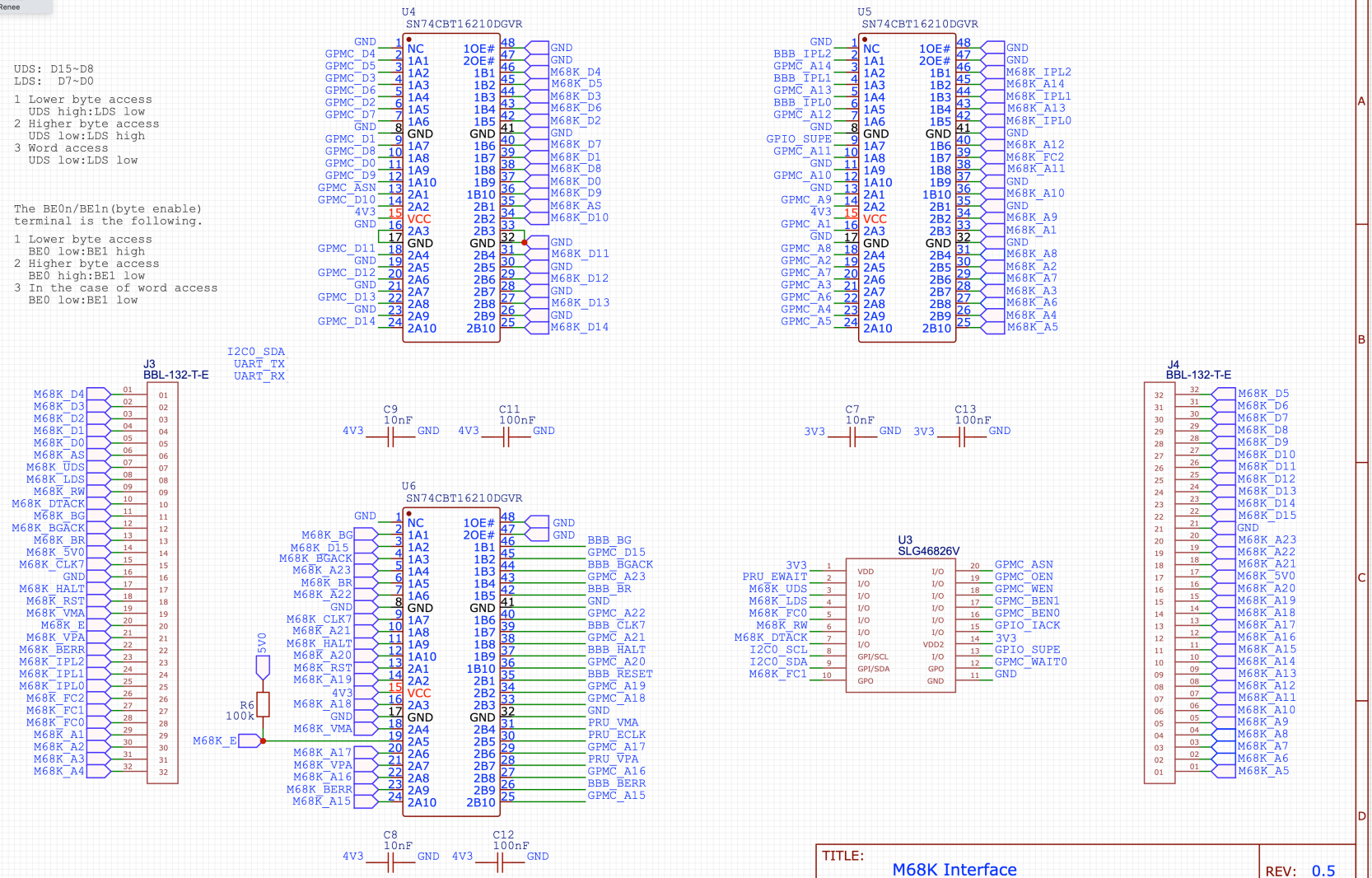
Title: Amiga-SMD500
Version: master
Owner: Renee

UDS: D15~D8
LDS: D7~D0

1 Lower byte access
UDS high:LDS low
2 Higher byte access
UDS low:LDS high
3 Word access
UDS low:LDS low

The BE0n/BE1n(byte enable) terminal is the following.

1 Lower byte access
BE0 low:BE1 high
2 Higher byte access
BE0 high:BE1 low
3 In the case of word access
BE0 low:BE1 low



TITLE: M68K Interface		REV: 0.5
EasyEDA	Company: The Buffee Project	Sheet: 4/4
	Date: 2021-04-08 Drawn By: Renee	