CPU Core

5V0

U1.1 OSD3358-512M-BSM

SIP A

Pin	Signal
P10 / R10 / T10	VIN_AC
P9 / R9 / T9	VIN_USB
P8 / R8 / T8	VIN_BAT
N7	PMIC_BAT_SENSE
N6	PMIC_TS
M13	PMIC_NRESET
T11	PMIC_PB_IN
N11	PMIC_PWR_EN
K9	PMIC_POWER_EN
N4	PMIC_LDO_PGOOD
N5	RTC_PWRONRSTN
J4	PMIC_NWAKEUP
M4	EXT_WAKEUP
E4	PMIC_NINT
D4	EXTINTN
D10	PMIC_SCL
G10	I2C0_SCL
D11	PMIC_SDA
G11	I2C0_SDA
M2	EEPROM_WP
R16	RTC_KALDO_ENN

GND to program EEPROM
I2C0
Reset

Pin	Signal
K6 / K7 / L6 / L7	SYS_VOUT
F6 / F7 / G6 / G7	SYS_VDD1_3P3V
F11 / G11	SYS_VDD2_3P3V
K11 / L11	SYS_RTC_1P8V
F8 / G8 / H7 / H8 / J7 / J8 / K8 / L8	SYS_VDD3_3P3V
J9 / K9 / L9 / F9 / G9 / H9	VDDSHV1 / VDDSHV2 / VDDSHV3 / VDDSHV4 / VDDSHV5 / VDDSHV6
F10 / G10 / H10 / H11 / H12 / J10 / J11 / K10 / L10	SYS_VDD_1P8V
N12	PMIC_PGOOD
P12	PWRONRSTN
R11	WARMRSTN

Connect together with pour
Connect to either: SYS_VDD_1P8V SYS_VDD3_3P3V

3V3
SYS_VOUT

C6 100nF   C5 22uF   C3 47uF
GND

R2 10k

U1.6 OSD3358-512M-BSM

SIP F — Do Not Use
Test Point per power rail recommended

Pin	Signal
F4	VDDS_DDR
G4	VDD_CORE
F13	VDD_MPU
G13	VDDS_PLL
D5	CAP_VDD_RTC
H6	VPP
D12 / J4 / K4	NC

Do Not Connect

U1.5 OSD3358-512M-BSM

SIP E — DGND (all pins)

NOTE: Can use pours to connect VSS pads instead of a via per pad.

GND

If the analog interface is not used, then VREFP and VREFN should be shorted to AGND.

X1 24MHz
GND OUT / OE# GND

CLK_IN

C9 18pF   C8 18pF
GND

U1.2 OSD3358-512M-BSM

SIP B

Pin	Signal
P16	OSC0_IN
N16	OSC0_OUT
N15	OSC0_GND
A6	OSC1_IN
A5	OSC1_OUT
B5	OSC1_GND
C1	TDI
C2	TDO
D1	TCK
D2	TMS
D3	TRSTN
E2	EMU0
E3	EMU1
J16	USB0_VBUS
K16	USB0_DM
J15	USB0_DP
H14	USB0_ID
K15	USB0_CE
J15	USB0_DRVVBUS

XTAL / RTC / JTAG / USB0 / USB1 / Analog Inputs / Analog Pwr & Gnd

Pin	Signal
A7	SYS_ADC_1P8V
B7	VREFP
A5	AGND_ADC
B9	VREFN
AIN0 – AIN7	Analog Inputs
D6	PMIC_MUX_OUT
N13	PMIC_MUX_IN
M15	USB1_VBUS
L15	USB1_DM
L16	USB1_DP
L14	USB1_ID
L13	USB1_CE
M14	USB1_DRVVBUS

CPUTDI / CPUTDO / CPUTCK / CPUTMS / CPURST

GND

32kHz Oscillator is used for RTC. If your application does not use the RTC, then this can be removed.

VBUS, ID, DP, and DM terminals may be connected to ground

The CE pin should be left floating

U3 SN74LVC1G07DRLR
1.8V IO — NC / A / GND — VCC / Y
SYS_RTC_1PV8   SYS_VDD1_3P3V
10k R24   R11
GND

3.3V IO
1.8V Out to Open-Collector to 3.3V drive for WARMRSTN

J1 TC2050-IDC-NL
SYS_VDD2_3P3V
CPUTMS / CPUTCK
CPURST / CPUTDI / CPUTDO
GND

Clamping Circuit (Optional)
3V3
R21 511   R22 10k
Q1 BC857BW
U9 AZ431LANTR-E1 — REF / CATHODE / ANODE
R23 39K
SYS_RTC_1PV8

SYS_RTC_1PV8

U2
S25FL127S
16MB Flash ROM

SYS_VDD1_3P3V

C7 100nF
DNI
DNI
R6 10k
R25 10k
R26 100k

VCC 8
C 6 — SPI0_SCLK
DQ0 5 — SPI0_D0
DQ1 2 — SPI0_D1
W# 3
S# 1 — SPI0_CS0
HOLD# 7
VSS 4
PAD

GND

J2
TC2030-MCP_TC2030-MCP

5V0

C4 100nF
SYS_VOUT

U5
1A 1 / VCC 8
3Y 2
2A 3 / 1Y 7
GND 4 / 3A 6
2Y 5
74LVC3G17DP,125

R20 10k

GND

UART_TX
UART_RX

U1.3
OSD3358-512M-BSM
SIP C

UART0_TXD B12
UART0_RXD A12
UART0_CTSN C12
UART0_RTSN C13

BBB_BR B11 — UART1_TXD
BBB_BG A11 — UART1_RXD
BBB_BERR B10 — UART1_CTSN
BBB_HALT A10 — UART1_RTSN

SPI0_SCLK A13 — SPI0_SCLK
SPI0_D0 B13 — SPI0_D0
SPI0_D1 B14 — SPI0_D1
SPI0_CS0 A14 — SPI0_CS0
GPIO_SUPE C14 — SPI0_CS1

GPMC_A24 B15 — MMC0_CLK
GPIO_IACK B16 — MMC0_CMD
GPMC_A23 A16 — MMC0_DAT0
GPMC_A22 A15 — MMC0_DAT1
GPMC_A21 C16 — MMC0_DAT2
GPMC_A20 C15 — MMC0_DAT3

BBB_VPA A1 — MCASP0_ACLKX
BBB_BGACK A2 — MCASP0_FSX
BBB_RESET B2 — MCASP0_AXR0
MCASP0_AHCLKR
BBB_CLK7 B1 — MCASP0_ACLKR
A3 — MCASP0_FSR
B3 — MCASP0_AXR1
BBB_E C4 — MCASP0_AHCLKX

XDMA_EVENT_INTR0
XDMA_EVENT_INTR1
ECAP0_IN_PWM0_OUT

GPMC_CLK T7
GPMC_A0 T12
GPMC_A1 R12 — GPMC_A1
GPMC_A2 P12 — GPMC_A2
GPMC_A3 T13 — GPMC_A3
GPMC_A4 R13 — GPMC_A4
GPMC_A5 P13 — GPMC_A5
GPMC_A6 T14 — GPMC_A6
GPMC_A7 R14 — GPMC_A7
GPMC_A8 P14 — GPMC_A8
GPMC_A9 T15 — GPMC_A9
GPMC_A10 R15 — GPMC_A10
GPMC_A11 T16 — GPMC_A11

GPMC_BEN1 N14 — GPMC_BEN1
GPMC_WAIT0 P15 — GPMC_WAIT0
GPMC_WPN R16

GPMC_CSN0
GPMC_CSN1
GPMC_CSN2
GPMC_CSN3

GPMC_AD0 R3 — GPMC_D0
GPMC_AD1 R2 — GPMC_D1
GPMC_AD2 R1 — GPMC_D2
GPMC_AD3 T3 — GPMC_D3
GPMC_AD4 T2 — GPMC_D4
GPMC_AD5 T1 — GPMC_D5
GPMC_AD6 P4 — GPMC_D6
GPMC_AD7 R4 — GPMC_D7
GPMC_AD8 T4 — GPMC_D8
GPMC_AD9 P5 — GPMC_D9
GPMC_AD10 R5 — GPMC_D10
GPMC_AD11 T5 — GPMC_D11
GPMC_AD12 P6 — GPMC_D12
GPMC_AD13 R6 — GPMC_D13
GPMC_AD14 T6 — GPMC_D14
GPMC_AD15 P7 — GPMC_D15

GPMC_ADVN_ALE M1 — GPMC_ADVN
GPMC_BEN0_CLE N3 — GPMC_BEN0
GPMC_WEN N2 — GPMC_WEN
GPMC_OEN_REN N1

D1 BAT54LP-7
GPMC_WAIT0 — BBB_DTACK

D2 BAT54LP-7
— BBB_VMA

D3 BAT54LP-7
— BBB_CLK7

U1.4
OSD3358-512M-BSM
SIP D

MII1_TX_CLK H16
MII1_TXD0 G15
MII1_TXD1 H14
MII1_TXD2 G16
MII1_TXD3 H15
MII1_TX_EN G14
MII1_CRS J15
MII1_COL J16

MII1_RX_CLK F16
MII1_RXD0 G13
MII1_RXD1 D15
MII1_RXD2 D14
MII1_RXD3 E15
MII1_RX_ER E16
MII1_RX_DV F16

RMII1_REF_CLK J14
MDC J13
MDIO E13

LCD_DATA0 G3
LCD_DATA1 G2
LCD_DATA2 G1
LCD_DATA3 H3
LCD_DATA4 H2
LCD_DATA5 H1
LCD_DATA6 J3
LCD_DATA7 J2
LCD_DATA8 J1
LCD_DATA9 K3
LCD_DATA10 K2
LCD_DATA11 K1
LCD_DATA12 L3
LCD_DATA13 L2
LCD_DATA14 L1
LCD_DATA15 M3

LCD_PCLK E2
LCD_VSYNC F3
LCD_HSYNC F1
LCD_AC_BIAS_EN E3

BBB_IPL2
BBB_IPL1
BBB_IPL0

GPMC_A12
GPMC_A13
GPMC_A14
GPMC_A15
GPMC_A16
GPMC_A17
GPMC_A18
GPMC_A19

RN1 100K
RN2 100K
RN3 100K
RN4 100K

SYS_VOUT

GND

SYSBOOT
15:14   01b   24MHz
13:12   00b   All other reserved
11:10   00b   Don't care for ROM code
9   0   Don't care for ROM code
8   0   Don't care for ROM code
7:6   00   MII EMAC
5   0   CLKOUT1 disabled
4:0   11000b Boot order: SPI0->MMC0->USB0->UART0

TITLE: CPU Interface
REV: 0.1
Company: Lost Cat Productions
Sheet: 2/3
Date: 2020-08-06   Drawn By: Renee
EasyEDA

UDS: D15~D8
LDS: D7~D0
1 Lower byte access
   UDS high:LDS low
2 Higher byte access
   UDS low:LDS high
3 Word access
   UDS low:LDS low

The BE0n/BE1n(byte enable) terminal is the following output.
1 Lower byte access
   BE0 low:BE1 high
2 Higher byte access
   BE0 high:BE1 low
3 In the case of word access
   BE0 low:BE1 low

U7 — SN74CBTD16210

Pin	Signal		Signal
1	NC	1nOE	GND
2	M68K_D5 → 1A1	2nOE	
3	M68K_D6 → 1A2	1B1	GPMC_D5
4	GND → 1A3	1B2	GPMC_D6
5	1A4	1B3	GND
6	1A5	1B4	
7	1A6	1B5	
8	GND	GND	
9	1A7	1B6	
10	1A8	1B7	
11	M68K_D4 → 1A9	1B8	GPMC_D4
12	M68K_D3 → 1A10	1B9	GPMC_D3
13	M68K_D2 → 2A1	1B10	GPMC_D2
14	M68K_D1 → 2A2	2B1	GPMC_D1
15	5V0 → VCC	2B2	GPMC_D0
16	M68K_D0 → 2A3	2B3	GND
17	GND	GND	
18	M68K_AS → 2A4	2B4	GPMC_ADVN
19	M68K_UDS → 2A5	2B5	GPMC_BEN1
20	M68K_LDS → 2A6	2B6	GPMC_BEN0
21	GND → 2A7	2B7	GND
22	M68K_RW → 2A8	2B8	GPMC_WEN
23	M68K_DTACK → 2A9	2B9	BBB_DTACK
24	GND → 2A10	2B10	GND

5V0 C1 100nF GND

U8 — SN74CBTD16210

Pin	Signal		Signal
1	NC	1nOE	GND
2	GPMC_D7 → 1A1	2nOE	GND
3	GPMC_D8 → 1A2	1B1	M68K_D7
4	GPMC_D9 → 1A3	1B2	M68K_D8
5	GPMC_D10 → 1A4	1B3	GND
6	GPMC_D11 → 1A5	1B4	M68K_D9
7	GND → 1A6	1B5	M68K_D10
8	GND	GND	
9	GPMC_D12 → 1A7	1B6	GND
10	GND → 1A8	1B7	M68K_D11
11	GPMC_D13 → 1A9	1B8	M68K_D12
12	GPMC_D14 → 1A10	1B9	M68K_D13
13	GPMC_D15 → 2A1	1B10	M68K_D14
14	GPMC_A23 → 2A2	2B1	M68K_D15
15	5V0 → VCC	2B2	M68K_A23
16	GPMC_A22 → 2A3	2B3	M68K_A22
17	GND	GND	
18	GPMC_A21 → 2A4	2B4	GND
19	GPMC_A20 → 2A5	2B5	M68K_A21
20	GPMC_A19 → 2A6	2B6	M68K_A20
21	GPMC_A18 → 2A7	2B7	M68K_A19
22	GPMC_A17 → 2A8	2B8	GND
23	2A9	2B9	M68K_A18
24	GND → 2A10	2B10	M68K_A17
			GND

5V0 C10 100nF GND

J7 — HDR-M-2.54_1x16

Pin	Signal
1	M68K_D4
2	M68K_D3
3	M68K_D2
4	M68K_D1
5	M68K_D0
6	M68K_AS
7	M68K_UDS
8	M68K_LDS
9	M68K_RW
10	M68K_DTACK
11	M68K_BG
12	M68K_BGACK
13	M68K_BR
14	5V0
15	M68K_CLK7
16	GND

J8 — HDR-M-2.54_1x16

Pin	Signal
1	M68K_HALT
2	M68K_RST
3	M68K_VMA
4	M68K_E
5	M68K_VPA
6	M68K_BERR
7	M68K_IPL2
8	M68K_IPL1
9	M68K_IPL0
10	M68K_FC2
11	M68K_FC1
12	M68K_FC0
13	M68K_A1
14	M68K_A2
15	M68K_A3
16	M68K_A4

U4 — SN74CBTD16210

Pin	Signal		Signal
1	NC	1nOE	GND
2	M68K_BG → 1A1	2nOE	
3	M68K_BGACK → 1A2	1B1	BBB_BG
4	GND → 1A3	1B2	BBB_BGACK
5	M68K_BR → 1A4	1B3	GND
6	M68K_CLK7 → 1A5	1B4	BBB_BR
7	M68K_HALT → 1A6	1B5	BBB_CLK7
8	GND	GND	
9	GND	GND	GND
10	M68K_RST → 1A7	1B6	BBB_HALT
11	GND → 1A8	1B7	BBB_RESET
12	M68K_VMA → 1A9	1B8	BBB_VMA
13	M68K_E → 1A10	1B9	BBB_E
14	M68K_VPA → 2A1	1B10	BBB_VPA
15	M68K_BERR → 2A2	2B1	BBB_BERR
16	5V0 → VCC	2B2	BBB_IPL2
17	M68K_IPL2 → 2A3	2B3	GND
18	GND	GND	
19	M68K_IPL1 → 2A4	2B4	BBB_IPL1
20	M68K_IPL0 → 2A5	2B5	BBB_IPL0
21	M68K_FC2 → 2A6	2B6	GPIO_SUPE
22	GND → 2A7	2B7	GND
23	M68K_FC1 → 2A8	2B8	BBB_FC1
24	M68K_FC0 → 2A9	2B9	BBB_FC0
	GND → 2A10	2B10	

5V0 C12 100nF GND

U6 — SN74CBTD16210

Pin	Signal		Signal
1	NC	1nOE	GND
2	M68K_A4 → 1A1	2nOE	GPMC_A4
3	M68K_A3 → 1A2	1B1	GPMC_A3
4	GND → 1A3	1B2	GND
5	M68K_A2 → 1A4	1B3	GPMC_A2
6	M68K_A1 → 1A5	1B4	GPMC_A1
7	M68K_A5 → 1A6	1B5	GND
8	GND	GND	
9	GND → 1A7	1B6	GPMC_A5
10	M68K_A6 → 1A8	1B7	GND
11	GND → 1A9	1B8	GPMC_A6
12	M68K_A7 → 1A10	1B9	GPMC_A7
13	M68K_A8 → 2A1	1B10	GPMC_A8
14	M68K_A9 → 2A2	2B1	GPMC_A9
15	5V0 → VCC	2B2	GPMC_A10
16	M68K_A10 → 2A3	2B3	GPMC_A11
17	GND	GND	GND
18	M68K_A11 → 2A4	2B4	GPMC_A12
19	M68K_A12 → 2A5	2B5	GPMC_A13
20	M68K_A13 → 2A6	2B6	GPMC_A14
21	M68K_A14 → 2A7	2B7	GND
22	GND → 2A8	2B8	GPMC_A15
23	M68K_A15 → 2A9	2B9	GPMC_A16
24	M68K_A16 → 2A10	2B10	GND
	GND		

5V0 C11 100nF GND

J4 — HDR-M-2.54_1x16

Pin	Signal
16	M68K_D5
15	M68K_D6
14	M68K_D7
13	M68K_D8
12	M68K_D9
11	M68K_D10
10	M68K_D11
9	M68K_D12
8	M68K_D13
7	M68K_D14
6	M68K_D15
5	GND
4	M68K_A23
3	M68K_A22
2	M68K_A21
1	5V0

J3 — HDR-M-2.54_1x16

Pin	Signal
16	M68K_A20
15	M68K_A19
14	M68K_A18
13	M68K_A17
12	M68K_A16
11	M68K_A15
10	M68K_A14
9	M68K_A13
8	M68K_A12
7	M68K_A11
6	M68K_A10
5	M68K_A9
4	M68K_A8
3	M68K_A7
2	M68K_A6
1	M68K_A5

U10 — SN74LVC00APWR

Pin	Signal		Signal
1	GPMC_A24 → 1A	VCC	SYS_VDD2_3P3V
2	nGPMC_A24 → 1B	4B	GPIO_IACK
3	1Y	4A	
4	2A	4Y	nGPIO_IACK
5	nGPIO_IACK → 2B	3B	nGPMC_A24
6	BBB_FC0 → 2Y	3A	BBB_FC1
7	GND	3Y	

C13 100nF
SYS_VDD2_3P3V — GND

FC2 = GPIO_SUPE
FC1 = A24 | GPIO_IACK
FC0 = ~A24 | GPIO_IACK

GPMC_A24