GigaDevice Semiconductor Inc.

GD32VF103 RISC-V 32-bit MCU

Datasheet



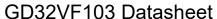
Table of Contents

Та	ble c	of Contents	1
Li	st of	Figures	4
Li	st of	Tables	5
1.	Gei	neral descriptionn	7
2.		· vice overview	
	2.1.	Device information	
	2.2.	Block diagram	
	2.3.	Pinouts and pin assignment	
	2.4.	Memory map	
	2.5.	Clock tree	
	2.6.	Pin definitions	
	2.6.	·	
	2.6.2		
	2.6.3	•	
	2.6.		
3.	Fur	nctional description	37
,	3.1.	System and memory architecture	37
;	3.2.	On-chip memory	37
,	3.3.	Clock, reset and supply management	37
į	3.4.	Boot modes	38
,	3.5.	Power saving modes	39
;	3.6.	Analog to digital converter (ADC)	39
,	3.7.	Digital to analog converter (DAC)	40
,	3.8.	DMA	40
,	3.9.	General-purpose inputs/outputs (GPIOs)	40
	3.10.	Timers and PWM generation	41
;	3.11.	Real time clock (RTC)	42
,	3.12.	Inter-integrated circuit (I2C)	42
;	3.13.	Serial peripheral interface (SPI)	44
;	3.14.	Universal synchronous asynchronous receiver transmitter (USART)	44



GigaDevice

_		1.4.10	
	3.15.	Inter-IC sound (I2S)	
	3.16.	Universal serial bus full-speed (USBFS)	
	3.17.	Controller area network (CAN)	
	3.18.	External memory controller (EXMC)	45
	3.19.	Debug mode	45
	3.20.	Package and operation temperature	46
4	. Ele	ctrical characteristics	47
	4.1.	Absolute maximum ratings	47
	4.2.	Operating conditions characteristics	47
	4.3.	Power consumption	49
	4.4.	EMC characteristics	53
	4.5.	Power supply supervisor characteristics	54
	4.6.	Electrical sensitivity	55
	4.7.	External clock characteristics	55
	4.8.	Internal clock characteristics	57
	4.9.	PLL characteristics	58
	4.10.	Memory characteristics	59
	4.11.	NRST pin characteristics	59
	4.12.	GPIO characteristics	60
	4.13.	ADC characteristics	62
	4.14.	Temperature sensor characteristics	63
	4.15.	DAC characteristics	63
	4.16.	I2C characteristics	64
	4.17.	SPI characteristics	65
	4.18.	I2S characteristics	67
	4.19.	USART characteristics	69
	4.20.	CAN characteristics	69
	4.21.	USBFS characteristics	70
	4.22.	EXMC characteristics	70
	4.23.	TIMER characteristics	71
	4.24.	WDGT characteristics	72





OBOLIT TOO BUILDON
72
73
73
75
77
79
81
83
84



List of Figures

Figure 2-1. GD32VF103 block diagram	10
Figure 2-2. GD32VF103Vx LQFP100 pinouts	11
Figure 2-3. GD32VF103Rx LQFP64 pinouts	12
Figure 2-4. GD32VF103Cx LQFP48 pinouts	13
Figure 2-5. GD32VF103Tx QFN36 pinouts	13
Figure 2-6. GD32VF103 clock tree	18
Figure 4-1. Recommended power supply decoupling capacitors (1)(2)	48
Figure 4-2. Typical supply current consumption in Run mode	53
Figure 4-3. Typical supply current consumption in Sleep mode	53
Figure 4-4. Recommended external NRST pin circuit ⁽¹⁾	60
Figure 4-5. I/O port AC characteristics definition	61
Figure 4-6. I2C bus timing diagram	65
Figure 4-7. SPI timing diagram - master mode	
Figure 4-8. SPI timing diagram - slave mode	
Figure 4-9. I2S timing diagram - master mode	
Figure 4-10. I2S timing diagram - slave mode	69
Figure 4-11. USBFS timings: definition of data signal rise and fall time	70
Figure 5-1. LQFP100 package outline	73
Figure 5-2. LQFP100 recommended footprint	74
Figure 5-3. LQFP64 package outline	
Figure 5-4. LQFP64 recommended footprint	76
Figure 5-5. LQFP48 package outline	
Figure 5-6. LQFP48 recommended footprint	
Figure 5-7. QFN36 package outline	79
Figure 5-8. QFN36 recommended footprint	80



List of Tables

Table 2-1. GD32VF103 devices features and peripheral list (LQFP64, LQFP100)	0
Table 2-2. GD32VF103 devices features and peripheral list (QFN36, LQFP48)	9
Table 2-3. GD32VF103 memory map	14
Table 2-4. GD32VF103Vx LQFP100 pin definitions	19
Table 2-5. GD32VF103Rx LQFP64 pin definitions	26
Table 2-6. GD32VF103Cx LQFP48 pin definitions	30
Table 2-7. GD32VF103Tx QFN36 pin definitions	34
Table 4-1. Absolute maximum ratings ⁽¹⁾⁽⁴⁾	47
Table 4-2. DC operating conditions	47
Table 4-3. Clock frequency ⁽¹⁾	
Table 4-4. Operating conditions at Power up/ Power down ⁽¹⁾	48
Table 4-5. Start-up timings of Operating conditions ⁽¹⁾⁽²⁾⁽³⁾	48
Table 4-6. Power saving mode wakeup timings characteristics ⁽¹⁾⁽²⁾	48
Table 4-7. Power consumption characteristics ⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾	
Table 4-8. EMS characteristics ⁽¹⁾	54
Table 4-9. Power supply supervisor characteristics	54
Table 4-10. ESD characteristics ⁽¹⁾	55
Table 4-11. Static latch-up characteristics ⁽¹⁾	55
Table 4-12. High speed external clock (HXTAL) generated from a crystal/ceramic	55
Table 4-13. High speed external clock characteristics (HXTAL in bypass mode)	56
Table 4-14. Low speed external clock (LXTAL) generated from a crystal/ceramic	
characteristics	56
Table 4-15. Low speed external user clock characteristics (LXTAL in bypass mode)	57
Table 4-16. High speed internal clock (IRC8M) characteristics	57
Table A AT I am an a l'otamal alcal (IDOANIA) al anatoriories	
Table 4-17. Low speed internal clock (IRC40K) characteristics	58
Table 4-17. Low speed internal clock (IRC40K) characteristics	
	58
Table 4-18. PLL characteristics	58 58 59
Table 4-18. PLL characteristics	58 58 59
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics Table 4-22. I/O port DC characteristics	58 58 59 59
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics	58 58 59 59
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics Table 4-22. I/O port DC characteristics	58 58 59 60 61
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics Table 4-22. I/O port DC characteristics ⁽¹⁾⁽³⁾ Table 4-23. I/O port AC characteristics ⁽¹⁾⁽²⁾	58 58 59 60 61
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics Table 4-22. I/O port DC characteristics ⁽¹⁾⁽³⁾ Table 4-23. I/O port AC characteristics ⁽¹⁾⁽²⁾ Table 4-24. ADC characteristics	58 59 60 61 62
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics Table 4-22. I/O port DC characteristics ⁽¹⁾⁽³⁾ Table 4-23. I/O port AC characteristics ⁽¹⁾⁽²⁾ Table 4-24. ADC characteristics Table 4-25. ADC R _{AIN} max for f _{ADC} = 14 MHz ⁽¹⁾	58 59 69 60 61 62 62
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics Table 4-22. I/O port DC characteristics ⁽¹⁾⁽³⁾ Table 4-23. I/O port AC characteristics ⁽¹⁾⁽²⁾ Table 4-24. ADC characteristics Table 4-25. ADC R _{AIN} max for f _{ADC} = 14 MHz ⁽¹⁾ Table 4-26. Temperature sensor characteristics ⁽¹⁾	58 59 60 61 62 63
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics Table 4-22. I/O port DC characteristics ⁽¹⁾⁽³⁾ Table 4-23. I/O port AC characteristics ⁽¹⁾⁽²⁾ Table 4-24. ADC characteristics Table 4-25. ADC R _{AIN} max for f _{ADC} = 14 MHz ⁽¹⁾ Table 4-26. Temperature sensor characteristics ⁽¹⁾ Table 4-27. DAC characteristics Table 4-28. I2C characteristics ⁽¹⁾⁽²⁾ Table 4-29. Standard SPI characteristics ⁽¹⁾	58 59 60 61 62 63 63 64
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics Table 4-22. I/O port DC characteristics ⁽¹⁾⁽³⁾ Table 4-23. I/O port AC characteristics ⁽¹⁾⁽²⁾ Table 4-24. ADC characteristics Table 4-25. ADC R _{AIN} max for f _{ADC} = 14 MHz ⁽¹⁾ Table 4-26. Temperature sensor characteristics ⁽¹⁾ Table 4-27. DAC characteristics Table 4-28. I2C characteristics ⁽¹⁾⁽²⁾	58 59 60 61 62 63 63 64
Table 4-18. PLL characteristics Table 4-19. PLL1/2 characteristics Table 4-20. Flash memory characteristics Table 4-21. NRST pin characteristics Table 4-22. I/O port DC characteristics ⁽¹⁾⁽³⁾ Table 4-23. I/O port AC characteristics ⁽¹⁾⁽²⁾ Table 4-24. ADC characteristics Table 4-25. ADC R _{AIN} max for f _{ADC} = 14 MHz ⁽¹⁾ Table 4-26. Temperature sensor characteristics ⁽¹⁾ Table 4-27. DAC characteristics Table 4-28. I2C characteristics ⁽¹⁾⁽²⁾ Table 4-29. Standard SPI characteristics ⁽¹⁾	58 59 60 61 62 63 63 64 65





Table 4-33. USBFS start up time		
Table 4-35. USBFS electrical characteristics ⁽¹⁾ 70 Table 4-36. Asynchronous multiplexed PSRAM/NOR read timings ⁽¹⁾⁽²⁾⁽³⁾ 70 Table 4-37. Asynchronous multiplexed PSRAM/NOR write timings ⁽¹⁾⁽²⁾⁽³⁾ 71 Table 4-38. TIMER characteristics ⁽¹⁾ 71 Table 4-39. FWDGT min/max timeout period at 40 kHz (IRC40K) ⁽¹⁾ 72 Table 4-40. WWDGT min/max timeout value at 54 MHz (f _{PCLK1}) ⁽¹⁾ 72 Table 5-1. LQFP100 package dimensions 73 Table 5-2. LQFP64 package dimensions 75 Table 5-3. LQFP48 package dimensions 75 Table 5-4. QFN36 package dimensions 75 Table 5-5. Package thermal characteristics ⁽¹⁾ 81 Table 6-1. Part ordering code for GD32VF103xx devices 83	Table 4-33. USBFS start up time	70
Table 4-36. Asynchronous multiplexed PSRAM/NOR read timings ⁽¹⁾⁽²⁾⁽³⁾	Table 4-34. USBFS DC electrical characteristics	70
Table 4-37. Asynchronous multiplexed PSRAM/NOR write timings ⁽¹⁾⁽²⁾⁽³⁾	Table 4-35. USBFS electrical characteristics ⁽¹⁾	70
Table 4-38. TIMER characteristics ⁽¹⁾	Table 4-36. Asynchronous multiplexed PSRAM/NOR read timings ⁽¹⁾⁽²⁾⁽³⁾	70
Table 4-39. FWDGT min/max timeout period at 40 kHz (IRC40K) ⁽¹⁾ 72 Table 4-40. WWDGT min/max timeout value at 54 MHz (f _{PCLK1}) ⁽¹⁾ 72 Table 5-1. LQFP100 package dimensions 73 Table 5-2. LQFP64 package dimensions 75 Table 5-3. LQFP48 package dimensions 77 Table 5-4. QFN36 package dimensions 79 Table 5-5. Package thermal characteristics ⁽¹⁾ 81 Table 6-1. Part ordering code for GD32VF103xx devices 83	Table 4-37. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)	71
Table 4-40. WWDGT min/max timeout value at 54 MHz (f _{PCLK1}) ⁽¹⁾ 72 Table 5-1. LQFP100 package dimensions 73 Table 5-2. LQFP64 package dimensions 75 Table 5-3. LQFP48 package dimensions 77 Table 5-4. QFN36 package dimensions 79 Table 5-5. Package thermal characteristics ⁽¹⁾ 81 Table 6-1. Part ordering code for GD32VF103xx devices 83	Table 4-38. TIMER characteristics ⁽¹⁾	71
Table 5-1. LQFP100 package dimensions73Table 5-2. LQFP64 package dimensions75Table 5-3. LQFP48 package dimensions77Table 5-4. QFN36 package dimensions79Table 5-5. Package thermal characteristics(1)81Table 6-1. Part ordering code for GD32VF103xx devices83	Table 4-39. FWDGT min/max timeout period at 40 kHz (IRC40K) ⁽¹⁾	72
Table 5-2. LQFP64 package dimensions	Table 4-40. WWDGT min/max timeout value at 54 MHz (f _{PCLK1}) ⁽¹⁾	72
Table 5-3. LQFP48 package dimensions	Table 5-1. LQFP100 package dimensions	73
Table 5-4. QFN36 package dimensions		
Table 5-4. QFN36 package dimensions	Table 5-3. LQFP48 package dimensions	77
Table 6-1. Part ordering code for GD32VF103xx devices		
_	Table 5-5. Package thermal characteristics ⁽¹⁾	81
Table 7-1. Revision history	Table 6-1. Part ordering code for GD32VF103xx devices	83
	Table 7-1. Revision history	84



1. General description

The GD32VF103 device is a 32-bit general-purpose microcontroller based on the RISC-V core with best ratio in terms of processing power, reduced power consumption and peripheral set. The RISC-V processor core is tightly coupled with an Enhancement Core-Local Interrupt Controller (ECLIC), SysTick timer and advanced debug support.

The GD32VF103 device incorporates the RISC-V 32-bit processor core operating at 108 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 128 KB on-chip Flash memory and 32 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connect to two APB buses. The devices offer up to two 12-bit ADCs, up to two 12-bit DACs, up to four general 16-bit timers, two basic timers plus a PWM advanced timer, as well as standard and advanced communication interfaces: up to three SPIs, two I2Cs, three USARTs, two UARTs, two I2Ss, two CANs, an USBFS.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32VF103 devices suitable for a wide range of interconnection applications, especially in areas such as industrial control, motor drives, power monitor and alarm systems, consumer and handheld equipment, POS, vehicle GPS, LED display and so on.



2. Device overview

2.1. Device information

Table 2-1. GD32VF103 devices features and peripheral list (LQFP64, LQFP100)

Part Number					VF103		•
		RB	R8	R6	R4	VB	V8
	Code area (KB)	128	64	32	16	128	64
Flash	Data area (KB)	0	0	0	0	0	0
_	Total (KB)	128	64	32	16	128	64
,	SRAM (KB)	32	20	10	6	32	20
	General	4	4	2	2	4	4
	timer(16-bit)	(1-4)	(1-4)	(1-2)	(1-2)	(1-4)	(1-4)
	Advanced	1	1	1	1	1	1
	timer(16-bit)	(0)	(0)	(0)	(0)	(0)	(0)
Timers	SysTick	1	1	1	1	1	1
Ţ	Basic timer(16-	2	2	2	2	2	2
	bit)	(5-6)	(5-6)	(5-6)	(5-6)	(5-6)	(5-6)
	Watchdog	2	2	2	2	2	2
	RTC	1	1	1	1	1	1
	U(S)ART	5	5	2	2	5	5
	I2C	2	2	1	1	2	2
ivity		(0-1)	(0-1)			(0-1)	(0-1)
Connectivity	SPI/I2S	3/2	3/2	1/-	1/-	3/2	3/2
Col	CAN	2	2	2	2	2	2
	USBFS	1	1	1	1	1	1
	GPIO	51	51	51	51	80	80
	EXMC	-	-	-	-	1	1
	EXTI	16	16	16	16	16	16
ပ္	Units	2	2	2	2	2	2
ADC	Channels	16	16	16	16	16	16
	DAC	2	2	2	2	2	2
	Package		LQF	P64		LQF	P100

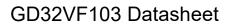




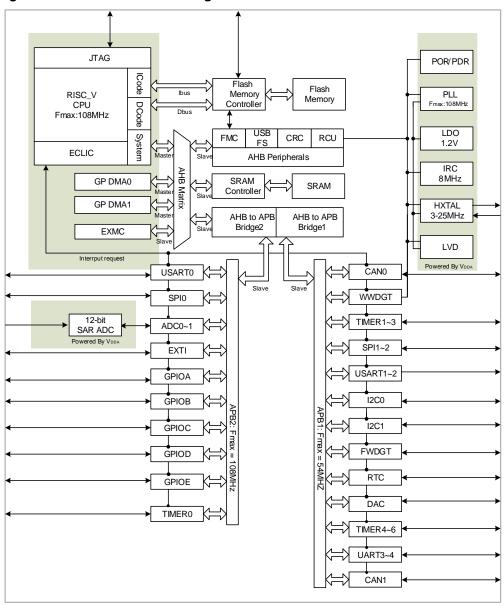
Table 2-2. GD32VF103 devices features and peripheral list (QFN36, LQFP48)

		(F103 devices features and peripheral list (QFN36, LQFP48) GD32VF103							
F	Part Number	ТВ	Т8	Т6	T4	СВ	C8	C6	C4
	Code area (KB)	128	64	32	16	128	64	32	16
Flash	Data area (KB)	0	0	0	0	0	0	0	0
	Total (KB)	128	64	32	16	128	64	32	16
;	SRAM (KB)	32	20	10	6	32	20	10	6
	General	4	4	2	2	4	4	2	2
	timer(16-bit)	(1-4)	(1-4)	(1-2)	(1-2)	(1-4)	(1-4)	(1-2)	(1-2)
	Advanced	1	1	1	1	1	1	1	1
	timer(16-bit)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
Timers	SysTick	1	1	1	1	1	1	1	1
i≡	Basic	2	2	2	2	2	2	2	2
	timer(16-bit)	(5-6)	(5-6)	(5-6)	(5-6)	(5-6)	(5-6)	(5-6)	(5-6)
	Watchdog	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1
	U(S)ART	2	2	2	2	3	3	2	2
rity	I2C	1	1	1	1	2 (0-1)	2 (0-1)	1	1
Connectivity	SPI/I2S	1/-	1/-	1/-	1/-	3/2	3/2	1/-	1/-
ŏ	CAN	2	2	2	2	2	2	2	2
	USBFS	1	1	1	1	1	1	1	1
	GPIO	26	26	26	26	37	37	37	37
	EXMC	-	-	-	-	-	-	-	-
	EXTI	16	16	16	16	16	16	16	16
ADC	Units	2	2	2	2	2	2	2	2
AE	Channels	10	10	10	10	10	10	10	10
	DAC	2	2	2	2	2	2	2	2
	Package		QFI	N36		LQFP48			



2.2. Block diagram

Figure 2-1. GD32VF103 block diagram





2.3. Pinouts and pin assignment

Figure 2-2. GD32VF103Vx LQFP100 pinouts

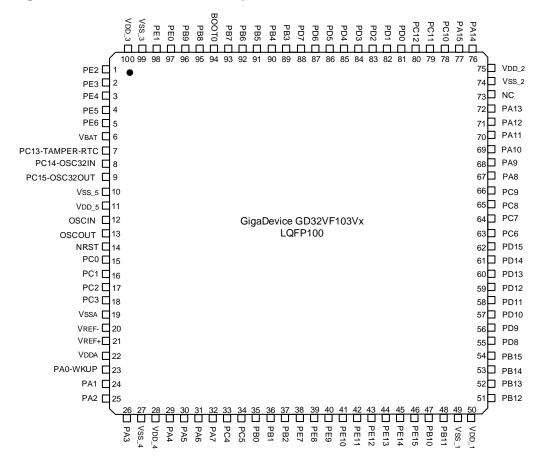




Figure 2-3. GD32VF103Rx LQFP64 pinouts

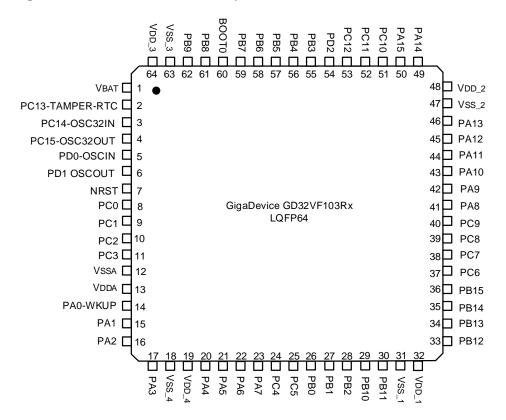




Figure 2-4. GD32VF103Cx LQFP48 pinouts

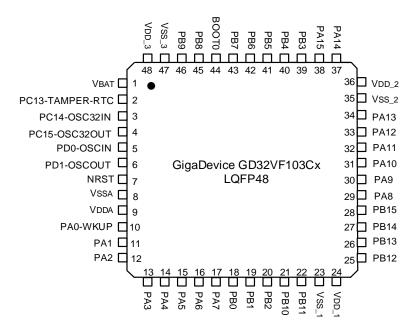
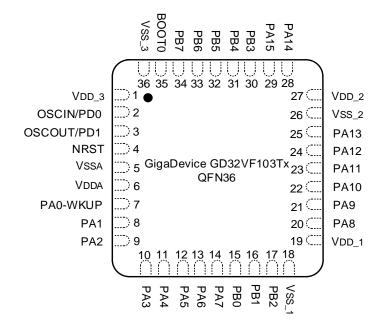


Figure 2-5. GD32VF103Tx QFN36 pinouts





2.4. Memory map

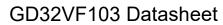
Table 2-3. GD32VF103 memory map

Pre-defined			
Regions	Bus	Address	Peripherals
External			
device		0xA000 0000 - 0xA000 0FFF	EXMC_SWREG
		0x9000 0000 - 0x9FFF FFFF	Reserved
	AHB	0x7000 0000 - 0x8FFF FFFF	Reserved
External RAM			EXMC -
		0x6000 0000 - 0x6FFF FFFF	NOR/PSRAM/SRA
			М
		0x5000 0000 - 0x5003 FFFF	USBFS
		0x4008 0000 - 0x4FFF FFFF	Reserved
		0x4004 0000 - 0x4007 FFFF	Reserved
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	Reserved
		0x4002 6800 - 0x4002 7FFF	Reserved
	АНВ	0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	Reserved
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	Reserved
		0x4002 3800 - 0x4002 3BFF	Reserved
Peripheral		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	Reserved
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
		0x4001 8400 - 0x4001 FFFF	Reserved





Pre-defined			
Regions Bus		Address	Peripherals
		0x4001 8000 - 0x4001 83FF	Reserved
		0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	Reserved
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	Reserved
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	Reserved
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	Reserved
		0x4001 4400 - 0x4001 47FF	Reserved
		0x4001 4000 - 0x4001 43FF	Reserved
	APB2	0x4001 3C00 - 0x4001 3FFF	Reserved
	AFDZ	0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	Reserved
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	GPIOE
		0x4001 1400 - 0x4001 17FF	GPIOD
		0x4001 1000 - 0x4001 13FF	GPIOC
		0x4001 0C00 - 0x4001 0FFF	GPIOB
		0x4001 0800 - 0x4001 0BFF	GPIOA
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	AFIO
		0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	Reserved
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
	APB1	0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU





Pre-defined Bus		Address	Peripherals
		0x4000 6C00 - 0x4000 6FFF	BKP
		0x4000 6800 - 0x4000 6BFF	CAN1
		0x4000 6400 - 0x4000 67FF	CAN0
		0x4000 6000 - 0x4000 63FF	Shared USB/CAN
			SRAM 512bytes
		0x4000 5C00 - 0x4000 5FFF	USB device FS registers
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	Reserved
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	Reserved
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
		0x2007 0000 - 0x3FFF FFFF	Reserved
		0x2006 0000 - 0x2006 FFFF	Reserved
		0x2003 0000 - 0x2005 FFFF	Reserved
SRAM	AHB	0x2002 0000 - 0x2002 FFFF	Reserved
		0x2001 C000 - 0x2001 FFFF	Reserved
		0x2001 8000 - 0x2001 BFFF	Reserved
		0x2000 0000 - 0x2001 7FFF	SRAM
		0x1FFF F810 - 0x1FFF FFFF	Reserved
Code	AHB	0x1FFF F800 - 0x1FFF F80F	Option Bytes
		0x1FFF B000 - 0x1FFF F7FF	Boot loader



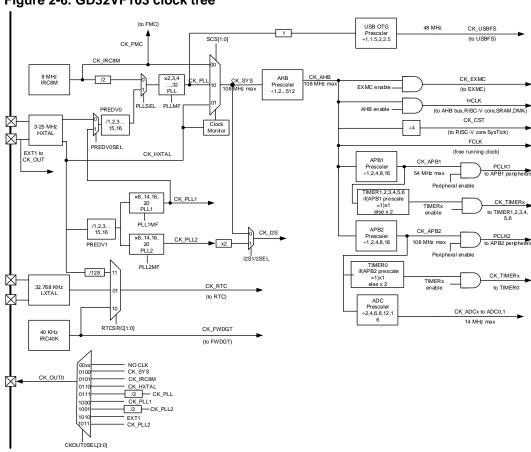
GD32VF103 Datasheet

Pre-defined Regions	Bus	Address	Peripherals
		0x1FFF 7A10 - 0x1FFF AFFF	Reserved
		0x1FFF 7800 - 0x1FFF 7A0F	Reserved
		0x1FFF 0000 - 0x1FFF 77FF	Reserved
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Reserved
		0x1001 0000 - 0x1FFE BFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	Reserved
		0x083C 0000 - 0x0FFF FFFF	Reserved
		0x0830 0000 - 0x083B FFFF	Reserved
		0x0802 0000 - 0x082F FFFF	Reserved
		0x0800 0000 - 0x0801 FFFF	Main Flash
		0x0030 0000 - 0x07FF FFFF	Reserved
		0x0000 0000 - 0x002F FFFF	Aliased to Main
		0x0000 0000 - 0x002F FFFF	Flash or Boot loader



2.5. Clock tree

Figure 2-6. GD32VF103 clock tree



Legend:

HXTAL: High speed external clock

LXTAL: Low speed external clock

IRC8M: High speed internal clock

IRC40K: Low speed internal clock



2.6. Pin definitions

2.6.1. GD32VF103Vx LQFP100 pin definitions

Table 2-4. GD32VF103Vx LQFP100 pin definitions

		Pin	1/0	pin definitions
Pin Name	Pins	Type ⁽¹⁾	Level ⁽²⁾	Functions description
DEG	,		=) /T	Default: PE2
PE2	1	I/O	5VT	Alternate: EXMC_A23
	_		_,	Default: PE3
PE3	2	I/O	5VT	Alternate: EXMC_A19
DE 4			=\ /T	Default: PE4
PE4	3	I/O	5VT	Alternate: EXMC_A20
DEC		1/0	E) /T	Default: PE5
PE5	4	I/O	5VT	Alternate: EXMC_A21
DEC		1/0	5\ /T	Default: PE6
PE6	5	I/O	5VT	Alternate: EXMC_A22
V _{BAT}	6	Р		Default: V _{BAT}
PC13-				Default: PC13
TAMPER-	7	I/O		Alternate: TAMPER-RTC
RTC				Allemate. TAIMPER-RTC
PC14-	8	I/O		Default: PC14
OSC32IN	0	1/0		Alternate: OSC32IN
PC15-	9	I/O		Default: PC15
OSC32OUT	9	1/0		Alternate: OSC32OUT
Vss_5	10	Р		Default: V _{SS_5}
V_{DD_5}	11	Р		Default: V _{DD_5}
OSCIN	12	ı		Default: OSCIN
000114	12	'		Remap: PD0
OSCOUT	13	0		Default: OSCOUT
	10			Remap: PD1
NRST	14	I/O		Default: NRST
PC0	15	I/O		Default: PC0
1 00	10	1/0		Alternate: ADC01_IN10
PC1	16	I/O		Default: PC1
	10	.,, C		Alternate: ADC01_IN11
PC2	17	I/O		Default: PC2
. 52	.,	., 0		Alternate: ADC01_IN12
PC3	18	I/O		Default: PC3
. 55	.0	., 0		Alternate: ADC01_IN13
Vssa	19	Р		Default: V _{SSA}



				OD32 VI 103 D8
Pin Name	Pins	Pin	I/O	Functions description
		Type ⁽¹⁾	Level ⁽²⁾	
V_{REF}	20	Р		Default: V _{REF-}
V_{REF+}	21	Р		Default: V _{REF+}
V_{DDA}	22	Р		Default: V _{DDA}
				Default: PA0
PA0-WKUP	23	I/O		Alternate: WKUP, USART1_CTS,
PAU-WKUP	23	1/0		ADC01_IN0, TIMER1_CH0 _ETI,
				TIMER4_CH0,
				Default: PA1
PA1	24	I/O		Alternate: USART1_RTS, ADC01_IN1,
				TIMER1_CH1, TIMER4_CH1,
				Default: PA2
PA2	25	I/O		Alternate: USART1_TX, ADC01_IN2,
				TIMER1_CH2, TIMER4_CH2
				Default: PA3
PA3	26	I/O		Alternate: USART1_RX, ADC01_IN3,
				TIMER1_CH3, TIMER4_CH3
Vss 4	27	Р		Default: Vss_4
V _{DD_4}	28	Р		Default: V _{DD_4}
	29	29 I/O		Default: PA4
				Alternate: SPI0_NSS, USART1_CK,
PA4				ADC01_IN4, DAC_OUT0
				Remap: SPI2_NSS, I2S2_WS
				Default: PA5
PA5	30	I/O		Alternate: SPI0_SCK, ADC01_IN5,
				DAC_OUT1
				Default: PA6
		I/O		Alternate: SPI0_MISO, ADC01_IN6,
PA6	31			TIMER2_CH0
				Remap: TIMER0_BRKIN
				Default: PA7
PA7				Alternate: SPI0_MOSI, ADC01_IN7,
	32	I/O		TIMER2_CH1
				Remap: TIMER0_CH0_ON
				Default: PC4
PC4	33	I/O		Alternate: ADC01_IN14
PC5 3-		I/O		Default: PC5
	34			Alternate: ADC01_IN15
				Default: PB0
PB0	35	I/O		Alternate: ADC01_IN8, TIMER2_CH2
יטט ז	33	1/0		·
i				Remap: TIMER0_CH1_ON



Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
				Default: PB1
PB1	36	I/O		Alternate: ADC01_IN9, TIMER2_CH3
				Remap: TIMER0_CH2_ON
PB2	37	I/O	5VT	Default: PB2, BOOT1
				Default: PE7
PE7	38	I/O	5VT	Alternate: EXMC_D4
				Remap: TIMER0_ETI
				Default: PE8
PE8	39	I/O	5VT	Alternate: EXMC_D5
				Remap: TIMER0_CH0_ON
				Default: PE9
PE9	40	I/O	5VT	Alternate: EXMC_D6
				Remap: TIMER0_CH0
				Default: PE10
PE10	41	I/O	5VT	Alternate: EXMC_D7
				Remap: TIMER0_CH1_ON
				Default: PE11
PE11	42	I/O	5VT	Alternate: EXMC_D8
				Remap: TIMER0_CH1
				Default: PE12
PE12	43	I/O	5VT	Alternate: EXMC_D9
				Remap: TIMER0_CH2_ON
				Default: PE13
PE13	44	I/O	5VT	Alternate: EXMC_D10
				Remap: TIMER0_CH2
				Default: PE14
PE14	45	I/O	5VT	Alternate: EXMC_D11
				Remap: TIMER0_CH3
				Default: PE15
PE15	46	I/O	5VT	Alternate: EXMC_D12
				Remap: TIMER0_BRKIN
				Default: PB10
PB10	47	I/O	5VT	Alternate: I2C1_SCL, USART2_TX,
				Remap: TIMER1_CH2
				Default: PB11
PB11	48	I/O	5VT	Alternate: I2C1_SDA, USART2_RX
				Remap: TIMER1_CH3
V _{SS_1}	49	Р		Default: Vss_1
V_{DD_1}	50	Р		Default: V _{DD_1}



				GD327F103 Da
Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
				Default: PB12
55.40			->	Alternate: SPI1_NSS, I2C1_SMBA,
PB12	51	I/O	5VT	USART2_CK, TIMER0_BRKIN, I2S1_WS,
				CAN1_RX
				Default: PB13
PB13	52	I/O	5VT	Alternate: SPI1_SCK, USART2_CTS,
				TIMER0_CH0_ON, I2S1_CK, CAN1_TX,
				Default: PB14
PB14	53	I/O	5VT	Alternate: SPI1_MISO, USART2_RTS,
				TIMER0_CH1_ON
				Default: PB15
PB15	54	I/O	5VT	Alternate: SPI1_MOSI, TIMER0_CH2_ON,
				I2S1_SD
				Default: PD8
PD8	55	I/O	5VT	Alternate: EXMC_D13
				Remap: USART2_TX
				Default: PD9
PD9	56	I/O	5VT	Alternate: EXMC_D14
				Remap: USART2_RX
			5VT	Default: PD10
PD10	57	I/O		Alternate: EXMC_D15
				Remap: USART2_CK
				Default: PD11
PD11	58	I/O	5VT	Alternate: EXMC_A16/EXMC_CLE
				Remap: USART2_CTS
				Default: PD12
PD12	59	I/O	5VT	Alternate: EXMC_A17/EXMC_ALE
				Remap: TIMER3_CH0, USART2_RTS
				Default: PD13
PD13	60	I/O	5VT	Alternate: EXMC_A18
				Remap: TIMER3_CH1
				Default: PD14
PD14	61	I/O	5VT	Alternate: EXMC_D0
			J V 1	Remap: TIMER3_CH2
				Default: PD15
PD15	62	I/O	5VT	Alternate: EXMC_D1
•	02	1/0	371	Remap: TIMER3_CH3
				Default: PC6
PC6	63	I/O	5VT	Alternate: I2S1_MCK
				Remap: TIMER2_CH0
				· ~



Pin Name					OD32 VI 103 D8
PC7 64 I/O 5VT Alternate: IZS2_MCK Remap: TIMER2_CH1 PC8 65 I/O 5VT Default: PC8 Remap: TIMER2_CH2 PC9 66 I/O 5VT Default: PC9 Remap: TIMER2_CH3 PA8 67 I/O 5VT Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF PA9 68 I/O 5VT Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS PA10 69 I/O 5VT Alternate: USART0_TX, TIMER0_CH1, USBFS_ID PA11 70 I/O 5VT Alternate: USART0_TX, TIMER0_CH2, USBFS_ID PA11 70 I/O 5VT Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3 PA12 71 I/O 5VT Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI PA13 72 I/O 5VT Default: JTMS Remap: PA13 NC 73 - - Vss 2 74 P Default: Vss 2 PA14 76 I/O 5VT Remap: PA14 PA15 77 I/O 5VT <th>Pin Name</th> <th>Pins</th> <th>Pin Type⁽¹⁾</th> <th>I/O Level⁽²⁾</th> <th>Functions description</th>	Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
Remap: TIMER2_CH1					Default: PC7
PC8 65 I/O SVT Default: PC8 Remap: TIMER2_CH2 PC9 66 I/O SVT Default: PC9 Remap: TIMER2_CH3 PA8 67 I/O SVT Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF PA9 68 I/O SVT Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS PA10 69 I/O SVT Alternate: USART0_RX, TIMER0_CH2, USBFS_ID PA11 70 I/O SVT Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3 PA12 71 I/O SVT Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI PA13 72 I/O SVT Default: PA12 ANC 73 - CAN0_TX, TIMER0_ETI PA13 72 I/O SVT Default: JTMS Remap: PA13 NC 73 - Default: Vss_2 Vob_2 75 P Default: JTCK Remap: PA14 PA14 76 I/O SVT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O <td>PC7</td> <td>64</td> <td>I/O</td> <td>5VT</td> <td>Alternate: I2S2_MCK</td>	PC7	64	I/O	5VT	Alternate: I2S2_MCK
PC8 65 I/O 5VT Remap: TIMER2_CH2 PC9 66 I/O 5VT Remap: TIMER2_CH3 Default: PC9 Remap: TIMER2_CH3 Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS Default: PA10 PA10 69 I/O 5VT Alternate: USART0_RX, TIMER0_CH2, USBFS_ID PA11 70 I/O 5VT Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3 PA12 71 I/O 5VT Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI PA13 72 I/O 5VT Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI PA13 72 I/O 5VT Remap: PA13 NC 73 - CAN0_TX, TIMER0_ETI PA14 76 I/O 5VT Default: Vss_2 Voo_2 75 P Default: Vss_2 Voo_2 75 P Default: JTCK Remap: PA14 Default: JTDI Alternate: SPI2_NS, I2S2_WS					Remap: TIMER2_CH1
Remap: TIMER2_CH2	DOG	0.5		5) (T	Default: PC8
PC9 66 I/O 5VT Remap: TIMER2_CH3 PA8 67 I/O 5VT Remap: TIMER2_CH3 PA9 68 I/O 5VT Alternate: USARTO_CK, TIMER0_CH1, USBFS_VBUS PA10 69 I/O 5VT Alternate: USARTO_RX, TIMER0_CH2, USBFS_ID PA11 70 I/O 5VT Alternate: USARTO_CTS, CANO_RX, USBFS_DM, TIMER0_CH3 PA12 71 I/O 5VT Alternate: USARTO_RTS, USBFS_DP, CANO_TX, TIMER0_ETI PA13 72 I/O 5VT Default: JTMS Remap: PA13 NC 73 - Default: Vss_2 Vob.2 75 P Default: Vbs_2 PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX	PC8	65	1/0	501	Remap: TIMER2_CH2
PA8	DOG	00	1/0	5) (T	Default: PC9
PA8 67 I/O 5VT Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF PA9 68 I/O 5VT Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS PA10 69 I/O 5VT Alternate: USART0_RX, TIMER0_CH2, USBFS_ID PA11 70 I/O 5VT Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3 PA12 71 I/O 5VT Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI PA13 72 I/O 5VT Default: JTMS Remap: PA13 NC 73 - - Vss_2 74 P Default: Vss_2 Vod_2 75 P Default: JTCK Remap: PA14 PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX	PC9	66	1/0	501	Remap: TIMER2_CH3
CK_OUT0, USBFS_SOF					Default: PA8
PA9 68 I/O 5VT Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS PA10 69 I/O 5VT Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID PA11 70 I/O 5VT Default: PA11 Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3 PA12 71 I/O 5VT Default: PA12 Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI PA13 72 I/O 5VT Default: JTMS Remap: PA13 NC 73 - Default: VDD_2 VSS_2 74 P Default: VDD_2 PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX	PA8	67	I/O	5VT	Alternate: USART0_CK, TIMER0_CH0,
PA9					CK_OUT0, USBFS_SOF
Default: PA10					Default: PA9
PA10 69	PA9	68	I/O	5VT	Alternate: USART0_TX, TIMER0_CH1,
PA10 69					USBFS_VBUS
Default: PA11					Default: PA10
PA11 70 I/O 5VT Default: PA11 Alternate: USARTO_CTS, CANO_RX, USBFS_DM, TIMERO_CH3 PA12 71 I/O 5VT Alternate: USARTO_RTS, USBFS_DP, CANO_TX, TIMERO_ETI PA13 72 I/O 5VT Default: JTMS Remap: PA13 NC 73 - Default: Vss_2 VDD_2 75 P Default: VDD_2 PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX	PA10	69	I/O	5VT	Alternate: USART0_RX, TIMER0_CH2,
PA11 70 I/O 5VT Alternate: USARTO_CTS, CANO_RX, USBFS_DM, TIMERO_CH3 PA12 71 I/O 5VT Alternate: USARTO_RTS, USBFS_DP, CANO_TX, TIMERO_ETI PA13 72 I/O 5VT Default: JTMS Remap: PA13 NC 73 - Default: Vss_2 VDD_2 75 P Default: VDD_2 PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX					USBFS_ID
Default: PA12					Default: PA11
PA12	PA11	70	I/O	5VT	Alternate: USART0_CTS, CAN0_RX,
PA12 71 I/O 5VT Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI PA13 72 I/O 5VT Default: JTMS Remap: PA13 NC 73 - Default: Vss_2 Vbd_2 75 P Default: Vbd_2 PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX					USBFS_DM, TIMER0_CH3
PA13 72 I/O 5VT Default: JTMS Remap: PA13 NC 73 -				5VT	Default: PA12
PA13 72 I/O 5VT Default: JTMS Remap: PA13 NC 73 - - Vss_2 74 P Default: Vss_2 Vpp_2 75 P Default: JTCK Remap: PA14 PA14 76 I/O 5VT Default: JTDI Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX	PA12	71	I/O		Alternate: USART0_RTS, USBFS_DP,
PA13 72 I/O 5VT Remap: PA13 NC 73 - - Vss_2 74 P Default: Vss_2 VDD_2 75 P Default: VDD_2 PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX					CAN0_TX, TIMER0_ETI
NC 73 -	DA42	70	1/0	C)/T	Default: JTMS
Vss_2 74 P Default: Vss_2 VDD_2 75 P Default: VDD_2 PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX	PAIS	12	1/0	501	Remap: PA13
VDD_2 75 P Default: VDD_2 PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX	NC	73			-
PA14 76 I/O 5VT Default: JTCK Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX	Vss_2	74	Р		Default: Vss_2
PA14 76 I/O 5VT Remap: PA14 PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK Default: PC11 PC11 79 I/O 5VT Alternate: UART3_RX	V _{DD_2}	75	Р		Default: V _{DD_2}
Remap: PA14 Default: JTDI	DA44	70	1/0	5) /T	Default: JTCK
PA15 77 I/O 5VT Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Alternate: UART3_RX	PA14	76	1/0	501	Remap: PA14
Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS					Default: JTDI
PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK Default: PC11 PC11 79 I/O 5VT Alternate: UART3_RX	PA15	77	I/O	5VT	Alternate: SPI2_NSS, I2S2_WS
PC10 78 I/O 5VT Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK PC11 79 I/O 5VT Default: PC11 Alternate: UART3_RX					Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS
Remap: USART2_TX, SPI2_SCK, I2S2_CK Default: PC11 PC11 79 I/O 5VT Alternate: UART3_RX					Default: PC10
PC11 79 I/O 5VT Alternate: UART3_RX	PC10	78	I/O	5VT	Alternate: UART3_TX
PC11 79 I/O 5VT Alternate: UART3_RX					Remap: USART2_TX, SPI2_SCK, I2S2_CK
					Default: PC11
Remap: USART2_RX, SPI2_MISO	PC11	79	I/O	5VT	Alternate: UART3_RX
					Remap: USART2_RX, SPI2_MISO
Default: PC12	DC40	00	1/0	E\	Default: PC12
PC12 80 I/O 5VT Alternate: UART4_TX	PU12	80	1/0	1 201	Alternate: UART4_TX



Pin Name						
Remap: USART2_CK, SPI2_MOSI, I2S2_SD	Pin Name	Pins	Pin	1/0	Functions description	
Default: PD0			Type ⁽¹⁾	Level ⁽²⁾	•	
PD0					Remap: USART2_CK, SPI2_MOSI, I2S2_SD	
Remap: CANO_RX					Default: PD0	
PD1	PD0	81	I/O	5VT	Alternate: EXMC_D2	
PD1					Remap: CAN0_RX	
Remap: CAN0_TX					Default: PD1	
PD2	PD1	82	I/O	5VT	Alternate: EXMC_D3	
PD2					Remap: CAN0_TX	
Alternate: TIMER2_ETI, UART4_RX	PD2	83	1/0	5\/T	Default: PD2	
PD3	1 02	00	1/0	371	Alternate: TIMER2_ETI, UART4_RX	
Remap: USART1_CTS	DD3	8/1	1/0	5\/T	Default: PD3	
PD4 85 I/O 5VT Alternate: EXMC_NOE Remap: USART1_RTS PD5 86 I/O 5VT Alternate: EXMC_NWE Remap: USART1_TX PD6 87 I/O 5VT Alternate: EXMC_NWAIT Remap: USART1_RX PD7 88 I/O 5VT Alternate: EXMC_NEO Remap: USART1_CK PB3 89 I/O 5VT Alternate: SPI2_SCK, I2S2_CK Remap: PB3, TIMER1_CH1, SPI0_SCK PB4 90 I/O 5VT Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO PB5 91 I/O Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,	1 00	07	1/0	371	Remap: USART1_CTS	
Remap: USART1_RTS					Default: PD4	
Default: PD5	PD4	85	I/O	5VT	Alternate: EXMC_NOE	
PD5 86 I/O 5VT Alternate: EXMC_NWE Remap: USART1_TX PD6 87 I/O 5VT Alternate: EXMC_NWAIT Remap: USART1_RX PD7 88 I/O 5VT Alternate: EXMC_NE0 Remap: USART1_CK PB3 89 I/O 5VT Alternate: SPI2_SCK, I2S2_CK Remap: PB3, TIMER1_CH1, SPI0_SCK PB4 90 I/O 5VT Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO PB5 91 I/O Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,					Remap: USART1_RTS	
Remap: USART1_TX					Default: PD5	
Default: PD6	PD5	86	I/O	5VT	Alternate: EXMC_NWE	
PD6 87 I/O 5VT Alternate: EXMC_NWAIT Remap: USART1_RX PD7 88 I/O 5VT Alternate: EXMC_NE0 Remap: USART1_CK PB3 89 I/O 5VT Alternate: SPI2_SCK, I2S2_CK Remap: PB3, TIMER1_CH1, SPI0_SCK PB4 90 I/O 5VT Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO PB5 91 I/O Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,					Remap: USART1_TX	
Remap: USART1_RX						Default: PD6
Default: PD7	PD6	87	I/O	5VT	Alternate: EXMC_NWAIT	
PD7 88 I/O 5VT Alternate: EXMC_NE0 Remap: USART1_CK PB3 89 I/O 5VT Alternate: SPI2_SCK, I2S2_CK Remap: PB3, TIMER1_CH1, SPI0_SCK PB4 90 I/O 5VT Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO PB5 91 I/O Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,					Remap: USART1_RX	
Remap: USART1_CK Default: JTDO					Default: PD7	
PB3 89 I/O 5VT Alternate:SPI2_SCK, I2S2_CK Remap: PB3, TIMER1_CH1, SPI0_SCK Default: NJTRST PB4 90 I/O 5VT Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI, Remap: TIMER2_CH1, SPI0_MOSI,	PD7	88	I/O	5VT	Alternate: EXMC_NE0	
PB3 89 I/O 5VT Alternate:SPI2_SCK, I2S2_CK Remap: PB3, TIMER1_CH1, SPI0_SCK PB4 90 I/O 5VT Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO PB5 91 I/O Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,					Remap: USART1_CK	
Remap: PB3, TIMER1_CH1, SPI0_SCK					Default: JTDO	
PB4 90 I/O 5VT Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,	PB3	89	I/O	5VT	Alternate:SPI2_SCK, I2S2_CK	
PB4 90 I/O 5VT Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,					Remap: PB3, TIMER1_CH1, SPI0_SCK	
PB5 PB5 Remap: TIMER2_CH0, PB4, SPI0_MISO Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,					Default: NJTRST	
PB5 91 I/O Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,	PB4	90	I/O	5VT	Alternate: SPI2_MISO	
PB5 91 I/O Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI,					Remap: TIMER2_CH0, PB4, SPI0_MISO	
PB5 91 I/O Remap: TIMER2_CH1, SPI0_MOSI,					Default: PB5	
Remap: TIMER2_CH1, SPI0_MOSI,	555	0.4	1/0		Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD	
CAN1_RX	PB5	91	1/0		Remap: TIMER2_CH1, SPI0_MOSI,	
					CAN1_RX	
Default: PB6					Default: PB6	
PB6 92 I/O 5VT Alternate: I2C0_SCL, TIMER3_CH0	PB6	92	I/O	5VT	Alternate: I2C0_SCL, TIMER3_CH0	
Remap: USART0_TX, CAN1_TX					Remap: USART0_TX, CAN1_TX	
Default: PB7					Default: PB7	
PB7 93 I/O 5VT Alternate: I2C0_SDA , TIMER3_CH1,	PB7	93	I/O	5VT	Alternate: I2C0_SDA , TIMER3_CH1,	
EXMC_NADV					EXMC_NADV	



Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
				Remap: USART0_RX
воото	94	I		Default: BOOT0
				Default: PB8
PB8	95	I/O	5VT	Alternate: TIMER3_CH2
				Remap: I2C0_SCL, CAN0_RX
				Default: PB9
PB9	96	I/O	5VT	Alternate: TIMER3_CH3
				Remap: I2C0_SDA, CAN0_TX
PE0	97	I/O	5VT	Default: PE0
PEU	97	1/0	501	Alternate: TIMER3_ETI, EXMC_NBL0
PE1	00	I/O	5VT	Default: PE1
PEI	98	1/0		Alternate: EXMC_NBL1
Vss_3	99	Р		Default: Vss_3
V _{DD_3}	100	Р		Default: V _{DD_3}

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.



2.6.2. GD32VF103Rx LQFP64 pin definitions

Table 2-5. GD32VF103Rx LQFP64 pin definitions

Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
V_{BAT}	1	Р		Default: V _{BAT}
PC13-	2	I/O		Default: PC13
TAMPER-RTC	2	1/0		Alternate: TAMPER-RTC
PC14-	3	I/O		Default: PC14
OSC32IN	3	1/0		Alternate: OSC32IN
PC15-	4	I/O		Default: PC15
OSC32OUT	'	","		Alternate: OSC32OUT
OSCIN	5	1		Default: OSCIN
		·		Remap: PD0
OSCOUT	6	0		Default: OSCOUT
				Remap: PD1
NRST	7	I/O		Default: NRST
PC0	8	I/O		Default: PC0
				Alternate: ADC01_IN10
PC1	9	I/O		Default: PC1
				Alternate: ADC01_IN11
PC2	10	I/O		Default: PC2
				Alternate: ADC01_IN12
PC3	11	I/O		Default: PC3
		_		Alternate: ADC01_IN13
Vssa	12	Р		Default: Vssa
V _{DDA}	13	Р		Default: V _{DDA}
				Default: PA0
PA0-WKUP	14	I/O		Alternate: WKUP, USART1_CTS, ADC01_IN0,
				TIMER1_CH0 _ETI, TIMER4_CH0 ⁽³⁾
-				Default: PA1
PA1	15	I/O		Alternate: USART1_RTS, ADC01_IN1, TIMER1_CH1,
				TIMER4_CH1 ⁽³⁾
DAG	16	1/0		Default: PA2
PA2		I/O		Alternate: USART1_TX, ADC01_IN2, TIMER1_CH2,
				TIMER4_CH2 ⁽³⁾
מאם	17	I/O		Default: PA3 Alternate: USART1_RX, ADC01_IN3, TIMER1_CH3,
PA3	17			TIMER4_CH3 ⁽³⁾
\/aa :	18	Р		
Vss_4		P		Default: Vss_4
V_{DD_4}	19	1		Default: V _{DD_4}



PA4 20 I/O Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4, DAC_OUTO Remap:SPI2_NSS ⁽³⁾ , I2S2_WS ⁽³⁾ PA5 21 I/O Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1 PA6 22 I/O Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BRKIN PA7 23 I/O Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1 Remap: TIMER0_CH0_ON PC4 24 I/O Default: PC4 Alternate: ADC01_IN14 PC5 25 I/O Default: PC5 Alternate: ADC01_IN15 PB0 26 I/O Default: PB1 Alternate: ADC01_IN8, TIMER2_CH2, Remap: TIMER0_CH2_ON PB1 27 I/O Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, Remap: TIMER0_CH2_ON PB2 28 I/O SVT Default: PB10 Alternate: IZC1_SCL ⁽³⁾ , USART2_TX ⁽³⁾ , Remap: TIMER1_CH2 Default: PB10 PB10 29 I/O SVT Alternate: IZC1_SDA ⁽³⁾ , USART2_RX ⁽³⁾ , Remap: TIMER1_CH2 Default: VSs_1 PB11 30 I/O SVT Alternate: IZC1_SDA ⁽³⁾ , USART2_RX ⁽³⁾ , Remap: TIMER1_CH3 Default: VSs_1 Default: VSs_1 Default: VSs_1 Default: VSs_1 Alternate: PB12 Alternate: PB12 Alternate: PB12 Alternate: SP11_NSS ⁽³⁾ , I2C1_SMBA ⁽³⁾ , USART2_CX ⁽³⁾ , CAN1_RX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ , TIMER0_CH0_ON, I2S1_CK ⁽³⁾ , CAN1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ , TIMER0_CH0_ON, I2S1_CK ⁽³⁾ , CAN1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , USART1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , USART1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , USART1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , USART1_CCTS ⁽³⁾ , TIMER0_CH0_ON, I2S1_CK ⁽³⁾ , CAN1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , USART1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , USART1_CCTS ⁽³⁾ , TIMER0_CH0_ON, I2S1_CK ⁽³⁾ , CAN1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , USART1_CCTS ⁽³⁾ , TIMER0_CH0_ON, I2S1_CK ⁽³⁾ , CAN1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , CAN1_TX Default: PB13 Alternate: SP11_SCK ⁽³⁾ , CAN1_TX Default: PB14 Alternate:	Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
PA4 20 I/O DAC_OUTO Remap:SPI2_NSS(3), I2S2_WS(3) PA5 21 I/O Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1 Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BRKIN Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1 Remap: TIMER0_CH0_ON Default: PC4 Alternate: ADC01_IN14 Default: PC5 Alternate: ADC01_IN14 Default: PC5 Alternate: ADC01_IN15 Default: PB0 PB0 26 I/O Alternate: ADC01_IN8, TIMER2_CH2, Remap: TIMER0_CH2_ON Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, Remap: TIMER0_CH2_ON PB2 28 I/O SVT Default: PB2, BOOT1 Default: PB1 Default:					
Remap:SPI2_NSS(3), I2S2_WS(3)	PA4	20	I/O		
PA5					
PA5					· · · · · · · · · · · · · · · · · · ·
Default: PA6	PA5	21	I/O		
Remap: TIMERO_BRKIN					
Default: PA7	PA6	22	I/O		Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0
PA7					Remap: TIMER0_BRKIN
Remap: TIMERO_CHO_ON					Default: PA7
PC4	PA7	23	I/O		Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1
PC4 24 I/O Alternate: ADC01_IN14 PC5 25 I/O Default: PC5 Alternate: ADC01_IN15 Default: PB0 26 I/O Alternate: ADC01_IN8, TIMER2_CH2, Remap: TIMER0_CH1_ON PB1 27 I/O Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, Remap: TIMER0_CH2_ON PB2 28 I/O 5VT Default: PB2, BOOT1 PB10 29 I/O 5VT Alternate: I2C1_SCL(3), USART2_TX(3), Remap: TIMER1_CH2 PB11 30 I/O 5VT Alternate: I2C1_SDA(3), USART2_RX(3), Remap: TIMER1_CH3 Vss_1 31 P Default: Vss_1 Vss_1 31 P Default: Vss_1 PB12 33 I/O 5VT Alternate: SPI1_NSS(3), I2C1_SMBA(3), USART2_CK(3), TIMER0_BRKIN, I2S1_WS(3), CAN1_RX PB13 34 I/O 5VT Alternate: SPI1_SCK(3), USART2_CTS(3),					Remap: TIMER0_CH0_ON
Alternate: ADC01_IN14	DC4	24	1/0		Default: PC4
PC5	PC4	24	1/0		Alternate: ADC01_IN14
Alternate: ADC01_IN15	DC5	25	1/0		Default: PC5
PB0	PC5	23	1/0		Alternate: ADC01_IN15
Remap: TIMER0_CH1_ON					Default: PB0
Default: PB1	PB0	26	I/O		Alternate: ADC01_IN8, TIMER2_CH2,
PB1 27 I/O Alternate: ADC01_IN9, TIMER2_CH3, Remap: TIMER0_CH2_ON PB2 28 I/O 5VT Default: PB2, BOOT1 PB10 29 I/O 5VT Alternate: I2C1_SCL(3), USART2_TX(3), Remap: TIMER1_CH2 PB11 30 I/O 5VT Alternate: I2C1_SDA(3), USART2_RX(3), Remap: TIMER1_CH3 Vss_1 31 P Default: Vss_1 VbD_1 32 P Default: VbD_1 PB12 33 I/O 5VT Alternate: SPI1_NSS(3), I2C1_SMBA(3), USART2_CK(3), TIMER0_BRKIN, I2S1_WS(3), CAN1_RX PB13 34 I/O 5VT Alternate: SPI1_SCK(3), USART2_CTS(3),					Remap: TIMER0_CH1_ON
Remap: TIMER0_CH2_ON					Default: PB1
PB2 28 I/O 5VT Default: PB2, BOOT1 PB10 29 I/O 5VT Alternate: I2C1_SCL(³), USART2_TX(³), Remap: TIMER1_CH2 PB11 30 I/O 5VT Alternate: I2C1_SDA(³), USART2_RX(³), Remap: TIMER1_CH3 Vss_1 31 P Default: Vss_1 VDD_1 32 P Default: VDD_1 PB12 33 I/O 5VT Alternate: SPI1_NSS(³), I2C1_SMBA(³), USART2_CK(³), TIMER0_BRKIN, I2S1_WS(³), CAN1_RX PB13 34 I/O 5VT Alternate: SPI1_SCK(³), USART2_CTS(³),	PB1	27	I/O		
PB10 29 I/O 5VT Alternate: I2C1_SCL(3), USART2_TX(3), Remap: TIMER1_CH2 PB11 30 I/O 5VT Alternate: I2C1_SDA(3), USART2_RX(3), Remap: TIMER1_CH3 Vss_1 31 P Default: Vss_1 Vbd_1 32 P Default: Vbd_1 Default: PB12 Alternate: SPI1_NSS(3), I2C1_SMBA(3), USART2_CK(3), TIMER0_BRKIN, I2S1_WS(3), CAN1_RX Default: PB13 PB13 34 I/O 5VT Alternate: SPI1_SCK(3), USART2_CTS(3),					Remap: TIMER0_CH2_ON
PB10 29 I/O 5VT Alternate: I2C1_SCL(3), USART2_TX(3), Remap: TIMER1_CH2 PB11 30 I/O 5VT Alternate: I2C1_SDA(3), USART2_RX(3), Remap: TIMER1_CH3 Vss_1 31 P Default: Vss_1 VDD_1 32 P Default: VDD_1 Default: PB12 Alternate: SPI1_NSS(3), I2C1_SMBA(3), USART2_CK(3), TIMER0_BRKIN, I2S1_WS(3), CAN1_RX Default: PB13 Default: PB13 PB13 34 I/O 5VT Alternate: SPI1_SCK(3), USART2_CTS(3),	PB2	28	I/O	5VT	Default: PB2, BOOT1
Remap: TIMER1_CH2					
PB11 30 I/O 5VT Alternate: I2C1_SDA ⁽³⁾ , USART2_RX ⁽³⁾ , Remap: TIMER1_CH3 Vss_1 31 P Default: Vss_1 VDD_1 32 P Default: VDD_1 Default: PB12 Alternate: SPI1_NSS ⁽³⁾ , I2C1_SMBA ⁽³⁾ , USART2_CK ⁽³⁾ , TIMER0_BRKIN, I2S1_WS ⁽³⁾ , CAN1_RX Default: PB13 Default: PB13 Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,	PB10	29	I/O	5VT	
PB11 30 I/O 5VT Alternate: I2C1_SDA ⁽³⁾ , USART2_RX ⁽³⁾ , Remap: TIMER1_CH3 Vss_1 31 P Default: Vss_1 VDD_1 32 P Default: VDD_1 Default: PB12 Alternate: SPI1_NSS ⁽³⁾ , I2C1_SMBA ⁽³⁾ , USART2_CK ⁽³⁾ , TIMER0_BRKIN, I2S1_WS ⁽³⁾ , CAN1_RX Default: PB13 Default: PB13 Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,					
Remap: TIMER1_CH3					
V _{SS_1} 31 P Default: V _{SS_1} V _{DD_1} 32 P Default: V _{DD_1} Default: PB12 Default: PB12 Alternate: SPI1_NSS ⁽³⁾ , I2C1_SMBA ⁽³⁾ , USART2_CK ⁽³⁾ , TIMER0_BRKIN, I2S1_WS ⁽³⁾ , CAN1_RX Default: PB13 Default: PB13 Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,	PB11	30	I/O	5VT	
VDD_1 32 P Default: VDD_1 PB12 33 I/O 5VT Default: PB12 Alternate: SPI1_NSS ⁽³⁾ , I2C1_SMBA ⁽³⁾ , USART2_CK ⁽³⁾ , TIMER0_BRKIN, I2S1_WS ⁽³⁾ , CAN1_RX Default: PB13 Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,		0.4			
PB12 33 I/O 5VT Default: PB12 Alternate: SPI1_NSS ⁽³⁾ , I2C1_SMBA ⁽³⁾ , USART2_CK ⁽³⁾ , TIMER0_BRKIN, I2S1_WS ⁽³⁾ , CAN1_RX Default: PB13 PB13 34 I/O 5VT Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,			_		_
PB12 33 I/O 5VT Alternate: SPI1_NSS ⁽³⁾ , I2C1_SMBA ⁽³⁾ , USART2_CK ⁽³⁾ , TIMER0_BRKIN, I2S1_WS ⁽³⁾ , CAN1_RX Default: PB13 PB13 34 I/O 5VT Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,	V _{DD_1}	32	Р		_
PB12 33 I/O 5VT USART2_CK ⁽³⁾ , TIMER0_BRKIN, I2S1_WS ⁽³⁾ , CAN1_RX Default: PB13 PB13 34 I/O 5VT Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,					
CAN1_RX Default: PB13 PB13 34 I/O 5VT Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,	PB12	33	I/O	5VT	
Default: PB13 PB13 34 I/O 5VT Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,					
PB13 34 I/O 5VT Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ ,					_
	PR13	34	I/O	5\/T	
	1 513	3-	I/O	3 7 1	
Default: PB14					
PB14 35 I/O 5VT Alternate: SPI1_MISO(3), USART2_RTS(3),	PB14	35	I/O	5VT	



				ODSZVI 103 Datasiit
Pin Name	Pins	Pin	I/O Level ⁽²⁾	Functions description
		Type ⁽¹⁾	Level	
				TIMER0_CH1_ON
				Default: PB15
PB15	36	I/O	5VT	Alternate: SPI1_MOSI ⁽³⁾ , TIMER0_CH2_ON,
				I2S1_SD ⁽³⁾
				Default: PC6
PC6	37	I/O	5VT	Alternate: I2S1_MCK ⁽³⁾
				Remap: TIMER2_CH0
				Default: PC7
PC7	38	I/O	5VT	Alternate: I2S2_MCK ⁽³⁾
				Remap: TIMER2_CH1
PC8	39	1/0	5VT	Default: PC8
FCo	39	1/0	371	Remap: TIMER2_CH2
DCO	40	I/O	5VT	Default: PC9
PC9	40	1/0	5 / 1	Remap: TIMER2_CH3
				Default: PA8
PA8	41	I/O	5VT	Alternate: USART0_CK, TIMER0_CH0, CK_OUT0,
				USBFS_SOF
			5VT	Default: PA9
PA9	42	I/O		Alternate: USART0_TX, TIMER0_CH1,
				USBFS_VBUS
PA10	42	I/O	5VT	Default: PA10
PATU	43	1/0	5 / 1	Alternate: USART0_RX, TIMER0_CH2, USBFS_ID
				Default: PA11
PA11	44	I/O	5VT	Alternate: USART0_CTS, CAN0_RX, USBFS_DM,
				TIMER0_CH3
				Default: PA12
PA12	45	I/O	5VT	Alternate: USART0_RTS, USBFS_DP, CAN0_TX,
				TIMER0_ETI
PA13	46	1/0	5VT	Default: JTMS
FAIS	40	1/0	371	Remap: PA13
V_{SS_2}	47	Р		Default: V _{SS_2}
V_{DD_2}	48	Р		Default: V _{DD_2}
PA14	49 I/O	r\/T	Default: JTCK	
PA14	49	1/0	5VT	Remap: PA14
				Default: JTDI
PA15	PA15 50 I/O	I/O	5VT	Alternate: SPI2_NSS ⁽³⁾ , I2S2_WS ⁽³⁾
			Remap: TIMER1_CH0 _ETI, PA15, SPI0_NSS	
				Default: PC10
PC10	51	I/O	5VT	Alternate: UART3_TX ⁽³⁾
				Remap: USART2_TX ⁽³⁾ , SPI2_SCK ⁽³⁾ , I2S2_CK ⁽³⁾



Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
				Default: PC11
PC11	52	I/O	5VT	Alternate: UART3_RX ⁽³⁾
				Remap: USART2_RX ⁽³⁾ , SPI2_MISO ⁽³⁾
				Default: PC12
PC12	53	I/O	5VT	Alternate: UART4_TX ⁽³⁾
				Remap: USART2_CK ⁽³⁾ , SPI2_MOSI ⁽³⁾ , I2S2_SD ⁽³⁾
DD2	E A	1/0	E\/T	Default: PD2
PD2	54	I/O	5VT	Alternate: TIMER2_ETI, UART4_RX ⁽³⁾
				Default: JTDO
PB3	55	I/O	5VT	Alternate:SPI2_SCK ⁽³⁾ , I2S2_CK ⁽³⁾
				Remap: PB3, TIMER1_CH1, SPI0_SCK
				Default: NJTRST
PB4	56	I/O	5VT	Alternate: SPI2_MISO ⁽³⁾
				Remap: TIMER2_CH0, PB4, SPI0_MISO
				Default: PB5
PB5	57	I/O		Alternate: I2C0_SMBA, SPI2_MOSI(3), I2S2_SD(3)
				Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX
				Default: PB6
PB6	58	I/O	5VT	Alternate: I2C0_SCL, TIMER3_CH0 ⁽³⁾
				Remap: USART0_TX, CAN1_TX
				Default: PB7
PB7	59	I/O	5VT	Alternate: I2C0_SDA, TIMER3_CH1(3)
				Remap: USART0_RX
воото	60	1		Default: BOOT0
				Default: PB8
PB8	61	I/O	5VT	Alternate: TIMER3_CH2 ⁽³⁾
				Remap: I2C0_SCL, CAN0_RX
				Default: PB9
PB9	62	I/O	5VT	Alternate: TIMER3_CH3 ⁽³⁾
				Remap: I2C0_SDA, CAN0_TX
Vss_3	63	Р		Default: Vss_3
V _{DD_3}	64	Р		Default: V _{DD_3}

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available in GD32VF103R8/B devices.



2.6.3. GD32VF103Cx LQFP48 pin definitions

Table 2-6. GD32VF103Cx LQFP48 pin definitions

Pin Name	Table 2 0. U	V I	.0001	_ 4 70	s pin definitions
PC13-	Pin Name	Pins			Functions description
Default: PC13	V_{BAT}	1	Р		Default: V _{BAT}
OSC32IN 3	TAMPER-	2	I/O		
OSC32OUT 4 I/O Alternate: OSC32OUT OSCIN 5 I Default: OSCIN Remap: PD0 OSCOUT 6 O Default: OSCOUT Remap: PD1 NRST 7 I/O Default: NRST Vssa 8 P Default: Vssa VDDA 9 P Default: Vssa PA0-WKUP 10 I/O Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0_ETI, TIMER4_CH0(3) PA1 11 I/O Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1(3),TIMER1_CH1 PA2 12 I/O Alternate: USART1_TX, TIMER4_CH2(3),ADC01_IN2, TIMER1_CH2 PA3 13 I/O Alternate: USART1_RX, TIMER4_CH3(3), ADC01_IN3, TIMER1_CH3 PA4 14 I/O Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 DAC_OUTO Remap: SPI2_NSS(3), I2S2_WS(3) PA5 15 I/O Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1	_	3	I/O		
OSCIN 5 I Remap: PD0 OSCOUT 6 O Default: OSCOUT Remap: PD1 NRST 7 I/O Default: NRST VssA 8 P Default: VssA VDDA 9 P Default: VDDA PA0-WKUP 10 I/O Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0_ETI, TIMER4_CH0(3) PA1 11 I/O Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1(3), TIMER4_CH1(3), TIMER1_CH1 PA2 12 I/O Alternate: USART1_TX, TIMER4_CH2(3), ADC01_IN2, TIMER1_CH2 PA3 13 I/O Default: PA3 Alternate: USART1_RX, TIMER4_CH3(3), ADC01_IN3, TIMER1_CH3 Default: PA4 PA4 14 I/O Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 DAC_OUT0 Remap: SPI2_NSS(3), I2S2_WS(3) Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1		4	I/O		
OSCOUT 6 O Remap: PD1 NRST 7 I/O Default: NRST VSSA 8 P Default: VSSA VDDA 9 P Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0_ETI, TIMER4_CH0(3) Default: PA1 PA1 11 I/O Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1(3), TIMER1_CH1 Default: PA2 Alternate: USART1_TX, TIMER4_CH2(3), ADC01_IN2, TIMER1_CH2 Default: PA3 Alternate: USART1_RX, TIMER4_CH3(3), ADC01_IN3, TIMER1_CH3 Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 DAC_OUT0 Remap: SPI2_NSS(3), I2S2_WS(3) PA5 15 I/O Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1	OSCIN	5	I		
VSSA 8 P Default: VSSA VDDA 9 P Default: VDDA PA0-WKUP 10 I/O Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0_ETI, TIMER4_CH0(3) PA1 11 I/O Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1(3), TIMER4_CH1 PA2 12 I/O Alternate: USART1_TX, TIMER4_CH2(3), ADC01_IN2, TIMER1_CH2 PA3 13 I/O Alternate: USART1_RX, TIMER4_CH3(3), ADC01_IN3, TIMER1_CH3 PA4 14 I/O Default: PA3	OSCOUT	6	0		
VDDA 9 P Default: VDDA PA0-WKUP 10 I/O Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0_ETI, TIMER4_CH0(3) PA1 11 I/O Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1(3), TIMER1_CH1 PA2 12 I/O Alternate: USART1_TX, TIMER4_CH2(3), ADC01_IN2, TIMER1_CH2 PA3 13 I/O Default: PA3	NRST	7	I/O		Default: NRST
PA0-WKUP 10 I/O Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0_ETI, TIMER4_CH0(3) PA1 11 I/O Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1(3), TIMER1_CH1 PA2 12 I/O Alternate: USART1_TX, TIMER4_CH2(3), ADC01_IN2, TIMER1_CH2 PA3 13 I/O Alternate: USART1_RX, TIMER4_CH3(3), ADC01_IN3, TIMER1_CH3 PA4 14 I/O Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 DAC_OUT0 Remap: SPI2_NSS(3), I2S2_WS(3) PA5 15 I/O Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1	V_{SSA}	8	Р		Default: Vssa
PA0-WKUP 10 I/O Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0_ETI, TIMER4_CH0 ⁽³⁾ PA1 11 I/O Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1 ⁽³⁾ , TIMER1_CH1 PA2 12 I/O Alternate: USART1_TX, TIMER4_CH2 ⁽³⁾ , ADC01_IN2, TIMER1_CH2 PA3 13 I/O Alternate: USART1_RX, TIMER4_CH3 ⁽³⁾ , ADC01_IN3, TIMER1_CH3 PA4 14 I/O Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 DAC_OUT0 Remap: SPI2_NSS ⁽³⁾ , I2S2_WS ⁽³⁾ PA5 15 I/O Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1	V_{DDA}	9	Р		Default: V _{DDA}
PA1 11 I/O Alternate: USART1_RTS, ADC01_IN1, TIMER4_CH1(3), TIMER1_CH1 PA2 12 I/O Default: PA2	PA0-WKUP	10	I/O		Alternate: WKUP, USART1_CTS, ADC01_IN0,
PA2 12 I/O Alternate: USART1_TX, TIMER4_CH2 ⁽³⁾ ,ADC01_IN2, TIMER1_CH2 PA3 13 I/O Default: PA3 Alternate: USART1_RX, TIMER4_CH3 ⁽³⁾ , ADC01_IN3, TIMER1_CH3 PA4 14 I/O Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 DAC_OUT0 Remap: SPI2_NSS ⁽³⁾ , I2S2_WS ⁽³⁾ PA5 15 I/O Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1	PA1	11	I/O		Alternate: USART1_RTS, ADC01_IN1,
PA3 13 I/O Alternate: USART1_RX, TIMER4_CH3 ⁽³⁾ , ADC01_IN3, TIMER1_CH3 PA4 14 I/O Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 DAC_OUT0 Remap: SPI2_NSS ⁽³⁾ , I2S2_WS ⁽³⁾ PA5 15 I/O Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1	PA2	12	I/O		Alternate: USART1_TX, TIMER4_CH2 ⁽³⁾ ,ADC01_IN2,
PA4 14 I/O Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 DAC_OUT0 Remap: SPI2_NSS ⁽³⁾ , I2S2_WS ⁽³⁾ PA5 15 I/O Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1	PA3	13	I/O		Alternate: USART1_RX, TIMER4_CH3 ⁽³⁾ , ADC01_IN3,
PA5 15 I/O Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1	PA4	14	I/O		Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 DAC_OUT0
PA6 16 I/O Default: PA6	PA5	15	I/O		
	PA6	16	I/O		Default: PA6



Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
				Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0
				Remap: TIMER0_BRKIN
				Default: PA7
PA7	17	I/O		Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1
				Remap: TIMER0_CH0_ON
		I/O		Default: PB0
PB0	18			Alternate: ADC01_IN8, TIMER2_CH2
				Remap: TIMER0_CH1_ON
				Default: PB1
PB1	19	I/O		Alternate: ADC01_IN9, TIMER2_CH3
				Remap: TIMER0_CH2_ON
PB2	20	I/O	5VT	Default: PB2, BOOT1
				Default: PB10
PB10	21	I/O	5VT	Alternate: I2C1_SCL ⁽³⁾ , USART2_TX ⁽³⁾
				Remap: TIMER1_CH2
		I/O		Default: PB11
PB11	22		5VT	Alternate: I2C1_SDA ⁽³⁾ , USART2_RX ⁽³⁾
				Remap: TIMER1_CH3
Vss_1	23	Р		Default: Vss_1
V_{DD_1}	24	Р		Default: V _{DD_1}
		I/O	5VT	Default: PB12
PB12	25			Alternate: SPI1_NSS ⁽³⁾ , I2S1_WS ⁽³⁾ , I2C1_SMBA ⁽³⁾ ,
				USART2_CK ⁽³⁾ , TIMER0_BRKIN, CAN1_RX
		I/O	5VT	Default: PB13
PB13	26			Alternate: SPI1_SCK ⁽³⁾ , I2S1_CK ⁽³⁾ , USART2_CTS ⁽³⁾ ,
				TIMER0_CH0_ON, CAN1_TX
	27	I/O	5VT	Default: PB14
PB14				Alternate: SPI1_MISO ⁽³⁾ , USART2_RTS ⁽³⁾ ,
				TIMER0_CH1_ON
PB15	28	I/O	5VT	Default: PB15
				Alternate: SPI1_MOSI ⁽³⁾ , TIMER0_CH2_ON, I2S1_SD ⁽³⁾
		I/O	5VT	Default: PA8
PA8	29			Alternate: USART0_CK, TIMER0_CH0, CK_OUT0,
				USBFS_SOF
PA9	30	I/O	5VT	Default: PA9
				Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	31			Default: PA10
			-	Alternate: USART0_RX, TIMER0_CH2, USBFS_ID
PA11	32	I/O	5VT	Default: PA11
				Alternate: USART0_CTS, CAN0_RX, TIMER0_CH3,



Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
				USBFS_DM
				Default: PA12
PA12	33	I/O	5VT	Alternate: USART0_RTS, CAN0_TX, TIMER0_ETI,
				USBFS_DP
PA13	34	I/O	5VT	Default: JTMS
TAIS	57	1/0	3 7 1	Remap: PA13
V_{SS_2}	35	Р		Default: V _{SS_2}
V_{DD_2}	36	Р		Default: V _{DD_2}
PA14	37	I/O	E\/T	Default: JTCK
PA14	31	1/0	5VT	Remap: PA14
				Default: JTDI
PA15	38	I/O	5VT	Alternate:SPI2_NSS ⁽³⁾ , I2S2_WS ⁽³⁾
				Remap: TIMER1_CH0 _ETI, PA15, SPI0_NSS
		I/O	5VT	Default: JTDO
PB3	39			Alternate:SPI2_SCK ⁽³⁾ ,I2S2_CK ⁽³⁾
				Remap: PB3, TIMER1_CH1, SPI0_SCK
		I/O	5VT	Default: NJTRST
PB4	40			Alternate:SPI2_MISO ⁽³⁾
				Remap: TIMER2_CH0, PB4, SPI0_MISO
	41	I/O		Default: PB5
PB5				Alternate: I2C0_SMBA ,SP12_MOSI(3), I2S2_SD(3)
				Remap: TIMER2_CH1, SPI0_MOSI,CAN1_RX
			5VT	Default: PB6
PB6	42	I/O		Alternate: I2C0_SCL, TIMER3_CH0 ⁽³⁾
				Remap: USART0_TX,CAN1_TX
	43	I/O	5VT	Default: PB7
PB7				Alternate: I2C0_SDA , TIMER3_CH1(3)
				Remap: USART0_RX
воото	44	[Default: BOOT0
PB8	45	I/O	5VT	Default: PB8
				Alternate: TIMER3_CH2 ⁽³⁾
				Remap: I2C0_SCL, CAN0_RX
PB9	46	I/O	5VT	Default: PB9
				Alternate: TIMER3_CH3 ⁽³⁾
				Remap: I2C0_SDA, CAN0_TX
V _{SS_3}	47	Р		Default: V _{SS_3}
V _{DD_3}	48	Р		Default: V _{DD_3}

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.



(3) Functions are available in GD32VF103C8/B devices.



2.6.4. GD32VF103Tx QFN36 pin definitions

Table 2-7. GD32VF103Tx QFN36 pin definitions

Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
OSCIN	2	I		Default: OSCIN Remap: PD0
OSCOUT	3	0		Default: OSCOUT Remap: PD1
NRST	4	I/O		Default: NRST
V _{SSA}	5	Р		Default: V _{SSA}
V _{DDA}	6	Р		Default: V _{DDA}
PA0-WKUP	7	I/O		Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0_ETI,TIMER4_CH0 ⁽³⁾
PA1	8	I/O		Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER1_CH1, TIMER4_CH1 ⁽³⁾
PA2	9	I/O		Default: PA2 Alternate: USART1_TX, ADC01_IN2, TIMER1_CH2, TIMER4_CH2 ⁽³⁾
PA3	10	I/O		Default: PA3 Alternate: USART1_RX, ADC01_IN3, TIMER1_CH3, TIMER4_CH3 ⁽³⁾
PA4	11	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4, DAC_OUT0
PA5	12	I/O		Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	13	I/O		Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BRKIN
PA7	14	I/O		Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1 Remap: TIMER0_CH0_ON
PB0	15	I/O		Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2 Remap: TIMER0_CH1_ON
PB1	16	I/O		Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3 Remap: TIMER0_CH2_ON



Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
PB2	17	I/O	5VT	Default: PB2,BOOT1
V_{SS_1}	18	Р		Default: V _{SS_1}
V_{DD_1}	19	Р		Default: V _{DD_1}
				Default: PA8
PA8	20	I/O	5VT	Alternate: USART0_CK, TIMER0_CH0, CK_OUT0,
				USBFS_SOF
PA9	21	I/O	5VT	Default: PA9
FA9	21	1/0		Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	22	I/O	5VT	Default: PA10
PAIU	22	1/0	371	Alternate: USART0_RX, TIMER0_CH2, USBFS_ID
				Default: PA11
PA11	23	I/O	5VT	Alternate: USART0_CTS, CAN0_RX, TIMER0_CH3,
				USBFS_DM
			5VT	Default: PA12
PA12	24	I/O		Alternate: USART0_RTS, CAN0_TX, TIMER0_ETI,
				USBFS_DP
DA40	25	I/O	5VT	Default: JTMS
PA13	25			Remap: PA13
V _{SS_2}	26	Р		Default: V _{SS_2}
V _{DD_2}	27	Р		Default: V _{DD_2}
DA44	20	I/O	5VT	Default: JTCK
PA14	28			Remap: PA14
PA15	29	9 1/0	5VT	Default: JTDI
PAIS	29			Remap: TIMER1_CH0 _ETI, PA15, SPI0_NSS
PB3	20	I/O	5VT	Default: JTDO
PB3	30			Remap: PB3, TIMER1_CH1, SPI0_SCK
DD4	21	I/O	5VT	Default: NJTRST
PB4	31			Remap: TIMER2_CH0, PB4, SPI0_MISO
		I/O		Default: PB5
PB5	32			Alternate: I2C0_SMBA
				Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX
		I/O	5VT	Default: PB6
PB6	33			Alternate: I2C0_SCL, TIMER3_CH0 ⁽³⁾
				Remap: USART0_TX, CAN1_TX
		I/O		Default: PB7
PB7	34			Alternate: I2C0_SDA, TIMER3_CH1(3)
				Remap: USART0_RX
воото	35	I		Default: BOOT0
V _{SS_3}	36	Р		Default: V _{SS_3}



Pin Name	Pins	Pin Type ⁽¹⁾	I/O Level ⁽²⁾	Functions description
V_{DD_3}	1	Р		Default: V _{DD_3}

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available in GD32VF103T8/B devices.



3. Functional description

3.1. System and memory architecture

The devices of GD32VF103 series are 32-bit general-purpose microcontrollers based on the 32bit RISC-V processor. The RISC-V processor includes three AHB buses known as I-Code, D-Code and System buses. All memory accesses of the RISC-V processor are executed on the three buses according to the different purposes and the target memory spaces. The memory organization uses a Harvard architecture, pre-defined memory map and up to 4 GB of memory space, making the system flexible and extendable.

3.2. On-chip memory

- Up to 128 Kbytes of Flash memory
- All memory region of the MCU executes instructions without waiting time
- 32 Kbytes of SRAM

The RISC-V processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 128 Kbytes of inner Flash at most, which includes code Flash and data Flash, is available for storing programs and data, and there is no waiting time within code Flash area when CPU executes instructions. The <u>Table 2-3. GD32VF103</u> <u>memory map</u> shows the memory map of the GD32VF103 series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 3 to 25 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control unit provides a range of frequencies and clock functions. These include an Internal 8M RC oscillator (IRC8M), a High Speed crystal oscillator (HXTAL), a Low Speed Internal 40K RC oscillator (IRC40K), a Low Speed crystal oscillator (LXTAL), a Phase Lock Loop (PLL), a HXTAL clock monitor, clock prescalers, clock multiplexers and clock gating circuitry. The frequency of AHB, APB2 and the APB1 domains can be configured by each prescaler. The maximum frequency of the AHB, APB2 and APB1 domains is 108 MHz/108 MHz/54 MHz. See *Figure 2-6. GD32VF103 clock tree* for details.

GD32VF103 Reset Control includes the control of three kinds of reset: power reset, system



reset and backup domain reset. The system reset resets the processor core and peripheral IP components except for the JTAG-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART1 (PD5 and PD6), USBFS in device mode (PA9, PA11 and PA12). It also can be used to transfer and update the Flash memory code, the data and the vector table sections.



3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

■ Sleep mode

In sleep mode, only clock of core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

■ **Deep-sleep** mode

In deep-sleep mode, all clocks in the 1.2V domain are off, and all of IRC8M, HXTAL and PLLs are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm/ time stamp/ tamper, the LVD output, USB Wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

■ Standby mode

In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLLs are disabled. The contents of SRAM and registers (except Backup registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm/ time stamp/ tamper, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC engine with up to 1MSPS conversion rate
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Conversion range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

Up to two 12-bit 1MSPS multi-channel ADCs are integrated in the device. Each is a total of up to 16 multiplexed external channels with 2 internal channels for temperature sensor and voltage reference measurement. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages.

The ADCs can be triggered from the events generated by the general level 0 timers (TIMERx=1,2,3) and the advanced timers (TIMER0) with internal connection. The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2.6 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.



To ensure a high accuracy on ADC and DAC, the ADC/DAC independent external reference voltage should be connected to V_{REF+}/V_{REF-} pins. According to the different packages, V_{REF+} pin can be connected to V_{DDA} pin, or external reference voltage, V_{REF-} pin must be connected to V_{SSA} pin. The V_{REF+} pin is only available on no less than 100-pin packages, or else the V_{REF+} pin is not available and internally connected to V_{DDA} . The V_{REF-} pin is only available on no less than 100-pin packages, or else the V_{REF-} pin is not available and internally connected to V_{SSA} .

3.7. Digital to analog converter (DAC)

- Two 12-bit DAC converters of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The two 12-bit buffered DAC channels are used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer TRGO outputs or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is VREF+.

3.8. DMA

- 7 channel DMA0 controller and 5 channel DMA1 controller
- Peripherals supported: TIMERs, ADC, SPIs, I2Cs, USARTs, DAC, I2S

The direct memory access (DMA) controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. General-purpose inputs/outputs (GPIOs)

- Up to 80 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 80 general purpose I/O pins (GPIO), named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15 for the device to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupt on the GPIO pins of the device have related control and configuration registers in the Interrupt/event Controller Unit (EXTI). The GPIO



ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the AF input or output pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Each GPIO pin can be configured as pull-up, pull-down or no pull-up/pull-down. All GPIOs are high-current capable except for analog mode.

3.10. Timers and PWM generation

- Up to one 16-bit advanced timer (TIMER0), four 16-bit general timers(TIMERx=1,2,3,4), and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 64-bit SysTick timer up counter
- 2 watchdog timers (Free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge-aligned or center-aligned counting modes)
- Single pulse mode output

If configured as a general 16-bit timer, it can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, known as TIMERx=1,2,3,4 can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 and TIMER6 are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32VF103 have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and a 3-bit prescaler, it is clocked from an independent 40 KHz internal RC and as it operates independently of the



main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard up counter. The features are shown below:

- A 64-bit up counter
- Maskable system interrupt generation when the counter and comparison values are equal
- Programmable clock source

3.11. Real time clock (RTC)

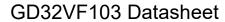
- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.12. Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 400 KHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to





transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.



3.13. Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 27 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14. Universal synchronous asynchronous receiver transmitter (USART)

- Up to three USARTs and two UARTs with operating frequency up to 6.75 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- USARTs support ISO 7816-3 compliant smart card interface

The USART (USART0, USART1 and USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication except UART4.

3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32VF103 contain two I2S-bus interfaces that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequency from 8 KHz to 192 KHz is supported with less than 0.5% accuracy error.



3.16. Universal serial bus full-speed (USBFS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers in device/host/OTG mode. Full-speed peripheral is compliant with the USB 2.0 specification. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HXTAL crystal oscillator) and the operating frequency divided from APB1 should be 12 MHz above.

3.17. Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for USB CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

3.18. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash
- Up to 16-bit data bus
- Support to interface with Motorola 6800 and Intel 8080 type LCD directly

External memory controller (EXMC) is an abbreviation of external memory controller. It has one bank for external device support. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.19. Debug mode

- Support standard JTAG debugging interface and mature interactive debugging tool GDB
- Support up to four hardware breakpoints



The RISC-V Core does not support trace debugging. Hardware breakpoints are mainly used to set breakpoints at read-only sections (such as Flash).

3.20. Package and operation temperature

- LQFP100 (GD32VF103Vx), LQFP64 (GD32VF103Rx), LQFP48 (GD32VF103Cx), QFN36 (GD32VF103Tx)
- Operation temperature range: -40°C to +85°C (industrial level)



4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings(1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range ⁽²⁾	V _{SS} - 0.3	V _{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V _{SSA} - 0.3	V _{SSA} + 3.6	V
V _{BAT}	External battery supply voltage	V _{SS} - 0.3	V _{SS} + 3.6	V
Vin	Input voltage on 5V tolerant pin ⁽³⁾	V _{SS} - 0.3	$V_{DD} + 3.6$	V
VIN	Input voltage on other I/O	V _{SS} - 0.3	3.6	V
AVDDX	Variations between different V _{DD} power pins	_	50	mV
Vssx -Vss	Variations between different ground pins	_	50	mV
lio	Maximum current for GPIO pins	_	±25	mA
TA	Operating temperature range	-40	+85	°C
	Power dissipation at T _A = 85°C of LQFP100	_	697	
P _D	Power dissipation at T _A = 85°C of LQFP64	_	647	mW
FD	Power dissipation at T _A = 85°C of LQFP48	_	621	IIIVV
	Power dissipation at T _A = 85°C of QFN36	_	926	
T _{STG}	Storage temperature range	-65	+150	°C
TJ	Maximum junction temperature	_	125	°C

⁽¹⁾ Guaranteed by design, not tested in production.

4.2. Operating conditions characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
V_{DD}	Supply voltage	_	2.6	3.3	3.6	V
V _{DDA}	Analog supply voltage	Same as V _{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	_	1.8	_	3.6	V

⁽¹⁾ Based on characterization, not tested in production.

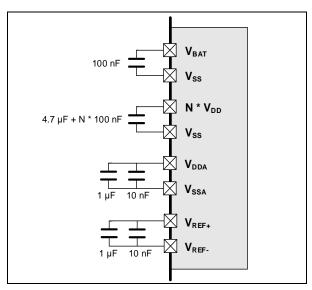
⁽²⁾ All main power and ground pins should be connected to an external power source within the allowable range.

⁽³⁾ V_{IN} maximum value cannot exceed 5.5 V.

⁽⁴⁾ It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.



Figure 4-1. Recommended power supply decoupling capacitors (1)(2)



- (1) The V_{REF+} and V_{REF-} pins are only available on no less than 100-pin packages, or else the V_{REF+} and V_{REF-} pins are not available and internally connected to V_{DDA} and V_{SSA} pins.
- (2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency⁽¹⁾

Symbol Parameter		Conditions	Min	Max	Unit
f _{HCLK}	AHB clock frequency	_		108	MHz
f _{APB1}	APB1 clock frequency	_	_	54	MHz
f _{APB2}	APB2 clock frequency		_	108	MHz

⁽¹⁾ Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down⁽¹⁾

Symbol Parameter		Conditions	Min	Max	Unit
t	V _{DD} rise time rate		0	8	us/V
t∨DD	V_{DD} fall time rate	_	20	8	μ5/ ν

⁽¹⁾ Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions (1)(2)(3)

Symbol	Parameter	Conditions	Тур	Unit
	Start up timo	Clock source from HXTAL	132	mo
Tstart-up	Start-up time	Clock source from IRC8M	132	ms

- (1) Based on characterization, not tested in production.
- (2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.
- (3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics⁽¹⁾⁽²⁾

Symbol	ymbol Parameter			
t _{Sleep}	t _{Sleep} Wakeup from Sleep mode			
4_	Wakeup from Deep-sleep mode (LDO On)	6.0	μs	
I Deep-sleep	Wakeup from Deep-sleep mode (LDO in low power mode)	6.0		
t _{Standby}	Wakeup from Standby mode	118.8	ms	



- (1) Based on characterization, not tested in production.
- (2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: $V_{DD} = V_{DDA} = 3.3 \text{ V}$, IRC8M = System clock = 8 MHz.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics (2)(3)(4)(5)

Symbol Parameter Conditions		Conditions	Min	Typ ⁽¹⁾	Max	Unit
		$V_{DD} = V_{DDA} = 3.3 \text{ V, HXTAL} = 25 \text{ MHz,}$				
		System clock = 108 MHz, All peripherals		35.00	_	mA
		enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
		System clock = 108 MHz, All peripherals	_	20.05	_	mΑ
		disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{ HXTAL} = 25 \text{ MHz},$				
		System clock = 96 MHz, All peripherals	_	32.30	_	mΑ
		enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
		System clock = 96 MHz, All peripherals	_	18.90	_	mA
		disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
	Supply current (Run mode)	System clock = 72 MHz, All peripherals	_	23.50	_	mΑ
		enabled				
I _{DD} +I _{DDA}		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
IDDTIDDA		System clock = 72 MHz, All peripherals	_	13.40	_	mA
		disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
		System clock = 48 MHz, All peripherals	_	16.60	_	mΑ
		enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{ HXTAL} = 25 \text{ MHz},$				
		System clock = 48 MHz, All peripherals	_	9.90	_	mΑ
		disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
		System clock =36 MHz, All peripherals	_	13.10	_	mΑ
		enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
		System clock = 36 MHz, All peripherals	_	8.10	_	mA
		disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{ HXTAL} = 25 \text{ MHz},$	_	9.80	_	mA
		System clock = 24 MHz, All peripherals		3.00	_	111/5



			ט טע			
Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Unit
		enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
		System clock = 24 MHz, All peripherals	_	6.50	_	mA
		disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
		System clock = 16 MHz, All peripherals	_	7.60	_	mA
		enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
		System clock = 16 MHz, All peripherals	_	5.30	_	mA
		disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{HXTAL} = 25 \text{ MHz},$				
		System clock = 8 MHz, All peripherals	_	5.30	_	mA
		enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V, HXTAL} = 25 \text{ MHz,}$				
		System clock = 8 MHz, All peripherals	_	4.10	_	mA
		disabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 4 MHz,				
		System clock = 4 MHz, All peripherals	_	1.80	_	mA
		enabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 4 MHz,				
		System clock = 4 MHz, All peripherals	_	1.30	_	mA
		disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V, HXTAL} = 2 \text{ MHz,}$				
		System clock = 2 MHz, All peripherals	_	1.30	_	mA
		enabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 2 MHz,				
		System clock = 2 MHz, All peripherals	_	1.00	_	mA
		disabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 25 MHz,				
		System Clock = 108 MHz, CPU clock off,	_	26.20	_	mA
		All peripherals enabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 25 MHz,				
		System Clock = 108 MHz, CPU clock off,	_	11.35	_	mA
		All peripherals disabled				
	Supply current	V _{DD} = V _{DDA} = 3.3 V, HXTAL = 25 MHz,				
	(Sleep mode)	System Clock = 96 MHz, CPU clock off, All	_	24.10	_	mA
		peripherals enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V, HXTAL} = 25 \text{ MHz,}$				
		System Clock = 96 MHz, CPU clock off, All	_	10.70	_	mA
		peripherals disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V, HXTAL} = 25 \text{ MHz,}$	_	18.70	_	mA
	l .	. 55 . 55A . 510 Y, 177.171E - 20 WII 12,		. 5.7 0		\



	GD32 V			,	atao	1100
Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Unit
		System Clock = 72 MHz, CPU clock off, All				
		peripherals enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{ HXTAL} = 25 \text{ MHz},$				
		System Clock = 72 MHz, CPU clock off, All	_	8.70	_	mA
		peripherals disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V, HXTAL} = 25 \text{ MHz,}$				
		System Clock = 48 MHz, CPU clock off, All	_	13.40	_	mA
		peripherals enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V, HXTAL} = 25 \text{ MHz,}$				
		System Clock = 48 MHz, CPU clock off, All	_	6.70	_	mA
		peripherals disabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 25 MHz,				
		System Clock = 36 MHz, CPU clock off, All	_	1.80	_	mA
		peripherals enabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 25 MHz,				
		System Clock = 36 MHz, CPU clock off, All	_	5.70	_	mA
		peripherals disabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 25 MHz,				
		System Clock = 24 MHz, CPU clock off, All	_	8.30	_	mA
		peripherals enabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 25 MHz,				
		System Clock = 24 MHz, CPU clock off, All	_	4.90	_	mA
		peripherals disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V, HXTAL} = 25 \text{ MHz,}$				
		System Clock = 16 MHz, CPU clock off, All	_	6.50	_	mA
		peripherals enabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 25 MHz,				
		System Clock = 16 MHz, CPU clock off, All	_	4.30	_	mA
		peripherals disabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 25 MHz,				
		System Clock = 8 MHz, CPU clock off, All	_	4.70	_	mA
		peripherals enabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V, HXTAL} = 25 \text{ MHz,}$				
		System Clock = 8 MHz, CPU clock off, All	_	3.60	_	mA
		peripherals disabled		0.00		
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 4 MHz,				
		System Clock = 4 MHz, CPU clock off, All	_	1.40	_	mA
		peripherals enabled		1.40		'''' \
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 4 MHz,				
		System Clock = 4 MHz, CPU clock off, All		0.90		mA
			_	0.90	_	11174
		peripherals disabled				



Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Unit
_		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 2 MHz,				
		System Clock = 2 MHz, CPU clock off, All	_	1.00	_	mA
		peripherals enabled				
		V _{DD} = V _{DDA} = 3.3 V, HXTAL = 2 MHz,				
		System Clock = 2 MHz, CPU clock off, All	_	0.70	_	mA
		peripherals disabled				
		$V_{DD} = V_{DDA} = 3.3 \text{ V, LDO in normal power}$		460.0		
	Supply current	and normal driver mode, IRC40K off, RTC	_	0	2200	μΑ
		off, All GPIOs analog mode				
, ,	(Deep-Sleep mode)	$V_{DD} = V_{DDA} = 3.3 \text{ V}$, LDO in normal power		427.5		
	mode)	and low driver mode, IRC40K off, RTC off,	_	0	2200	μΑ
		All GPIOs analog mode				
		$V_{DD} = V_{DDA} = 3.3 \text{ V}, \text{LDO off, LXTAL off,}$		7.00	00	
		IRC40K on, RTC on	_	7.62	22	μΑ
	Supply current	V _{DD} = V _{DDA} = 3.3 V, LDO off, LXTAL off,				
	(Standby mode)	IRC40K on, RTC off	_	7.49	22	μA
		V _{DD} = V _{DDA} = 3.3 V, LDO off, LXTAL off,		0.00	00	^
		IRC40K off, RTC off	_	6.32	22	μA
		V _{DD} off, V _{DDA} off, V _{BAT} = 3.6 V, LXTAL on		2.18		μA
	Rattery supply	with external crystal, RTC on		2.10		μΑ
I _{BAT}	Battery supply current (Backup	V _{DD} off, V _{DDA} off, V _{BAT} = 3.3 V, LXTAL on		2.10		μΑ
IBAT	mode)	with external crystal, RTC on		2.10		μΑ
	illoue)	V _{DD} off, V _{DDA} off, V _{BAT} = 2.6 V, LXTAL on		1.97		μΑ
		with external crystal, RTC on		1.07		μΛ

⁽¹⁾ Based on characterization, not tested in production.

⁽²⁾ Unless otherwise specified, all values given for $T_A = 25$ °C and test result is mean value.

⁽³⁾ When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed,

⁽⁴⁾ When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

⁽⁵⁾ When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.



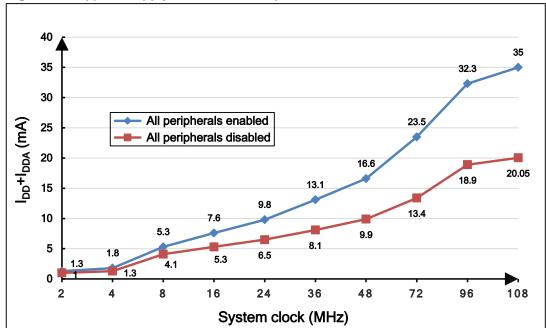
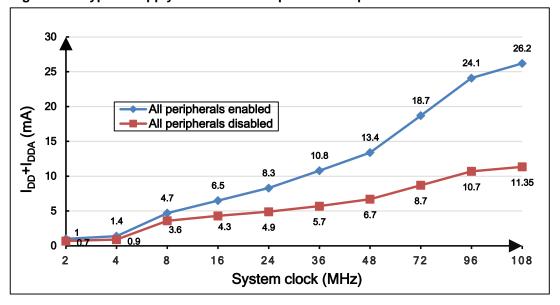


Figure 4-2. Typical supply current consumption in Run mode





4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the <u>Table 4-8. EMS characteristics</u>, based on the EMS levels and classes compliant with IEC 61000 series standard.



Table 4-8. EMS characteristics⁽¹⁾

Symbol	Parameter	Conditions	Level/Class
	Voltage applied to all device pine to	V_{DD} = 3.3 V, T_{A} = 25 °C	
VESD	Voltage applied to all device pins to	LQFP100, f _{HCLK} = 108 MHz	ЗА
	induce a functional disturbance	conforms to IEC 61000-4-2	
	Fast transient voltage burst applied to	V _{DD} = 3.3 V, T _A = 25 °C	
V _{FTB}	induce a functional disturbance through	LQFP100, f _{HCLK} = 108 MHz	4A
	100 pF on V_{DD} and V_{SS} pins	conforms to IEC 61000-4-2	

⁽¹⁾ Based on characterization, not tested in production

4.5. Power supply supervisor characteristics

Table 4-9. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		LVDT<2:0> = 000(rising edge)		2.18		
		LVDT<2:0> = 000(falling edge)	-	2.08		
		LVDT<2:0> = 001(rising edge)	_	2.29	_	
		LVDT<2:0> = 001(falling edge)	_	2.19	_	
		LVDT<2:0> = 010(rising edge)	_	2.38	_	
V _{LVD} ⁽¹⁾		LVDT<2:0> = 010(falling edge)	_	2.28	_	
		LVDT<2:0> = 011(rising edge)	_	2.49	_	
	Low voltage Detector level selection	LVDT<2:0> = 011(falling edge)	_	2.38	_	
VLVD('')		LVDT<2:0> = 100(rising edge)	_	2.58	_	V
		LVDT<2:0> = 100(falling edge)	_	2.48	_	
		LVDT<2:0> = 101(rising edge)	_	2.68	_	
		LVDT<2:0> = 101(falling edge)	_	2.58	_	
		LVDT<2:0> = 110(rising edge)	_	2.78	_	
		LVDT<2:0> = 110(falling edge)	_	2.68	_	
		LVDT<2:0> = 111(rising edge)	_	2.88	_	
		LVDT<2:0> = 111(falling edge)	_	2.78	_	
V _{LVDhyst} ⁽²⁾	LVD hystersis	_	_	100	_	mV
V _{POR} ⁽¹⁾	Power on reset threshold		_	2.44	_	V
V _{PDR} ⁽¹⁾	Power down reset			1.86	_	V



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	threshold					
V _{PDRhyst} ⁽²⁾	PDR hysteresis		_	600	_	mV
trsttempo ⁽²⁾	Reset temporization		_	2	_	ms

⁽¹⁾ Based on characterization, not tested in production

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-10. ESD characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
\/	Electrostatic discharge	T _A = 25 °C;			5000	V
VESD(HBM)	voltage (human body model)	JESD22-A114		_	5000	V
V _{ESD(CDM)}	Electrostatic discharge	T _A = 25 °C;			500	.,
	voltage (charge device model)	e device model) JESD22-C101		_	500	V

⁽¹⁾ Based on characterization, not tested in production.

Table 4-11. Static latch-up characteristics(1)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
111	I-test	T _A = 25 °C; JESD78			±200	mA
LU	V _{supply} over voltage	1A = 23 O, JESD16			5.4	V

⁽¹⁾ Based on characterization, not tested in production.

4.7. External clock characteristics

Table 4-12. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

⁽²⁾ Guaranteed by design, not tested in production



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HXTAL} ⁽¹⁾	Crystal or ceramic frequency	$2.6 \text{ V} \le \text{V}_{DD} \le 3.6 \text{ V}$	3	8	25	MHz
R _F ⁽²⁾	Feedback resistor	$V_{DD} = 3.3 \text{ V}$	_	400	_	kΩ
	Recommended matching					
C _{HXTAL} ⁽²⁾⁽³⁾	capacitance on OSCIN and	_	_	20	30	pF
	OSCOUT					
Ducy _(HXTAL) ⁽²⁾	Crystal or ceramic duty cycle	_	48	50	52	%
g _m (2)	Oscillator transconductance	Startup	_	35	_	mA/V
	Crystal or coromic aparating	V_{DD} = 3.3 V, f_{HCLK} =				
I _{DDHXTAL} ⁽¹⁾	Crystal or ceramic operating current	$f_{IRC8M} = 8 MHz$	_	1.4	_	mA
	current	T _A = 25 °C				
		V_{DD} = 3.3 V, f_{HCLK} =				
t _{SUHXTAL} (1)	Crystal or ceramic startup time	$f_{IRC8M} = 8 \text{ MHz}$	_	1.8	_	ms
		T _A = 25 °C				

⁽¹⁾ Based on characterization, not tested in production.

Table 4-13. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HXTAL_ext} (1)	External clock source or oscillator	V _{DD} = 3.3 V	1		50	MHz
THXTAL_ext\''	frequency	VDD - 3.3 V		_	30	IVIITZ
V _{HXTALH} ⁽²⁾	OSCIN input pin high level		0.7 Vpp		V _{DD}	V
	voltage V _{DD} = 3.		0.7 VDD	_	V DD	V
V _{HXTALL} ⁽²⁾	OSCIN input pin low level voltage		Vss	_	$0.3 V_{DD}$	V
t _{H/L(HXTAL)} (2)	OSCIN high or low time	_	5	_	_	ns
t _{R/F(HXTAL)} (2)	OSCIN rise or fall time	_	_	_	10	ns
C _{IN} ⁽²⁾	OSCIN input capacitance	_	1	5	_	pF
Ducy _(HXTAL) (2)	Duty cycle	_	40	_	60	%

⁽¹⁾ Based on characterization, not tested in production.

Table 4-14. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{LXTAL} (1)	Crystal or ceramic frequency	V _{DD} = 3.3 V	_	32.768		kHz
	Recommended matching					
C _{LXTAL} ^{(2) (3)}	capacitance on OSC32IN and	_	_	10	20	pF
	OSC32OUT					
Ducy _(LXTAL) (2)	Crystal or ceramic duty cycle	_	48	50	52	%
g _m (2)	Oscillator transconductance		_	11	_	μA/V
IDDLXTAL (1)	Crystal or ceramic operating			1.07		
	current	_	_	1.97	_	μΑ

⁽²⁾ Guaranteed by design, not tested in production.

⁽³⁾ $C_{\text{HXTAL1}} = C_{\text{HXTAL2}} = 2*(C_{\text{LOAD}} - C_{\text{S}})$, For C_{HXTAL1} and C_{HXTAL2} , it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD} , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_{S} , it is PCB and MCU pin stray capacitance.

⁽²⁾ Guaranteed by design, not tested in production.

tsulxtal ⁽¹	(4)	Crystal or ceramic startup time	_	_	1.8	_	s	
------------------------	-----	---------------------------------	---	---	-----	---	---	--

- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.
- (3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} C_S)$, For C_{LXTAL1} and C_{LXTAL2} , it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD} , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S , it is PCB and MCU pin stray capacitance.
- (4) tsulxtal is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-15. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{LXTAL_ext} (1)	External clock source or oscillator	V _{DD} = 3.3 V		32.768	1000	kHz
ILX IAL_ext\ /	frequency	י טט – טט ס		32.700	1000	KI IZ
V _{LXTALH} (2)	OSC32IN input pin high level		0.7 Vpp		V _{DD}	
VLXIALH\-/	voltage	_	U.7 VDD	_	V DD	V
V _{I XTALI} (2)	OSC32IN input pin low level		Vss		0.3 V _{DD}	V
VLXTALL(=/	voltage	1	VSS		U.S VDD	
t _{H/L(LXTAL)} (2)	OSC32IN high or low time		450	_	_	50
t _{R/F(LXTAL)} (2)	OSC32IN rise or fall time	_	_	_	50	ns
C _{IN} ⁽²⁾	OSC32IN input capacitance	_	_	5	_	pF
Ducy _(LXTAL) (2)	Duty cycle	_	30	50	70	%

- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-16. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	High Speed Internal					
f _{IRC8M}	Oscillator (IRC8M)	$V_{DD} = V_{DDA} = 3.3 \text{ V}$	_	8	_	MHz
	frequency					
		$V_{DD} = V_{DDA} = 3.3 V$	-2.5		+1.5	%
	IDCOM appillator Fraguency	$T_A = -40^{\circ}C \sim +85^{\circ}C^{(1)}$	-2.5		+1.5	70
400	IRC8M oscillator Frequency	$V_{DD} = V_{DDA} = 3.3 \text{ V},$	1.0		+1.2	%
	accuracy, Factory-trimmed	$T_A = 0^{\circ}C \sim +85 {\circ}C^{(1)}$	-1.2		+1.2	70
ACC _{IRC8M}		$V_{DD} = V_{DDA} = 3.3 \text{ V}, T_A = 25 ^{\circ}\text{C}$	-1	_	+1	%
	IRC8M oscillator Frequency					
	accuracy, User trimming	_	_	0.5	_	%
	step ⁽¹⁾					
Ducy _{IRC8M} (2)	IRC8M oscillator duty cycle	$V_{DD} = V_{DDA} = 3.3 \text{ V}$	48	50	52	%
I _{DDAIRC8M} ⁽¹⁾	IRC8M oscillator operating	$V_{DD} = V_{DDA} = 3.3 \text{ V},$		00		
IDDAIRC8M(1)	current	f _{HCLK} = f _{HXTAL_PLL} = 108 MHz		80	_	μA
. (1)	IRC8M oscillator startup	$V_{DD} = V_{DDA} = 3.3 \text{ V},$		0		
tsuirc8m ⁽¹⁾	time	f _{HCLK} = f _{HXTAL_PLL} = 108 MHz		2	_	μs



- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.

Table 4-17. Low speed internal clock (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{IRC40K} ⁽¹⁾	Low Speed Internal oscillator (IRC40K) frequency	$V_{DD} = V_{DDA} = 3.3 \text{ V},$ $T_A = -40 \text{ °C} \sim +85 \text{ °C}$	30	40	60	kHz
I _{DDAIRC40K} ⁽²⁾	IRC40K oscillator operating current	$V_{DD} = V_{DDA} = 3.3 \text{ V},$ $f_{HCLK} = f_{HXTAL_PLL} = 108 \text{ MHz}$ $T_A = 25 \text{ °C}$	_	2	_	μА
t _{SUIRC40K} ⁽²⁾	IRC40K oscillator startup	$V_{DD} = V_{DDA} = 3.3 \text{ V},$ $f_{HCLK} = f_{HXTAL_PLL} = 108 \text{ MHz}$ $T_A = 25 \text{ °C}$	_	100	_	μs

⁽¹⁾ Guaranteed by design, not tested in production.

4.9. PLL characteristics

Table 4-18. PLL characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{PLLIN} ⁽¹⁾	PLL input clock frequency	_	1	_	25	MHz
f _{PLLOUT} (2)	PLL output clock frequency	_	16	_	108	MHz
f _{VCO} (2)	PLL VCO output clock		32			MHz
TVCO.	frequency	_	52	_		IVI⊓Z
t _{LOCK} (2)	PLL lock time	_	_	_	400	μs
I _{DDA} ⁽¹⁾⁽³⁾	Current consumption on	VCO freq = 216 MHz	— 906	006		
IDDA	V_{DDA}	VCO IIeq - 210 WI12		900		μΑ
	Cycle to cycle Jitter			35		
litterpu (1)(4)	(rms)	System clock		33		ne
Jitter _{PLL} (1)(4)	Cycle to cycle Jitter	System Clock		371		ps
	(peak to peak)			3/1		

⁽¹⁾ Based on characterization, not tested in production.

Table 4-19. PLL1/2 characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{PLLIN} ⁽¹⁾	PLL input clock frequency	_	1	_	25	MHz
f _{PLLOUT} (2)	PLL output clock frequency		16		108	MHz
f _{VCO} ⁽²⁾	VCO output frequency	_	32	_	216	MHz
t _{LOCK} (2)	PLL lock time				400	μs
I _{DDA} (1)(3)	Current consumption on	VCO freq = 216 MHz		145		
IDDA ⁽¹⁾⁽³⁾	V_{DDA}	VCO 1164 – 210 MHZ	_	143		μΑ

⁽²⁾ Based on characterization, not tested in production.

⁽²⁾ Guaranteed by design, not tested in production.

⁽³⁾ System clock = HXTAL = 8 MHz, $f_{PLLOUT} = 108 MHz$.

⁽⁴⁾ Value given with main PLL running.

Jitter _{PLL} ⁽¹⁾⁽⁴⁾	Cycle to cycle Jitter (rms)	Suptam alaak	35		
JillerPLL	Cycle to cycle Jitter (peak to peak)	System clock	371	ps	

- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.
- (3) System clock = HXTAL = 8 MHz, fpllout = 108 MHz.
- (4) Value given with main PLL running

4.10. Memory characteristics

Table 4-20. Flash memory characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽²⁾	Unit
	Number of guaranteed					
PEcyc	program /erase cycles	$T_A = -40 ^{\circ}\text{C} \sim +85 ^{\circ}\text{C}$	100	_	_	kcycles
	before failure (Endurance)					
t _{RET}	Data retention time	T _A = 125 °C	_	20	_	years
wt _{PROG}	Word programming time	T _A = -40 °C ~ +85 °C	_	37.5	86	μs
t _{ERASE}	Page erase time	T _A = -40 °C ~ +85 °C	_	45	300	ms
t _{MERASE(128K)}	Mass erase time	T _A = -40 °C ~ +85 °C	_	1	3.2	S

⁽¹⁾ Based on characterization, not tested in production.

4.11. NRST pin characteristics

Table 4-21. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IL(NRST)} ⁽¹⁾	NRST Input low level voltage	0.03/43/	-0.5		0.3 V _{DD}	.,
V _{IH(NRST)} ⁽¹⁾	NRST Input high level voltage	T Input high level voltage $2.6 \text{ V} \le \text{V}_{DD} = \text{V}_{DDA} \le 0.00$			V _{DD} + 0.5	V
V _{hyst} (1)	Schmidt trigger Voltage hysteresis	3.6 V	_	210	_	mV
R _{pu} ⁽²⁾	Pull-up equivalent resistor	_		40	_	kΩ

⁽¹⁾ Based on characterization, not tested in production.

⁽²⁾ Guaranteed by design, not tested in production.

⁽²⁾ Guaranteed by design, not tested in production.



External reset circuit $\frac{V_{DD}}{10 \text{ k}\Omega}$

Figure 4-4. Recommended external NRST pin circuit⁽¹⁾

(1) Unless the voltage on NRST pin go below $V_{\text{IL}(NRST)}$ level, the device would not generate a reliable reset.

4.12. **GPIO** characteristics

Table 4-22. I/O port DC characteristics⁽¹⁾⁽³⁾

Symbol	Parame	ter	Conditions	Min	Тур	Max	Unit
V/a	Standard IO Low voltag	-	$2.6 \text{ V} \leq \text{V}_{DD} = \text{V}_{DDA} \leq 3.6 \text{ V}$	_	_	0.3 V _{DD}	>
VıL	5V-tolerant IO input volt		$2.6 \text{ V} \le \text{V}_{DD} = \text{V}_{DDA} \le 3.6 \text{ V}$	_	_	0.3 V _{DD}	٧
N/	Standard IO Finput volt	-	2.6 V ≤ V _{DD} = V _{DDA} ≤ 3.6 V	0.7 V _{DD}	_	_	٧
V _{IH}	5V-tolerant IO input volt		$2.6 \text{ V} \le \text{V}_{DD} = \text{V}_{DDA} \le 3.6 \text{ V}$	0.7 V _{DD}	_	_	٧
	Low level outp	ut voltage	$V_{DD} = 2.6 \text{ V}$	_		0.3	
Vol	for each IO Pins (I _{IO} = +8 mA)		$V_{DD} = 3.3 \text{ V}$	_	1	0.3	V
			$V_{DD} = 3.6 \text{ V}$	_	1	0.3	
	Low level outp	ut voltage	$V_{DD} = 2.6 \text{ V}$	_	1	1	
Vol	for each IC) Pins	$V_{DD} = 3.3 \text{ V}$	_	1	0.8	V
	(I _{IO} = +20	mA)	$V_{DD} = 3.6 \text{ V}$	_	1	0.7	
	High level outp	ut voltage	$V_{DD} = 2.6 \text{ V}$	2.3	1	_	
Vон	for each IC) Pins	$V_{DD} = 3.3 \text{ V}$	3.0	_	_	V
	(I _{IO} = +8	mA)	$V_{DD} = 3.6 \text{ V}$	3.3	_	_	
	High level outp	ut voltage	$V_{DD} = 2.6 \text{ V}$	1.5	_	_	
Vон	for each IC) Pins	$V_{DD} = 3.3 \text{ V}$	2.6	_	_	V
	(I _{IO} = +20 mA)		V _{DD} = 3.6 V	2.8	_	_	
R _{PU} ⁽²⁾	Internal pull-up	All pins	V _{IN} = V _{SS}	_	40	_	kΩ
L PU'-	resistor	PA10		_	10	_	K12
R _{PD} ⁽²⁾	Internal pull-	All pins	$V_{IN} = V_{DD}$	_	40	_	kΩ



down resistor	PA10	_	_	10		
---------------	------	---	---	----	--	--

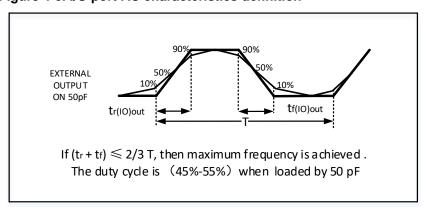
- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.
- (3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

Table 4-23. I/O port AC characteristics(1)(2)

GPIOx_MDy[1:0] bit value ⁽³⁾	Parameter	Conditions	Max	Unit	
		$V_{DD} = 2.6 \text{ V}, C_L = 10 \text{ pF}$	6		
		$V_{DD} = 2.6 \text{ V}, C_L = 30 \text{ pF}$	4		
$GPIOx_CTL->MDy[1:0] = 10$	Maximum frequency ⁽⁴⁾	$V_{DD} = 2.6 \text{ V}, C_L = 50 \text{ pF}$	2	MHz	
(IO_Speed = 2 MHz)	Maximum requercy	$V_{DD} = 3.3 \text{ V}, C_L = 10 \text{ pF}$	8	IVII IZ	
		$V_{DD} = 3.3 \text{ V}, C_L = 30 \text{ pF}$	6		
		$V_{DD} = 3.3 \text{ V}, C_L = 50 \text{ pF}$	4		
		$V_{DD} = 2.6 \text{ V}, C_L = 10 \text{ pF}$	16		
	Maximum frequency ⁽⁴⁾	$V_{DD} = 2.6 \text{ V}, C_L = 30 \text{ pF}$	12		
GPIOx_CTL->MDy[1:0] = 01		$V_{DD} = 2.6 \text{ V}, C_L = 50 \text{ pF}$	10	MHz	
(IO_Speed = 10 MHz)		$V_{DD} = 3.3 \text{ V}, C_L = 10 \text{ pF}$	20	IVII IZ	
		$V_{DD} = 3.3 \text{ V}, C_L = 30 \text{ pF}$	16		
		$V_{DD} = 3.3 \text{ V}, C_L = 50 \text{ pF}$	14		
		$V_{DD} = 2.6 \text{ V}, C_L = 10 \text{ pF}$	108		
		$V_{DD} = 2.6 \text{ V}, C_L = 30 \text{ pF}$	100		
GPIOx_CTL->MDy[1:0] = 11	Maximum frequency ⁽⁴⁾	$V_{DD} = 2.6 \text{ V}, C_L = 50 \text{ pF}$	72	MHz	
(IO_Speed = 50 MHz)	waximum nequency	$V_{DD} = 3.3 \text{ V}, C_L = 10 \text{ pF}$	108	ıvı⊓Z	
		$V_{DD} = 3.3 \text{ V}, C_L = 30 \text{ pF}$	100		
		$V_{DD} = 3.3 \text{ V}, C_L = 50 \text{ pF}$	80		

- (1) Based on characterization, not tested in production.
- (2) Unless otherwise specified, all test results given for T_A = 25 $\,^{\circ}$ C.
- (3) The I/O speed is configured using the GPIOx_CTL -> MDy[1:0] bits. Refer to the GD32VF103xx user manual which is selected to set the GPIO port output speed.
- (4) The maximum frequency is defined in Figure 4-5 and maximum frequency cannot exceed 108 MHz.

Figure 4-5. I/O port AC characteristics definition





4.13. ADC characteristics

Table 4-24. ADC characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DDA}^{(1)}$	Operating voltage	_	2.6	3.3	3.6	V
$V_{IN}^{(1)}$	ADC input voltage range	_	0	_	V _{REF+}	٧
f _{ADC} ⁽¹⁾	ADC clock	_	0.6	_	14	MHz
		12-bit	0.04	_	1	
fs ⁽¹⁾	Sampling rate	10-bit	0.05	_	1.17	MSPS
IS ^(··)	Sampling rate	8-bit	0.06	_	1.4	MSPS
		6-bit	0.08	_	1.75	
V _{AIN} ⁽¹⁾	Analog input voltage	16 external; 2 internal	0	_	V _{DDA}	V
V _{REF+} ⁽²⁾	Positive Reference Voltage	_	2.4	_	V _{DDA}	V
V _{REF-} (2)	Negative Reference Voltage	_	_	Vssa	_	V
R _{AIN} ⁽²⁾	External input impedance	See <u>Equation 1</u>	_	_	320	kΩ
R _{ADC} ⁽²⁾	Input sampling switch resistance	_	_	_	0.55	kΩ
C _{ADC} ⁽²⁾	Input sampling capacitance	No pin/pad capacitance included	_	_	5.5	pF
t _s (2)	Sampling time	f _{ADC} = 14 MHz	0.1	_	17.1	μs
	Takal as assessation	12-bit	_	14	_	
Total conversion tconv ⁽²⁾ time(including sampling		10-bit	_	12	_	4/5
	8-bit	_	10	_	1/ f _{ADC}	
	time)	6-bit	_	8	_	
tsu ⁽²⁾	Startup time		_	_	1	μs

⁽¹⁾ Based on characterization, not tested in production.

$$\textit{Equation 1}: \text{ R}_{\text{AIN}} \text{ max formula } \text{ R}_{\text{AIN}} < \frac{\text{T}_{\text{s}}}{\text{f}_{\text{ADC}} * \text{C}_{\text{ADC}} * \text{In}(2^{N+2})} - \text{R}_{\text{ADC}}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-25. ADC R_{AIN} max for f_{ADC} = 14 $MHz^{(1)}$

T _s (cycles)	t _s (us)	R _{AINmax} (kΩ)
1.5	0.11	1.46
7.5	0.54	9.49
13.5	0.96	17.5
28.5	2.04	37.6
41.5	2.96	55
55.5	3.96	73.7
71.5	5.11	95

⁽²⁾ Guaranteed by design, not tested in production.



T _s (cycles)	t _s (us)	R _{AINmax} (kΩ)
239.5	17.11	320

⁽¹⁾ Guaranteed by design, not tested in production.

4.14. Temperature sensor characteristics

Table 4-26. Temperature sensor characteristics⁽¹⁾

Symbol	Parameter	Min	Тур	Max	Unit
T∟	V _{SENSE} linearity with temperature		±1.5	_	°C
Avg_Slope	Average slope	_	4.1	_	mV/°C
V ₂₅	Voltage at 25 °C	_	1.45	_	V
ts_temp (2)	ADC sampling time when reading the temperature	_	17.1	_	μs

⁽¹⁾ Based on characterization, not tested in production.

4.15. DAC characteristics

Table 4-27. DAC characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DDA}^{(1)}$	Operating voltage		2.6	3.3	3.6	V
V _{REF+} ⁽²⁾	Positive Reference Voltage		2.4		V_{DDA}	V
V _{REF-} (2)	Negative Reference Voltage		_	Vssa		V
R _{LOAD} ⁽²⁾	Load resistance	Resistive load with buffer ON	5	_		kΩ
Ro ⁽²⁾	Impedance output with buffer OFF	ı	l	_	15	kΩ
C _{LOAD} ⁽²⁾	Load capacitance	No pin/pad capacitance included		_	50	pF
DAC_OUT min ⁽²⁾	Lower DAC_OUT voltage with buffer ON		0.2	_		٧
DAC_OUT max ⁽²⁾	Higher DAC_OUT voltage with buffer ON	_	_	_	V _{DDA} -	V
DAC_OUT min ⁽²⁾	Lower DAC_OUT voltage with buffer OFF	-	_	0.5	_	mV
DAC_OUT max ⁽²⁾	Higher DAC_OUT voltage with buffer OFF	_	_	_	V _{DDA} -	٧
I _{DDA} ⁽¹⁾	DAC current consumption	With no load, middle $code(0x800)$ on the input, $V_{REF+} = 3.6 \text{ V}$	_	470	_	μΑ
	in quiescent mode	With no load, worst code(0xF1C) on the input,	_	570	_	μА

⁽²⁾ Shortest sampling time can be determined in the application by multiple iterations.



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V _{REF+} = 3.6 V				
. (1)	DAC current consumption	With no load, middle code(0x800) on the input, $V_{REF+} = 3.6 \; V$	_	90	_	μА
IDDVREF+ ⁽¹⁾	in quiescent mode	With no load, worst code(0xF1C) on the input, VREF+ = 3.6 V	_	298	_	μА
DNL ⁽¹⁾	Differential non-linearity error	DAC in 12-bit mode	_	_	±3	LSB
INL ⁽¹⁾	Integral non-linearity	DAC in 12-bit mode	_	_	±4	LSB
Offset ⁽¹⁾	Offset error	DAC in 12-bit mode	_		±12	LSB
GE ⁽¹⁾	Gain error	DAC in 12-bit mode	_	ı	±0.5	%
T _{setting} ⁽¹⁾	Settling time	$C_{LOAD} \leqslant~50$ pF, $R_{LOAD} \geqslant~5$ $k\Omega$	_	0.3	1	μs
T _{wakeup} (2)	Wakeup from off state	_	_	5	10	μs
Update rate ⁽²⁾	Max frequency for a correct DAC_OUT change from code i to i ± 1 LSBs	$C_{\text{LOAD}} \leqslant~50$ pF, $R_{\text{LOAD}} \geqslant~5$ $k\Omega$	_	1	4	MS/s
PSRR ⁽²⁾	Power supply rejection ratio (to V _{DDA})	_	55	80	_	dB

⁽¹⁾ Based on characterization, not tested in production.

4.16. I2C characteristics

Table 4-28. I2C characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
t _{SCL(H)}	SCL clock high time	_	4.0	_	0.6	_	0.2		μs
t _{SCL(L)}	SCL clock low time	_	4.7	_	1.3		0.5	1	μs
t _{su(SDA)}	SDA setup time	_	250		100		50	l	ns
t _{h(SDA)}	SDA data hold time	_	0(3)	3450	0	900	0	450	ns
t _r (SDA/SCL)	SDA and SCL rise time	_	_	1000	_	300	_	120	ns
t _{f(SDA/SCL)}	SDA and SCL fall time	_		300	_	300	_	120	ns
t _{h(STA)}	Start condition hold	_	4.0	_	0.6	_	0.26		μs

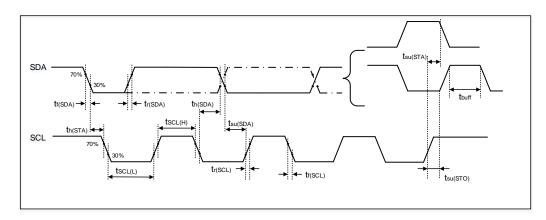
⁽²⁾ Guaranteed by design, not tested in production.



Symbol	Parameter Condition	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
	time								
t _{s(STA)}	Repeated Start condition setup time		4.7	_	0.6	_	0.26	_	μs
t _{s(STO)}	Stop condition setup time	_	4.0	_	0.6		0.26	-	μs
t _{buff}	Stop to Start condition time (bus free)		4.7	_	1.3	_	0.5	_	μs

- (1) Guaranteed by design, not tested in production.
- (2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.
- (3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-6. I2C bus timing diagram



4.17. SPI characteristics

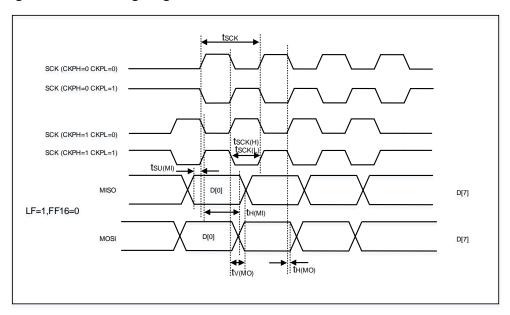
Table 4-29. Standard SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{SCK}	SCK clock frequency	_			27	MHz
tsck(H)		Master mode, f _{PCLKx} = 108 MHz, presc = 8	35	37	39	ns
t _{SCK(L)}	SCK clock low time	Master mode, f _{PCLKx} = 108 MHz, presc = 8	35	37	39	ns
		SPI master mode				
t _{V(MO)}	Data output valid time	_		7		ns
t _{H(MO)}	Data output hold time	_		4	_	ns

tsu(MI)	Data input setup time	_	1	_	_	ns
t _{H(MI)}	Data input hold time	_	0	_		ns
		SPI slave mode				
tsu(NSS)	NSS enable setup time	f _{PCLK} = 54 MHz	0	_	_	ns
t _{H(NSS)}	NSS enable hold time	f _{PCLK} = 54 MHz	1	_		ns
t _{A(SO)}	Data output access time	_	_	9	_	ns
t _{DIS(SO)}	Data output disable time	_		8	١	ns
t _{V(SO)}	Data output valid time	_	_	10	_	ns
t _{H(SO)}	Data output hold time	_		10		ns
t _{SU(SI)}	Data input setup time	_	0	_		ns
t _{H(SI)}	Data input hold time	_	1	_		ns

⁽¹⁾ Based on characterization, not tested in production.

Figure 4-7. SPI timing diagram - master mode





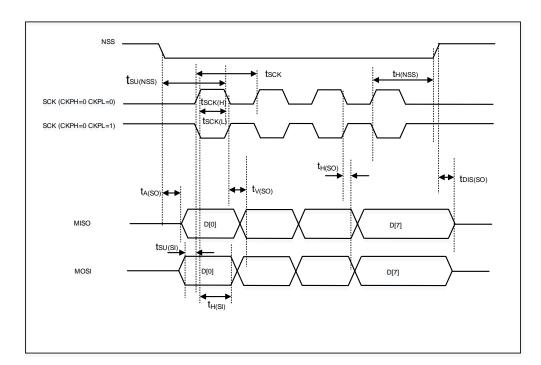


Figure 4-8. SPI timing diagram - slave mode

4.18. I2S characteristics

Table 4-30. I2S characteristics(1)(2)

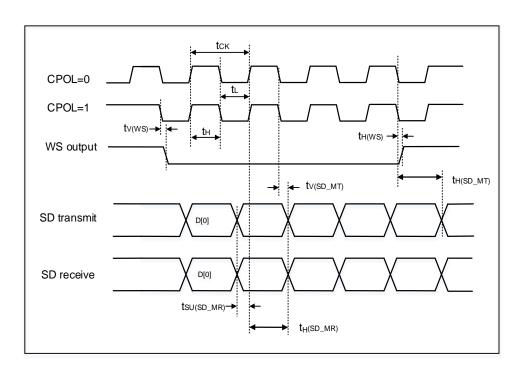
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		Master mode (data: 16 bits,	3.070	2 072	3.074	
fcĸ	Clock frequency	Audio frequency = 96 kHz)	3.070	3.072	3.074	MHz
		Slave mode	_	10	_	
t _H	Clock high time		I	162	ı	ns
t∟	Clock low time		I	163	ı	ns
t _{V(WS)}	WS valid time	Master mode	_	2		ns
t _{H(WS)}	WS hold time	Master mode	_	2		ns
tsu(ws)	WS setup time	Slave mode	0	_		ns
t _{H(WS)}	WS hold time	Slave mode	1	_		ns
Duevease	I2S slave input clock duty	Slave mode		50		%
Ducy _(SCK)	cycle	Slave Illoue		50		/0
tsu(SD_MR)	Data input setup time	Master mode	3		_	ns
$t_{\text{su}(\text{SD_SR})}$	Data input setup time	Slave mode	0	_	1	ns
t _{H(SD_MR)}	Data input hold time	Master receiver	0	_		ns
th(SD_SR)	Data input hold time	Slave receiver	1	_		ns
tues es	Data output valid time	Slave transmitter		12		nc
t _{V(SD_ST)}	Data output valid time	(after enable edge)		12		ns
th(SD_ST)	Data output hold time	Slave transmitter		10		ns



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		(after enable edge)				
	Data output valid time	Master transmitter	_	10	_	20
t _{V(SD_MT)}		(after enable edge)				ns
	Data output hold time	Master transmitter		7	_	
th(SD_MT)		(after enable edge)	_			ns

- (1) Guaranteed by design, not tested in production.
- (2) Based on characterization, not tested in production.

Figure 4-9. I2S timing diagram - master mode



th(SD_ST)



CPOL=0
CPOL=1
WS input

t∨(SD_ST)

► t_H(SD_SR)

Figure 4-10. I2S timing diagram - slave mode

tsu(ws) ◀

tsu(sd_sr)

4.19. USART characteristics

SD transmit

SD receive

Table 4-31. USART0 characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{SCK}	SCK clock frequency	$f_{PCLKx} = 108 \text{ MHz}$	_	_	54	MHz
t _{SCK(H)}	SCK clock high time	f _{PCLKx} = 108 MHz	4.63	_	_	ns
t _{SCK(L)}	SCK clock low time	f _{PCLKx} = 108 MHz	4.63	_	_	ns

⁽¹⁾ Guaranteed by design, not tested in production.

Table 4-32. USART1-2/UART3-4 characteristics(1)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{SCK}	SCK clock frequency	f _{PCLKx} = 108 MHz	_		54	MHz
t _{SCK(H)}	SCK clock high time	f _{PCLKx} = 108 MHz	9.26	_	_	ns
t _{SCK(L)}	SCK clock low time	f _{PCLKx} = 108 MHz	9.26	_	_	ns

⁽¹⁾ Guaranteed by design, not tested in production.

4.20. CAN characteristics

Refer to <u>Table 4-22. I/O port DC characteristics</u>(1) for more details on the input/output alternate function characteristics (CANTX and CANRX).



4.21. USBFS characteristics

Table 4-33. USBFS start up time

Symbol	Parameter	Max	Unit
tstartup ⁽¹⁾	USBFS startup time	1	μs

⁽¹⁾ Guaranteed by design, not tested in production.

Table 4-34. USBFS DC electrical characteristics

Symbol		Parameter	Conditions	Min	Тур	Max	Unit
	V_{DD}	USBFS operating voltage		3	_	3.6	>
Input	V_{DI}	Differential input sensitivity	I(USBDP, USBDM)	0.2	_	_	
levels ⁽¹⁾	V _{CM}	Differential common mode range	Includes V _{DI} range	0.8	_	2.5	V
	Vse	Single ended receiver threshold	_	1.3	_	2.0	
Output	Vol	Static output level low	R_L of 1.55 $k\Omega$ to 3.3 V	_	0.04	0.3	V
levels ⁽²⁾	Vон	Static output level high	R_L of 21 $k\Omega$ to V_{SS}	2.8	3.3	3.6	V

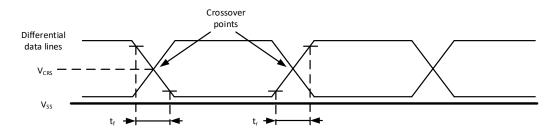
⁽¹⁾ Guaranteed by design, not tested in production.

Table 4-35. USBFS electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _R	Rise time	CL = 50 pF	4	_	20	ns
t _F	Fall time	CL = 50 pF	4	_	20	ns
t _{RFM}	Rise / fall time matching	t _R / t _F	90	_	110	%
VCRS	Output signal crossover voltage	_	1.3	_	2.0	V

⁽¹⁾ Guaranteed by design, not tested in production.

Figure 4-11. USBFS timings: definition of data signal rise and fall time



4.22. EXMC characteristics

Table 4-36. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

	·		<u> </u>		
	Symbol	Symbol Parameter		Max	Unit
	t _{w(NE)}	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		66.1	ns
	$t_{V(NOE_{_NE})}$			_	ns
	t _{w(NOE)}			38.2	ns
Ī	t _{h(NE_NOE)}	EXMC_NOE high to EXMC_NE high hold time	0	_	ns

⁽²⁾ Based on characterization, not tested in production.



t _{v(A_NE)}	EXMC_NEx low to EXMC_A valid	0 —		ns
t _{v(A_NOE)}	Address hold time after EXMC_NOE high	0	_	ns
t _{v(BL_NE)}	EXMC_NEx low to EXMC_BL valid	0	_	ns
t _{h(BL_NOE)}	EXMC_BL hold time after EXMC_NOE high	0	_	ns
t _{su(DATA_NE)}	Data to EXMC_NEx high setup time	37.2	_	ns
t _{su(DATA_NOE)}	Data to EXMC_NOEx high setup time	C_NOEx high setup time 37.2 —		ns
t _{h(DATA_NOE)}	Data hold time after EXMC_NOE high	0	_	ns
t _{h(DATA_NE)}	Data hold time after EXMC_NEx high	ADV low 0 —		ns
t _{v(NADV_NE)}	EXMC_NEx low to EXMC_NADV low			ns
t _{w(NADV)}	EXMC_NADV low time			ns
T _{h(AD_NADV)}	EXMC_AD(address) valid hold time after EXMC_NADV high	8.3	10.3	ns

⁽¹⁾ $C_L = 30 \text{ pF}.$

Table 4-37. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Min	Max	Unit
t _{w(NE)}	EXMC_NE low time	45.5	47.5	ns
t _{V(NWE_NE)}	$\begin{array}{ccc} t_{\text{V(NWE_NE)}} & \text{EXMC_NEx low to EXMC_NWE low} & 8.3 \\ \\ t_{\text{W(NWE)}} & \text{EXMC_NWE low time} & 26.9 \\ \\ t_{\text{h(NE_NWE)}} & \text{EXMC_NWE high to EXMC_NE high hold time} & 8.3 \\ \end{array}$		_	ns
t _{w(NWE)}			28.9	ns
t _{h(NE_NWE)}			_	ns
t _{v(A_NE)}	EXMC_NEx low to EXMC_A valid	0	_	ns
t _{V(NADV_NE)}	EXMC_NEx low to EXMC_NADV low	0	_	ns
t _{w(NADV)}	EXMC_NADV low time	EXMC_NADV low time 8.3		ns
t	EXMC_AD(address) valid hold time after	8.3	_	ns
t _{h(AD_NADV)}	EXMC_NADV high			
t _{h(A_NWE)}	Address hold time after EXMC_NWE high	8.3	_	ns
t _{h(BL_NWE)}	EXMC_BL hold time after EXMC_NWE high	8.3	_	ns
t _{v(BL_NE)}	EXMC_NEx low to EXMC_BL valid	0 —		ns
t _{v(DATA_NADV)}	(V(DATA_NADV) EXMC_NADV high to DATA valid		_	ns
t _{h(DATA_NWE)} Data hold time after EXMC_NWE high		8.3	_	ns

⁽¹⁾ $C_L = 30 pF$.

4.23. TIMER characteristics

Table 4-38. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
+	Timer resolution time	_	1	_	tTIMERXCLK
t _{res}		f _{TIMERxCLK} = 108 MHz	9.26	_	ns
f _{EXT}	Timer external clock	_	0	f _{TIMERxCLK} / 2	MHz

⁽²⁾ Guaranteed by design, not tested in production.

⁽³⁾ Based on configure: f_{HCLK} = 108 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

⁽²⁾ Guaranteed by design, not tested in production.

 $^{(3) \}quad \text{Based on configure: } f_{\text{HCLK}} = 108 \text{ MHz, AddressSetupTime} = 0, \\ \text{AddressHoldTime} = 1, \\ \text{DataSetupTime} = 1.$

GD32VF103 Datasheet

	Symbol	Parameter	Conditions	Min	Max	Unit
		frequency	ftimerxclk = 108 MHz	0	54	MHz
	RES	Timer resolution	_	_	16	bit
		16-bit counter clock period	_	1	65536	t _{TIMERxCLK}
	tCOUNTER	when internal clock is	ftimerxclk = 108 MHz	0 0003	607	
		selected	TIIMERXCLK = TOO MINZ	0.0093	007	μs
	tury count	Maximum possible count		_	65536x65536	timerxclk
	tmax_count	waximum possible count	f _{TIMERxCLK} = 108 MHz	_	39.8	s

⁽¹⁾ Guaranteed by design, not tested in production.

4.24. WDGT characteristics

Table 4-39. FWDGT min/max timeout period at 40 kHz (IRC40K)(1)

B	DDIO 01 Life	Min timeout RLD[11:0] =	Max timeout RLD[11:0]	
Prescaler divider	PR[2:0] bits	0x000	= 0xFFF	Unit
1/4	000	0.025	409.525	
1/8	001	0.025	819.025	
1/16	010	0.025	1638.025	
1/32	011	0.025	3276.025	ms
1/64	100	0.025	6552.025	
1/128	101	0.025	13104.025	
1/256	110 or 111	0.025	26208.025	

⁽¹⁾ Guaranteed by design, not tested in production.

Table 4-40. WWDGT min/max timeout value at 54 MHz (f_{PCLK1})⁽¹⁾

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	75.8		4.85	
1/2	01	151.7		9.7	mo
1/4	10	303.4	μs	19.4	ms
1/8	11	606.8		38.8	

⁽¹⁾ Guaranteed by design, not tested in production.

4.25. Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C.



5. Package information

5.1. LQFP100 package outline dimensions

Figure 5-1. LQFP100 package outline

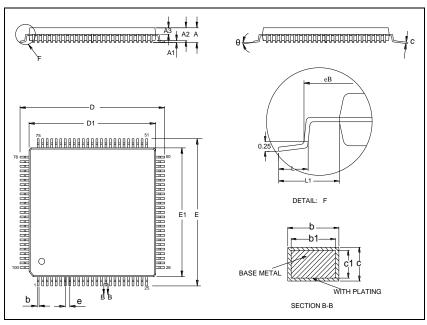
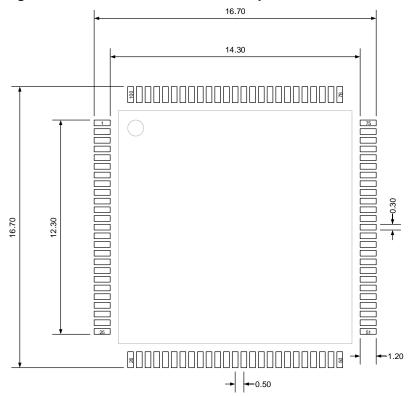


Table 5-1. LQFP100 package dimensions

Symbol	Min	Тур	Max
А	_	_	1.60
A1	0.05	_	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18		0.26
b1	0.17	0.20	0.23
С	0.13	_	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
е	_	0.50	_
eB	15.05	_	15.35
L	0.45		0.75
L1	_	1.00	_
θ	0°	_	7°



Figure 5-2. LQFP100 recommended footprint





5.2. LQFP64 package outline dimensions

Figure 5-3. LQFP64 package outline

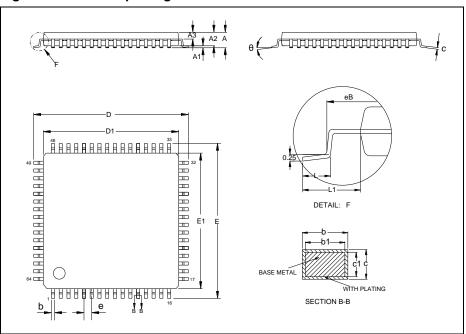
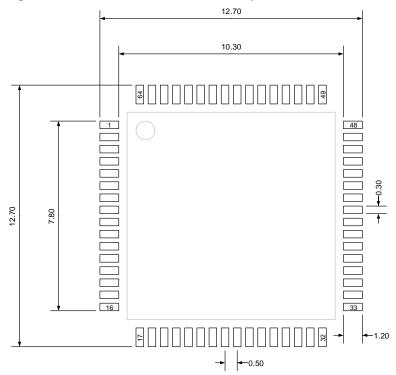


Table 5-2. LQFP64 package dimensions

Symbol	Min	Тур	Max
Α	_	_	1.60
A1	0.05	_	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	_	0.26
b1	0.17	0.20	0.23
С	0.13	_	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
е	_	0.50	_
eB	11.25	_	11.45
L	0.45	_	0.75
L1	_	1.00	_
θ	0°	_	7°



Figure 5-4. LQFP64 recommended footprint





5.3. LQFP48 package outline dimensions

Figure 5-5. LQFP48 package outline

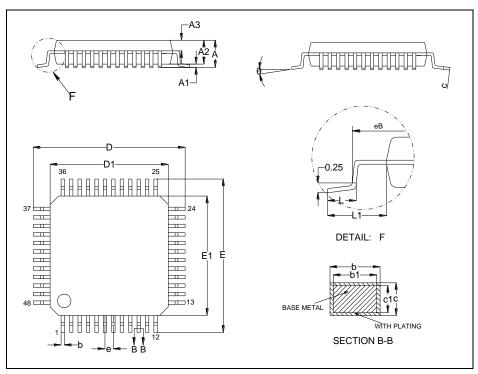
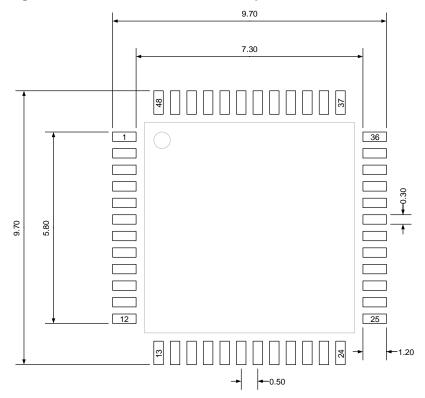


Table 5-3. LQFP48 package dimensions

Symbol	Min	Тур	Max
Α	_	_	1.60
A1	0.05	_	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	_	0.26
b1	0.17	0.20	0.23
С	0.13	_	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
е	_	0.50	_
eB	8.10	_	8.25
L	0.45	_	0.75
L1	_	1.00	_
θ	0°	_	7°



Figure 5-6. LQFP48 recommended footprint





5.4. QFN36 package outline dimensions

Figure 5-7. QFN36 package outline

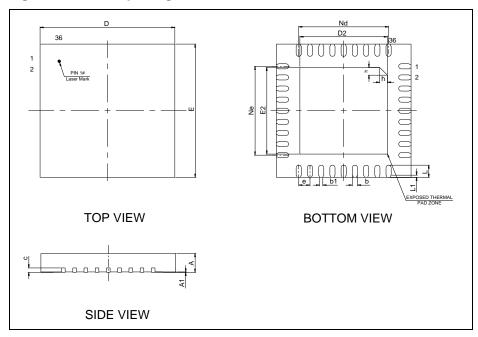
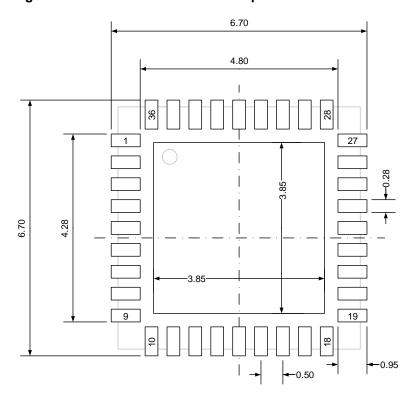


Table 5-4. QFN36 package dimensions

Symbol	Min	Тур	Max
Α	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.18	0.23	0.30
b1	_	0.16	_
С	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	3.80	3.90	4.00
Е	5.90	6.00	6.10
E2	3.80	3.90	4.00
е	_	0.50	_
h	0.30	0.35	0.40
L	0.50	0.55	0.60
L1	_	0.10	_
Nd	3.95	4.00	4.05
Ne	3.95	4.00	4.05



Figure 5-8. QFN36 recommended footprint





5.5. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "0". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

 θ_{JA} : Thermal resistance, junction-to-ambient.

 θ_{JB} : Thermal resistance, junction-to-board.

 θ_{JC} : Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

ΨJT: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA} = (T_J - T_A)/P_D \tag{5-1}$$

$$\theta_{JB} = (T_J - T_B)/P_D \tag{5-2}$$

$$\theta_{JC} = (T_J - T_C)/P_D \tag{5-3}$$

Where, T_J = Junction temperature.

 T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

 P_D = Total power dissipation

 θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

 θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

 θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-5. Package thermal characteristics⁽¹⁾

Symbol	Condition	Package	Value	Unit	
		LQFP100	57.42		
	Natural convention 2020 DOD	LQFP64	61.80	°C/W	
θυα	Natural convection, 2S2P PCB	LQFP48	64.40		
		QFN36	43.20		
0	Cold plate 2020 DOD	LQFP100	31.68	0000	
θЈВ	Cold plate, 2S2P PCB	LQFP64	42.83	°C/W	



GD32VF103 Datasheet

Symbol	Condition	Package	Value	Unit
		LQFP48	42.32	
		QFN36	16.51	
		LQFP100	13.85	
θ _{JC}	Cold plate, 2S2P PCB	LQFP64	21.98	°C/W
⊕ 1C		LQFP48	22.47	C/VV
		QFN36	16.18	
	Natural convection, 2S2P PCB	LQFP100	41.28	
III		LQFP64	43.05	°C/W
Ψ_{JB}		LQFP48	42.42	
		QFN36	16.64	
	Notural convection 2020 DCD	LQFP100	0.75	
		LQFP64	1.58	°C/W
$\Psi_{ m JT}$	Natural convection, 2S2P PCB	LQFP48	1.74	C/VV
		QFN36	1.07	

⁽¹⁾ Thermal characteristics are based on simulation, and meet JEDEC specification.



6. Ordering information

Table 6-1. Part ordering code for GD32VF103xx devices

	Table 0-1. Fait ordering code for 9D32V1 103XX devices								
Ordering code	Flash (KB)	Package	Package type	Temperature operating range					
GD32VF103VBT6	128	LQFP100	Green	Industrial					
OD32VI 103VD10	120	EQT 100	Orcen	-40 °C to +85 °C					
GD32VF103V8T6	64	LQFP100	Green	Industrial					
0502111001010		2011100	0.00	-40 °C to +85 °C					
GD32VF103RBT6	128	LQFP64	Green	Industrial					
				-40 °C to +85 °C					
GD32VF103R8T6	64	LQFP64	Green	Industrial					
				-40 °C to +85 °C					
GD32VF103R6T6	32	LQFP64	Green	Industrial					
				-40 °C to +85 °C					
GD32VF103R4T6	16	LQFP64	Green	Industrial					
				-40 °C to +85 °C					
GD32VF103CBT6	128	LQFP48	Green	Industrial					
				-40 °C to +85 °C					
GD32VF103C8T6	64	LQFP48	Green	Industrial					
	-	-, -		-40 °C to +85 °C					
GD32VF103C6T6	32	LQFP48	Green	Industrial					
				-40 °C to +85 °C					
GD32VF103C4T6	16	LQFP48	Green	Industrial					
	-	-, -		-40 °C to +85 °C					
GD32VF103TBU6	128	QFN36	Green	Industrial					
	-	-,		-40 °C to +85 °C					
GD32VF103T8U6	64	QFN36	Green	Industrial					
	-			-40 °C to +85 °C					
GD32VF103T6U6	32	QFN36	Green	Industrial					
				-40 °C to +85 °C					
GD32VF103T4U6	16	QFN36	Green	Industrial					
	-			-40 °C to +85 °C					



7. Revision History

Table 7-1. Revision history

Revision No.		Description	Date
1.0		Initial Release	Jun.5, 2019
	1.	Clock tree modification, the factor for CK_CST changes	
1.1		from 8 to 4, refers to Clock tree.	Sep.16,2019
1.1	2.	Add I2C fast mode plus related information, refers to <u>I2C</u>	ОСР. 10,2013
		<u>characteristics</u> .	
	1.	Chapter <u>Electrical characteristics</u> electrical	
		characteristics update.	
1.2	2.	Chapter <u>Package information</u> package information	Feb.15,2020
1.2		update.	1 eb. 15,2020
	3.	Delete the PD0,PD1 remap to OSC pins information in	
		packages no less than100 pins, refers to Pin definitions .	
	1.	Chapter <u>PLL characteristics</u> modification.	
	2.	Add description of $V_{\text{REF+}}$ and $V_{\text{REF-}}$ connection in chapter	
		Analog to digital converter (ADC).	
4.2	3.	Modify the LDO mode conditions in Power consumption .	Dag 45 2020
1.3	4.	Delete EXMC characteristics comments in chapter EXMC	Dec.15,2020
		<u>characteristics</u> .	
	5.	T _{STG} range changes to -65°C~+150°C in <i>Absolute</i>	
		maximum ratings.	
	1.	Add I2C, SPI, I2S timing diagrams, refers to <u>I2C</u>	
1.4		characteristics, SPI characteristics and I2S	Mar.29,2021
		<u>characteristics</u> .	
	1.	Update SPI and I2S timing diagrams, refers to <u>SPI</u>	
		characteristics and I2S characteristics.	
	2.	Update package information and ordering information,	
1.5		refers to Package information and Ordering	Dec.14, 2021
		<u>information</u> .	
	3.	Modify WDGT characteristics, refers to WDGT	
		<u>characteristics</u> .	
	1.	Add P _D parameter in <i>Table 4-1. Absolute maximum</i>	
		<u>ratings</u> (1)(4).	
	2.	Modify I2C timing diagrams, refers to <u>I2C</u>	
1.0		<u>characteristics</u> .	lum 7, 0000
1.6	3.	Modify LQFP64 package information, refer to <u>LQFP64</u>	Jun.7, 2022
		package outline dimensions.	
	4.	Update NRST external pin circuit, refer to Figure 4-4.	
		Recommended external NRST pin circuit(1)	



GD32VF103 Datasheet

5	5.	EXMC related pin update, refer to <i>Pin definitions</i> .	



Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the "Product"), is owned by the Company under the intellectual property laws and treaties of the People's Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as it's suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as it's suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products.

Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and Products and services described herein at any time, without notice.

© 2022 GigaDevice - All rights reserved