MIDWESTERN STATE UNIVERSITY

DEPARTMENT OF COMPUTER SCIENCE
CMPS 3023: Logic Design
Spring semester 2022

Project Assignment
03/09/2022 - due on April 25, 2022

RISC-V is an open source hardware instruction set originally developed at UC Berkeley. It supports 3 word widths, 32, 64, 128 bits. One of its characteristics is to have a subset of compressed instructions utilizing 16 bits, used to reduce program size when intermixed with the regular instructions. In this project, your team will design the hardware component (mini micro processor) required to execute some of these instructions. This project is to be performed either individually or by a group of at most 4 students.

For this project, you will design (using VHDL or schematics capture and components library) and simulate an 8-bit processor (8-bit registers), which includes four registers R0, R1, R2 and R3, able to execute the instructions similar to a subset of the compressed RISC-V instruction set as shown on the table below.

Table RISC-V Compressed Instruction subset

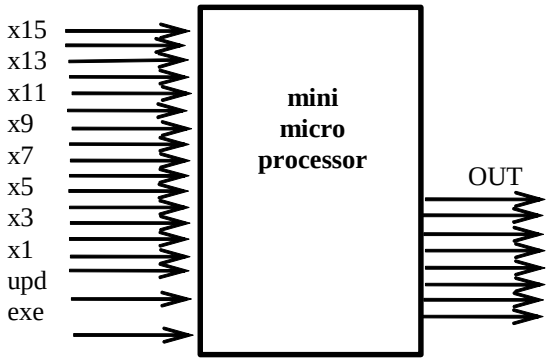
Mnemonic	Action	15 14 13	12	11 10	9 8 7	6 5	4 3 2	1 0
LI Rd,imm	Load Rd with immediate	010	imm5	rd		imm4:0		01
AND Ri,imm	Logical product Ri = Ri AND imm	100	imm5	10	rs/rd	imm4:0		01
SUB Rd,Rs2	Subtract Rd = Rd minus Rs2	100	1	11	rs/rd	00	rs2	01
OR Rd,Rs2	Logical sum Rd = Rd or Rs2	100	0	11	rs/rd	10	rs2	01
ADD Rd,Rs2	Add Rd = Rd plus Rs2	100	1	11	rs/rd	01	rs2	01
MV Rd,Rs	Copy Rs to Rd	100	0	rd		rs		10
OUT Rs	Displays contents of Rs*	100	0	00	000	rs		11

Rs: source register; Rd: destination register; Register numbers = 000, 001, 010, 011
*Not part of the RISC-V standard

The block diagram of the micro RISC-V processor is shown on next page. The machine has 18 input signals and 8 output signals. The 18 input signals consist of 16 bits used for instructions and 2 extra bits used to clock the operations: one clock signal will command the execution of the operation (EXE) and the other will update the destination register (UPD) (clock activates devices when zero, these two bits cannot be zero at the same time). The 8 output bits should show the value contained in R0 (in binary format), except when instructed to do it differently by the instruction OUT. Notice that immediate values have only 6 bits.

Coding example:

LI	R1,5	in binary 0100 0000 1001 0101
LI	R2,13	in binary 0100 0001 0011 0101
ADD	R1,R2	in binary 1001 1100 1010 1001
OUT	R1	in binary 1000 0000 00000 111



VERY IMPORTANT:

1. Clock signals activate circuit components when they are zero.

Project report:

Use computer word processing and drawing tools of your choice to generate your report. It must consist of the following items:

1. Block diagram (planned drawing) of the circuit implementation (show major components like registers, logic units, multiplexers, connections, etc.).

2. Printout of the circuit schematics (from Quartus) or VHDL code used to implement the design.

3. Electronic copy of the .vhd or the .bdf file required to run the simulation. **Do not submit any other file**.

4. Brief report on the simulation results (which instructions were simulated and success or not of the functionality of the design). Make sure to run a simulation that loads values in the registers before trying any operation such as ADD or SUB. Include snapshots or printouts of the simulation waveforms

Your project is due on April 25, 2022. You need to start working NOW!!!! Anything that you try to do in the last week before the due date will not work for sure. Time is an important factor in this project. **If you write your solution in VHDL and the entire solution has less than 3 entities described, then your solution was not well planned.** If your project does not work or you cannot justify why it does not work, then your grade will be zero. Acceptable justifications are based on software limitations only, and in this case you must show you had every component defined and tested and only the integration failed. Failure in reporting the simulation experiment will reduce your grade by twenty points. **NO EXTENSIONS!!**