

**TOSHIBA**

INTEGRATED CIRCUIT

TECHNICAL DATA

## 2,097,152 word x 9-bit Rambus DRAM INTRODUCTION

The TC59R1809VK/HK Rambus DRAM (RDRAM) is a next-generation high-speed CMOS DRAM with a 2,097,152-word x 9-bit organization and built-in slave logic. The 36,864 sense amps of the DRAM core are used as cache to achieve data transfer rates of up to 500MB/s. I/O is at the Rambus level, the open drain system being used for output.

The TC59R1809VK/HK uses a 32-pin plastic surface vertical mount package (SVP) enabling a high mounting density, and uses surface horizontal mount package (SHP). Also, the data transfer, which is synchronized with the high-speed clock, the self-refresh function, random access mode function, bit masking, byte masking function and the address mapping function obviate the need for external control circuits, making this DRAM ideal for use in main memory and graphics applications where high performance and low cost are essential.

## FEATURES

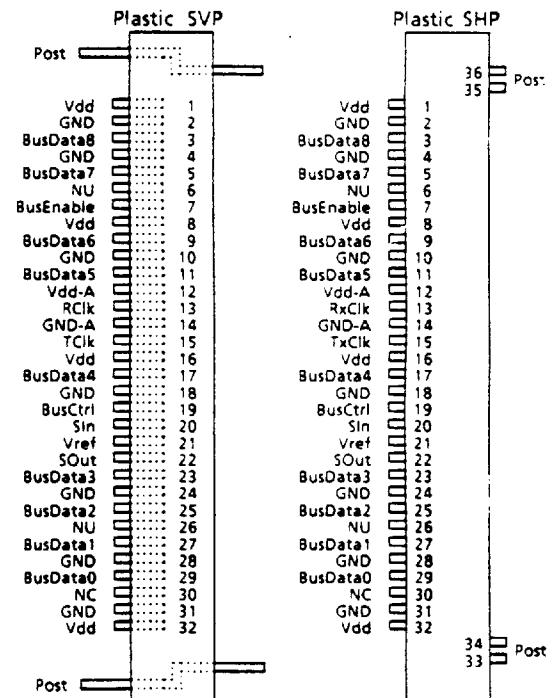
Main Characteristics		TC59R1809VK	
Maximum data transfer rate		2ns	
Minimum access time (cache hit)	Writing	16ns	
	Reading	40ns	
Minimum access time (cache miss)	Dirty	Writing	132ns
	Miss	Reading	156ns
Minimum access time (cache miss)	Clean	Writing	100ns
	Miss	Reading	124ns
Current consumption		220mA	

- Organization    RAM : 2,092,152 words x 9 bits (2 banks)  
Cache : 1024x9x2 (number of sense amps)  
Slave logic
- Self-refresh, Address mapping, and mask-write functions.  
Random Access Mode, Bit Mask, Byte Mask, Serial Control Packet.
- 1K refresh cycles per / 32ms
- Package : SVP / SHP
- 3.3V single power supply : 3.3V ± 0.3V
- IO : Rambus™ level

## PIN NAMES

BusData0-8	Bus data I/O
BusCtrl	Bus control I/O
BusEnable	Bus enable input
RClk	High-speed sync clock (for receiving data)
TClk	High-speed sync clock (for sending data)
Sin	Serial signal input
SOut	Serial signal output
Vref	Reference voltage
Vdd / GND	Power supply terminal (+ 3.3V) / ground
Vdd-A / GND-A	Power supply terminal (+ 3.3V) / ground (for DLL)
NC	Not connected
NU	Not used (substrate voltage)

## PIN CONFIGURATION (Top view)



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SILICON GATE CMOS

TENTATIVE

~~PRELIMINARY~~

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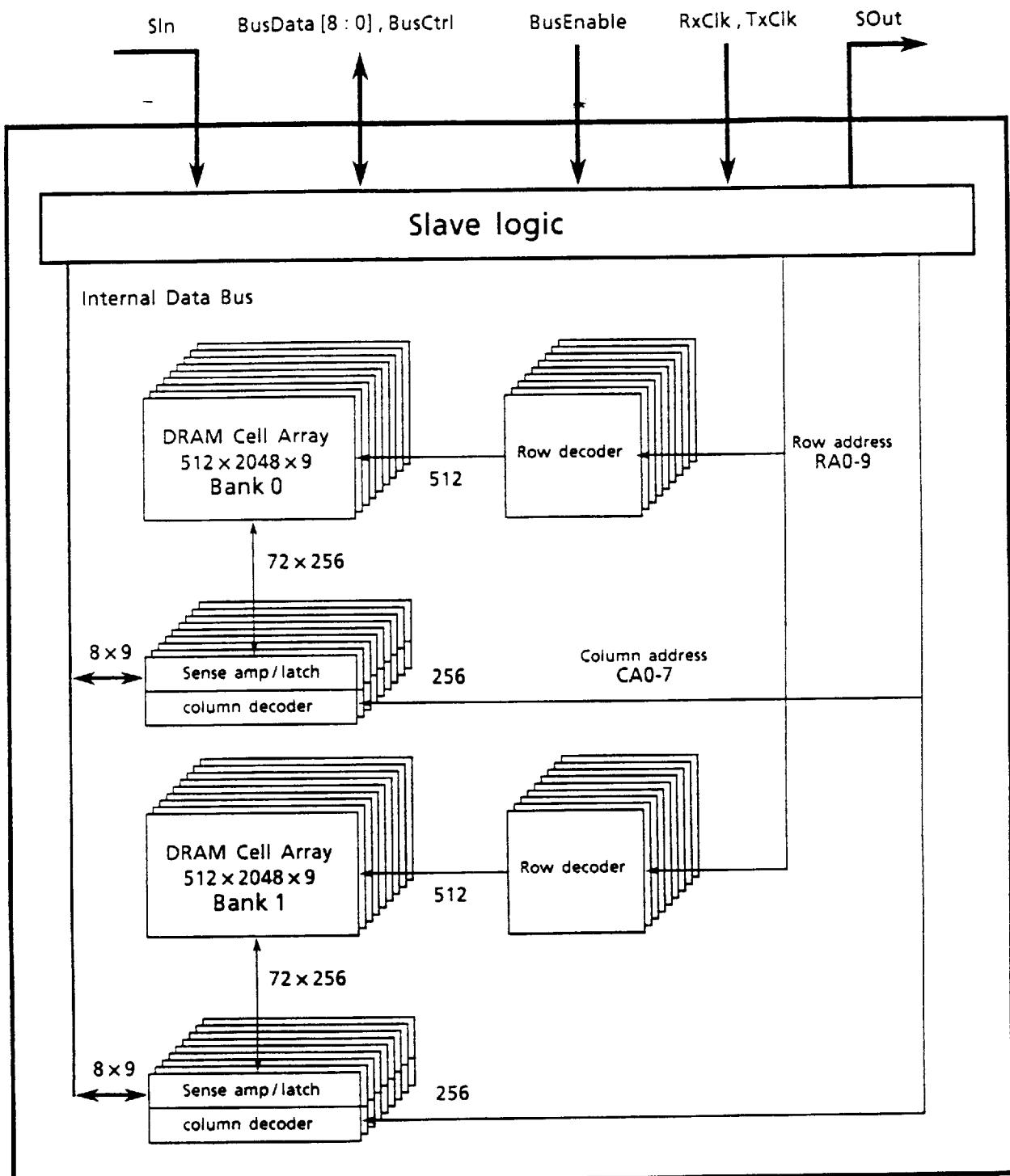
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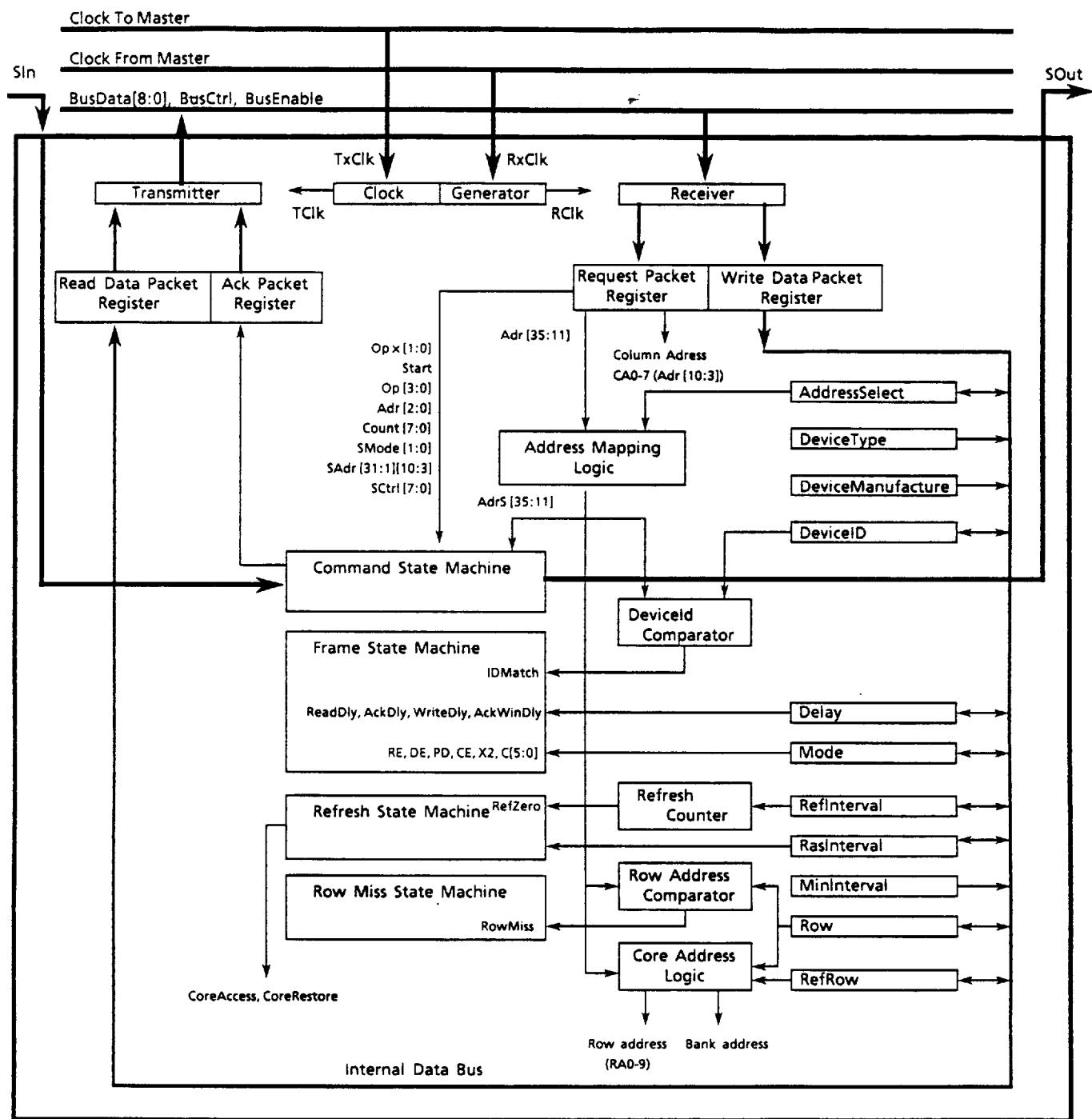


Internal Block Diagram of RDRAM

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Internal Block Diagram of Slave Logic

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## Maximum Ratings

Symbol	Item	Ratings	Unit	Note
V <sub>IN</sub>	Input Voltage	-0.5~V <sub>DD</sub> +0.5	V	1
V <sub>IN</sub>	Input Voltage (TTL)	-0.5~5.5	V	1
V <sub>DD</sub> , V <sub>DD-A</sub>	Power supply voltage	-0.5~6.5	V	1
T <sub>OPR</sub>	Operation temperature	0~70	°C	1
T <sub>STG</sub>	Storage temperature	-55~125	°C	1
T <sub>SOLDER</sub>	Soldering temperature	260	°C	1
P <sub>D</sub>	Power dissipation	3	W	1
I <sub>OUT</sub>	Output short-circuit current	50	mA	1

## RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C) Note 13

Symbol	Item	MIN.	TYP.	MAX.	Unit	Note
V <sub>DD</sub> , V <sub>DD-A</sub>	Power supply voltage	3.0	3.3	3.6	V	2
V <sub>REF</sub>	Reference voltage	1.9	2.2	2.4	V	2
V <sub>IH</sub>	High-level input voltage	V <sub>REF</sub> +0.35	-	V <sub>REF</sub> +0.4	V	2, 13
V <sub>IL</sub>	Low-level input voltage	V <sub>REF</sub> -0.4	-	V <sub>REF</sub> -0.35	V	2, 13
V <sub>IH</sub> (TTL)	High-level input voltage (S <sub>IN</sub> pin only)	2.0	-	5.5	V	2
V <sub>IL</sub> (TTL)	Low-level input voltage (S <sub>IN</sub> pin only)	-0.5	-	0.8	V	2

CAPACITANCE(V<sub>CC</sub> = 3.3V, f = 1MHz, Ta = 25

Symbol	Item	MIN.	MAX.	Unit
C <sub>I</sub>	Input capacity (RxClk,TxClk,Busble,V <sub>REF</sub> )	-	2	pF
C <sub>I</sub> (TTL)	Input capacity (S <sub>IN</sub> )	-	10	
C <sub>O</sub>	Output capacity (BusData[8:0],BusCtrl)	-	2	
C <sub>O</sub> (TTL)	Output capacity (S <sub>OUT</sub> )	-	15	

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D.C. Electrical Characteristics

Symbol	Item	MIN.	MAX.	Unit	Note
I <sub>CC</sub> 1	OPERATING CURRENT	-	220	mA	3, 4, 5
I <sub>CC</sub> 2	STANDBY CURRENT	-	65		3
I <sub>CC</sub> 3	REFRESH CURRENT	-	220		3, 5
I <sub>CC</sub> 4	MEAN OPERATING CURRENT (Typical)	TBD			13

Symbol	Item	MIN.	MAX.	Unit	Note
V <sub>OH</sub>	High-level output voltage	V <sub>ref</sub> + 0.4	-	V	
V <sub>OL</sub>	Low-level output voltage	-	V <sub>ref</sub> - 0.4		
V <sub>OH</sub> (TTL)	High-level output voltage (SOut only)	2.4	V <sub>dd</sub>		
V <sub>OL</sub> (TTL)	Low-level output voltage (SOut only)	0.0	0.4		
I <sub>OL</sub>	Output current (at low-level output)	-	35		mA
I <sub>OH</sub>	Output current (at high-level output)	-10	10		μA
I <sub>I(L)</sub>	Input leak current	-10	10		μA
I <sub>O(L)</sub>	Output leak current	-10	10		μA
I <sub>REF</sub>	V <sub>ref</sub> current	-10	10		μA

A.C. Permissible Operating Conditions and Characteristics

Symbol	Item	MIN.	MAX.	Unit	Note
t <sub>CR</sub> , t <sub>CF</sub>	Rise time and fall time of TxClk and RxClk	0.3	0.7	ns	7
t <sub>QR</sub> , t <sub>QF</sub>	Rise time and fall time of output data	0.4	0.6		
t <sub>CYCLE</sub>	TxClk and RxClk cycle times	4	5		
t <sub>TIK</sub>	Data transfer time	0.5	0.5	t <sub>CYCLE</sub>	8
t <sub>CH</sub> , t <sub>CL</sub>	High-level and low-level time of TClk and RxClk	45%	55%	t <sub>CYCLE</sub>	
t <sub>TR</sub>	TxClk-RxClk differential	0	t <sub>CYCLE</sub> - 0.6		
t <sub>S</sub>	Data setup time for RxClk	0.35	-	ns	
t <sub>H</sub>	Data hold time for RxClk	0.35	-		
t <sub>Q</sub>	Data output time for TClk	(1-0.4)(t <sub>CYCLE</sub> /4)	(1-0.4)(t <sub>CYCLE</sub> /4)		
t <sub>REF</sub>	Refresh Interval		32	ms	
t <sub>LOCK, ACTIVE</sub>	Lock time of interval clock generator in ActiveMode		750	t <sub>CYCLE</sub>	11
t <sub>LOCK, STANDBY</sub>	Lock time of interval clock generator in StandbyMode		750	t <sub>CYCLE</sub>	11

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## RDRAM Access Timing

Symbol	Description	MIN.	MAX.	Unit	Note
tCYCLE	TxClock and RxClock cycle-times	4	5	ns	tCYCLE
tRESPONSE	Time from start of request packet to start of read data packet (row hit)	7	10		
tREADHIT	Time from start of request packet to start of write data packet (row hit)	10	41		
tWRITEHIT	Interval between row miss and sending of next request packet	4	35		
tRETRYSENED CLEAN	Start of request packet for row miss (Nack) to start of request packet for row hit. The previous row is unmodified	21			
tRETRYSENED DIRTY	Start of request packet for row miss (Nack) to start of request packet for row hit. The previous row is modified	29			
tREADBURST32	Time from start of request packet to end of 32-byte read data packet (row hit)	26			
tREADBURST256	Time from start of request packet to end of 256-byte read data packet (row hit)	138			
tWRITEBURST32	Time from start of request packet to end of 32-byte write data packet (row hit)	20			
tWRITEBURST256	Time from start of request packet to end of 256-byte write data packet (row hit)	132			
tPOSTREGWRITEDELAY	Delay from the end of the current transaction to the beginning of the next transaction	4			
tPOSTMEMWRITEDELAY	Delay from the end of the current transaction to the beginning of the next transaction	2			
tSERIALREADOFFSET	Delay from the beginning of a serial address subpacket or serial control packet	13		tCYCLE	
tSERIALWRITEOFFSET	Delay from the beginning of a serial address subpacket or serial control packet to the beginning of the read data subpacket	5		tCYCLE	

## Row Miss and Refresh Parameters

symbol	Description	MIN.	MAX.	Unit	Note
RowOverhead	Overhead time (Standard value)	9	-	tCYCLE	
RowPrecharge	Minimum precharge time (Standard value) (既定値)	9	-	tCYCLE	
RowSense	RasInterval [ 1 ] [ 4 : 0 ] register	8	-	tCYCLE	
tRAS	RAS pulse width	60	-	ns	

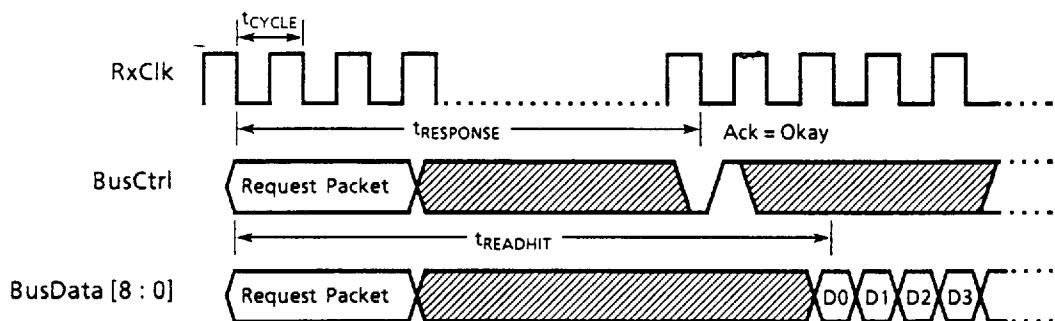
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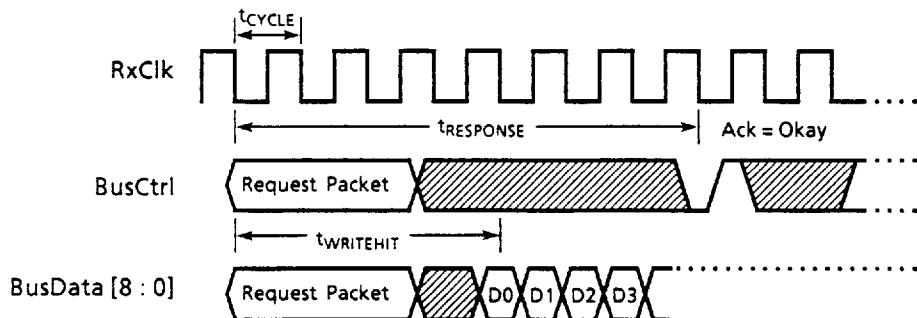
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Access Timing Chart

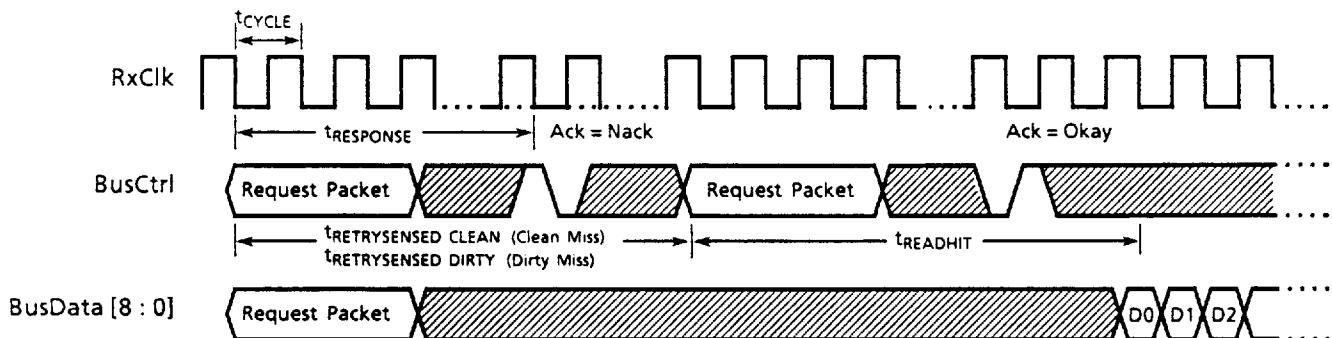
## 1. Read Timing (Row Hit)



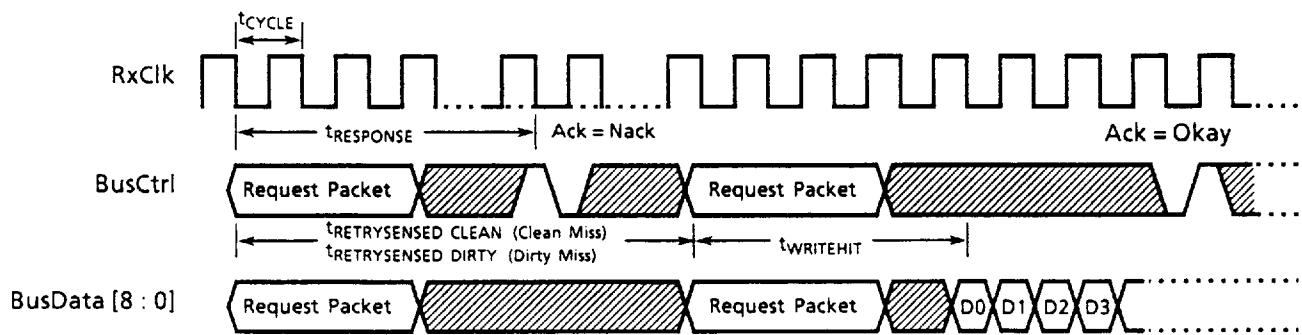
## 2. Write Timing (Row Hit)

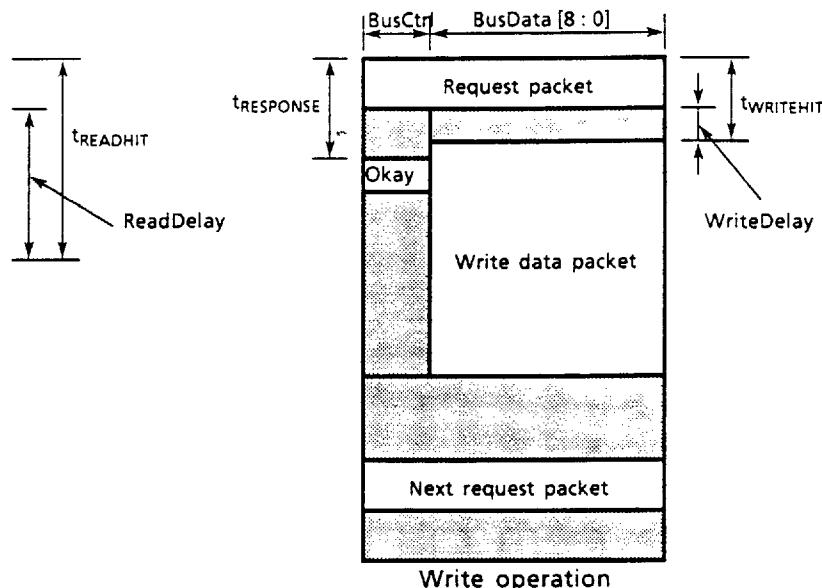
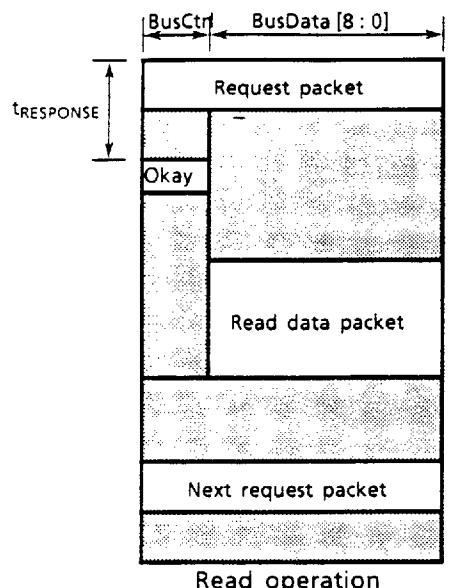
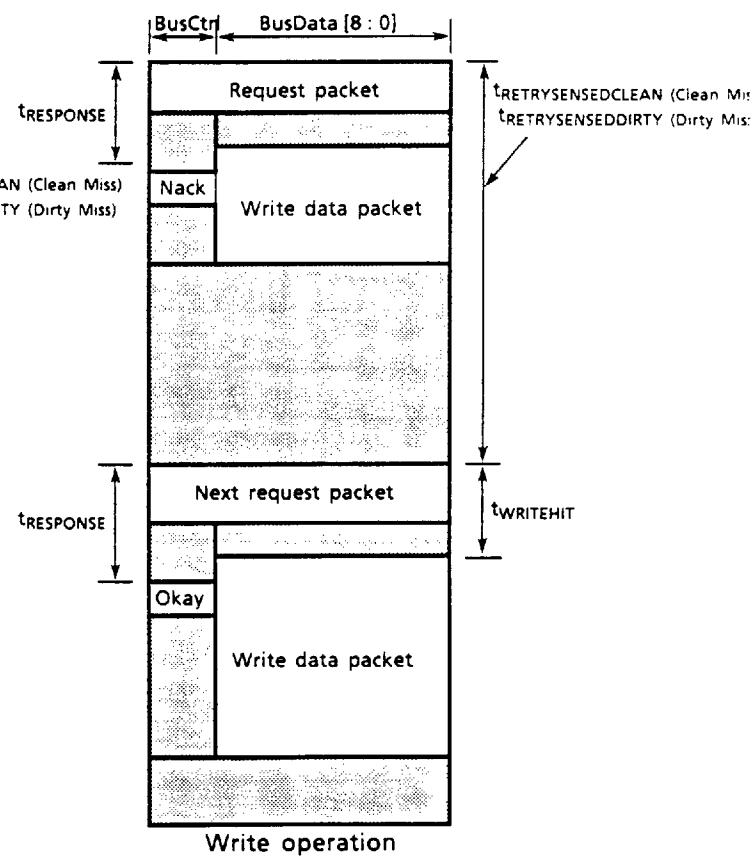
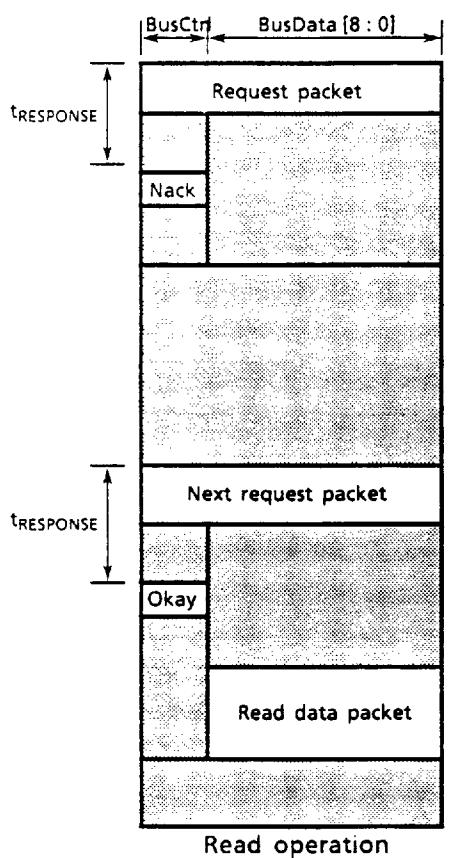


## 3. Read Timing (Row Miss)

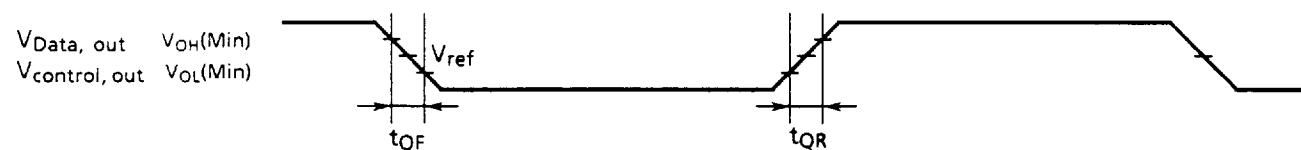


## 4. Write Timing (Row Miss)

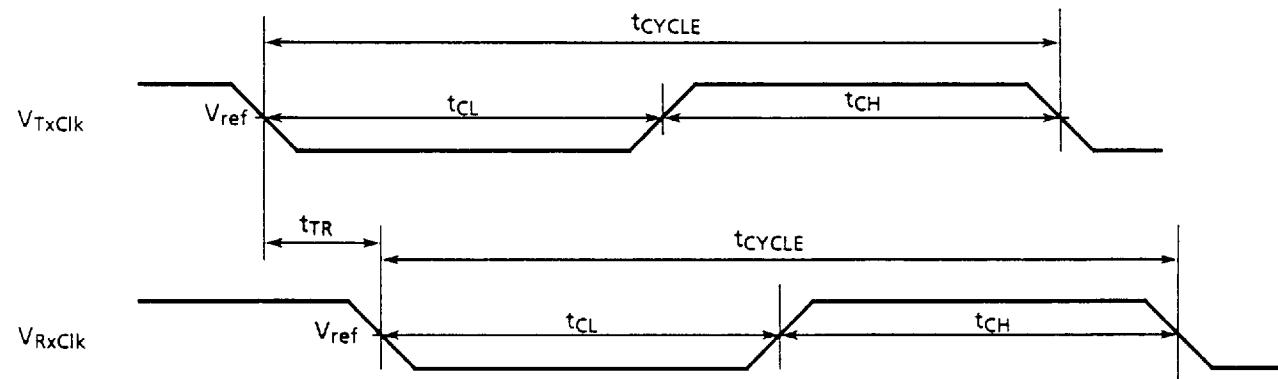


Access Time For Row Sense Amp Cache HitAccess Time For Row Sense Amp Cache Miss

Rise and Fall Timing in I/O Waveform



TxClk, RxClk timing



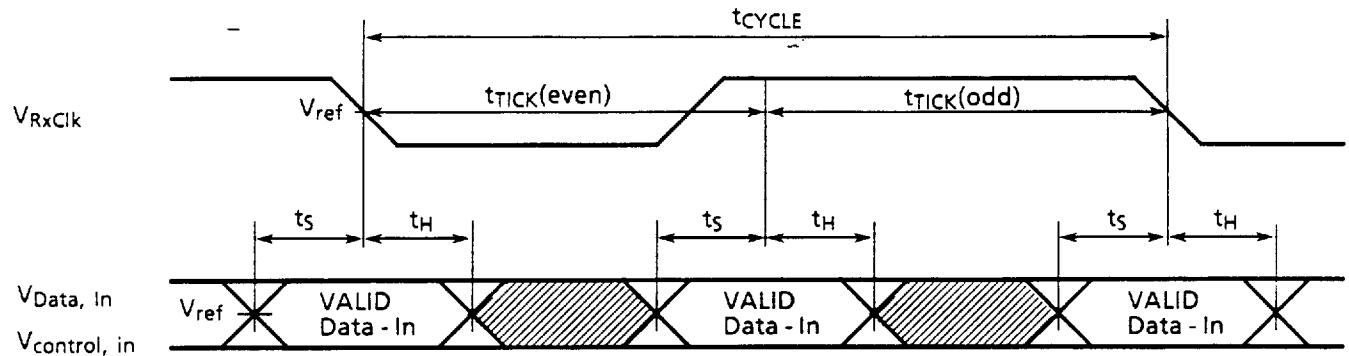
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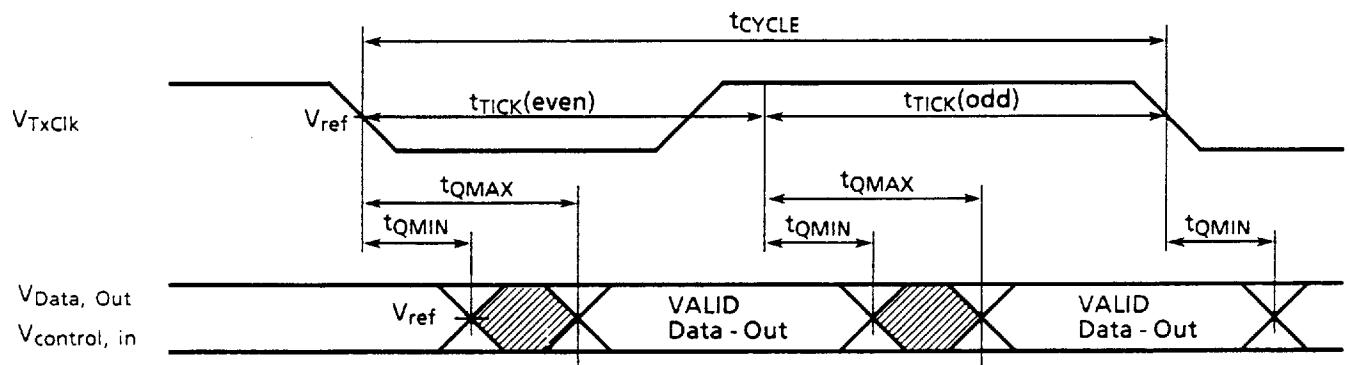
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Write Data Set up and Hold timing for RxClk



Read Data Output Timing for TxClk



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1. Stress greater than the maximum rated value may subject the device to permanent damage.
2. All voltages are given with GND as the reference.
3. These values do not include the BusData[8:0] or BusCtrl output currents.
4. This value is valid when 16 bytes of data are written to memory when the row sense amp cache is hit.
5. These values are valid when  $t_{CYCLE} = 4\text{ns}$ . They are strongly affected by the value of  $t_{CYCLE}$ .
6. The low - level output current is the current when the RDRAM outputs logical level "1".  
This parameter can be set in the mode register in the slave logic.
7. Vref is used as the reference voltage when measuring the input signal timing.
8. Calculated from the following conditions :  $t_{CYCLE} = 4\text{ns}$ , and  $t_{RP}(\text{Min})$ ,  $t_{RP}(\text{Max})$ , and RowOverhead =  $2t_{CYCLE}$ .
9. Value calculated from tREADHIT (Min).
10. Value calculated from tWRITEHIT (Min).
11. These values are  $3\mu\text{s}$  when  $t_{CYCLE}=4\text{ns}$ .
12. These values are the average operation current for graphics apprication systems.
13. Data input swing =  $V_{ref} \pm 0.35\text{V}$  min.  
Clock input swing = 1 Volt min peak to peak, 425mV min from Vref.

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**[1] PIN FUNCTIONS****Bus Data I/O : Bus Data[8:0]**

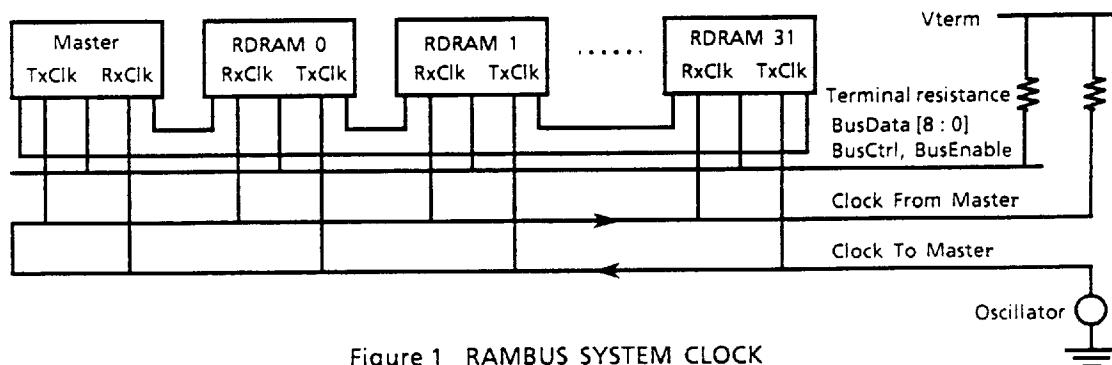
This pin is used for inputting request packets and write data packets, and for outputting read data packets. The signal level is referenced to Vref, low - level being logical "1", high - level being logical "0".

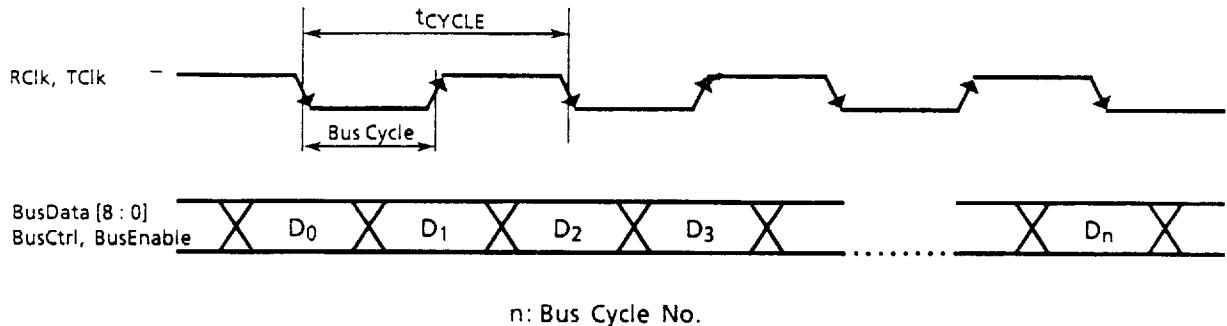
**Bus Control I/O : Bus Ctrl**

This pin is used for request packet input and acknowledge packet output. The signal level is referenced to Vref, low - level being logical "1", high - level being logical "0".

**Bus Enable Input : Bus Enable**

This pin is used for selecting the Rambus DRAM (RDRAM) operating mode (reset, active, standby, or power - down). Transition among the four modes is mainly achieved by varying the length of signal input (pulse width). When no signal is input, standby mode is automatically selected. Active mode is selected with a narrow signal pulse, while reset mode is selected by a wider pulse width. The signal level is referenced to Vref, low - level being logical "1", high - level being logical "0".

**Figure 1 RAMBUS SYSTEM CLOCK**



n: Bus Cycle No.

Figure 2 BUS CYCLE

#### High-Speed Sync Clocks: RClk and TClk

These are high-speed sync clocks for input and output data. RClk is used for input data, TClk is used for output data. In the Rambus system, both clock edges are used for sending data (see Figure 2). The rate between clock edges is known as the bus cycle, with data sent on the trailing edge being known as even bus cycle data and data sent on the leading edge being known as odd bus cycle data. RDRAM access is all referenced to the even bus cycle (trailing edge of clock).

In Rambus systems using RDRAM, skewing between clock signals and data signals must be minimized in order to achieve high-speed data transfer. For this reason, the clock signal line is looped as shown in Figure 1 as the ClockFromMaster and ClockToMaster. In addition, the clock signal line and the data signal line must be arranged in parallel so as to have the same impedance. In Figure 1, the clock traveling from the RDRAM (RDRAM31) at the end of the bus toward the master is known as the ClockToMaster, while that traveling back from the master to the RDRAM is called the ClockFromMaster. Because ClockToMaster is used as the sync clock when sending data from the RDRAM to the master, ClockToMaster becomes TClk at the RDRAM and RClk at the master. Vice versa, when data is sent from the master to the RDRAM, ClockFromMaster becomes the sync clock and is TClk at the master and RClk at the RDRAM.

	Master	RDRAM
ClockToMaster	RxClk	TxClk
ClockFromMaster	TxClk	RxClk

The use of this clock system means that the data and clock are always in the same direction, minimizing any skewing between them.

Serial Signal Input and Output: SIn and SOut

These signals are used to initialize the RDRAM and to create the Rambus daisy chain.

These signals are the only RDRAM active signals that are CMOS level low-speed signals.

In the Rambus system, each device (RDRAM) must be initialized after powering up. The process of initialization requires the allocation of unique addresses (DeviceID) to each RDRAM in the group. This is achieved continuously using SIn and SOut. SIn and SOut link the whole system as a daisy chain (see Figure 3). In addition to initialization, SIn and SOut are also used for refresh clock input when the RDRAM are in the power-down operating mode. They are not otherwise used in normal operation.

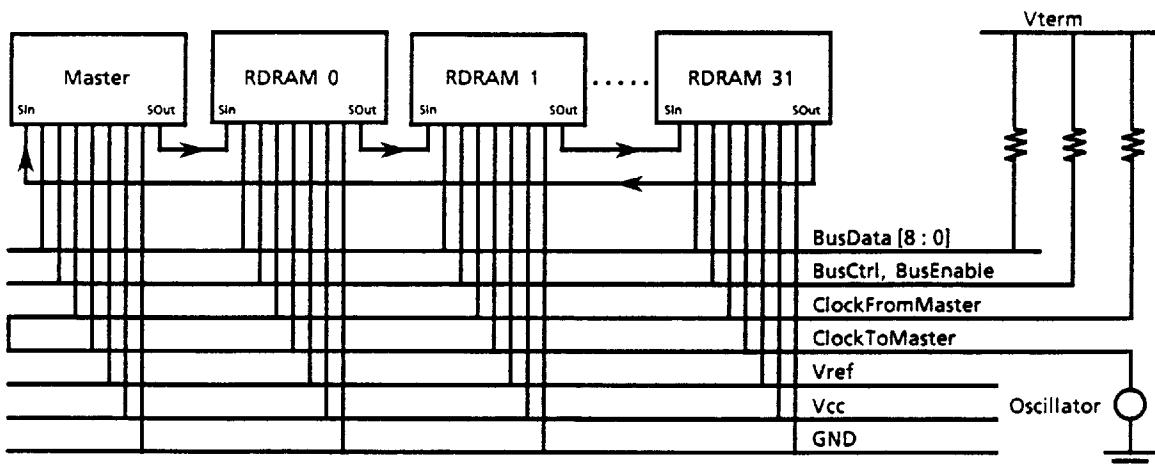


Figure 3 RAMBUS SYSTEM

Reference Voltage: Vref

This is the reference level for the high-speed small-amplitude signals (BusData [8 : 0], BusCtrl, BusEnable, RClk, and TClk) used by the RDRAM. When an input signal level is higher than Vref, it is logical "0"; when lower, it is logical "1".

Post

These pins support the package. They are not electrically connected to the chip.

NU (Not Usable)

This pin is connected internally to the lead frame. Because this pin outputs the board potential, do not connect it electrically.

## [2] RDRAM Basic Operation

RDRAM access is basically accomplished using request packets, acknowledge packets, and data packets. A packet is a group of contiguous bits sent via the 10 I/O bus lines of BusCtrl and BusData [8 : 0]. These packets play the following roles.

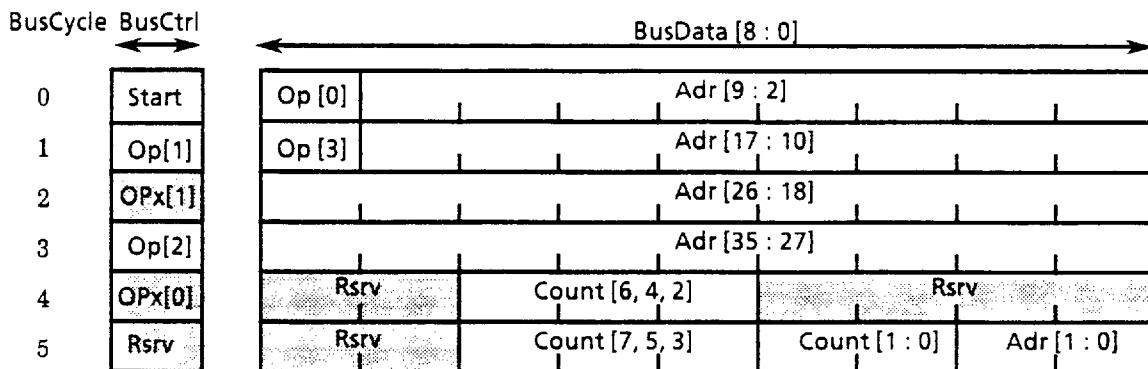


Figure 4 STRUCTURE OF REQUEST PACKET

## (1) Request Packet

The request packet is the first packet sent when accessing RDRAM. The request packet, which is made up of 6 cycles  $\times$  10 bits of data, includes RDRAM address information, the write / read data packet size, the operation command (to select reading or writing to memory or register), and the mask command for the write data. Figure 4 shows the request packet structure.

## · Start

The start bit shows the start of a request packet and is a logical "1" (low level electrically). Thus, the RDRAM interprets the output of a "1" on the BusCtrl line as the start of a request packet.

## · Adr [35 : 3] (= Address [35 : 3])

The adr bits show the address requested by the master. As shown in Table 1, the 33-bit address space includes the device ID address and bank address, and the row address and column address.

Table 1 ADDRESS SPACE OF REQUEST PACKET

	Memory space	Register space
Adr [10 : 3]	Column address	Register address
Adr [19 : 11]	Row address	Don't Care
Adr [20]	Bank address	Don't Care
Adr [35 : 21]	Device ID address	Device ID address

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## · Op [3:0]/OPx[1:0] (= Operation Command)

These bits select the RDRAM operation command. Table 2 shows the operations for Op[3:0]/OpX[1:0].

**Table 2 Operation Commands**

Op [3:0]	OpX [1:0]	Name	Description of Operation
0000	00	Rseq	Read sequential data from memory space
0000	01	Rnsq	Read non - sequential data from memory space.
0100	00	WseqNpb	Write sequential data to memory space with no per - bit mask
0100	01	WseqDpb	Write sequential data to memory space with data - per - bit masking
0100	10	WseqBpb	Write sequential data to memory space with both - per - bit masking
0100	11	WseqMpb	Write sequential data to memory space with mask - per - bit masking
0110	00	Rreg	Read sequential data from reg. space
0111	00	Wreg	Write sequential data to reg. space
1000	00	WnsqNpb	Write non - sequential data to mem. space with no per - bit mask.
1000	01	WnsqDpb	Write non - sequential data to memory space with data - per - bit masking.
1000	10	WnsqBpb	Write non - sequential data to memory space with mask - per - bit masking.
1000	11	WnsqMpb	Write non - sequential data to memory space with mask - per - bit masking
1100	00	WbnsNpb	Write non - sequential data to memory space with byte masking and no per - bit mask operation.
1100	01	WbnsDpb	Write non - sequential data to memory space with byte masking.
1100	11	WbnsMpb	Write non - sequential data to memory space with byte masking and mask - per - bit masking.
1111		WregB	Broadcast write to reg. space of all responding devices with no acknowledge permitted.

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## · Count [7:3]

The count bits show the size of the write/read data packet. The oct-byte (OB) unit is used as the unit of data packet size. A value between 1OB (8 bytes) and 32OB (256 bytes) can be specified.

Count [7:3]=00000 means 1OB, Count [7:3] = 00001 means 2OB, Count [7:3] =11111 means 32OB.

## · Adr [2:0] / Count [2:0]

These bits select master information for the write data. Adr[2:0] and Count[2:0] are the mask information for the first and last OB in the write packet.

## · Rsrv ( Reserved )

These bits are unused. Use the master to set them to "0" when a request is issued.

## (2) Acknowledge Packet

The acknowledge packet (Ack[1:0]) is the RDRAM response signal to the request packet. Table 3 shows the meaning of the respective Ack[1:0] signals.

Table 3 ACKNOWLEDGE PACKET

Ack [1:0]	Command	Description
00	Nonexistent	Nonexistent shows that no RDRAM has the requested address if no output is detected on the BusCtrl line within a set time after the end of the request packet.
01	Okay	Okay shows the completion of receipt of the request packet.
10	Nack	Nack shows that the requested device cannot respond to the request. Nack is output for RDRAM in the case of a row miss or refresh, etc. If a Nack is returned, the master waits before sending the request again.
11	Reserved	Reserved is not currently used. RDRAM does not output Reserved.

## (3) Data Packet

The data packet is a group of contiguous write or read data for memory or register address space. The data packet consists of between 1OB(8 bytes) and 32OB(256 bytes). (It is always 1OB when reading or writing to registers.)

## (4) Serial Mode Packet

The serial mode packet(SMode[1:0]) controls the state of the Count00[7:0] and Count11[7:0] counters. These counters cause operating mode transitions when they reach special values.

Figure 5 shows the format of the serial mode packet.

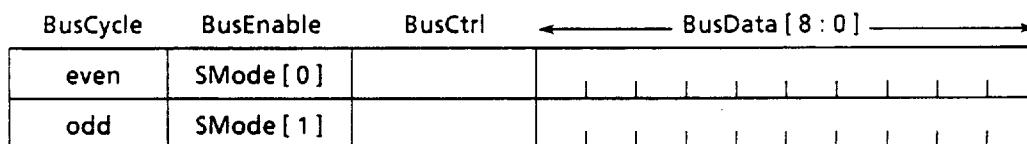


Figure 5. Serial Mode Packet Format

Table 4 shows the meaning of SMode[1:0] signals

Table 4. Serial Mode Fields

SMode [1:0]	Description
00	Increments Count00[3:0], Clears Count11[7:0]
01	-
10	-
11	Increments Count11[7:0], Clears Count00[3:0]

## (5) Serial Address Packet

The serial address packet ( $SAdr[i][10:3]$ ) provides eight low-order address bits for each octbyte which is accessed in memory space. These eight address bits are transferred serially on the BusEnable pin on The RDRAM, thus these are called "a serial address. This packet is used in random access mode.

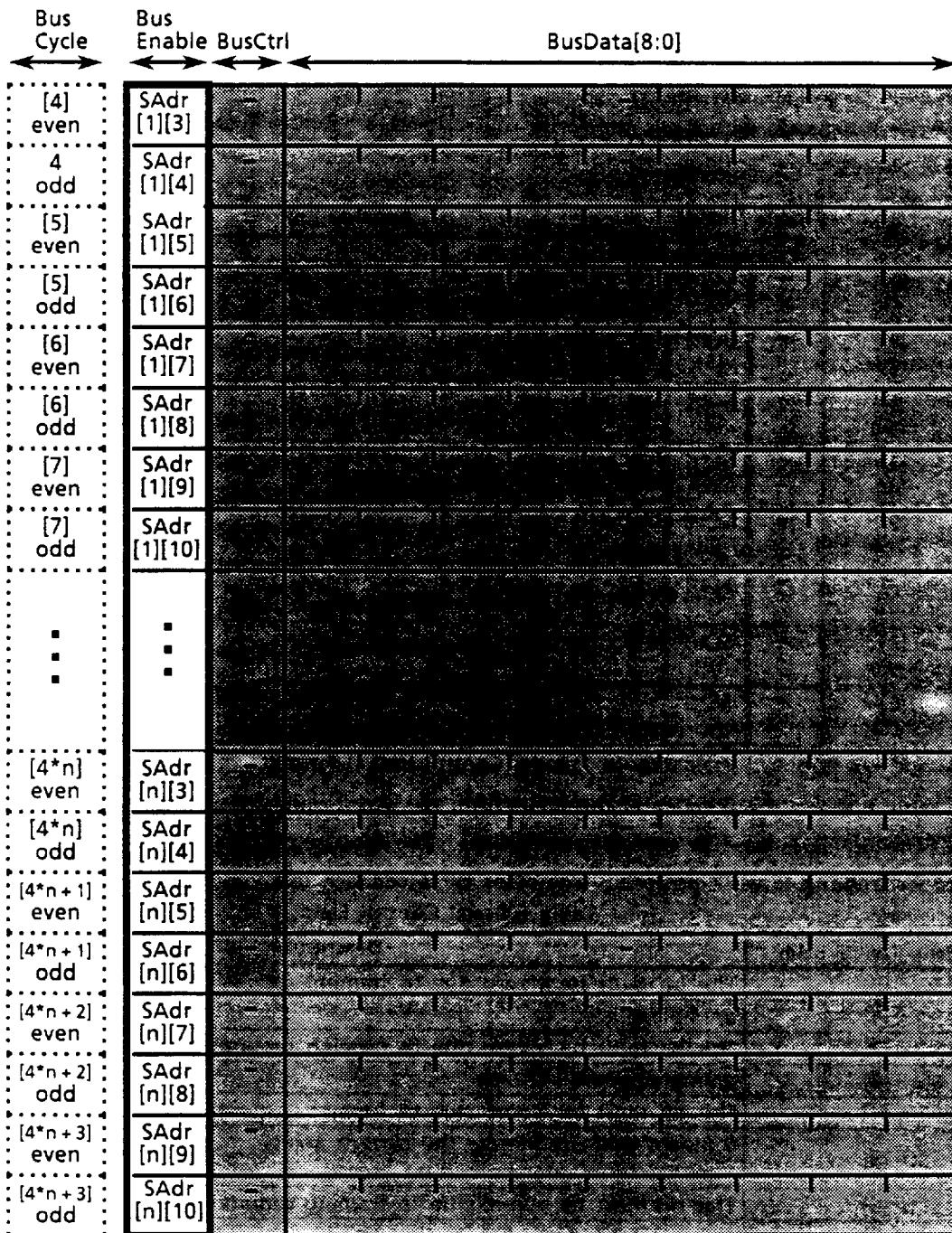


Figure 6. Serial Address Packet Format

Table 5 Serial Address Packet

Serial Address Fields	Description
SAdr[i][10:3]	Low-order address bits for each octbyte

## (6) Serial Control Packet

The serial control packet provides for the early termination of a memory space read or write transaction. It consists of eight bits transferred serially on the BusCtrl pin of the device. The commands which use this packet are all of those which access memory space. The register read and write commands do not use the serial control packet. Figure 7 shows the format of the serial control packet.

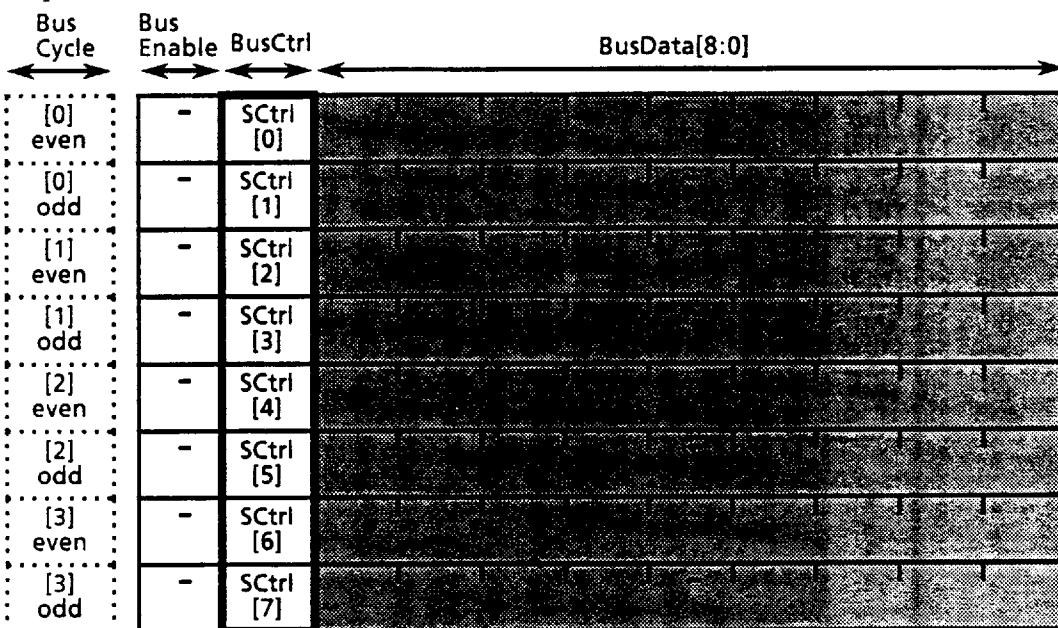


Figure 7 Serial Control Packet Format

Table 6 shows the function of the bits within the serial control fields.

The SCtrl[5] bit is used to control termination. The bits in the even bus ticks must be zero in order for framing to work properly. The other three odd tick bits are unimplemented.

Table 6 Serial Control Fields

Serial Control Fields	Description
SCtrl[0]	This bit must be a zero due to framing requirements
SCtrl[1]	unimplemented
SCtrl[2]	This bit must be a zero due to framing requirements
SCtrl[3]	unimplemented
SCtrl[4]	This bit must be a zero due to framing requirements
SCtrl[5]	0 means don't terminate the current access 1 means terminate the current access
SCtrl[6]	This bit must be a zero due to framing requirements
SCtrl[7]	unimplemented

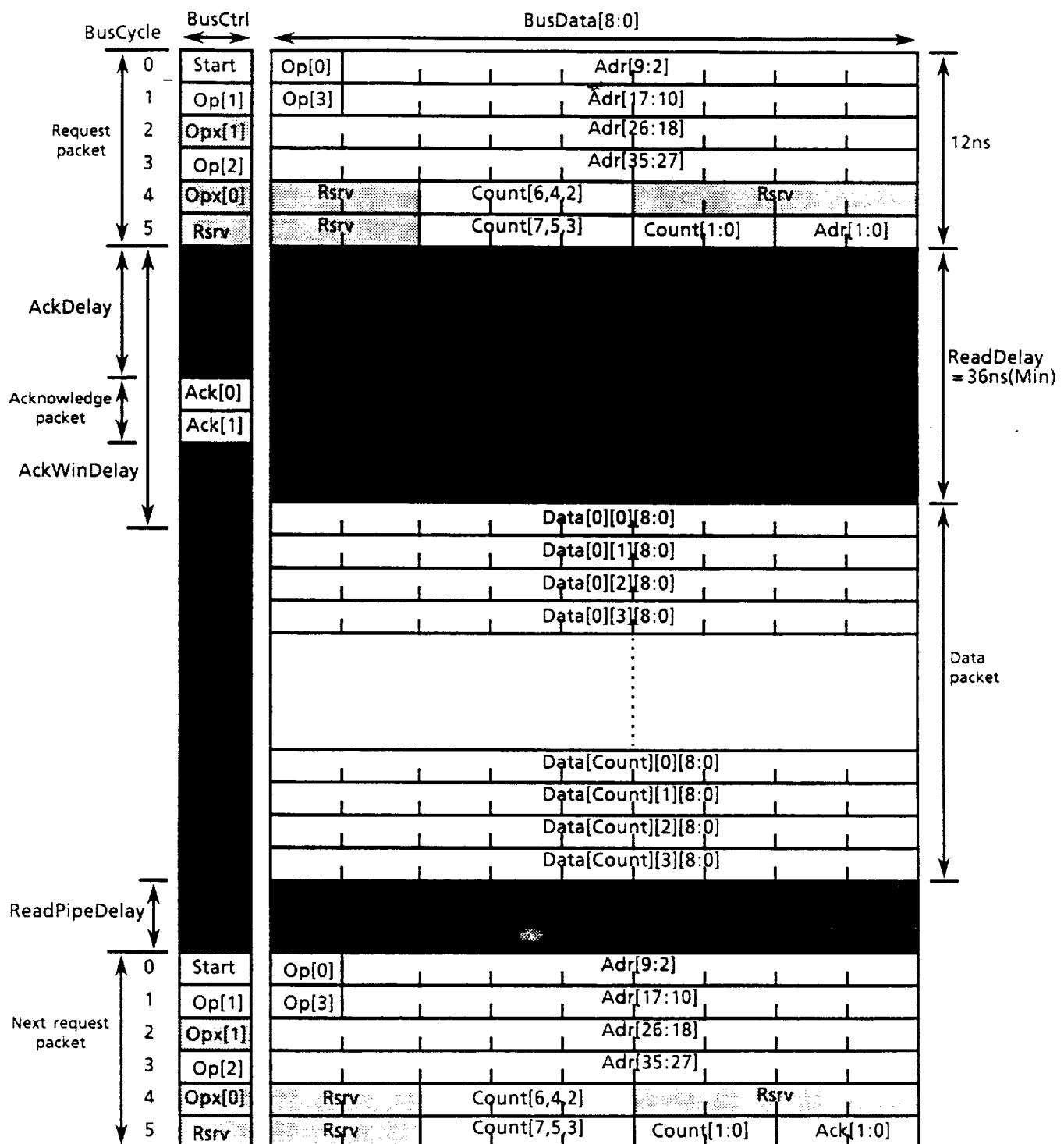


Figure 8. Read Operation for Memory or Register Address Space  
(Ackpacket = Okay)

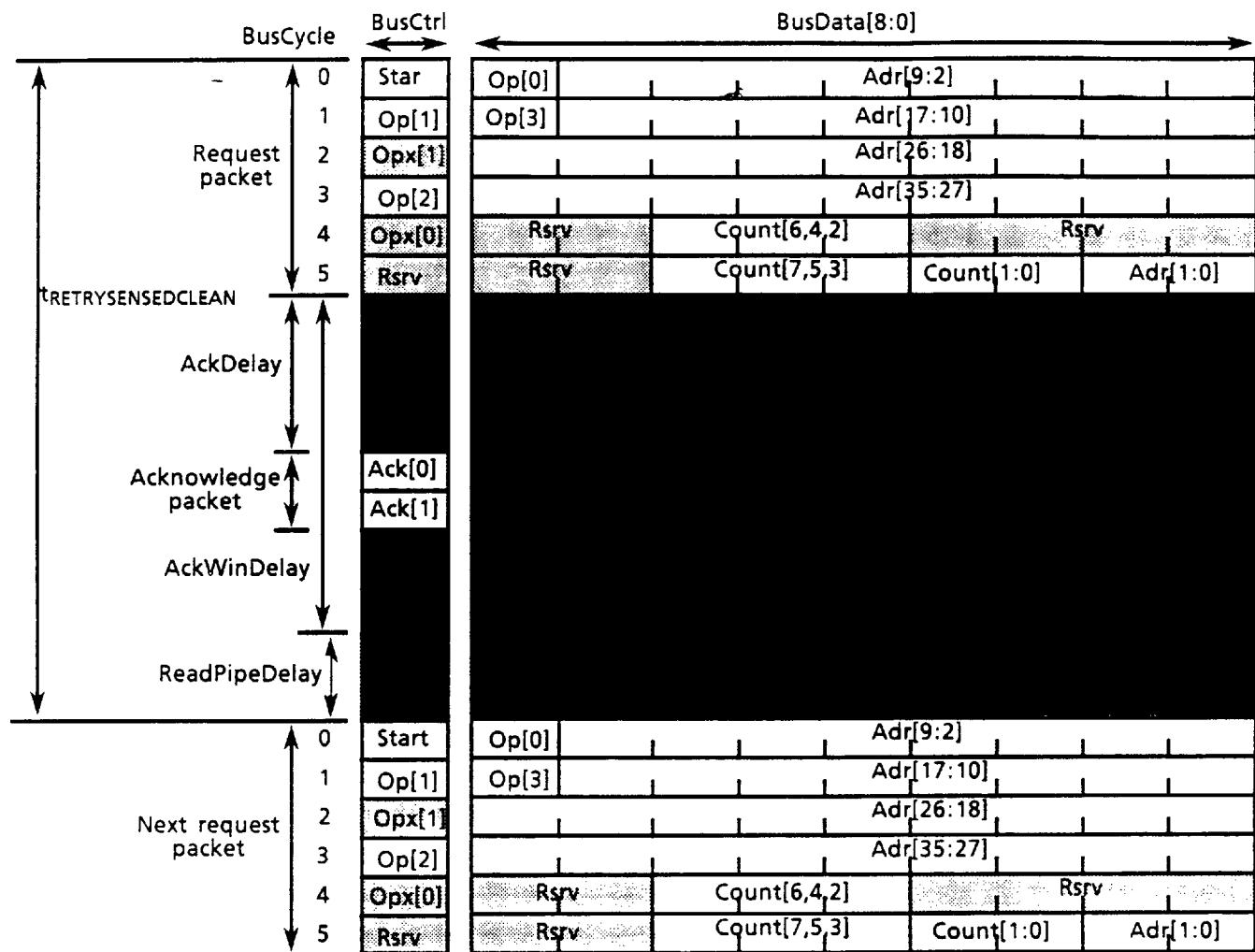


Figure 9. Read Operation for Memory or Register Address Space  
(Ack packet = Nack or Nonexistent)

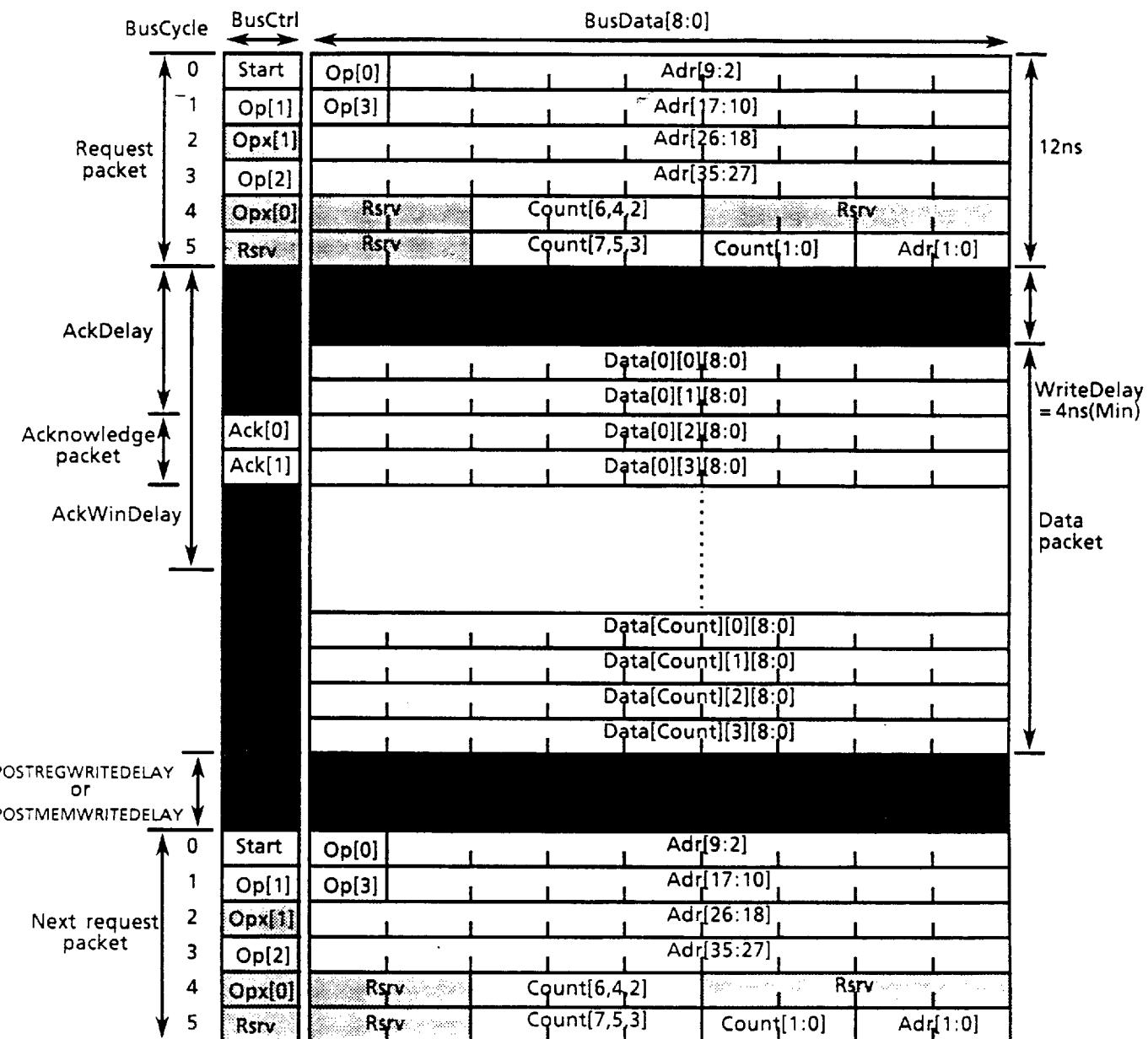


Figure 10. Write Operation for Memory or Register Address Space  
(Ack packet = Okay)

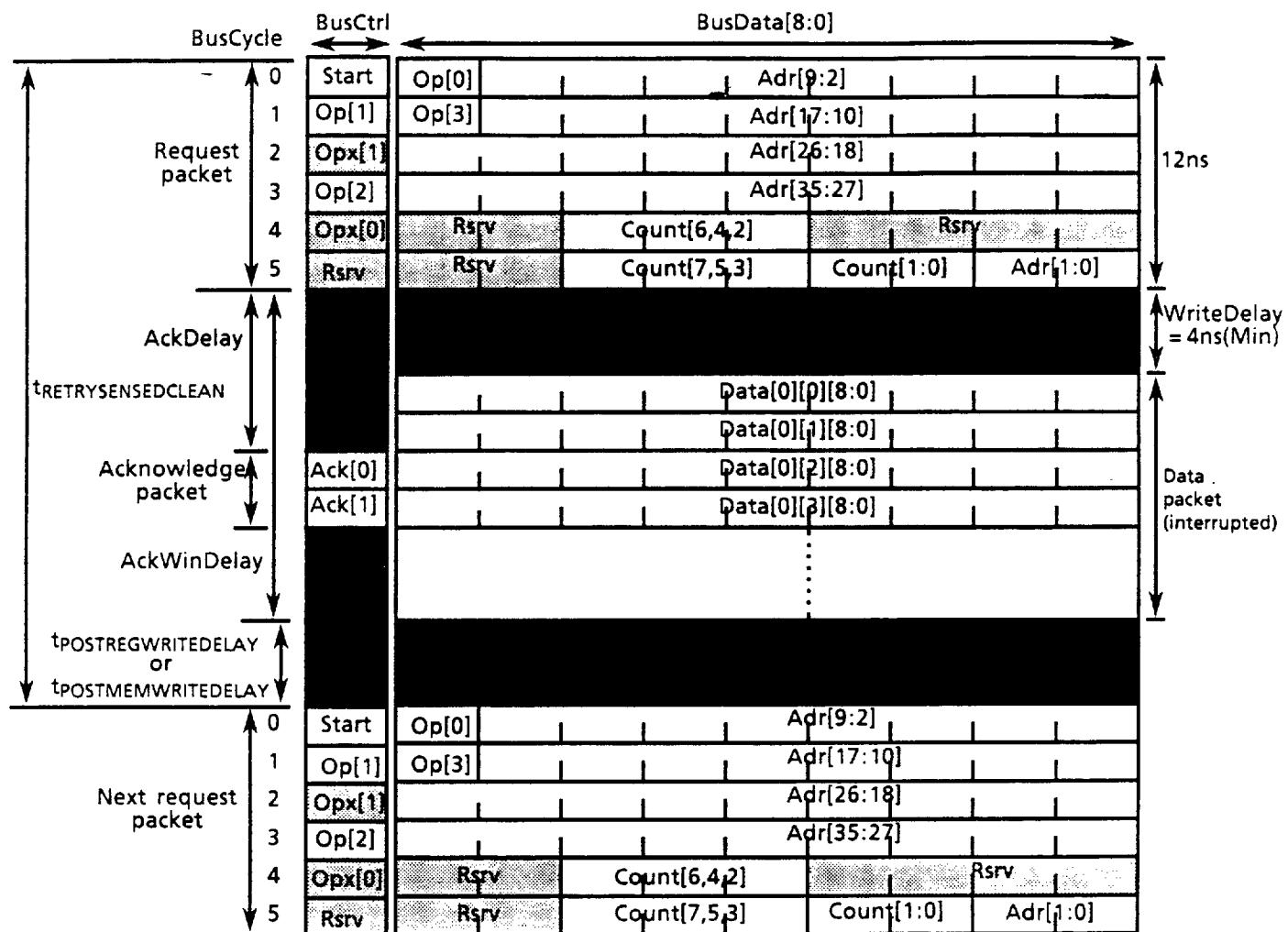


Figure 11. Write Operation for Memory or Register Address Space  
(Ack packet = Nack or Nonexistent)

**[3] Read Operation From Memory or Register****(1) Normal Read Operation**

Actual memory or register access using each of the packets is following. Figure 8 shows the process when a read operation is executed on the RDRAM memory or register space and the RDRAM sends an Okay Ack packet.

RDRAM access starts with a 6-cycle request packet transmission from the master. The RDRAM detects the request packet from the output (Start bit) on the BusCtrl line. On completion of the request packet, and after AckDelay, the RDRAM outputs a 2-cycle Ack packet.

All devices connected to the Rambus system ignore output on the BusCtrl line for a set interval (AckWinDelay) after the end of the request packet. Therefore, output of the Ack packet cannot be confused with the Start bit of the request packet.

When the RDRAM responds with an Okay Ack packet, the read data packet is output after a delay (ReadDelay) after the end of the request packet. The read operation ends at whichever is last, the end of the AckWindow (AckWinDelay delay after the end of the request packet) or the end of the data packet.

Next, if another operation is to be executed, it starts after a delay of ReadPipeDelay from the end of the preceding data packet. (The standard value of ReadPipeDelay is 0CYCLE.)

The values of AckWinDelay, AckDelay, ReadDelay, and WriteDelay can be programmed by accessing the Delay register in the slave logic.

**(2) Read Operations When Nack or Nonexistent is Returned**

As Figure 9 shows, no read data packet is output when the RDRAM returns a Nack or Nonexistent Ack packet in a read operation. When the Ack packet is Nack, the RDRAM prepares for another request packet to be sent. The time it takes to prepare depends on the cause of the Nack (row miss or refresh). In the case of a row miss, the preparation time is the time for row precharging (TROWPRECHARGE), row access (TROWSENSE) and RowOverhead. The value of tROWPRECHARGE and tROWSENSE can be programmed by accessing the RasInterval register in the slave logic. In the case of a refresh, an additional four row cycles are added. During this preparation interval, the RDRAM must wait for the master to output the next request packet.

When the Ack packet is Nonexistent (Ack[1:0] = "00", (that is, when no output is detected on the BusCtrl line within the AckWindow), either no RDRAM has the requested address or the it was not possible to confirm the requested memory or register space.

**(3) Read Operation Commands**

Rseq : Executes a read operation on the RDRAM memory space. The RDRAM configures a read data packet to send to the master.

Rreg : Executes a read operation on RDRAM register space. The RDRAM configures a read data packet to send to the master.

## [4] Write Operations to Memory or Registers

## (1) Normal Write Operation

In contrast to read operations, the write data packet is sent from the master before the Ack packet is output, as shown in Figure 10. When another operation is performed immediately after a write operation, it starts after a delay of tPOSTRGWRTEDELAY or tPOSTMEMWRITEDELAY from the end of the preceding data packet.

## (2) Write Operations When Nack or Nonexistent is Returned (see Figure 11)

In a write operation, the write data packet starts to be sent before the Ack packet is output. Therefore, if a Nack or Nonexistent Ack packet is output, the master interrupts the output of the write data packet.

## (3) Write Operation Commands

WnsqNpd : Executes a write operation on RDRAM memory space.

Wreg : Executes a write operation on RDRAM register space.

WregB : The RDRAMs can return a Nack, the master is able to confirm that there is a device under internal operation and cannot perform the write operation.

## [5]Random Access Mode

In this mode, non-contiguous blocks of memory can be accessed through the use of the read and write non-sequential operations. Using these commands, multiple eight-byte blocks(octbytes) of data within a cache line can be accessed in a non-sequential mode. To do this, the master device sends a request packet specifying a non-sequential operation along with the address of the first octbyte to be accessed.

The master device also generates a serial address packet on the BusEnable signal that specifies the address of the next octbyte. Successive serial address packets continue to specify new addresses in the cache line while data is continuously transferred until the access is complete.

Figure 12 shows a memory space read transaction for a command which uses the serial address packet. And figure 13 shows a memory space write transaction with serial address packet.

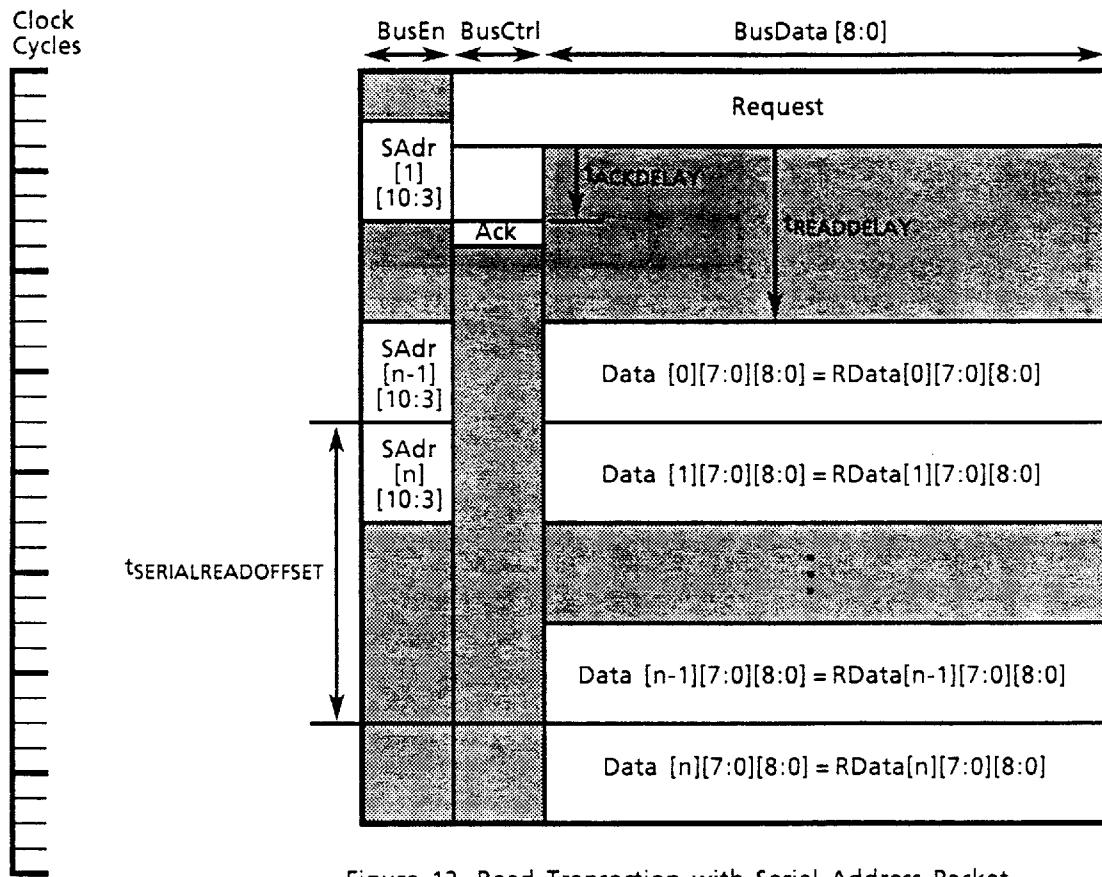


Figure 12 Read Transaction with Serial Address Packet.

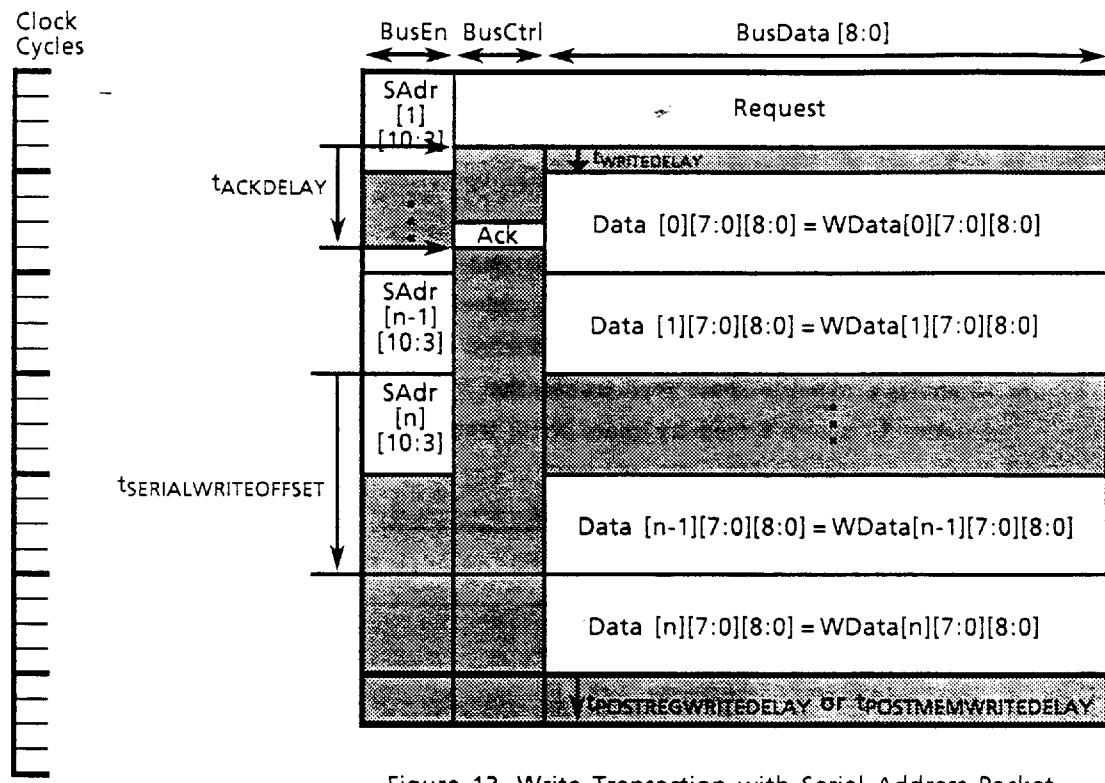


Figure 13 Write Transaction with Serial Address Packet

## [6]Serial Control Packet

The serial control packet provides for the early termination of a memory space read or write transaction before the specified data count (data packet length) in the Count[7:3] field has elapsed.

Figure 14 shows a memory space read transaction for a command which uses the serial control packet, and figure 15 shows a memory space write transaction with serial control packet.

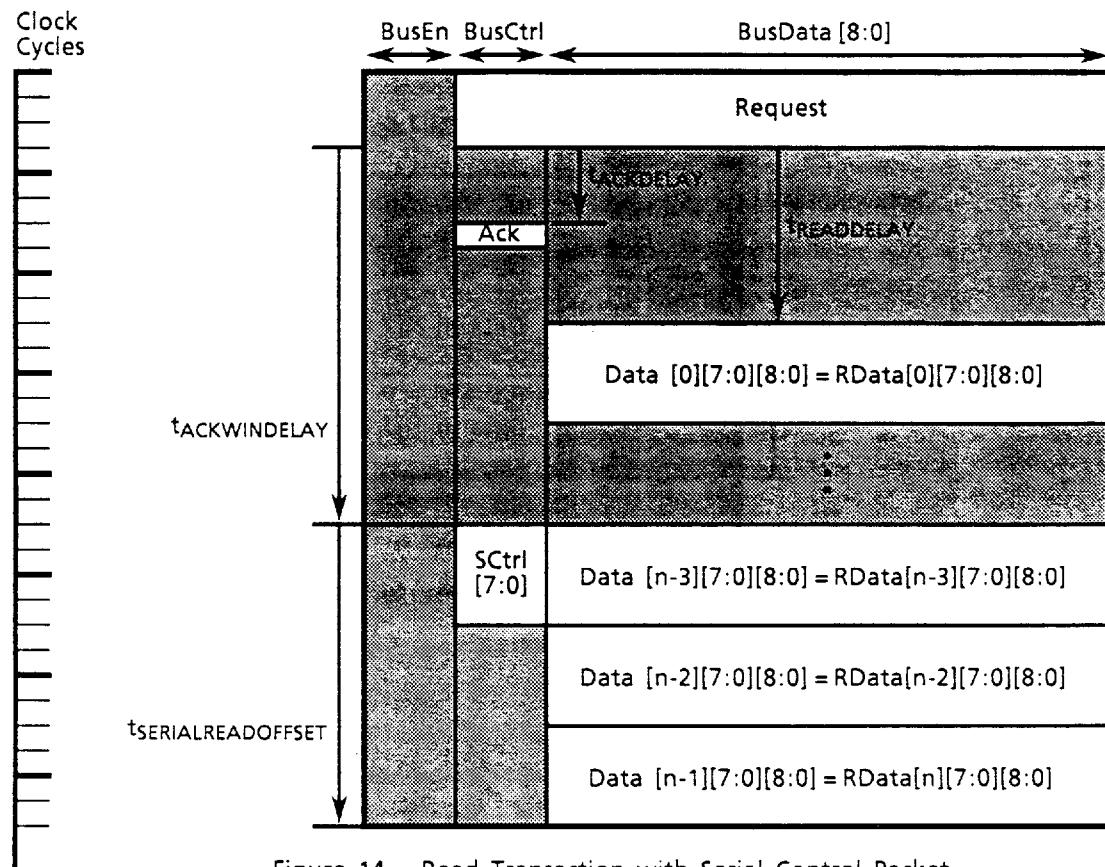


Figure 14 Read Transaction with Serial Control Packet

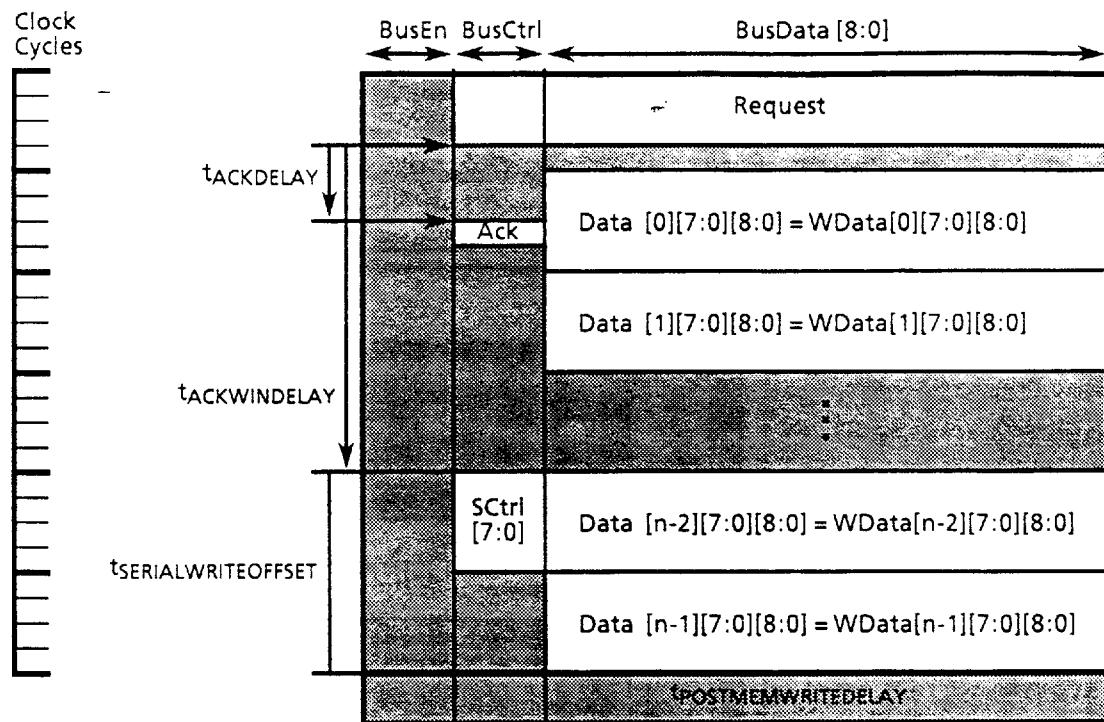


Figure 15 Write Transaction with Serial Control Packet

## [ 7 ] The Mask Function

The RDRAM mask function is valid for the first and last 1OB of write data packets. The mask information for each OB can be selected using Count [2 : 0] and Adr [2 : 0], as shown in Table 5.

Table 7 Mask Selection Bits

Mask information for 1st QB		Mask information for last OB	
Adr [2:0]	ByteMaskLS [7:0]	Count [2:0]	ByteMaskMS [7:0]
000	11111111	000	00000001
001	11111110	001	00000011
010	11111100	010	00000111
011	11111000	011	00001111
100	11110000	100	00011111
101	11100000	101	00111111
110	11000000	110	01111111
111	10000000	111	11111111

The "0"s in Table 7 indicate masking. All 1OBs other than the first and last are therefore "1111" (all are written). If the data packet is only 1OB (Count [7 : 3]=00000), the logical AND of Mask [7 : 4] and Mask [3 : 0] becomes the mask information, as shown in Table 8. In this case, the transmitted data can be controlled in 1-byte units. Figure 16 shows a masked write operation when sending 8 bytes.

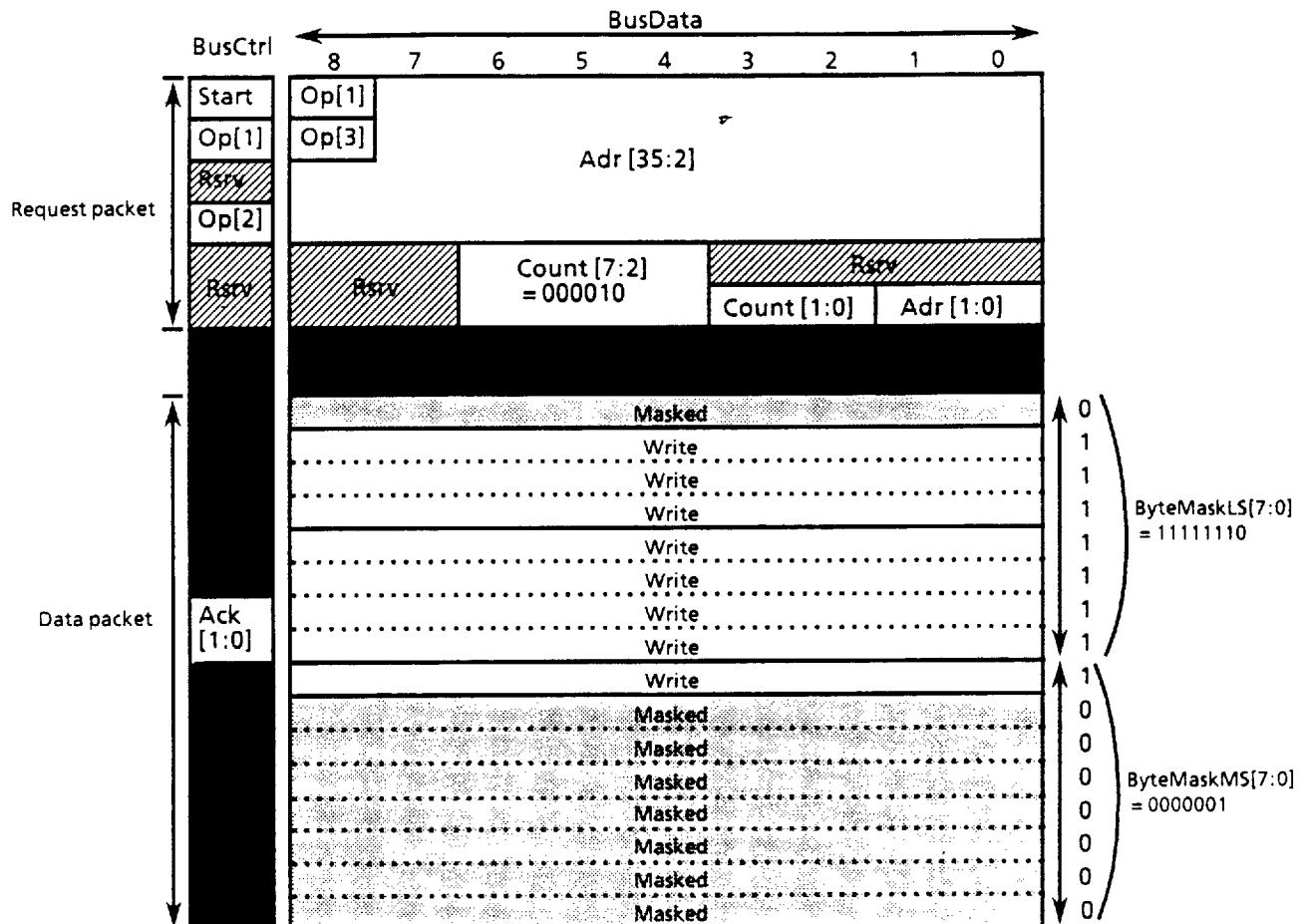


Figure 16 Mask Function

Table 8 Mask Selection bits and Size of Transmitted Data Packet

## • 1 Byte Transmission

Count [7:3]	Count [2:0]	Adr [2:0]	ByteMaskMS [7:0]	Middle ByteMask [7:0]	ByteMaskLS [7:0]	ByteMaskLS[7:0] and ByteMaskMS[7:0]
00000	000	000	00000001	n/a	11111111	00000001
00000	001	001	00000011	n/a	11111110	00000010
00000	010	010	00000111	n/a	11111100	00000100
00000	011	011	00001111	n/a	11111000	00001000
00000	100	100	00011111	n/a	11110000	00010000
00000	101	101	00111111	n/a	11100000	00100000
00000	110	110	01111111	n/a	11000000	01000000
00000	111	111	11111111	n/a	10000000	10000000

## • 2 Byte Transmission

Count [7:3]	Count [2:0]	Adr [2:0]	ByteMaskMS [7:0]	Middle ByteMask [7:0]	ByteMaskLS [7:0]	ByteMaskLS[7:0] and ByteMaskMS[7:0]
00000	001	000	00000011	n/a	11111111	00000011
00000	010	001	00000111	n/a	11111110	00000110
00000	011	010	00001111	n/a	11111100	00001100
00000	100	011	00011111	n/a	11111000	00011000
00000	101	100	00111111	n/a	11110000	00110000
00000	110	101	01111111	n/a	11100000	01100000
00000	111	110	11111111	n/a	11000000	11000000
00001	000	111	00000001	n/a	10000000	n/a

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## • 4 Byte Transmission

Count [7:3]	Count [2:0]	Adr [2:0]	ByteMaskMS [7:0]	Middle ByteMask [7:0]	ByteMaskLS [7:0]	ByteMaskLS[7:0] and ByteMaskMS[7:0]
00000	011	000	00001111	n/a	11111111	00001111
00000	100	001	00011111	n/a	11111110	00011110
00000	101	010	00111111	n/a	11111100	00111100
00000	110	011	01111111	n/a	11111000	01111000
00000	111	100	11111111	n/a	11110000	11110000
00001	000	101	00000001	n/a	11100000	n/a
00001	001	110	00000011	n/a	11000000	n/a
00001	010	111	00000111	n/a	10000000	n/a

## • 8 Byte Transmission

Count [7:3]	Count [2:0]	Adr [2:0]	ByteMaskMS [7:0]	Middle ByteMask [7:0]	ByteMaskLS [7:0]	ByteMaskLS[7:0] and ByteMaskMS[7:0]
00000	111	000	11111111	n/a	11111111	11111111
00001	000	001	00000001	n/a	11111110	n/a
00001	001	010	00000011	n/a	11111100	n/a
00001	010	011	00000111	n/a	11111000	n/a
00001	011	100	00001111	n/a	11110000	n/a
00001	100	101	00011111	n/a	11100000	n/a
00001	101	110	00111111	n/a	11000000	n/a
00001	110	111	01111111	n/a	10000000	n/a

## [8] Bit Masking

TC59R1809VK / HK supports three forms of bit masking that are available for write operations. These operations are referred to as data-per-bit(Dpb), mask-per-bit(Mpb), and both-per-bit(Bpb) masking.

## (1) Data-per-bit(Dpb) mode

In the Dpb operation, the MDReg is used to hold a static mask that is applied to all octbytes of data written to the RDRAM core.

Figure 17 shows the format of the Data-per-bit(Dpb) write transactions.

## (2) Mask-per-bit(Mpb) mode

In the Mpb operation, the MDReg is used to hold an octbyte of static data that is masked by dynamic bit masks supplied in the data packets before being written to RDRAM. Figure 18 shows the format of the Both-per-bit(Bpb) write transactions.

## (3) Both-per-bit(Bpb) mode

The Bpb operation requires data packets to alternate between mask and data octbytes. The even data packets carry bit masking information which is placed in the MDReg while the odd data packets carry the data to be masked by the latest contents on the MDReg. Figure 19 shows the format of the Both-per-bit(Bpb) write transactions.

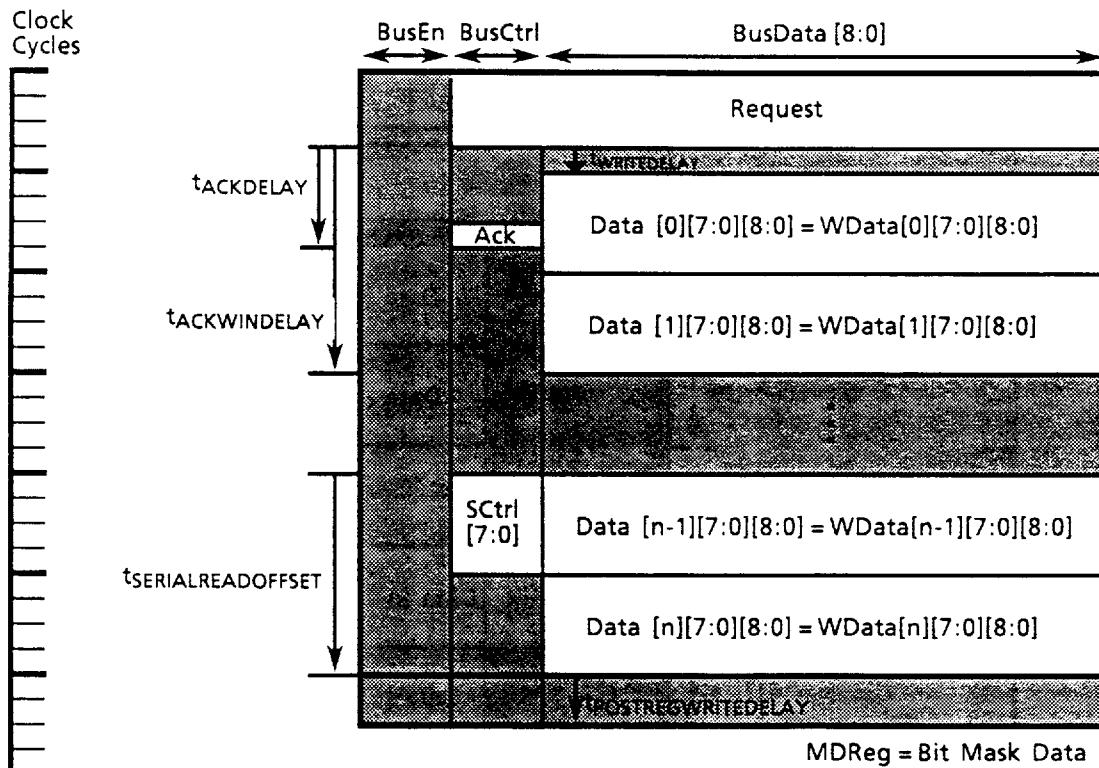


Figure 17 Data - per - bit (Dpb) Write Transactions

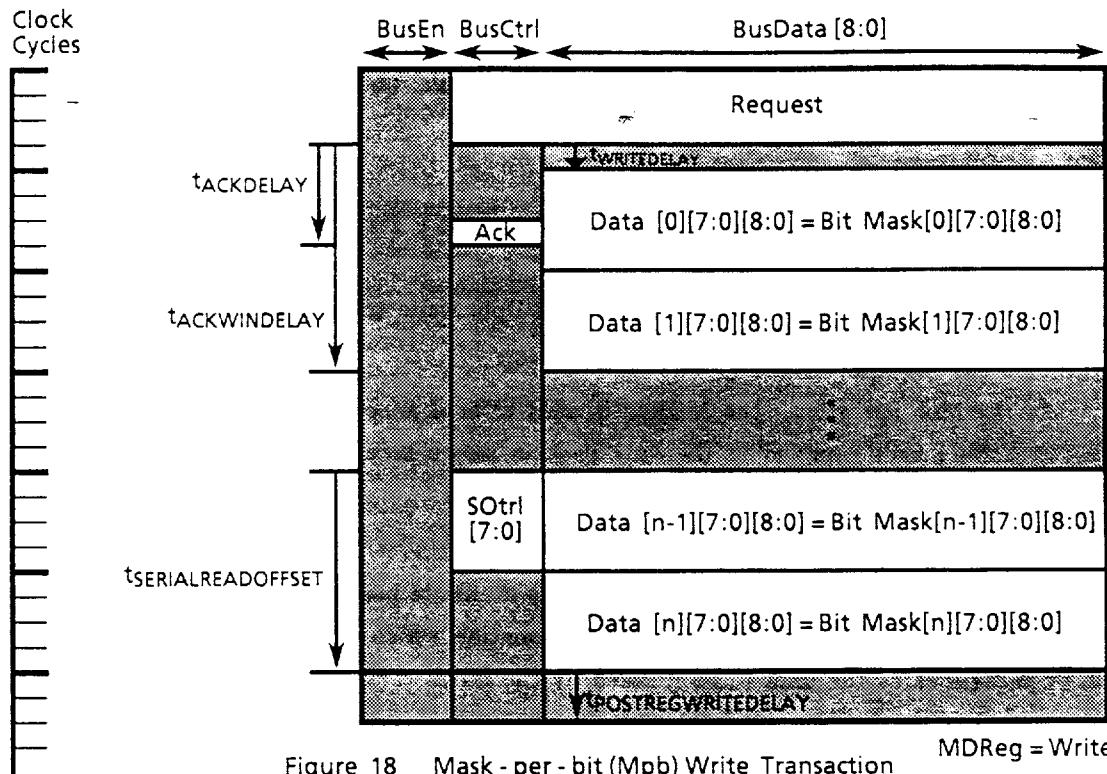


Figure 18 Mask - per - bit (Mpb) Write Transaction MDReg = Write Data

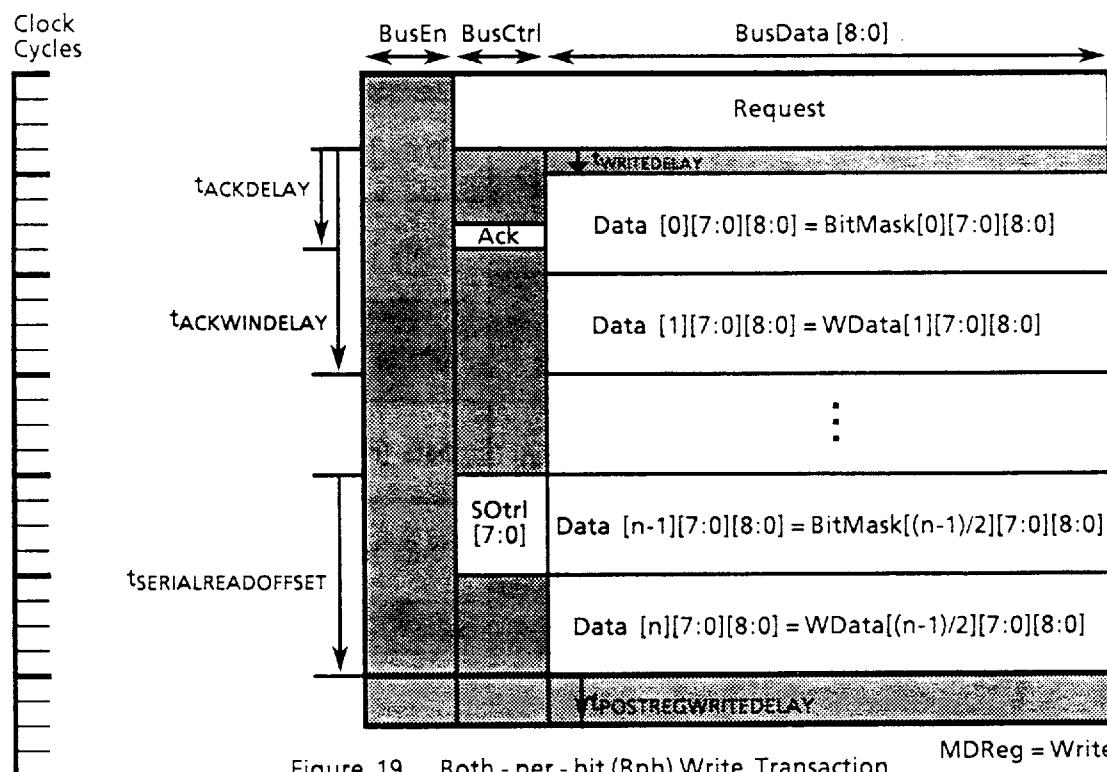


Figure 19 Both - per - bit (Bpb) Write Transaction MDReg = Write Data

## [9] Byte masking

TC59R1809VK / HK supports non-sequential byte masked writes that may include Dpb or Mpib bit masking as an option. Bpb bit masking is not supported in conjunction with byte masking.

In this function, the first data packet, and every ninth thereafter, contain byte masking information that is applied to the eight data packets that follow. This means data packet 0, 9, 18, 27, etc. are not written to memory, but are instead used as byte masks for the eight octbytes of data that follow.

Figure 20 and 21 shows the format of the non-sequential data write transaction with byte masking(Npb / Dpb) and (Mpib).

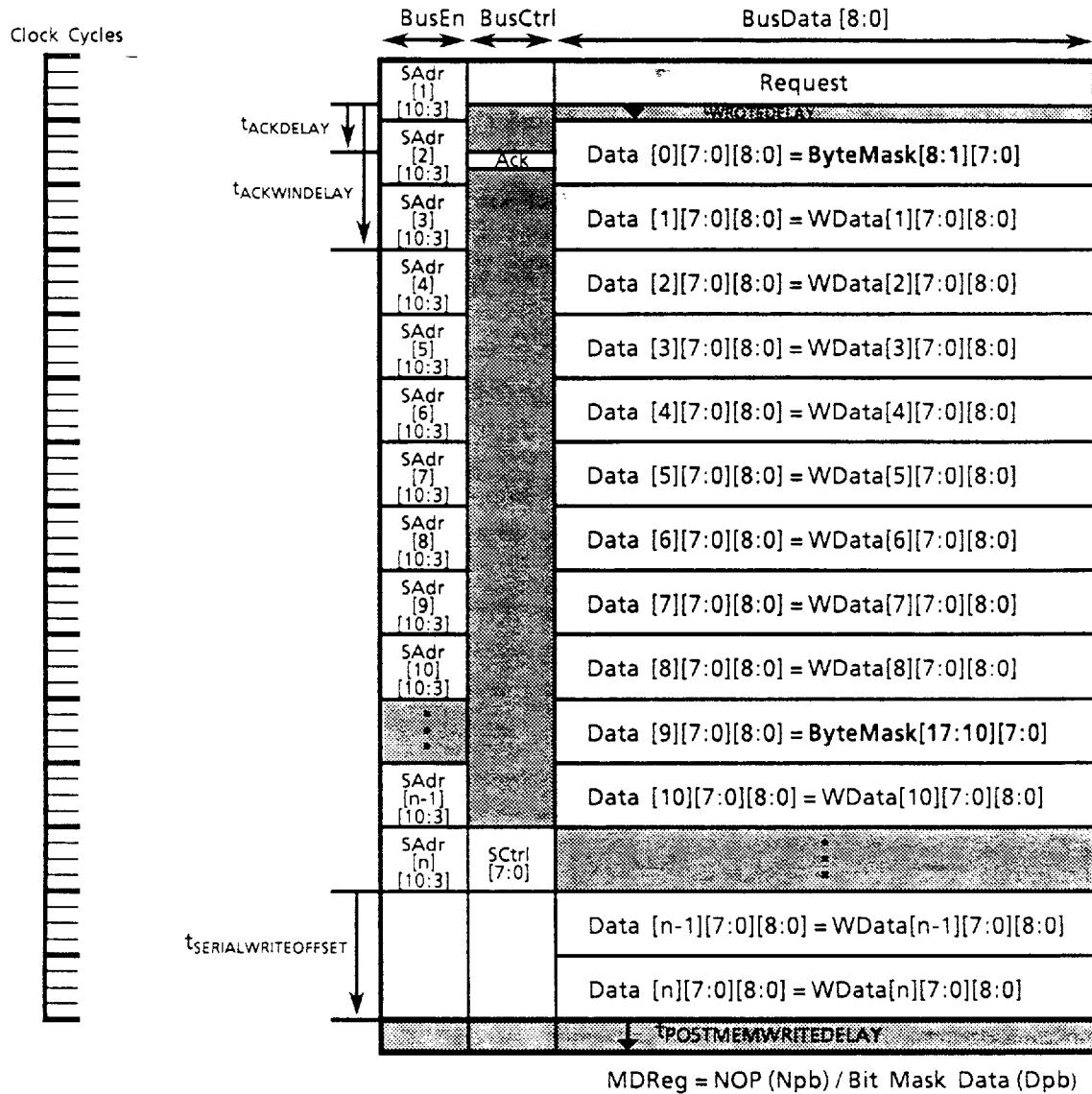


Figure 20 Non-sequential data write transaction with Byte Masking(Npb/Dpb)

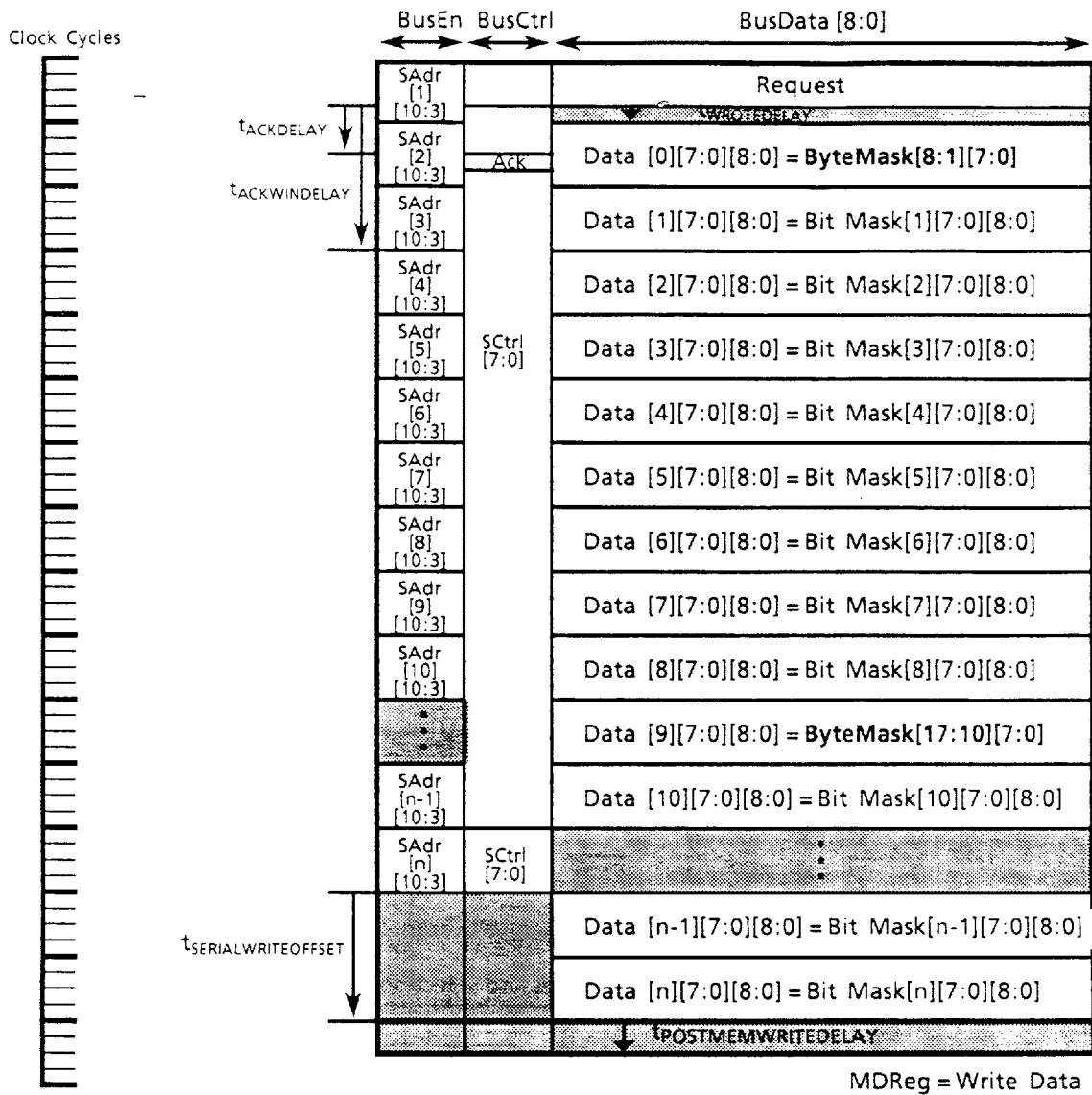


Figure 20 Non-sequential data write transaction with Byte Masking(Mpb)

## [11] Operation of Registers in Slave Logic

As shown in Figure 22, all registers have a standard group of 4, with register name [byte] [bit] format. Bytes are specified in the range [3 : 0], bits are specified in the range [8 : 0]. The bit weight within the bit field is indicated by arrows from the least significant bit (LSB) to the most significant bit (MSB). The master outputs "0" for the "reserved" bit in Figure 22 during write operations, while undefined data is output during read operations.

"0", "1" : Reset value

"x" : Not changed at reset (or bit is retained)

"r" : Read-only. Always the same value

Each register is selected, as shown in Table 9, according to the value of Adr [9 : 2] in the request packet.

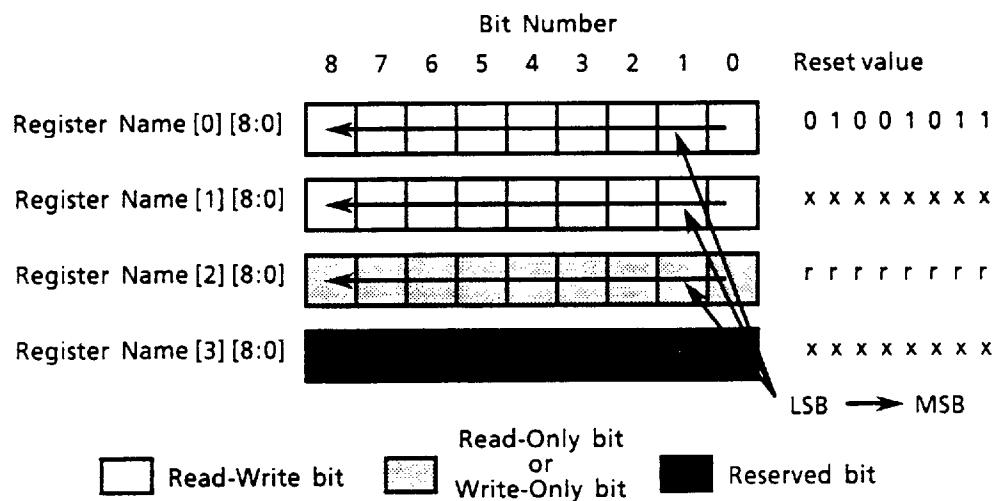


Figure 22 Register Format

Table 7 Register Types and Selection Addresses

Register Name	Adr [9 : 2]	Comment
DeviceType [3 : 0] [8 : 0]	0 0 0 0 0 0 0 0	Device type register
DeviceID [3 : 0] [8 : 0]	0 0 0 0 0 0 0 1	Device ID register
Delay [3 : 0] [8 : 0]	0 0 0 0 0 0 1 0	Delay register
Mode [3 : 0] [8 : 0]	0 0 0 0 0 0 1 1	Mode register
RefInterval [3 : 0] [8 : 0]	0 0 0 0 0 1 0 0	Refresh interval register
RefRow [3 : 0] [8 : 0]	0 0 0 0 0 1 0 1	Refresh row register
RasInterval [3 : 0] [8 : 0]	0 0 0 0 0 1 1 0	RAS interval register
MinInterval [3 : 0] [8 : 0]	0 0 0 0 0 1 1 1	Minimum interval register
AddressSelect [3 : 0] [8 : 0]	0 0 0 0 1 0 0 0	Address select register
DeviceManufacture [3 : 0] [8 : 0]	0 0 0 0 1 0 0 1	Manufacturer setting register
Row [3 : 0] [8 : 0]	1 0 0 0 0 0 0 0	Row register

## (1) DeviceType register (all Read-Only bits)

- Version ... DeviceType [3] [7 : 4]  
These bits show the RDRAM version.
- Type ... DeviceType [3] [3 : 0]  
These bits show the device type. "0000" shows that the device is RDRAM.
- BankBits ... DeviceType [1] [7 : 4]  
These bits show the number of bank addresses in RDRAM memory cells. Because the TC59R1809VK/HK has two banks, these bits are set to "0001" (1 bit).
- RowBits ... DeviceType [1] [3 : 0]  
These bits show the number of row address bits (number of rows) per RDRAM memory cell bank. Because the TC59R1809VK/HK has 512 rows per bank, these bits are set to "1001" (9 bits).
- ColumnBits ... DeviceType [1] [7 : 4]  
These bits specify the number of column address bits (including Adr[1:0]) in RDRAM memory cells. Because the TC59R1809VK/HK has 2048 columns per row, these bits are set to "1011" (11 bits). When accessing memory, you cannot exceed the last column address in the currently accessed row.
- Par... DeviceType [0] [2]  
Indicates whether the RDRAM has a×9 structure. "1" indicates a×9 structure; "0" indicates ×8 structure.

	Bit Number									
	8	7	6	5	4	3	2	1	0	Reset value
DeviceType [0] [8:0]				Column Bit			Par			- 1 0 1 1 - 1 - -
DeviceType [1] [8:0]				Bank Bit		Row Bit				- 0 0 0 1 1 0 0 1
DeviceType [2] [8:0]										- - - - - - - - - -
DeviceType [3] [8:0]				Version		Type				- 0 0 0 0 0 0 0 0 0

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## (2) Device ID Register (All Read-Write bits)

## • Device ID

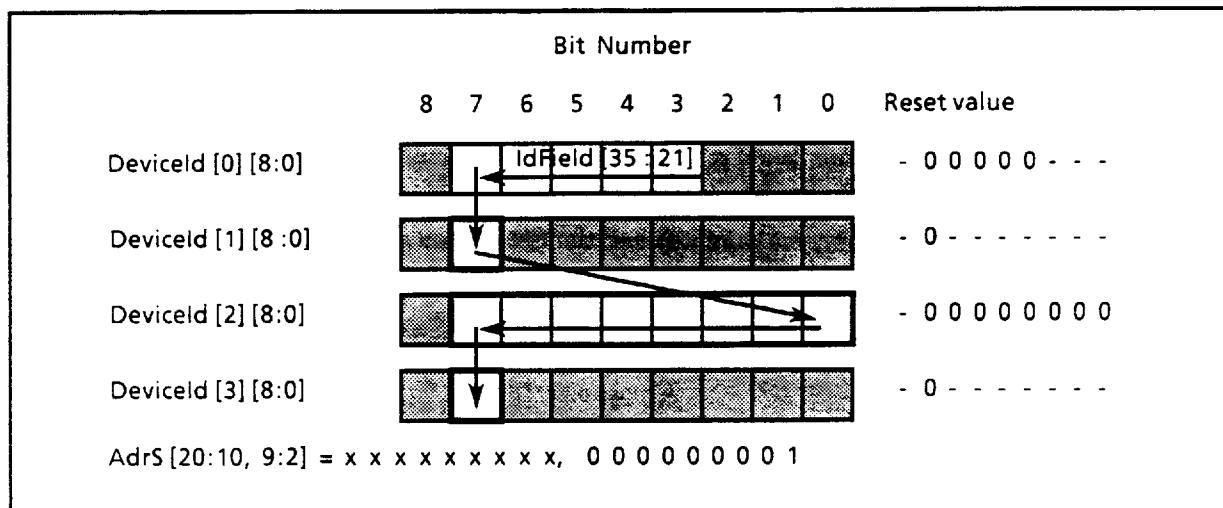
At initialization, the master sets a unique 17-bit DeviceID for each device. The DeviceID register is used for this purpose. The DeviceID data is used, as shown below, for comparison with the request packet address Adr [35 : 21] (swapped address). If they match, the IDMatch signal is issued. IDMatch is not generated by the broadcast register write instructions (Write RegB).

IdField [25 : 21] ... DeviceId [0] [7 : 1]

IdField [26] ... DeviceId [1] [7]

IdField [34 : 27] ... DeviceId [2] [7 : 0]

IdField [35] ... DeviceId [3] [7]

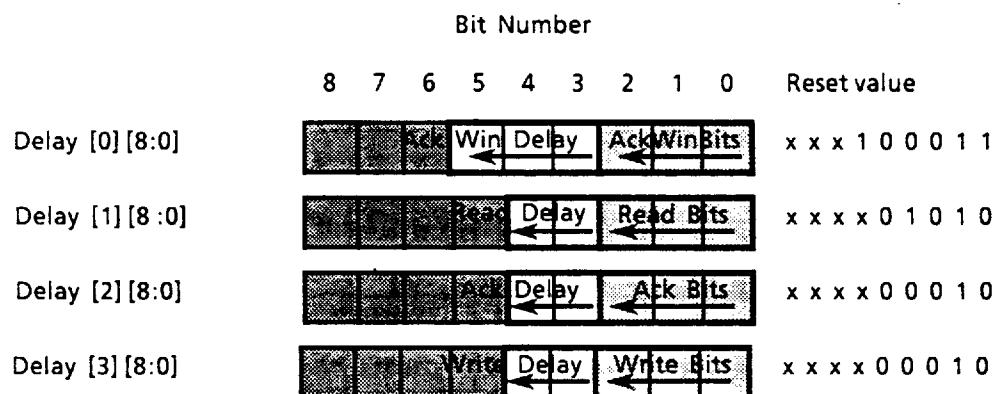


(3) Delay Register

The Delay register is used to select the values of the AckWin, Read, Ack, and Write delays, and to specify the number of bits (Read-Only bits). (See Table 10.)

Table 10 Delay Register Settings

	Register Used	Bits	Description
AckWinBits	Delay [0] [2 : 0]	3	Specifies the number of bits in AckWinDelay
ReadBits	Delay [1] [2 : 0]	2	Specifies the number of bits in ReadDelay
AckBits	Delay [2] [2 : 0]	2	Specifies the number of bits in AckDelay
WriteBits	Delay [3] [2 : 0]	2	Specifies the number of bits in WriteDelay
AckWinDelay	Delay [0] [5 : 3]	3	Stipulates the delay of AckWindow from the end of a request packet. (See Table 9.)
ReadDelay	Delay [1] [7 : 3]	5	Stipulates the delay between the end of a request packet and the start of a read data packet. (See Table 10.)
AckDelay	Delay [2] [4 : 3]	2	Stipulates the delay between the end of a request packet and the start of an Ack packet. (See Table 11.)
WriteDelay	Delay [3] [7 : 3]	5	Stipulates the delay between the end of a request packet and the start of a write data packet. (See Table 12.)



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Table 9. AckWinDelay

Delay [0] [5 : 3]	AckWinDelay	Delay [0] [5 : 3]	AckWinDelay
101	5 tCYCLE	001	9 tCYCLE
110	6 tCYCLE	010	10 tCYCLE
111	7 tCYCLE	011	11 tCYCLE
000	8 tCYCLE	100	12 tCYCLE

Table 10. ReadDelay

Delay [1] [7 : 3]	ReadDelay	Delay [1] [7 : 3]	ReadDelay	Delay [1] [7 : 3]	ReadDelay	Delay [1] [7 : 3]	ReadDelay
00111	7 tCYCLE	01111	15 tCYCLE	10111	23 tCYCLE	11111	31 tCYCLE
01000	8 tCYCLE	10000	16 tCYCLE	11000	24 tCYCLE	00000	32 tCYCLE
01001	9 tCYCLE	10001	17 tCYCLE	11001	25 tCYCLE	00001	33 tCYCLE
01010	10 tCYCLE	10010	18 tCYCLE	11010	26 tCYCLE	00010	34 tCYCLE
01011	11 tCYCLE	10011	19 tCYCLE	11011	27 tCYCLE	00011	35 tCYCLE
01100	12 tCYCLE	10100	20 tCYCLE	11100	28 tCYCLE	00100	36 tCYCLE
01101	13 tCYCLE	10101	21 tCYCLE	11101	29 tCYCLE	00101	37 tCYCLE
01110	14 tCYCLE	10110	22 tCYCLE	11100	30 tCYCLE	00110	38 tCYCLE

Table 11. AckDelay

Delay [2] [5 : 3]	AckDelay	Delay [2] [5 : 3]	AckDelay
00	4 tCYCLE	10	6 tCYCLE
01	5 tCYCLE	11	7 tCYCLE

Table 12. WriteDelay

Delay [3] [7 : 3]	WriteDelay	Delay [3] [7 : 3]	WriteDelay	Delay [3] [7 : 3]	WriteDelay	Delay [3] [7 : 3]	WriteDelay
00001	1 tCYCLE	01001	9 tCYCLE	10001	17 tCYCLE	11001	25 tCYCLE
00010	2 tCYCLE	01010	10 tCYCLE	10010	18 tCYCLE	11010	26 tCYCLE
00011	3 tCYCLE	01011	11 tCYCLE	10011	19 tCYCLE	11011	27 tCYCLE
00101	4 tCYCLE	01100	12 tCYCLE	10100	20 tCYCLE	11100	28 tCYCLE
00110	5 tCYCLE	01101	13 tCYCLE	10101	21 tCYCLE	11101	29 tCYCLE
00110	6 tCYCLE	01110	14 tCYCLE	10100	22 tCYCLE	11110	30 tCYCLE
00111	7 tCYCLE	01111	15 tCYCLE	10111	23 tCYCLE	11111	31 tCYCLE
01000	8 tCYCLE	10000	16 tCYCLE	11000	24 tCYCLE	00000	32 tCYCLE

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## (4) Mode Register

- CE ... Mode [0][7] (1 bit)

This bit selects automatic thermal compensation for the output driver drive current. When set to "1", fluctuations in the output current level due to temperature change are automatically corrected. This bit is inverted when read.

- X2 ... Mode [0][6] (1 bit)

This bit selects whether register X1 or X2 is used for the current control counter. "0" selects register X1; "1" selects register X2.

- C [5 : 0] ... Mode [3 : 1][7 : 6] ( $3 \times 2 = 6$  bits)

This bit field sets the device output current drive level in the range 0 to 63. The RDRAM output driver uses the open-drain system and consists of six transistors with different current drive capacities. C [5 : 0] specifies the combination in which these six drivers are used. Each bit sets a transistor ON when set to "0" or OFF when set to "1".

- DE ... Mode [0][1] (1 bit)

This DeviceEnable bit is related to initialization of the device. When DE = "0", operations other than broadcast register write cannot be executed. Also, when DE = "0", SOut is not output. See the section on initialization for more details.

- PD ... Mode [0][2] (1 bit)

This bit sets the RDRAM operation mode to PowerDown. Setting this bit to "1" selects PowerDown mode, enabling considerable energy savings.

- RE ... Mode [0][0] (1 bit)

This bit selects refresh. Setting this bit to "1" selects the self-refresh function.

- AS ... Mode [0][2] (1 bit)

This bit is used for testing.

- SK ... Mode [0][3] (1 bit)

This bit is used for testing.

- SV ... Mode [0][4] (1 bit) (Read only bit)

This bit is used for testing.

- PL ... Mode [0][5] (1 bit) (Read only bit)

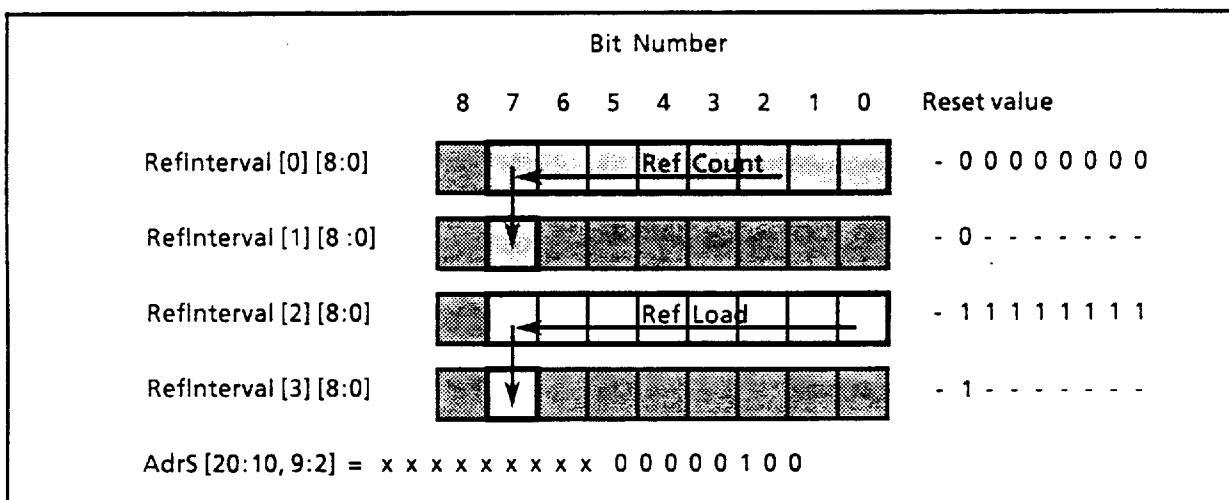
This bit is used to select the powerdown wake up latency.

	Bit Number									Reset value
	8	7	6	5	4	3	2	1	0	
Mode [0][8:0]	[ ]	CE	X2	PL	SV	SK	AS	DE	RE	- 1 1 0 0 0 1 0 0
Mode [1][8:0]	[ ]	C5	C2	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	- 1 1 - - - - -
Mode [2][8:0]	[ ]	C4	C1	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	- 1 1 - - - - -
Mode [3][8:0]	[ ]	C3	C0	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	- 1 1 - - - - -
Adrs [20:10, 9:2] =	x	x	x	x	x	x	x	x	x	0 0 0 0 0 0 1 1

## (5) RefInterval Register

- RefCount...RefInterval [1][7] and RefInterval [0][7:0] (total : 9 bits) (Write only bit)  
This register counts down the division clock for dividing RClk by 256. When RefCount becomes "0", the refresh execution signal (RefZero) is output.
- RefLoad...RefInterval [3][7] and RefInterval [2][7:0] (total : 9 bits) (Read - Write bit)  
This register sets the initial RefCount value. When RefCount becomes "0", the RefLoad value is loaded into RefCount.

The RefInterval register is used to determine the refresh interval for self-refresh. The self-refresh interval is calculated as (RefLoad value\* output clock rate from prescaler). Because RClk is the input clock to the prescaler, a higher RClk frequency means that the refresh interval becomes shorter than necessary. This is related to increased power dissipation and increased bus lockout times. Therefore RefLoad must be set bearing in mind the operating frequency and the device characteristics.



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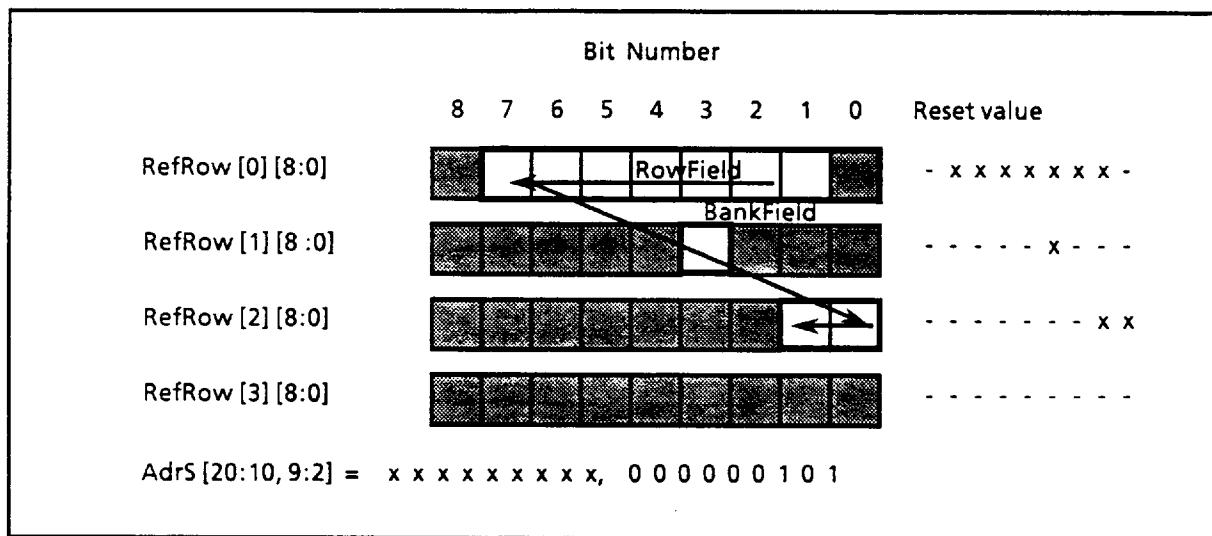
TECHNICAL DATA

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## (6) RefRow Register (Read-Write bit)

The RefRow register is used to store the bank address and row address for refreshing.

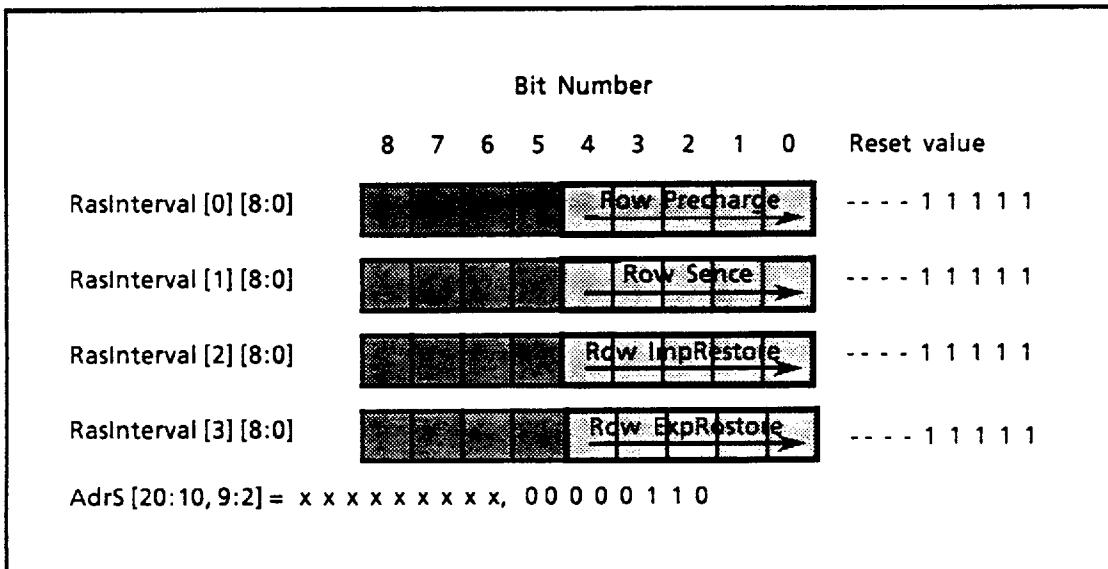
- Row ... RefRow [0] [7 : 1] (9 bits)  
Specifies the currently refreshed row
- Bank ... RefRow [1] [3] (1 bit)  
Specifies the currently refreshed bank



## (7) RasInterval Register (All write only bit)

When RDRAM access is prevented by a row-miss or self-refresh (when the Ack packet is Nack), the master has to wait a set interval until the next access. The RasInterval register determines the length that the master waits. The RasInterval register includes the RowPrecharge, RowAccess, and RowDelay registers. As shown in Figure 16, the total of these registers constitutes the row cycle time.

- RowPrecharge ... RasInterval [0] [0 : 4] (5 bits)  
Specifies the RAS access precharge interval in the range 0 to 31tBCP
- RowAccess ... RasInterval [1] [0 : 4] (5 bits)  
Specifies the RAS access interval in the range 0 to 31tBCP
- RowDelay ... RasInterval [2] [0 : 4] (5 bits)  
Specifies the RAS access delay interval in the range 0 to 31tBCP



(8) MinInterval Register (All Read-Only bits)

This register specifies, in tCYCLE units, the minimum values for the three delays (Ack, Read, and Write Delay) in the Delay register.

Table 15 MinInterval Register

	Register	Bits	Description
MinAckDelay	MinInterval [0 : 3] [5]	4	Stipulates the minimum AckDelay value in tCYCLE units
MinReadDelay	MinInterval [0 : 3] [4]	4	Stipulates the minimum ReadDelay value in tCYCLE units
MinWriteDelay	MinInterval [0 : 3] [3]	4	Stipulates the minimum WriteDelay value in tCYCLE units

	Bit Number									Reset value	
		8	7	6	5	4	3	2	1	0	
MinInterval [0] [8:0]		↑	↑	↑							- 0 0 0 - - - - -
MinInterval [1] [8:0]		↑	↑	↑	↑	↑	↑	↑	↑		- 0 1 0 - - - - -
MinInterval [2] [8:0]		↑	↑	↑	↑	↑	↑	↑	↑		- 1 1 0 - - - - -
MinInterval [3] [8:0]		↑	↑	↑	↑	↑	↑	↑	↑	← SpecFunc	- 1 1 1 0 0 0 0 0
AdrS [20:10, 9:2]	=	x	x	x	x	x	x	x	x		0 0 0 0 0 1 1 1
		(Write Only Field)									

SpecFumc [4:0] is a write-only field which affects control bit which are otherwise not directly accessible.

Table 16. WriteDelay Encoding

SpecFumc [4:0]	Description
00000	NOP
xxxx1	SetRR - RefreshRequest bit
x0x10	ClrRE - Clear the Refresh Enable bit of the Mode register.
x01xx	SetPD - Set the PD bit
x1x0x	SetRE - Set the Refresh Enable bit of the Mode register.
1xxxx	Rsv

## (9) AddressSelect Register (Read-Write bit)

- SwapField ... AddressSelect [0][7:0] (9 bits) and [1][1:0]

For address mapping, RDRAM allows Adr [28 : 20], and [19 : 11] to be swapped in 1-bit units.

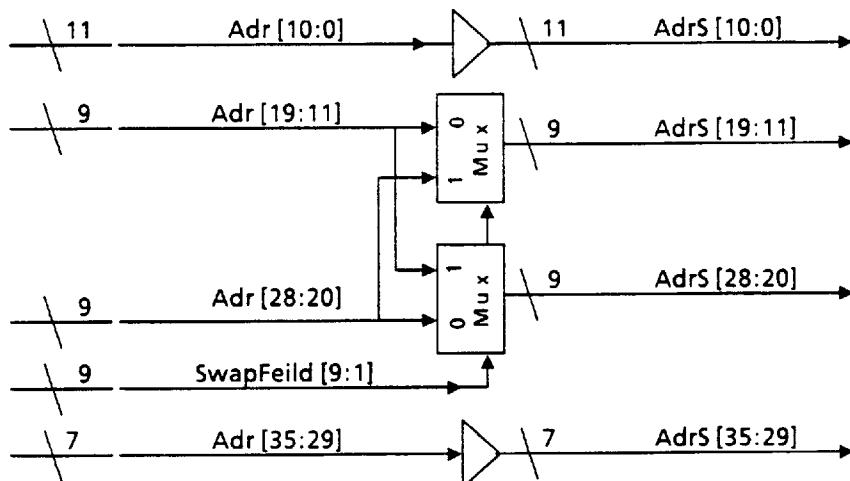
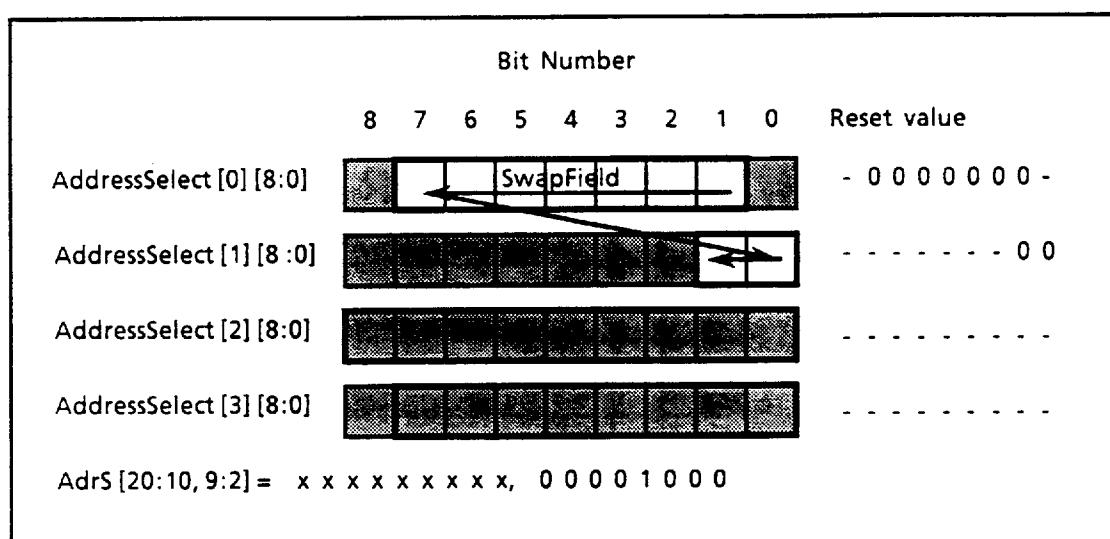
Address swapping is executed as follows when each bit in the AddressSelect register is "1"

Adr [19 : 11] → AdrS [28 : 20], and Adr [28 : 20] → AdrS [19 : 11]

When all bits in the AddressSelect register are "0", no swapping is executed.

Adr [19 : 11] → AdrS [19 : 11], Adr [28 : 20] → AdrS [28 : 20]

Address mapping thereby enables greater hit rates for the row sense amp caches of each bank. See the section on address mapping for details.



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(10) Device Manufacture Register (all Read-Only bits)

This register stipulates manufacturing specifications such as the manufacturer and revision No.

- Manufacture : This field specifies the device manufacturer.
- Manufacture Code : Manufacturer's code

	Bit Number									
	8	7	6	5	4	3	2	1	0	Reset value
Device Manufacture [0] [8:0]										x mmmmmmmm
Device Manufacture [1] [8:0]										x mmmmmmmm
Device Manufacture [2] [8:0]										x rrrrrrrrrr
Device Manufacture [3] [8:0]										x rrrrrrrrrr
AdrS [20:10, 9:2] =	x	x	x	x	x	x	x	x	x	0 0 0 0 1 0 0 1

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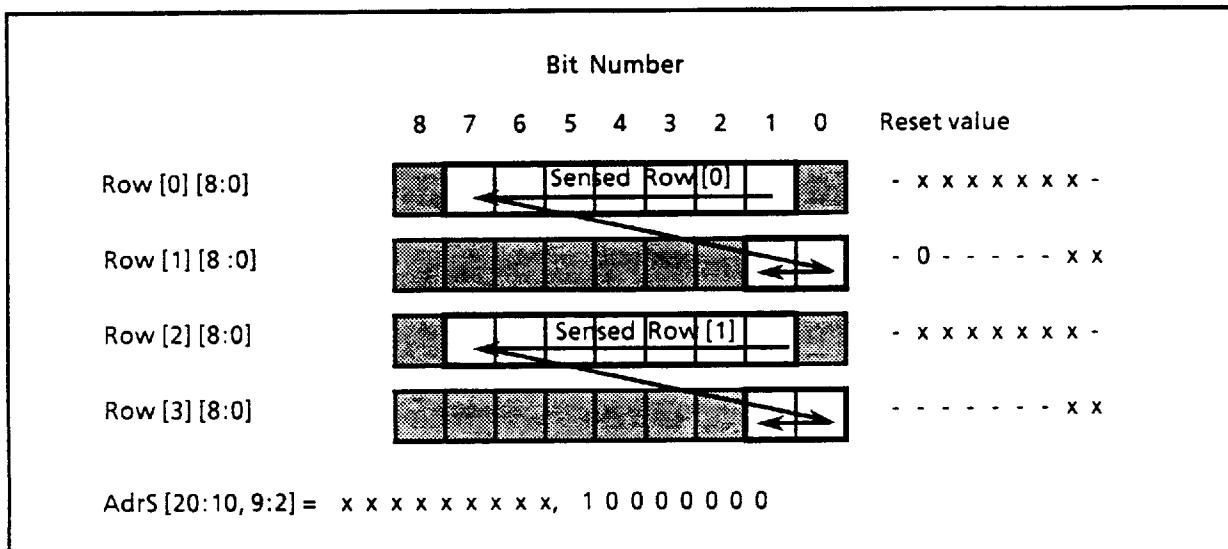
## (11) Row Register (Read-Only bit)

- Sensed Row [0] ... Row [0][7:1] (9 bits) and [1][1:0]

These bits show the address of the previously accessed row in bank "0". That is, they show the address of the row's sense amp cache. When bank "0" ( $\text{AdrS}[20]=0$ ) is accessed, the content of this register is compared against that of  $\text{AdrS}[19:11]$ . If they match, the requested column address ( $\text{Adr}[10:3]$ ) is accessed. If they do not match, (row miss), the cell array is refreshed by the RDRAM's internal control logic, and the requested row then accessed.

- Sensed Row [1] ... Row [2][7:1] and [3][1:0] (9 bits)

This shows the address of the row sense amp cache in Bank "1". This register is used when bank "1" is accessed. Other details are the same as for Sensed Row [0].



## [12] RDRAM Function

## (1) Operation Mode

TC59R1809VK/HK have four operation modes: reset, active, standby, and powerdown. Active mode is the default, permitting a device to frame the packets of a transaction. In reset mode, RDRAM places its control registers into a known state. In standby mode, the RDRAM dissipates less power than in active mode. In this mode, the RDRAM watches the BusEnable pin but does not sample the BusCtrl or BusData [8:0] Pins. Powerdown mode saves more power, shutting down more of the device than in standby mode. This increases the RDRAM latency, because the clock generator is one of the functions which is shut down.

Figure 23 shows the block diagram of the Frame state machine. A serial mode packet SMode [1:0] is received in every clock cycle. The SMode [1:0]=11 combination increments the Count11 [7:0] counter, and clears the Count00 [3:0] counter. If the Count11 [7:0] counter is incremented more than 255 times, it is left at its maximum value of 255. In a clear the Count11 [7:0] counter. If the Count00 [3:0] counter is incremented more than 15 times, it is left at its maximum value of 15.

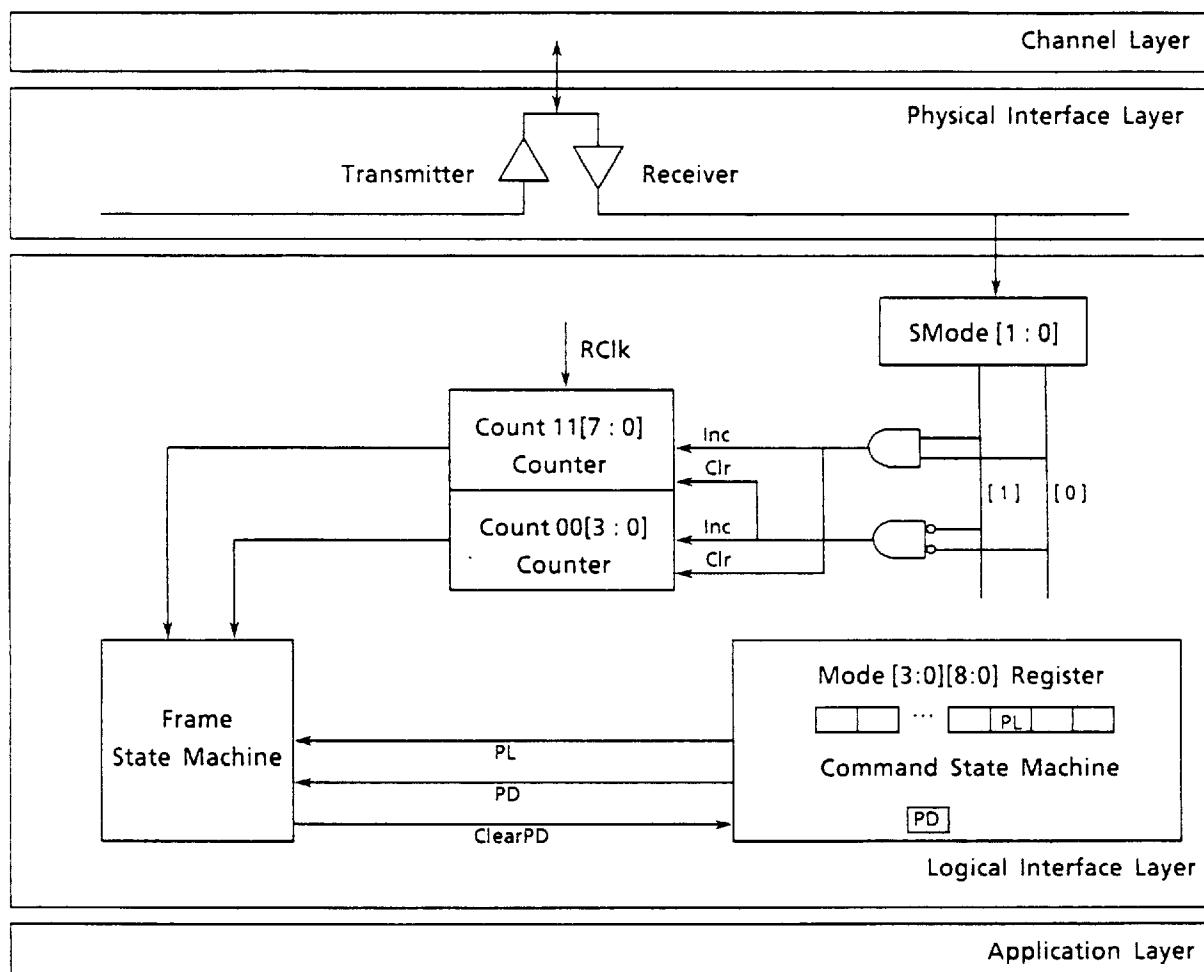
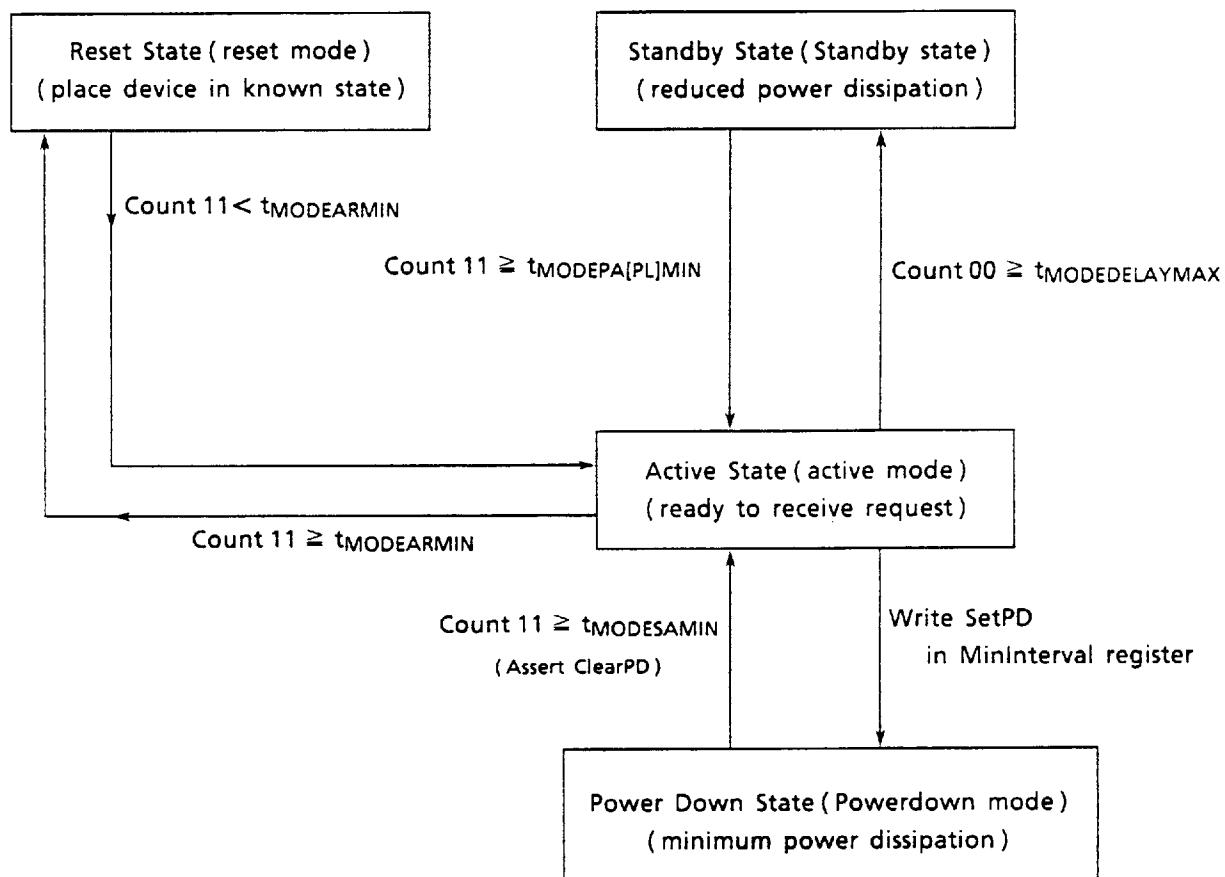


Figure 23 Frame State Machine - Block Diagram

Figure 24 shows the Frame State Machine - State Diagram. The RDRAM will enter reset mode when power is initially applied. In reset state, the RDRAM will be in the reset operating mode, in which all control registers assume a known state. If the power has been applied, the RDRAM will pass through active state and settle in standby state, and remain there until serial mode packets are received from an initiating RDRAM.

After power on, TC59R1809VK/HK will re-enter reset state when the value of the Count11[7:0] counter is greater than or equal to tMODEAR, MIN. This will happen when an SMode[1:0] bit of 00 is received, causing the Count11[7:0] counter to clear.

TC59R1809VK/HK will enter Standby state when the value of the Count00[3:0] counter is greater than or equal to tMODEDELAY, MAX. The device will leave standby state when the value of the Count11[7:0] counter is greater than or equal to tMODESE, MIN.



24 Frame State Machine - State Diagram

TC59R1809VK/HK will enter power down mode when the PD bit is set. The RDRAM will leave power down state when the value of the Count11[7:0] counter is greater than or equal to tMODEDPA[PL], MIN. PL is a bit in the Mode register.

Table 17 show the Responding Device Parameters for Operating Mode Transitions.

Table 17 Responding Device Parameters for Operating Mode Transitions

-	Min (clock cycles)	Max (clock cycles)	Description
tMODESA	1	4	Number of SMode packets to cause a transition from StandbyMode to ActiveMode
Rsrv	5	9	Reserved for future functionality
Undef	10	15	Undefined
tMODEPA [0]	16	20	Number of SMode packets to cause a transition from PowerdownMode[0] to ActiveMode
Rsrv	21	189	Reserved for future functionality
Undef	190	207	Undefined
tMODEPA [1]	208	224	Number of SMode packets to cause a transition from PowerdownMode[1] to ActiveMode
Rsrv	225	253	Reserved for future functionality
Undef	254	271	Undefined
tMODEAR	272	-	Number of SMode packets to cause a transition from ActiveMode to ResetMode
tMODEOFFSET	4		Offset from beginning of SMode packet to request packet for standby to active transition
tMODEDELAY	-	10	Delay from end of SMode packet to request packet for standby to active transition

Figure 25 shows the transitions between active and standby modes. A SMode [1:0] bits are shown as "11" in BusEn column. TC59R1809VK/HK begins the transition to active mode, after the first tMODESA, MIN serial mode packets. It reaches active mode after tOMDEOFFSET, MIN after the start of the first serial mode packet. If the serial mode packet to active mode transition are not followed by tMODEOFFSET, MAX after the last serial mode packet, TC59R1809VK/HK will return to standby mode.

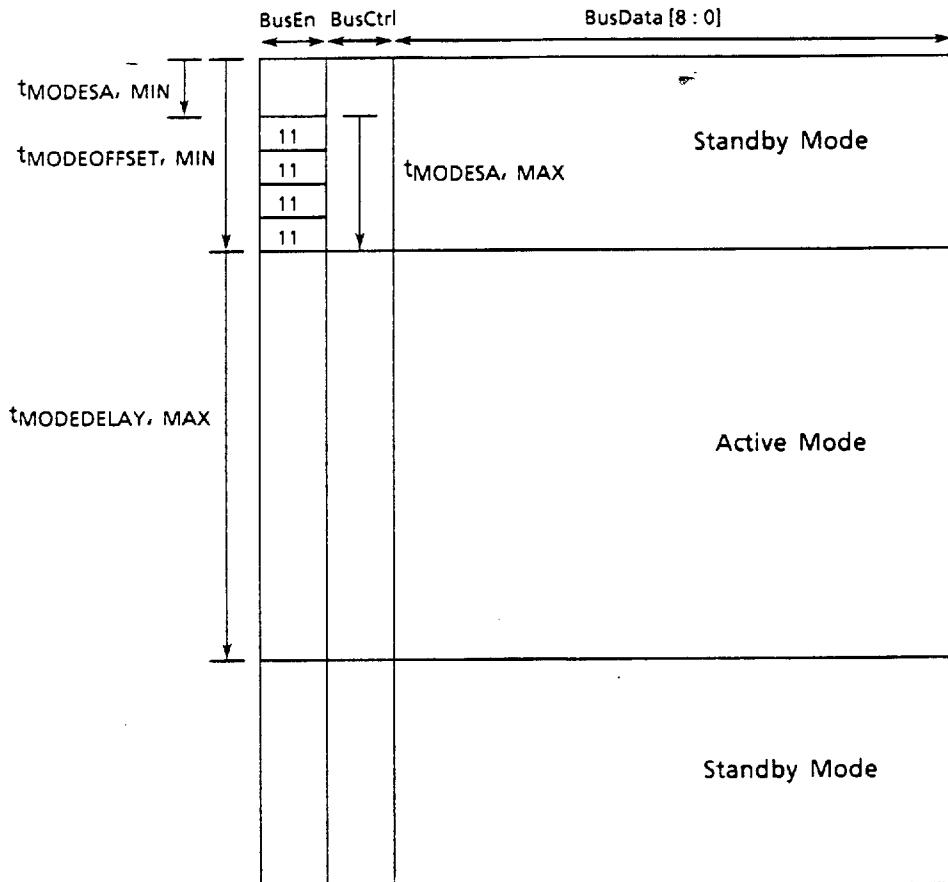


Figure 25. Basic Active Mode / Standby Mode Transitions

When TC59R1809VK/HK is given a consecutive sequence of tMODEAR, MIN serial mode packets with a value of 11, Reset mode is entered. The RDRAM remains in reset mode for as long as serial mode packets with a 11 value are received. When one or more serial mode packets with a value of 00 are seen, TC59R1809VK/HK enters the active mode state.

In order to keep the RDRAMs in active mode during this synchronization, it is necessary to provide a burst of serial mode packets every tMODEDELAY, MAX. If the RDRAM is not kept in active mode during synchronization, the synchronization cycles requires tLOCK, STANDBY, MIN.

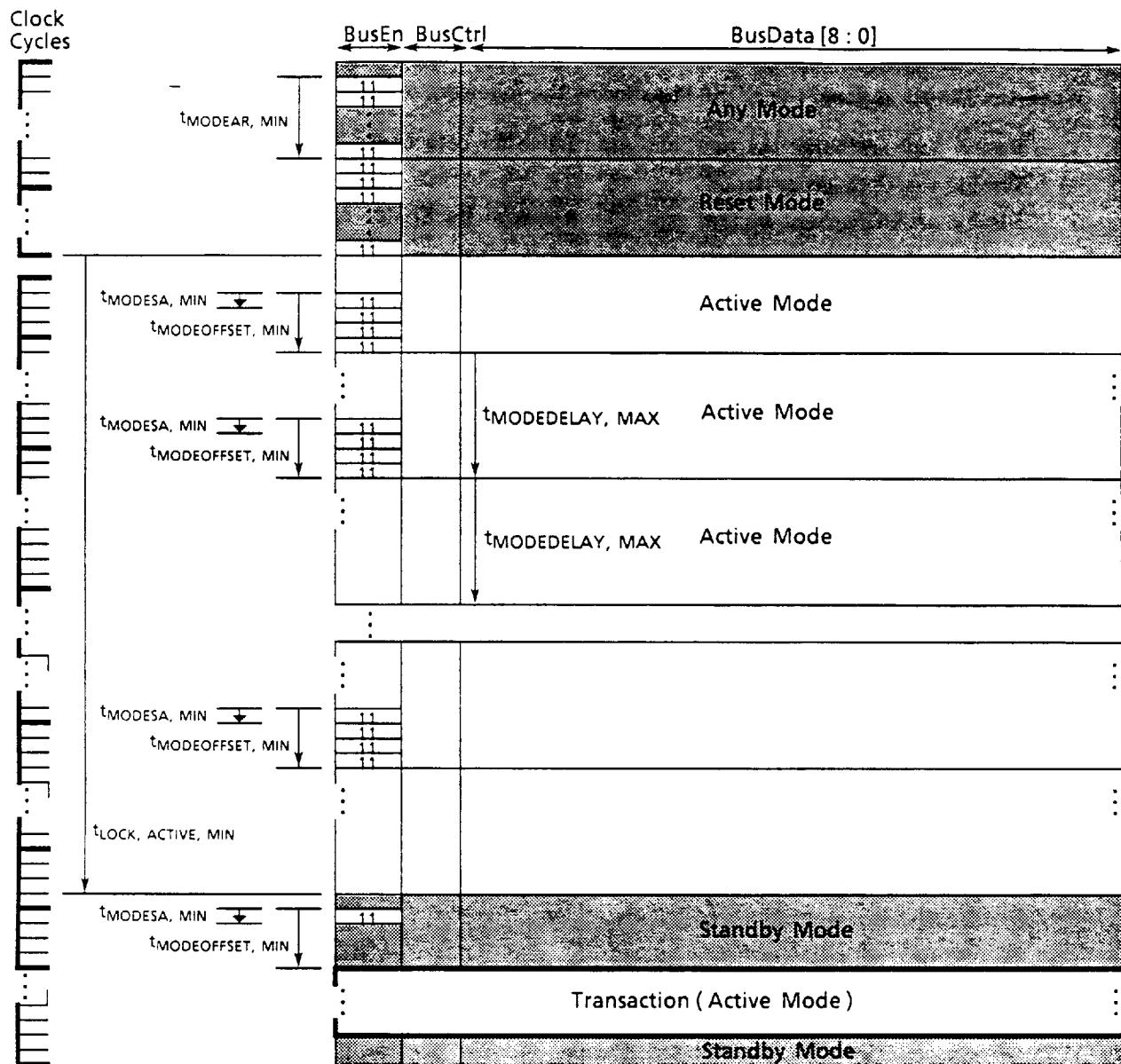


figure 26 Reset Mode Transition

Powerdown mode is controlled by the PD bit. This bit is not directly accessible in the register space. Instead, the "SetPD" is written to the SpecFunc field in the MinInterval register. Figure 27 shows the active mode to power down mode transition.

When the PD bit is done, the RDRAM performs the following operations.

- Restore and precharge the RowSenseAmp Latch for both banks
- Disable the clock generator
- Disable all DC current sources except for a special BusEnable receiver.

When these operations have completed, the RDRAM is in powerdown mode.

Figure 28 shows the power down mode to active mode transition,

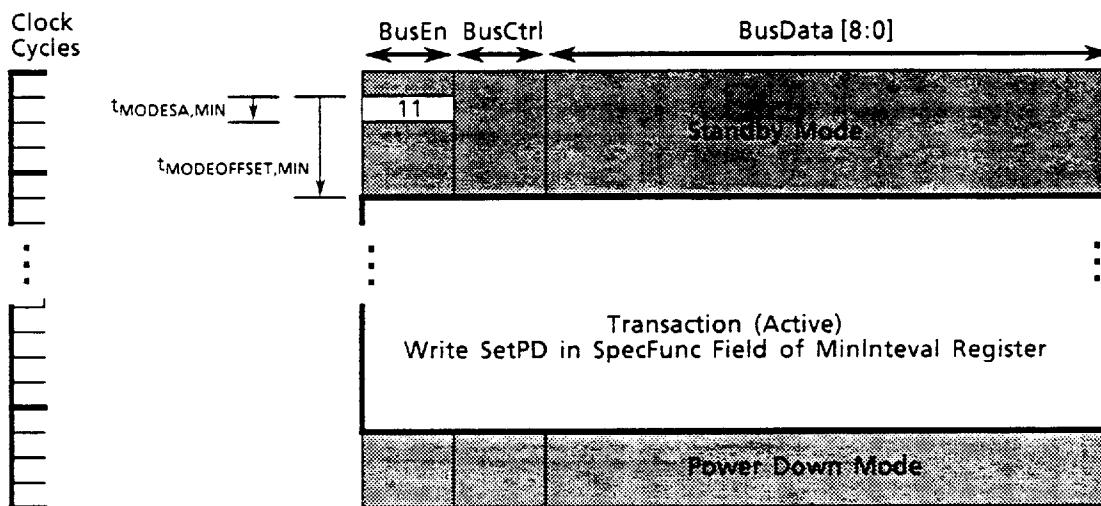


Figure 27 Active MOde to Power Down Mode Transition

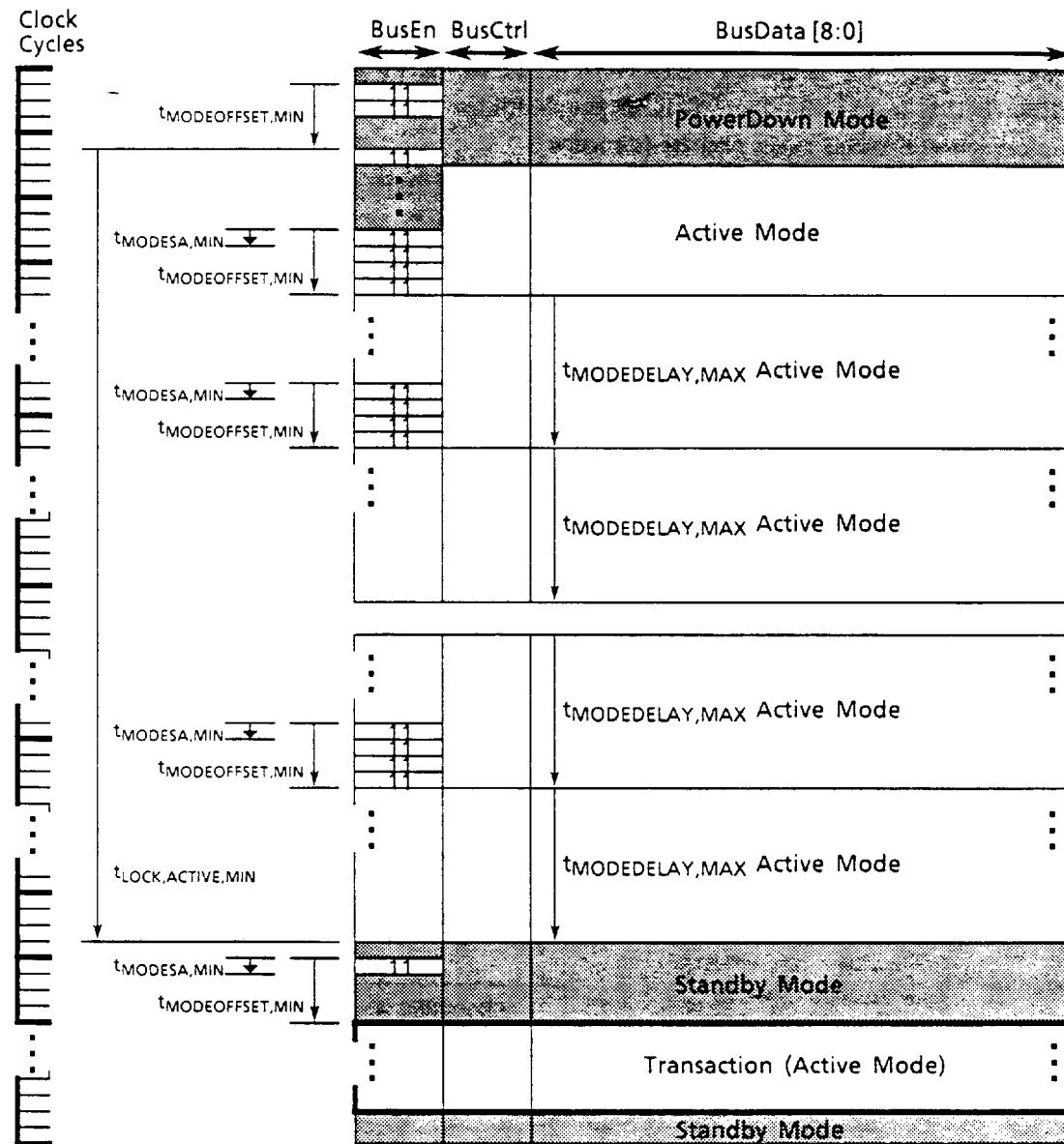


Figure 28 Power Down Mode to Active Mode Transition

## (2) Refresh functions

The RDRAM have three refresh methods which can be used with RDRAM.

There are automatic refresh, manual refresh and power down refresh. There are three ways to accomplish this. RE is the RefreshEnable bit in the Mode Register. PD is a control bit set by writing SetPD in the SpecFunc field of the Mininterval register and cleared when a sufficiently long sequence of serial mode packets is received.

- RE/PD=10 (automatic refresh) The Refresh Counter block periodically invokes the Refresh state machine to perform a burst refresh of four rows.
- RE/PD=00 (manual refresh) An initiating device uses a register write transaction to the (SetRR) to perform a single burst refresh of four rows.
- RE/PD=x1 (powerdown mode) A single row is refreshed with each pulse on the SIn/SOut Pins.

Figure 29 shows the refresh counter logic for the RDRAM. The RE bit resets to a logic zero. When it is set to a logic one, the Prescale [7:0] counter is preset to its maximum value and begins decrementing every clock cycle. Every time the Prescale counter reaches zero, it decrements the RefCount field of the RefInterval register. When the RefCount field reaches zero, it loads the contents of the RefLoad field of the RefInterval register into the RefCount field. When both RefCount and Prescale are zero, they assert RefZero. RefZero sets an SR latch called RR. The RR causes the Refresh state machine to refresh four rows in a burst.

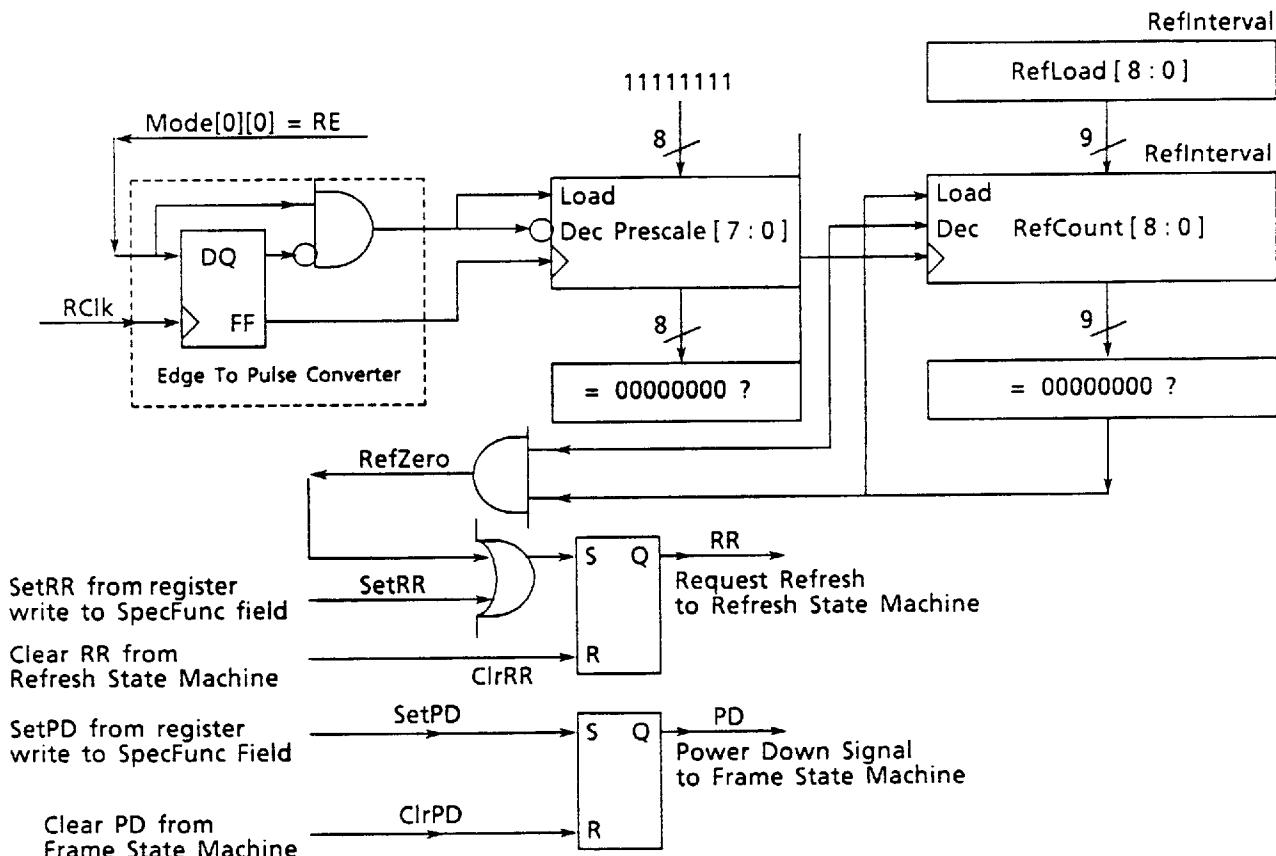


Figure 29 Refresh Counter Logic - Block Diagram

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Manual refresh uses the following sequence to cause the refresh state machine to perform a burst refresh of the next four rows specified by the RefInterval register.

- 1) Perform a register write transaction to the RefInterval register :

RefLoad=11111111

RefCount=00000000

- 2) Perform a register write transaction to the Mode register :

RE=1

- 3) Wait  $((256\text{tcycle}) + t_{RETRYREFRESH}) = (256 + 130)4\text{ns} = 1544\text{ns}$

- 4) Perform a register write transaction to the Mode register :

RE=0

The first step places the maximum value in the MinInterval value in the RefCount field. The second step the RefreshEnable bit of the mode register without changing any of the other fields. This causes the prescale counter to begin counting down. The third step involves waiting for prescale counter to reach zero, and then waiting for the refresh burst to complete. The fourth step clears the RefreshEnable, leaving the RDRAM ready for the next manual burst. This should only be used if compatibility with 4M RDRAMs is an issue.

The preferable manual refresh sequence is the following.

- (1) Perform a register write transaction to the MinInterval register

SpecFunc=SetRR

WinWriteDly, MinReadDly, MinAckDly=0000, 0000, 0000

Since the MinWriteDly, MinReadDly, and MinAckDly fields of the MinInterval register are read-only, it actually doesn't matter what is written to them. The above transaction will set the RR latch. When the Frame state machine returns to ActiveState, a refresh of four rows will be started. At the end of the burst, the RR latch will be cleared. The RE bit of the Mode register will be left at zero throughout this whole process.

The third and last refresh method is used when the RDRAM is in PowerDown operation mode. In this state, DLL is stopped and RxCLK cannot be used as the clock for measuring the refresh timing. Therefore, in PowerDown mode, the refresh clock must be input SIn and SOut. In this case, the input clock input SIn is the same as the RAS waveform for RAS only Refresh for normal DRAM. The internal row address counter is incremented by 1 bit at each trailing edge of SIn. The high SIn output level corresponds to tRP, and the low output level to tRC = tRP, and each cycle is with 31,625us so that all rows can be accessed tREF=32ms.

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## (3) Address Mapping

Address mapping is a function for improving the hit rate for the sense amp cache in the RDRAM memory cells. In concrete terms, address AdrS [35 : 3] for the RDRAM memory space is formed by changing the combination in RDRAM of the request packet address Adr [35 : 3] according to the setting of AddressSelect [0] [7 : 0]. (See Figure 30.) AdrS [35 : 3] refers to the following addresses in the RDRAM memory cells.

$C_M[7:0]$  (AdrS [10 : 3]) : Column address (in QBs)

$R_M[8:0]$  (AdrS [19 : 10]) : Row address

$D_M[15:0]$  (AdrS [35 : 29]) : Device ID address (DeviceID)

Of the Adr[35 : 3], only Adr[28 : 20] and Adr[19 : 11] are swapped by address mapping. Each address is swapped for AdrS [28 : 20] and AdrS [19 : 11] according to the 9-bit data of the AddressSelect register [0] [7 : 0]. In Figure 30, AddressSelect [0] [7 : 1] and [1] [1 : 0] is "11111111", and all Adr [28 : 20] and Adr [19 : 11] bits are therefore swapped.

Address swapping is valuable when the master accesses contiguous address space. That is, when Adr [35 : 3] is accessed from the LSB (Adr [3]) to the MSB (Adr [35]). When the master performs such access without address mapping, we get the following:

Adr [28 : 20] → AdrS [28 : 20]

Adr [19 : 11] → AdrS [19 : 11]

In this case, each time the value of DR [8 : 0] in the request packet changes, the row address RM [8 : 0] also changes, resulting in a cache miss. Even if several RDRAMs are connected to increase the number of cache lines, there will be no improvement in the cache hit rate. In contrast, if address mapping is used, we get:

Adr [28 : 20] → AdrS [19 : 11]

Adr [19 : 11] → AdrS [28 : 20]

In this case, even if the value of request address DR [8 : 0] from the master changes, RM [8 : 0] remains constant and the device ID address DM [8 : 0] changes. This enables cache lines of different devices to be accessed continuously, improving the cache hit rate.

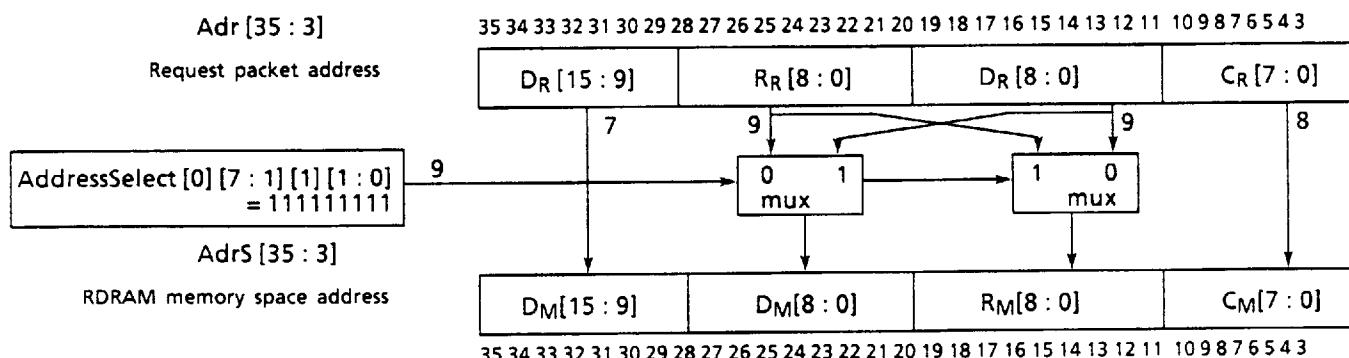


Figure 20 Address Mapping (System with 128 RDRAMs)

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In Figure 30, AddressSelect [0] [7:1][1][1:0] = "1111111". Therefore, we are assuming address mapping in a 256 RDRAM (256 bank) system (currently, address mapping is only available for a maximum of 256 DRAMs). In contrast, Figure 31 shows address mapping for a more realistic RDRAM system. From the top, we have 8, 16, 24, and 32-RDRAM systems. If the number of RDRAMs is expressed as  $2N$ , N bits of the 9 bits of AddressSelect [0] [7:0][1][1:0] are swapped. In a system such as the 24 RDRAM system, in which the number of RDRAMs is expressed as  $P*2Q$  (where P is an odd number), Q bits are swapped, and the system consists of P RDRAM blocks ( $2Q$ ). This is to prevent the creation of blanks in the address space as a result of address mapping. In the 24RDRAM system in Figure 31,  $N=3$  and  $P=3$ , and each block is selected by D [5:4].

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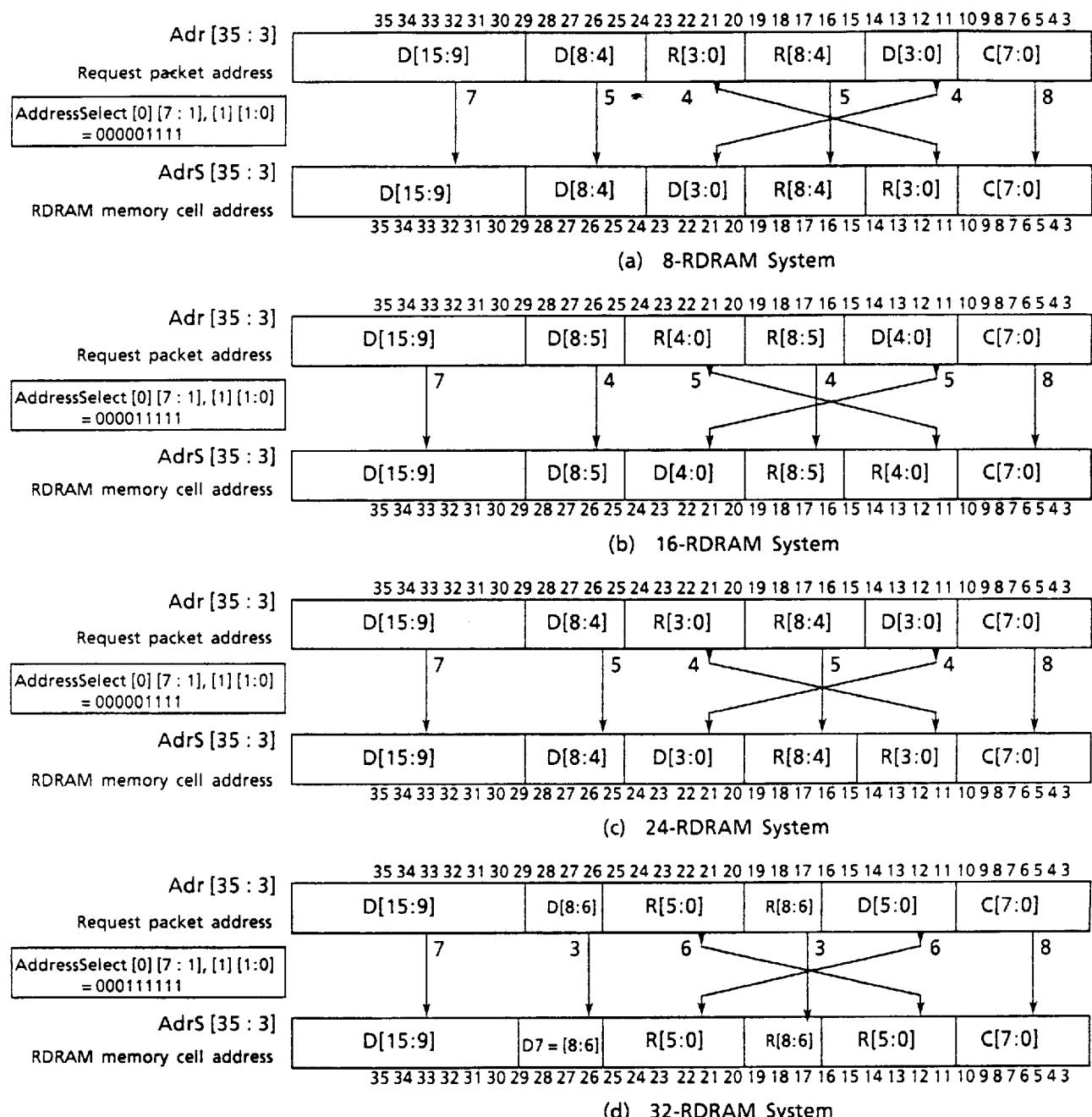


Figure 21 Address Mapping (8, 16, 24, and 32-RDRAM Systems)

As an example, let's take a system consisting of 8 RDRAMs. If we say that each RDRAM's cache line address is  $R[3:0] = "0000"$ , we can use address mapping to contiguously access the 16 cache lines of the 8 RDRAMs, as shown in Figure 32.

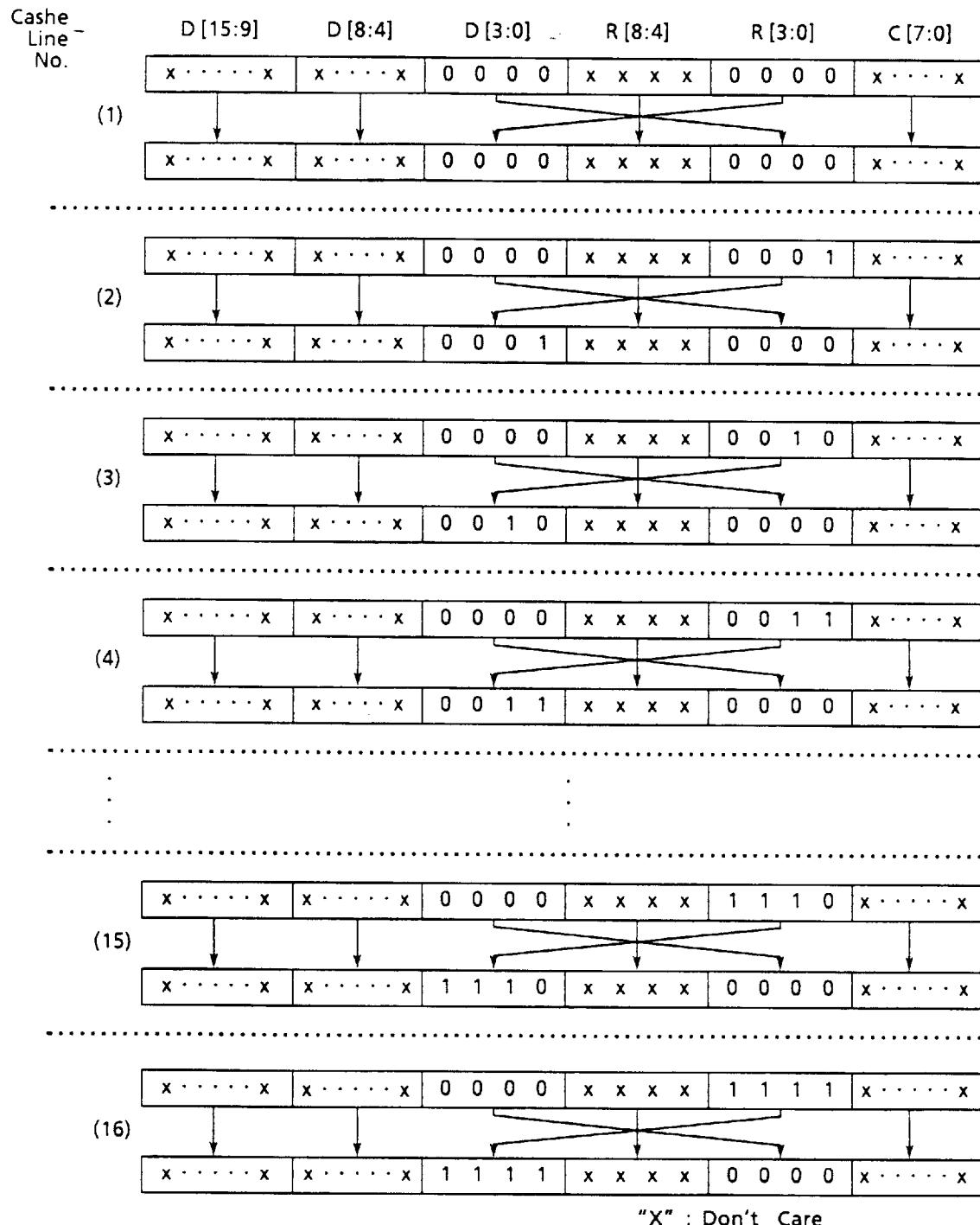


Figure 22 Address Swapping Using Address Mapping (8-RDRAM System)

(4) RDRAM Initialization

RDRAM must be initialized by the master before starting normal operations. The main function of initialization is the allocation of device IDs for each of the device connected to the Rambus system. The Device allows the master to select any device, without the need to use an external control circuit.

Figure 33 shows a Rambus system with a single master, a single primary channel. SOut of the configuration master connects to SIn of the first device and so on through each bus device in daisy chain fashion. SOut of the last device connects to SIn of the configuration master.

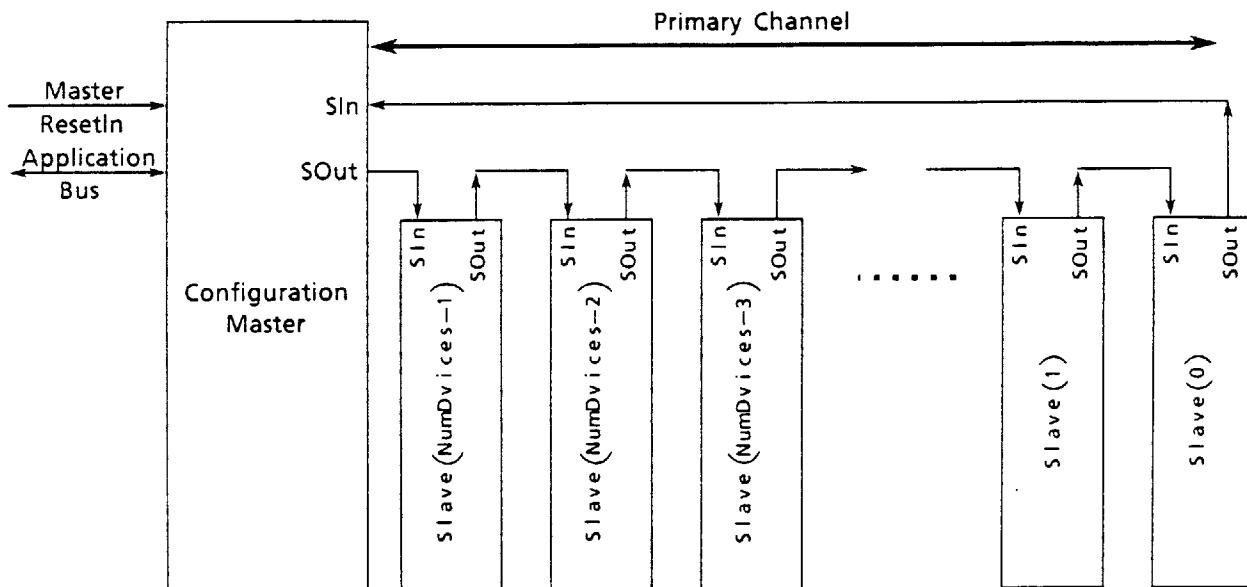


Figure 33 shows a Rambus system with a single configuration wafer device a single Primary channel

Figure 34 shows the RDRAM Slave Device Logic. DeviceEnable is a bit in the Mode register. The reset pulse on the BusEnable pin sets all control registers to default values. Most commands are gated by IdMatch, which is formed by comparing Adr[35:18] in the request packet with the address in the DeviceId register. In addition, DeviceEnable gates the WwwwBbbAaa', RrrrAaa', Wreg', and Rreg' commands. At Initialization time when DeviceEnable=0 most commands are disabled. What remains is the Wreg' path gated by SIn and IdMatch. This path permits the assignment of unique DeviceID values. The broadcast write command, WRegB', which is always enabled.

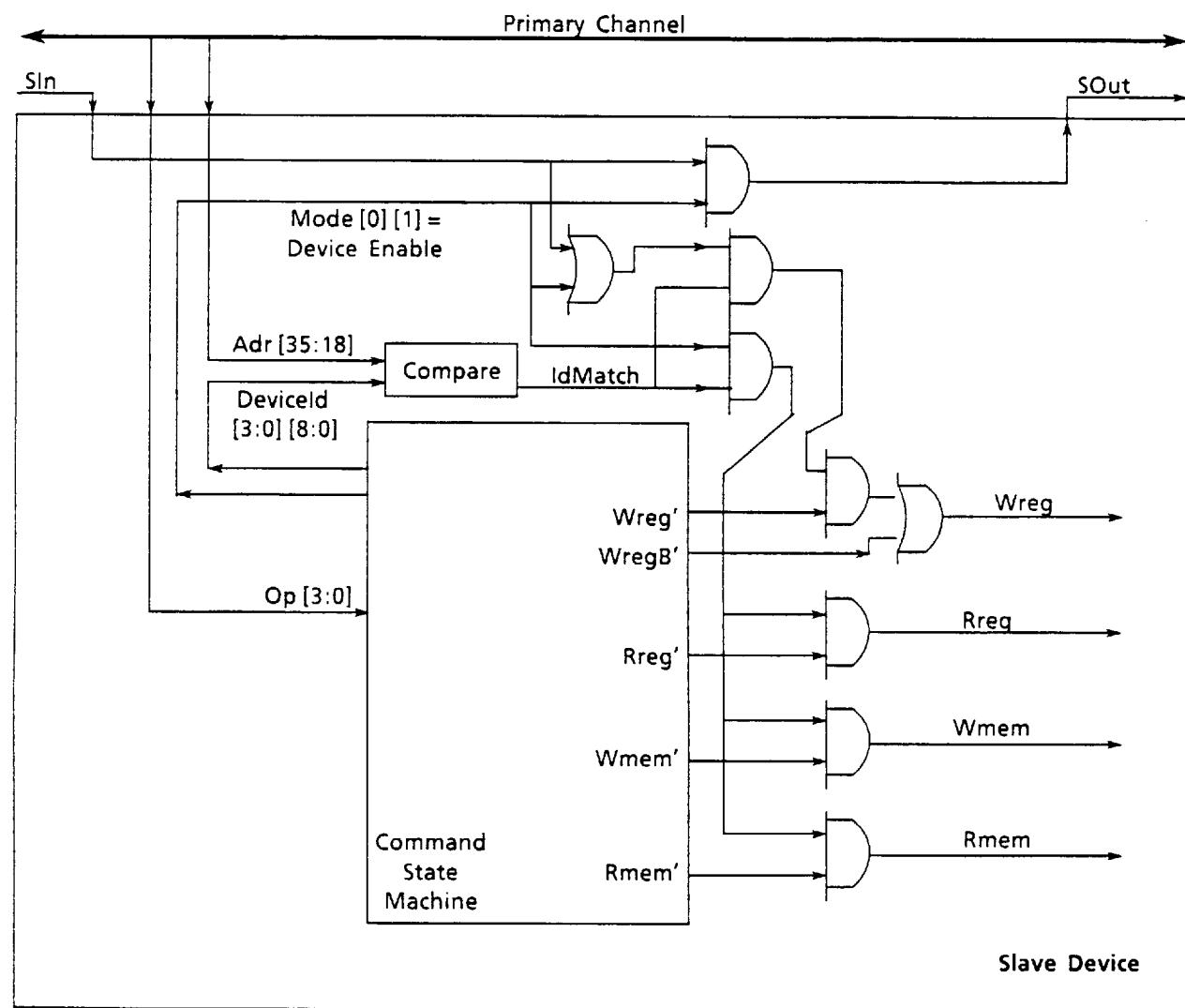


Figure 34 RDRAM スレーブデバイスロジック

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(5) IOL Calibration

The following formula stand for VOL and VLH.

$$\begin{aligned} - \quad V_{OH} &= V_{TERM} - I_{OH} * R_0 \\ V_{OL} &= V_{TERM} - I_{OL} * R_0 \end{aligned}$$

Where  $R_0$  is the resistance of the channel termination register which matches the effective impedance of the channel. The  $V_{OH}$  voltage level is essentially equivalent to the  $V_{TERM}$  voltage because of the small value of the  $I_{OH}$  output current. The  $V_{OL}$  level is a function of  $V_{TERM}$ ,  $I_{OL}$  and  $R_0$ .  $I_{OL}$  and  $R_0$ . The CE bit of the Mode register is set to a one.  $I_{OL}$  is programmable over the range from zero to  $I_{OL, MAX}$  according to the following formula.

$$I_{OL} = (I_{OL, MAX} * f_1 * f_2 * f_3 * f_4) + (\Delta I_{OL, MIN}, \Delta I_{OL, MAX})$$

$$f_1 = (63 - C[5:0]) / 63$$

$$f_2 = (1 + X_2)$$

$$f_3 = t_{CYCLE, MIN} / t_{CYCLE}$$

$$f_4 = V_{REF} / V_{REF, MAX}$$

Where  $C[5:0]$  is an unsigned, 6bit, binary number in the mode register,  $X_2$  is a 1bit field in the Mode register. The  $f_1$  factor is adjusted by placing the appropriate 6 bit value in to the  $C[5:0]$  field. The resulting  $I_{OL}$  will then generate a  $V_{OL}$  that is lower than the  $V_{IL, MAX}$  by the appropriate margin.

The  $f_2$  factor is normally one (the  $X_2$  field is zero). However, if the  $f_3$  and  $f_4$  factors limit the upper programmable limit of  $I_{OL}$ , then  $X_2$  may be set to one.

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**TOSHIBA CORPORATION**

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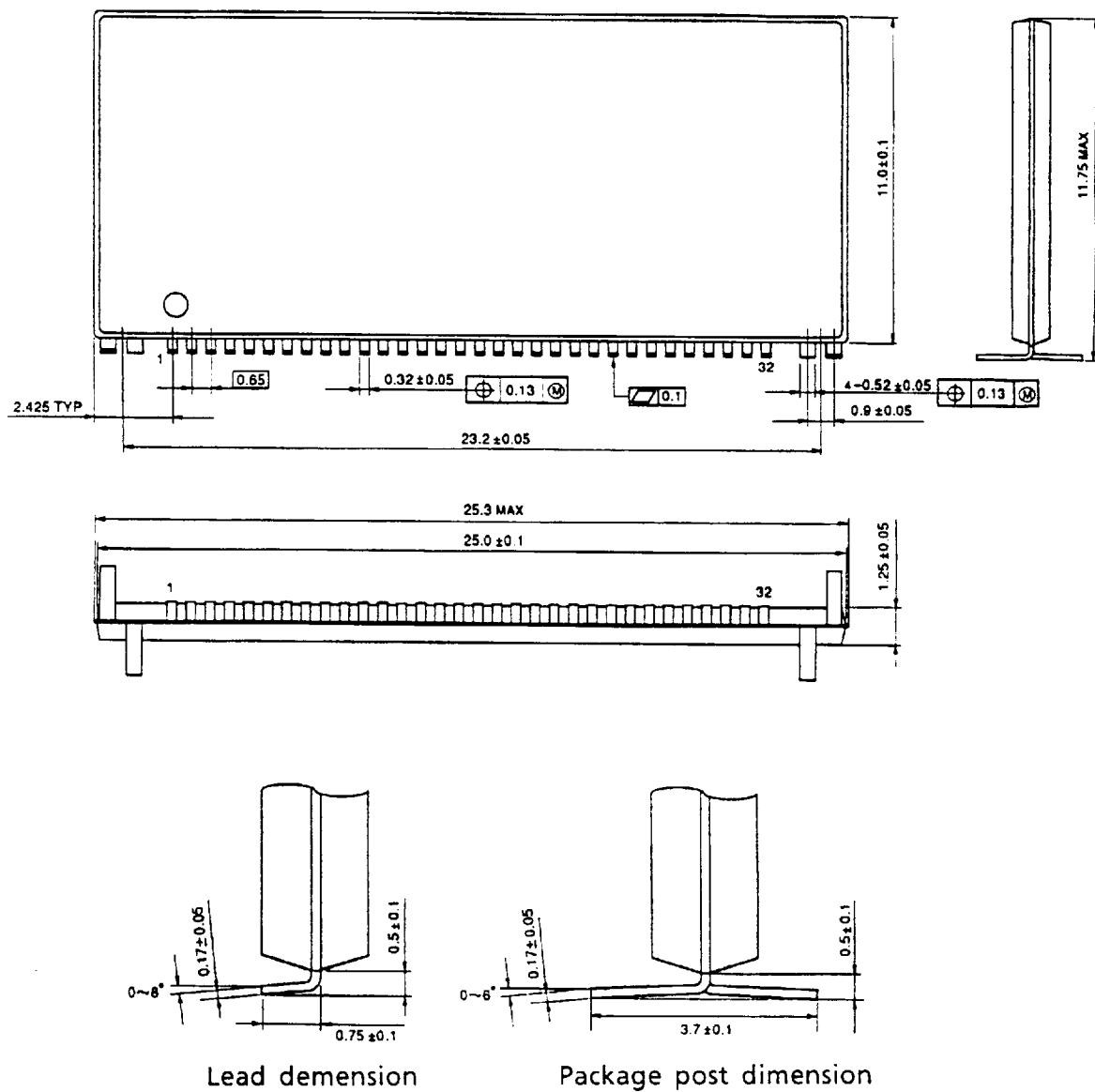
INTEGRATED CIRCUIT

TECHNICAL DATA

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OUTLINE DRAWING (SVP32-P-1125A)

Unit : mm



Weight : 0.75g (TYP.)

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