TC59R0808HK

PRELIMINARY

1,048,576 WORD x 8 BITS RAMBUS DYNAMIC RAM

Description

The TC59R0808HK Rambus Dynamic RAM (DRAM) is a next-generation high-speed CMOS DRAM with a 1,048,576 x 8 bits organization and built-in slave logic. The 16,384 sense amps of the DRAM core are used as cache to achieve data transfer rates of up to 500MB/s. I/O is at the Rambus level, the open drain system being used for output.

The TC59R0808HK use a surface horizontal mount package (SHP). Also, the data transfer, which is synchronized with the high-speed clock, the self-refresh function, random access mode function, byte masking function and the address mapping function obviate the need external control circuits, masking this DRAM ideal for use in main memory and graphics applications where high performance and low cost are essential.

Features

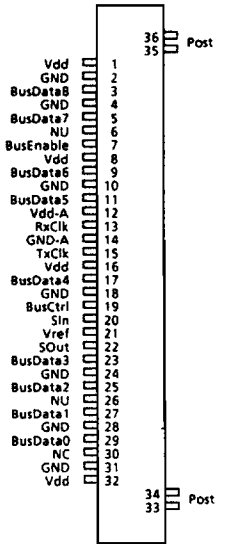
- Organization:
  - RAM: 32K words x 32 bits
  - Cache: 2048 x 8 x 1 (number of sense amps)
  - Slave logic
- Self-Refresh, Address mapping, and mask-write functions. Random Access Mode, Bit Mask, Serial Control Packet
- 1K refresh cycles per/32ms
- Package: SHP
- 3.3V single power supply: 3.3V±0.3V
- I/O: Rambus™ level

Pin Names

Bus Data0~8	Bus Data I/O
BusCtrl	Bus Control I/O
BusEnable	Bus Enable Input
RxClk	High-Speed Sync Clock (for Receiving Data)
TxClk	High-Speed Sync Clock (for Sending Data)
SIn	Serial Signal Input
SOut	Serial Signal Output
Vref	Reference Voltage
Vdd/GND	Power Supply Terminal (+3.3V)/ground
Vdd/GND-A	Power Supply Terminal (+3.3V)/ground (for DLL)
NC	No Connection
NU	Not Usable Input

Pin Connection (Top View)

Plastic SHP



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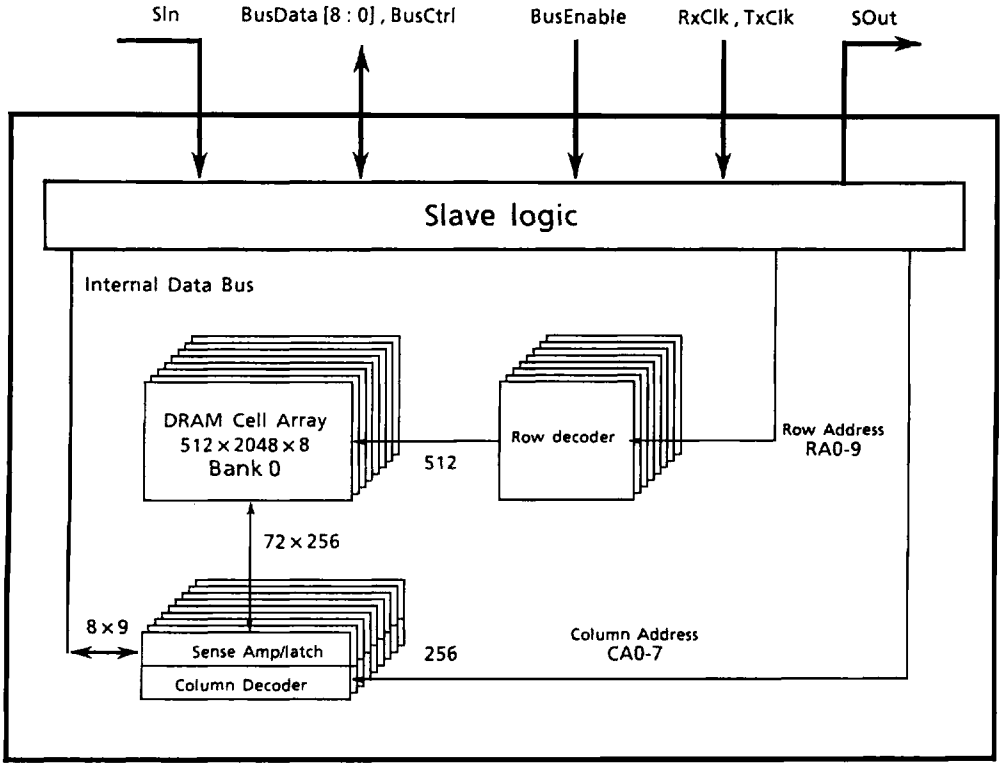
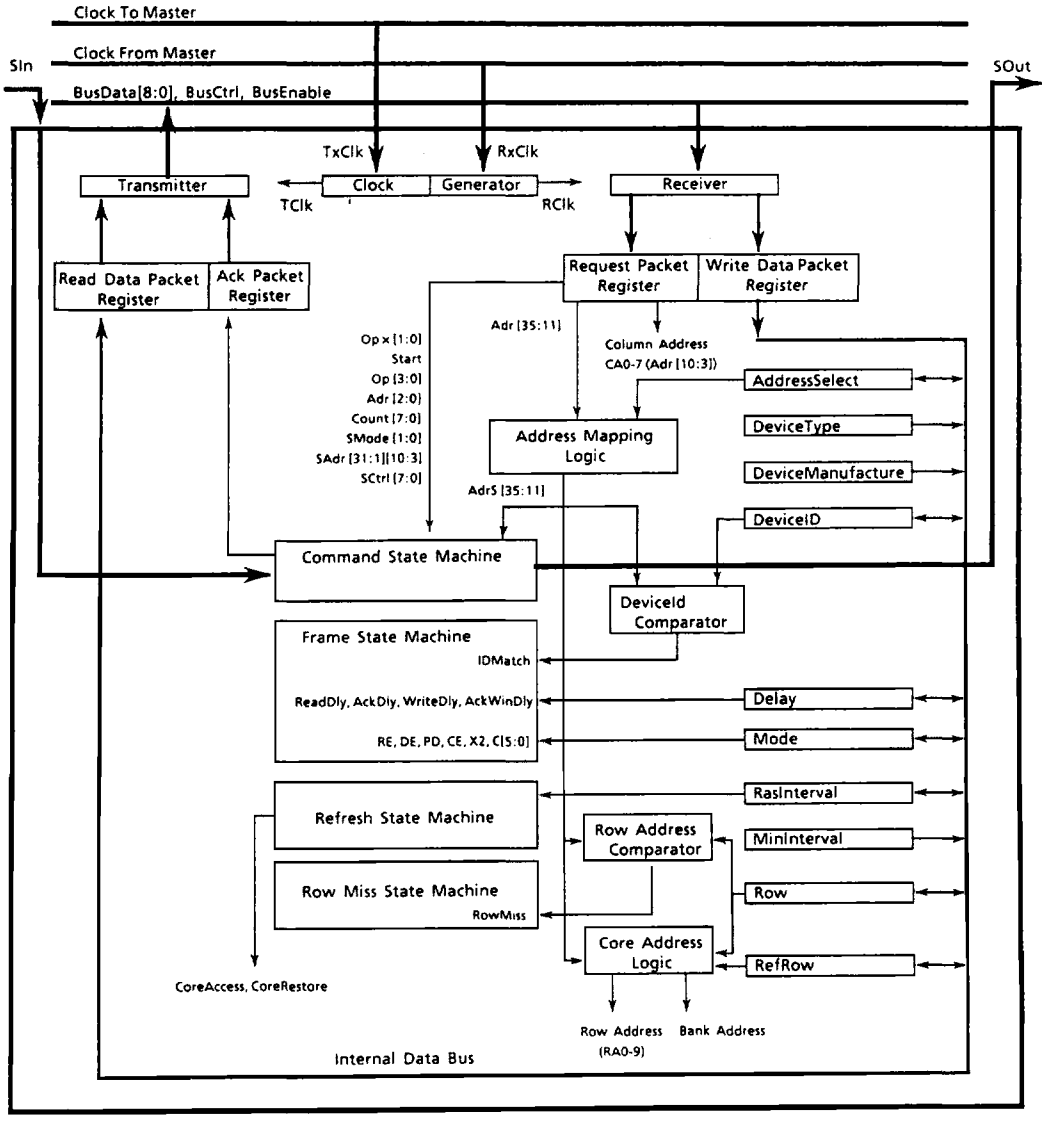
Internal Block Diagram of RDRAM



Internal Block Diagram of Slave Logic



Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}	Input Voltage	-0.5 ~ V_{DD} + 0.5	V	1
V_{IN}	Input Voltage (TTL)	-0.5 ~ 5.5	V	1
V_{dd}, V_{dd}-A	Power Supply Voltage	-0.5 ~ 6.5	V	1
T_{OPR}	Operating Temperature	0 ~ 70	°C	1
T_{STG}	Storage Temperature	-55 ~ 125	°C	1
T_{SOLDER}	Soldering Temperature	260	°C	1
P_D	Power Dissipation	3	W	1
I_{OUT}	Output Short-Circuit Current	50	mA	1

DC Recommended Operating Conditions (Ta = 0 ~ 70°C) Note 13

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{dd}, V_{dd}-A	Power Supply Voltage	3.0	3.3	3.6	V	2
V_{REF}	Reference Voltage	1.9	2.2	2.4	V	2
V_{IH}	High-Level Input Voltage	Vref + 0.35	–	Vref + 0.8	V	2, 14
V_{IL}	Low-Level Input Voltage	Vref + 0.8	–	Vref + 0.35	V	2, 14
V_{IH} (TTL)	High-Level Input Voltage (SIn Pin Only)	2.0	–	5.5	V	2, 14
V_{IL} (TTL)	Low-Level Input Voltage (SIn Pin Only)	-0.5	–	0.8	V	2, 14

Capacitance (V_{CC} = 3.3V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MAX.	UNIT	NOTE
C_I	Input Capacity (RxClk, TxClk, Busble, Vref)	–	2	pF
C_I (TTL)	Input Capacity (SIn)	–	10	
C_{IO}	Output Capacity (BusData[8:0], BusCtrl)	–	1	
C_{IO} (TTL)	Output Capacity (SOut)	–	15	

DC Electrical Characteristics

SYMBOL	ITEM	MIN.	MAX.	UNIT	NOTE
$I_{CC}1$	Operating Current	–	220	μA	3, 4, 5
$I_{CC}2$	Standby Current	–	65		3
$I_{CC}3$	Refresh Current	–	220		3, 5
$I_{CC}4$	Mean Operating Current (Typical)	TBD			13

SYMBOL	ITEM	MIN.	MAX.	UNIT	NOTE
V_{OH}	High-Level Output Voltage	Vref + 0.4	–	V	
V_{OL}	Low-Level Output Voltage	–	Vref - 0.4		
V_{OH} (TTL)	High-Level Output Voltage (SOut only)	2.4	Vdd		
V_{OL} (TTL)	Low-Level Output Voltage (SIn only)	0	0.4		
I_{OL}	Output Current (at low-level output)	–	35	mA	6
I_{OH}	Output Current (at high-level output)	-10	10	μA	
$I_{I(L)}$	Input Leak Current	-10	10	μA	
$I_{O(L)}$	Output Leak Current	-10	10	μA	
I_{OH}	Vref Current	-10	10	μA	

AC Permissible Operating Conditions and Characteristics

SYMBOL	ITEM	MIN.	MAX.	UNIT	NOTE
t_{CR}, t_{CF}	Rise Time and Fall Time of TxClk and RxClk	0.3	0.7	ns	7
t_{QR}, t_{QF}	Rise Time and Fall Time of Output Data	0.4	0.6		
t_{CYCLE}	TxClk and RxClk Cycle Times	4	6		
t_{TICK}	Data Transfer Time	0.5	0.5	t_{CYCLE}	8
t_{CH}, t_{CL}	High-level and low-level Time of TxClk and RxClk	45%	55%	t_{CYCLE}	
t_{TR}	TxClk and RxClk Differential	0	$0.7*t_{CYCLE}$	ns	
t_S	Data Set-up Time for RxClk	0.45	–		
t_H	Data Hold Time for RxClk	0.45	–		
t_Q	Data Output Time for RxClk	(1 - 0.45) (t_{CYCLE}/4)	(1 + 0.45) (t_{CYCLE}/4)		
t_{REF}	Refresh Interval	–	17	ms	
t_{LOCK}, t_{ACTIVE}	Look Time of Interval Clock Generator in ActiveMode	–	750	t_{CYCLE}	11
t_{LOCK}, $t_{STANDBY}$	Look Time of Interval Clock Generator in Standby-Mode	–	750	t_{CYCLE}	11

RDRAM Access Timing

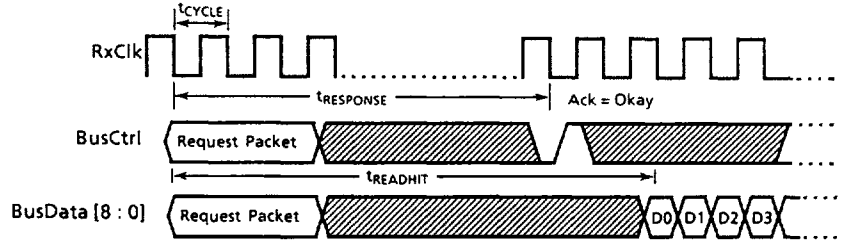
SYMBOL	ITEM	MIN.	MAX.	UNIT	NOTE
t_{CYCLE}	TxClk and RxClk Cycle-Times	4	6	ns	
$t_{RESPONSE}$	Time from start of request packet to start of read data packet (Row hit)	7	10	t_{CYCLE}	
$t_{READHIT}$	Time from start of request packet to start of read write packet (Row hit)	10	41		
$t_{WRITEHIT}$	Interval between row miss and sending of next request packet	4	35		8
$t_{RETRYSENSED\ CLEAN}$	Start of request packet for row miss (Nack) to start of request packet for row hit. The precious row is modified.	21			
$t_{RETRYSENSED\ DIRTY}$	Start of request packet for row miss (Nack) to start of request packet for row hit. The precious row is unmodified.	29			9
$t_{READBURST32}$	Time from start of request packet to end of 32-byte read data packet (Row hit).	26			9
$t_{READBURST256}$	Time from start of request packet to end of 256-byte read data packet (Row hit).	138			9
$t_{WRITEBURST32}$	Time from start of request packet to end of 32-byte write data packet (Row hit).	20			10
$t_{WRITEBURST256}$	Time from start of request packet to end of 256-byte write data packet (Row hit).	132			10
$t_{POSTREGWRITEDELAY}$	Delay from the end of the current transaction to the beginning of the next transaction	4			
$t_{POSTMEMWRITEDELAY}$	Delay from the end of the current transaction to the beginning of the next transaction	2			
$t_{SERIALREADOFFSET}$	Delay from the beginning of a serial address subpacket or serial control packet	13		t_{CYCLE}	
$t_{SERIALWRITEOFFSET}$	Delay from the beginning of a serial address subpacket or serial control packet to the beginning of the read data subpacket	5		t_{CYCLE}	

Row Miss and Refresh Parameters

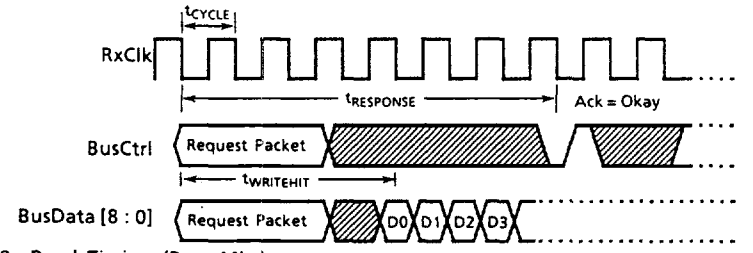
SYMBOL	ITEM	MIN.	MAX.	UNIT	NOTE
RowOverhead	Overhead time (Standard value)	9	–	t_{CYCLE}	
RowPrecharge	Minimum precharge time (Standard value)	9	–	t_{CYCLE}	
RowSense	Rasinterval [1] [4 : 0] register	8	–	t_{CYCLE}	
t_{RAS}	RAS pulse width	60	–	ns	

Access Timing Chart

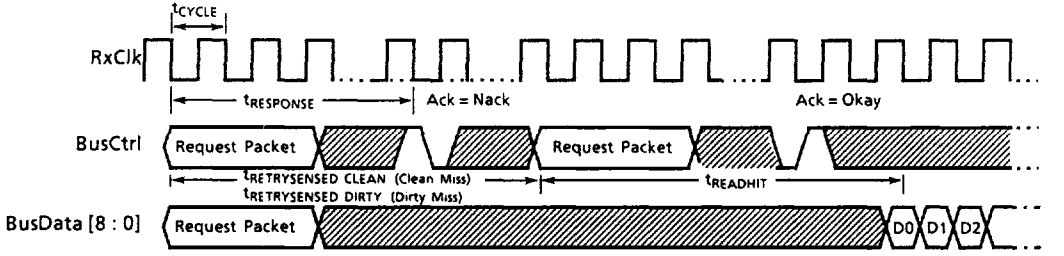
1. Read Timing (Row Hit)



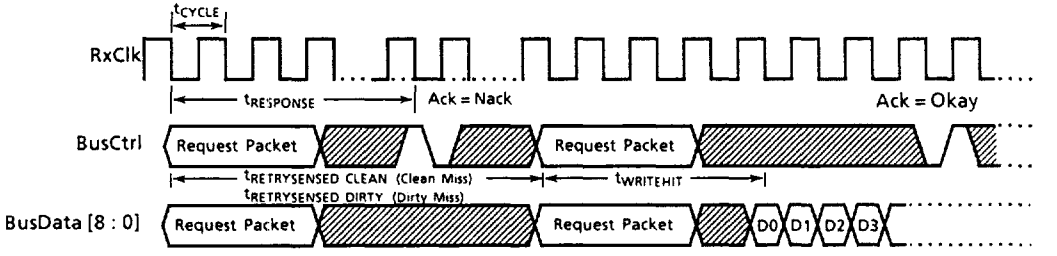
2. Write Timing (Row Hit)



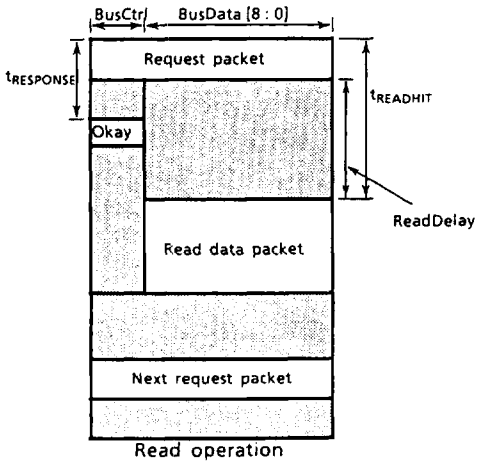
3. Read Timing (Row Miss)

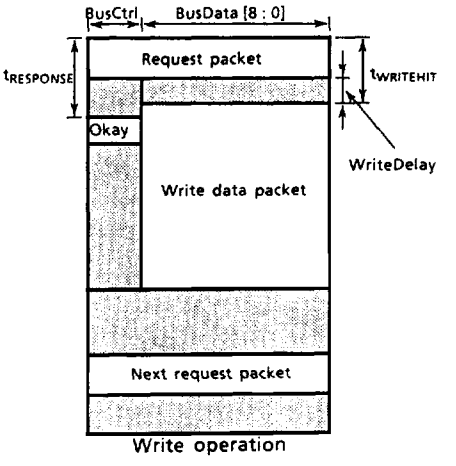


4. Write Timing (Row Miss)

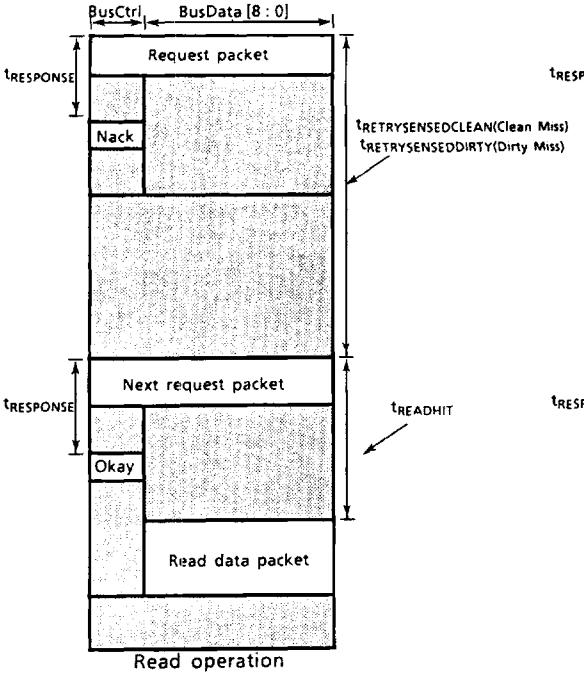


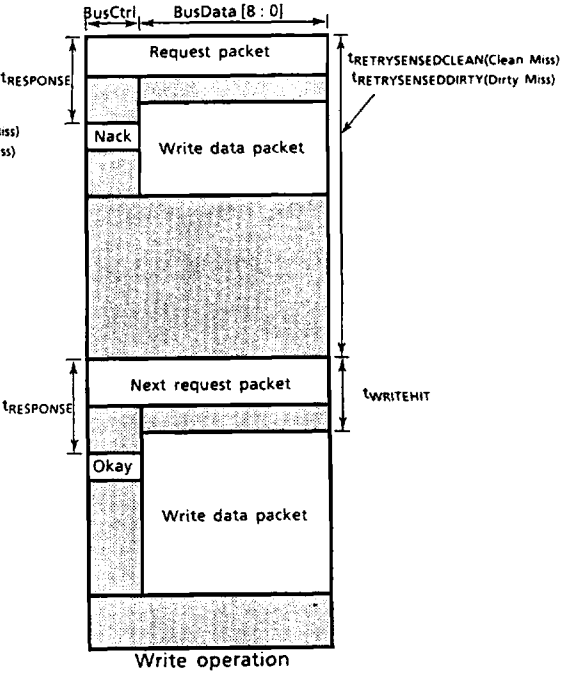
Access Time For Row Sense Amp Cache Hit



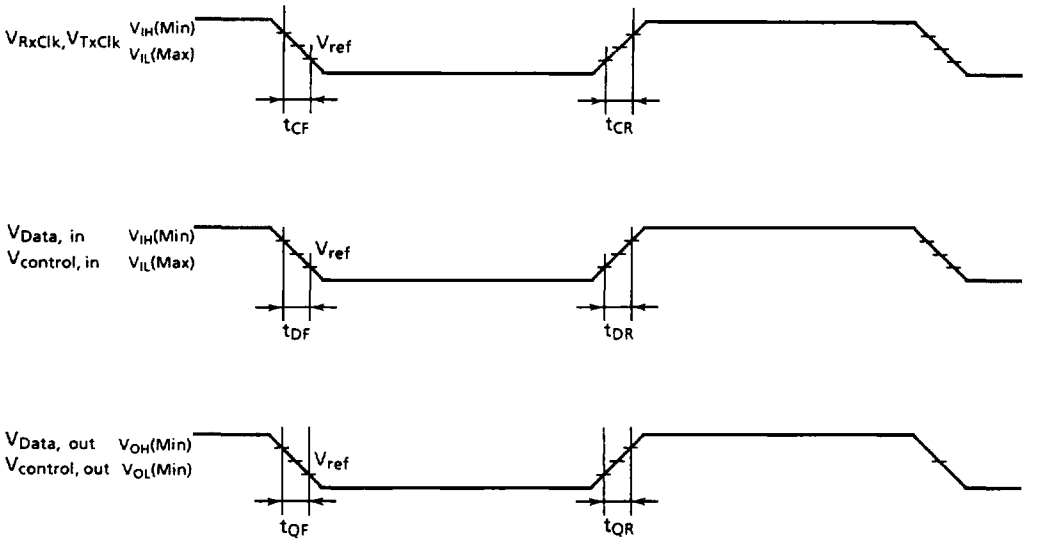


Access Time

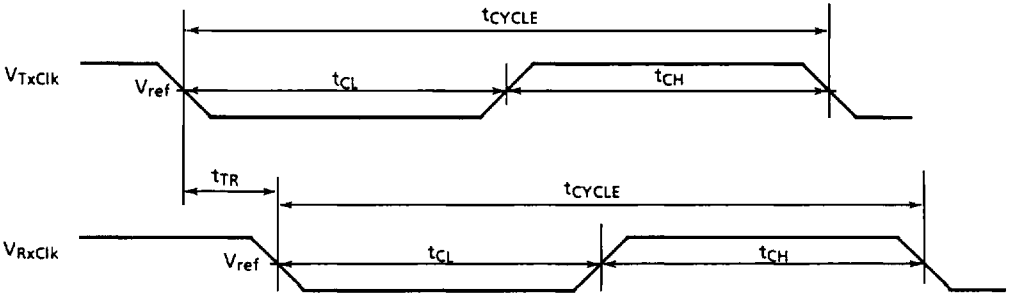




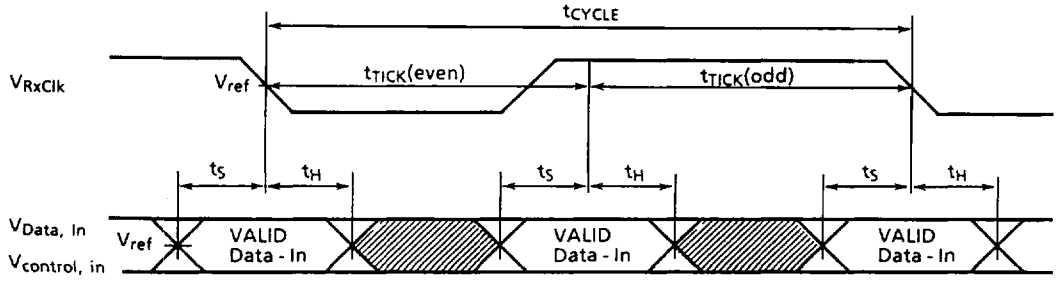
Rise and Fall Timing I/O Waveform



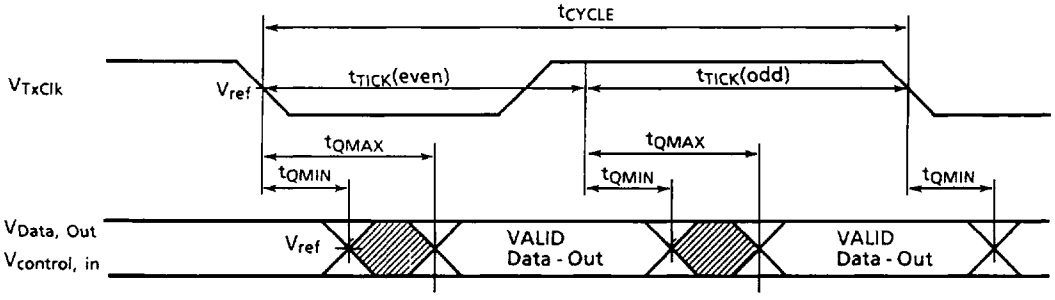
TxClk, RxClk Timing



Write Data Set Up and Hold Timing for RxClk



Write Data Output Timing for TxClk



Notes:

1. Stress greater than the maximum rated value may subject the device to permanent damage.
2. All voltages are given with GND as the reference.
3. These values do not include the BusData [8 : 0] or BusCtrl output currents.
4. This value is valid when 16 bytes of data are written to memory when the row sense amp cache is hit.
5. These values are valid when t_{CYCLE} = 4ns. They are strongly affected by the value of t_{CYCLE}.
6. The low-level output current is the current when the RDRAM outputs logical level "1". This parameter can be set in the Mode Register in the slave logic.
7. Vref is used as the reference voltage when measuring the input signal timing.
8. Calculated from the following conditions: t_{CYCLE} = 4ns, and t_{RP} (Min.), t_{RP} (Max.), and RowOverhead = $2t_{CYCLE}$.
9. Value calculated from $t_{READHIT}$ (Min).
10. Value calculated from $t_{WRITEHIT}$ (Min).
11. These values are 3μs when t_{CYCLE} = 4ns.
12. These values are the average operation current for graphics application systems.
13. Data input swing = Vref+ / -0.35Vmin.
    Clock input swing = 1Volt min. peak to peak, 450mV min. from Vref.

[1] Pin Function

Bus Data I/O: BusData [8 : 0]

This pin is used inputting request packets and write data packets, and for outputting read data packets. The signal level is referenced to Vref, low-level being logical "1", high-level being "0".

Bus Control I/O: BusCtrl

This pin is used for request packet input and acknowledge packet output. This signal level is referenced to Vref, low-level being logical "1", high-level being logical "0".

Bus Enable Input: BusEnable

This pin is used for selecting the Rambus DRAM (RDRAM) operating mode (reset, active, standby, or power-down). Transition among the four modes is mainly achieved by varying the length of signal input (pulse width). When no signal is input, standby mode is automatically selected. Active mode is selected with a narrow signal pulse, while reset mode is selected by a wider pulse width. The signal level is referenced to Vref, low-level being logical "0".

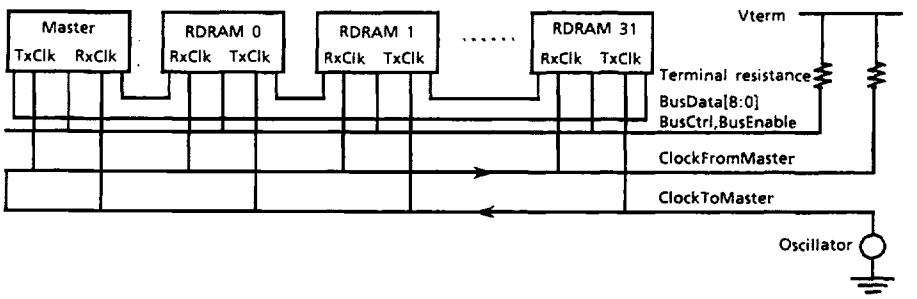
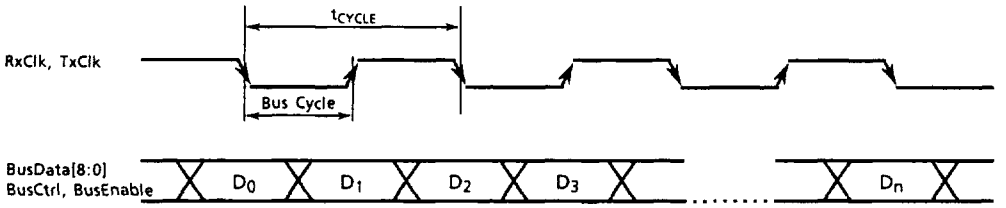


Figure 1. Rambus System Clock



n : Bus Cycle NO.

Figure 2. Bus Cycle

High-Speed Sync Clocks: RxClk, TxClk

These are high-speed sync clocks for input and output data. RxClk is used for input data, TxClk is used for output data. In the Rambus system, both clock edges are used for sending data (see Figure 2). The rate between clock edges is known as the bus cycle, with data sent on the trailing edge being known as even bus cycle data and data sent on the leading edge being known as odd bus cycle data. RDRAM access is all referenced to even bus cycle (trailing edge of clock).

In Rambus systems using RDRAM, skewing between the clock signals and data signals must be minimized in order to achieve high-speed data transfer. For this reason, the clock signal line is looped as shown in Figure 1 as the ClockFrom Master. In addition, the clock signal line and the data signal line must be arranged in parallel so as to have the same impedance. In Figure 1, the clock traveling from the RDRAM (RDRAM31) at the end of the bus toward the master is known as the ClockToMaster, while that traveling back from the master to the RDRAM is called the CLockFrom Master. Because ClockToMaster is used as the sync clock when sending data from the RDRAM to the master, ClockToMaster becomes TxClk at the RDRAM and Rx at the master. Vice versa, when data is sent form the master to the RDRAM ClockFromMaster becomes the sync clock and is TxClk at the master and RxClk at the RDRAM.

	Master	RDRAM
ClockToMaster	RxClk	TxClk
ClockFromMaster	TxClk	RxClk

The use of this clock system means that the data and clock are always in the same direction, minimizing any skewing between them.

Serial Signal Input and Output: SIn, SOut

These signals are used to initialized the RDRAM and to create the Rambus daisy chain. These signals are the only RDRAM active signals that are CMOS level low-speed signals.

In the Rambus system, each device (RDRAM) must be initialized after powering up. The process of initialization requires the allocation of the unique addresses (DeviceID) to each RDRAM in the group.

This is achieved continuously using SIn and SOut. SIn and SOutlink the whole system as a daisy chain (see Figure 3). In addition to initialization, SIn and SOut are also used for refresh clock input when the RDRAM are in the power-down operating mode. They are not otherwise used in normal operation.

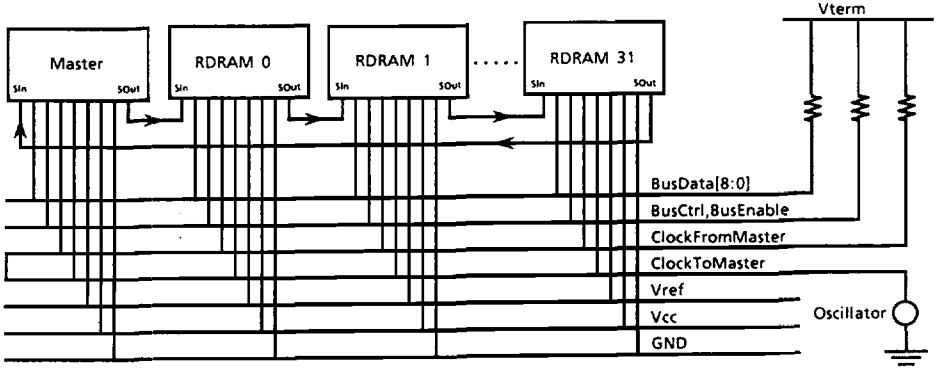


Figure 3. Rambus System

Reference Voltage: Vref

This is the reference level for the high-speed small-amplitude signals (BusData [8 : 0], BusCtrl, BusEnable, RxClk, TxClk) used by the RDRAM. When signal levels higher than Vref, it is logical "0"; when lower, it is logical "1".

Post

These pins support the package. They are not electronically connected to the chip.

NU (Not Usable)

This pin is connected internally to the lead frame. Because this pin outputs the board potential, do not connect it electrically.

[2] RDRAM Basic Operation

RDRAM access is basically accomplished using request packets, acknowledge packets, and data packets. A packet is a group of contiguous bits sent via the 10 I/O bus lines of BusCtrl and BusData [8 : 0]. These packets play the following roles.

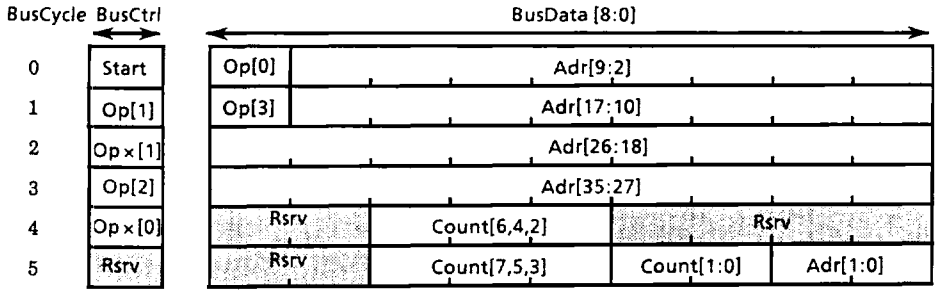


Figure 4. Structure

(1) Request Packet

The request packet is the first packet sent when accessing RDRAM. The request packet, which is made up of 6cycles X 10bits of data, includes RDRAM address information, the write/read data packet size, the operation command (to select reading or writing to memory or register), and the mask command for the write data. Figure 4 shows the request packet structure.

• Start

The start bit shows the start of a request packet and is a logical low "1" (low level electrical). Thus, the RDRAM interprets the output of a "1" on the BusCtrl line as the start of a request packet.

• Adr [35 : 3] (= Address [35 : 3])

The address bits show the address requested by the master. As shown in Table 1, the 33-bit address space includes the device ID address and bank address, and the row address and column address.

Table 1. Address Space of Request Packet

	Memory Space	Register Space
Adr [10 : 3]	Column address	Register address
Adr [19 : 11]	Row address	Don't Care
Adr [20]	Bank address	Don't Care
Adr [35 : 21]	Device ID address	Device ID address

• Op [3 : 0]/Op X [1 : 0] (= Operation Command)
These bits select the RDRAM operation command.

Table 2 shows the operations for Op [3 : 0]/Op X [1 : 0].

Table 2. Operation Commands

Op [3 : 0]	Op X [1 : 0]	Name	
0000	00	Rseq	Read sequential data from memory
0000	01	Rseq	Read non-sequential data from memory
0100	00	WseqNpb	Write sequential data to memory space with no per-bit mask
0100	01	WseqDpb	Write sequential data to memory space with data-per-bit masking
0100	10	WseqBpb	Write sequential data to memory space with both-per-bit masking
0110	11	WseqMpb	Write sequential data to memory space with mask-er-bit masking
0111	00	Rreg	Read sequential data from register
1000	00	Wreg	Write sequential data from register
1000	01	WnsqNpb	Write non-sequential data to memory space with data-per-bit masking
1000	10	WnsqBpb	Write non-sequential data to memory space with mask-per-bit masking
1000	11	WbnsMpb	Write non-sequential data to memory space with mask-per-bit masking
1100	00	WbnsNpb	Write non-sequential data to memory space with byte masking and no per-bit masking
1100	01	WbnsDpb	Write non-sequential data to memory space with byte masking
1100	11	WbnsMpb	Write non-sequential data to memory space with byte masking and mask-per-bit masking
1111		WregB	Broadcast write to register space of all responding devices with no acknowledge permitted.

• Count [7 : 3]
The count bits show the size of the write/read data packet. The oct-byte (OB) unit is used as the unit of the data packet size. A value between 1OB (8bytes) and 32OB (256bytes) can be specified.
Count [7 : 3] = 00000 means 1OB, Count [7 : 3] = 00001 means 2OB, Count [7 : 3] = 11111 means 32OB.

• Adr [2 : 0]/ Count [2 : 0]
These bits select mask information for write data. Adr [2 : 0] and Count [2 : 0] are the mask information for the first and last OB in the write packet.

• Rsrv (Reserved)
These bits are unused. Use the master to set them to "0" when a request is issued.

(2) Acknowledge Packet
The acknowledge Packet (Ack [1 : 0]) is the RDRAM response signal to the request packet. Table 3 shows the meaning of the respective Ack [1 : 0] signals.

Table 3. Acknowledge Packet

Ack [1 : 0]	Command	Description
00	Nonexistent	Nonexistent shows that no RDRAM has the requested address if no output is detected on the BusCtrl line within a set time after the end request packet.
01	Okay	Okay shows the completion of receipt of the request packet.
10	Nack	Nack shows that the requested device cannot respond to the request. NAck is output for RDRAM in the case of a row or refresh, etc. If a Nack is returned, the master waits before sending the request again.
11	Reserved	Reserved is not currently used. RDRAM does not output Reserved.

(3) Data Packet
The data packet is a group of contiguous write or read data for memory or register address space. The data packet consists of between 1OB (8byte) and 32OB (256bytes). (It is always 1OB when reading or writing to registers.)

(4) Serial Mode Packet
The serial mode packet (SMode [1 : 0]) controls the state of the Count00 [3 : 0] and Count11 [7 : 0] counters. These counters cause operating mode transitions when they reach special values. Figure 5 shows the format of the serial mode packet.

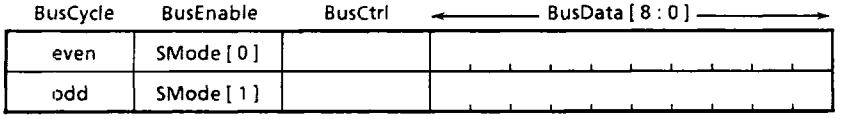


Figure 5. Serial Mode Packet Format

Table 4 shows the meaning of SMode [1 : 0] signals.

Table 4. Serial Mode Fields

SMode [1 : 0]	Description
00	Increments Count00 [3 : 0], Clears Count11 [7 : 0]
01	–
10	–
11	Increments Count11 [7 : 0], Clears Count00 [3 : 0]

(5) Serial Address Packet

The serial address packet (SAdr [i] [10 ; 3]) provides eight low-order address bits for each octbyte which is accessed in memory space. These eight address bits are transferred serially on the BusEnable pin on the RDRAM, thus these are called a serial address. This packet is used in random access mode.

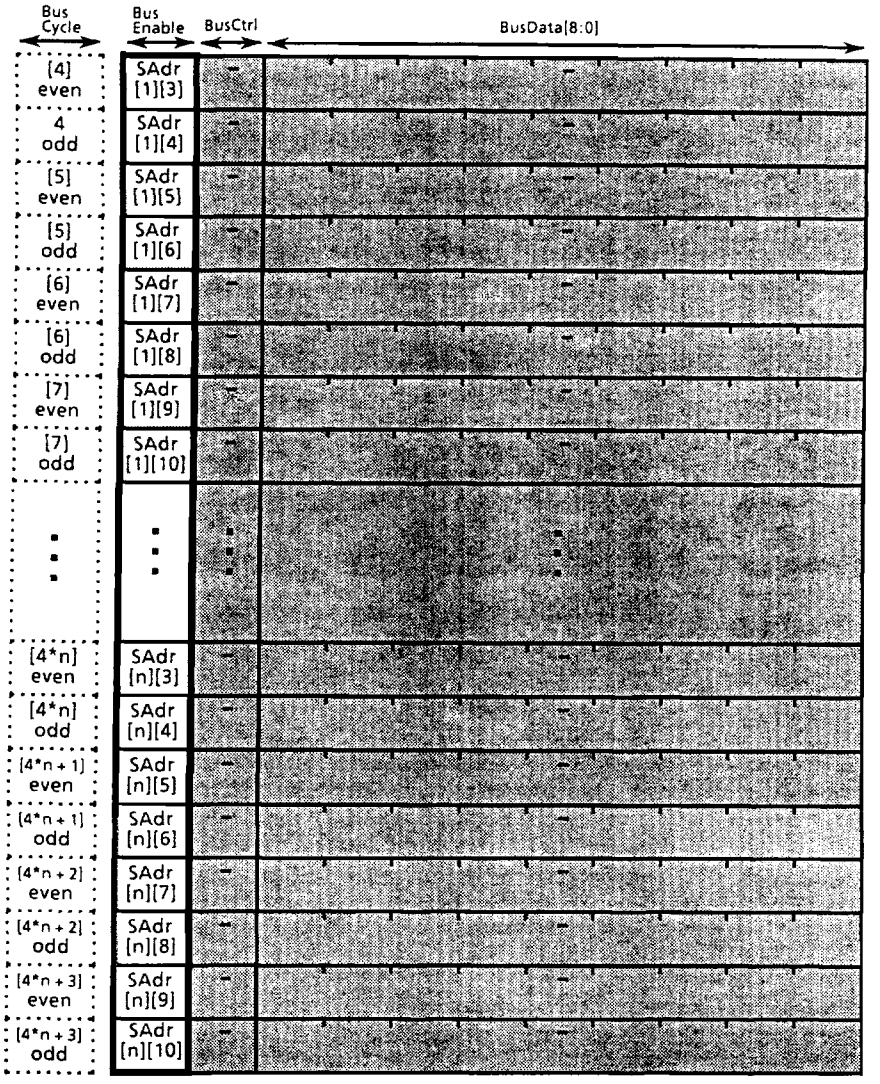


Figure 6. Serial Address Packet Format

Table 5. Serial Address Packet

Serial Address Fields	Description
SAdr [i] [10 : 3]	Low-order address bits for each octbyte

(6) Serial Control Packet

The serial control packet provides for the early termination of a memory space read or write transaction. It consists of eight bits transferred serially on the BusCtrl pin of the device. The commands which use this packet are all of those which access memory space. The register read and write commands do not use the serial control packet. Figure 7 shows the format of the serial control packet.

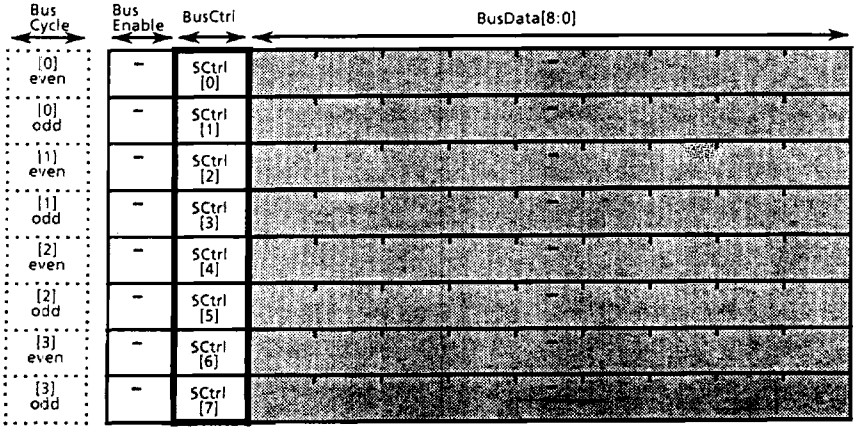


Figure 7. Serial Control Packet Format

Table 6 shows the function of the bits within the serial control fields. The SCtrl [5] bit is used to control termination. The bits in the even bus ticks must be zero in order for framing to work properly. The other three odd tick bits are unimplemented.

Table 6. Serial Control Fields

Serial Control Fields	Description
SCtrl [0]	This bit must be a zero due to framing requirements
SCtrl [1]	unimplemented
SCtrl [2]	This bit must be a zero due to framing requirements
SCtrl [3]	unimplemented
SCtrl [4]	This bit must be a zero due to framing requirements
SCtrl [5]	0 means don't terminate the current access 0 means terminate the current access
SCtrl [6]	This bit must be a zero due to framing requirements
SCtrl [7]	unimplemented

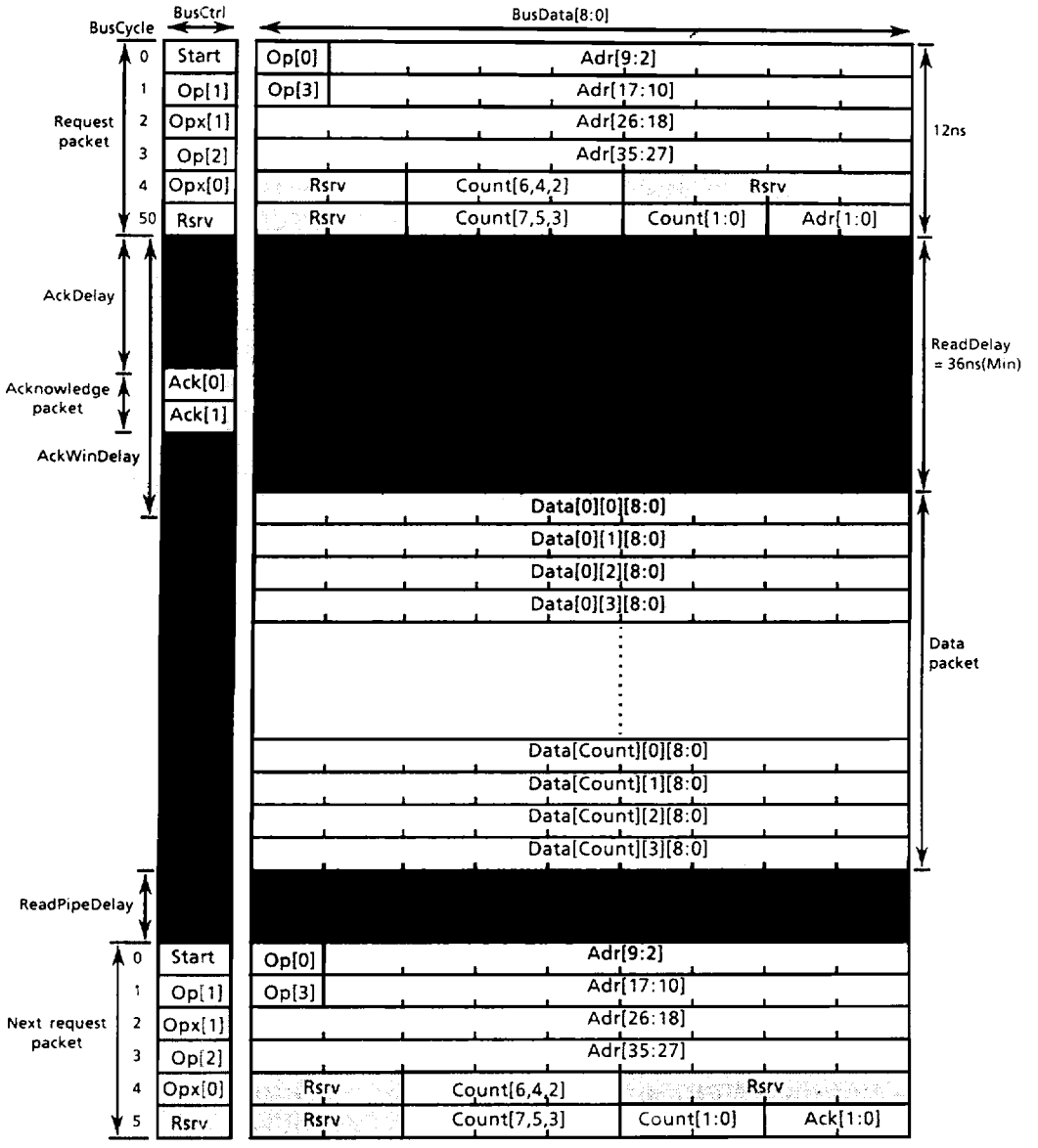


Figure 8. Read Operation for Memory or Register Address Space (Ack packet = Okay)

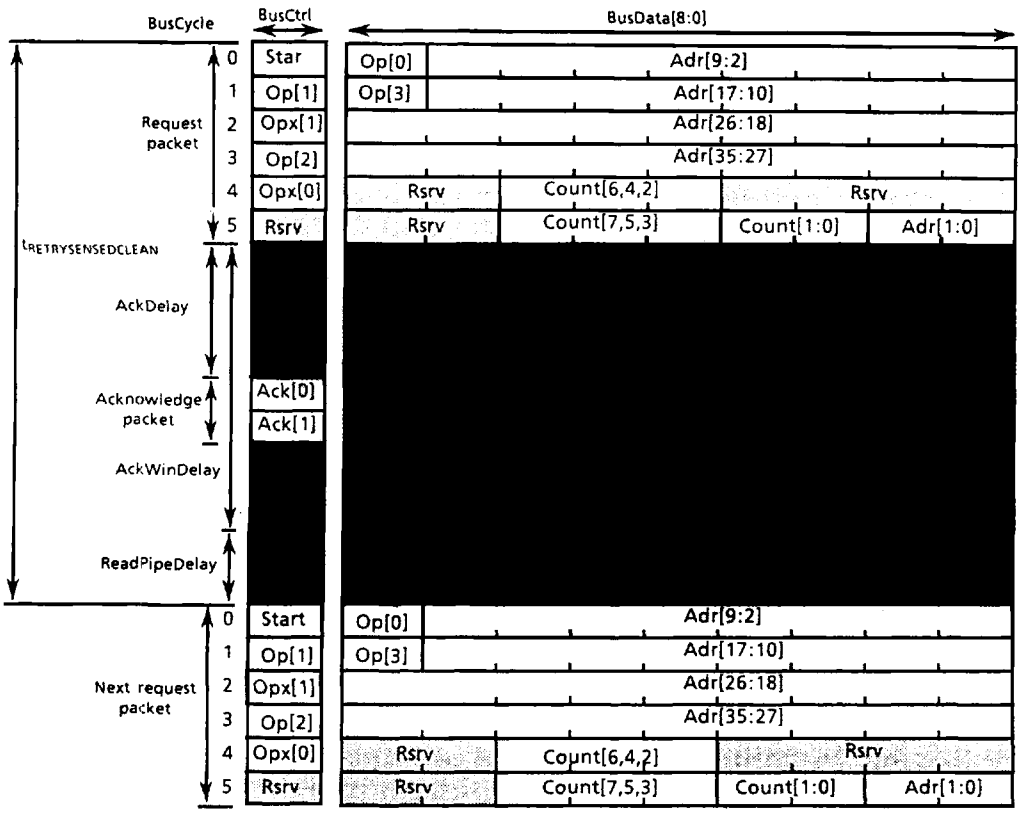


Figure 9. Read Operation for Memory or Register Address Space (Ack packet = Nack or Nonexistent)

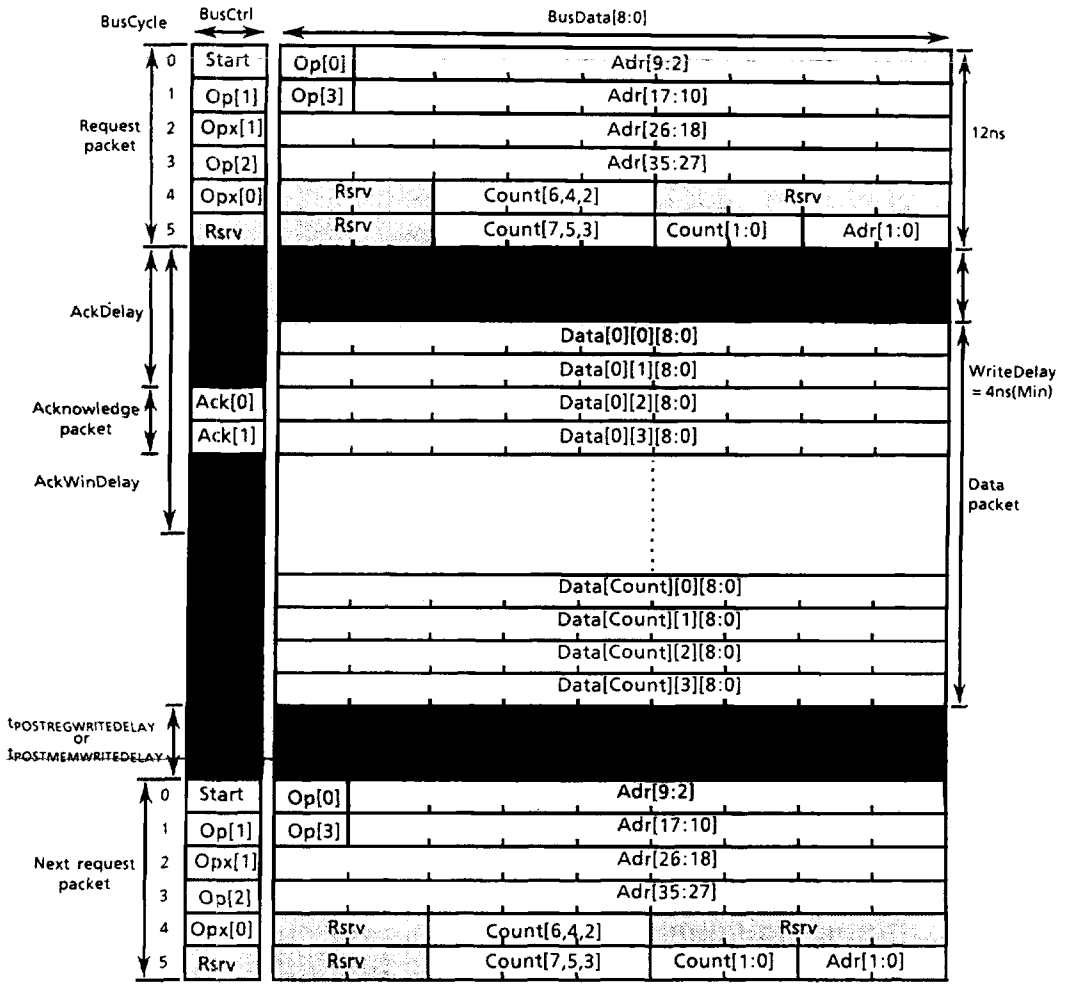


Figure 10. Write Operation for Memory or Register Address Space (Ack packet = Okay)

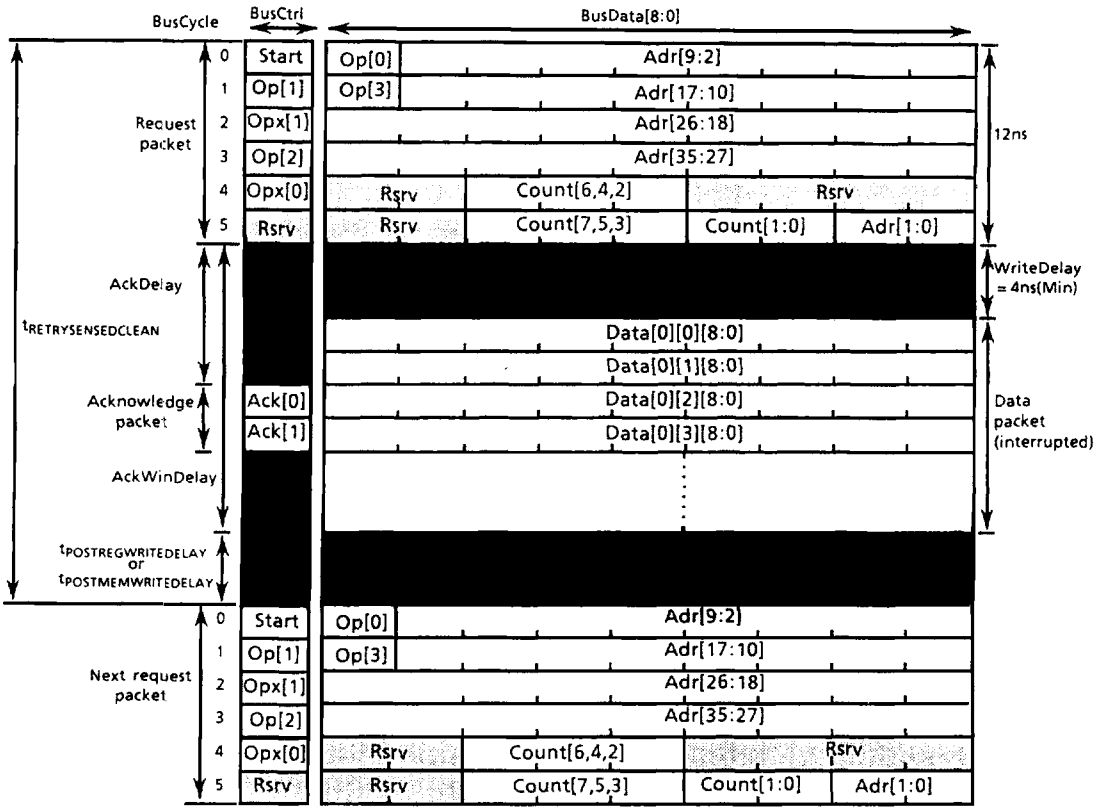


Figure 11. Write Operation for Memory or Register Address Space (Ackpacket = Nack or Nonexistent)

[3] Read Operation From Memory or Register

(1) Normal Read Operation

Actual memory or register access using each of the packets is following. Figure 8 shows the process when a read operation is executed on the RDRAM memory or register space and the RDRAM sends an Okay Ack package.

RDRAM access starts a 6-cycle request packet transmission from the master. The RDRAM detects the request packet from the output (Start bit) on the BusCtrl line. On completion of the request packet, and after AckDelay, the RDRAM outputs a 2-cycle packet.

All devices connected to the Rambus system ignore output on the BusCtrl line for a set interval (AckWinDelay) after the end of the request packet. Therefore, output of the Ack packet cannot be confused with the Start bit of the request packet.

When the RDRAM responds with an Okay Ack packet, the read data packet is output after a delay (ReadDelay) after the end of the request packet. The read operation ends at whichever is last, the end of the AckWindow (AckWinDelay delay after the end of the request packet) or the end of the data packet.

Next, if another operation is to be executed, it starts after a delay of ReadPipeDelay from the end of the preceding data packet. (The standard value of ReadPipeDelay is tCYCLE.)

The values of AckWinDelay, AckDelay, ReadDelay, and WriteDelay can be programmed by accessing the Delay register in the slave logic.

(2) Nack or Nonexistent

As Figure 9 shows, no read data packet is output when the RDRAM returns a nack or Nonexistent Ack packet in read operation. When the Ack packet is NAck, the RDRAM prepares for another request packet to be sent. The time it takes to prepare depends on the cause of the Nack (row miss or refresh). In the case of a row miss, the preparation time is the time for row precharging ($t_{ROWPRECHARGE}$), row access ($t_{ROWSENSE}$) and RowOverhead.

The value of $t_{ROWPRECHARGE}$ and $t_{ROWSENSE}$ can programmed by accessing the RasInterval register in the slave logic. In the case of a refresh, an additional four row cycles are added. During this preparation interval, the RDRAM must wait for the master to output the next request packet.

(3) Read Operation

Resq: Executes a read operation on the RDRAM memory space. The RDRAM configures a read data packet to send to the master

Rreg: Executes a read operation on RDRAM register space. The RDRAM configures a read data packet to send to the master

[4] Write Operations to Memory or Registers

(1) Normal Write Operation

In contrast to read operations, write data packet is sent from the master before the Ack packet is output, as shown in Figure 10. When another operation is performed immediately after a write operation, it starts after a delay of $t_{POSTREGWRITEDELAY}$ or $t_{POSTMEMWRITEDELAY}$ from the end of the proceeding data packet.

(2) Write Operations When Nack or Nonexistent is Returned (see Figure 11)

In a write operation, the write data packet starts to be sent before the Ack packet is output. Therefore, if Nack or Nonexistent Ack packet is output, the master interrupts the output of the write data packet.

(3) Write Operation Commands

WnsqNpb: Executes a write operation on RDRAM memory space.

Wreg: Executes a write operation on RDRAM register space.

WregB: The RDRAMs can return a Nack, the master is able to confirm that there is a device under internal operation and cannot perform the write operation.

[5] Random Access Mode

In this mode, non-contiguous blocks of memory can be accessed through the use of the read and write non-sequential operations. Using these commands, multiple eight-byte blocks (octbytes) of data within a cache line can be accessed in a non-sequential mode. To do this, the master device sends a request packet specifying a non-sequential operation along with the address of the first octbyte to be accessed.

The master device also generates a serial address packet on the BusEnable signal that specifies that specifies the address of the next octbyte. Successive serial address packets continue to specify new addresses in the cache line while data is continuously transferred until the access is complete.

Figure 12 shows a memory space read transaction for a transaction for a command which uses the serial address packet. Figure 13 shows a memory space write transaction with the serial address packet.

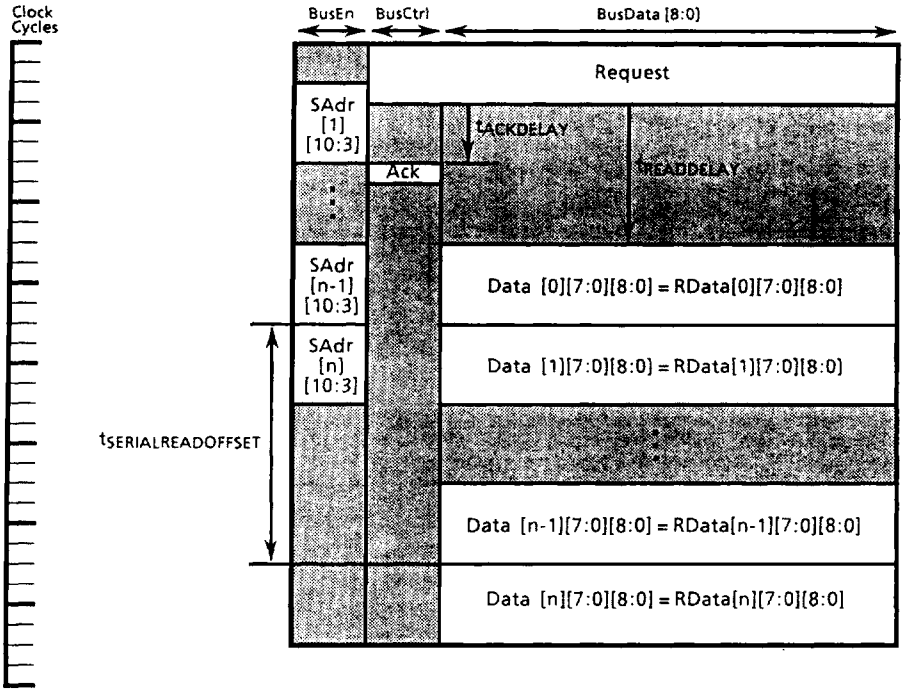


Figure 12. Read Transaction with Serial Address Packet

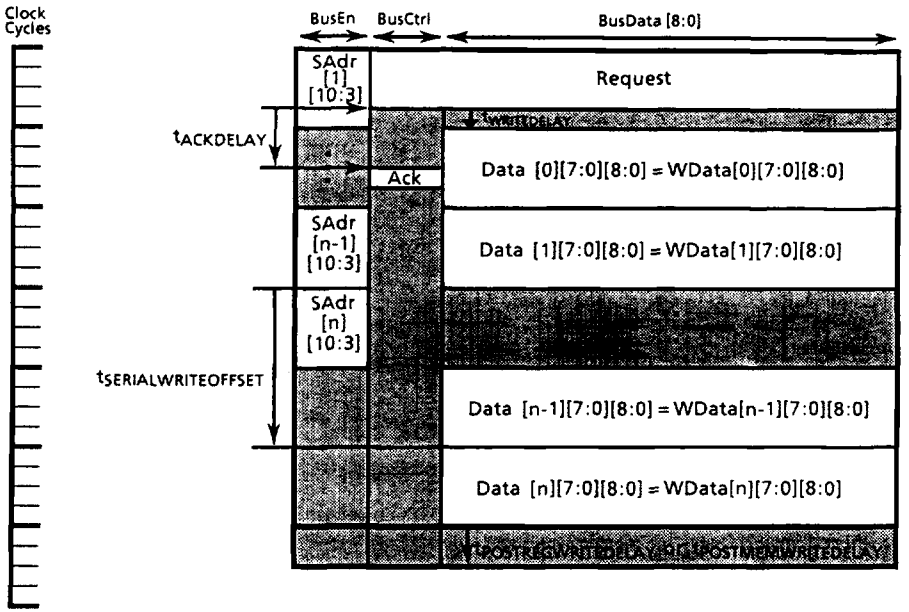


Figure 13. Write Transaction with Serial Address Packet

[6] Serial Control Packet

The serial controls packet provides for the early termination of a memory space read or write transaction before the specified data count (data packet length) in the Count [7 : 3] field has elapsed. Figure 14 shows a memory space read transaction for a command which uses the serial control packet, and Figure 15 shows a memory space write transaction with serial control packet.

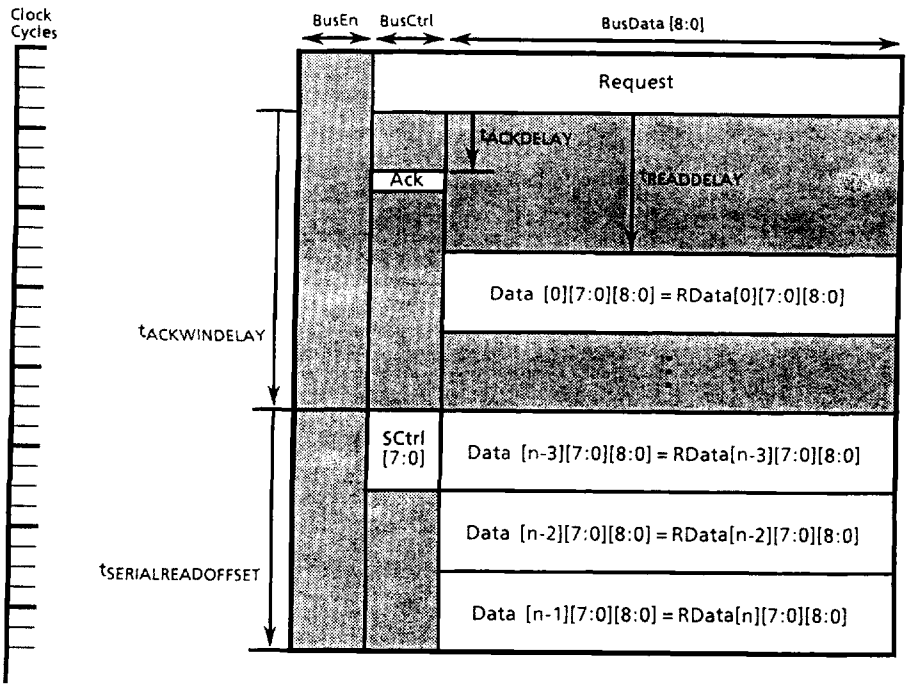


Figure 14. Read Transaction with Serial Control Packet

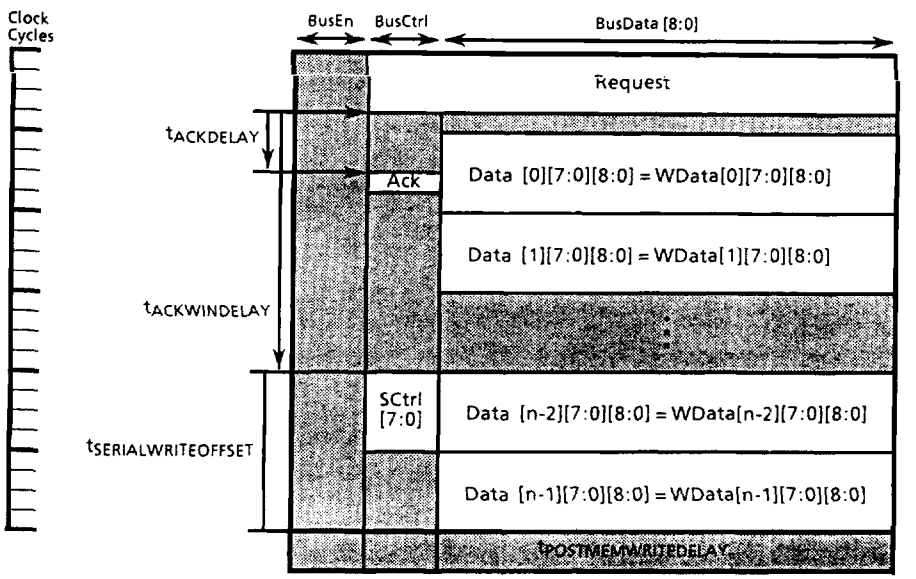


Figure 15. Write Transaction with Serial Control Packet

[7] The Mask Function

The RDRAM mask function is valid for the first and last 1OB of the write data packets. The mask information for each OB can be selected using Count [2 : 0] and Adr [2 : 0], as shown in Table 5.

Table 7. Mask Selection Bits

Mask information for 1st QB		Mask information for 1st QB	
Adr [2 : 0]	ByteMaskLS [7 : 0]	Count [2 : 0]	ByteMaskMS [7 : 0]
000	11111111	000	00000001
001	11111110	001	00000011
010	11111100	010	00000111
011	11111000	011	00001111
100	11110000	100	00011111
101	11100000	101	00111111
110	11000000	110	01111111
111	10000000	111	11111111

The "0's" in Table 7 indicate masking. All 10Bs other than the first and last are therefore "1111" (all are written). If the data packet is only 1OB (Count [7 : 3} = 00000), the logical "AND" of Mask [7 : 4] and Mask [3 : 0] becomes the mask information, as shown in Table 8. In this case, the transmitted data can be controlled in 1-byte units. Figure 16 shows a masked write operation when sending 8 bytes.

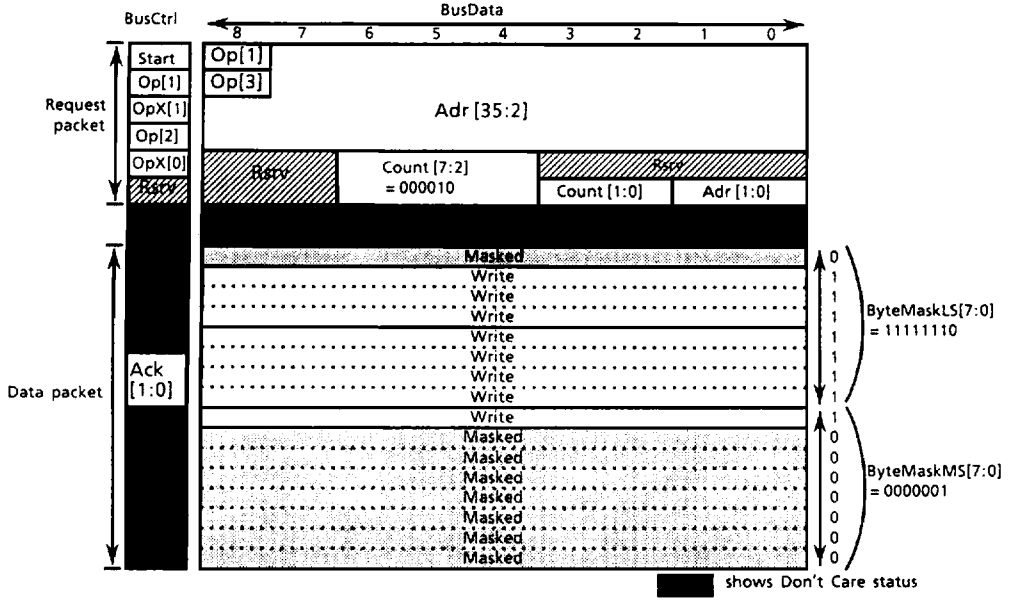


Figure 16. Mask Function

Table 8. Mask Selection bits and Size of Transmitted Data Packet

• 1 Byte Transmission

Count [2 : 0]	Count [7 : 0]	Adr [2 : 0]	ByteMaskMS [7 : 0]	Middle ByteMask [7 : 0]	ByteMaskLS [7 : 0]	ByteMaskLS [7 : 0] and ByteMaskMS [7 : 0]
0000	000	000	00000001	n/a	11111111	00000001
0000	001	001	00000011	n/a	11111110	00000010
0000	010	010	00000111	n/a	11111100	00000100
0000	011	011	00001111	n/a	11111000	00001000
0000	100	100	00011111	n/a	11110000	00010000
0000	101	101	00111111	n/a	11100000	00100000
0000	110	110	01111111	n/a	11000000	01000000
0000	111	111	11111111	n/a	10000000	10000000

• 2 Byte Transmission

Count [2 : 0]	Count [7 : 0]	Adr [2 : 0]	ByteMaskMS [7 : 0]	Middle ByteMask [7 : 0]	ByteMaskLS [7 : 0]	ByteMaskLS [7 : 0] and ByteMaskMS [7 : 0]
0000	000	000	00000001	n/a	11111111	00000011
0000	001	001	00000011	n/a	11111110	00000110
0000	010	010	00000111	n/a	11111100	00001100
0000	011	011	00001111	n/a	11111000	00011000
0000	100	100	00011111	n/a	11110000	00110000
0000	101	101	00111111	n/a	11100000	01100000
0000	110	110	01111111	n/a	11000000	11000000
0000	111	111	11111111	n/a	10000000	n/a

• 4 Byte Transmission

Count [2 : 0]	Count [7 : 0]	Adr [2 : 0]	ByteMaskMS [7 : 0]	Middle ByteMask [7 : 0]	ByteMaskLS [7 : 0]	ByteMaskLS [7 : 0] and ByteMaskMS [7 : 0]
0000	000	000	00000001	n/a	11111111	00001111
0000	001	001	00000011	n/a	11111110	00011110
0000	010	010	00000111	n/a	11111100	00111100
0000	011	011	00001111	n/a	11111000	01111000
0000	100	100	00011111	n/a	11110000	11110000
0000	101	101	00111111	n/a	11100000	n/a
0000	110	110	01111111	n/a	11000000	n/a
0000	111	111	11111111	n/a	10000000	n/a

• 8 Byte Transmission

Count [2 : 0]	Count [7 : 0]	Adr [2 : 0]	ByteMaskMS [7 : 0]	Middle ByteMask [7 : 0]	ByteMaskLS [7 : 0]	ByteMaskLS [7 : 0] and ByteMaskMS [7 : 0]
0000	000	000	00000001	n/a	11111111	11111111
0000	001	001	00000011	n/a	11111110	n/a
0000	010	010	00000111	n/a	11111100	n/a
0000	011	011	00001111	n/a	11111000	n/a
0000	100	100	00011111	n/a	11110000	n/a
0000	101	101	00111111	n/a	11100000	n/a
0000	110	110	01111111	n/a	11000000	n/a
0000	111	111	11111111	n/a	10000000	n/a

[8] Bit Masking

TC59R0808HK supports three forms of bit masking that are available for write operations. These operations are referred to as data-per-bit (Dpb), mask-per-bit (Mbp), both-per-bit (Bbp)masking.

- Data-per-bit (Dpb) mode

In the Dpb operation, the MDReg is used to hold a static mask that is applied to all octbytes of data written to the RDRAM core.

- Mask-per-bit (Mpb) mode

In the Mpb operation, the MDReg is used to hold an octbyte of static data that is masked by dynamic bit masks supplied in the data packets before being written to RDRAM. Figure 18 shows the format of the Both-per-bit (Bpb) write transactions.

- Both-per-bit (Mpb) mode

The Bpb operation requires data packets to alternate between mask and data octbytes. The even data packets carry bit masking information which is placed in the MDReg while the odd data packets carry bit masking information which is placed in the MDReg while the odd data packets carry the data to be masked by the latest contents on the MDReg. Figure 19 shows the format for the Both-per-bit (Bpb) write transactions.

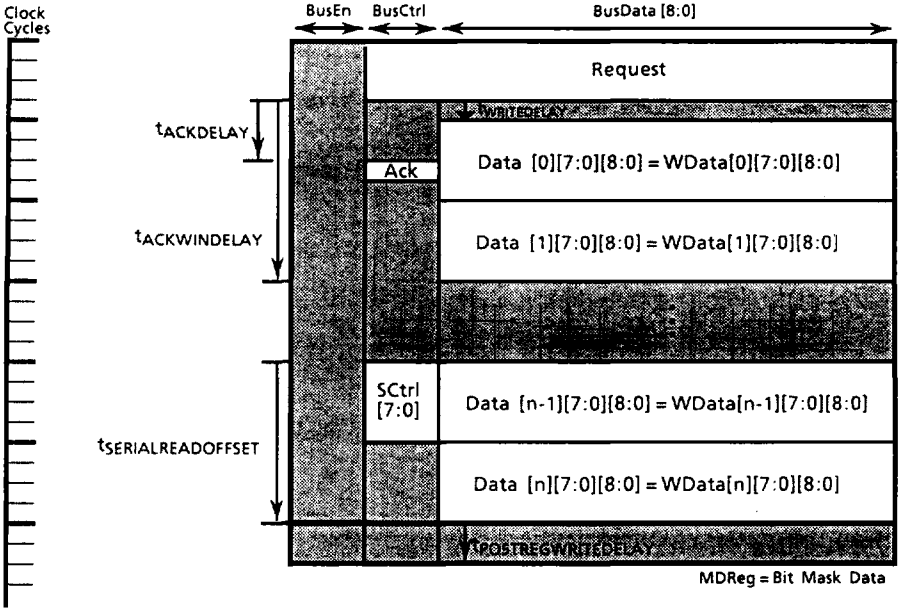


Figure 17. Data-per-bit (Dpb) Write Transactions

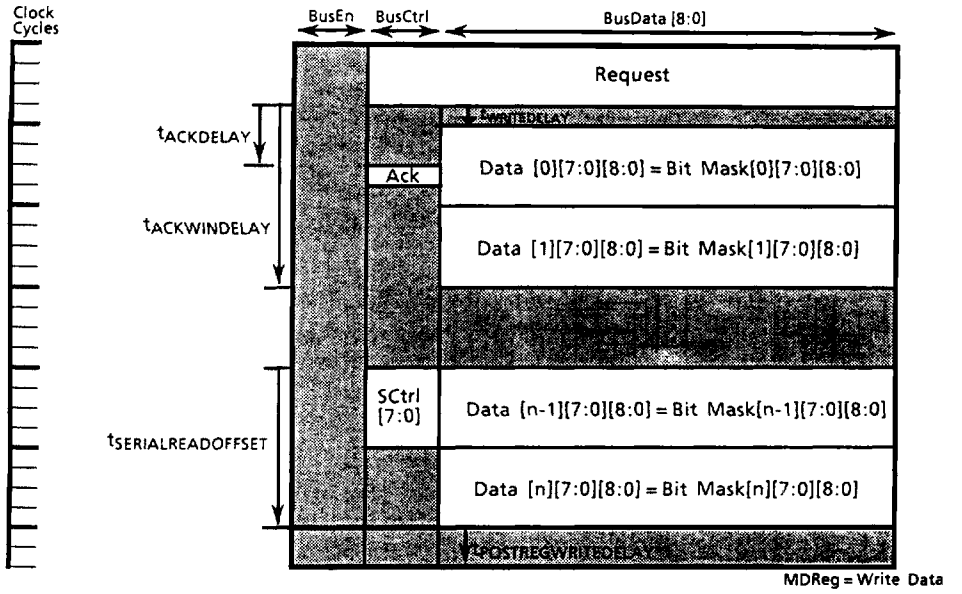


Figure 18. Mask-per-bit (Mpb) Write Transactions

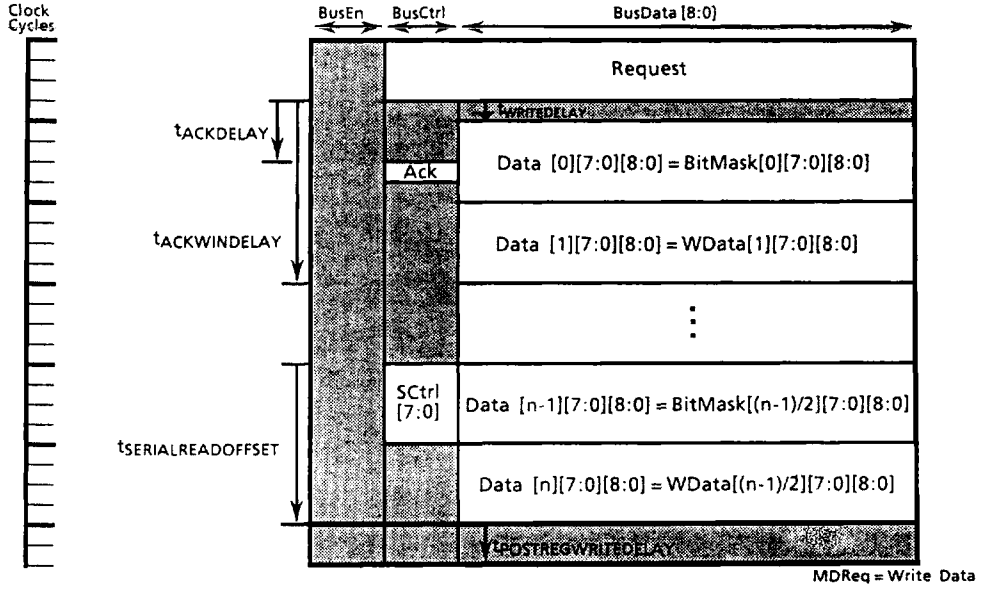


Figure 19. Both-per-bit (Bpb) Write Transactions

[9] Byte Masking (Wbns)

TC59R0808HK supports non-sequential byte masked writes that may include Dpb or Mpb bit masking as an option. Bpb masking is not supported in conjunction with byte masking. In this function, the first data packing, and every ninth thereafter, contain byte masking information that is applied to the eight data packets that follow. This means data packet 0, 9, 18, 27, etc. are not written to memory, but are instead used as byte masks for the eight octbytes of data that follow.

Figures 20 and 21 show the format of the non-sequential data write transaction with byte masking (Npb/Dpb) and (Mpb).

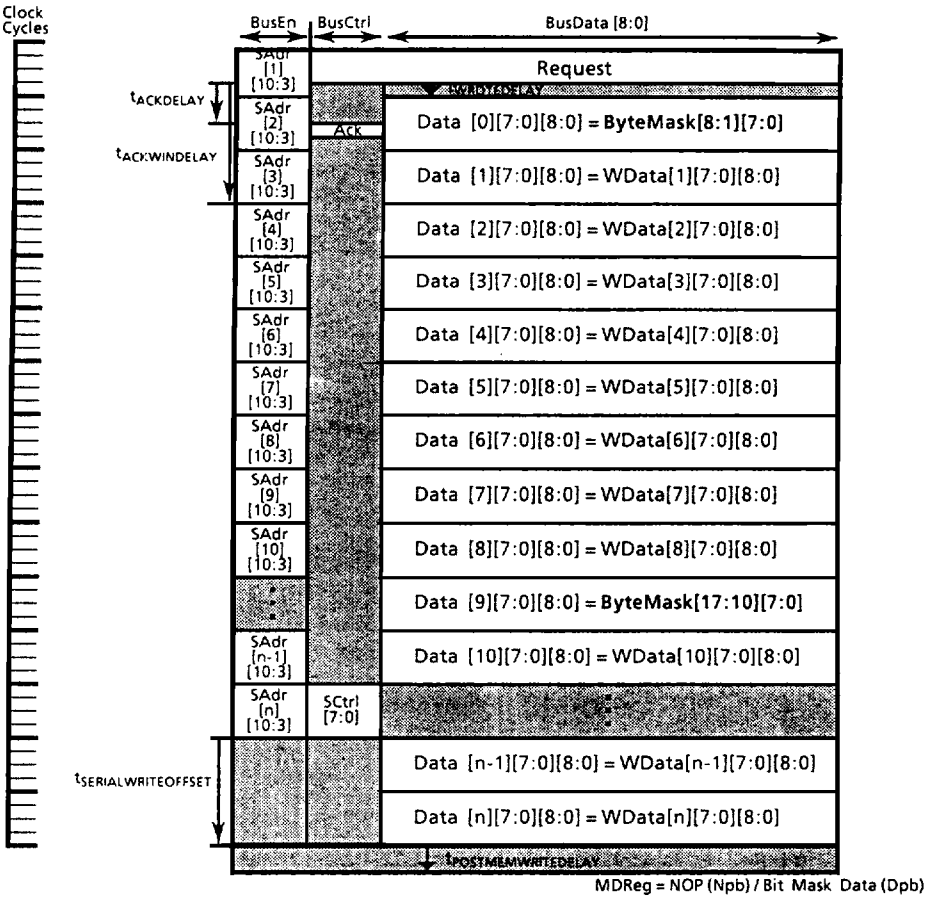


Figure 20. Non-sequential Data Write Transaction with Byte Masking (Npb/Dbp)

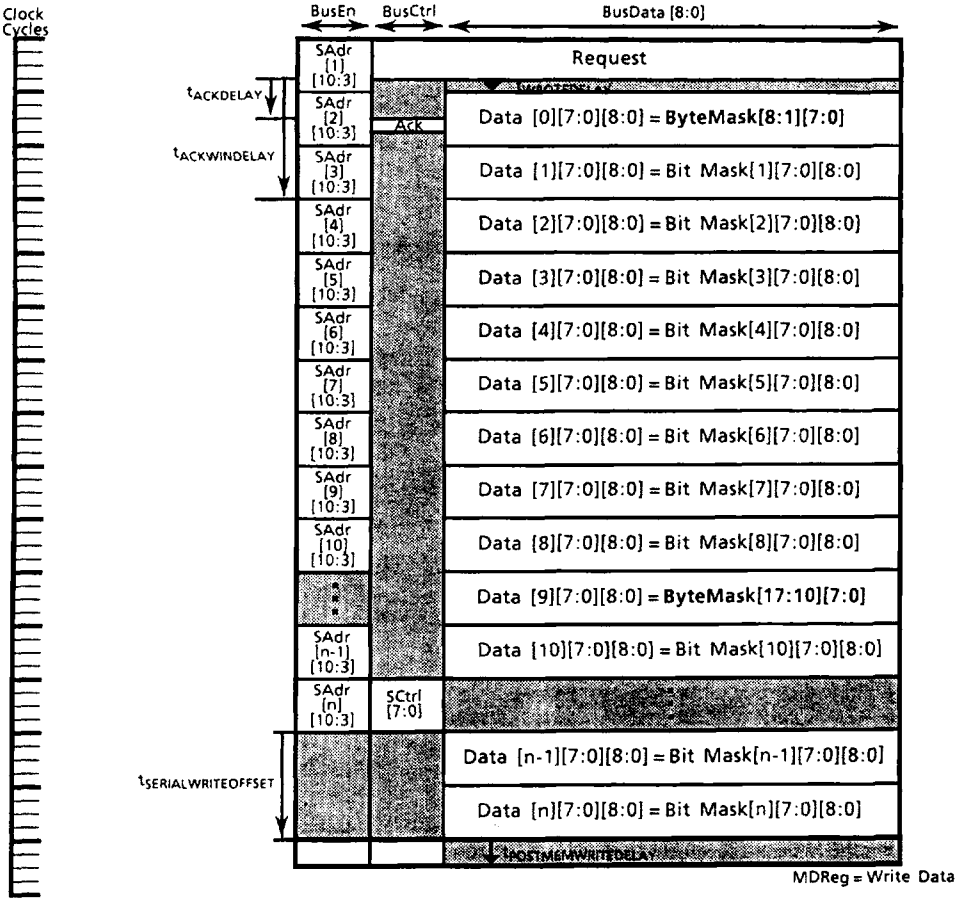


Figure 21. Non-sequential Data Write Transaction with Byte Masking (Mbp)

[10] The Cache Function

In the TC59R0808HK, the WL level selected by row access is maintained until another row address is selected. Therefore, the cell data in the last row address accessed is latched into the sense amp connected to BL, thereby operating as a cache for high-speed data transfer.

The row address used as the cache address is written to the Row register in the slave logic and is compared against the row address for the request packet sent from the master. If they match (the RDRAM sends an Okay Ack packet to the master in the case of a row hit), the memory cell is accessed. If the master selects a different row address (the RDRAM sends a Nack Ack packet to the master in the case of a row miss), the current WL is closed (row precharging) and the requested row address is accessed.

The TC59R0808HK has one bank X 8bits with 2048 column per row. The cache size is therefore 2kByte.

[11] Operation of Registers in Slave Logic

As shown in Figure 22, all registers have a standard group of 4, with register name [byte] [bit] format. Bytes are specified in the range [3 : 0], bits are specified in the range [8 : 0]. The bit wright within the bit field is indicated by arrows from the least significant bit (LSB) to the most significant bit (MSB). The master output "0" for the "reserved" bit in Figure 22 during write operations, while undefined data is output during read operations.

"0", "1": Reset value
"x": Not changed a at reset (or bit is retained)
"r": Read-only. Always the same value.

Each register is selected, as shown in Table 9, according to the value of AdrS [9 : 2] in the request packet.

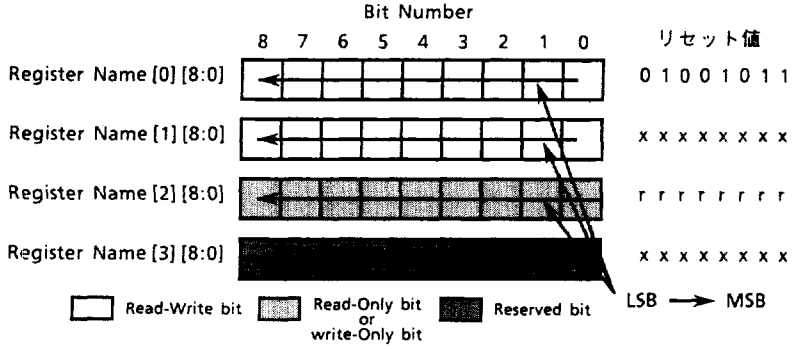


Figure 22. Register Format

Table 7. Register Types and Selection Addresses

Register Name	Adr S [9 : 2]	Comment
DeviceType [3 : 0] [8 : 0]	00000000	Device type register
DeviceId [3 : 0] [8 : 0]	00000001	Device ID register
Delay [3 : 0] [8 : 0]	00000010	Delay register
Mode[3 : 0] [8 : 0]	00000011	Mode register
RefRow [3 : 0] [8 : 0]	00000101	Refresh row register
RasInterval [3 : 0] [8 : 0]	00000110	RAS interval register
MidInterval [3 : 0] [8 : 0]	00000111	Minimum interval register
AddressSelect [3 : 0] [8 : 0]	00001000	Address select register
DeviceManufacture [3 : 0] [8 : 0]	00001001	Manufacturer setting register
Row [3 : 0] [8 : 0]	10000000	Row register

(1) Device Type Register (All Read-Only bits)

• Version . . . DeviceType [3] [7 : 4]
These bits show the RDRAM version.

• Type . . . DeviceType [3] [3 : 0]
These bits show the device type. "0 0 0 0" shows that the device is RDRAM.

• BankBits . . . DeviceType [1] [7 : 4]
These bits show the number of bank addresses in RDRAM memory cells. Because the TC59R0808HK has two banks, these bits are set to "0000" (0 bit).

• RowBits. . . DeviceType [1] [3 : 0]
These bits show the number of row address bits (number of rows) per RDRAM memory cell bank. Because the TC59R0808HK has 512 rows per bank, bits are set to "1000" (9 bits).

• ColumnBits . . . DeviceType [1] [7 : 4]
These bits specify the number of column address bits (including Adr [1 : 0]) in RDRAM memory cells. Because the TC59R0808HK has 2048 columns per row, bits are set to "1011" (11 bits). When accessing memory, you cannot exceed the last column address in the currently accessed row.

• Par . . . DeviceType [0] [2]
Indicates whether the RDRAM has a X9 structure. "1" indicates X9 structure; "0" indicated X8 structure.

	Bit Number 8 7 6 5 4 3 2 1 0	Reset value
DeviceType [0] [8:0]		- 1 0 1 1 - 0 - -
DeviceType [1] [8:0]		- 0 0 0 0 1 0 0 1
DeviceType [2] [8:0]		- - - - - - - - -
DeviceType [3] [8:0]		- 0 0 0 1 0 0 0 0

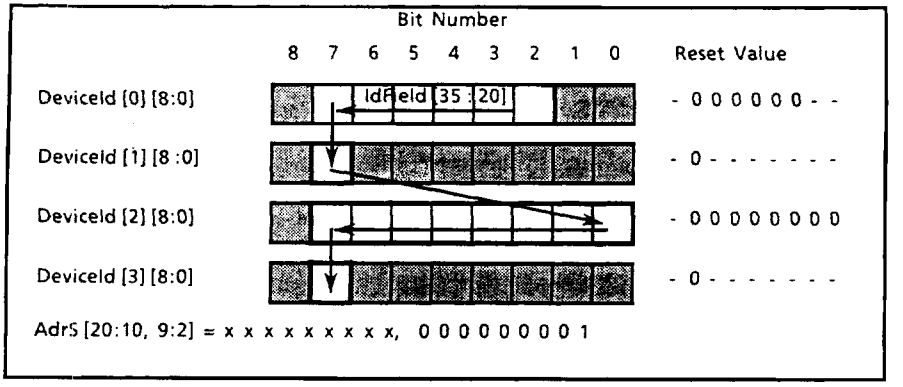
AdrS [20 : 10, 9 : 2] = x x x x x x x x x, 0 0 0 0 0 0 0 0

(2) Device ID Register (All Read-Write bit)

• Device ID

At initialization, the master sets a unique 17-bit DeviceID for each device. The DeviceID register is used for this purpose. The DeviceID data is used, as shown below, for comparison with the request packet address Adr [35 : 21] (swapped address). If they match, the IDMatch signal is issued. IDMatch is not generated by the broadcast register write instructions (Write RegB).

IdField [25 : 21]	. . .	DeviceId [0] [7 : 1]
IdField [26]	. . .	DeviceId [1] [7]
IdField [34 : 27]	. . .	DeviceId [2] [7 : 0]
IdField [35]	. . .	DeviceId [3] [7]



(3) Delay Register

The Delay Register is used to select the values of the Ack-Win, Read, Ack, Write delays, and to specify the number of the bits (Read-Only bit). (See Table 10)

Table 10. Delay Register Setting

	Register Used	Bits	Description
AckWinBits	Delay [0] [2 : 0]	3	Specifies the number of bits in AckWinDelay
ReadBits	Delay [1] [2 : 0]	2	Specifies the number of bits in AckWinDelay
AckBits	Delay [2] [2 : 0]	2	Specifies the number of bits in AckWinDelay
WriteBits	Delay [3 [2 : 0]	2	Specifies the number of bits in AckWinDelay
AckWinDelay	RefRow [0] [5 : 3]	3	Stipulates the delay of AckWindow from the end of a request packet. (See Table 9)
ReadDelay	RasInterval [1] [5 : 3]	5	Stipulates the delay between the end of a request packet and the start of a read data packet. (See Table 10)
AckDelay	MidInterval [2] [4 : 3]	2	Stipulates the delay between the end of a request packet and the start of an Ack packet. (See Table 11)
WriteDelay	Delay [3] [5 : 3]	5	Stipulates the delay between the end of a request packet and the start of a write data packet. (See Table 12)

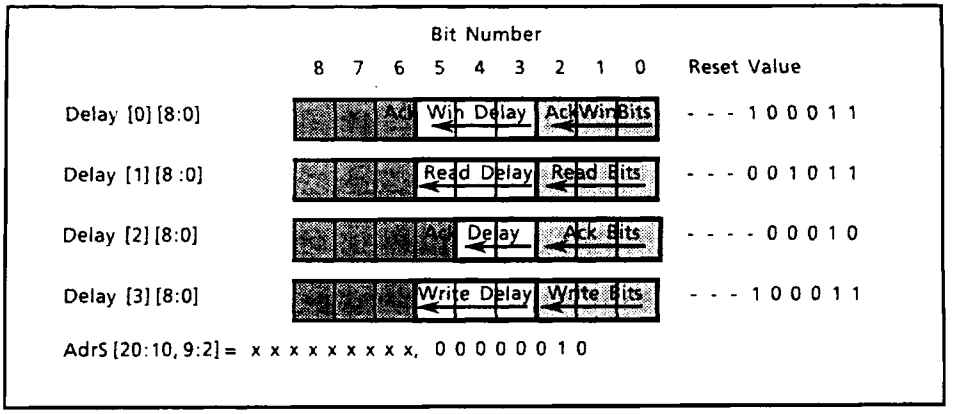


Table 11. AckWinDelay

Delay [0] [5 : 3]	AckWinDelay	Delay [0] [5 : 3]	AckWinDelay
101	5 t_{CYCLE}	001	9 t_{CYCLE}
110	6 t_{CYCLE}	010	10 t_{CYCLE}
111	7 t_{CYCLE}	011	11 t_{CYCLE}
000	8 t_{CYCLE}	100	12 t_{CYCLE}

Table 12. AckWinDelay

Delay [0] [5 : 3]	AckWinDelay	Delay [0] [5 : 3]	AckWinDelay
111	7 t_{CYCLE}	011	11 t_{CYCLE}
000	8 t_{CYCLE}	100	12 t_{CYCLE}
001	9 t_{CYCLE}	101	13 t_{CYCLE}
010	10 t_{CYCLE}	110	14 t_{CYCLE}

Table 13. AckDelay

Delay [0] [5 : 3]	AckWinDelay	Delay [0] [5 : 3]	AckWinDelay
00	4 t_{CYCLE}	10	6 t_{CYCLE}
01	5 t_{CYCLE}	11	3 t_{CYCLE}

Table 14. WriteDelay

Delay [0] [5 : 3]	AckWinDelay	Delay [0] [5 : 3]	AckWinDelay
001	1 t_{CYCLE}	101	5 t_{CYCLE}
010	2 t_{CYCLE}	110	6 t_{CYCLE}
011	3 t_{CYCLE}	111	7 t_{CYCLE}
100	4 t_{CYCLE}	000	8 t_{CYCLE}

(4) Mode Register

• CE . . . Mode [0] [7] (1 bit)
This bit selects automatic thermal compensation for the output driver drive current. When set to "1", fluctuations in the output current level due to temperature change are automatically corrected.

• X2 . . . Mode [0] [6] (1 bit)
This bit selects whether register X1 or X2 is used for the current control counter. "0" selects register X1: "1" selects register X2.

• C [5 : 0]. . . Mode [3 : 1] [7 : 6] (3 X 2 = bits)
This bit field sets the device output current drive level in the range 0 to 63. The RDRAM output driver uses the open-drain system and consists of six transistors with different current drive capacities. C [5 : 0] specifies the combination in which these six drivers are used. Each bit sets a transistor ON when set to "0" or OFF when set to "1".

• DE . . . Mode [0] [1] (1 bit)
This sets the RDRAM operation mode to Power-Down. When DE = "0", operations other than broadcast register write cannot be executed. Also, when DE = "0", SOut is not output. See the section on initialization for more details.

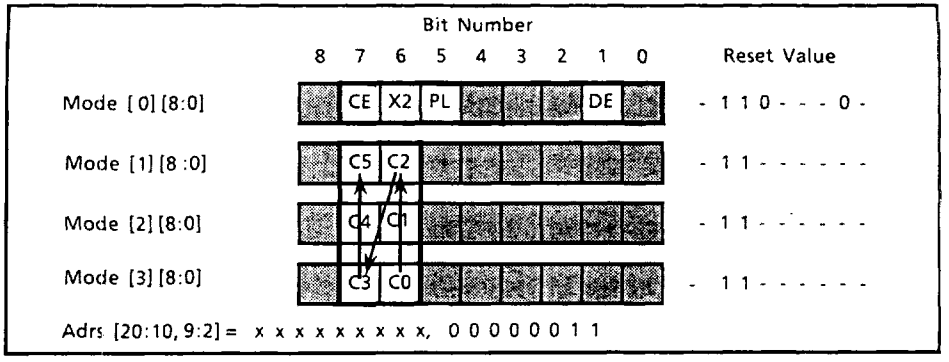
• RE . . . Mode [0] [0] (1 bit)
This bit sets the RDRAM operation mode Power-Down. Setting this bit to "1" selects PowerDown mode, enabling considerable energy savings.

• AS . . . Mode [0] [2] (1 bit)
This bit is used for testing.

• SK . . . Mode [0] [3] (1 bit)
This bit is used for testing.

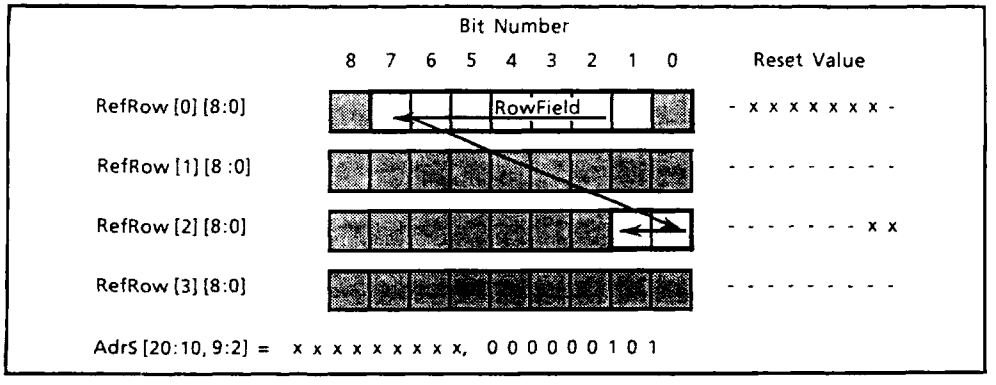
• SV . . . Mode [0] [4] (1 bit)
This bit is used for testing.

• PL . . . Mode [0] [5] (1 bit)
This bit is used to select the PowerDown wake up latency.



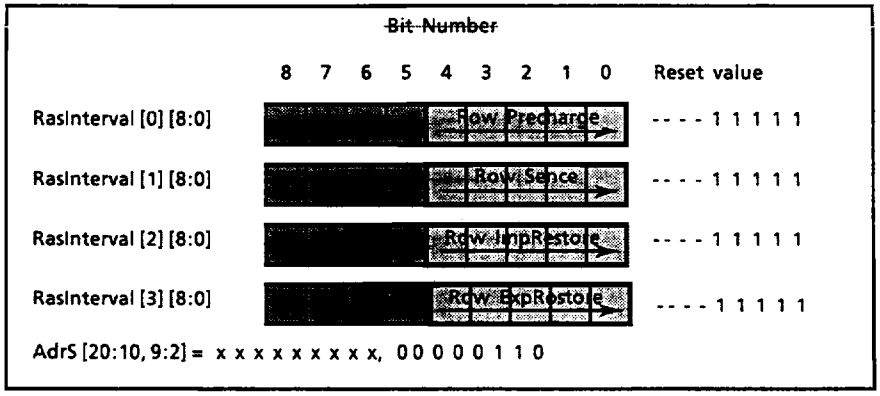
(5) RefRow Register (Read-Write bit)
The refRow register is used to store the bank address and row address for refreshing.

• RowField . . . RefRow [0] [7 : 1]
RefRow [1 : 0] (9 bit))
Specifies the currently refreshed bank.



(6) RasInterval Register (All write only bit)
When RDRAM access is prevented by a row-miss or self-refresh (when the Ack packet is Nack), the master has to wait a set interval until the next access. The RasInterval register determines the length that the master waits. The RasInterval register includes the RowPrecharge, RowSense, RowImpRestore and RowExpRestore resgisters. As shown in the Figure 16, the total of these registers constitutes the row cycle time.

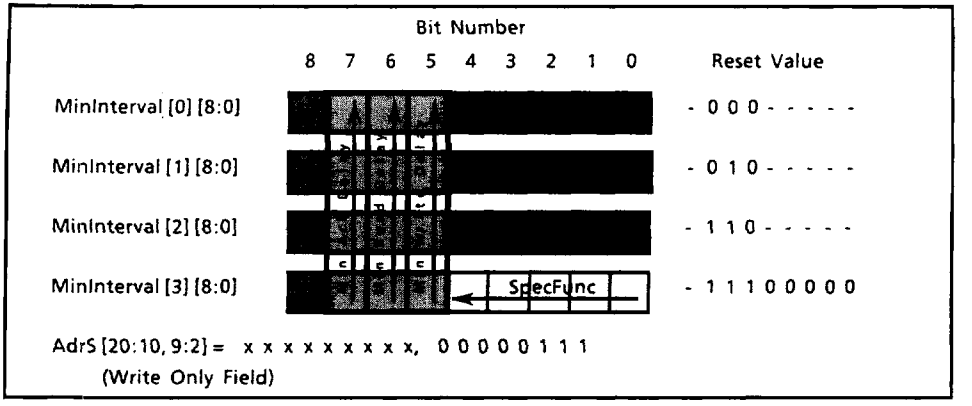
• RowPrecharge . . . RasInterval [0] [0 : 4] (5 bits)
Specifies the RAS access precharge interval in the range 0 to 31 t_{CYCLE}.
• RowSense . . . RasInterval [1] [0 : 4] (5 bits)
Specifies the RAS access interval in the range 0 to 31 t_{CYCLE}.
• RowImpRestore . . . RasInterval [2] [0 : 4] (5 bits)
Specifies the RAS access implicit in the range 0 to 31 t_{CYCLE}.
• RowExpRestore . . . RasInterval [3] [0 : 4] (5 bits)
Specifies the RAS access explicit in the range 0 to 31 t_{CYCLE}.



(7) MinInterval Register (All Read-Only bits)
This register specifies, in tCYCLE units, the minimum values for the three delays (Ack, Read and Write Delay) in the Delay register.

Table 15. MinInterval Register

	Register	Bits	Description
MinAckDelay	MinInterval [0 : 3] [5]	4	Stipulates the minimum AckDelay Value in t_{CYCLE} units
MinReadDelay	MinInterval [0 : 3] [4]	4	Stipulates the minimum ReadDelay Value in t_{CYCLE} units
MinWriteDelay	MinInterval [0 : 3] [3]	4	Stipulates the minimum WriteDelay Value in t_{CYCLE} units

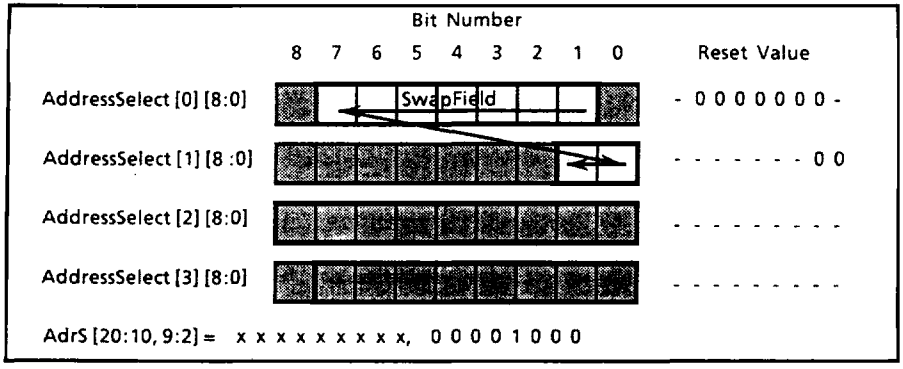


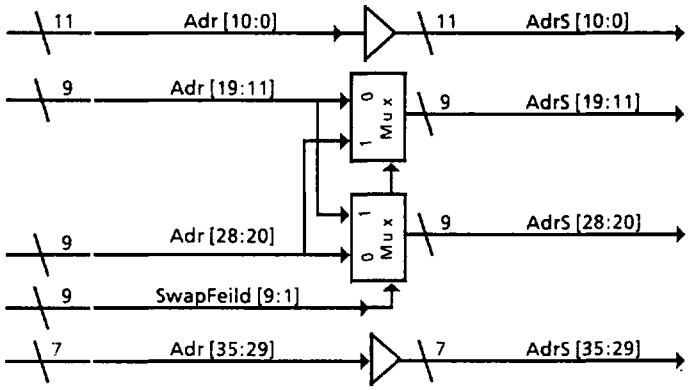
SpecFumc [4 : 0] is a write-only field which affects control bit which are otherwise not directly accessible.

Table 16. WriteDelay Encoding

SpecFumc [4 : 0]	Description
00000	NOP
xxxx1	SetRR - RefreshRequest bit
x01xx	SetPD - PD bit

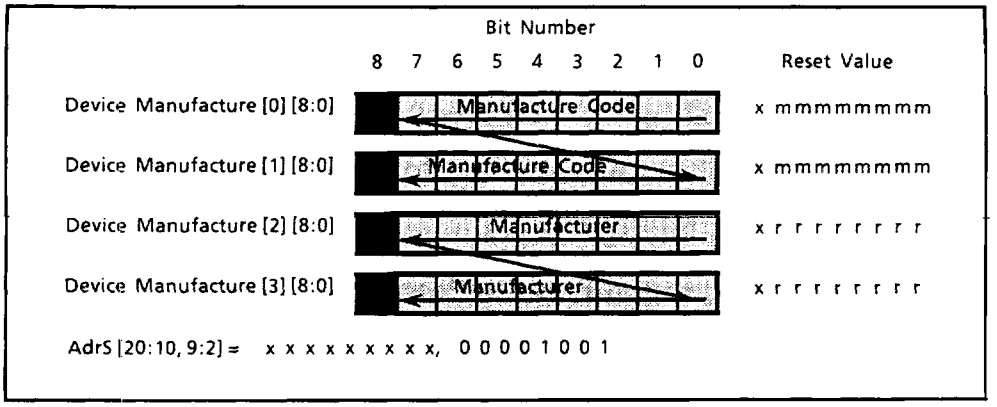
(8) AddressSelect Register (Read-Write bit)
• SwapField . . . AddressSelect [0] [7 : 0] and [1] [1 : 0] (9 bits)
For address mapping, RDRAM allows Adr [28 : 20] and [19 : 11] to be swapped in 1-bit units. Address swapping is executed as follows when each bit in the Address Select register is "1".
Adr [19 : 11] - >
When all bits in the AddressSelect register are "0", no swapping is executed.
Adr [19 : 11] - >
Address mapping thereby enables greater hit rates for the rates for the row sense amp caches of each bank. See the section on address mapping details.





(9) DeviceManufacture Register (Read-Write bits)
This register stipulates manufacturing specifications such as the manufacturer and revision No.

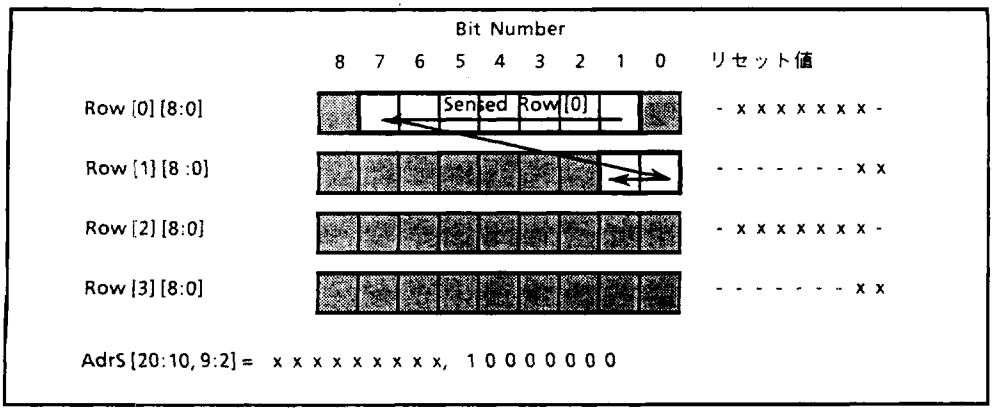
- Manufacture: This field specifies the device manufacturer.
- Manufacture Code: Manufacturer's code



(10) DeviceManufacture Register (Read-Only bit)

- Sensed Row [0] . . . Row [0] [7 : 1] and [1] [1 : 0] (9 bits)

These bits show the address of the previously accessed row in bank "0". That is, they show the address of the row's sense amp cache. When bank "0" (AdrS [20] = "0") is accessed, the content of this register is compared against that of AdeS [19 : 11]. If they match, the requested column address (Adr [10 : 3]) is accessed. If they do not match, (Row miss), the cell array is refreshed by the RDRAM's internal control logic, and the requested row then accessed.



[12] RDRAM Function

(1) Operation Mode

TCR0808HK have four operation modes; reset, active, standby, and PowerDown. Active mode is the default, permitting a device to frame the packets of a transaction.In reset mode, RDRAM places its control registers into a known state. In standby mode, the RDRAM dissipates less power than in active mode. In this mode, the RDRAM watches the BusEnable pin but does not sample the BusCtrl or BusData [8 : 0 Pins]. PowerDown mode saves more power, shutting down more of the device than in standby mode. This increase in the RDRAM latency, because the clock generator is one of the functions which is shut down. Figure 23 shows the block diagram of the Frame state machine. A serial packet SMode [1 : 0] is received in every clock cycle. The SMode [1 : 0] = 11 combination increments the Count11 [7 : 0] counter, and clears the Count00 [3 : 0] counter. If the Count11 [7 : 0] counter is incremented more than 255 times, it is left at its maximum value of 255. In a clears the Count11 [7 : 0] counter. If the Count00 [3 : 0] counter is incremented more than 15 times, it is left at its maximum value of 15.

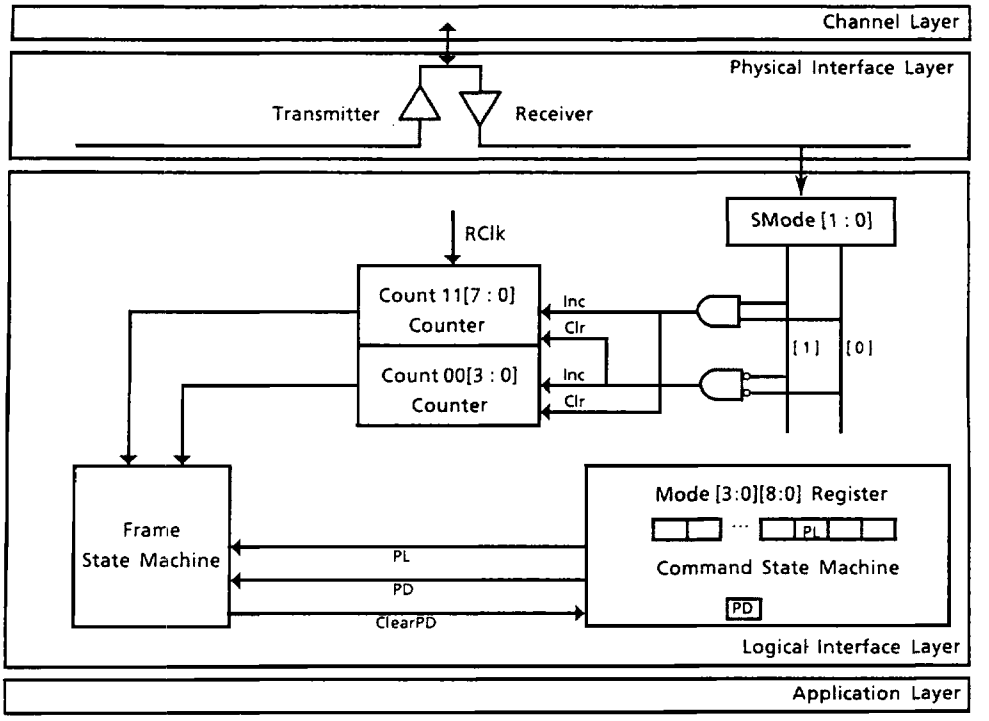


Figure 23. Frame State Machine - Block Diagram

Figure 24 shows the Frame State Machine - State Diagram. The RDRAM will enter reset mode when power is initially applied. In reset state, the RDRAM will be in the reset operating mode, in which all control registers assume a known state. If the power has been applied, the RDRAM will pass through active state and settle in standby state, and remain there until serial mode packets are received from the initiating RDRAM.

After power on, TC59R0808HK will re-enter reset state when the value of the Count11 [7 : 0] counter is greater than or equal to $t_{MODEAR, MIN}$. This will happen when an SMode [1 : 0] bit of 00 is received, causing the Count11 [7 : 0] counter to clear. TC59R0808HK will enter Standby state when the value of the Count00 [3 : 0] counter is greater than or equal to $t_{MODEAR, MAX}$. The device will leave standby state when the value of the Count11 [7 : 0] counter is greater than equal to $t_{MODES, MIN}$.

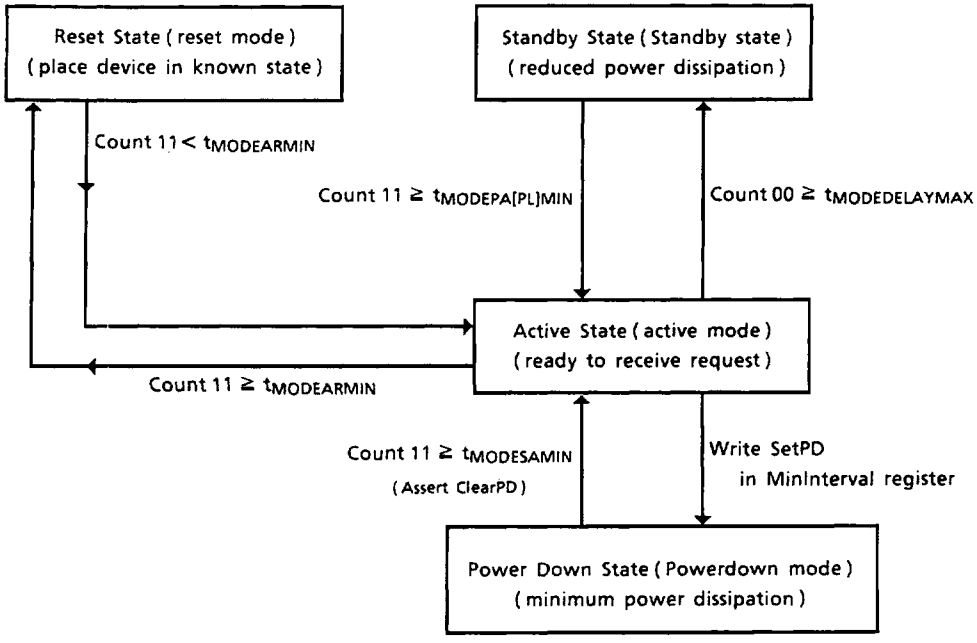


Figure 24. Frame State Machine - State Diagram

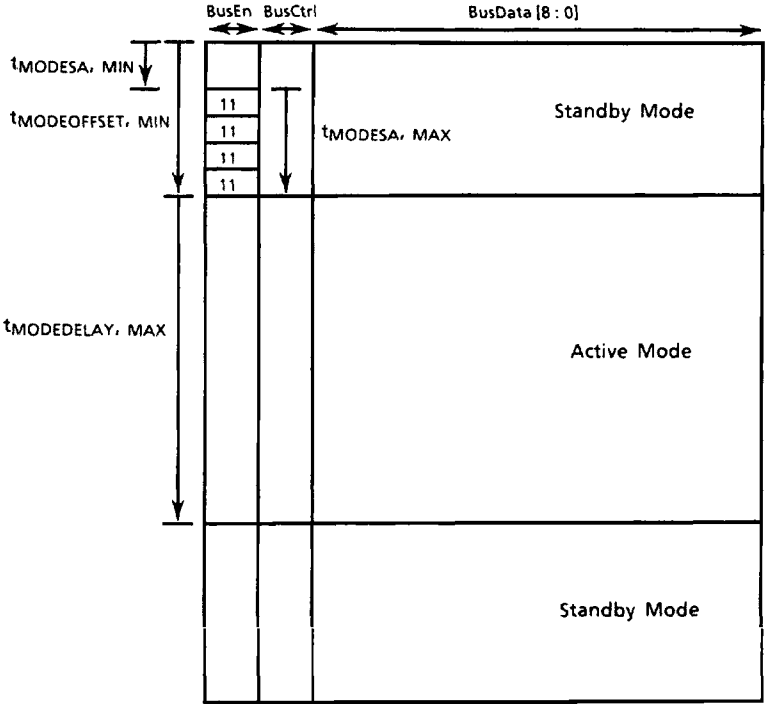
TC59R0808HK will enter PowerDown mode when the PD bit is set. The RDRAM will leave PowerDown state when the value of the Count11 [7 : 0] count is greater than or equal to $t_{MODEPA\ [PL],\ MIN}$. PL is a bit in the mode.

Table 17 shows the Responding Device Parameters for Operating Mode Transitions.

Table 17. Responding Device Parameters for Operating Mode Transitions

	Min (clock cycles)	Max (clock cycles)	Description
t_{MODESA}	1	4	Number of SMode packets to cause a transition from StandbyMode to ActiveMode
Rsrv	5	9	Reserved for future functionality
Undef	10	15	Undefined
t_{MODEPA} [0]	16	20	Number of SMode packets to cause a transition from PowerdownMode[1] to ActiveMode
Rsrv	21	189	Reserved for future functionality
Undef	190	207	Undefined
t_{MODEPA} [1]	208	224	Number of SMode packets to cause a transition from PowerdownMode[1] to ActiveMode
Rsrv	225	253	Reserved for future functionality
Undef	254	271	Undefined
t_{MODEAR}	272	–	Number of SMode packets to cause a transition from ActiveMode to ActiveMode
$t_{MODEOFFSET}$	4	–	Offset from beginning of SMode packet to request packet for standby to active transition
$t_{MODEDELAY}$	–	10	Offset from end of SMode packet to request packet for standby to active transition

Figure 25 shows the transitions between active and standby modes. A SMode [1 : 0] bits are shown as "11" in BusEn column. TC59R0808HK begins the transition to active modes. A SMode [1 : 0] bits are shown as "11" in BusEn column. It reaches active mode after $t_{MODEOFFSET, MIN}$. after the start of the first serial mode packet. If the serial mode packet to active mode transition are not followed by $t_{MODEOFFSET, MAX}$. after the last serial mode packet, TC59R0808HK will return to standby mode.



When TC59R0808HK is given a consecutive sequence of $t_{MODEDELAY, MAX}$ serial mode packets with a value of 11, reset mode is entered. The RDRAM remains in reset mode for as long as serial mode packets with a 11 value are received. When one or more serial mode packets with a value of 00 are seen, TC59R0808HK enters the active mode state.

In order to keep the RDRAMs in active mode during this synchronization, it is necessary to provide a burst of serial mode packets every $t_{MODEDELAY, MAX}$. If the RDRAM is not kept in active mode during synchronization cycles requires $t_{LOCK, STANDBY, MIN}$.

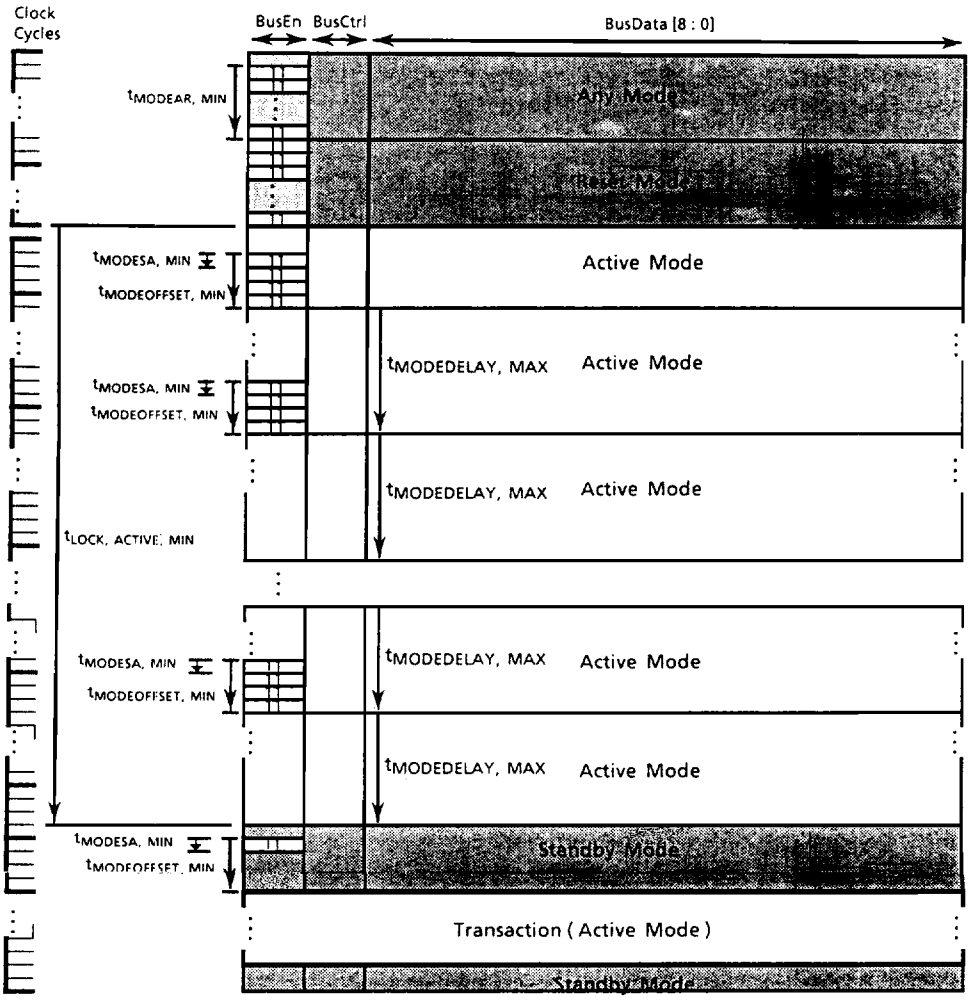


Figure 26. Reset Mode Transition

Powerdown mode is controlled by the PD bit. This bit is not directly accessible in the register space. Instead, the "SetPD" is written to the SpecFunc field in the MinInterval register. Figure 27 shows the active mode to PowerDown Mode transition. When the PD bit is done, the RDRAM performs the following operations.

- Restore and precharge the RowSenseAmp Latch for both banks
- Disable the clock generator
- Disable all DC current sources except for a special BusEnable receiver

When these operations have been completed, the RDRAM is in the Powerdown Mode.
Figure 28 shows the PowerDown Mode to Active Mode transitions.

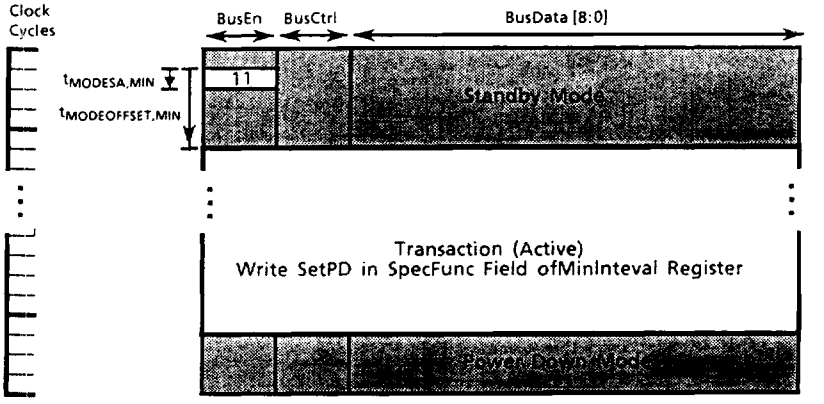


Figure 27. Active Mode to Power Down Mode Transition

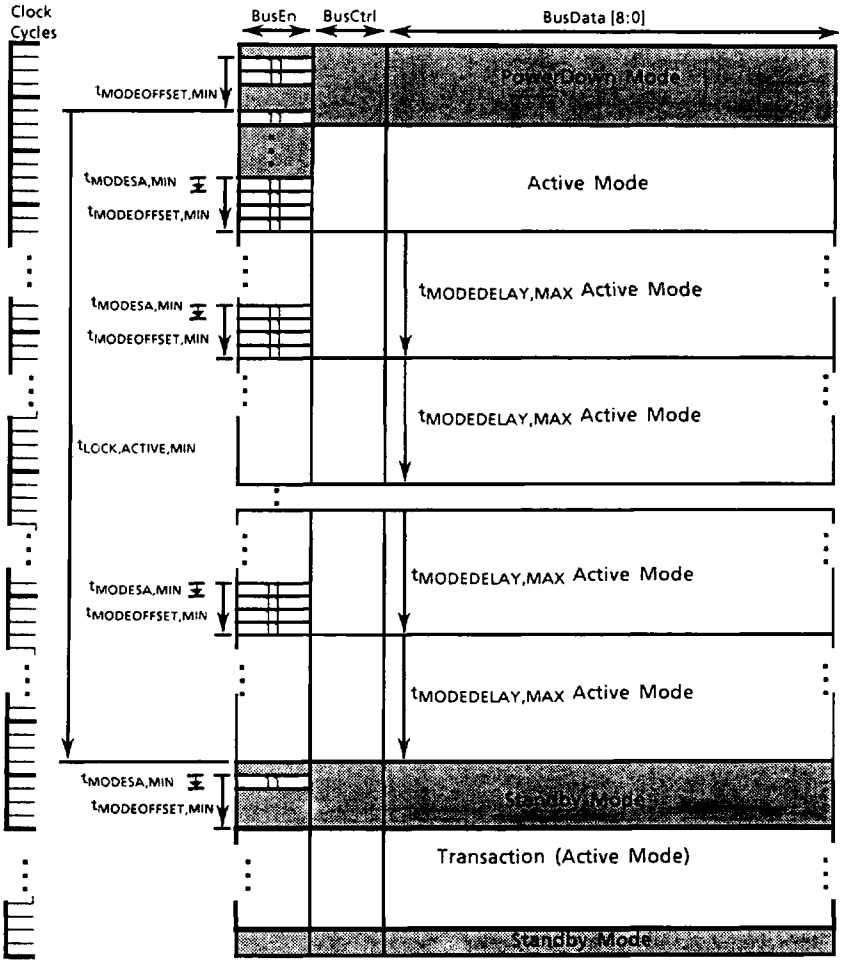


Figure 28. PowerDown Mode to Active Mode Transition

(2) Address Mapping

Address mapping is a function for improving the hit rate for the sense amp cache in the RDRAM memory cells. In concrete terms address AdrS [35 : 3] for the RDRAM memory space is formed by changing the combination of RDRAM of the request packet address Adr [35 : 3] according to the setting of AddressSelect [0] [7 : 0] See Figure 30). AdrS [35 : 3] refers to the following addresses in the RDRAM memory cells.

C_M [7 : 0] (AdrS [10 : 3]): Column address (in QB)
R_M [8 : 0] (AdrS [19 : 11]): Row address
D_M [15 : 0] (AdrS [35 : 29]): Device ID address (DeviceId)

Of the Adr [35 : 3], only Adr [28 : 20] and Adr [19 : 11] are swapped by address mapping. Each address is swapped for AdrS [28 : 20] and AdrS [19 : 11] according to the 9-bit data of the AddressSelect register [0] [7 : 0]. In Figure 29, AddressSelect [0] [7 : 1] and [1] [1 : 0] is "111111111", and all Adr [28 : 20] and Adr [19 : 11] bits are therefore swapped. Address swapping is valuable when the master accesses contiguous address space. That is, when Adr [35 : 3] is accessed from ALSB 9Adr [3]) to the MSB (Adr [35]). When the master performs such access without address mapping, we get the following:

Adr [28 : 20] – AdrS [28 : 20]
Adr [19 : 11] – AdrS [19 : 11]

In this case, each time of the value of D_R [7 : 0] in the request packet changes, the row address R_M [8 : 0] also changes, resulting in a cache miss. Even if several RDRAMs are connected to increase the number of cache lines, there will be no improvement in the cache hit rate. In contrast, if address mapping is used, we get:

Adr [28 : 20] – AdrS [19 : 11]
Adr [19 : 11] – AdrS [28 : 20]

In this case, even if the value of request address D_R [8 : 0] from the master changes, R_M [8 : 0] remains constant and the device ID address DM [8 :] changes. This enables cache line of different devices to be accessed continuously, improving the cache hit rate.

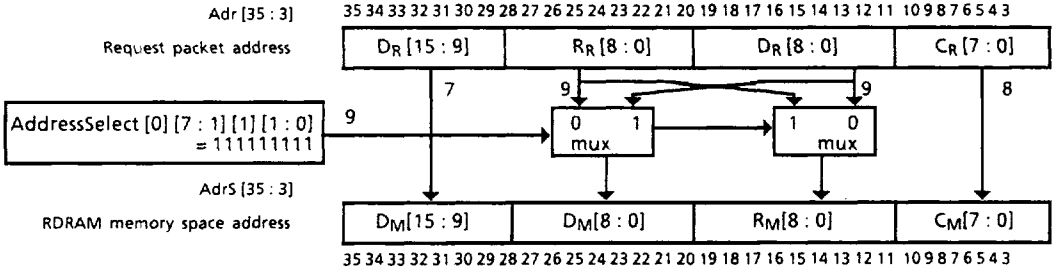


Figure 29. Address Mapping (System with 128 RDRAMs)

In Figure 29, AddressSelect [0] [7 : 1] [1] [1 : 0] = "111111111". There, we are assuming address mapping in a 256 RDRAM (256 bank) system (currently, address mapping is only available for a maximum of 256 DRAMs). In contrast, Figure 30 shows address mapping for a more realistic RDRAM system. From the top, we have 8, 16, 24 and 32-RDRAM systems. If the number of DRAMs is expressed as 2N, N bits of the 9 bits of AddressSelect [0] [7 : 1] [1] [1 : 0] are swapped. In a system such as the 24 RDRAM system, in which the number of RDRAMs is expressed as $P \bullet 2^{Q}$ (where P is an odd number), Q bits are swapped, and the system consists of P RDRAM blocks (2Q). This is to prevent the creation of blanks in the address space as a result of address mapping. In 24 RDRAM system in Figure 30, N = 3 and N = 3 and P = 3 and each block is selected by D [5 : 4].

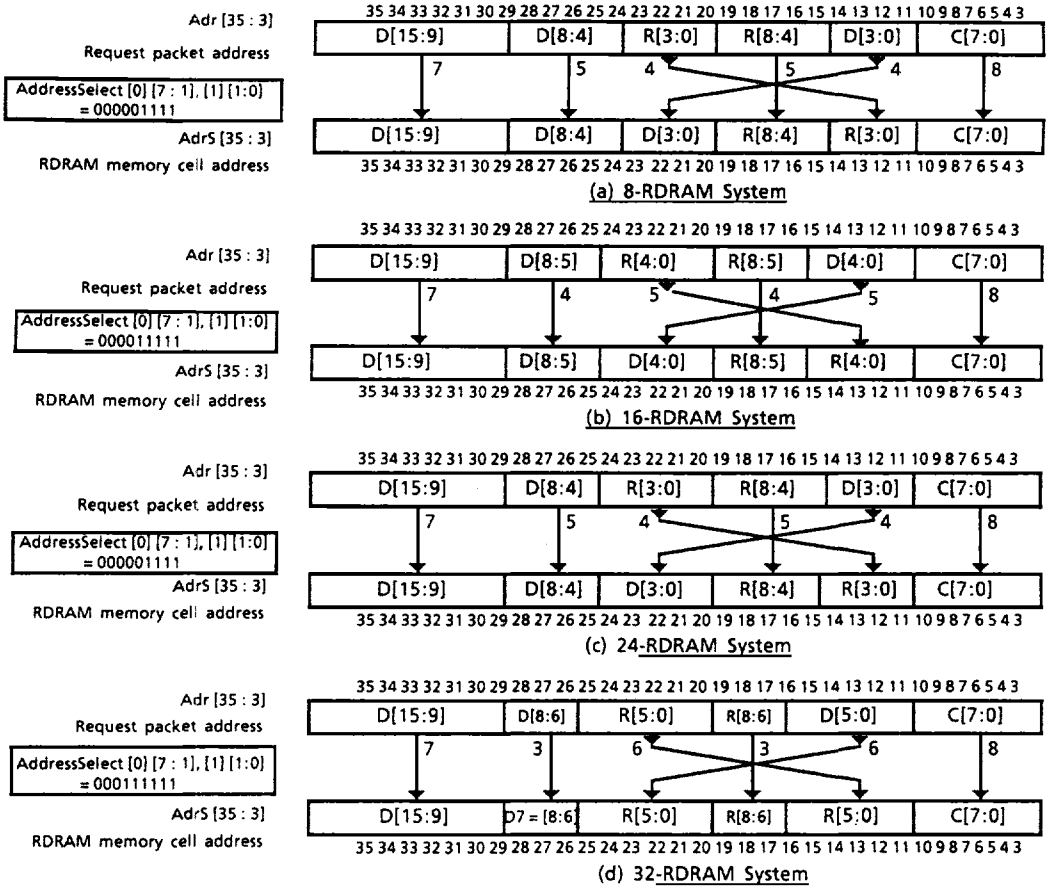


Figure 30. Address Mapping (8, 16, 24 and 32 Systems)

As an example, let's take a system consisting of 8 RDRAMs. If we say that each RDRAM's cache line address is R [3 : 0] = "0000", we can use address mapping to contiguously access the 16 cache lines of the 8 RDRAMs, as shown in Figure 31.

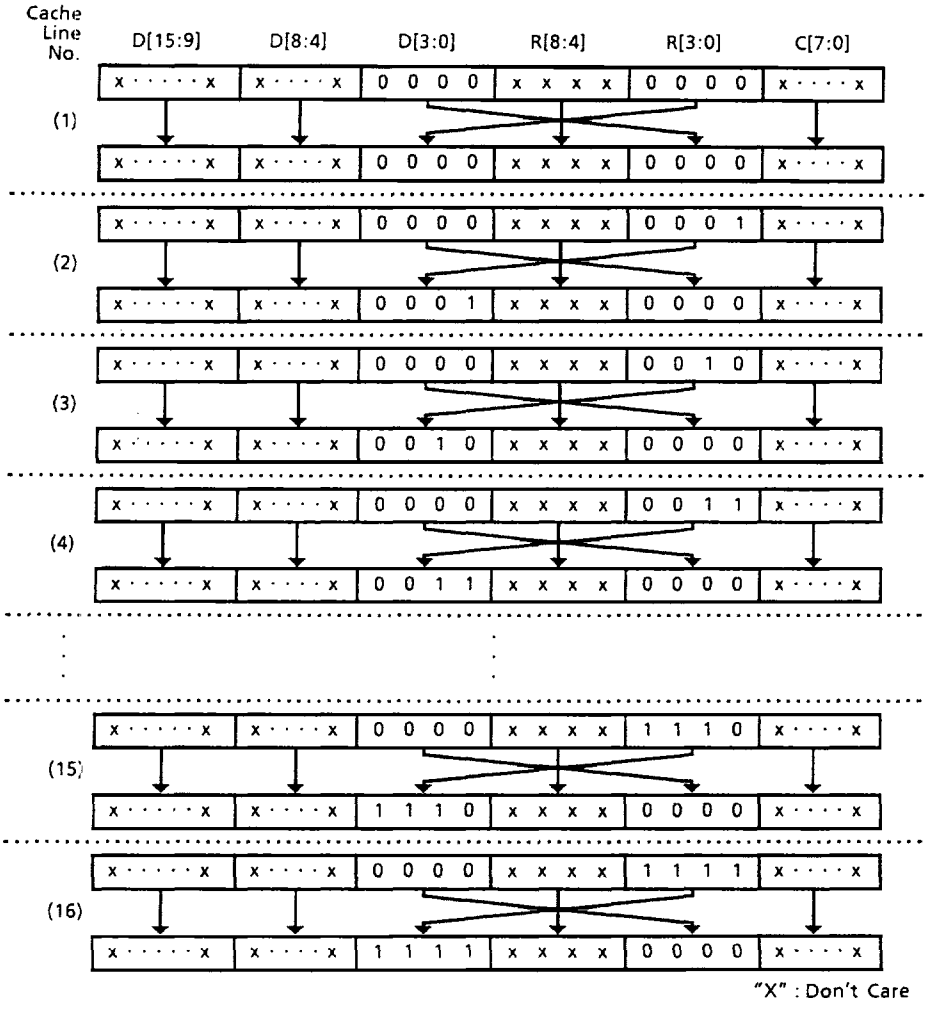


Figure 31. Address Swapping Using Address Mapping (RDRAM System)

(3) RDRAM Initialization

RDRAM must be initialized be the master before starting normal operations. The main function of initialization is the allocation of device IDs for each of the device connected to the Rambus system. The Device allows the master to select any device, without the need to use an external control unit.

Figure 32 shows a Rambus system with a single master, a single primary channel. SOut of the configuration master connects to SIn of the first device and so on through each bus device in daisy chain fashion. SOut of the last device connects to SIn of the configuration master.

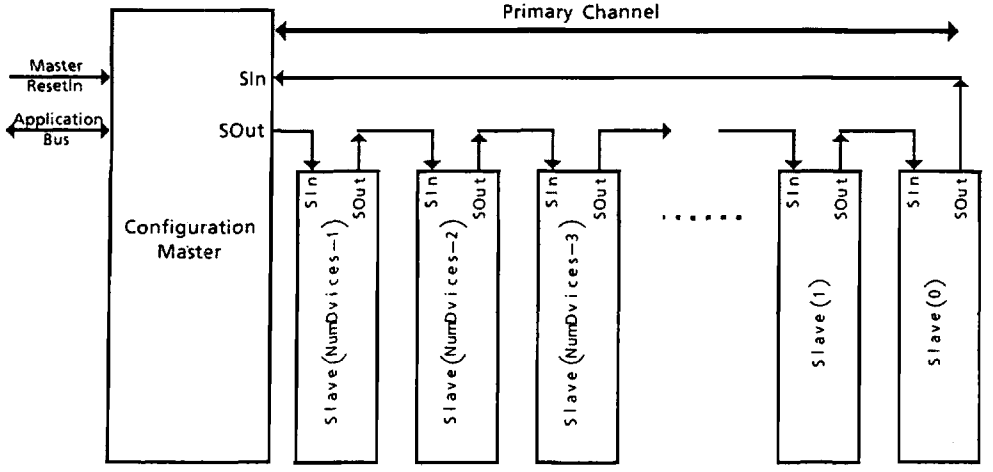


Figure 32. Shows a Rambus System with a Single Configuration Wafer Device a Single Primary Channel

Figure 33 shows the RDRAM Slave Device Logic. DeviceEnable is a bit Mode Register. The reset pulse on the BusEnable pin sets-all control registers to default values. Most commands are gated by IdMatch, which is formed by comparing Adr [35 : 18] in the request packet with the address in the DeviceId Register. In addition, Device Enable gates the WwwwBbbAaa', RrrAaa', Wreg', and Rreg' commands. At Initialization time when DeviceEnable = 0 most commands are disable. What remains is the Wreg' path dated by SIn and IdMatch. This path permits the assignment of unique DeviceID Values. The broadcast write command, WRregB', which is always enabled.

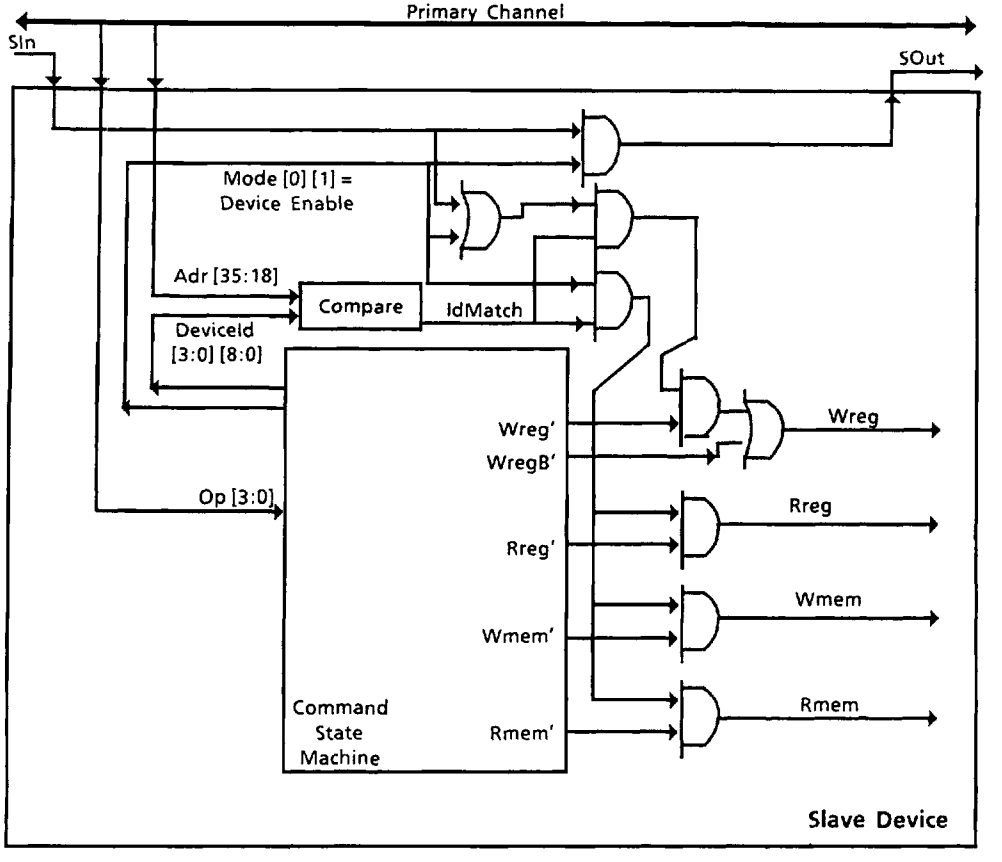


Figure 33. RDRAM Slave Device Logic

(4) I_{OL} Calibration

The following formula stands for V_{OL} and V_{OH}.

$V_{OH} = V_{TERM} - I_{OH} * R_O$

$V_{OL} = V_{TERM} - I_{OL} * R_O$

Where R_O is the resistance of the channel termination register which matches the effective impedance of the channel. The V_{OH} voltage level is essentially equivalent to the Vterm voltage because of the small value of the I_{OH} output current. The V_{OL} level is a function of Vterm, I_{OL} and R_O. The CE bit of the Mode Register is set to a one. I_{OL} is programmable over the range from zero to I_{OL}, max according to the following formula.

$I_{OL} = (I_{OL, MAX} * f1 * f2 * f3 * f4) + (\Delta I_{OL, MIN}, \Delta I_{OL, MAX})$

$f1 = (63 - C [5 : 0]) / 63$

$f2 = (1 + X2)$

$f3 = t_{CYCLE, MIN} / t_{CYCLE}$

$f4 = V_{REF} / V_{REF, MAX}$

Where C [5 : 0] is a unsigned, 6bit, binary number in the Mode Register, X2 is a 1bit field in the Mode Register. The F1 factor is adjusted by placing the appropriate 6 bit value into the C [5 : 0] field. The resulting Iol will then generate a V_{OL} that is lower than the V_{IL}, max by the appropriate margin.

The f2 factor is normally one (the X2 field is zero). However, if the f3 and f4 factors limit the upper programmable limit of I_{OL}, then X2 may be set to one.

Outline Drawings **Unit in mm**

(SHP36-P-1125)