SM5L1/5L2/5L3

4-Bit Single-Chip Microcomputer (LCD Driver)

DESCRIPTION

The SM5L1/5L2/5L3 is CMOS 4-bit single-chip microcomputers operated in single 1.5 V power supply. This microcomputer integrates 4-bit parallel processing function, ROM, RAM, display RAM, 15-stage divider, 2-kind of interrupt and 4-level of subroutine stack. With a built-in LCD drive circuit for maximum of 84/136/168/ (SM5L1/5L2/5L3) elements, a 2-mode standby function, and a melody generator circuit in a single chip, the SM5L1/5L2/5L3 permits the design of system configuration with a minimum of peripheral components. It can be used in a variety of products from handheld equipment to electrical appliances, such as audio timers, and also achieves low power consumption.

FEATURES

- ROM capacity : 2 048 x 8 bits (SM5L1)
  3 072 x 8 bits (SM5L2)
  4 096 x 8 bits (SM5L3)
- RAM capacity :
  69 x 4 bits (including 21 x 4 bits display RAM) (SM5L1)
  130 x 4 bits (including 34 x 4 bits display RAM) (SM5L2)
  170 x 4 bits (including 42 x 4 bits display RAM) (SM5L3)
- Instruction sets : 51
- Subroutine nesting : 4 levels
- I/O port :

Input	1
Output	5
Input/output	8

- Interrupts :

Internal interrupt	x 1 (INTA)
External interrupt	x 1 (divider overflow)

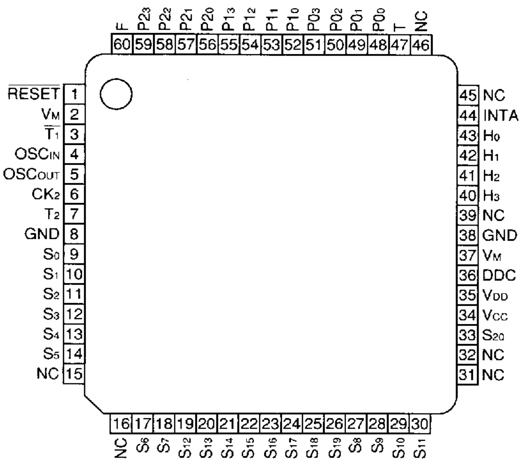
- Built-in main clock oscillator for system clock
- Signal generation for real time clock
- Built-in 15 stages divider for real time clock
- Built-in LCD driver :
  84 segments (SM5L1) / 136 segments (SM5L2) / 168 segments (SM5L3), 1/2 bias, 1/4 duty cycle
- Built-in melody generator circuit :
  Melody ROM
  160 steps (SM5L1), 256 steps (SM5L2/5L3)
  Generating time (at 32.768 kHz)
  20 s (MAX.) (SM5L1)
  32 s (MAX.) (SM5L2/5L3)
- Instruction cycle time : 61 μs (TYP., at 32.768 kHz)
- Standby function
- Supply voltage :
  1.5 V ± 10% (SM5L1)
  1.5 V ± 20% (SM5L2/5L3)
- Packages :
  60-pin QFP (QFP060-P-1414) (SM5L1)
  72-pin QFP (QFP072-P-1010) (SM5L2)
  80-pin QFP (QFP080-P-1420) (SM5L2/5L3)

In the absence of confirmation by device specification sheets, SHARP takes no responsibility for any defects that may occur in equipment using any SHARP devices shown in catalogs, data books, etc. Contact SHARP in order to obtain the latest device specification sheets before using any SHARP device.

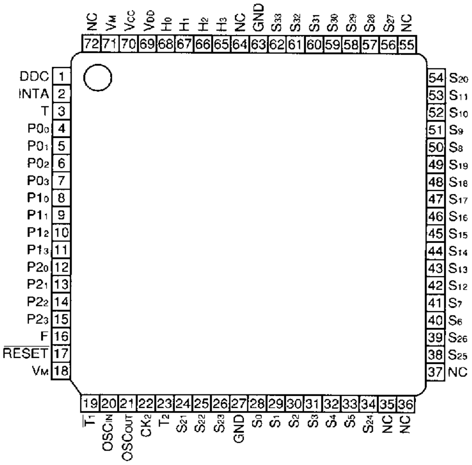
PIN CONNECTIONS

TOP VIEW

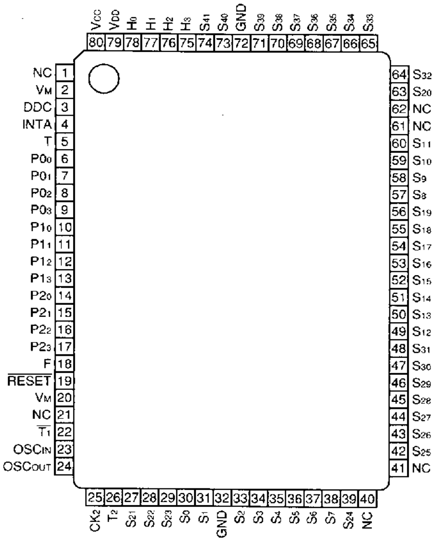
60-PIN QFP (SM5L1)



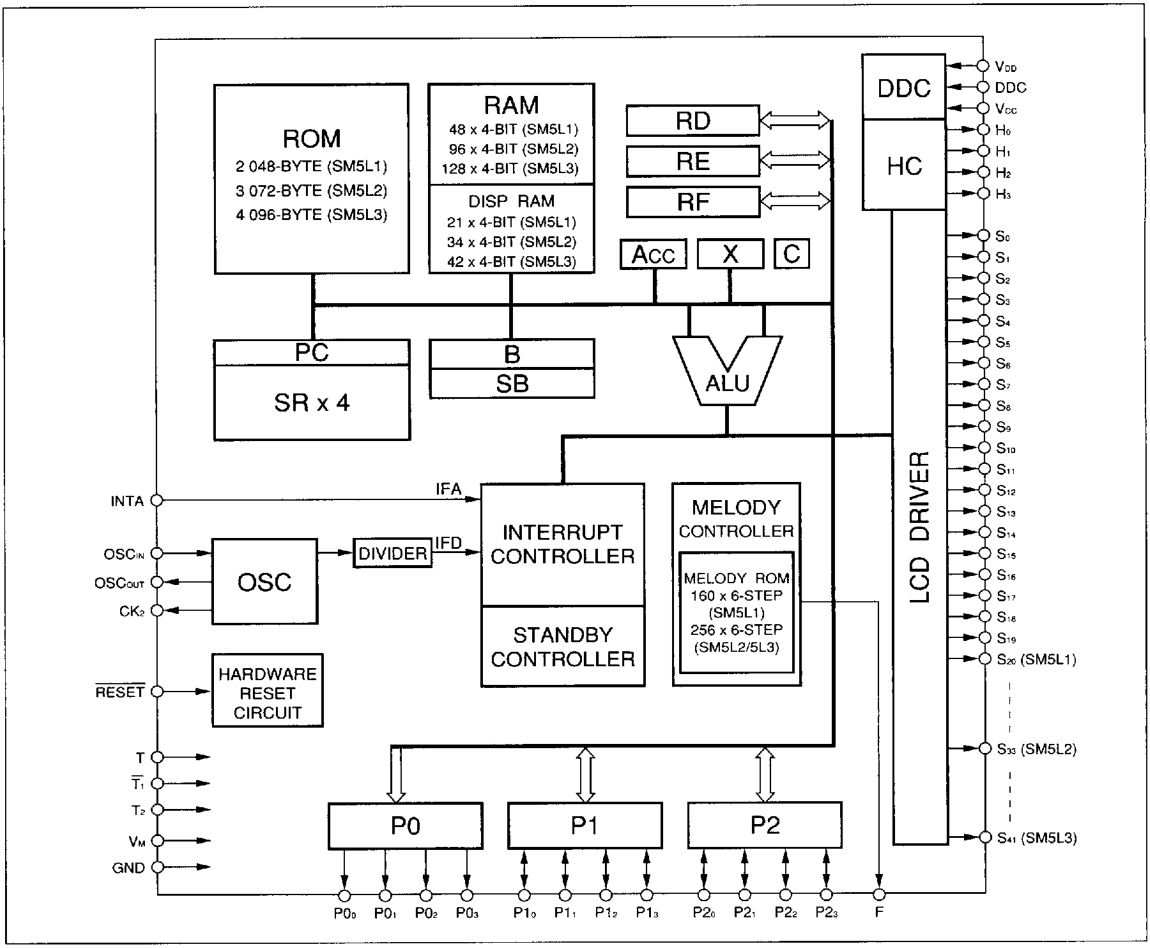
72-PIN QFP (SM5L2)



80-PIN QFP (SM5L2/SM5L3)



BLOCK DIAGRAM



Nomenclature

Acc	: Accumulator	P0-P2	: Port registers
ALU	: Arithmetic logic unit	PC	: Program counter
B	: RAM address register	RAM	: Data memory
C	: Carry flag	RD, RE, RF	: Mode registers
DDC	: Display boost circuit	ROM	: Program memory
HC	: Backplate signal generator circuit	SB	: Stack B register
IFA	: External interrupt flag	SR	: PC stack register
IFD	: Divider overflow flag	X	: X register
OSC	: System clock oscillator		

PIN DESCRIPTIONS

PIN NAME	I/O	FUNCTION
GND, V_M	I	Power supply pins. The V_M pin applies a positive supply with respect to the GND.
T, $\overline{T_1}$, T_2	I	LSI chip test pins. Cannot be used by the user. Connect T and T_2 pin to GND. Connect $\overline{T_1}$ pin to V_M.
$\overline{\text{RESET}}$	I	Input pin with built-in pull-up register. Hardware-reset the LSI chip when a Low level signal is input. Normally, a capacitor is connected between it and GND to form a power-on reset circuit.
OSC_{IN}, OSC_{OUT}, CK_2	I/O	CR or crystal oscillator pins. Connect a CR or crystal oscillating element across [OSC_{IN} - OSC_{OUT} (crystal)] or [OSC_{IN} - CK_2 (CR)] to form a clock generator circuit. (Use of a CR or crystal oscillating element is determined by the mask option)
F	O	Melody output pin. Outputs the contents of a melody ROM with 12-musical scale (555 to 2114 Hz) in two octaves.
H_0-H_3	O	Backplate output pins. Pins for the LCD's backplate signals.
S_0-S_{20} (SM5L1) S_0-S_{33} (SM5L2) S_0-S_{41} (SM5L3)	O	Pins for the LCD's segment signals.
INTA	I	Input pin for external interrupt. The IFA flag is set at the leading edge of INTA.
$P0_0$-$P0_3$	O	Output pins. The accumulator A_{CC} can be transferred to this port by instruction.
$P1_0$-$P1_3$, $P2_0$-$P2_3$	I/O	I/O pins which can switch to input or output pins in 4-bit units by instruction. They can be used as output pins when configured for a key matrix. The SM5Lx is forced to hardware-reset when all of $P1_0$ to $P1_3$ pins are High level. (By mask option)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Power supply voltage	V_M	−0.3 to 2.0	V	
	V_{DD}	−0.3 to 4.0		
Input voltage	V_I	−0.3 to V_M + 0.3	V	
Output voltage	V_O	−0.3 to V_M + 0.3	V	
Source output current for each pin	I_{O1}	2	mA	1
	I_{O2}	2	mA	2
	I_{O3}	2	mA	3
	I_{O4}	2	mA	4
Sink output current for each pin	I_{O5}	2	mA	1
	I_{O6}	100	μA	2
	I_{O7}	2	mA	3
	I_{O8}	2	mA	4
Total source output current	I_{OH}	10	mA	
Total sink output current	I_{OL}	10	mA	
Operating temperature	T_{OPR}	0 to 50	°C	
Storage temperature	T_{STG}	–55 to 150	°C	

NOTES :

1. Applicable pins : $P0_0$-$P0_3$
2. Applicable pins : $P1_0$-$P1_3$, $P2_0$-$P2_3$
3. Applicable pins : F
4. Applicable pins : H_0-H_3, S_0-S_{20} (SM5L1), S_0-S_{33} (SM5L2), S_0-S_{41} (SM5L3)

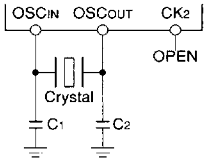
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Power supply voltage	V_M	1.35 to 1.65 (SM5L1) 1.2 to 1.8 (SM5L2/5L3)	V	
	V_{DD}	2.4 to 3.6		
Instruction cycle	T_{SYS}	122 to 50	μs	
Oscillation starting voltage	V_{OSC}	1.4	V	1

NOTE :

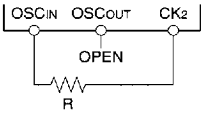
1. Use the crystal oscillation circuit

Oscillation Circuit



Crystal : 32.768 kHz
C_1 = 8 pF
C_2 = 8 pF

Crystal oscillation (frequency = 32.768 kHz)



Degree of fluctuation frequency : ± 30%
(V_M = 1.5 V, T_{OPR} = 25°C)

CR oscillation (frequency = 40 kHz)

NOTE :

Mount the R, C and crystal as close to the LSI chip as possible to minimize the effects of stray capacitance.

DC CHARACTERISTICS

(V_M = 1.5 ± 0.1 V, Ta = 0 to +50°C)

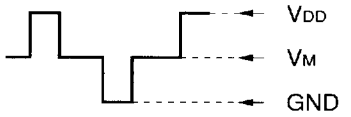
PARAMETER	SYMBOL	CONDITIONS	MIN.*1	TYP.*2	MAX.*1	UNIT	NOTE
Input voltage	V_{IH1}		0.8 x V_M		V_M	V	1
	V_{IL1}		0		0.2 x V_M		
	V_{IH2}		V_M−0.25		V_M	V	2
	V_{IL2}		0		0.25		
Input current	I_{IH1}	V_{IH} = V_M			1.0	µA	3
	I_{IH2}	V_{IH} = V_M		1.5/3/3			4
	I_{IL1}	V_{IL} = 0 V		1.5/3/3			5
Boost output voltage	V_{DD1}	V_M = 1.4 V RL = 5 MΩ	2.5			V	6
	V_{DD2}	V_M = 1.6 V RL = 5 MΩ	2.9				
Output current	$-I_{OH1}$	V_{OH} = V_M−0.5 V	100			µA	7
	I_{OL1}	V_{OL} = 0.5 V	100				
	$-I_{OH2}$	V_{OH} = V_M−0.5 V	100				8
	I_{OL2}	V_{OL} = 0.5 V	3.0				
Output impedance	D_{COM}	V_M = 1.5 V		15		kΩ	9
	D_S	V_M = 1.5 V		30			10
Supply current	I_{DA}	V_M = 1.5 V T_{SYS} = 122 µs		8/10/12	15	µA	11
	I_{DH1} (Halt mode)			5/7/8	8		12
	I_{DH2} (Halt mode)			3/4/5	5		13
	I_{DS} (Stop mode)			1/1.5/2	3		14

*1 : SM5L1's spec.

*2 : */*/* → SM5L1/5L2/5L3

NOTES :

1. Applicable pins : $P1_0$-$P1_3$, $P2_0$-$P2_3$
2. Applicable pins : OSC_{IN}, $\overline{RESET}$, T, INTA
3. Applicable pins : $P2_0$-$P2_3$
4. Applicable pins : T, INTA, $P1_0$-$P1_3$
5. Applicable pins : $\overline{RESET}$
6. Applicable pins : V_{DD}
7. Applicable pins : $P0_0$-$P0_3$, F
8. Applicable pins : $P1_0$-$P1_3$, $P2_0$-$P2_3$
9. Applicable pins : H_0-H_3
10. Applicable pins : S_0-S_{20} (SM5L1), S_0-S_{33} (SM5L2), S_0-S_{41} (SM5L3)
11. No-load condition. Supply current under the operation when driving a CR oscillator.
12. No-load condition. Supply current when driving a CR oscillator and turning LCD ON placed the device in halt mode.
13. No-load condition. Supply current when driving a CR oscillator and turning LCD OFF placed the device in halt mode.
14. No-load condition. Supply current when the entire system is inactivated.



LCD wave form (EXAMPLE)

SYSTEM CONFIGURATION

A Resister and X Register

The A register (or accumulator : Acc) is a 4-bit general purpose register. The register is mainly used in conjunction with the ALU, C flag and RAM, to transfer numerical value and data to perform various operations. The A register is also used to transfer data between input and output pins.

The X register (or auxiliary accumulator) is a 4-bit register and can be used as a temporary register. It loads contents of the A register or its content is transferred to the A register.

When the table reference instruction PAT is used, the X and A registers load ROM data.

A pair of A and X registers can accommodate 8-bit data.

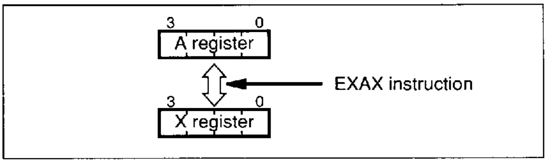


Fig. 1 Data Transfer Example Between A Register, and X Register

Arithmetic and Logic Unit (ALU) and Carry Signal Cy

The ALU performs 4-bit parallel operation.

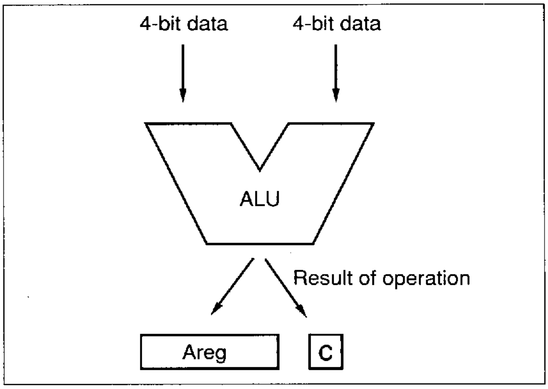


Fig. 2 ALU

The ALU operates binary addition in conjunction with RAM, C flag and A register. The carry signal Cy is generated if a carry occurs during ALU operation. Some instructions use Cy : ADC instruction sets/clear the content of the C flag; ADX instruction causes the program to skip the next instruction. Note that Cy is the symbol for carry signal and not for C flag.

B Register and SB Register

- **B register (B_M, B_L)**

The B register is an 8-bit register that is used to specify the RAM address.

The upper 4-bit section is called B_M register and lower 4-bit B_L.

- **SB register**

The SB register is an 8-bit register used as the save register for the B register. The contents of B register and SB register can be exchanged through EX instruction.

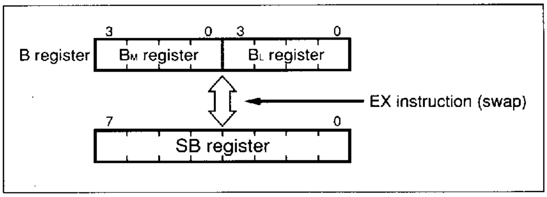


Fig. 3 B Register and SB Register

Data Memory (RAM)

The data memory (RAM) is used for data storage. The RAM capacity consists of

- SM5L1 : 69 x 4-bit (include 21 x 4-bit display RAM)
- SM5L2 : 130 x 4-bit (include 34 x 4-bit display RAM)
- SM5L3 : 170 x 4-bit (include 42 x 4-bit display RAM)

Display RAM which outputs data to an external pin for driving the segments of the LCD. Therefore, by writing data to the display RAM, the LCD can be driven at 1/4 duty (1/2 bias) to enable automatic display of the LCD.

As shown in Fig. 7 the display RAM is connected to segment outputs

- SM5L1 : Port S_0 to S_{20}
- SM5L2 : Port S_0 to S_{33}
- SM5L3 : Port S_0 to S_{41}

which correspond to the LCD backplate outputs H_0 to H_3. Data M_0 to M_3 for one column of the display RAM is output pins as a LCD drive waveform which corresponds to outputs H_0 to H_3. As a RAM, the display RAM operates exactly the same as other RAMs.

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
8	S_0	S_2	S_4	S_6	S_8	S_{10}	S_{12}	S_{14}	S_{16}	S_{18}	S_{20}					
9	S_1	S_3	S_5	S_7	S_9	S_{11}	S_{13}	S_{15}	S_{17}	S_{19}						

* The area surrounded by the thick line represents the display RAM where S_0 to S_{20} corresponds to the segment output.

Fig. 4 RAM Organization (SM5L1)

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
8	S_0	S_2	S_4	S_6	S_8	S_{10}	S_{12}	S_{14}	S_{16}	S_{18}	S_{20}	S_{22}	S_{24}	S_{26}	S_{28}	S_{30}
9	S_1	S_3	S_5	S_7	S_9	S_{11}	S_{13}	S_{15}	S_{17}	S_{19}	S_{21}	S_{23}	S_{25}	S_{27}	S_{29}	S_{31}
A	S_{32}															
B	S_{33}															

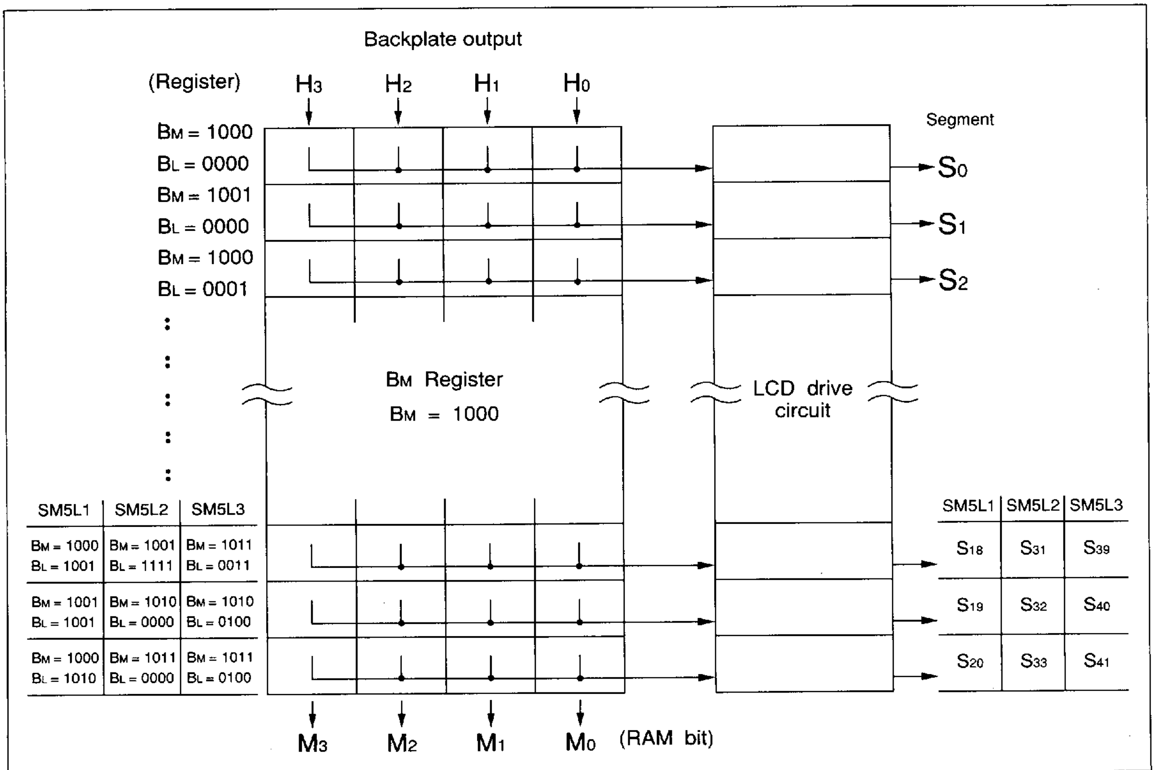
* The area surrounded by the thick line represents the display RAM where S_0 to S_{33} corresponds to the segment output.

Fig. 5 RAM Organization (SM5L2)

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																
8	S_0	S_2	S_4	S_6	S_8	S_{10}	S_{12}	S_{14}	S_{16}	S_{18}	S_{20}	S_{22}	S_{24}	S_{26}	S_{28}	S_{30}
9	S_1	S_3	S_5	S_7	S_9	S_{11}	S_{13}	S_{15}	S_{17}	S_{19}	S_{21}	S_{23}	S_{25}	S_{27}	S_{29}	S_{31}
A	S_{32}	S_{34}	S_{36}	S_{38}	S_{40}											
B	S_{33}	S_{35}	S_{37}	S_{39}	S_{41}											

* The area surrounded by the thick line represents the display RAM where S_0 to S_{41} corresponds to the segment output.

Fig. 6 RAM Organization (SM5L3)



SM5L1	SM5L2	SM5L3
B_M = 1000 B_L = 1001	B_M = 1001 B_L = 1111	B_M = 1011 B_L = 0011
B_M = 1001 B_L = 1001	B_M = 1010 B_L = 0000	B_M = 1010 B_L = 0100
B_M = 1000 B_L = 1010	B_M = 1011 B_L = 0000	B_M = 1011 B_L = 0100

SM5L1	SM5L2	SM5L3
S_{18}	S_{31}	S_{39}
S_{19}	S_{32}	S_{40}
S_{20}	S_{33}	S_{41}

Fig. 7 Relationship between the Display RAM and LCD Segment Outputs / Backplate Outputs

Program Counter PC and Stack Register SR

A ROM address is specified by the program counter (PC). The PC comprises 12-bit where 6-bit (P_U) are used to specify the page (see Fig. 8) and 6-bit (P_L) are used to specify the step. P_U is a register and P_L is a binary counter.

The table reference instruction PAT executes a similar operation to that of the subroutine jump and uses one level of the stack register.

Program Memory (ROM)

The ROM is used for program storage. The ROM capacity of the SM5Lx is 2 048/3 072/4 096-step (SM5L1/5L2/5L3). The ROM is organized into 32/48/64 (SM5L1/5L2/5L3)-page where one page is organized into 64-step.

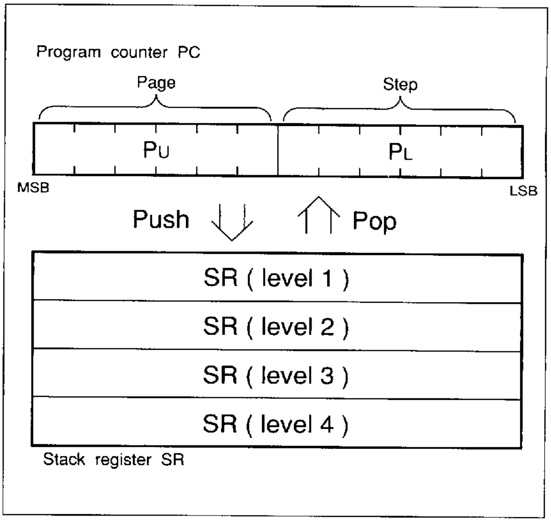


Fig. 8 Program Counter PC and Stack Register SR

Page	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH
Pu	000000	000001	000010	000011	000100	000101	000110	000111	001000	001001	001010	001011	001100	001101	001110	001111
	Program start	First page of subroutine TRS	Interrupt	Standby release	Table reference page PAT											

Page	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
Pu	010000	010001	010010	010011	010100	010101	010110	010111	011000	011001	011010	011011	011100	011101	011110	011111
																Last page (SM5L1)

Page	20H	21H	22H	23H	24H	25H	26H	27H	28H	29H	2AH	2BH	2CH	2DH	2EH	2FH
Pu	100000	100001	100010	100011	100100	100101	100110	100111	101000	101001	101010	101011	101100	101101	101110	101111
																Last page (SM5L2)

Page	30H	31H	32H	33H	34H	35H	36H	37H	38H	39H	3AH	3BH	3CH	3DH	3EH	3FH
Pu	110000	110001	110010	110011	110100	110101	110110	110111	111000	111001	111010	111011	111100	111101	111110	111111
																Last Page (SM5L3)

Fig. 9 ROM Organization

Flags

The SM5Lx provides 3-flag (C flag and interrupt request flag <IFA, IF0>) which can be used to set or determine conditions.

Output Latch Registers and Mode Registers

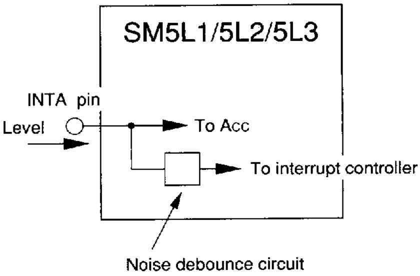
The output latch registers are connected to the P0, P1 and P2 pins. By instruction, the contents of the Acc can be transferred to the output latch registers. The SM5Lx also contains mode registers RD, RE, and RF. Setting the value of each register enables the LCD or interrupt to be controlled. Setting a register is performed in the same way as the other output pins. The functions of the mode registers are shown in Table 1.

- **INTA pin**

INTA level can be loaded to Acc (bit 0), as follows.

```
LBLX    4
IN
```

In case, INTA level does not through the noise debounce circuit.



CAUTION :

Connecting considerations of I/O port

When using an I/O port as bidirectional bus such as data bus, avoid setting the I/O port to output when the target pin is also set to output.

Whenever the both output data conflict each other, system failure will be causes due to damage to circuits or instantaneous supply voltage drop.

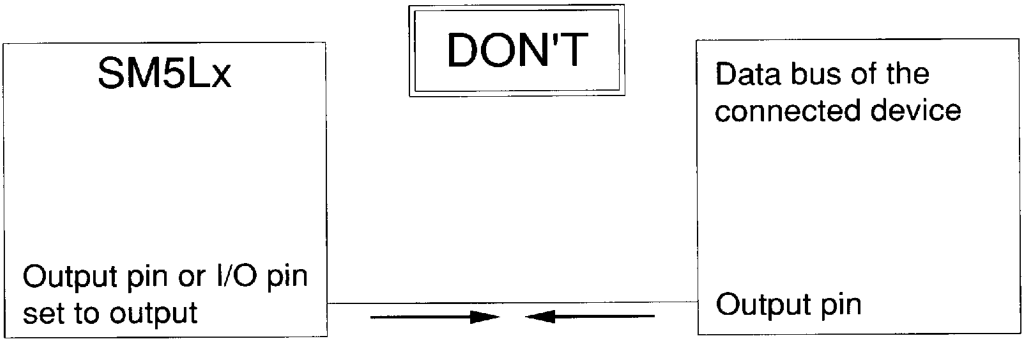

DON'T
SM5Lx
Output pin or I/O pin set to output
Data bus of the connected device
Output pin

Table 1 Mode Register Setting

REGISTER		SET VALUE	MODE DESCRIPTION
TYPE	BIT		
RD	RD0	0	Clear the ME F/F to stop a melody.
		1	Set the ME F/F to start a melody from a ROM pointer address.
	RD1		Set by stop instruction (of melody code) and reset by TPB instruction.
	RD2	–	Set to "0" only.
	RD3		
RE	RE0	0	Mask the interrupt based on the IFA flag.
		1	Accept the interrupt based on the IFA flag.
	RE1	–	Set to "0" only.
	RE2	0	Mask the interrupt based on the IFD flag.
		1	Accept the interrupt based on the IFD flag.
	RE3	–	No setting.
RF	RF0	0	Turn off the LCD.
		1	Turn on the LCD.
	RF1	0	Stop the function of a booster circuit.
		1	Operate the function of a booster circuit.
	RF2	0	Create the system clock frequency by dividing two the main oscillation frequency.
		1	Create the system clock frequency by dividing four the main oscillation frequency.
	RF3	–	Set to "0" only.

System Clock Generator and Dividers

The main oscillation frequency which is input through "OSC$_{IN}$ - OSC$_{OUT}$" or "OSC$_{IN}$ - CK$_2$" is divided into 2 or 4 to generate the system clock f$_{SYS}$ (Fig. 10).

System clock f$_{SYS}$ determines the execution instruction cycle so that the system clock period is the same as the instruction cycle.

However, the instruction execution cycle of two-word instruction is twice that of one-word instructions.

Use of a CR oscillating element or a crystal oscillating element for the oscillator circuit is determined by the mask option. On the final stage of the divider, fc can be set to 1 Hz or 2 Hz (in case of 32 kHz crystal oscillation) depending on the mask option.

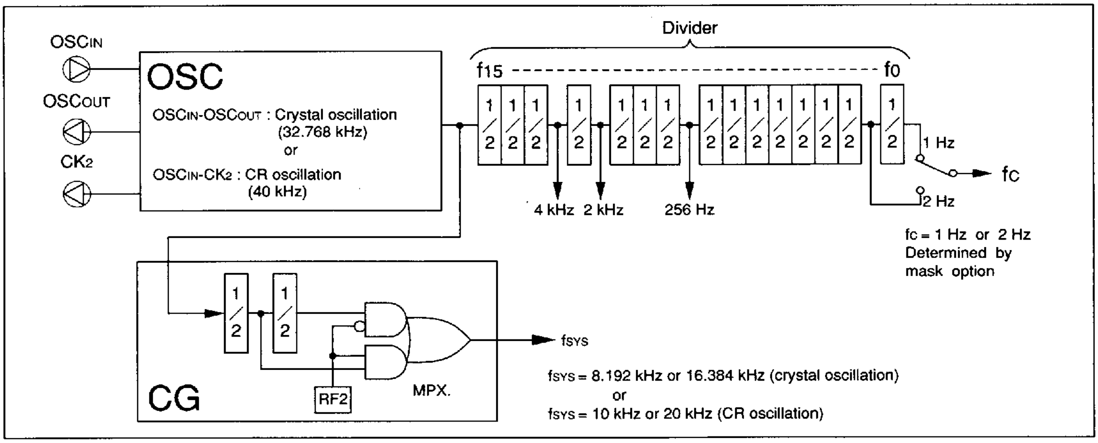

OSC$_{IN}$
OSC$_{OUT}$
CK$_2$
OSC
OSC$_{IN}$-OSC$_{OUT}$: Crystal oscillation (32.768 kHz)
or
OSC$_{IN}$-CK$_2$: CR oscillation (40 kHz)
Divider
f$_{15}$
f$_0$
1/2
4 kHz
2 kHz
256 Hz
1 Hz
2 Hz
fc
fc = 1 Hz or 2 Hz Determined by mask option
CG
RF2
MPX.
f$_{SYS}$
f$_{SYS}$ = 8.192 kHz or 16.384 kHz (crystal oscillation)
or
f$_{SYS}$ = 10 kHz or 20 kHz (CR oscillation)

Fig. 10 System Clock Generator and Divider

Either of the system clock frequencies 16.384 kHz or 8.192 kHz (in case of 32.768 kHz oscillation) can be selected by the RF2 flag (See Table 2). The 8.192 kHz clock has slower command execution speed, but uses less power for the same function.

The system clock is initialized to 16.384 kHz after Hardware reset operation.

The Table 2 shows the relationship between the contents of RF2 flag for OSC resonator and the generated frequency, f$_{SYS}$.

Table 2 OSC Resonator and Frequency f$_{SYS}$

FOR OSC RESONATOR	CONTENTS OF RF2 FLAG	GENERATED FREQUENCY f$_{SYS}$
32.768 kHz crystal oscillation	0	16.384 kHz
	1	8.192 kHz
40 kHz CR oscillation	0	20 kHz
	1	10 kHz

FUNCTIONAL DESCRIPTION

Melody Output Function

The built-in chip melody generation circuit provides a variety of sound signals. Fig. 11 shows the block diagram of the melody generating circuit.

The melody ROM can store notes, rest and stop commands in 160/256/256 (SM5L1/5L2/5L3)-step (1 step consists of 6-bit), allowing the generation of 12-scale over two octaves (555 to 2 097 Hz) and the section of the time base for notes (125/62.5 ms).

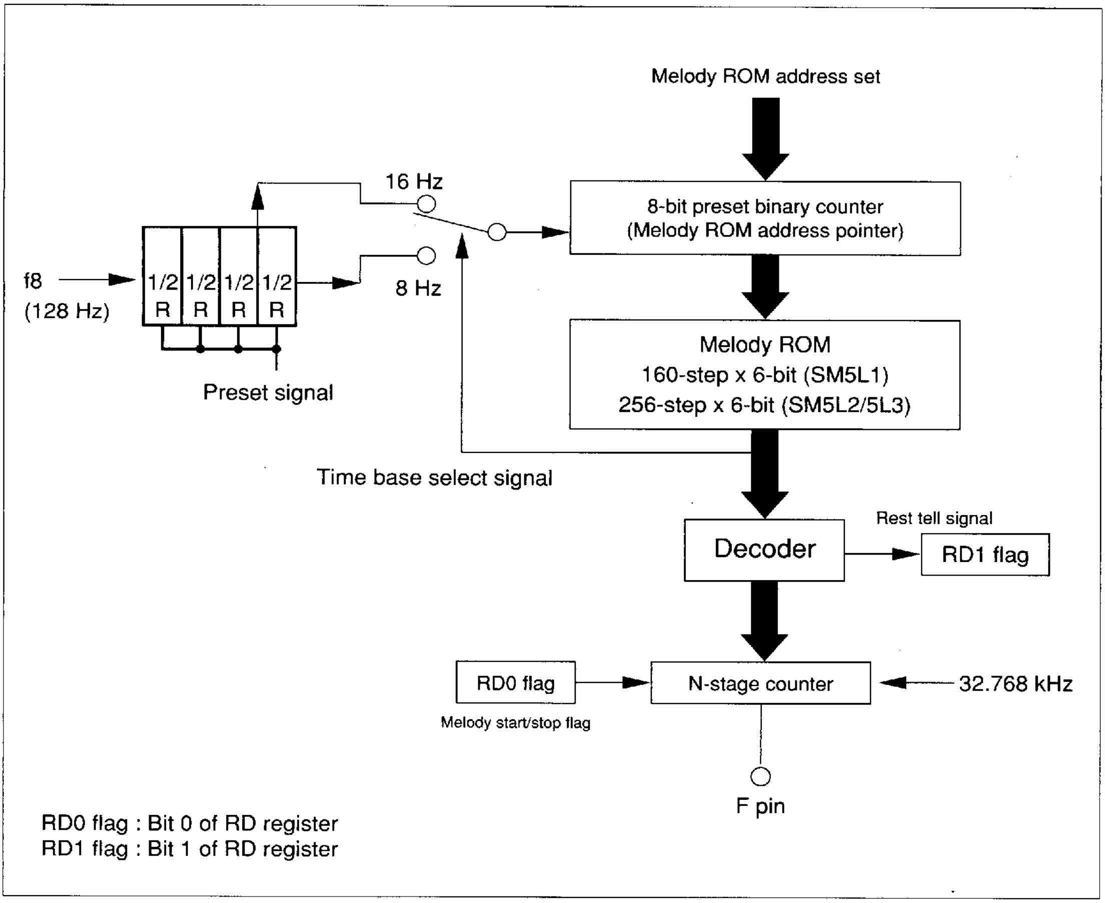


Fig. 11 Melody Generating Circuit

CONTROL PROCEDURE

The binary counter for designating the address of the melody ROM can be arbitrarily set using the PRE instruction. A performance is started and stopped by the RD0-flag to "1" and "0".

The stop code generates a "rest tell signal", and at the same time, sets the RD1 flag. The end of the melody can be found by testing the RD1 flag.

Accordingly, to stop a performance at the end of melody, the RD0 flag must be clear upon detection of RD1 flag = 1.

Next step of PRE instruction, put the NOP instruction.

The following is an example of a melody generating program.

```
MELO    LAX     2
        ATX
        LAX     1
        PRE                     ; Set the starting address of
                                  the melody at the 21st.
                                  Hexadecimal step.
        NOP                     ; Dummy command
        :
        :
        LBLX    0DH
        LAX     1
        OUT                     ; Start the melody
        TPB     1               ; Executed for clear the
                                  RD1 flag
        NOP                     ; Dummy command
        :
        :
        LBLX    0DH
L1      TPB     1               ; Test the RD1 flag
        TR      L1              ; Loop for detect the stop
                                  code
        LAX     0
        OUT                     ; Stop the melody
```

Using these functions, the user can generate music, sound effects, alarm signals, etc. as desired, and any portion of the music can be repeated. Table 3 lists the melody output frequencies. The output frequency can be halved by making bit 5 (OCT) of the melody ROM 0 (Low). In Table 3, m0 to m3 show data in bits 1 to 4 of the melody ROM.

Table 3 Melody Output Frequency

	m_3 m_2 m_1 m_0	OUTPUT FREQUENCY (Hz)	CLOCK NUMBER *1	*2			
do	0 0 1 0	2114.1	15.5	7	8	8	8
si	0 0 1 1	1985.9	16.5	8	8	8	9
la#	0 1 0 0	1872.4	17.5	8	9	9	9
la	0 1 0 1	1771.2	18.5	9	9	9	10
sol#	0 1 1 0	1680.4	19.5	9	10	10	10
sol	0 1 1 1	1560.4	21.0	10	11	10	11
fa#	1 0 0 0	1489.5	22.0	11	11	11	11
fa	1 0 0 1	1394.4	23.5	11	12	12	12
mi	1 0 1 0	1310.7	25.0	12	13	12	13
re#	1 0 1 1	1236.5	26.5	13	13	13	14
re	1 1 0 0	1170.3	28.0	14	14	14	14
do#	1 1 0 1	1110.8	29.5	14	15	15	15

*1 Number of clocks for one cycle

*2 The number (n) in the waveforms represents the number of periods of the oscillation frequency (32.768 kHz) from the crystal oscillator for the duration in that particular part of the waveform.

MELODY ROM INSTRUCTION

The melody ROM instruction is composed of 6-bit. This 6-bit instruction (1 set), corresponding to a musical note, generates a sound signal.

I	OCT	m_3	m_2	m_1	m_0

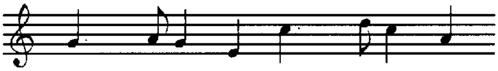
I : Control the tone length. When "1", 125 ms; when "0", 62.5 ms.

OCT : When the octave is "1", the frequency is determined by m_3 -m_0.
When the octave is "0", 1/2 the frequency determined by m_3 -m_0.

m_3 - m_0 : Frequency as shown in Table 3.
Pause when m_3 = m_2 = m_1 = m_0 = 0, stop instruction when m_3 = m_2 = m_1 = 0, m_0 = 1.

EXAMPLE OF WRITING ON THE MELODY ROM

An example of writing a tune such as the following, on the melody ROM will be shown.



MUSICAL SCALE	TONE LENGTH (ms)	OCT	m_3	m_2	m_1	m_0
sol	375	0	0	1	1	1
la	125	0	0	1	0	1
sol	250	0	0	1	1	1
mi	250	0	1	0	1	0
do	375	1	0	0	1	0
re	125	1	1	1	0	0
do	250	1	0	0	1	0
la	250	0	0	1	0	1

ADDRESS	DATA	MUSICAL NOTE INSTRUCITON
00	00	pause
01	27	sol
02	27	sol
03	27	sol
04	25	la
05	27	sol
06	27	sol
07	2A	mi
08	2A	mi
09	22	do
0A	22	do
0B	22	do
0C	3C	re
0D	22	do
0E	22	do
0F	25	la
10	25	la
11	01	stop

The tone length of an initial musical note which is generated from ROM addressed data assigned by a PRE instruction has an error of maximum ±4 ms. Therefore, by applying a pause as an initial note, a melody performs with a precisely regulated tone length.

Standby Function

A standby function is available which temporary stops program execution to conserve power consumption. The state during which a program is in execution is called the operation mode and the state during which the execution is temporary stopped is called the standby mode.

The standby mode further contains two modes, the stop mode and the halt mode. The stop mode stops the system section. In the stop mode, the display (LCD) is blanked. And the response speed of LCD returning to the display state (the operation) drops slightly.

The halt mode stops only system clock generator circuit (the state of the LCD is retained). This mode is used to activate the system immediately after a condition cause a release to the operation mode.

To enter the standby mode, select either stop mode or halt mode whichever appropriate. (Fig. 12)

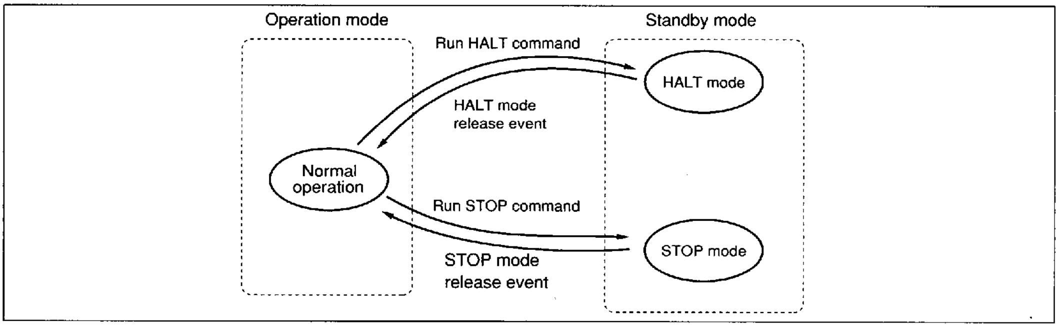


Fig. 12 Operation Shift of Program

During the standby mode, the contents of the RAM and C flag are retained. The contents of the flags, registers and output latches shown below are also retained.

FLAG
IFA flag
IFD flag
IME flag

REGISTER
Acc
X register
BM, BL register
SP
SR

OUTPUT LATCH REGISTER
P0 register
P1 register
P2 register

A release from the standby mode to the operation mode is performed by a reset port input, an interrupt from the nonmaskable INTA, and divider. A maskable interrupt request cannot become a factor in releasing back to the operation mode. The mask setting is performed with RE register. (see Table 2)

CAUTION :

When all of P10 to P13 level are High, the SM5Lx is performed to release the standby mode and enter normally hardware reset operation. (Mask option)

Next, the transition of the standby mode and the release method from the standby mode are described.

TRANSITION FORM THE OPERATION MODE TO THE STANDBY MODE

The HALT instruction is executed to set the halt mode and the STOP instruction is executed to set the stop mode.

Since the interrupt is used to release from the standby mode, the mode does not transfer to the standby mode if any of the following conditions are satisfied during execution of the STOP or HALT instruction.

a) RE0 is set and the INTA level is High.

b) RE2 is set and the IFD flag is set.

If any of the conditions above is satisfied, the mode does not transfer to the standby mode even if the STOP or HALT instruction is executed and the instruction at the address following that of the STOP or HALT instruction is executed. Therefore, place the JUMP instruction which specifies step 0 on page 3 to the location at the address following that of the STOP or HALT instruction.

RELEASE FROM THE STANDBY MODE TO THE OPERATION MODE

Release based on an interrupt request from the INTA pin, or divider overflow. However, the reset is limited to a nonmaskable interrupt request.

The program restarts from step 0 on page 3. However, if the IME flag is set, the instruction at step 0 on page 3 is executed and a subroutine jump is performed to the interrupt processing routine specified on page 2 according to the type of interrupt.

Even if Low level input on INTA pin is removed before 900 command cycles, the stop mode is released.

However, the program will not jump to 20_H page (interrupt process routine).

Interrupt request flag IFA is not set : the program continues at step 0 of 03_H page.

Interrupts

Interrupts originate from an INTA input or divider overflow. The IFA, and IFD flags become interrupt request flags.

The interrupt block is composed of mask flags (RE0, RE2), the IME flag and interrupt processing circuit.

As shown in Fig. 13, resetting a mask flag enables the interrupt request flag to be independently masked. Thus, the mask flags can be used in a program to establish the interrupt priority. The priority for interrupts generated simultaneously is shown in Table 4.

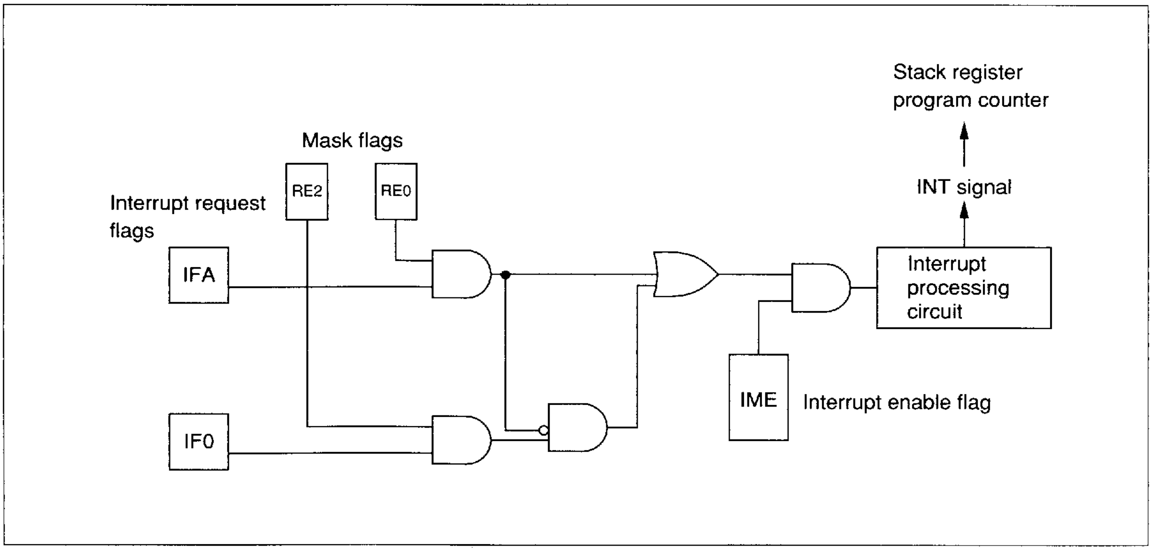


Fig. 13 Interrupt Block

Table 4 Interrupt Event Summary

INTERRUPT REQUEST (REQUEST FLAG)	JUMP DESTINATION		PRIORITY ORDER	INTERRUPT ENABLE FLAG
	PAGE	STEP		
INTA input (IFA)	2	0	1	RE0
Divider overflow (IFD)	2	4	2	RE2

When the IME flag is set, the interrupt circuit activates according to the interrupt request and a subroutine jump is performed to the specified address. The jump destinations according to interrupt origin are shown in Table 4. When the IME flag is cleared, an interrupt is not accepted even if an interrupt request is generated. The interrupt timing are shown in Fig. 14 and Fig. 15. The timing chart shown in Fig. 14 shows the interrupt enable state when an interrupt request has been generated. In this case, the interrupt processing signal INT goes High, one instruction cycle after the interrupt request flag is set. When INT goes High, the contents of the program counter are pushed into the stack register and execution jumps to the specified address. At this time, the INT signal and the IME flag are cleared to establish the interrupt disable mode. The IME flag is set again when the RTNI instruction is executed to establish the interrupt enable mode.

The timing chart shown in Fig. 15 shows the state when interrupts are enabled while multiple interrupts are generated. In this case, a subroutine jump is performed according to the interrupt having the highest priority. When returning from the subroutine by executing the RTNI instruction, the instruction (two words are executed for a two-word instruction) at the location of return is executed and the interrupt for the next highest priority is accepted.

If an interrupt request is generated during execution of a two-cycle instruction, the instruction is executed after which interrupt processing is performed. If consecutive LAX instructions are skipped or if the SKIP conditions are satisfied, the skip operation is terminated after which interrupt processing is performed.

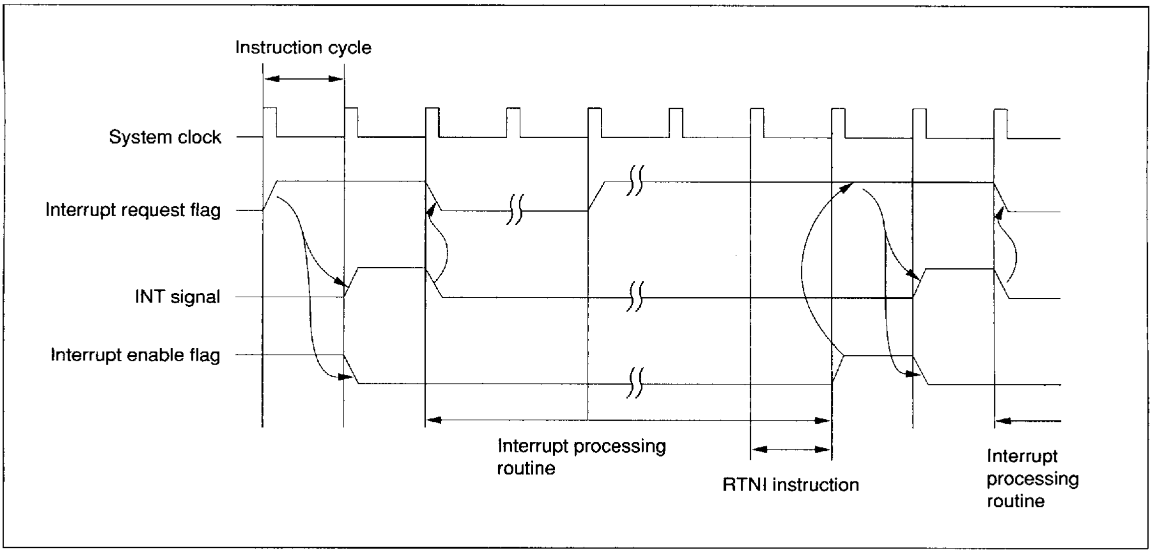


Fig. 14 Interrupt Timing Chart

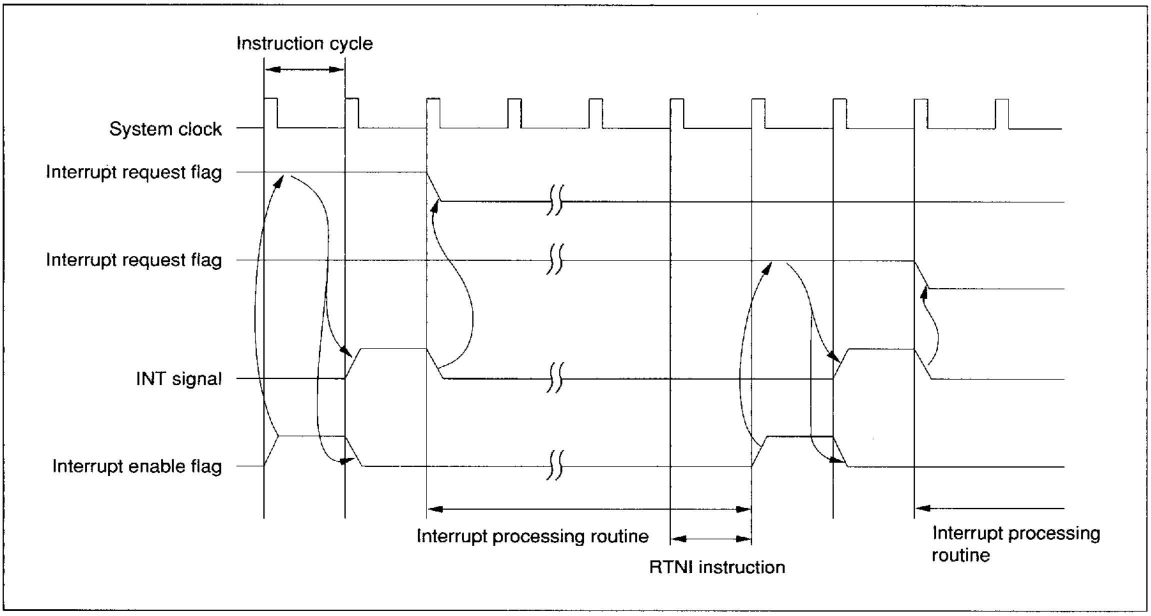


Fig. 15 Interrupt Timing Chart

NOTE :

Fig. 14 and Fig. 15 show the case where the interrupt request flags are not masked.

Hardware Reset Function

The hardware reset function mode activated two instruction cycles after the trailing edge from the RESET pin. When the RESET pin is changed from High to Low, the pulse which is input by the OSC$_{IN}$ pin is counted 2^{15} times after which the reset mode clears and the program counter starts from address 0 on page 0.

The initialized status of the system after reset is shown in Table 5.

The following reset functions are available.

- The I/O port is set as an input port and the mode register RD, RE and RF are cleared. The output only port (P0) is cleared and output Low.
- The interrupt request flags (IFA, IFD) and the interrupt enable flag (IME) are clear and all interrupts become disabled.
- The program counter start from step 0 on page 0.

For activate reset function, when power is turned on, you must be connect a capacitor (0.1 μF, TYP.) across the RESET pin and GND.

Table 5 Reset Status

FLAG OR REGISTER, X-REGISTER	STATUS (in reset mode and at program start)
PC	0
SP	Level 1
RAM	Undefined
A$_{CC}$	Undefined
X-register	Undefined
P0-P2 output latch registers	0
Divider	0
IFA flag	0
IFD flag	0
IME flag	0
C flag	Undefined
B$_M$, B$_L$ registers	Undefined
Register RD (bit 0)	0
Register RD (bit 1)	Undefined
Register RE (bit 2, 1, 0)	0
Register RF (bit 3, 2, 1, 0)	0

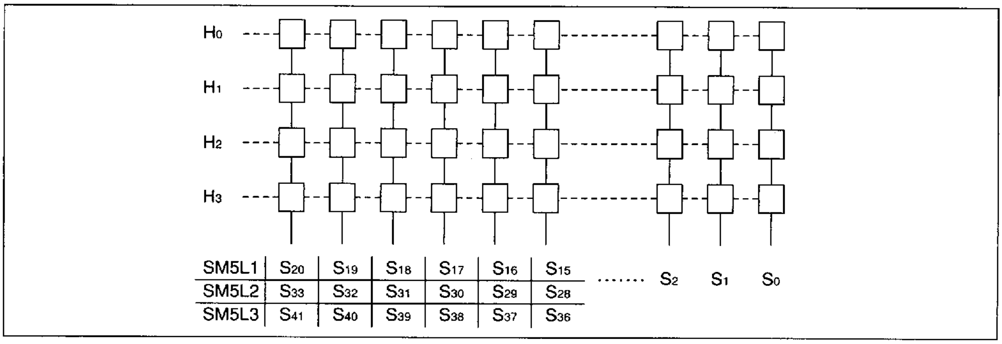
NOTE :

When all of P1 pins (P1$_0$ to P1$_3$) level goes to High, the SM5Lx is performed to reset operation. (Mask option)

LCD Function

• Display segment

The SM5Lx contains a built-in circuit which directly drive a 1/4 duty, 1/2 bias LCD.
A sample LCD pattern is shown in Fig. 16.



SM5L1	S_{20}	S_{19}	S_{18}	S_{17}	S_{16}	S_{15}	......	S_2	S_1	S_0
SM5L2	S_{33}	S_{32}	S_{31}	S_{30}	S_{29}	S_{28}				
SM5L3	S_{41}	S_{40}	S_{39}	S_{38}	S_{37}	S_{36}				

Fig. 16 LCD Pattern

A segment of the LCD can be turned on or off by setting the corresponding bit in the display RAM (see Fig. 7) to "1" or "0". The displayed segments can assume any configuration containing up to a maximum of 84/136/168 (SM5L1/5L2/5L3) segments. An example of a 7-segment numeric display is shown in Fig. 17.

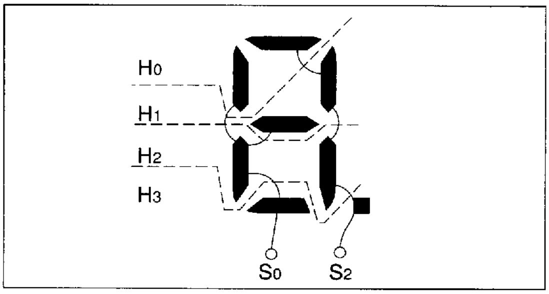


Fig. 17 Sample LCD Pattern for 7-Segment Numeric Display

• LCD drive waveforms

The LCD drive waveforms for the LCD pattern of Fig. 17 displaying a "5" are shown in Fig. 18 (the segment output uses S_0 and S_1). For Fig. 18, 3 V is applied to the V_{DD} pin, and 1.5 V is applied to the V_M pin.

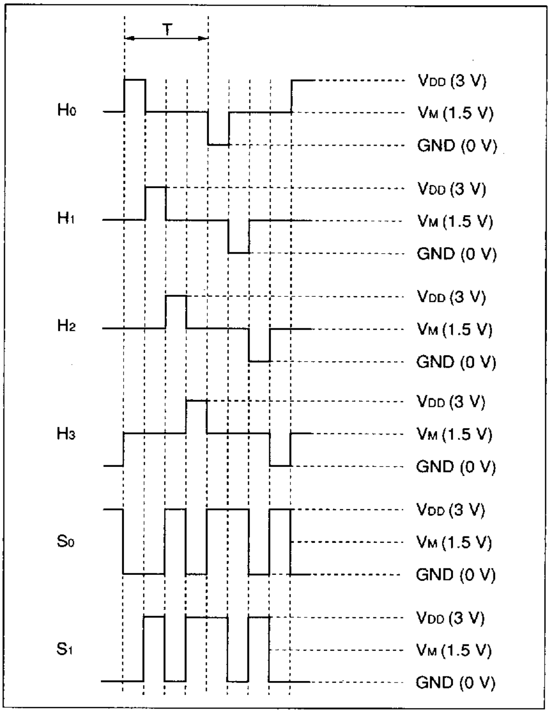


Fig. 18 LCD Drive Waveforms
(frame frequency = 1/T = 64 Hz or 128 Hz)

* Frame frequency is selectable by mask option.

- **Booster circuit**

The device contains a booster circuit which generates a voltage two times higher than the 1.5 V power supply.

Then, it is necessary to apply external capacitors between DDC pin and V_{CC} pin as well as V_{DD} pin and GND (see Fig. 19).

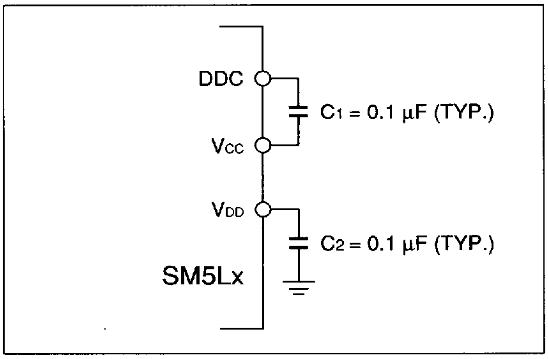


Fig. 19 Booster Circuit

- **Blank display**

There are two way to blank the entire display to match the purpose.

(a) Blanking the display for a short time.

Set bit 0 of the RF register to "1" : Display

Set bit 0 of the RF register to "0" : Blank state

(b) Blanking the display for a long period mainy to reduce supply current.

Set bit 0 and 1 of the RF register to "1" : Display

Set bit 0 and 1 of the RF register to "0" : Blank state

When bit 1 of the RF register is set to "0", the booster circuit does not operate and the backplate outputs and segment outputs are dropped to V_M level, and the display blanks. By stepping the function of the booster circuit, the supply current can be greatly reduced. However, when the display is blanked using method (b), the response speed of the LCD returning to the display state drops slightly. The RF register is on the blank state after initialization from hardware reset.

INSTRUCTION SET

Definition of Symbols

The following symbols are used in descriptions for the instructions.

M : Contents of RAM at the address specified by the B register

← : Transfer direction

∪ : Logical OR

∩ : Logical AND

⊕ : Logical XOR

Ai : ith bit of the Acc

Push : Content of the PC are decremented to the stack register.

Pop : The decremented contents are transferred back to the PC.

Pj : Pj register (j = 0, 1, 2, 3)

Rj : Rj register (j = D, E, F)

ROM ( ) : ROM contents for address within ( )

Cy : Carry of ALU (different from the C flag)

- Each bit of a register can be represented. For example, the ith bit of X register and R(0) register are represented as Xi and R(0) i. (i = 0, 1, 2, 3, ...)
- Increment and decrement denote the binary addition of 1_H and F_H, respectively.
- To skip a certain instruction means that the instruction is ignored and that no operation is performed until the execution transfers to the next instruction. In other words, the instruction is regarded as a NOP instruction. Therefore, one cycle is required to skip a one-word instruction and two cycles are required to skip a two-word instruction.

Instruction Summary

MNEMONIC	MACHINE CODE	OPERATION
ROM Address Control Instructions		
TR x	80 to BF	P_L ← x (I_5-I_0)
TL xy	E0 to EF 00 to FF	P_U ← x (I_{11}-I_6) P_L ← y (I_5-I_0)
TRS x	C0 to DF	Push, P_U ← 01_H P_L ← x (I_4, I_3, I_2, I_1, I_0, 0)
CALL xy	F0 to FF 00 to FF	Push, P_U ← x (I_{11}-I_6) P_L ← y (I_5-I_0)
RTN	7D	Pop
RTNS	7E	Pop, Skip the next step
RTNL	7F	Pop, IME ← 1
Data Transfer Instructions		
LAX x	10 to 1F	Acc ← x (I_3-I_0)
LBMX x	30 to 2F	B_M ← x (I_3-I_0)
LBLX x	20 to 2F	B_L ← x (I_3-I_0)
LDA x	50 to 53	Acc ← M B_{Mi} ← B_{Mi} ⊕ x (I_1, I_0) (i = 1, 0)
EXC x	54 to 57	M ↔ Acc B_{Mi} ← B_{Mi} ⊕ x (I_1, I_0) (i = 1, 0)
EXCI x	58 to 5B	M ↔ Acc, B_L ← B_L+1 B_{Mi} ← B_{Mi} ⊕ x (I_1, I_0) (i = 1, 0) Skip if Cy = 1 (B_L = F_H → 0)
EXCD x	5C to 5F	M ↔ Acc, B_L ← B_L+F_H B_{Mi} ← B_{Mi} ⊕ x (I_1, I_0) (i = 1, 0) Skip if Cy = 1 (B_L = 0 → F_H)
EXAX	64	Acc ↔ X
ATX	65	x ← Acc
EXBM	66	B_M ↔ Acc
EXBL	67	B_L ↔ Acc
EX	68	B ↔ SB
Arithmetic Instructions		
ADX x	00 to 0F	Acc ← Acc+x (I_3-I_0), Skip if Cy = 1
ADD	7A	Acc ← Acc+M
ADC	7B	Acc ← Acc + M+C, C ↔ Cy Skip if Cy = 1
COMA	79	Acc ← $\overline{\text{Acc}}$
INCB	78	B_L ← B_L+1, Skip if B_L = F_H
DECB	7C	B_L ← B_L–1, Skip if B_L = 0

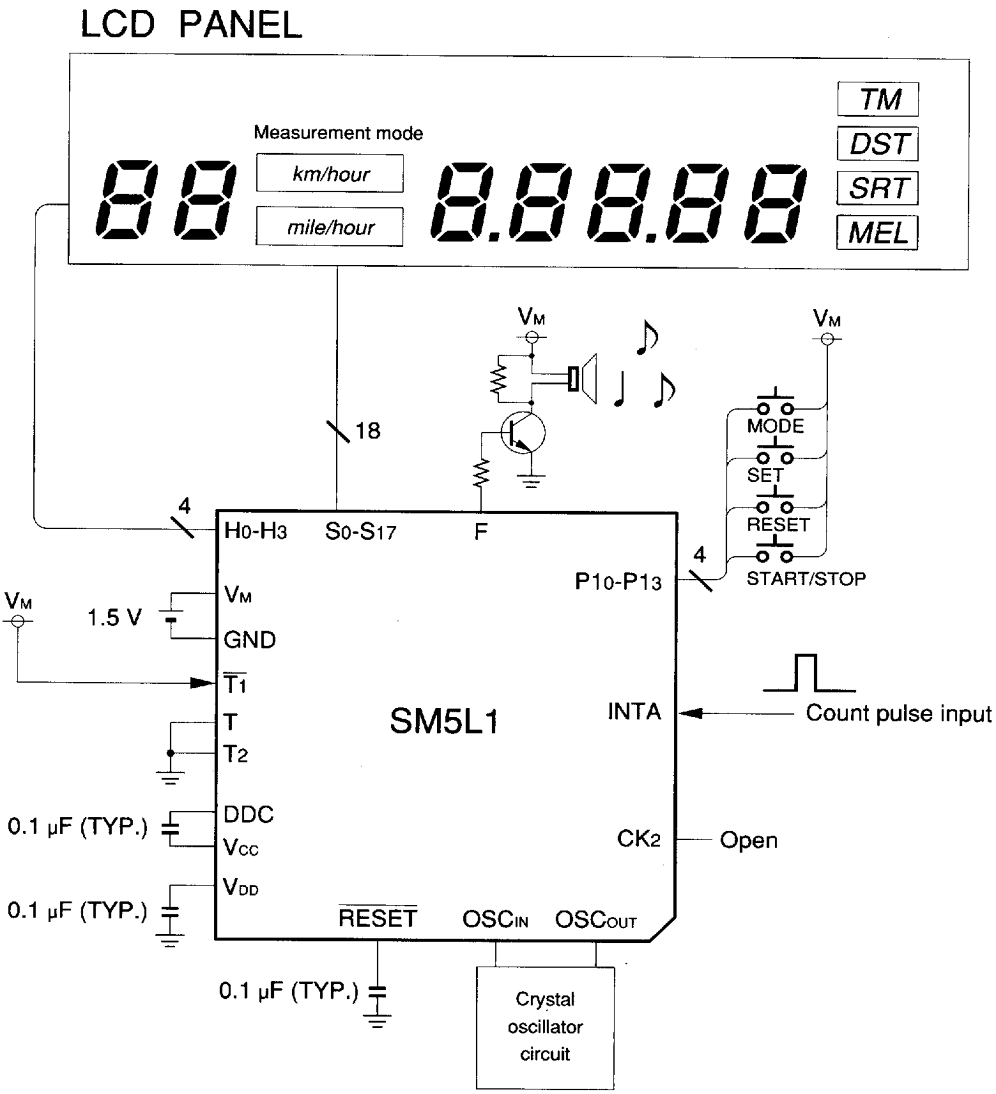
MNEMONIC	MACHINE CODE	OPERATION
Test Instructions		
TAM	6F	Skip if Acc = M
TC x	6E	Skip if C = 1
TM	48 to 4B	Skip if Mi = 1 (i = 3 to 0)
TABL	6B	Skip if A = B_L
TPB x	4C to 4F	Skip if P (R) i = 1 (i = I_1, I_0)
TA	6C	Skip if IFA = 1, and (IFA ← 0)
TD	69 02	Skip if IFD = 1, and (IFD ← 0)
Bit Manipulation Instructions		
SM x	44 to 47	Mi ← 1 (i = 3 to 0)
RM x	40 to 43	Mi ← 0 (i = 3 to 0)
SC	61	c ← 1
RC	60	c ← 0
IE	63	IME ← 1
ID	62	IME ← 0
I/O Control Instructions		
INL	70	Acc ← P1i (i = 3 to 0)
OUTL	71	P0i ← Acc (i = 3 to 0)
ANP	72	Pj ← Pj ∩ Acc (j = 3 to 0)
ORP	73	Pj ← Pj ∪ Acc (j = 3 to 0)
IN	74	Acc ← Pj (j = 3, 2, 1)

OUT	75	Pj ← Acc (j = 3 to 0)
		Rj ← Acc (j = F to D)

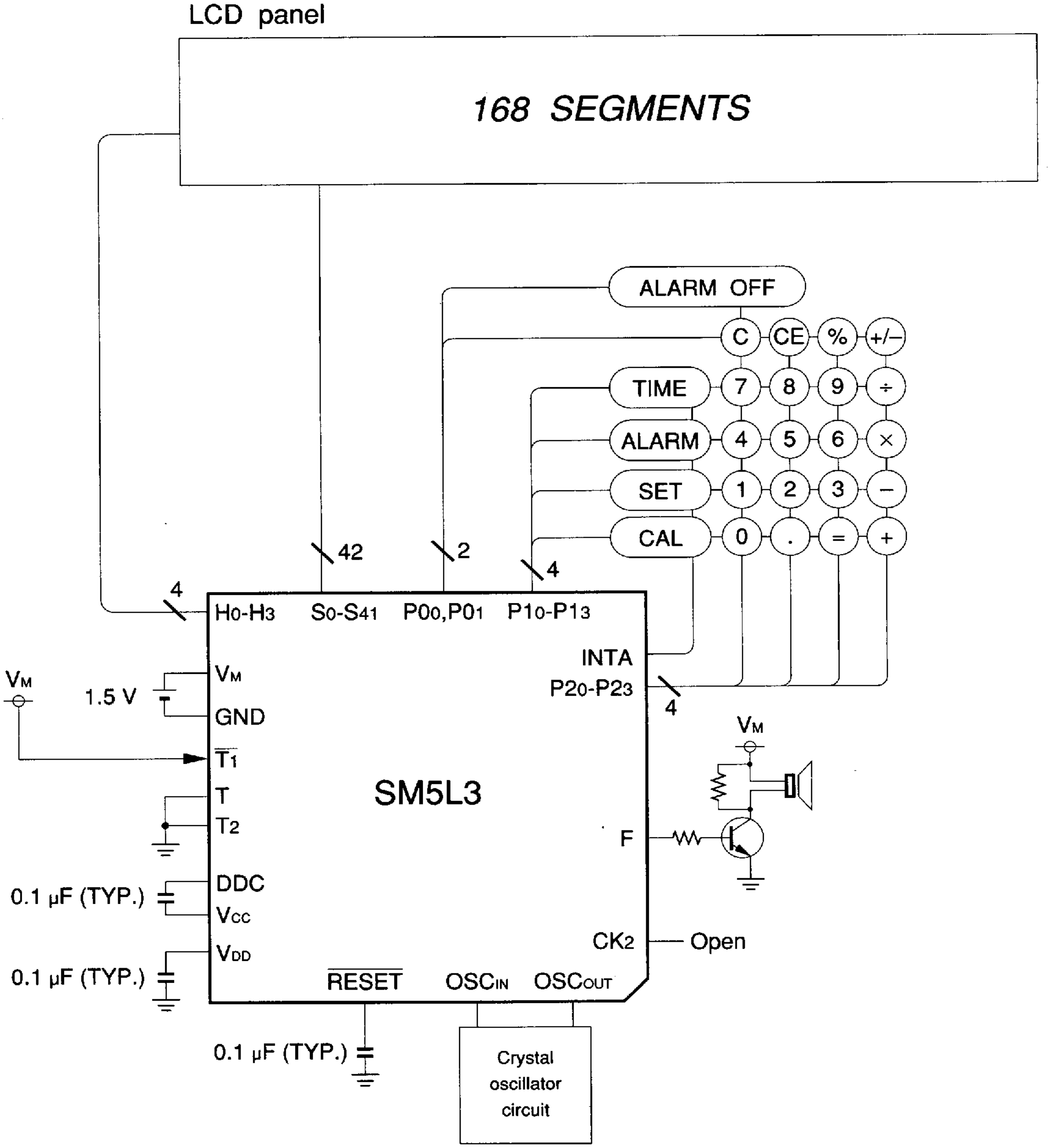
Table Reference Instructions		
PAT	6A 00 to FF	Push P_U ← (0, 4), P_L (X_1, X_0, Acc) (X, Acc) ← I_7-I_0 Pop
Divider Instructions		
DR	69 03	DIV (f_7-f_0) Reset
DTA	69 04	Acc ← Divider (f_3 to f_0)
Melody Control Instructions		
PRE	6B	Melody ROM pointer preset Melody ROM pointer ← X, A
Special Instructions		
STOP	76	Standby mode (STOP)
HALT	77	Standby mode (HALT)
NOP	00	No operation

SYSTEM CONFIGURATION EXAMPLE

- **Sports watch**



- **Watch and calculator**


LCD panel
168 SEGMENTS
ALARM OFF
C
CE
%
+/–
TIME
7
8
9
÷
ALARM
4
5
6
×
SET
1
2
3
–
CAL
0
.
=
+
4
42
2
4
H0-H3
S0-S41
P00,P01
P10-P13
INTA
P20-P23
4
VM
1.5 V
VM
GND
T1
T
T2
SM5L3
F
VM
0.1 μF (TYP.)
DDC
VCC
VDD
0.1 μF (TYP.)
CK2
Open
RESET
OSCIN
OSCOUT
0.1 μF (TYP.)
Crystal oscillator circuit