Circuit Design of Voltage Mode Center of Gravity Defuzzifier in CMOS Process

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***Abstract*—In this paper a voltage input-output center of gravity (COG) defuzzifier circuit is designed without using divider in CMOS 0.35 µm process. We have used transconductance amplifier (TCA) structure as a multiplier with voltage-input - current-output for implementation of defuzzifier by exploiting of voltage follower aggregation principle. Good results have been obtained from the point of accuracy and speed.**

***Keywords*—Center of Gravity Defuzzifier; Transconductance Amplifier; Voltage Follower Aggregation Principle**

I. INTRODUCTION

With fuzzy operational development in recent decades need for systems that expose fuzzy operations with better quality, has received great increase. Herein hardware and circuit realization is very important because it has higher speed and lower power consumption making it suitable for real time applications.

Analog circuits are main candidates for making fuzzy systems because in contrast to their digital counterparts they have superiorities such as higher speed and lower power consumption. Further, fuzzy systems are not generally very accurate systems so lower accuracy of analog circuits is less important. In addition, implementation of COG defuzzifier by digital multipliers and dividers needs large chip area, making analog approaches more preferred.

In this paper an analog circuit is proposed in CMOS 0.35 µm process that converts fuzzy quantities to crisp output. To perform defuzzification we have used COG method that is the most useful and proper way in the most cases. The circuit is made in voltage mode because communication with sensors and auxiliary devices needs that fuzzy system works with voltage input-output and for the same reason working in voltage mode does not need to V-I (voltage to current) and I-V circuits.

Many defuzzifier circuits have been proposed by use of normalization loops [1, 2]. They have the problem that only effect of dominant inputs is calculated correctly [2]. Some approaches have used multiplier-divider structures [3, 4]. Here circuit designing based on voltage follower aggregation principle has the form that does not need the divider. This is an important advantage along with simplicity and less chip area.

The rest of the paper is organized as follows. In section II, theory of the circuit operation is presented. In section III, defuzzifier circuit is proposed. In section IV, results of simulations are shown. Finally, section V concludes the paper. All the circuit simulations have been performed by Hspice level 49 software.

II. FORMULATION

The formula of COG method for discrete inputs is according to (1).

$$z^* = \frac{\sum \mu_i \times z_i}{\sum \mu_i} \quad (1)$$

where μ (inference voltage) is a coefficient for z (consequent voltage) and z^* is output crisp value. Now, if we use a multiplier circuit that takes two input voltages and gives product in current form, we can realize (1) by connecting outputs of all multipliers according to Fig. 1.

With noticing to Fig. 1 difference of V_{out} and V_zs is multiplied with V_μ signals in TCA circuit, and results of multiplication operations enter to V_{out} node in the current form. Mathematical proof based on KCL is described in the following:

$$\sum_{i\in G(i)} I_i = \sum_{i\in G(i)} (z_i - out) \times \mu_i = 0 \rightarrow out \times \sum_{i\in G(i)} \mu_i = \sum_{i\in G(i)} z_i \times \mu_i \rightarrow out = \frac{\sum_{i\in G(i)} z_i \times \mu_i}{\sum_{i\in G(i)} \mu_i} \quad (2)$$

where *out* is output voltage, I_i is product of (z_i-*out*) and μ_i voltages in the current form, and $G(i)$ is the set of all TCA circuits.

As mentioned before, we have used transconductance amplifier (TCA) for multiplier circuit as its output current is defined as:

$$I_{diff} = V_{diff} \times \sqrt{2 \times K \times I_T - K^2 \times V_{diff}^2} \quad (3)$$

where K=0.5×μ×C_{ox}, V_{diff} is differential voltage, and I_T is differential pair's tail current. Now, if I_T be current of a transistor in saturation region so it is related to square of gate-source voltage. Thus, these voltages are same as V_μs in the Fig. 1 by a coefficient which is multiplied to V_{diff}, considering:

$$I_{diff} = C \times V_{diff} \times V_\mu \quad (4)$$

where C is a constant. We deduce (5) based on (2) and (4).

$$V_{out} = \frac{\sum_{i\in G(i)} V_{zi} \times V_{\mu i}}{\sum_{i\in G(i)} V_{\mu i}} \quad (5)$$

We see that the output voltage gives crisp quantity as a result of (1).

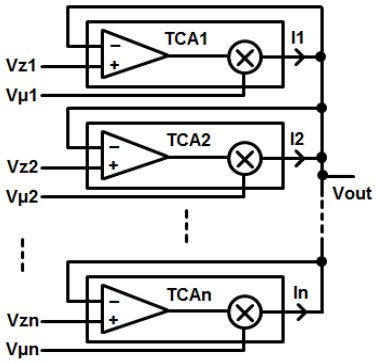

Fig. 1. General schema of the defuzzifier

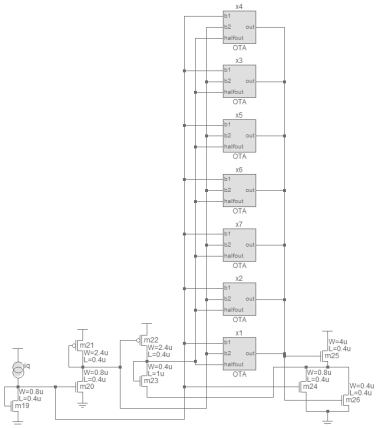

Fig. 2. Block diagram of each multiplier incorporated to central circuit of the defuzzifier

III. DEFUZZIFIER CIRCUIT

The proposed defuzzifier works with singleton consequent values which it contains seven (or any other number which is needed) TCA multipliers in addition to a central circuit, as shown in Fig. 2. The central circuit contains bias, voltage attenuator, and voltage level shifter circuits. In Fig. 3, TCA multiplier is into the frame and out of frame transistors are system's central circuit connected to every seven multipliers.

In (3), expression $K^2 \times V_{diff}^2$ is a nonlinear factor and to cancel it voltage attenuator (M13, M14, M24, M25) is used for V_z and V_{out} voltages that enter to differential pairs. In this way that by attenuation of these two voltages, V_{diff} is decreased and as a result nonlinearity will be reduced.

On the other hand, by using Gilbert structure (M1, M2, M3, M4, M7, M8) the formula of TCA's output current is changed as:

$$I_{diff} = V_{diff} \times \left(\sqrt{2 \times K \times I_{T1} - K^2 \times V_{diff}^2} - \sqrt{2 \times K \times I_{T2} - K^2 \times V_{diff}^2}\right) \quad (6)$$

V_b is a little more than V_{th} (threshold voltage of MOS transistors). Transistor M8 almost is off for large V_μs (i.e. large I_{TI}) and just a differential pair will be on. Great I_{TI} causes nonlinear factor be less effective in (3) and for decreasing power consumption we have not need to use Gilbert format. On the other hand, when V_μ is low, transistor M8 starts to work with low current and according to (6) linearization will be done by cancelling the nonlinear factors of two differential pairs. In this state of low I_T currents, nonlinear factor has more effect and for this reason Gilbert format is used in this condition.

For increasing speed, current amplifiers (M5, M6, M9, M10, M11, M12) is used which for limitation of power consumption, transistors M9 and M11 have less currents in contrast to M10 and M12.

Transistors M18, M19, and M20 are for biasing of the circuit. Transistors M15, M16, M17, M21, M22, and M23 are voltage level shifter circuits that placed for differential pair's biasing. They are designed in order to have small influence of input voltages on them and also in the purpose of voltage increase that they produce always be equal to a number.

Current source I_q is assumed to be 12 μA. The circuit has a 3.3 V power supply (Vdd). Channel length and width of transistors are shown in Table I. Layouts of multiplier cell and complete defuzzifier circuit are shown in Fig. 4 and Fig. 5, respectively. Also dimensions of defuzzifier circuit (Fig. 5) are 114×90 μm^2.

IV. SIMULATION RESULTS

Results of the simulation with Hspice software at input voltage range from 0 V to 1.2 V for V_μ and from 1 V to 1.9 V for V_z are shown in the next figures.

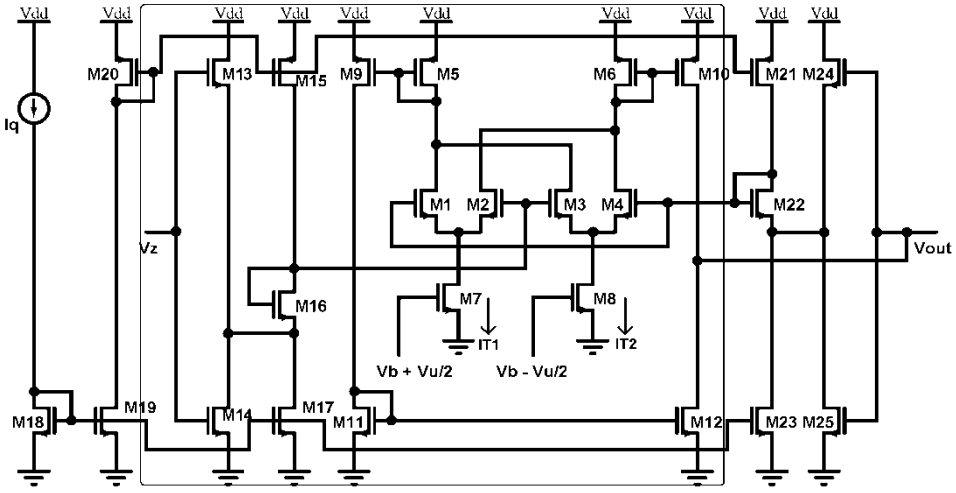

Fig. 3. Multiplier circuit along with the central circuit

Seven quantities of V_z are assumed with equal 150 mV distances at input voltage range. Outputs of defuzzifier while dc sweeping V_μ (when other V_μs in each sweep are zero) for each seven quantities of V_z, are shown in Fig. 6.

Table I. Channel length and width of transistors

Transistor	W(μm)	L(μm)
M1-M4, M11	1	0.4
M5, M6, M9	3	0.4
M7, M8, M12	2	0.4
M10	6	0.4
M13, M24	4	0.4
M14, M25	0.4	0.4
M15, M20, M21	2.4	0.4
M16, M22	0.4	1
M17-M19, M23	0.8	0.4

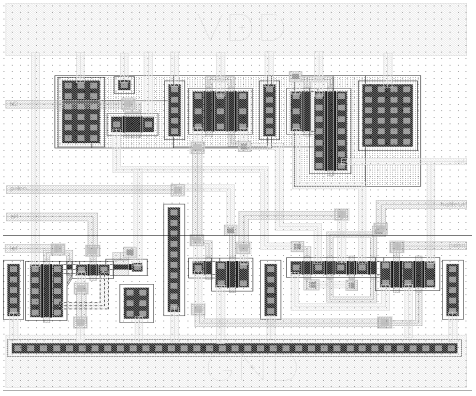

Fig. 4. Layout of the multiplier cell

Fig. 5. Layout of the total defuzzifier circuit

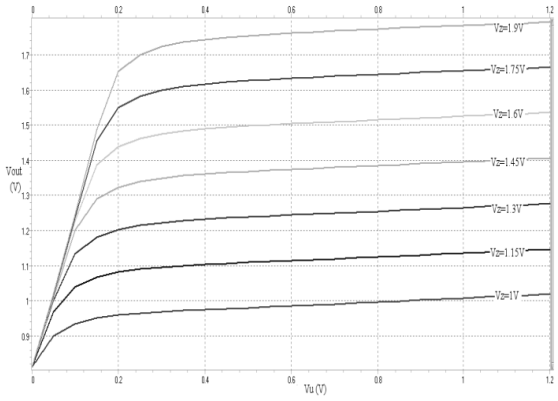

Fig. 6. Defuzzifier output as V_μ swept for every seven values of V_z

As illustrated, for values of V_μ greater than 0.2 V, defuzzifier operates accurately. Also for some quantities of inference voltages (V_μ) output, output error, and power consumption diagrams are shown. In two examples, we have employed two pulses for each inference voltage, which their values are illustrated in Table II.

Fig. 7, Fig. 8, and Fig. 9 indicate output, output error, and power consumption of the circuit for first pulse, respectively. Power consumption of the whole defuzzifier circuit at its maximum value (i.e. all V_μs be equal to 1.2 V) is equal to 8.917 mW. Actually if we limit input range to 0.6 V, power consumption will be equal to 3.61 mW in the worst condition. Therefore if we want to have low power consumption we can decrease input range.

Table II. Two pulse shape examples of V_μ

	First pulse		Second pulse	
	Level 2	Level 1	Level 2	Level 1
$V_{\mu1}$ (v)	1.2	1.2	0.15	0.85
$V_{\mu2}$ (v)	1.1	1.2	0.85	1.2
$V_{\mu3}$ (v)	0.9	1.2	1.0	0.3
$V_{\mu4}$ (v)	0.6	1.2	0.6	0.25
$V_{\mu5}$ (v)	0.4	1.2	0.35	0.0
$V_{\mu6}$ (v)	0.1	1.2	0.4	0.7
$V_{\mu7}$ (v)	0.2	1.2	1.1	0.65

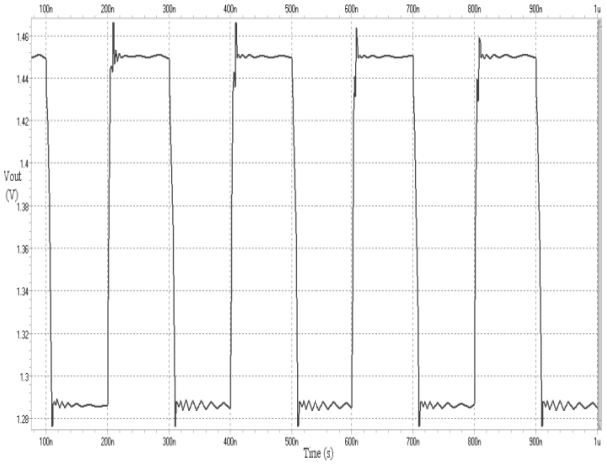

Fig. 7. Output of first pulse

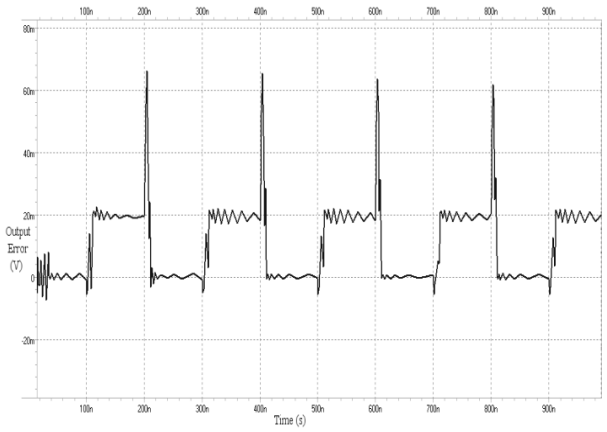

Fig. 8. Output error of first pulse

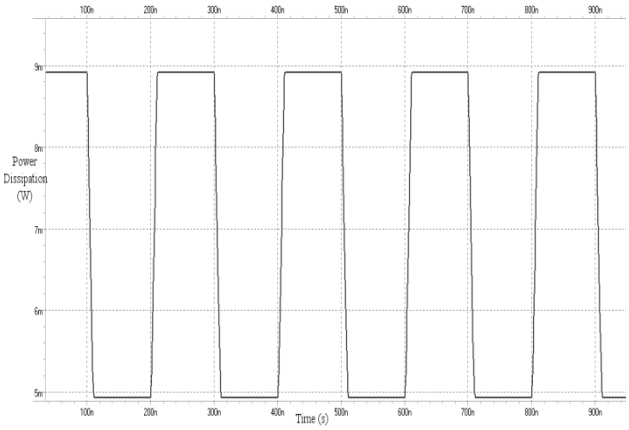

Fig. 9. Power dissipation of first pulse

In Fig. 8 the error is 200 µV and 19 mV in two levels. Outcome related to second pulse is depicted in Fig. 10 and Fig. 11. Output error of the second pulse is between 14 mV and -16 mV and power consumption is between 4.48 mW and 4.85 mW.

Frequency of the input pulses was 5 MHz and the proposed circuit has ability to work with higher frequencies. A dc sweep analysis is performed in corners ss, sf, fs, ff and temperatures 125 ^{o}C, 0 ^{o}C for $V_{\mu 5}$ (V_{μ} for singleton with V_z=1.6 V) that obtained results are shown in Fig. 12.

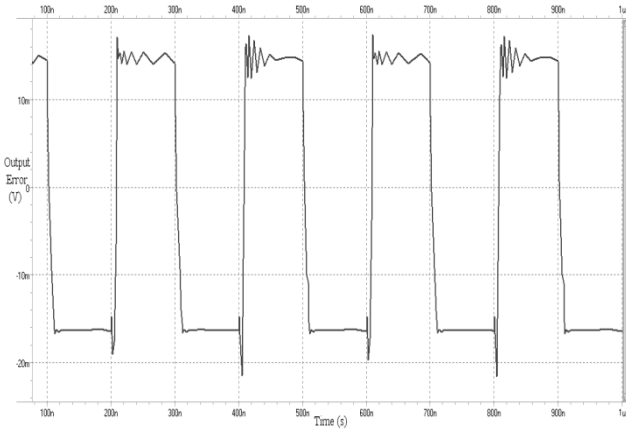

Fig. 10. Output error of second pulse

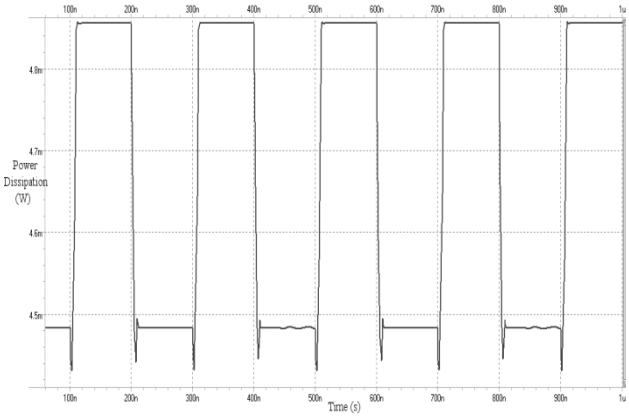

Fig. 11. Power dissipation of second pulse

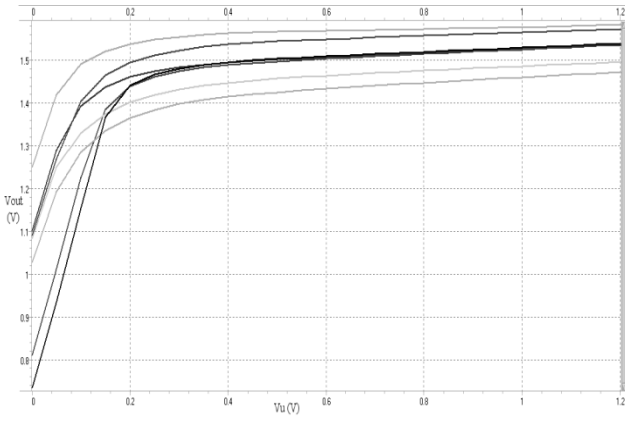

Fig. 12. Sweep of $V_{\mu 5}$ in different corners and temperatures

At last to compare the proposed circuit with other works, Table III demonstrates inaccuracy of the proposed circuit and that presented in [5] for some inputs. In Table III, step of consequent singletons related to our work is 225 mV (V_z voltages are 1, 1.225, 1.45, 1,675, and 1.9 volts) and in [5] consequent voltages are 0, 1, 2, 3, 4, and 5 volts.

Table III. Comparison between the proposed circuit and [5]

Examples	$V_{\mu 1}$ (v)	$V_{\mu 2}$ (v)	$V_{\mu 3}$ (v)	$V_{\mu 4}$ (v)	$V_{\mu 5}$ (v)	((Error)/(step of V_zs))%	
						Our work	[5]
Example 1	0.5	0.5	1	1	0.5	14.8	24.6
Example 2	1	1	1	1	1	3.4	0
Example 3	0.5	0	1	0.5	0	10.2	25
Example 4	0.1	0.3	0.5	0.7	1	23.6	69.78
Example 5	0.9	0.7	0.5	0.3	0	4.7	48.3

V. CONCLUSIONS

The proposed defuzzifier circuit is a novel work with improved functionality. It has been implemented in CMOS 0.35 µm process and also its layout was presented. Good results from the point of accuracy and speed have been obtained. Compared to [5] error of the proposed circuit show notable improvement. The proposed defuzzifier is practical for producing crisp output in all voltage mode fuzzy systems.

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