# RAM

# COMP 273 Assignment 5 – Fall 2021

**Due: February 4, 2021, at 4 PM on myCourses**

## Submission instructions

All work must be your own and must be submitted to myCourses. Include your name and student number in a comment at the top of your documents / Logisim circuits. **Submit only one file: a5.circ**. Do not use a zip archive. Check your submission by downloading it from myCourses and checking that it was correctly submitted. You will not receive marks for work that is incorrectly submitted.

## Purpose

- Learning about the basic circuitry in the RAM
- To get used to using flip-flops
- To get used to using addresses
- To get used to splitting and merging signals
- To learn that we need to respect the direction of a signal



## Helpful

- Tutorial E should be completed before you start this assignment
- The lecture recordings on RAM (two recordings) had the professor draw most of the key circuit components for this assignment (specifically Oct 26 (end) & 28 (beginning)).
- Assuming you have completed Tutorial E, this assignment should take about two days to complete.

## Implementation

Using Logisim Evolution create the circuit for the following problem:

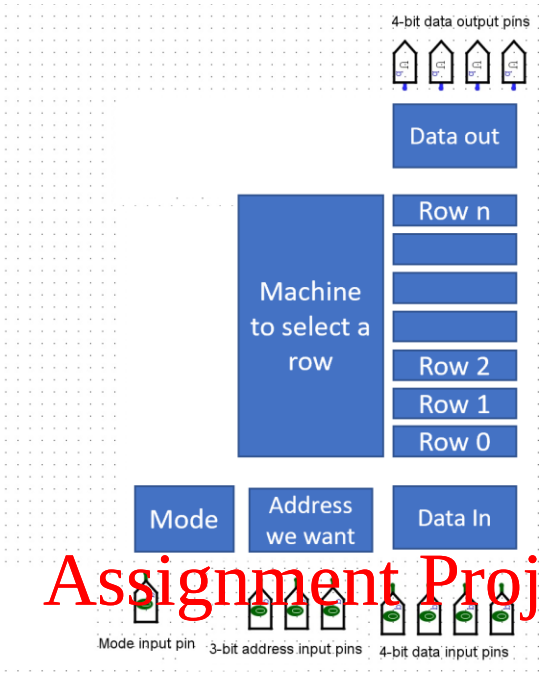


Figure 1: High-level view of RAM



- Task: Build the circuit (blue boxes) of figure 1.
- Inputs: Mode, Address, Data In
- Outputs: Data Out
- Circuits: 8 nibbles of RAM, and row selector circuit, data-in/data-out unidirectional buses

NOTE: Your final circuit does not need to look exactly like figure 1. However, the input and output pins must look like figure 1.

NOTE 2: Your final circuit must use designs we covered during class. You cannot use any outside (other sourced) circuit designs.

## Steps

- Begin by placing the input and output pins onto the circuit. These pins will be used to enter and see values.
- Mode, Address, Data In, and Data Out are registers. Create these registers from scratch using flip-flops. Do not use the Logisim Register pre-built unit. You can pick any flip-flop you want. Group and synchronize the flip-flops for one register as a single unit. As seen in class.
- Row 0 to Row 7 are the eight nibbles of RAM. Also create them from scratch using any flip-flop you want. Do not use the Logisim Byte pre-built unit. Group and synchronize them into units.
- Build the row selector circuit connecting the Address and Mode registers with the Nibbles.
- Use the row selector and Mode register with the Data In and Data out registers (proper read/write gating circuitry).

- Add a clock to control the execution of this circuit.

## Execution

Your RAM circuit must be able to do the following:

1. TA will input an Address and a Data-In value and will place 1 in Mode for write to nibble.
2. TA will turn the clock on to save the information into the nibble.
3. TA will turn the clock off.
4. TA will input an Address and a 0 in Mode to read a nibble to Data Out.
5. TA will turn the clock on to read the information from the nibble into Data Out.
6. The TA will turn the clock off.
7. The TA will then be able to see the Data-Out pins displaying the expected value.
8. The TA should be able to repeat this process as often as they want. Data previously stored in the nibbles should still be present unless they are overwritten.

## Bonus

The following bonus point cannot increase your score beyond 20 points. It is helpful only in two ways: if you lost a point somewhere else you can get an extra point, and it is educational.



- +1 bonus point – merge the Data-In and Data-Out registers into a single register (as it is done in reality). You will need to keep the input and output pins.



## Marking



- Maximum 20 points
  - +1 Mode register
  - +2 Address register
  - +1 Data In register
  - +1 Data Out register
  - +3 Row selector circuit
  - +3 8 nibbles
  - +3 Saves data to nibble
  - +3 Reads data from nibble
  - +3 Repeatable infinitely
- -10% per day late with max 2 late days
- -3 points for not following instructions
- -5 points for not using the clock
- Assignment must execute to be graded