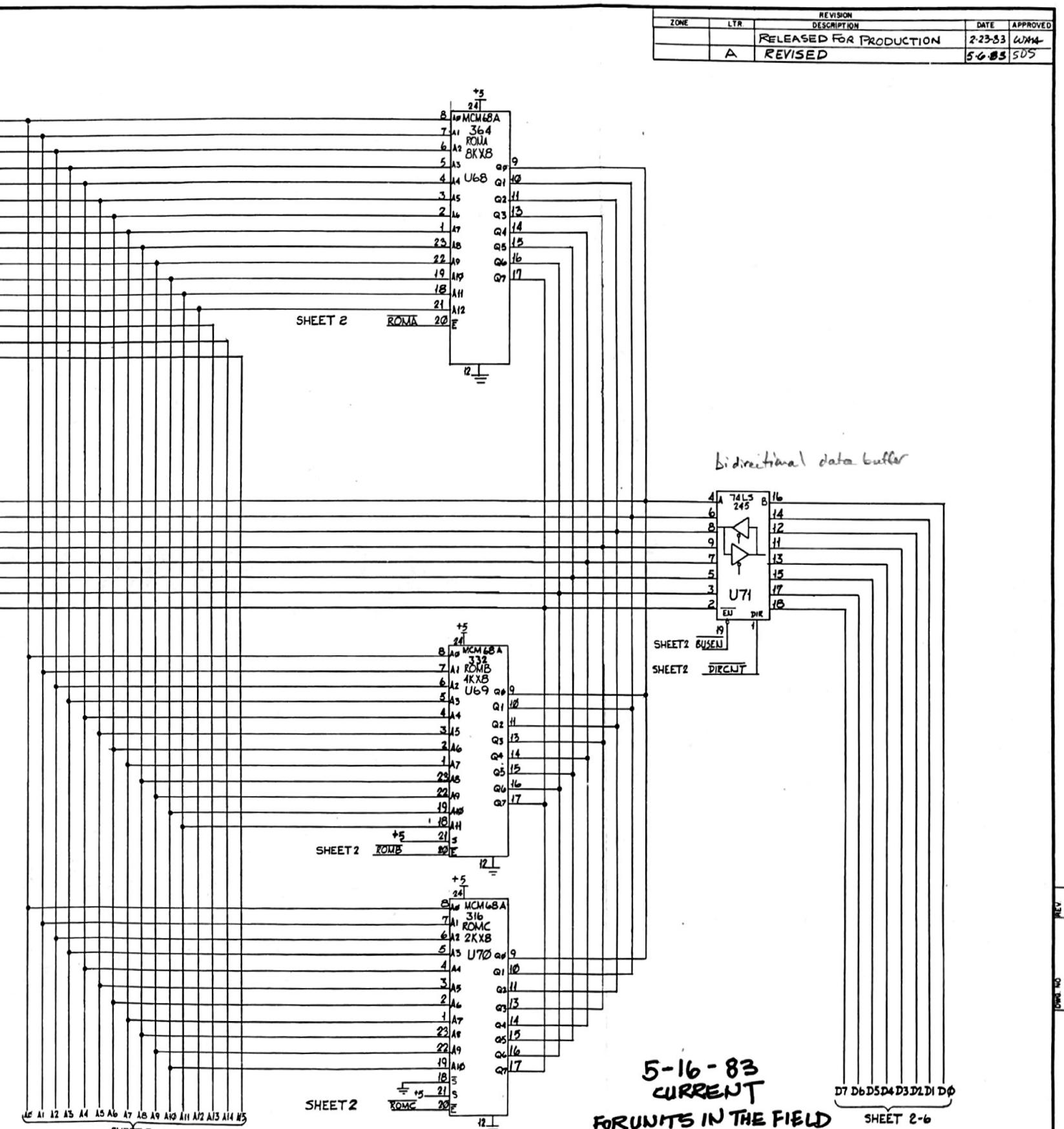


#### CPU, ROM, ADDRESS BUFFERS, AND DATA BUFFER



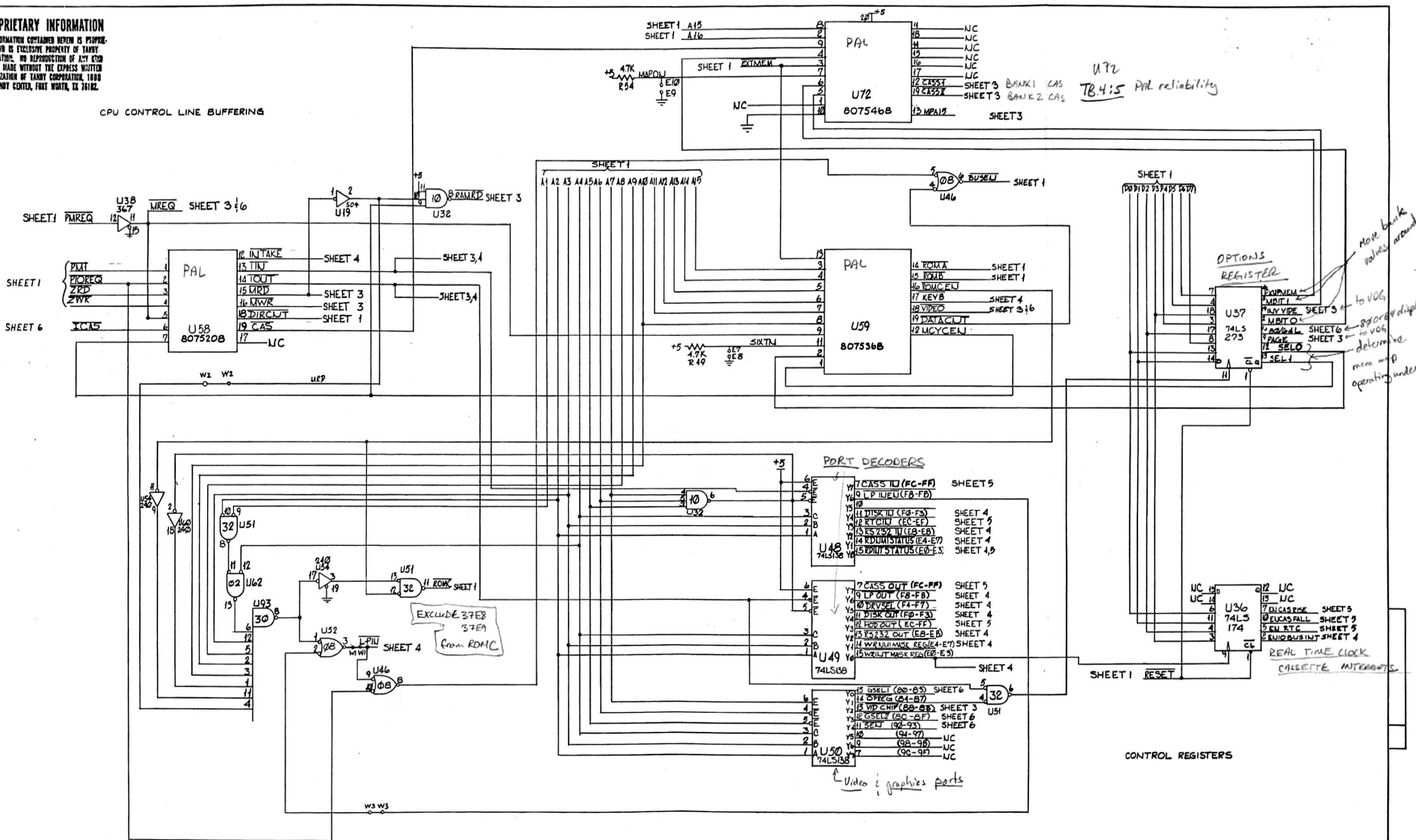
5-16-83  
CURRENT  
FOR UNITS IN THE FIELD

MATERIAL		UNLESS OTHERWISE SPECIFIED		DRAFT S.D.HATFIELD	DATE 11-1-82	TITLE  SCHEMATIC - PROJECT R #471  CPU
		TOLERANCES $.XX = \pm .010$ $XXX = \pm .005$ ANGLES = $\pm 1^\circ$		CHECK GEG	DATE	
		HOLE DIA TOLERANCES $.014 - .250 = + .005$ $.251 - .750 = + .008$ $.751 - UP = + .015$		DESIGN G.E.GAULKE	DATE 2/22/83	
				APPD <i>Murphy D. Brown</i>	DATE 1-23-83	
				APPD <i>W. Harrel</i>	DATE 2/23/83	
		DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING	471			
		DO NOT SCALE THIS DRAWING	NEXT ASSY.	USED ON		

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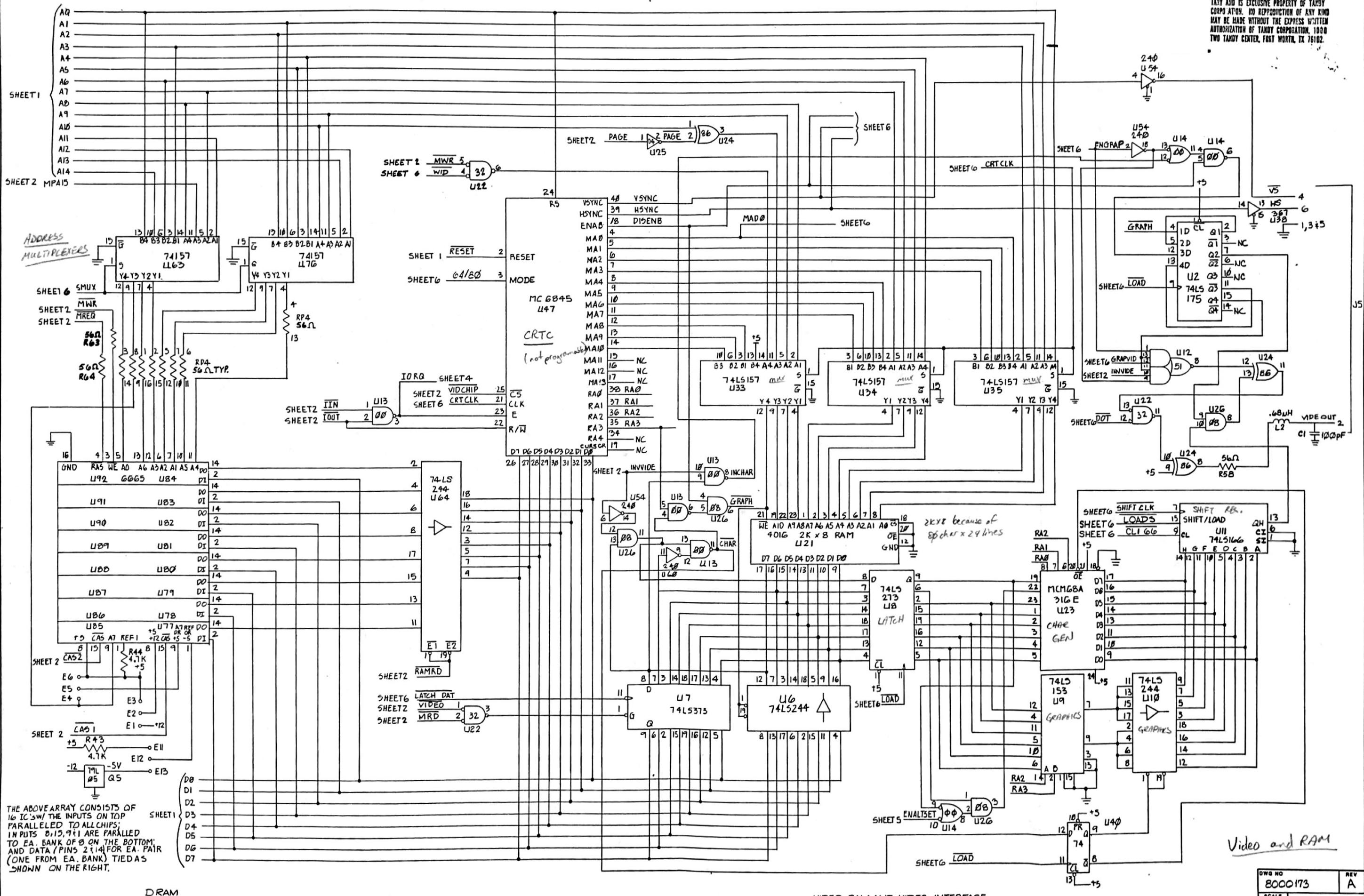
### CPU CONTROL LINE BUFFERING



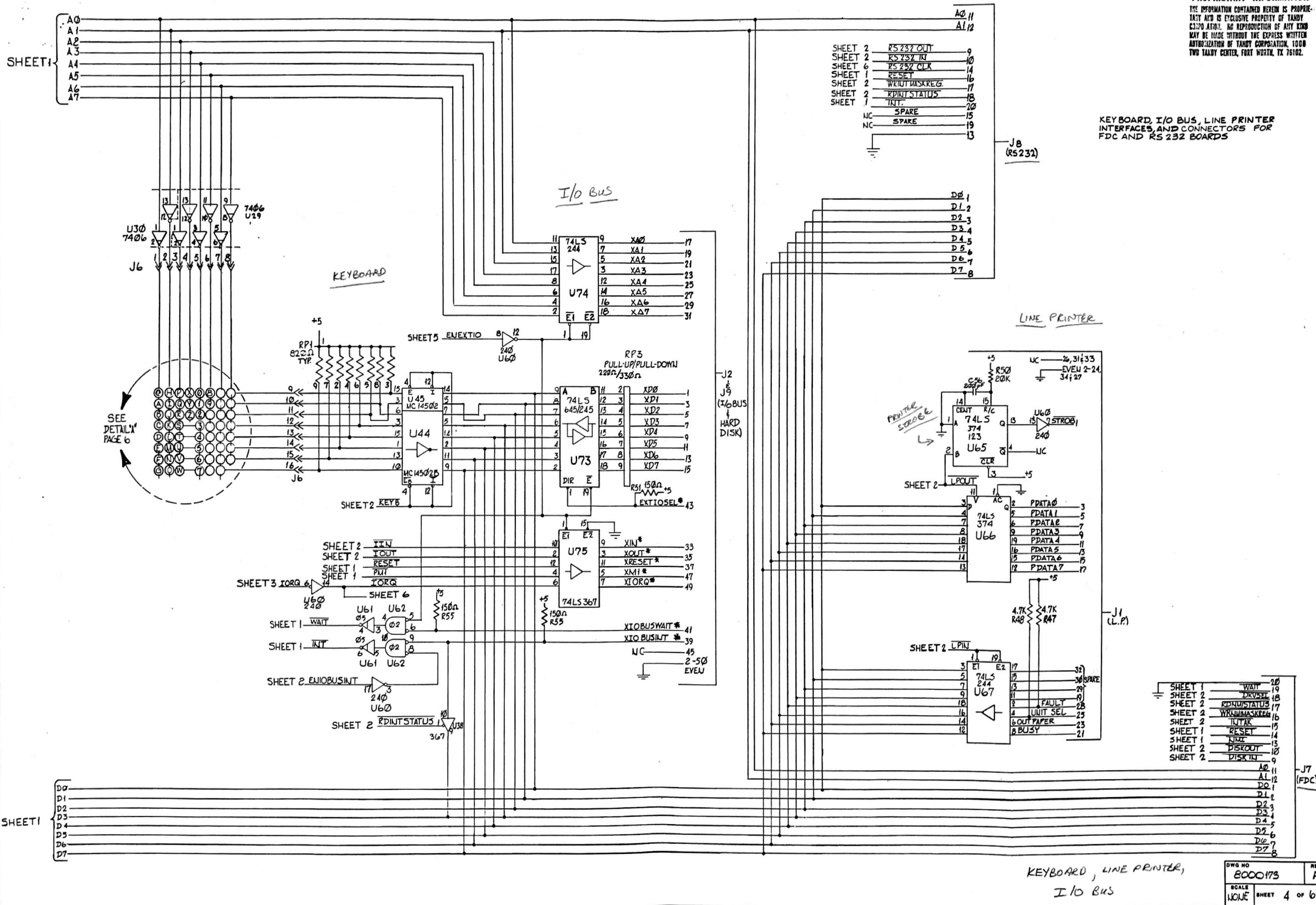
## ADDRESS RECO

## ADDRESS DECODING

DWG NO  
8000173  
REV  
A

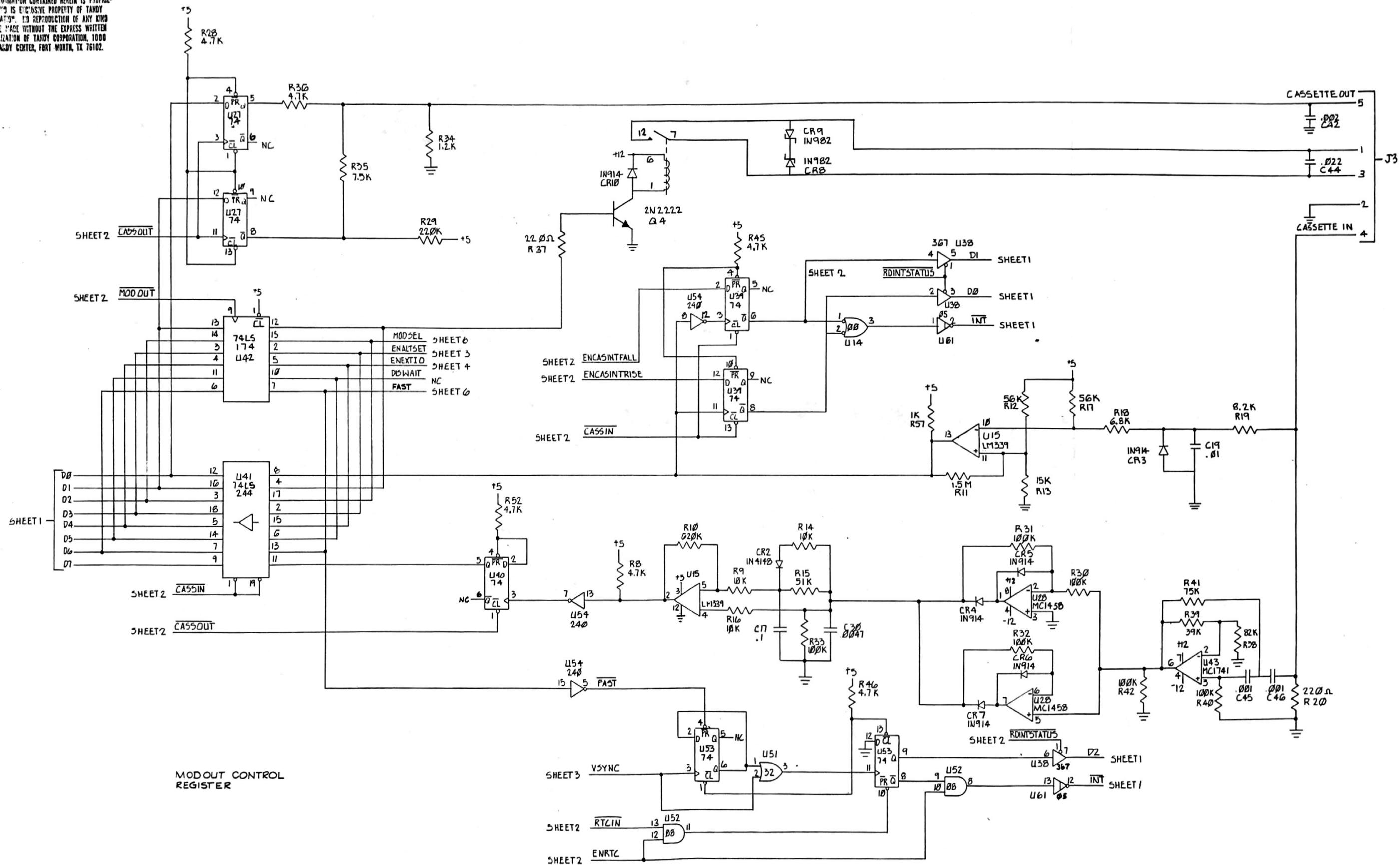


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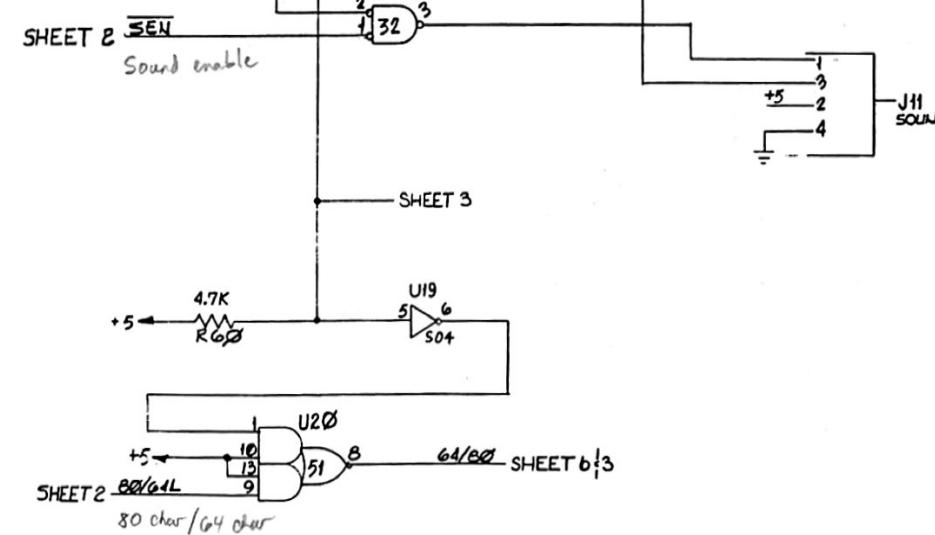
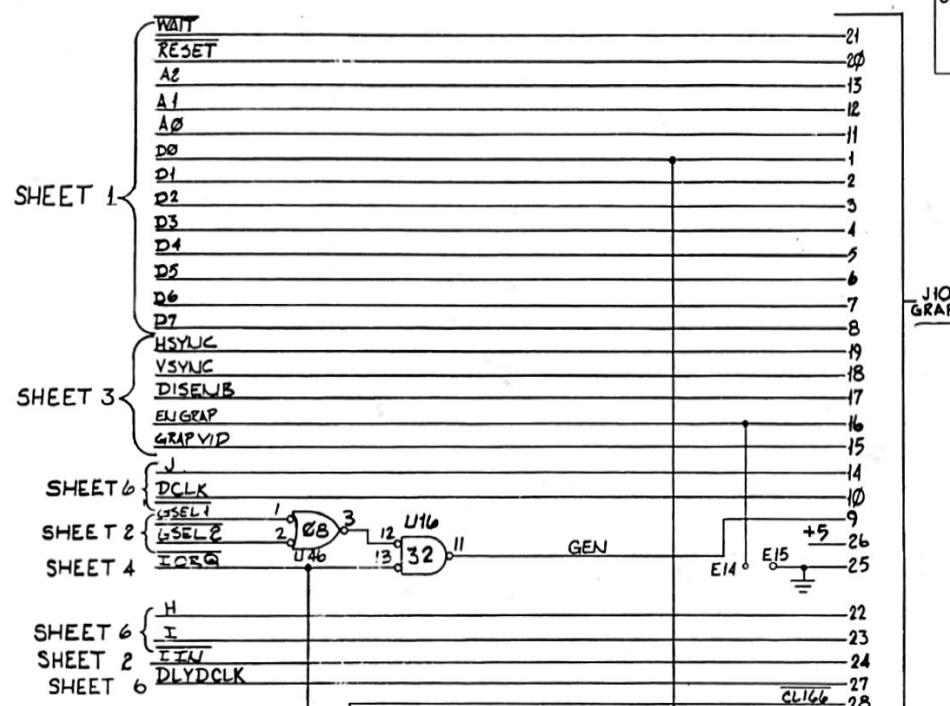


CASSETTE IF,  
MODE SELECT,  
RTC Circuit.

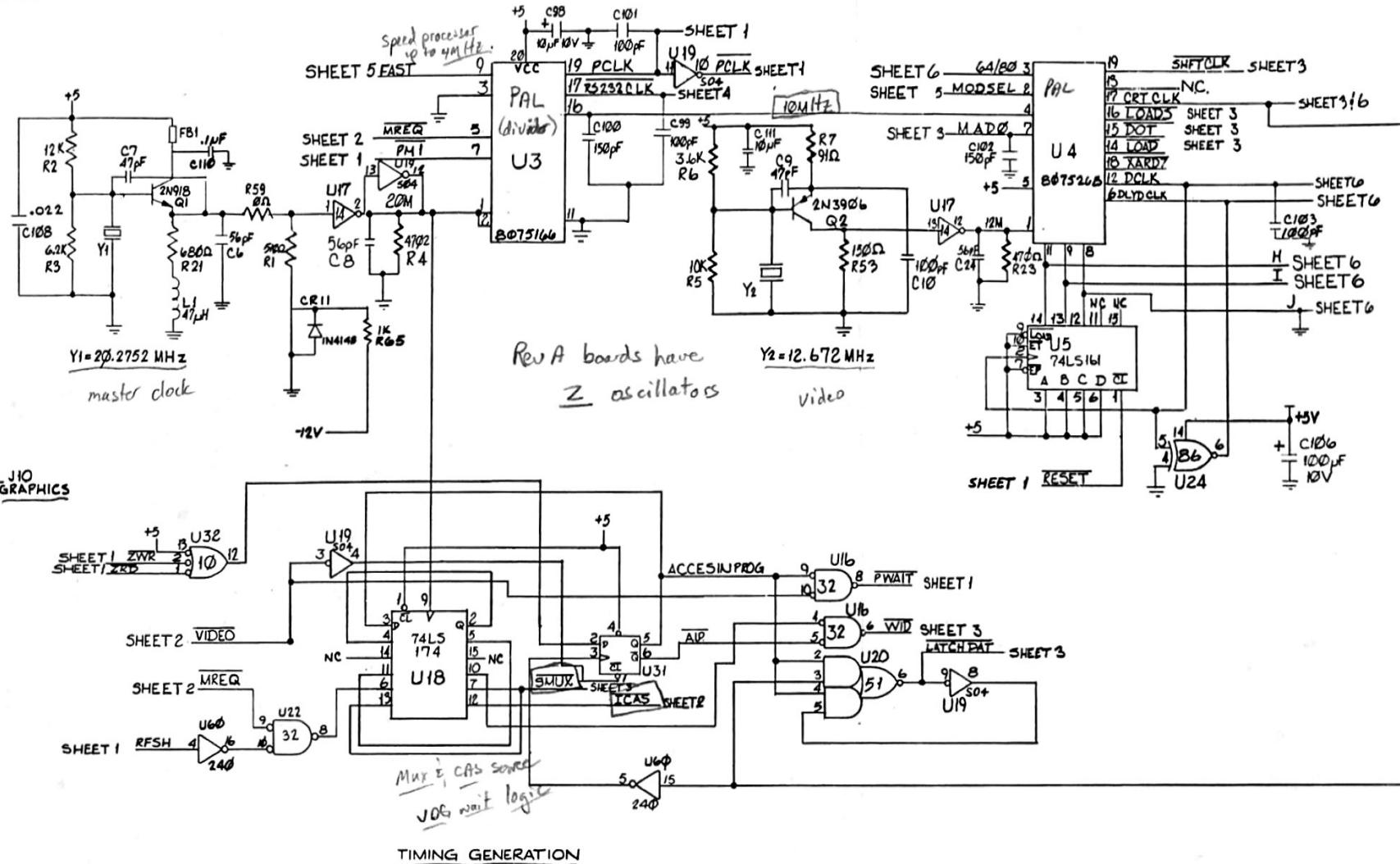
DWG NO	REV	
8000173	A	
SCALE		
NONE	SHEET	5 OF 6

PROPRIETARY INFORMATION

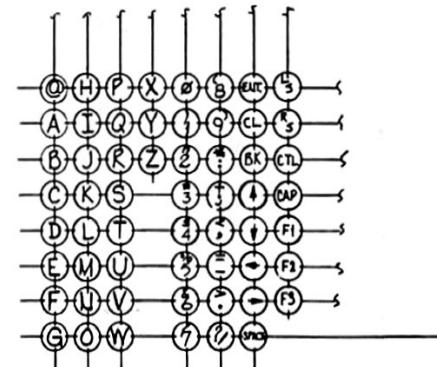
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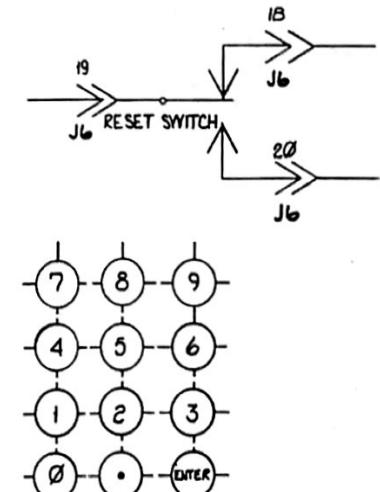
#### **GRAPHICS AND SOUND BOARD CONNECTORS**



## TIMING GENERATION



DETAIL "A"  
FROM PAGE 4



THE ABOVE KEYS (THE NUMERIC KEYPAD) ARE CONNECTED IN PARALLEL WITH SIMILAR KEYS OF THE KEYBOARD MATRIX.

#### KEYBOARD DETAIL