

Radio Shack®

Service Manual

TRS-80®

65-Watt Switching Power Supply

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1/ SYSTEM DESCRIPTION

Basic Principle

A switching power supply circuit employs a high-speed semiconductor switch to control the storage and release of electrical energy in an inductor and provide regulated DC output voltages with a minimum loss of energy in heat-dissipating elements. There are several schemes for achieving this result which differ primarily in the arrangement of the basic circuit elements. These elements include a switch, an inductor, a rectifier, a capacitor and a DC voltage source.

An arrangement well-suited for economical power supplies with rated power outputs under 100 watts is the FLYBACK CONVERTER shown in Figure 1. The waveforms in Figure 2 are used to describe the operation of the Flyback Converter circuit. For the purpose of this discussion we will assume that the duration of the "ON" time equals the duration of the "OFF" time.

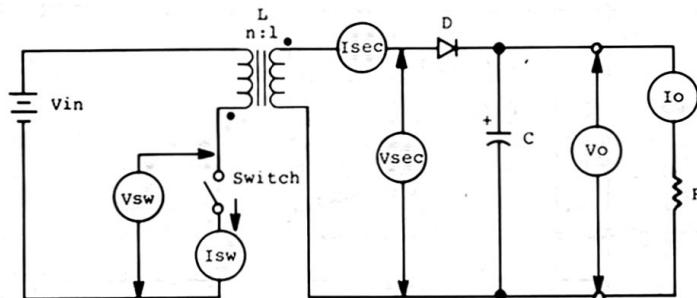


FIGURE 1. BASIC FLYBACK CONVERTER

When the switch is closed (ON) at time t_a , V_{in} is impressed across the primary winding of inductor L and the current I_{sw} increases linearly from zero until the switch opens (OFF) at time t_b . Note that I_{sec} is zero while the switch is closed. This is because V_{sec} is negative with respect to V_o thus reverse-biasing diode D . Note that V_{sw} is also zero while the switch is closed.

When the switch opens at time t_b , the magnetic field of L instantly collapses and reverses polarity. At this moment, V_{sw} is equal to V_{in} plus the voltage across L just before

the switch opened (also equal to V_{in}). Therefore, at the instant the magnetic field reverses polarity, $V_{sw} = 2V_{in}$.

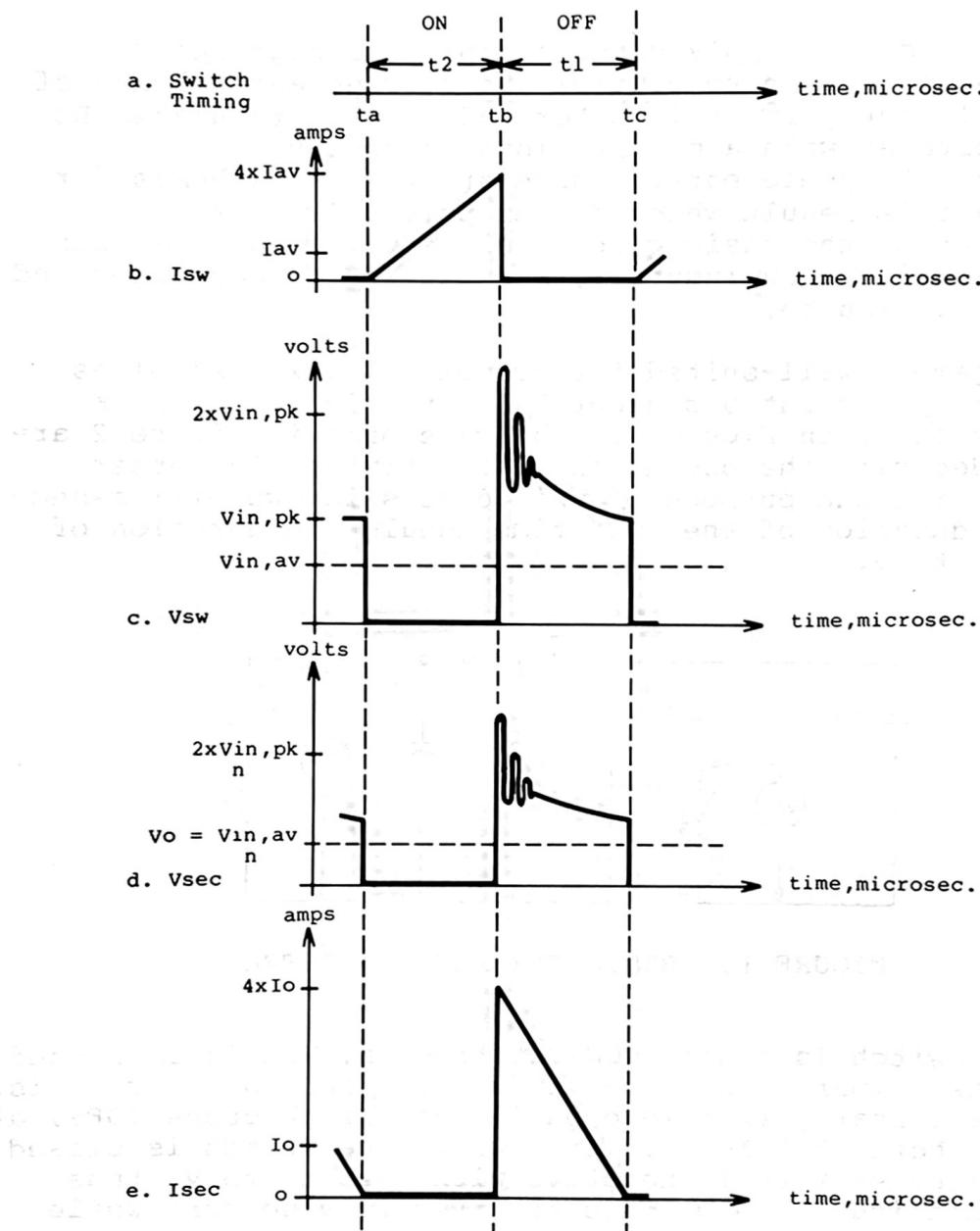


Figure 2. Waveforms for Figure 1.

During the interval when the switch is open (t_b to t_c), the secondary voltage, V_{sec} , is a replica of the primary voltage V_{sw} . Diode D is now forward biased due to the polarity of the inductor windings and because the turns ratio, n , is such that:

$$V_{sec} \times n > V_o$$

This biasing replenishes the charge in capacitor C that was delivered to the load R during the t_a - t_b interval. This is the "flyback" interval and is so named because the inductor releases the energy stored in its magnetic field while the switch is OFF.

Several other facts are illustrated by the waveforms of Figure 2. First, the voltage across the switch V_{sw} decays exponentially from $2V_{in}$ to V_{in} during the "OFF" interval. This is because the inductor and the switch timing are adjusted to transfer all of the energy that was stored in the inductor while the switch was ON, into the secondary while the switch is OFF. (Observe that I_{sec} DECREASES linearly with time to zero at the end of the "OFF" time period.) This is known as resetting the core. Thus, at time t_c when the switch is ready to turn on again, the DC input voltage V_{in} is again available to charge the inductor. Also at this time, all currents in the inductor are zero.

Second, since we have assumed that I_{sw} increases linearly with time and that the ON and OFF time periods are equal (50% duty cycle), the average current in the primary, I_{sw} (av), is 1/4 the peak current I_{sw} . Also, the average current in the secondary, which is equal to the load current I_o , is 1/4 the peak current in the secondary.

Third, the turns ratio is set by the ratio of the average primary voltage (V_{sw}) over a full cycle at its lowest value to the maximum permissible output voltage, V_o . The lowest V_{sw} value occurs at low AC line and maximum output load. In practice, the actual turns ratio, the ratio of peak-to-average voltages and currents, and the duty cycle may be adjusted to compensate for circuit losses.

Fourth, notice the ringing or oscillation that appears on the peak portion of V_{sw} and V_{sec} . This oscillation occurs at the resonant frequency of the leakage inductance of the inductor L and the parasitic capacitance of the circuit. The parasitic capacitance includes the interwinding capacitance of the inductor and stray capacitance of the switch. If this oscillation is not damped by a suitable means, the peak voltages may easily exceed the breakdown rating of the switch or the insulation in the inductor.

Block Diagram

The basic circuit illustrated in Figure 1 can be divided into three functional blocks: Input DC supply, primary, and secondary. To make use of this model, we need to expand it to provide control for the switch timing and to include sufficient circuitry to satisfy performance and reliability specifications. The complete block diagram is shown in Figure 3.

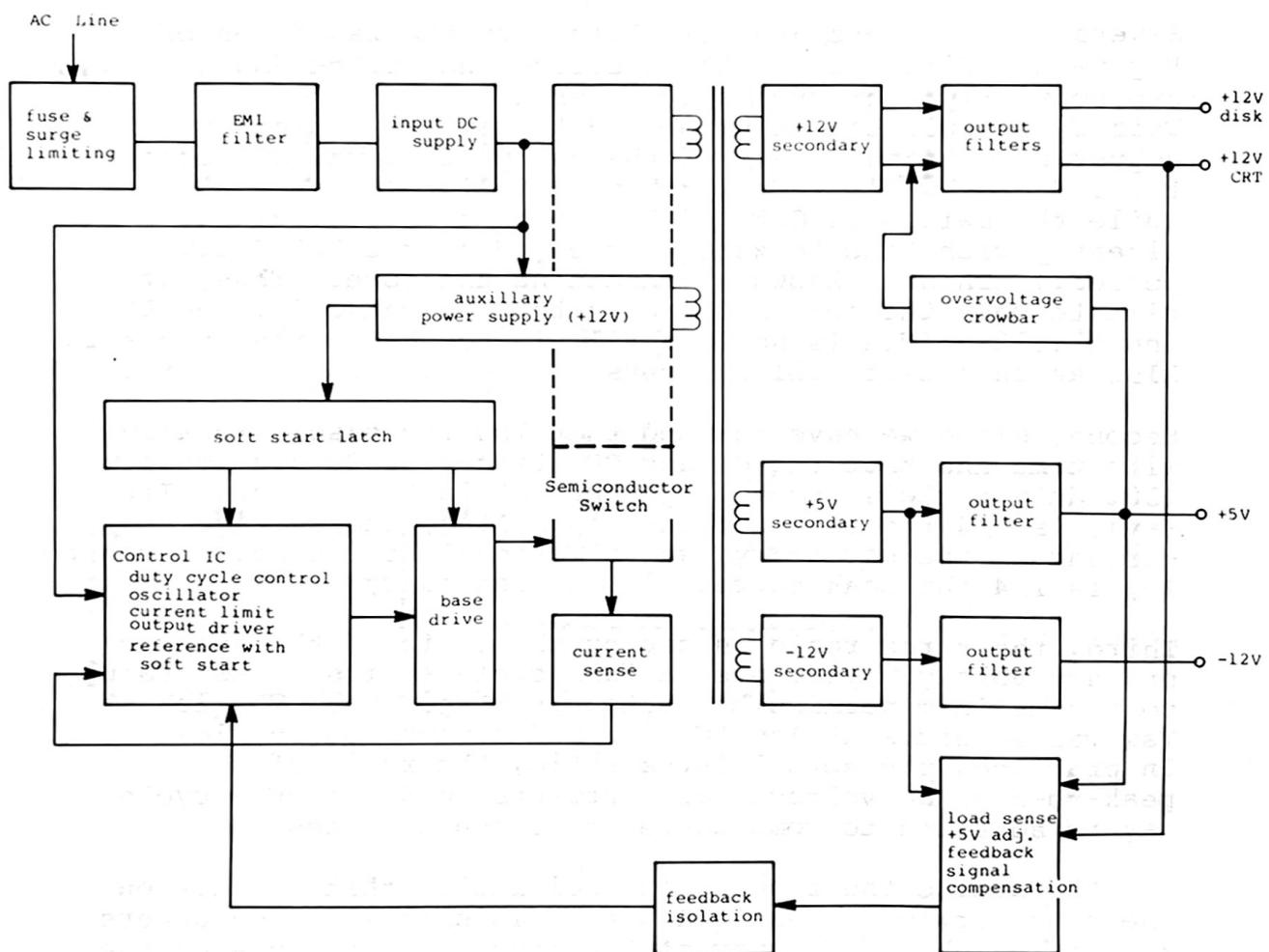


FIGURE 3. BLOCK DIAGRAM

The other blocks provide additional output voltages, add safety or protective features, reduce circuit noise, and

develop signals for use by the control section. The control section continuously operates the bipolar transistor switch and varies the proportion of ON time to OFF time in response to changes in AC input line voltage or output load current. This is accomplished by feeding back a signal from the output terminals that instructs the control section to increase or decrease the ON time to compensate for a change in the output voltage.

The DC voltage supply to the control section is controlled by the latch circuit when AC power is first applied to the power supply. A built-in timing circuit allows the input DC supply filter capacitor to become fully charged before power is applied to the control section. After the control section circuit starts and secondary voltages reach their regulated output levels, the auxiliary power supply provides the required DC voltage to operate the control section. The latch is reset when the current limit or under-voltage sensors operate, thus removing DC voltage to the Control IC.

There are four secondary or output voltages in addition to the auxiliary supply: +5.05 volt, +12 volt CRT, +12 volt Disk, and -12 volt. The +5.05 and +12 DISK voltages are regulated by the control circuit response to the frequency compensated feedback control signal which comes from the load sense section. Since the load sensing occurs on the secondary side, an optical coupler circuit is necessary to provide safety isolation between the primary side common ground and the secondary side common ground.

All the secondary voltages, including the auxiliary +12 voltage, share the same magnetic flux linkage in the transformer core and are controlled by the flyback inductor. Any change in secondary load currents cause a change in the shared magnetic flux. This change in the flux of the inductor sets up an EMF (electromotive force) which causes a flux in opposition to the one which resulted from the change in load current. Thus, the original change tends to be counteracted and the current delivered to the load remains constant.

The output filters reduce the remaining ripple voltage components of the AC line and switching frequencies to levels low enough to prevent interference with the circuits operated by the supply. Switching frequency components that could be conducted out the AC input terminals are suppressed by the EMI filter to avoid interference with other equipment connected to the power line.

The overvoltage crowbar senses an abnormal rise in the +5.1 volt output and short-circuits the voltage line to the common secondary ground, thus tripping the current limiting circuit which finally shuts down the supply.

The surge limiter at the AC line input prevents the input filter capacitor in-rush current surge from exceeding component ratings or unnecessarily tripping external fuses.

The power supply is designed to provide a stable +5.1 volt output over a wide range of line voltage and load conditions. The +5.1 volt output is derived from a full bridge rectifier and a series inductor. The output voltage is controlled by a feedback system which monitors the output voltage and compares it with a reference voltage. The reference voltage is generated by a zener diode and a resistor. The feedback signal is compared with the reference signal and the error signal is used to control the power supply. The power supply is also protected against overcurrent and overtemperature conditions.

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2/ TECHNICAL SPECIFICATIONS

Environment:

Temperature; Operating	0 to 50 C (32 to 122 F)
Storage	-40 to 85 C (-40 to 185 F)
Humidity; Operating	85% r.h. @ 35 C (95 F) max.
Storage	95% r.h. @ 55 C (131 F) max.

Input Voltage:

90 to 135 VAC rms, 47 to 63 Hz

Input Surge Current:

48 amps max.

Efficiency:

70% min. at full load with 115 VAC rms input

Output Voltages:

V1, +5.05 VDC
V2, +12 VDC CRT
V3, +12 VDC DISK
V4, -12 VDC

Output Power:

continuous 65 watts max.

Output Current:

	Output	Load	
Condition 1 (Model III use)	V1	Min.	Max.
	V2	1.35 A	4.0 A
	V3	0.60 A	1.5 A
	V4	0.40 A	2.1 A
		0.005 A	0.10 A
(Hard Disk use)	V1	2.5 A	5.0 A
	V3	0.75 A	2.0 A*
	V4	0.005 A	0.10 A

*NOTE: V2 and V3 connect in parallel to provide the V3 output. The V3 output will support a 5.0 A peak load which decays to 1.0 A in approx. 8 seconds. V1 and V3 must be within specified regulation when this surge decays to 4.0 A.

Output Ripple Voltage:

V1	(5.05 VDC)	50mV p-p
V2	(+12 VDC)	150mV p-p
V3	(+12 VDC)	150mV p-p
V4	(-12 VDC)	150mV p-p

NOTE: Ripple is the composite 100/120 Hz ripple due to the line, plus the high frequency ripple due to the power oscillator. Common mode noise which may be observed due to oscilloscope connections should be ignored.

Output Voltage Regulation:

After initially setting V1, output voltage tolerances under all conditions of rated line, load, and temperature should remain within the following limits:

V1	(+5.05 VDC)	+/- 3%
V2	(+12 VDC)	see *NOTE
V3	(+12 VDC)	+/- 5%
V4	(-12 VDC)	+25%, -8.3%

- *NOTE: a) The initial value of V2 must not change by more than +/- 100mV under the following load conditions of V3:
-- A step increase in output current from 0.6 A (initial condition) to 2.4 A, decaying within 60 msec to 2.1 A.
-- A step decrease in output current from 2.1 A (initial condition) to 0.6 A.
b) V2 output voltage may vary +/- 5% under all other conditions of rated line, load, and temperature as defined in the specification.

Over-Current Protection:

Power supply will shut down before total power exceeds the point where damage would result. No damage will result when any output is short circuited continuously with 100 milliohms or less.

Over-Voltage Protection:

The +5.05 VDC circuit is protected with a "crowbar" circuit with a trip range of 5.8 to 6.8 VDC.

Hold-Up Time at Continuous Max Load:

Nominal Line 16 mSec minimum
Low Line 10 mSec minimum

3/ THEORY OF OPERATION

The basic operating principles of a flyback converter and the necessary functional blocks to form a complete power supply were reviewed in the System Description section. In this part, the operation of each section of the circuit will be analyzed and later these sections will be connected to illustrate the signal flow in the power supply.

AC Input

A conventional bridge rectifier and a filter capacitor are connected directly across the AC line to provide the DC input voltage to the power supply.

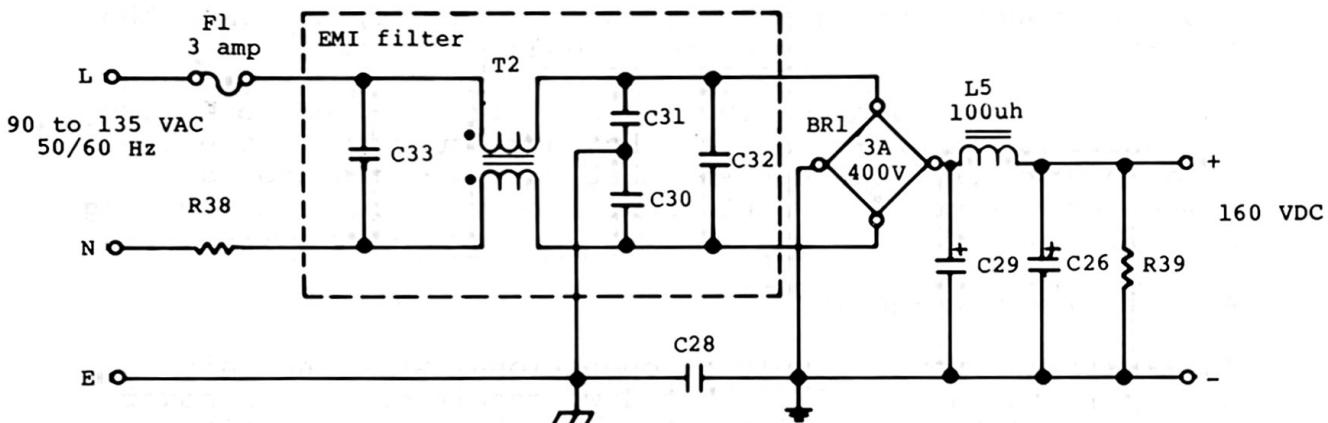


FIGURE 4. INPUT AC SUPPLY

An EMI filter consisting of capacitors C30-C33 and choke T2 are inserted at the input to the rectifier. This filter circuit keeps the high frequency signals generated in the power supply from being conducted into the AC power line. C30 and C31 provide a low impedance to the earth ground terminal for signals common to both hot and neutral sides of the AC line. C32 provides a low impedance dissipative path for the RF signal energy which appears across the line. T2 blocks RF signals common to both sides of the line and reflects them back toward the lower impedance elements near the rectifier. T2 also helps block differential (across-the-line) signals by using the EMF set up by the signal current on one side of the line to oppose the signal current flowing in the other side. C33 serves as a

transient bypass capacitor to protect the power supply from large transient voltages that appear on the AC power line. C33 also improves the efficiency of the RFI filter choke T2 by terminating the line in a low impedance to absorb and dissipate any remaining differential RF energy.

R38 is a negative-temperature-coefficient-thermistor which limits the turn-on surge current of the power supply filter capacitor C29. The resistance of this thermistor when "cold" is approximately 10 ohms. As the filter capacitor charges toward the peak value of the AC input voltage, it draws less current from the line. At the same time, the heating effect of the current flowing in the thermistor causes its resistance to decrease until it reaches its rated "hot" resistance of less than 1 ohm. As you can see, the thermistor dissipates very little power when the power supply is in operation. The thermistor is designed to cool rapidly enough, during power loss or turn-off, to limit the turn-on surge after only a few seconds cool-down.

The fuse, a fast acting 3.0 amp unit, is selected to ignore the short term turn-on surges, but open quickly in the event of an abnormally high current that would result from a component failure in the DC input supply or current limiting circuits.

Auxiliary Power Supply

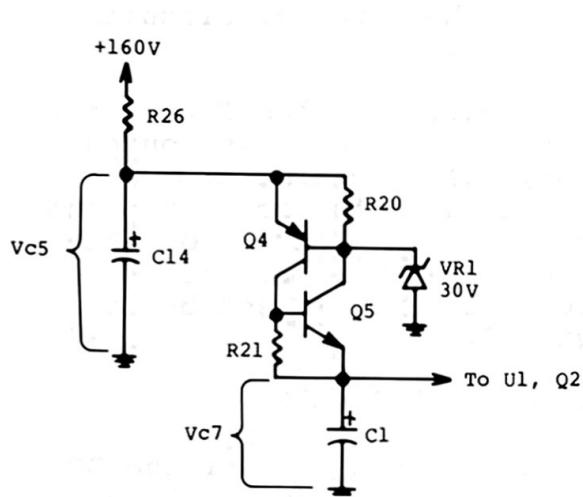
The auxiliary power supply is operational when the main supply is on and not in a shut-down condition. This power supply consists of winding 2-3 on T1, half-wave rectifier CR4, and filter capacitor C14. The voltage output is approximately +15 volts under normal conditions but momentarily reaches about +31 volts during start-up.

Kick Start Latch

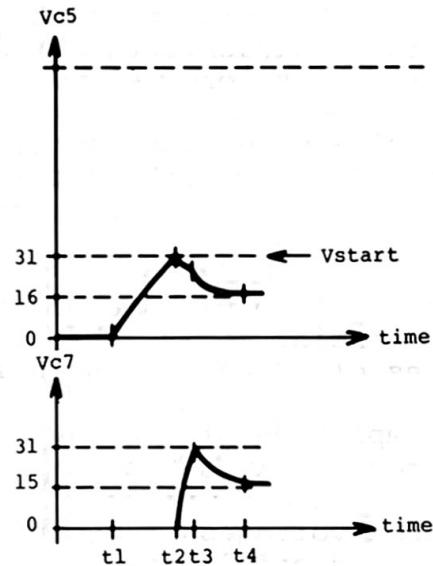
Start up of the circuit is initiated by the kick start latch. This latch is shown in simplified form in Figure 5a along with the accompanying waveforms in Figure 5b. When power is applied, C14 charges toward $V_{in} = +160$ volts through R26 with a time constant of approximately RC or 37.5 seconds. However, as we'll see, the kick start latch turns on in 2 or 3 seconds, the time required for the voltage across C14 to reach $30 + V_{be4} = 30.7$ volts. At this point Q4 turns on and develops a bias across R21 which turns on Q5.

Referring to Figure 5b, as C_{14} dumps its charge into C_1 beginning at time t_2 , the voltage across C_{14} starts to decrease toward a level that will be determined by the load composed of U_1 and the base drive circuit. Notice that the voltage across C_1 momentarily approaches the full 31 volts at time t_3 before it drops down under load to about +15 volts at time t_4 .

(a) Latch Circuit



(b) Waveforms



t_1 : Power applied
 t_2 : Latch turns ON
 t_3 : C_1 peak charge
 t_4 : C_1 voltage at loaded value
 $V_{in} = 160$ volts

FIGURE 5. KICK-START LATCH

With C_1 charging rapidly through the low resistance of a saturated Q_4 via V_{be5} , the reference supply inside U_1 develops its 5.0 volt output when the voltage across C_1 exceeds about 8 volts. At this point, the supply has not quite yet started, but U_1 has a DC supply at pin 10. All that remains is to start up the pulse generator so that the supply operates and replenishes the charge in C_{14} on each cycle, thus maintaining a DC source for U_1 of about +15 volts. Completion of the start-up sequence occurs when the soft start circuit, described in the next section, has started the pulse generator.

Control Section

The control section consists of the control IC, the primary half of the feedback optocoupler U2, and the base drive circuit for the switching transistor. The control circuit IC has three major parts: an internal regulator, a pulse generator, and an error amplifier section.

The internal reference is a regulated +5.0 DC voltage. This voltage provides the reference voltages for the comparators used in the pulse generator as well as the DC supply voltage for the feedback optical coupler and the internal circuits of U1 except for its output transistors.

The pulse generator section of the control IC has four major parts: (a) sawtooth oscillator; (b) wave-shaping and output circuit; (c) regulating comparator; (d) dead-time comparator. Figure 6 illustrates the sawtooth oscillator and output circuit waveforms and the approximate levels of the DC control voltages applied by the comparators to the wave-shaping logic. The oscillator frequency is set by the values of R3 and C7 shown in Figure 7.

The amplitude of the sawtooth is set at 3.0 volts (approximately 60% of the 5.0 volt reference voltage). Whenever the sawtooth voltage, V_{osc} , exceeds both of the DC control voltages, V_{reg} and V_{dt} , the output circuit will be in the ON condition.

The DC control voltage, V_{reg} , set at a quiescent value by R6 and R9, varies in response to changes in the supply's DC output voltages as sensed by U3 and coupled through U2. Notice that these voltages will vary because of changes in output loading, AC input voltage, and also because of the residual 120 Hz ripple component from the main DC supply.

The dead-time control voltage, V_{dt} , is set at a constant value by R4 and R5 and ensures that the pulse generator "OFF" time will be at least 50% of the sawtooth period. This allows adequate time for the complete transfer of stored energy from the primary to the secondary of transformer T1 as discussed in the section on basic principles.

A concept known as duty cycle was introduced in earlier paragraphs. Duty cycle is defined as the ratio of the "ON" time of the sawtooth cycle to the total length of the sawtooth period. Since the sawtooth has a linear ramp characteristic, the duty cycle is also equal to:

$$\text{duty cycle } d = \frac{V_{osc, \text{pk}} - V_{reg}}{V_{osc, \text{pk}}} = \frac{t_{on}}{T \text{ period}}$$

There are three possible conditions of the duty cycle:

$d = 0$ which occurs when either control voltage V_{reg} or V_{dt} exceeds the peak value of the sawtooth waveform V_{osc}

$d = 50\%$ which occurs when V_{reg} is less than V_{dt} . This happens when the loading on the output of the supply is heaviest and the AC input voltage is at its lowest permitted level (see specifications)

$0 < d < 50\%$ which occurs during normal operation.

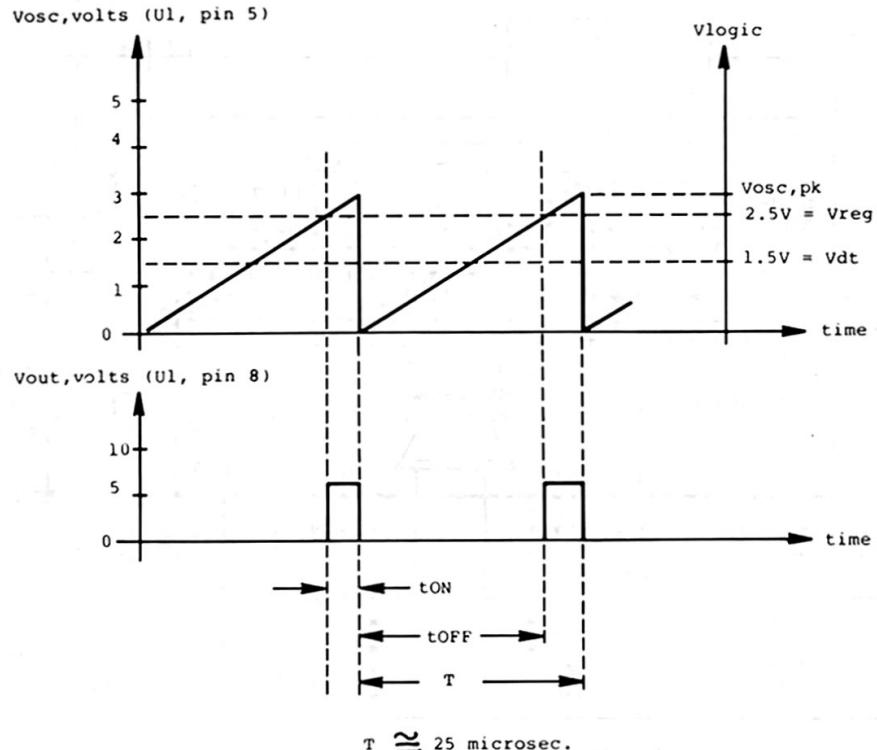


FIGURE 6. OSCILLATOR, PULSE GENERATOR WAVEFORMS

The dead-time control voltage is used in one other important way. Notice the 4.7 ufd capacitor, C2, connected across R4 in Figure 7. When power is first applied to the supply, the

voltage across the capacitor is zero. Therefore, $V_{dt} = V_{ref}$ = 5.0 volts and no pulses appear at the output because V_{dt} is greater than $V_{osc,pk}$. As C_2 charges, V_{dt} decreases toward $1/2 (V_{osc,pk})$ in a time determined by R_5 and C_2 as $t = 5 \times 15k \text{ ohm} \times 4.7 \text{ ufd} = 1/3 \text{ second}$. As V_{dt} decreases past $V_{osc,pk}$, very narrow pulses begin appearing at pin 8 of U1. The pulses become successively wider until V_{dt} is less than V_{reg} . C_2 continues charging until V_{dt} reaches the final correct value of about 1.5 volts. This action provides the soft start feature of the power supply and allows sufficient time for the DC input supply and latch to reach normal operating conditions before the supply is started. In effect, the load is connected to the supply gradually by the soft start circuit.

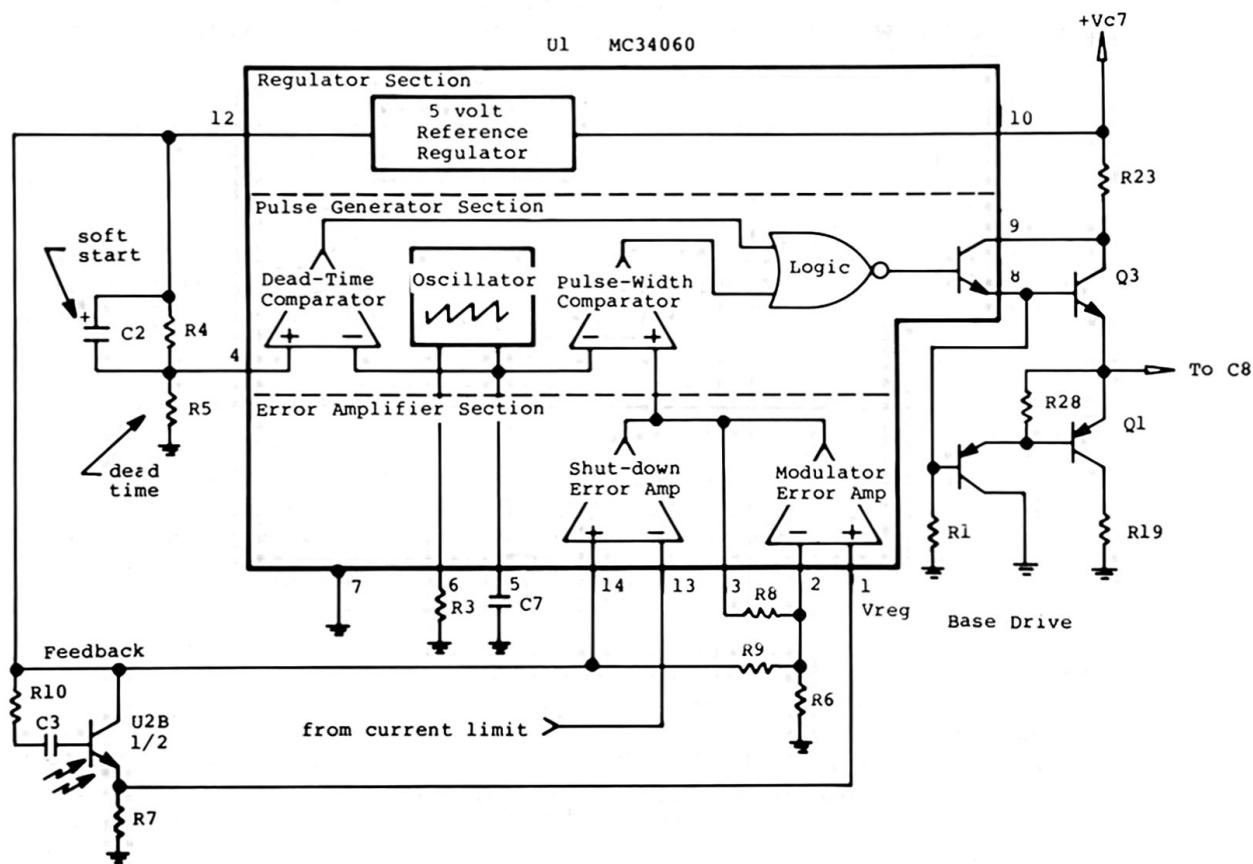


FIGURE 7. CONTROL SECTION

Frequency stability of the sawtooth oscillator is provided by the 2% tolerance and polyester construction of the timing capacitor, C7, and the 100 parts-per-million temperature stability and 1% tolerance of R3. Voltage stability of the DC control voltages is provided by the +/- 2 1/2 percent stability of the 5.0 volt reference.

The control section consists of two error amplifiers in U1, the primary half of U2, and associated circuitry shown in Figure 7. One of the error amplifiers serves as a regulator or pulse-width modulator which derives the DC control voltage, Vreg, from the signal voltage developed across R7 by the current in U2. This current is a replica of the current developed by U3 in response to the condition of the output voltage at the +5.1v and +12v outputs. This amplifier has a gain of about 10 determined by:

$$A = \frac{R8}{R9 \parallel R6} = \frac{22k \text{ ohm}}{2.35k \text{ ohm}} = 10$$

The other error amplifier in U1 serves as a shut-down comparator. The positive terminal, pin 14, is set at the +5.0 volt reference and pin 13, the negative terminal or shut-down pin, is tied to the current limit latch. The output of this error amplifier (equal to Vreg since both error amplifier outputs are tied to the wave-shaping logic) will rapidly increase toward the +5.0 volt reference when pin 13 drops below 5.0 volts. Recall that if Vreg exceeds the peak sawtooth voltage, pulses are inhibited and the power supply shuts-down.

Base Drive

Figure 8 illustrates the BASE DRIVE circuitry which turns switching transistor Q7 on and off in response to the output of the pulse generator portion of U1. The "ON" circuit is shown in Figure 8a and the "OFF" circuit is shown in Figure 8b. Waveforms for these circuits appear in Figure 9.

The output transistor of U1 combined with Q3 forms a Darlington pair. This circuit provides the relatively large current necessary (through coupling capacitor C8) to turn on Q7. R23 limits this base current to a value large enough to turn on Q7 quickly, but not so large that it will exceed the ratings of Q3, C8, or the base emitter junction of Q7, or so large that the turn-off time of Q7 is excessive.

As Q3 turns on, C8 charges to approximately +5 volts and Q7 is driven into saturation. Energy is stored in the primary winding of T1 as the collector current of Q7 increases or "ramps up" at a rate determined by the inductance of the transformer primary winding.

When the output transistor of U1 turns off, the emitters of Q1 and Q2 are initially at the +6 volt level determined by the charge on C8, the Vbe drop of Q7, and the drop across R37. Both base-emitter junctions of the Q1-Q2 darlington pair are biased ON and the positive terminal of C8 is clamped to near-ground by the saturating Q1. At this point, C8 still has most of its charge and the base voltage of Q7 is approximately -4.5 volts with respect to ground.

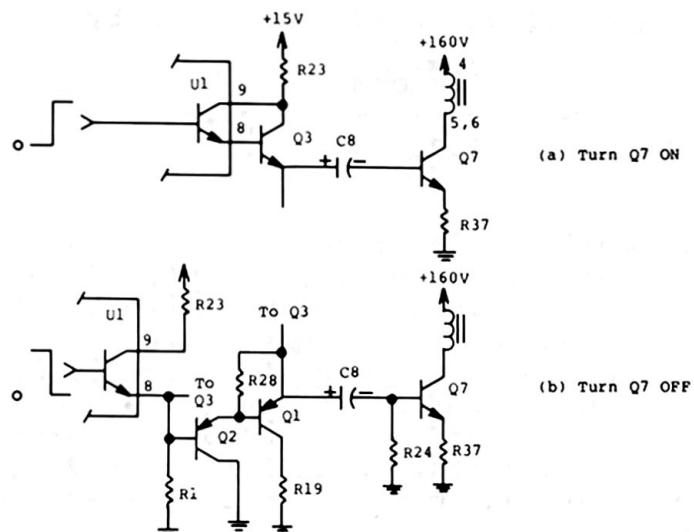


FIGURE 8. BASE DRIVE CIRCUIT

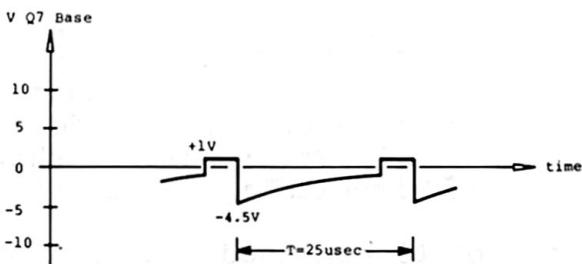


FIGURE 9. Q7 BASE VOLTAGE WAVEFORM

With the strong reverse polarity provided by C8 across the base emitter junction of Q7, the "forward" charge stored in the junction capacitance is quickly swept out and Q7 is turned off. C8 continues to discharge through R24 to

prepare for the next "ON" cycle. R19 limits the initial discharge of C8 while Q7 is turning off.

Notice the symmetry in the base drive circuit and the key role played by C8 in both the turn-on and turn-off sequences. Because of this crucial role in the circuit, this capacitor is specified as a high temperature, low-equivalent-series-resistance component.

Primary Circuit and Current Limit Shutdown

The Primary Circuit

The Primary circuit, shown in Figure 10a, functions exactly as described earlier in the "Basic Principle" section. That is, the switch (Q7) is controlled by the base drive waveform developed by the control section.

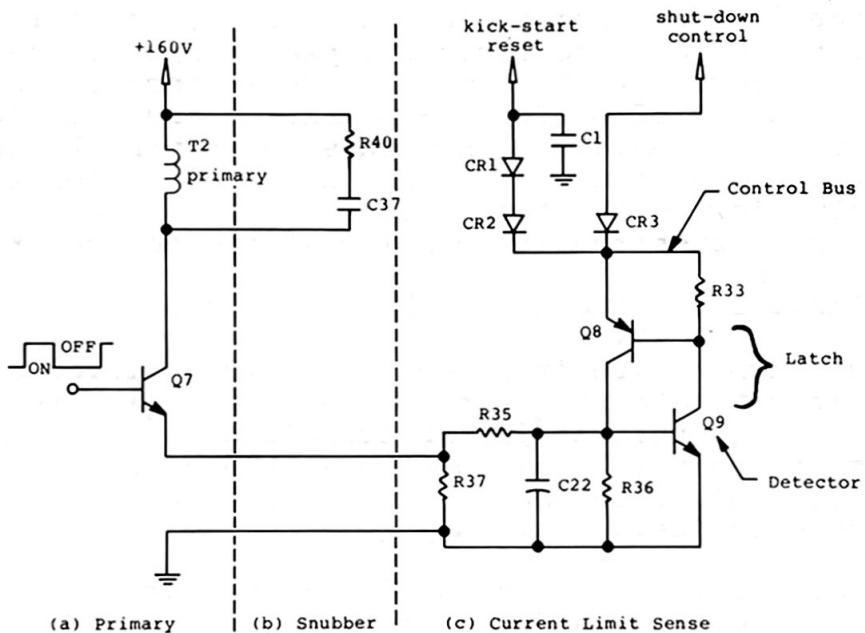


FIGURE 10. PRIMARY SIDE PROTECTION

The Snubber Circuit

Practical transformers cannot couple 100% of the stored energy from the primary to the secondary since all of the flux from the primary fails to link all the secondary turns. A circuit using this practical transformer behaves as though a small fraction of the primary inductance was not wound on

the core of the transformer, but instead placed apart from the primary and in series with it. This small, separately-acting inductance does not participate in the transformer action and is called the leakage inductance.

If the resonant circuit, consisting of this leakage inductance and the stray capacitance in the adjacent circuit, has sufficient Q (relatively low resistance losses), a damped oscillation will occur in this resonant circuit when the transistor switch opens. The peak value of this oscillation will add to the $V_{ce} = 2 \times V_{in}$ which appears across the transistor switch just after turn-off. The combined peak V_{ce} may exceed the transistor breakdown rating if not damped out by the action of a snubber circuit.

When Q7 turns off, the energy stored in the leakage inductance is transferred to the electric field of the total capacitance of C37 plus stray capacitance. (Since C37 capacitance is much larger than the strays, it dominates in this action and tends to limit the peak value of the Q7 turn-off voltage.) If there were no resistance in this series connection of C37-plus-parasitics and leakage inductance, they would exchange this energy back and forth indefinitely. R40 is used to damp this oscillation without excessively slowing the turn-off of Q7, thus effectively snubbing the turn-off voltage spike at the collector of Q7.

Current Limit Circuit and the Shut-Down Sequence

The current limit circuit forces the voltage level at a control pin of U1 to change to a near-zero value very quickly when the current in the transistor switch exceeds a predetermined point. It also removes the supply voltage from the control circuit and resets the kick start latch and soft-start circuits.

The current limit circuit shown in Figure 10c has three parts: a control bus, a detector, and a latch. The control bus supplies the operating DC voltage to the current limit circuit. It also conducts the current limit signal to control pin 13 and to the reset point in the kick start latch circuit. Diodes CR2 and CR3 steer this signal.

The normal maximum peak current in switching transistor Q7 is 3 amps. The detector transistor Q8 is biased to turn on by the divider action of R35 and R36 whenever the Q7 peak current through R37 exceeds 4 amps. A low-pass filter, formed by R35 and C22, prevents false detections on transient signals that don't represent an over-current condition.

As soon as Q9 turns on, its collector current develops the turn-on bias for Q8 across R33, and the Q8-Q9 pair "latches" in the "ON" state until the DC source for the latch is removed. Removal of this DC source occurs when C1 discharges through CR1, thus removing DC voltage from the control IC. Notice also that the kick start latch, Q4 and Q5, is still in the "ON" state and thus provides a discharge path for C14. When the decreasing voltage across C14 is less than approximately one volt, the Q4-Q5 latch also switches off.

At this point in time, all circuits are in an OFF condition except the input DC supply. C14 now begins to re-charge toward the input DC supply to restart the power supply. If a fault remains, the kick start and current limit circuits will continue to shut-down and re-start the power supply several times per second until the fault is removed or AC power to the supply is turned-off.

Under-Voltage Lockout

The Under-Voltage Lockout, UVL, shuts down the supply whenever the AC input voltage drops below about 90 volts. This occurs when the voltage at pin 13, set by the divider action of R27 and R25, diminishes to a level below the internal reference supply of the control IC. Pulses are inhibited immediately and because the DC supply to the Control IC is no longer replenished by the auxiliary supply, it discharges toward zero.

Why is it important to shut down the supply if the input AC line drops below 90 volts? The answer will become clear when an inherent characteristic of the circuit is discussed, namely, its negative input resistance.

Imagine the situation where the supply is delivering full power to its load and the AC input voltage drops five or ten volts. The supply control circuit responds by increasing the "ON" time of the switching transistor thus increasing the average current in the primary winding. The only way the DC supply can deliver more current is to draw it from the AC line. So the negative change in AC input voltage was accompanied by a positive change in AC input current.

Another way to describe this characteristic is that the supply is a constant power device, that is:

$$\text{Pin} = \text{Vin} \times \text{Iin} = \text{constant.}$$

Thus if V decreases, I will increase, and vice versa. The supply will thus draw more and more current from the AC line if the AC voltage continues to decrease. In order to limit the average current to a safe value, the control circuit senses the input voltage and shuts down the supply before the AC voltage level becomes too low or the AC current input becomes too high.

Secondary Outputs

Each of the secondary windings consist of a half-wave rectifier followed by a pi filter. The input capacitor of the filter stores the charge delivered to it when the rectifier is biased ON by the polarity of the transformer winding. The inductor and the output capacitor form a low-pass filter which removes the switching frequency ripple component.

The current output of the -12 volt supply is much smaller than that of the positive voltage outputs. Because of this, the current limit circuit response is not sufficiently effective to prevent damage to the -12 volt circuit. Therefore, a three terminal regulator with its own current limiting circuit is used to protect the -12 volt output.

All of the 12-volt rectifiers are fast recovery types and the +5 volt rectifier is a Schottky type. These diodes feature high switching speeds during turn-off. Their low forward voltage drop minimizes dissipation resulting in maximum efficiency. Each of the positive outputs has a bleeder resistor.

The reason for two separate +12 volt outputs is to provide sufficient isolation between different types of loads. It is easier to regulate the +12 volts if the load which contains the DC motors in the disk drives is separated from the rest of the loads. In addition, the +12 volt "Disk" output (V3) is included in the load sense network in order to minimize the load transients which occur when the disk drives turn on and off. The supply is then better able to regulate the other +12 volt output (V2) during the severe V3 transitions.

Load Sense and Feedback Signal Development

The circuit of Figure 11 has three parts. In part (a), the IC's U2 and U3 are biased ON by resistors R11 and R22. These resistors also sense the changes in AC line input

voltage to provide line regulation. U2A is the LED half of an optocoupler which serves to isolate the DC ground circuits of primary and secondary while coupling the AC feedback signal via optical coupling. U3 serves as both a stable DC reference voltage which the output voltages are compared against and as an error amplifier which provides the gain necessary for adequate sensitivity of the control IC to load changes.

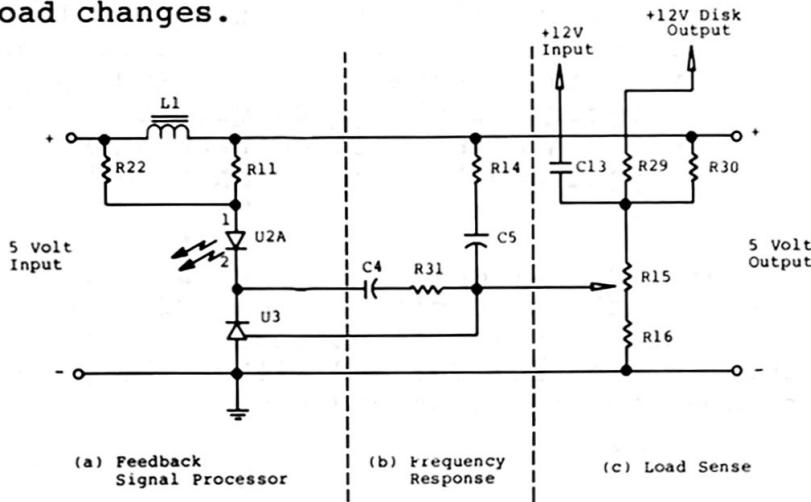


FIGURE 11. FEEDBACK SIGNAL DEVELOPMENT

Each of the passive components in the load sensing network is a high stability ($\pm 100\text{ppm}$) part to assure stability of the network over the operating temperature range of the power supply.

Part (b) of Figure 11 includes the network which tailors the frequency response of the error amplifier so that it responds to low frequency change only. This network, consisting of R14/C5 and R13/C4, also determines the stability of the power supply by ensuring that the power supply control circuit has no tendency to oscillate.

Part (c) illustrates the load sensing network. Equal currents through R15 are supplied from the +12V DISK and +5.05V outputs by R29 and R30. In addition, a portion of the transient signal occurring on the +12V CRT output (when the motors turn on or off) is fed to R15 by C17. The wiper of R15 feeds a control signal which represents the status of the current loads to the error amplifier U3. U3 amplifies and compensates it then U2 couples that control signal to U1 where it is used to vary the switching transistor (Q7) ON time to adjust the output voltages as necessary. R15 is adjustable to provide the initial set-up of the +5.05V output when it is installed in a computer.

of the +5.05 volt output when it is installed in a computer.

Overvoltage Crowbar

Some of the circuits supplied by the +5 volt output are quite sensitive to voltages in excess of 7 volts. Since some circuits require both +5 and +12 volts, a failure in those circuits could apply +12 volts to the +5-volt bus and thus damage some of the +5-volt circuits. To prevent the +5-volt bus from exceeding a safe level, an SCR, Q6, is used to "crowbar" or short-circuit the +5.05 volt output to the secondary ground bus. This short circuit triggers the current limiting circuit and the supply shuts down until it tries to restart.

Referring to Figure 12, VR2 sets the turn-on point of the SCR and R17 develops the gate signal when VR2's Zener breakdown voltage of 5.6 volts is exceeded. C6 and R17 provide current limiting for VR2 and filter the gate signal so Q6 won't respond to transient signals.

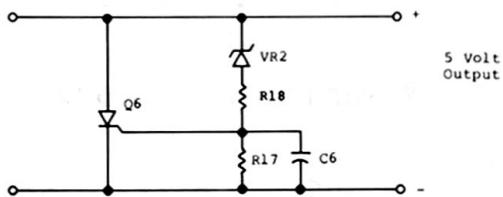


FIGURE 12. OVERVOLTAGE CROWBAR

Power Chain

In a sense we have already analyzed the power chain in the section on basic principle of operation. The base drive causes the switching transistor to turn on and off at a prescribed rate. This action alternately stores energy from the DC input in the primary inductance and releases it into the secondary through the flyback transformer action. The energy is then stored in the input filter capacitor at a voltage determined by the transformer turns ratio. Notice that the turns ratio determines the ratio of collector voltage to secondary voltage, both of which are alternating voltages. The ratio of input-to-output DC voltage is determined by the duty cycle and the turns ratio together.

For example, lets look at the +5 volt output of Figure 13 at normal loading and approximately 120 VAC input. Under these conditions, the DC input voltage is 168 VDC and the duty cycle is approximately 40%. Thus, our average DC voltage at the switching transistor collector (or across the primary)

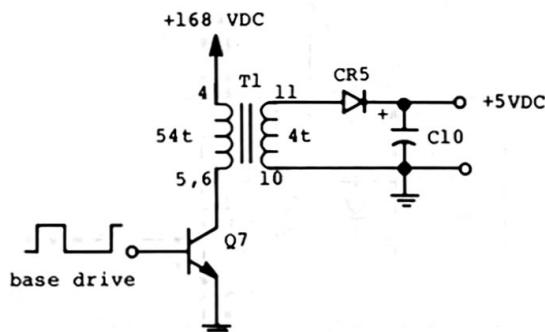


FIGURE 13. POWER CHAIN

is 40% of 168 or 67.5 volts. Dividing this average DC voltage by the turns ratio for the 5 volt secondary (54 : 4 = 13.5) gives us 5.0 volts.

$$\frac{67.5V}{13.5} = 5V$$

Control Chain

Imagine the load end of the feedback path disconnected from the +5.1 volt output terminal and unfolded so that the load sense network is now at the "input". The secondary rectifier (CR5) and filter (C10/C11, L1, C12) remain as the output. The circuit as it now appears, redrawn in simplified form in Figure 14, is known as the control chain. To see how the regulation action occurs, assume a small negative voltage change at the "input" of the feedback network and follow it through the control chain.

This negative voltage change, which would correspond to a slightly heavier load current, appears at pin 1 of U3 as a decreasing voltage. The error amplifier in U3 inverts and amplifies this signal. The positive-going output voltage of U3 at pin 3 causes less current to flow in the internal LED of U2A. A replica of this smaller current, optically coupled and induced in the phototransistor of U2B, develops a reduced voltage across R7 at the non-inverting input of the regulator error amplifier in U1.

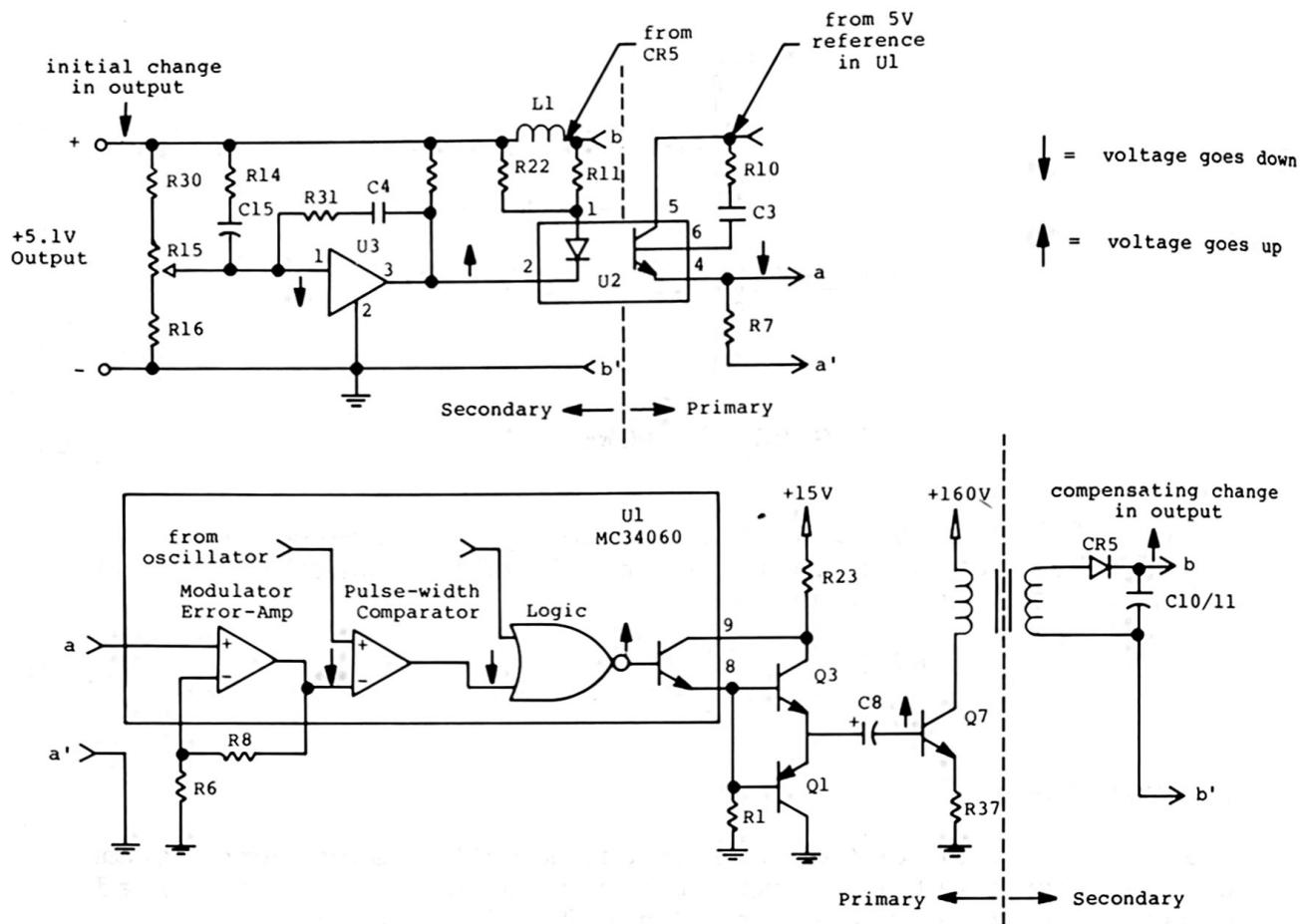


FIGURE 14. CONTROL CHAIN SIMPLIFIED SCHEMATIC

The regulator error amplifier in U1 does not invert the signal, but further amplifies it, improving the sensitivity of the control chain to small changes at the power supply output. The regulator error amplifier output is Vreg. Since we established earlier that a negative-going Vreg increases the length of the base drive pulse, Q7 is turned on a little sooner so that it can store more energy from the AC line in the primary inductance. Finally, this increased energy is stored in the filter capacitor C10/C11 during the flyback interval and supplies the increased demand for current that resulted in the original reduction in the output voltage.

More simply stated, the control chain uses an amplified version of the output voltage CHANGE to adjust the width of the base drive pulse through the action of a control voltage at a comparator input.

4/ TROUBLESHOOTING CHART FOR 65 WATT POWER SUPPLY

Trouble	Cause	Remedy
open fuse	shorted line input filter capacitor	check and/or replace C33, C32, C31, C30
	shorted bridge	check BR1
	shorted filter capacitor	check C29, C26, R39
	shorted switching transistor	check Q7, C37, R40, C26, T1 pri., Q3, Q1, R37
Current limit cycle	single rectifier open in bridge	check and/or replace BR1
	open filter capacitor	check C29
	shorted snubber capacitor or resistor	check C37, R40
	open opto-coupler	check U2
	shorted supply output	check computer for short on +5V, +12V CRT, +12V DISK, -12V outputs and clear shorted condition
	shorted output rectifier	check CR5, CR6, CR7, CR8
	open or shorted output filter capacitor	check C16, C18, C25, C23, C10, C11, C12, C19, C20
	defective crowbar	check Q6

Troubleshooting Chart (cont'd)

Trouble	Cause	Remedy
no pulses at pin 8 of U1, (i.e., supply shut down)	no aux. DC supply	Check and/or replace CR4, CL4, T1 aux.
	no "kick start"	check R26, Q4, Q5, VR1, CR1, C1
	no base drive	check U1, Q3, R23, C8, R24
	dead-time control divider malfunction	check C2, R4, R5, U1 (for V ref.)
	under-voltage protect divider malfunction	check R27, R25, C9, Q9
	PWM feedback malfunction	check and/or replace U1, U2, C3

5/ TESTING AND ADJUSTMENTS

The following tests should be performed to guarantee correct operation of the power supply after repairs have been made. The first test checks the primary circuits and is to be made without AC power applied. The second test is a complete operational test with AC power applied.

Primary, Checks T2, U1**NO AC POWER APPLIED**

1. Apply +35 volts DC via 3900 ohm resistor from Q5 emitter to primary side ground. Observe the voltage across C5 as it charges. As it reaches a value near +31 volts (about 2 seconds), it should drop to near +15 volts as Q5 turns on.
2. Check U1 pin 8 and/or Q8 base for a base drive pulse: a 40 kHz square wave of 8 volts/4 volts amplitude respectively.
3. Apply +35 volts DC through a 120K ohm resistor and a normally closed SPST switch to U1 pin 13. Operate the switch and observe Q8 base (TP1) for loss of base drive pulses.

Operational, Checks T2, U1, U2**APPLY AC POWER**

1. Apply rated maximum loading for condition 1 (Model III use) or condition 2 (5 1/4" Hard Disk use).
2. Apply 120 VAC input voltage and observe Q7 current (via loop on PCB) and voltage (at TP2). Supply should start in two to four seconds.
3. Observe the +5.05 volt output and adjust R15 until the output is exactly +5.05 volts DC.
4. Measure +12V and -12V outputs.

5. Check all outputs at Vin = 90 VAC and 135 VAC at:
 - (a) minimum and maximum loads
 - (b) check +12V CRT when +12V DISK varies in transient test.
6. Measure ripple. See Measurement Techniques below.
7. Measure efficiency. See Measurement Techniques below.
8. Test operation of current limit and over-voltage protection circuits by applying +7.0 volts to the +5 volt output.

Measurement Techniques

1. Ripple -- Unit connected to full load at low line. One end of 50 ohm coaxial cable connected to output terminals. Other end of cable (terminated with 0.01uF ceramic cap in series with 51 ohm resistor) connected to scope using BNC T-fitting. Two components at 120 Hz and 40 kHz.
2. Efficiency -- Use Diego Systems Series 200 power monitor. Efficiency = Power Out / Power In

6/ 65 WATT POWER SUPPLY PARTS LIST

SYMBOL	DESCRIPTION	R.S. PART #
Capacitors		
C1	10F, 35V, elect., radial	8326103
C2	4.7F, 25V, elect., radial	8325470
C3	0.047F, 50/63V	8393474
C4	0.47F, 50/63V	8394474
C5	0.068F, 50/63V	8393684
C6	1F, 50, elect., radial	8325014
C7	0.001F, 63V	8392104
C8	47F, 25V, elect., radial	8326472
C9	1F, 50V, elect., radial	8325014
C10	2200F, 10V, elect., radial	832----
C11	2200F, 10V, elect., radial	832----
C12	2200F, 6.3V, elect., radial	8328220
C13	0.01F, 50/63V	8393104
C14	100F, 35V, elect., radial	8327103
C15	1000pF, 100V, ceramic disc	8302106
C16	2200F, 16V, elect., radial	8328221
C17	0.1F, 50/63V	8304104
C18	3300F, 16V, elect., radial	8328331
C19	100F, 25V, elect., radial	8327102
C20	100F, 25V, elect., radial	8327102
C21	0.01F, 50/63V	8393104
C22	0.1F, 50/63V	8394104
C23	470F, 16V, elect., radial	8327461
C24	0.1F, 250VDC	
C25	2200F, 16V, elect., radial	8328221
C26	220F, 200V, elect., radial	8327226
C27	Not Used	
C28	0.01F, 250VAC	8393106
C29	220F, 200V, elect., radial	8327226
C30	4700pF, 125VAC, ceramic disc	8303475
C31	4700pF, 125VAC, ceramic disc	8303475
C32	0.1F, 250VAC	8394106
Diodes		
CR1	1N4148, switching	8150148
CR2	1N4001, 1A/50PIV	8150001
CR3	1N4001, 1A/50PIV	8150001
CR4	1N4939, 1A/100PIV	8150934
CR5	MBR1035, 8/10A, 35V, TO-220	8150035
CR6	MUR810, 8A/100PIV, TO-220	8150810
CR7	1N4934, 1A/100PIV	8150934

SYMBOL	DESCRIPTION	R.S. PART #
Diodes (cont'd)		
CR8	MUR810, 8A/100PIV, TO-220	8150810
BR1	Bridge, 2A, 600PIV	8160402
VR1	Zener, 1N5232B, 5.6V	8150232
VR2	Zener, 1N5256B, 30V	8150256
VR3	A79M12	
Fuse		
F1	3 amp, AGC	8479104
Inductors		
L1	5.0h, 10A	8419006
L2	30h, 5A	8419008
L3	Not Used	
L4	30h, 5A	8419008
L5	100h, 2A	8419009
Integrated Circuits		
U1	MC34060 Switching Regulator	8060060
	uA/TL494 Switching Regulator	8060494
U2	Opto-isolator, 4N35	8170035
U3	uA/TL431, Positive Shunt Reg.	8060428
Resistors		
R1	1K, 1/4W, 5%	8207210
R2	68 ohm, 1/4W, 5%	8207068
R3	28K, 1/4W, 1%	8200328
R4	39K, 1/4W, 5%	8207339
R5	15K, 1/4W, 5%	8207315
R6	4.7K, 1/4W, 5%	8207247
R7	4.7K, 1/4W, 5%	8207247
R8	22K, 1/4W, 5%	8207322
R9	4.7K, 1/4W, 5%	8207247
R10	4.7K, 1/4W, 5%	8207247
R11	100 ohm, 1/4W, 5%	8207110
R12	620 ohm, 1/4W, 5%	
R13	18K, 1/4W, 5%	8207318
R14	330 ohm, 1/4W, 5%	8207133
R15	1K, 20%, linear Pot.	8275211
R16	3.31K, 1/4W, 1%	8200232
R17	100 ohm, 1/4W, 5%	8207110
R18	10 ohm, 1/4W, 5%	8207010
R19	1 ohm, 1/4W, 5%	8207001
R20	4.7K, 1/4W, 5%	8207247
R21	220 ohm, 1/4W, 5%	8207122

SYMBOL	DESCRIPTION	R.S. PART #
Resistors (cont'd)		
R22	330 ohm, 1/4W, 5%	8207133
R23	27 ohm, 2W, 10%	8248127
R24	22 ohm, 1/2W, 5%	8217022
R25	22K, 1/4W, 5%	8207322
R26	75K, 1W, 10%	8248127
R27	430K, 1/4W, 5%	8207443
R28	22 ohm, 1/4W, 5%	8207022
R29	28K, 1/4W, 1%	8200328
R30	6.65K, 1/4W, 1%	8200266
R31	1K, 1/4W, 5%	8207210
R32	1K, 1/4W, 5%	8207210
R33	470 ohm, 1/4W, 5%	8207470
R34	1K, 1/4W, 5%	8207210
R35	470 ohm, 1/4W, 5%	8207470
R36	1K, 1/4W, 5%	8207210
R37	0.22 ohm, 2W, 10%	8248022
R38	Thermistor	8298016
R39	75K, 1W, 10%	8248375
R40	82K, 5W, 10%	8248268
Transistors		
Q1	MPSU51A, PNP, TO-202	8100051
Q2	MPSA55, PNP, TO-92	8100055
Q3	MPSU01A, NPN, TO-202	8111001
Q4	MPSU51A, PNP, TO-202	8100051
Q5	MPSU01A, NPN, TO-202	8111001
Q6	SCR, 8A/50PIV, TO-220	8140122
Q7	MJE13006, NPN, 8A, 400V	8110006
Q8	MPSA55, PNP, TO-92	8100055
Q9	MPSA05, NPN, TO-92	8110005
Transformers		
T1	Power, ferrite core, 65W flyback	8790046
T2	Line Choke, 5.5mH/side, 2A	8790045

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Service Manual
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7/ PRINTED CIRCUIT BOARDS

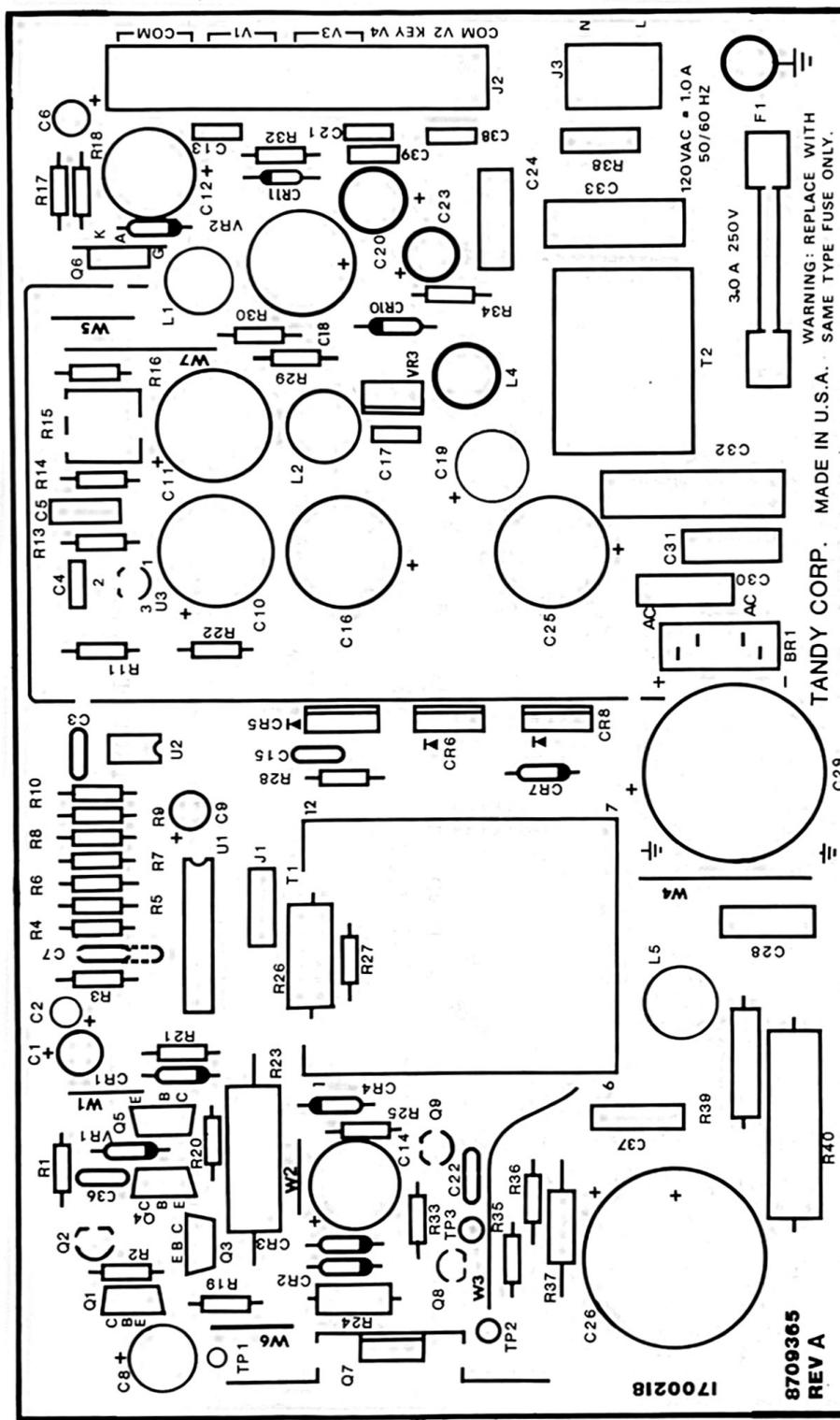


FIGURE 15. PRINTED CIRCUIT BOARD -- COMPONENT SIDE

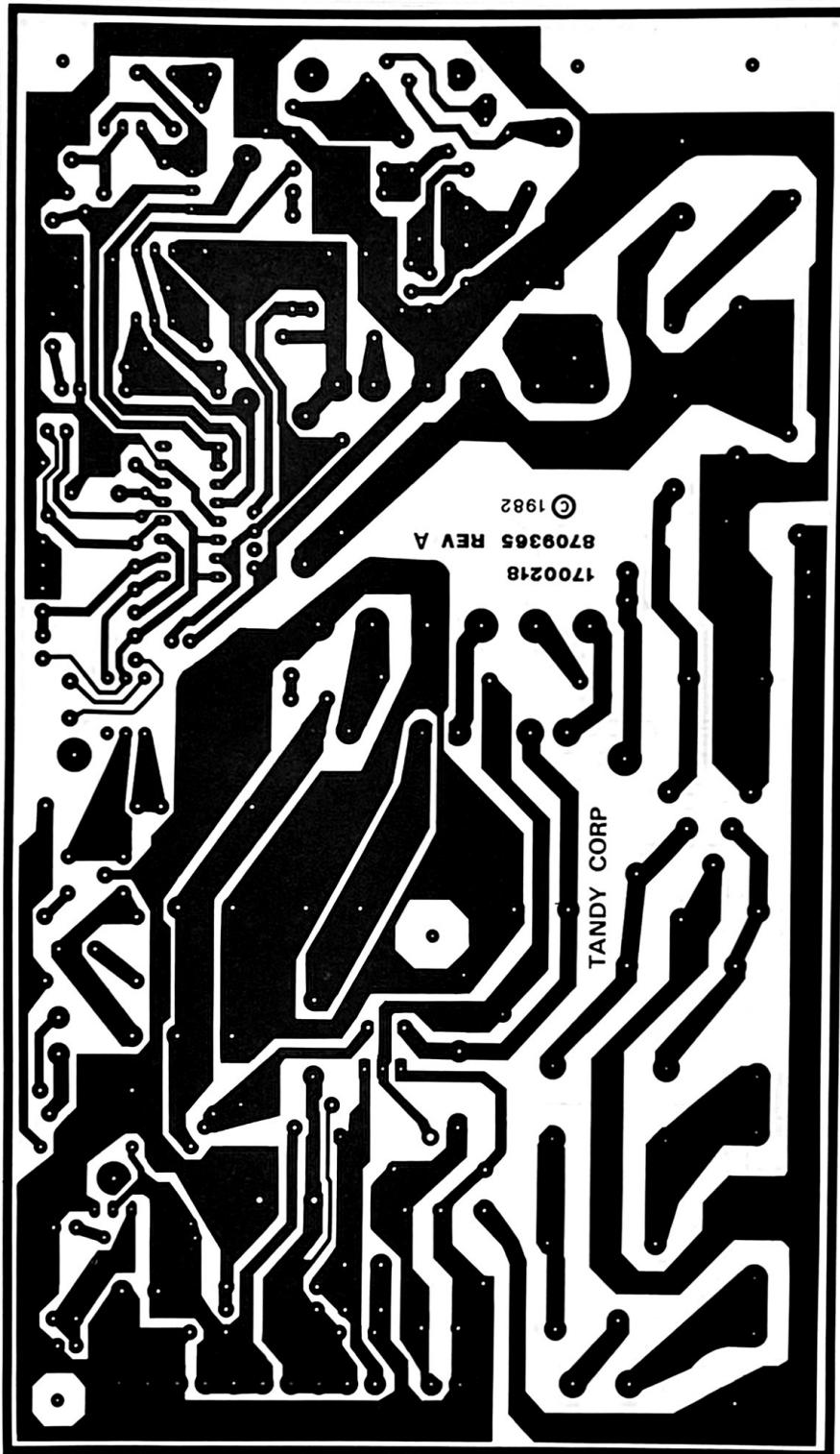
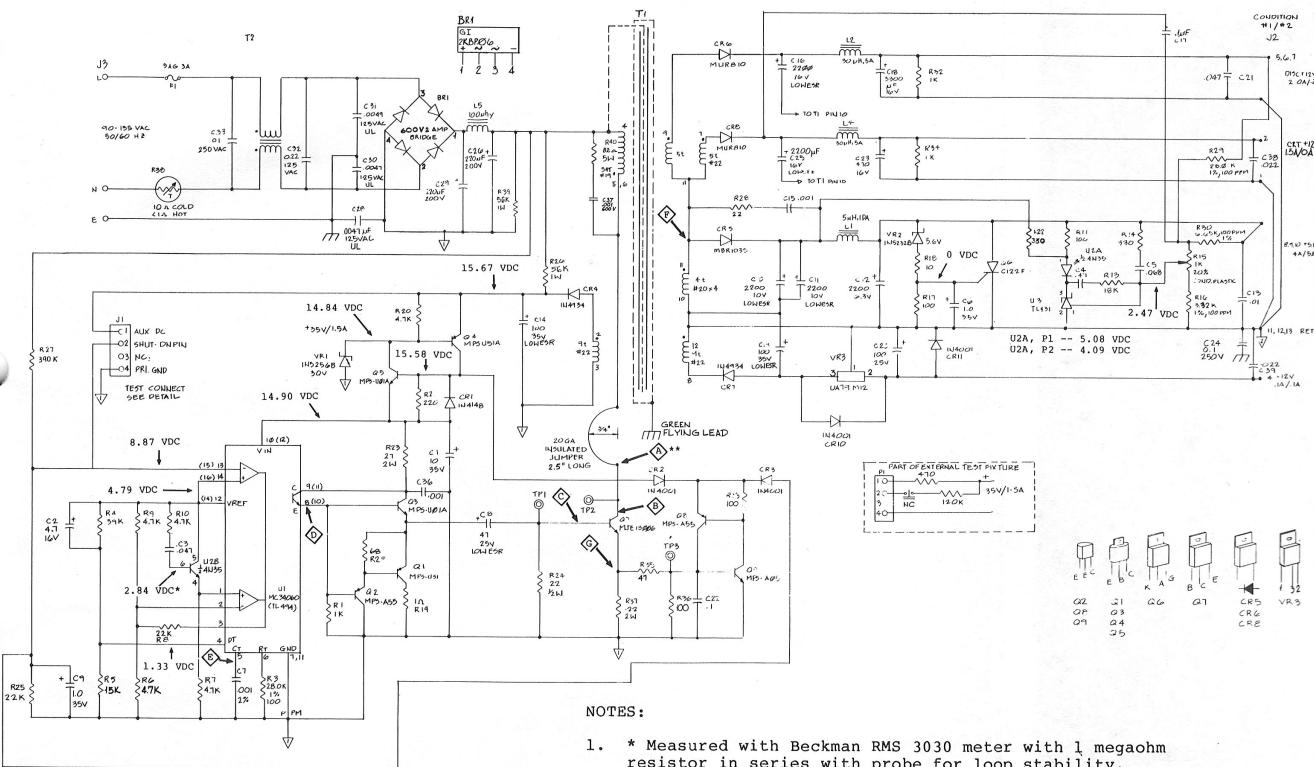


FIGURE 16. PRINTED CIRCUIT BOARD -- CIRCUIT SIDE

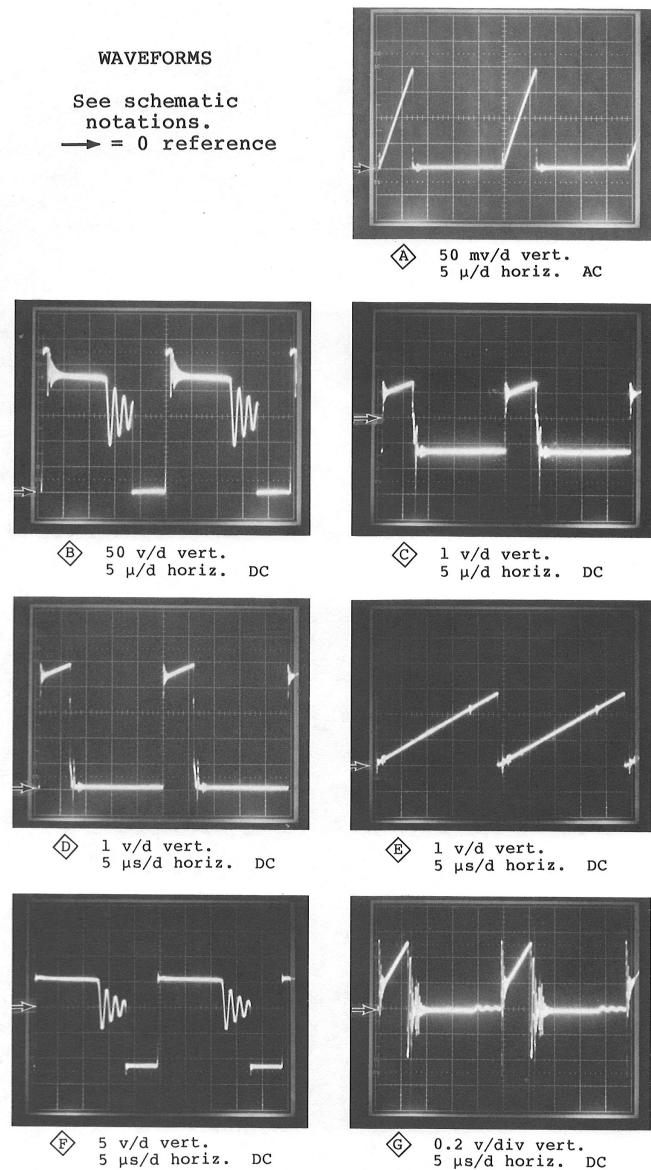


NOTES:

1. * Measured with Beckman RMS 3030 meter with 1 megachm resistor in series with probe for loop stability.
2. ** Measure with Tektronics P6021 AC current probe with 10 mA/mV termination.

WAVEFORMS

See schematic notations.
→ = 0 reference



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