

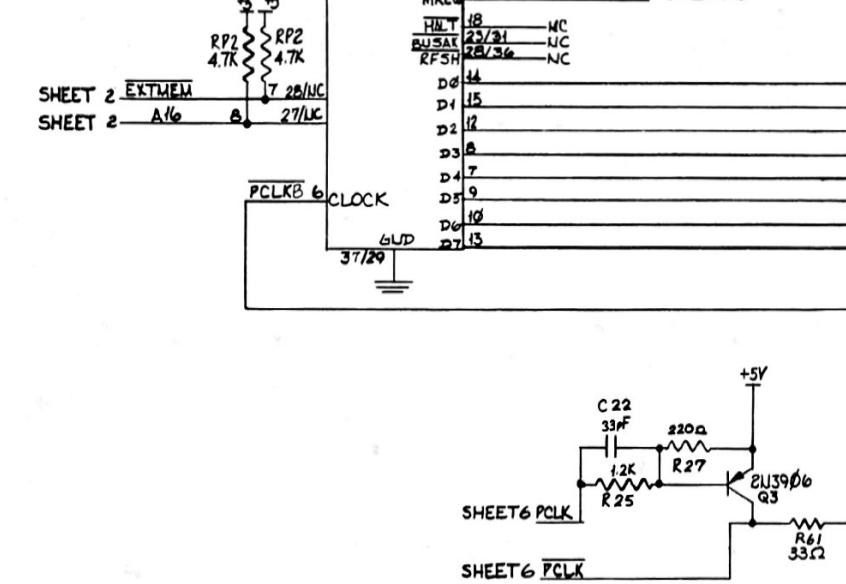
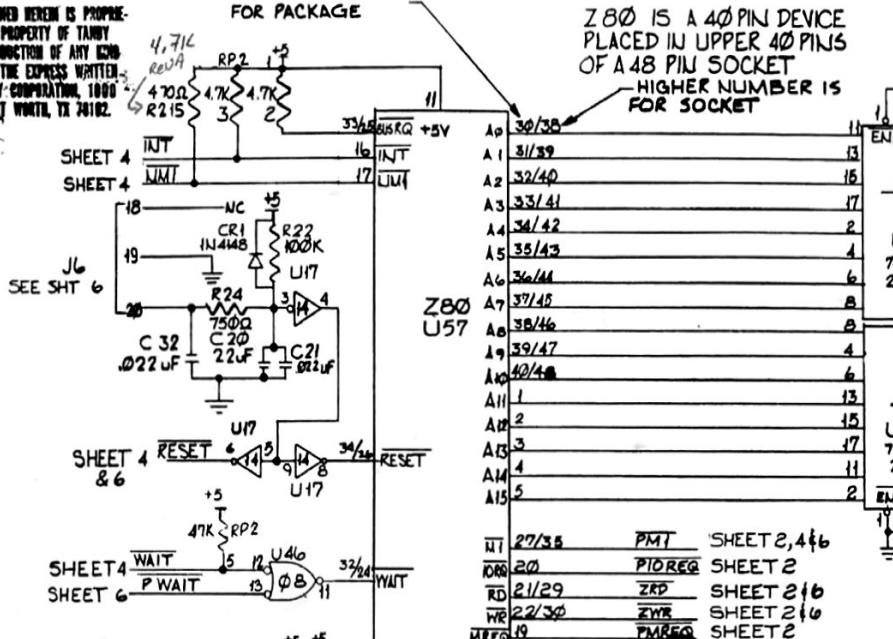
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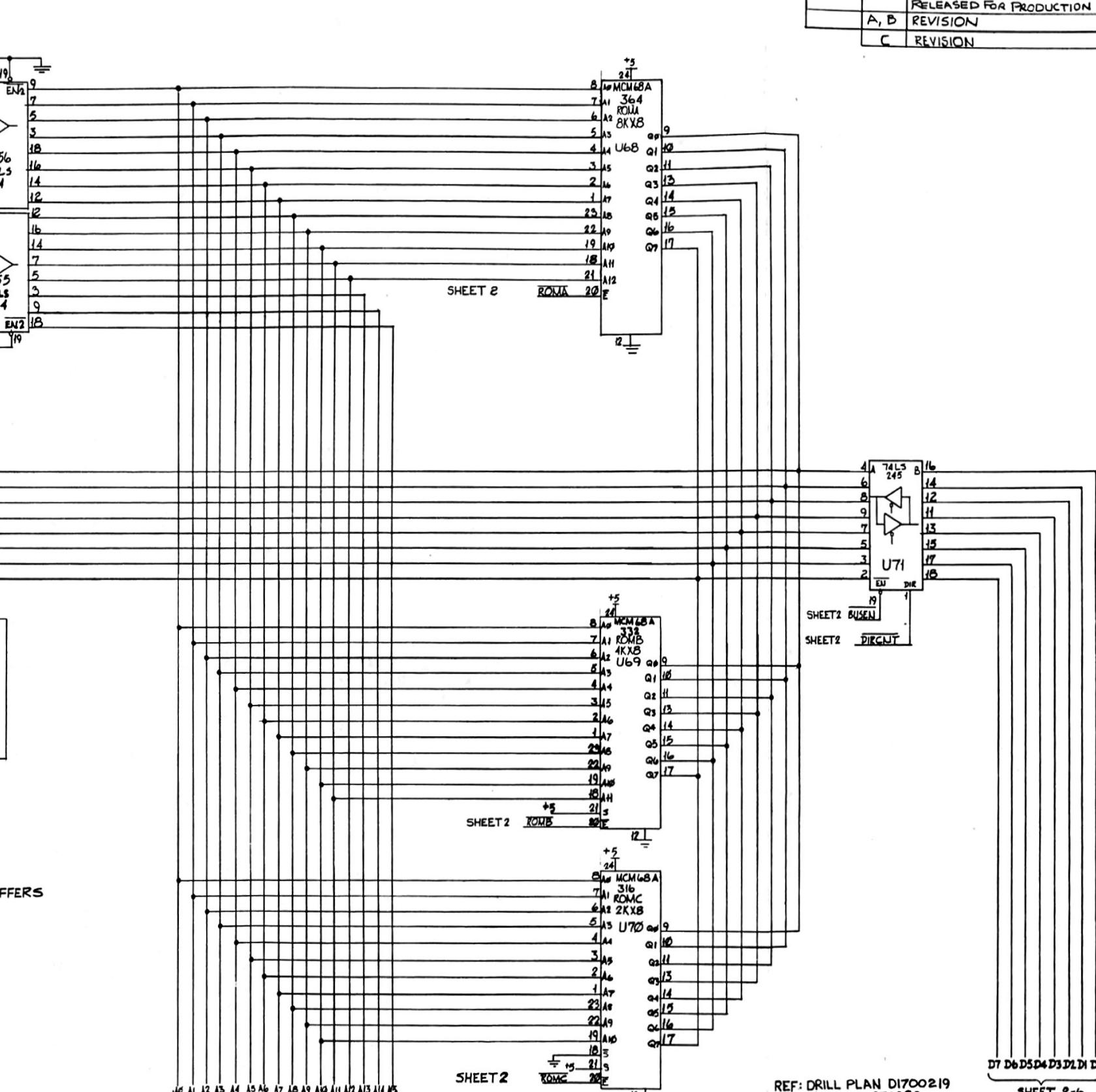
LOWER NUMBER
FOR PACKAGE

Z80 IS A 40 PIN DEVICE
PLACED IN UPPER 40 PINS
OF A 48 PIN SOCKET

HIGHER
FOR SOON



CPU, ROM, ADDRESS BUFFERS AND DATA BUFFERS



REF: DRILL PLAN D1700219
PART NO. 870929

MATERIAL		UNLESS OTHERWISE SPECIFIED			DRAFT S.D.HATFIELD	DATE 11-182	TITLE
		TOLERANCES		CHECK G.E.G.	DATE	SCHEMATIC-	
		.XX = ± .010 XXX = ± .005		DESIGN G.E.GAULKE	DATE 2/22/83	CPU/MAIN LOGIC	
		ANGLES = ± 1°		APD <i>Sawyer</i>	DATE 2/23/83	MODEL 4	
		HOLE DIA TOLERANCES		APD <i>Wharrel</i>	DATE 2/23/83		
FINISH		.014 - .250 = + .005				REV. C	
		.251 - .750 = + .008					
		.751 - UP = + .015					
		DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING	471				
		DO NOT SCALE THIS DRAWING	NEXT ASSY.	USED ON		DWG NO. 8000173	
					SCALE NONE	SIZE D	
					SHEET 1	OF 6	

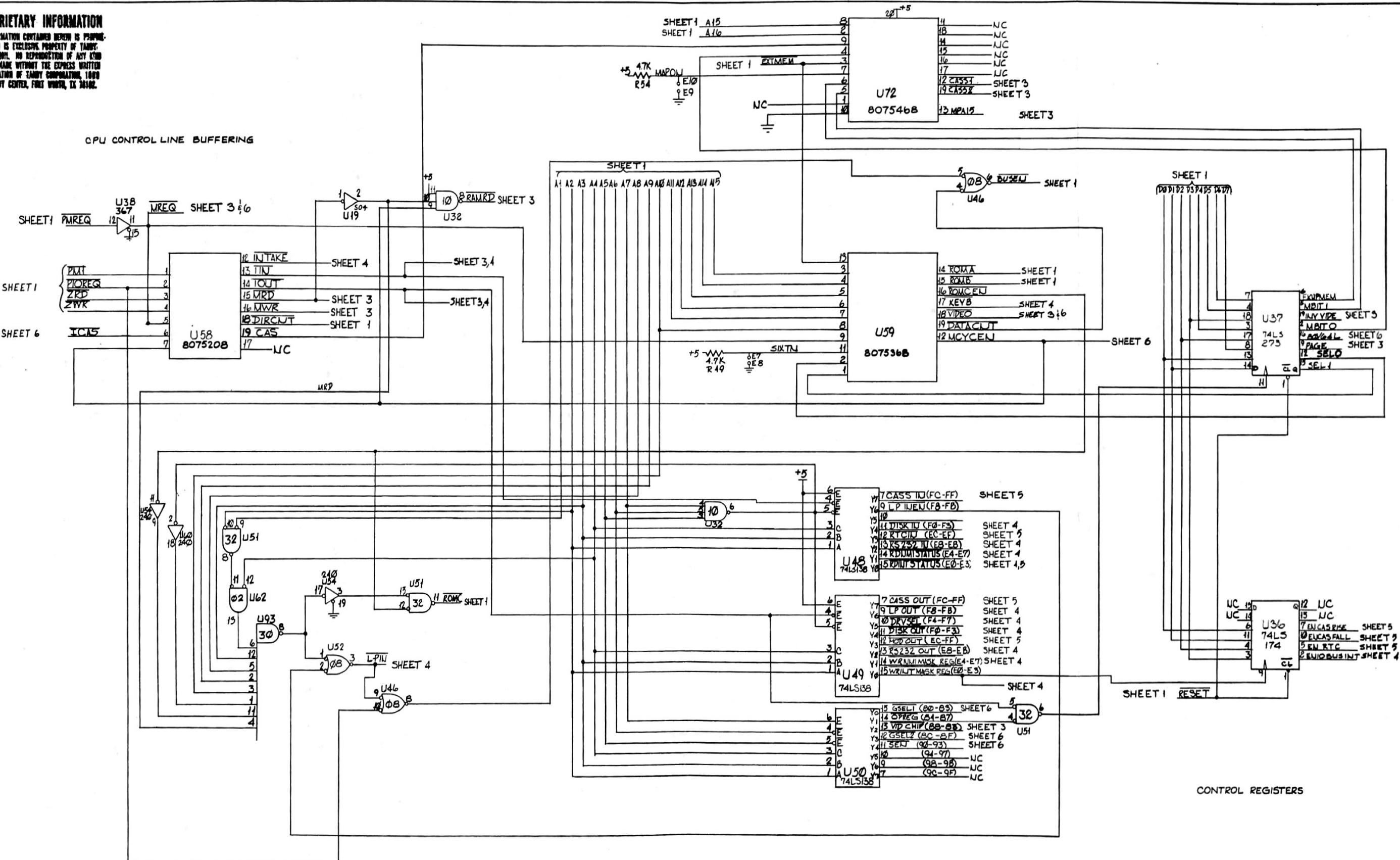
SCHEMATIC-
CPU/MAIN LOGIC
MODEL 4

tandy

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CPU CONTROL LINE BUFFERING



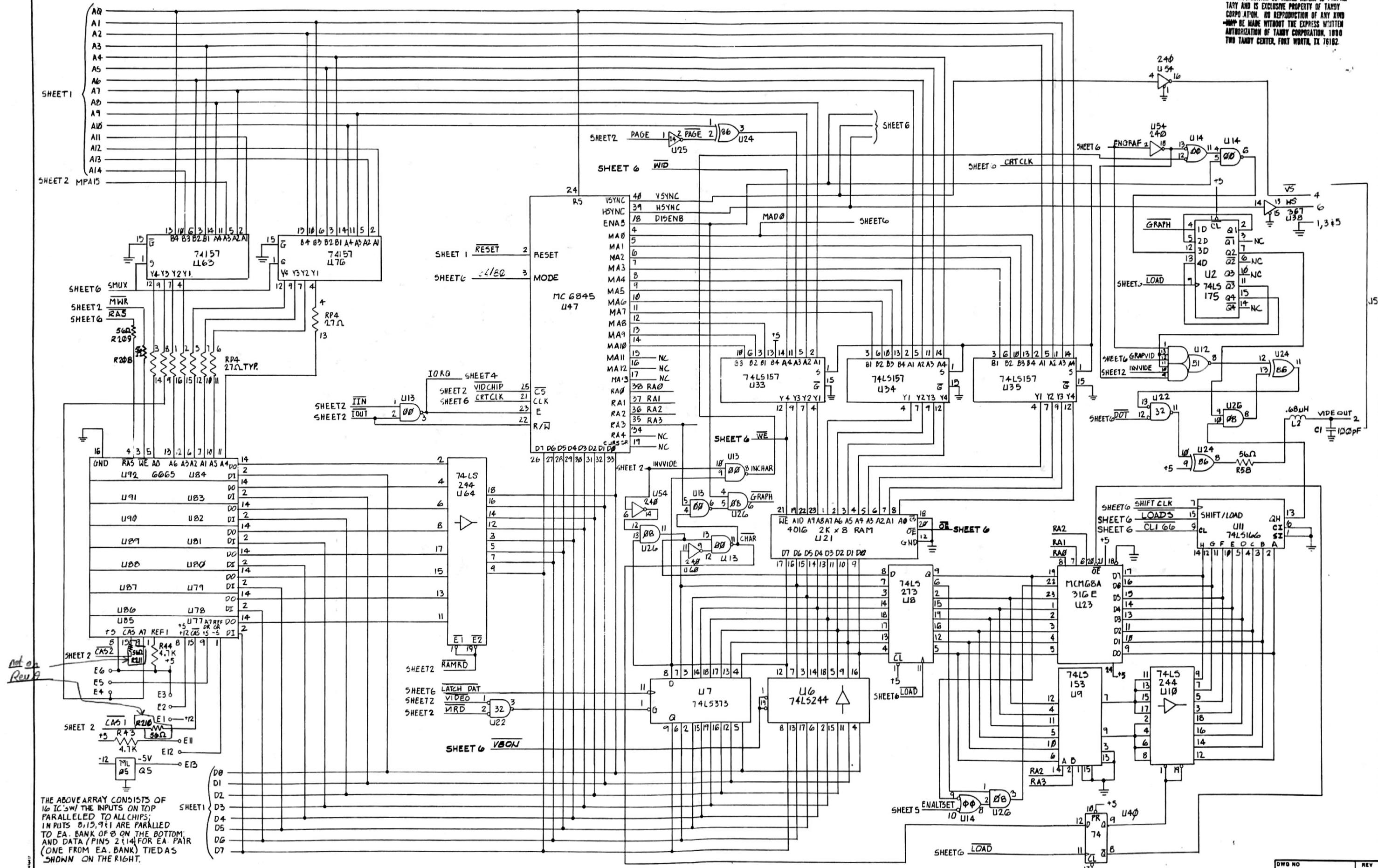
ADDRESS DECODE

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DWG NO	8000173	REV C
SCALE	NONE	
	SHEET 2	OF 6

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THE ABOVE ARRAY CONSISTS OF
16 IC'S! THE INPUTS ON TOP
PARALLELED TO ALL CHIPS;
INPUTS B, 15, 9, 1 ARE PARALLEL
TO EA. BANK OF 8 ON THE BOTTOM;
AND DATA/PINS 2 & 14 FOR EA. PAIR
(ONE FROM EA. BANK) TIEDAS
SHOWN ON THE RIGHT

DRAM

VIDEO RAM AND VIDEO INTERFACE

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DWG NO

R

80000173

1

HOME SHEET 3

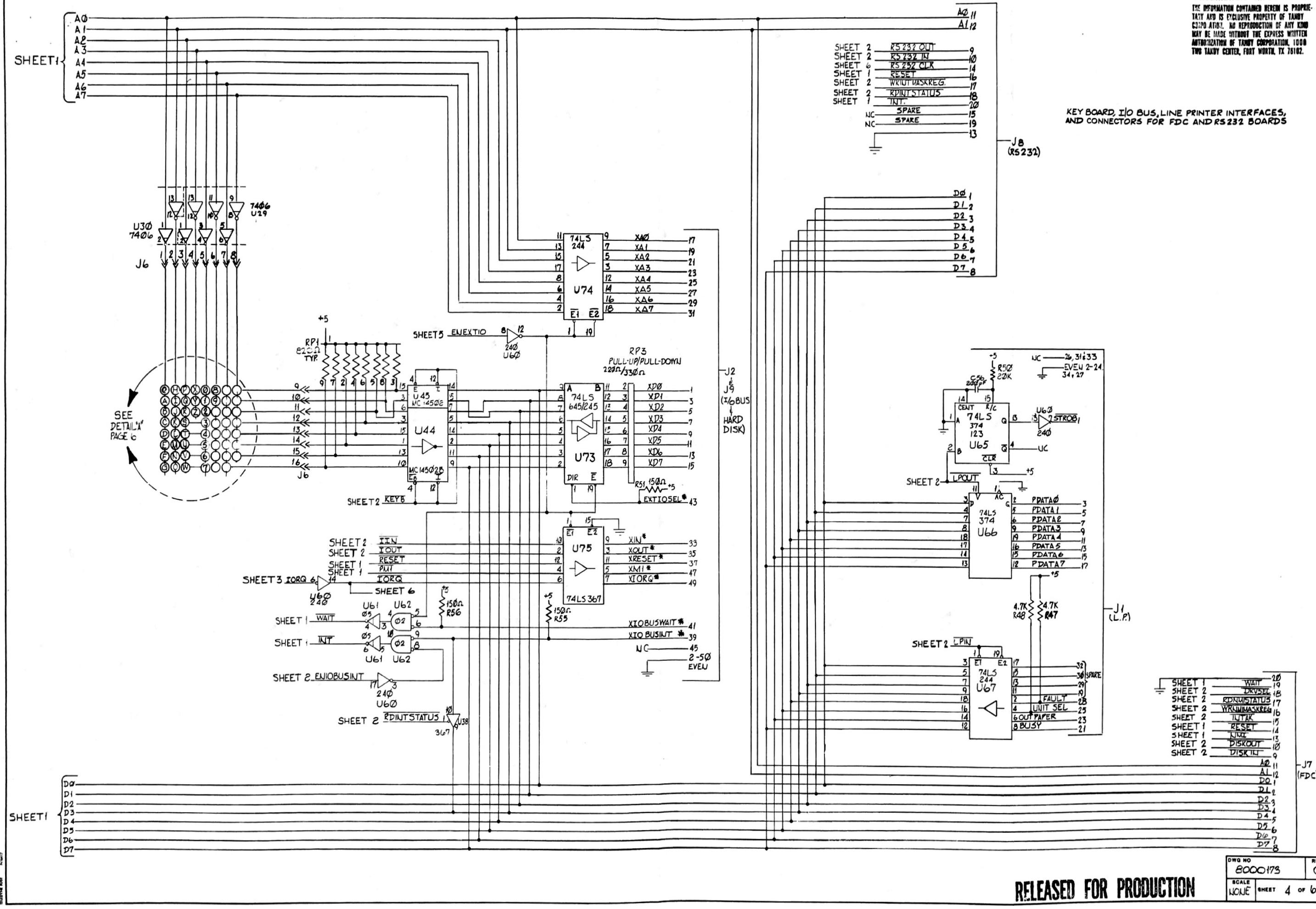
OF 6

10 of 10

1

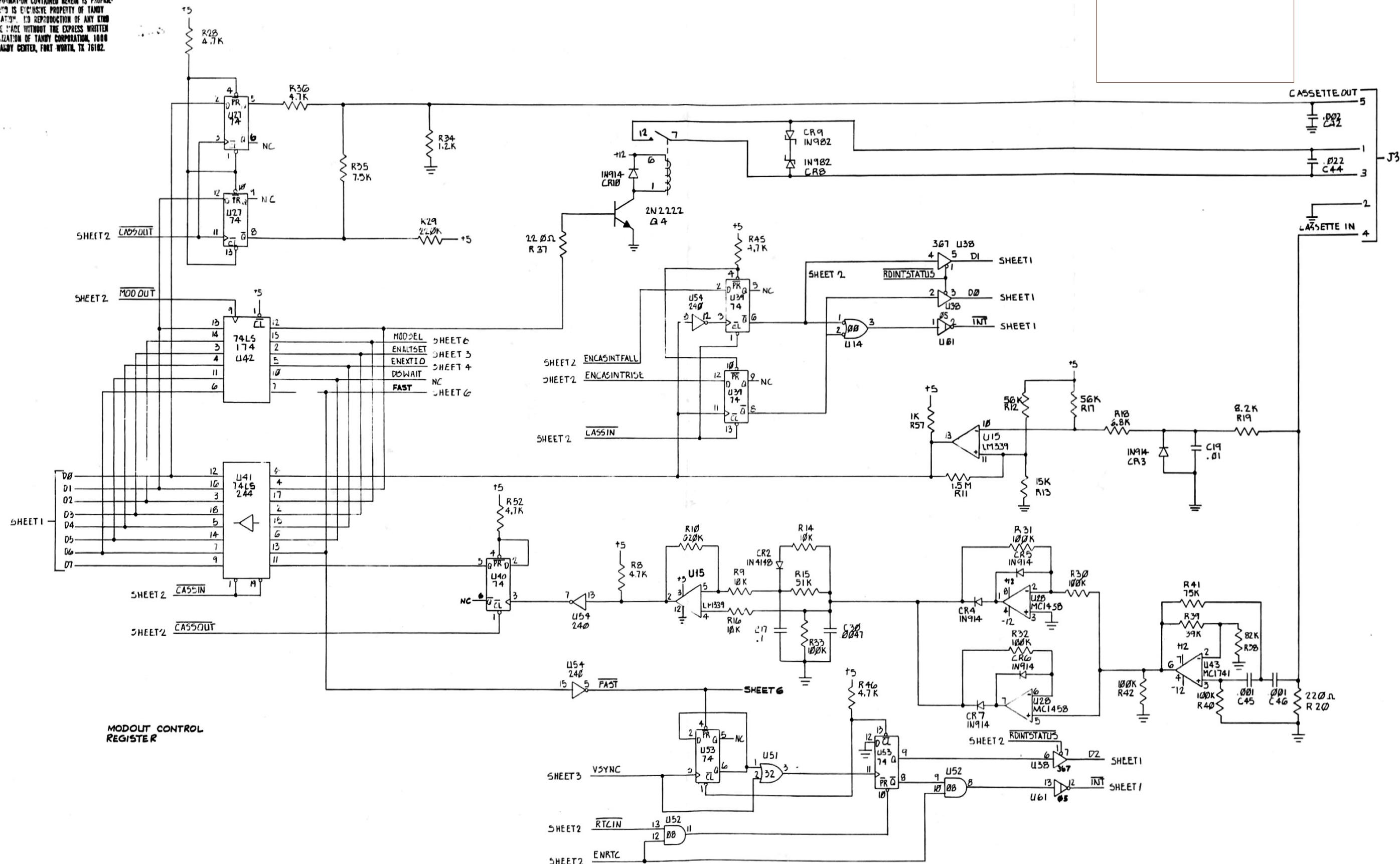
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TWO TANDY CENTER, FORT WORTH, TX 76102.



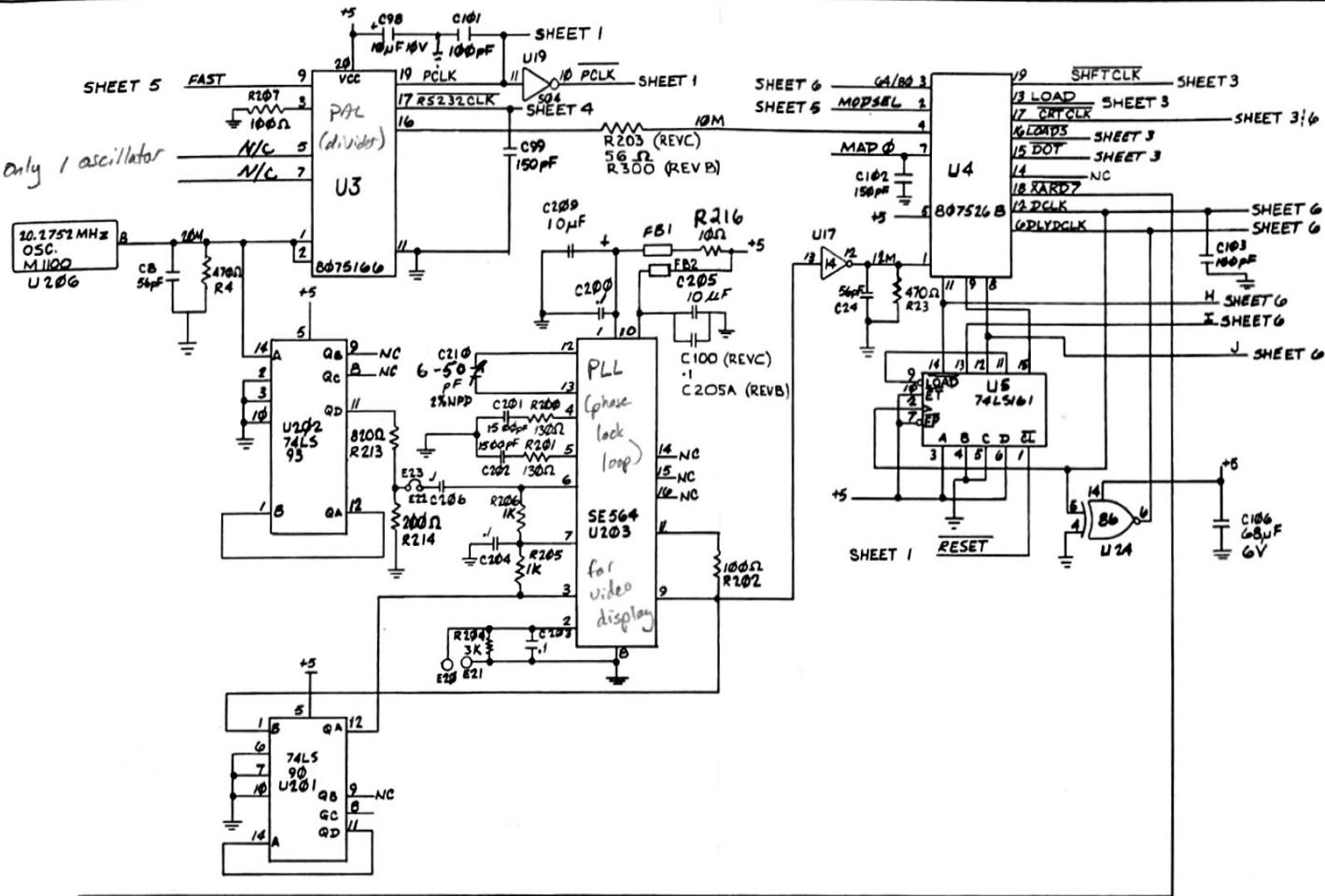
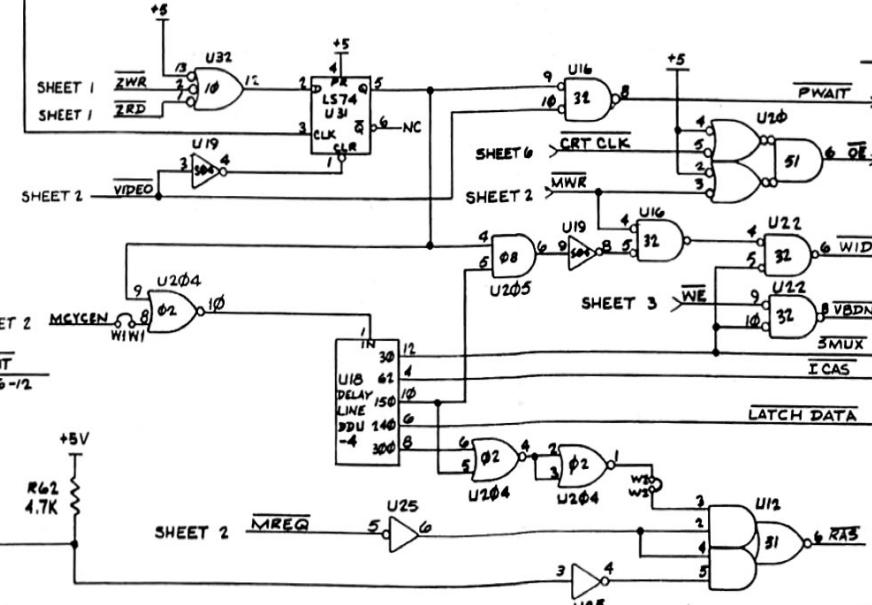
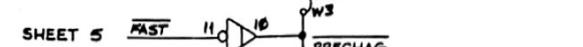
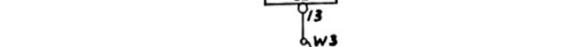
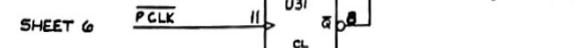
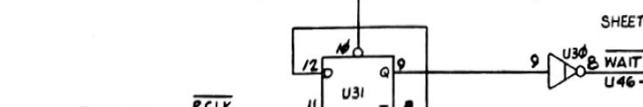
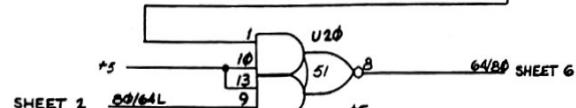
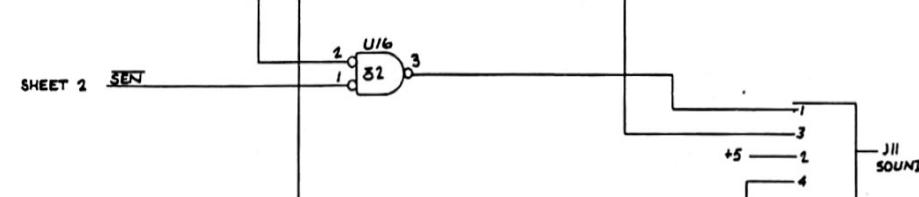
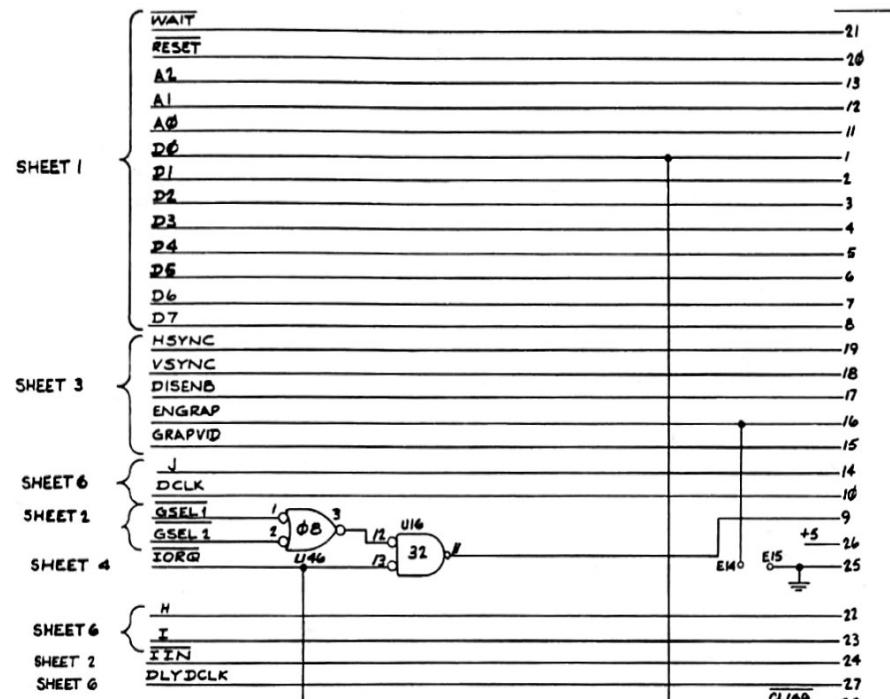
CASSETTE INTERFACE

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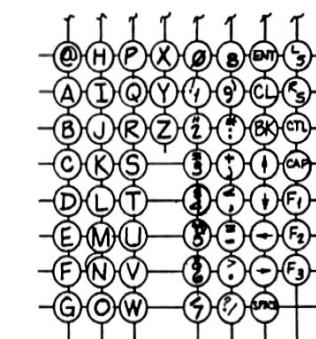
DWG NO	8000173	REV C
SCALE	NONE	
	SHEET	5 OF 6

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TANDEM CORPORATION, 1980
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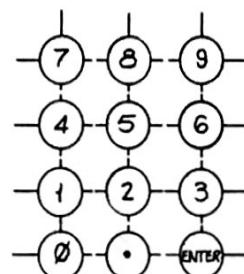
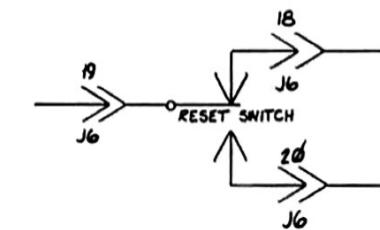
GRAPHICS AND SOUNDBOARD CONNECTORS



CPU AND VIDEO TIMING GENERATION



DETAIL "A"



THE ABOVE KEYS (THE NUMERIC KEYPAD)
ARE CONNECTED IN PARALLEL WITH SIMILAR KEYS
OF THE KEYBOARD MATRIX.

KEYBOARD DETAIL

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DWG NO	8000173	REV C
SCALE NONE	SHEET 6	OF 6