

**Radio Shack**

**Technician Series  
Diagnostics Software**

**TRS-80®**

**8" SYSTEM DIAGNOSTICS**

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## TABLE OF CONTENTS

PREFACE.....	i
COPYRIGHT NOTICES.....	ii
CHAPTER 1: SYSTEM TEST.....	1:0
Features.....	1:1
Quick Reference.....	1:2
Module Description.....	1:4
Cable Pinout.....	1:10
CTC Port addresses.....	1:11
CHAPTER 2: MEMII.....	2:0
Introduction.....	2:1
Quick Reference.....	2:1
The Screen.....	2:2
Module Description.....	2:2
Using MEMII.....	2:8
Theory of Banking.....	2:10
CHAPTER 3: DT-1 DIAGNOSTICS.....	3:0
General Description and Features.....	3:1
DT-1 Operation.....	3:2
Loading and executing DT1DIAG.....	3:2
Display Format.....	3:3
Module Description.....	3:5
Memory Map Decoding.....	3:6
Set up parameters.....	3:6
Cable Interfacing.....	3:9
Program Listing.....	3:10
CHAPTER 4: FDCALG.....	4:0
Late style board.....	4:1
Early style board.....	4:2
Waveforms.....	4:3
CHAPTER 5: HIRES.....	5:0
Introduction.....	5:1
Video Board Tests.....	5:2
Graphics Board Tests.....	5:4
CHAPTER 6: ARCTST.....	6:0
Objective.....	6:1
Installing ARCTST.....	6:1
Running ARCTST.....	6:3
Controls.....	6:4
Counters.....	6:5
Interpreting Errors.....	6:6

CHAPTER 7: 8 MEG HARD DRIVE.....	7:0
Introduction.....	7:1
Quick Reference.....	7:2
Technical Section.....	7:5
HDIFAC.....	7:7
HDDIAG.....	7:9
Adjustment Procedures.....	7:12
CHAPTER 8: 12 MEG HARD DRIVE.....	8:0
Introduction.....	8:1
Quick Reference.....	8:2
HDREL56.....	8:2
HDDIAG56.....	8:3
Technical Section.....	8:5
Adjustment Procedures.....	8:10
CHAPTER 9: 68000 DIAGNOSTICS.....	9:0
Introduction.....	9:1
How the Diagnostics Work.....	9:1
Operating the Diagnostics.....	9:3
Module Description.....	9:4
Other Programs.....	9:8
CHAPTER 10: AUTOTND and AUTODRV8.....	10:0
Introduction.....	10:1
Running the Programs.....	10:1
Commands.....	10:3
Status Display.....	10:5
CHAPTER 11: TDCTL.....	11:0
Description and Features.....	11:1
Loading and Operating TDCTL.....	11:2
The Display.....	11:2
Selecting the Drive.....	11:3
Control Functions.....	11:3
Test Description.....	11:5
Specifications and Jumpers.....	11:9
Component and Test Point Location Diagrams.....	11:11
Waveforms.....	11:13
CHAPTER 12: TDC.....	12:0
Features.....	12:2
Loading and Operating TDC.....	12:2
The Display.....	12:2
Selecting the Drive Type.....	12:3
Control Functions.....	12:3
Test Description.....	12:5
Specifications and Jumpers.....	12:9
Component and Test Point Location Diagrams.....	12:12
Waveforms.....	12:18

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**TRS-80®**

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**SYSTEM**

**Z-80 FAMILY DIAGNOSTIC TESTS**

**CHAPTER 1**

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**Radio Shack®**

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SYSTEM TEST FEATURES

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SYSTEM is a series of tests designed to test the Z80 family LSI parts in a Model II, Model 12, Model 16, or Model 16B. Currently these ICs are the DMA, the PIO, the SIO, and the CTC's if there are more than one. Two of these tests require loopback cables. The SIO loop back test will require a serial loopback cable and the PIO loopback test will require a printer to expansion bay loopback cable. The serial loopback cable and the parallel loopback connector are available from National Parts.

These programs require a minimum 64K computer and should be run on all Model II/12/16/16B computers as part of the normal checkout of the computer.

QUICK REFERENCE

---

```
*****  
*** WARNING WARNING WARNING WARNING WARNING WARNING WARNING ***  
*****  
***  
*** WHEN RUNNING THIS DIAGNOSTIC, BE SURE THAT THE TWO LOOPBACK ***  
*** CABLES ARE PROPERLY PLUGGED INTO THE COMPUTER. IF THEY ARE ***  
*** LEFT DISCONNECTED, ERRONEOUS ERROR MESSAGES WILL OCCUR. IF ***  
*** OTHER DEVICES ARE PLUGGED INTO THE COMPUTER, THEY MAY REACT ***  
*** IN AN UNPREDICTABLE MANNER TO THE TESTS BEING USED. ***  
***  
*****
```

## SYSTEM

---

**Execution:**

1. At TRSDOS READY type SYSTEM <ENTER>.
2. When the name and date appear, press <BREAK> to continue.

**OPTIONS:**

- <P> Brings up the menu of PIO tests.
- <C> Brings up the menu of CTC tests.
- <S> Brings up the menu of SIO tests.
- <D> Brings up the menu of DMA tests.
- <I> Brings up the menu of interrupt tests.
- <A> Will automatically run all of the above tests and report any errors at the end.  
*This should be the option normally used.*
- <B> Allows the user to enter the DEBUG mode.
- <T> Allows the setting of the timer function.
- <E> Allows the user to change the addresses of the ICs being tested.
- <HOLD> Causes the current test to pause.
- <BREAK> Aborts the current test and returns the user to the main menu.
- <ESC> Quits the current test.
- <Q> Exits the program and reboots the system.

SUB MENU FOR THE PIO, CTC, SIO, AND DMA TESTS

---

- <B> Checks the data bus between the Z-80 and the IC being tested.
- <P> Checks the functions of the IC. The PIO and SIO tests require a loopback connector.
- <I> Tests the ICs ability to interrupt the Z-80 processor.
- <A> The auto function runs all of the above tests automatically.

SUB MENU FOR THE EDIT MODE

---

To remap one of the ICs, the test device is first entered, in lower case, such as p0 for PIO channel 0 or c3 for CTC channel 3. Then the port address where the IC is located is entered, again in lower case, from 00 to ff.

SUB MENU FOR THE DEBUG FUNCTION

---

The DEBUG mode is used to read and write memory locations and ports either singly or continuously. The commands are:

```
r xxxx      : read from memory location xxxx
w xxxx dd   : write dd to memory location xxxx
i pp        : input from port pp
o pp dd    : output dd to port pp
```

Typing the first letter in uppercase will cause the command to execute in an endless loop which can only be broken by the <BREAK> key.

**MODULE DESCRIPTION**

---

**Main Menu**

The Main Menu controls the major flow of the program. It allows the user to modify the control flags, choose which chip to test, or enter the DEBUG mode. The menu also provides a counter which controls how many times each test is executed and an auto mode for burn-in testing. Just press the letter of the desired option. The control keys are displayed in the lower right hand corner of the screen. All except the <Q> key will work at any time. The <BREAK> key will finish the current pass of the test in progress and then return the status of that test. The <Q> key will reboot the system and the <HOLD> will stop the test to allow viewing of error messages, etc. The other options control the various tests and flags.

**Notes:**

The keyboard is scanned every NMI for input. If NMI's are not working there will be no keyboard. If the program locks up, reboot the system to TRSDOS READY and turn on the CLOCK. If the clock does not function properly, check the NMI interrupt system.

The error counters can only handle numbers up to 65535. If an error count ever exceeds that number it will wrap around to 0 and start over. Due to this wrap around effect, if a test is run a long time the counters may appear to show fewer errors than actually occurred.

**PIO Test**

The PIO test requires the use of a loopback connector to operate in any mode except the bus test mode. The "output" mode then writes and reads back an incrementing pattern to the channel B data port. If the data read back does not agree with the data written an error is logged. At the end a summary of the results is displayed on the screen.

The "program" test makes use of the loopback connector to test both channels of the PIO. The connector loops the output of channel B into the input of channel A. The program sets up the PIO to output from channel B and input from channel A. The program then writes an incrementing pattern to channel B and reads it back from channel A. If the data read back is different from the data written the test displays the data written and read back, and then logs an error. At the end of the test the number of errors are displayed.

The "interrupt" test also requires the loopback connector to function. This routine tests the PIO's ability to create a Mode 2 interrupt. Channel A is programmed to interrupt if Bit 0 goes high. This condition is created by giving the FDC a Force Interrupt command. If this test fails be sure to check that the FDC is actually trying to cause an interrupt. Channel B is programmed to interrupt on a data transfer acknowledge. This feature demonstrates the capability of an using an interrupt-driven printer but this feature is not currently used by any RADIO SHACK software.

**Notes:**

The "program" and the "interrupt" tests both require the FDC to be functioning properly. If both tests fail, suspect the FDC section.

**DMA Test**

The DMA "bus" test writes an incrementing pattern to the DMA address registers then reads it back. If there are any differences the test displays the value written and the value read back, and then logs an error. At the end of the test the number of errors are displayed.

The DMA "program" test exercises the DMA's block move capabilities. First a dummy move is done to white out the screen in order to get the DMA warmed up and ready to go. Then a memory-to-memory transfer is attempted from 7000H to A000H and the results verified. Then a memory-to-port transfer is attempted from A000H to the FDC data port and the results verified. With any of the modes if the data transferred is not the same as the source data an error is logged.

The DMA "interrupt" test checks the DMA's ability to interrupt at the end of a block move. The DMA is programmed for interrupt mode and a move is attempted. If no interrupt is received or if more than one interrupt is received the test will log an error.

**Notes:**

The "program" test uses the DMA in a Force Ready mode. The "program" test does not test the DRQ line from the FDC or the XFFER\* line to the DMA. If these lines are not functioning properly the test will not log any errors but floppy disk I/O may not work properly.

**SIO Test**

The SIO test also requires a loopback connector for any mode other than the "bus" test. The bus test programs SIO channel B with an incrementing pattern to the interrupt vector register then reads it back. If the number read back is not equal to the number written the test displays the number written and the number read back, and then logs an error.

The "program" test requires a loopback connector to function properly. The "program" test transmits from one RS232 channel to the other changing baud rates, word length, and parity. The routine will continue transmitting even during an error condition to allow tracing of signals. Errors cause the data written and data read at that baud rate and word length to be left on the screen. At the end of the test the number of errors is reported.

The "interrupt" test also requires the serial loopback connector. This test transmits and receives characters in an interrupt-driven mode. The number of interrupts received is displayed on the screen. If no interrupt is received or if more than one interrupt is received the test will log an error.

The "bus" test does not test bit 1, bit 2 or bit 3 of the SIO command port. The tests reprogram the SIO for each byte sent. This is different than the way the operating system does serial I/O.

**CTC Test**

The CTC "bus" test programs the CTC for the timer mode, writes a count to register  $\emptyset$ , and then reads it back. If the number read back is not the same as the number written an error is logged and an error message is displayed along with the value written and the value read back.

The CTC "program" test uses the CTC in counter mode, timer X16, and timer X256 mode. This test uses software timing loops and requires the wait state jumpers to be in standard Model 2 positions. The test programs the CTC to count from FFH to  $\emptyset\text{1H}$  then compares the number in the count register of the CTC to its own count and logs an error if there are any differences.

The CTC "interrupt" test programs the CTC to generate an interrupt at the end of its count. Each channel is programmed to count from 1 and the number of interrupts generated from each channel is displayed. Errors are logged if no interrupts are received or if more than one is received.

**Notes:**

All the tests rely on software timing loops to function properly. If a clock other than 4 MHZ is used or if any wait states other than those in a standard Model II are added or deleted the test will not give accurate results. If a great number of errors occur during this test, check the WAIT state jumpers first.

**Interrupt priority Test**

This routine tests the daisy chain interrupt logic in the Z80 family LSI ICs. The interrupt test disables interrupts in the CPU then causes all of the Z80 family chips to generate interrupts. Then interrupts are enabled and the order in which the interrupts were received is displayed on the screen. Errors are logged if the interrupts do not occur in standard Model 2 order.

**Notes:**

The test will log errors if the interrupts are received in any order other than that of a standard Model 2. If the edit defaults option is used this will cause errors to be logged.

**Debug Mode**

The debug mode is designed to help find faults at the board level. There are four basic commands:

```
r xxxx      : read from memory location xxxx
w xxxx dd  : write dd to memory location xxxx
i pp        : input from port pp
o pp dd    : output dd to port pp
```

The upper case of these commands do the same operation only in a loop mode which can only be stopped by the BREAK key. The debugger accepts hex numbers in either upper or lower case and also a few special port numbers:

```
CTC = the port currently mapped to channel 0 of the CTC
PIO = channel B data port of the PIO
SIO = channel A command port of the SIO
DMA = DMA command port
FDC = FDC data port
```

These allow quick loops to be set up without having to remember port numbers. The command "0 CTC 55" will continuously output a 55 hex to whatever port CTC channel 0 is mapped. An oscilloscope can then be used to verify the data and port decoding.

**Notes:**

The loop mode can only be exited by the <BREAK>. In order to do this NMI's must be left on which causes code other than just the loop to be executed. The routine used to convert the input will take any key inputs and convert them to binary.

**Auto test**

This option is used for unmonitored testing of a machine. The auto mode will execute each of the tests and report status at the end. The timer can be used to control the number of times each test is executed. Each loop requires approximately 15 minutes so for an overnight test a count of 50 works well.

**Notes:**

The Auto test uses the same routines as the standard test. Any notes that apply to them also apply during the auto test.

**Timer**

The timer provides a means of executing any test a set number of times. The timer will accept a count up to 65534. A count of 0 will put the test in a continuous loop. Counts are entered in decimal.

**Notes:**

Any input other than a decimal number will abort the command.

**Edit Defaults**

This provides the user with a way of changing the ports to which the LSI's are mapped. For example the CTC can be mapped to port C4 thru C7 and the CTC test will then test the hard disk CTC. Other hardware considerations may have to be taken into account. With the hard disk a  $\emptyset A$  must be output to port Cl to enable the hard disk board before the test will operate. Also the results may be different than expected. With the hard disk the counter test will fail because the CTC is used in a different manner than in the CPU board. By using the edit mode with the interrupt priority test all of the interrupts in the machine can be tested. First run the CTC interrupt test then map channel  $\emptyset$  to the next CTC such as the hard disk and run the CTC interrupt test again. The thing to remember is that the interrupt vector is only programed into channel  $\emptyset$  so each CTC must be tested individually to get the proper vector. After all the CTC'S have been programed then the interrupt priority test can be run and the order in which the interrupts were received can be determined. The test will log errors but this only means the interrupts occurred in an order different than the test was expecting. Also note the CTC is used as a baud rate generator for the SIO. If the CTC is mapped to another port the SIO tests may not function properly.

**Notes:**

When testing CTCs other than the one on the CPU board, the tests may appear to generate errors. This is due to the fact that the CTCs are probably connected differently than the program expects. See the appendix on the addresses of other CTCs and the responses to expect.

**Appendix A****Loopback cable pin assignments****PIO Loopback Connector**

BRDY	J2.1	<-->	J2.19	BSTB
DØ	J2.3	<-->	J4.44	WP
D1	J2.5	<-->	J4.1Ø	2 SIDE
D2	J2.7	<-->	J4.12	DO
D3	J2.9	<-->	J4.42	TRACK ØØ
D4	J2.11	<-->	J2.28	FAULT
D5	J2.13	<-->	J2.25	PSEL
D6	J2.15	<-->	J2.23	PE
D7	J2.17	<-->	J2.21	BUSY

**SIO Loopback Connector****Port A      Port B**

2	<-->	3
3	<-->	2
4	<-->	5
5	<-->	4
6	<-->	2Ø,8
7	<-->	7
2Ø,8	<-->	6

**Appendix B****Other CTC port addresses**

When other CTC's are used for the CTC test, the counter test will fail.  
This is normal.

**Hard disk CTC****channel #      port address**

c0	C4H
c1	C5H
c2	C6H
c3	C7H

Before testing the hard disk CTC an OUT must be done in the Debug mode.  
The command is 'o c1 0a'.

**ARCNET CTC****channel #      port address**

c0	B0H
c1	B1H
c2	B0H
c3	B1H

The other two CTC channels are not available on the ARCNET board.

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MEMII

Z-80 BASED MEMORY DIAGNOSTICS

CHAPTER 2

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**Radio Shack®**

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INTRODUCTION

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MEMII is a powerful diagnostic tool designed to root out memory problems in the Model II computer. It can also be used to check Model II equivalent portions of the Model 16 computer.

It will test the Model II CPU card BOOT ROM, Model II memory cards, Model II hard disk interfaces with memory, and Model II video and graphics cards. In short, it will enable the technician to test the memory on almost any device that can be logically inserted into the Model II memory scheme. MEMII does not check the 16-bit memory sections found in the Model 16 or upgraded Model IIs and 12s.

This test has been constructed so that multiple boards can be tested at one time. Questionable boards can be inserted into a known good machine for test. Also, boards that have multiple errors to the extent that other memory test would not even acknowledge the presence of the board can be tested.

In addition, there is a timer function on the board so that a schedule can be set up for unattended testing of selected boards.

Quick Reference

---

MEMII is provided on a TRSDOS 2.0a diskette. It will run ONLY on TRSDOS 2.0a, 2.0b, or 4.x. Do NOT transfer this to another operating system as the results are unpredictable.

MEMII is initiated by typing **MEMII <ENTER>** at TRSDOS Ready. The program will find all RAM that is in the system in either the Bank select memory map or the video map.

There are a few things that MEMII will not test. It will not test the Model 16 memory. Since the Model 16 uses page 0 as the memory location when looking from the Z80, this page is not tested by this program. It is not even looked at and does not appear in the memory table.

All RAM test start at location 29FFH. MEMII will not test below this address. To test a board below this address, replace the board with a known good board and jumper the suspect board using the instructions in the supplement titled **BANKING**.

All test operations can be halted by pressing the <BREAK> key. Most test operations can be paused by pressing the <HOLD> key. If a test displays errors, the program will halt after listing 12 errors to the screen, it will continue testing by pressing the <HOLD> key. The <Q> key is used to exit the program and reboot the system. Direct re-entry to TRSDOS from MEMII is not supported.

#### The Screen

---

The MEMII video display is organized into three sections. The top is the version and copyright notice. The middle is the status section and the bottom section is the command listing.

The status section will tell you three things of importance. The first is the memory size defined by the system. This total also includes the RAM below 29FFH which is not available for testing. On entry to MEMII the program will attempt to locate all the RAM in the system, good or bad, and it will be in this total. To see where the RAM was found, use the <D> function. You do not have to test all the RAM in the system, that is, you can remove it from the system using the <D> command if you don't want to test it. Likewise, you can define RAM as in the system that didn't show up on entry. This is especially useful in tracing problems on boards that are so bad that the system doesn't know that they are installed.

Next is the video size. It will display how much video RAM it found in the system. It will look for the standard 2K of video RAM as well as the Model II graphics board RAM. Again, you can use the <D> command to add or remove memory from testing.

On the right side is the clock display. For information on the use of the clock/timer function, see the detailed description in the Using MEMII section.

#### Module Description

---

The MEMII Memory Test consists of several memory tests aimed at completely testing all memory within the TRS-80 Model II. Each test provides a means of isolating memory faults and determining if the fault is a RAM I.C. or the associated circuitry.

Upon execution of the program, the sizes and allocation of RAM and Video memory are determined and stored. The Main Menu is then displayed giving the title, RAM and Video Memory sizes, clock, and a menu of the memory tests and test functions. The program then waits for a selection of a memory test or test function.

Three keys are recognized as control functions for use in control of each memory test: <HOLD>, <BREAK>, and <Q>. The <HOLD> key is a Halt/Continue function which allows the user to halt an executing memory test to check the test status information or stop the scrolling of errors being displayed. Halt is displayed as the test status to indicate to the user that the memory test is in a halt mode. If a memory test has already been halted, the <HOLD> key will allow the memory test to continue testing. The <BREAK> key will allow the user to return to the Main Menu at any time. The <Q> key is a Quit function which allows the user to terminate the program and reboot TRSDOS.

The <HOLD> key is only functional during execution of a memory test, the <BREAK> and <Q> keys are functional at all times.

The main program has three test functions: Auto Function, Timer Function, and Display>Select Memory Function.

#### <A> Auto

The Auto Function will advance through each test sequentially, displaying the title, status of the test, and number of errors after each test has executed. If Run Time is set during Auto Mode, each test will run for the set run time and then advance to the next memory test.

#### <T> Timer

The Timer Function consists of 4 functions: Set Run Time, Delete Run Time Mode, Continuous Run Time, and Set Clock. Set Run Time will allow the user to select the amount of time a memory test will execute. After the preset time has elapsed, the test will end and display all status information and errors. Delete Run Time Mode will delete the set Run Time or Continuous Mode. Continuous Run Time will cause a memory test (except Shadow ROM Checksum) to execute continuously. Set Clock will allow the user to set the program clock.

Note: If enough time is not allowed for a memory test to execute at least one sub-pass, the status of the memory test may not be valid. If this condition occurs, the message 'Not Enough Time to Complete All Test' will be displayed.

**<D> Display>Select memory**

Display>Select Memory Function will display a RAM and Video Memory Allocation Map of all current memory. After display of the memory maps, it allows selection of 4 functions: Select RAM or Video Memory, Delete RAM or Video Memory, Map RAM and Video Memory, and Return to Display>Select Menu. Select RAM or Video Memory allows manual selection of a minimum of 16K RAM and/or Normal or Graphics Board memory. Delete RAM or Video Memory allows deletion of the RAM or Video memory. The purpose of the above 2 functions is to allow the user to force the computer to test or ignore any desired part of memory. Map RAM and Video Memory will recalculate the sizes and allocation of both RAM and Video memory. MEMII will update the display any time memory is added or deleted to match the Map. Return to Display>Select Menu will do as titled.

The Memory tests are as follows:

- <N> Normal Video RAM Test
- <G> Graphics Board RAM Test
- <S> Shadow ROM Checksum
- <C> Checker Board RAM Test
- <M> Modified Address RAM Test
- <O> Coincidence Address Test
- <B> Bank Select RAM Test

**<N> Normal Video RAM Test:**

The Normal Video RAM Test provides a means of testing the normal video RAM (2K). This test executes 256 sub-passes to complete 1 pass. Each sub-pass will completely fill and check all Normal video memory. During each sub-pass, test patterns, which are generated by the same method used in Modified Address RAM Test, are written in video memory and then read back and compared. All 256 byte combinations are checked at all memory locations. As errors occur, each will be logged until 12 errors have been accumulated. After 12 errors, the test will automatically halt and the test status information and errors will be displayed. The error information given are: Address, Data Written, Data read, and Bad Bit(s). Depressing the <HOLD> key will allow the test to continue. This test will halt each time 12 errors have accumulated.

All control functions are operational during execution of this memory test.

**<G> Graphics Board RAM Test:**

RAM memory (19.2K). This test functions the same as Normal Video RAM Test except it does not display the contents of the video memory during testing. If an error occurs, Y/X Position, Address, Data Written, Data Read, and Bad Bit(s) are displayed. The Y/X Position (Y/X-Pos:) is the Y/X coordinates of the video screen and the Address is the true address location of the RAM chips. The test will display the first page of errors and then halt. Depressing the <HOLD> key will continue the test and scroll any additional errors.

All control functions are operational during execution of this memory test.

**<S> Shadow ROM Checksum:**

The Shadow ROM Checksum provides a means of testing the Shadow ROM. This test will calculate and display the checksum. At the end of the test the message FINISHED will be displayed.

The Timer and Continuous function are not operational during this test. All other functions operate as stated.

**<C> Checker Board RAM Test:**

The Checker Board RAM Test provides a quick RAM memory test. This test executes 4 sub-passes to complete 1 pass. During each sub-pass, all mapped RAM memory is filled with a checker board pattern and then read back and compared. The first sub-pass the checker board pattern is 00H-FFH, the second sub-pass is FFH-00H, the third is 55H-AAH, and the fourth is AAH-55H. If an error occurs, the Page #, Address, Data Written, Data Read, and Bad Bit(s) are given. The test will display the first page of errors and then halt. Depressing the <HOLD> key will continue the test and scroll any additional errors.

All control functions are operational during execution of this memory test.

**<M> Modified Address RAM Test:**

The Modified Address RAM Test provides a complete and thorough RAM memory test. This test executes 256 sub-passes to complete 1 pass. During each sub-pass, all mapped memory is filled, read back, and compared. The test pattern used is generated from the address and is written to that location. The test pattern is generated by XORing the MSB and LSB of the address with a mask byte which is incremented after each sub-pass. This generates a unique and fairly random pattern though out memory. All 256 byte combinations are tested at all address locations. If an error occurs, the Page #, Address, Data Written, Data Read, and Bad Bit(s) are giving. The first page of error will be displayed and then the test halted. Depressing the <HOLD> key will continue the test and scroll any additional errors generated.

All control functions are operational during execution of this memory test.

Note: All RAM memory tests start testing memory at 29FFH. If the problem is suspected to be between 0000H and 29FEH, configure the memory board under test to another Bank such as Pages 2 and 3, then install a known good memory board at pages 0 and 1. Delete pages 0 and 1 from RAM Memory Allocation Map and then run one of the RAM memory tests. This will allow testing of all 64K on the suspected bad memory board. See the section on BANKING for more information.

**<0> Coincidence Address Test:**

The Coincidence Address Test provides a means of testing for possible shorted address lines. This test executes 6 sub-passes to complete 1 pass. During each sub-pass, all mapped RAM memory is filled with test patterns generated from the address and then is read back and compared. The test patterns are generated by dividing the address into 4 nibbles and writing 2 of the 4 nibbles to that address location. (Example: Address = 95AFH - Nibble #1 = 9H, Nibble #2 = 5H, Nibble #3 = AH, and Nibble #4 = FH) During the first sub-pass, the test patterns are generated by using nibbles 3 & 4 or the LSB of the address, the second sub-pass, nibbles 1 & 2 or the MSB of the address, the third sub-pass, nibbles 1 & 4, the fourth sub-pass, nibbles 2 & 3, the fifth sub-pass, nibbles 2 & 4, and the sixth sub-pass, nibbles 1 & 3. This will test all address lines to all others. When the test reads back the data, a bit is rotated though the test pattern address area allowing only certain address location to be checked.

Example: If in the first sub-pass, the test pattern address area would be nibbles 3 & 4 or the LSB of the address. If the start address was 8000H, the first location read back would be 8001H, then 8002H, 8004H - 8008H, then 8101H, 8102H, etc. This allows the test to determine which address line was in error, if any errors occur. When an error does occur, the Page #, Address, Data Written, Data Read, and Possible Fault will be displayed. Possible faults will indicate any address line pulled high when it should have been low and any that is grounded when it should have been high. If only one address line is displayed, it alone is pulled high or grounded. If two or more are displayed, it will possibly mean that they are shorted together. Also, bad RAM or a Bank Select problem can cause erroneous errors to be indicated. Check these areas of memory if above conditions occur.

The first page of errors are displayed and the test will be halted. Depressing the <HOLD> key will continue the test and allow scrolling of any additional errors.

All control functions are operational during execution of this memory test.

**<B> Bank Select RAM Test:**

The Bank Select RAM Test provides the means of testing the Bank and Page Select circuitry on each RAM memory board. This test executes 1 sub-pass to complete 1 pass. The test writes FFH to 128 non-adjacent locations on every page, then starting with page 15, it will come back and rewrite one page with its own page #. The test will read these 128 locations on each mapped page and compare for an FFH or the page number if it was the last page to be rewritten. This allows the test to check if by selecting one page it also selects another page in error. If an error occurs, the error is checked to determine if valid. It compares the data read to the page # of the last rewritten page, if not the same, the error is not valid and test continues checking for other errors. Second, the test will check if 65 consecutive errors have occurred. This will eliminate the hard disk interface from being reported as an error. If not, no error is displayed and test continues checking. If both above conditions are met, then the error will be displayed giving the Page Selected and the Page Selected in Error. The first page of errors will be displayed and then the test halted. Depressing the <HOLD> key will continue the test and scroll any additional errors.

Note: Because of the feature to eliminate the false reporting of an error when testing the Hard Disk Interface boards, this test will not report errors in bank selecting on boards of 16K OR LESS.

All control functions are operational during execution of this memory test.

### Using MEMII

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There are three function keys and three control keys displayed on the right side of the screen in the main menu. They are:

- <A> Auto function
- <D> Display function
- <T> Timer function
  
- <HOLD> Hold/continue key
- <BREAK> Return to main menu
- <Q> Reboot to TRSDOS

These are all described at the beginning of the Module description. This will be a sample use of these functions.

#### <D> Display Function

Press the <D> key. A map of the system will be displayed. Any defined location with memory will be displayed as an X in a white block. Notice the lack of Page # Ø in the map. This is intentional. It is not the same as the Base Page. It cannot be accessed using MEMII.

#### Deleting Memory

If you don't want to test a particular portion of memory, Use the Delete function to remove it from the map. Press the <D> key. The program will ask if it is Video or RAM (R or V) you want to delete. Assume that we don't want to waste time testing the video looking for a memory problem, so hit the <V> key. The program will then ask Normal or Graphic (N or G). Hit the <N> key and notice that the X block for the video RAM turns off. At this point the display should not show the video RAM in the total at the top of the screen.

If you had selected RAM instead of the Video, the procedure would be similar. For example, the Hard disk interface will normally show up on page 14 and 15 in the map. This is because of the lack of a data bit on the page select for that board. In continuous testing, the hard disk interface would be tested twice on each pass through the map instead of once. You can delete page 14 by hitting the <R> key for RAM and then typing 14<ENTER> for page 14.

#### Selecting Memory

The <S> key works the same as the <D> key, only it ADDS memory to the map instead of taking it away.

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**Mapping Memory**

The system will hunt and find memory just like at entry to the program by typing <M> for Map. This is useful if you have modified the Map and want to return to what was originally in the system without rebooting.

**<A> Auto Function**

Pressing the <A> key makes the program fall through each of the test listed in the Module section.

**<T> Timer Function**

Pressing the <T> key lets you access the Timer control function. These are:

- <R> Set Runtime mode
- <D> Delete Runtime mode
- <C> Continuous Runtime
- <S> Set clock

**<R> Set Runtime mode**

Pressing the <R> key lets you set the Runtime mode. This is the maximum amount of time each test will run before going to the next test. Care must be used so that each test is allowed at least one complete pass before continuing on to the next test.

**<D> Delete Runtime mode**

Pressing the <D> key deletes the Runtime mode and lets the test run normally.

**<C> Continuous Runtime**

This lets you set up the program for continuous testing, such as overnight or unattended for a day.

**<S> Set clock**

Pressing the <S> key lets you set the real time clock. It is similar to the TRSDOS clock except all the information is required, including the seconds.

**Banking and Page select**

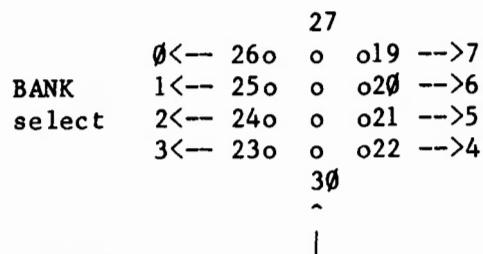
To understand Banking and Page select, an understanding of how the Model II addresses its memory is first required. It is known that the Z80 in the Model II can address up to 64K of RAM, but how is that done in the Model II?

The total of 64K of RAM that is possible in a Model II is divided into two 32K sections. The lower section, addresses 0000H - 7FFFH, will be called the BASE PAGE. This is because it can never be changed out of the system. The upper section, addresses 8000H - FFFFH, will be called the SWITCHABLE PAGE. No matter what is done, the Z80 can only look at 64K at one time -- a BASE PAGE of 32K and one SWITCHABLE PAGE of 32K.

The Model II MUST have a BASE PAGE in the system to power up. The SWITCHABLE PAGE is optional. This means that somewhere in the system, a memory card must have the BASE PAGE jumpers installed. Only one card can have these jumpers.

With a memory board laying in front of you with the motherboard connector toward you, the BASE PAGE jumpers would be to the upper right in the group of jumpers.

PAGE 0	11o 07			18o 015	BASE PAGE
	12o 08		U	17o 016	
	13o 09		29		
PAGE 1	14o 010				



NOTE: All center pins are common  
and tied to Bank Select

The Model II can have up to 16 different SWITCHABLE PAGES of 32K each. This is not to say that the Z80 can address more than 64K of memory, just that you can have more memory in the machine ready to be switched in at any time. By now it should be obvious why you can't switch out the lower 32K BASE PAGE. You need a common area of RAM to control the Z80 while it is doing the switching.

Page switching is by 32K worth of RAM, however the RAM cards generally have 64K of RAM. The terminology for each card is a BANK of 64K each. There can be 8 BANKS of RAM in a Model II and they would be numbered 0-7. Each BANK has two 32K PAGES of RAM. Each PAGE is labeled as PAGE 0 or PAGE 1 for that card.

To select a RAM page, the system will output to port FF a value in the least significant nibble of from 0 to F. In binary it would be 0000 to 1111. Data bits 3, 2, and 1 are the BANK and data bit 0 is the PAGE on that BANK. To correlate this to our memory test, multiply the BANK (0-7) by two and add the page jumper (0-1) and this will be where that 32K PAGE of memory will show up in the MAP function of MEMII.

Experimentation with this feature is encouraged. Try to jumper memory boards for each PAGE and put them in a Model II for testing. This is a very good way to test suspect RAM boards. Jumper them for an unused page, i.e., 10 and 11, and install one in a known good Model II for testing. Do not exceed the power limits of the Model II supply. It can handle 5 cards total on the bus, however 6 may cause erratic problems.

As a final note, there is a lack of PAGE 0 in the MAP function of MEMII. This is because there will not normally be any memory jumpered for PAGE 0 in a Model II. The only option that uses PAGE 0 is the Model 16 enhancement. Due to its design, this memory should be checked with the memory test designed for the Model 16, not with MEMII, therefore it was not included in the MAP for possible test.

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**TRS-80®**

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**DT-1 DIAGNOSTIC PROGRAM**

**CHAPTER 3**

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**DATA TERMINAL-1 TEST**

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**GENERAL DESCRIPTION**

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The Data Terminal-1 Test program (DT1DIAG) is designed to aid in the detection of certain visual-attribute problems, which may otherwise become non-perceptive to the user. The program, being sent to the DT-1 via RS-232C, inputs various codes which command the 8051 CPU to execute distinct internally programmed schemes that control many of the visible and non-visible display features of the terminal. Since DT1DIAG is executed by a host computer and all program entries are made on the DT-1, the program is actually testing the receive circuitry of the DT-1, along with output data from the terminal. If the DT-1 transmits properly, the program will execute effectively.

**Features**

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Self-prompting user oriented software  
Selectable execution speed (Baud = 75 thru 19200)  
Fast memory fault detection  
Allows the video memory to be tested  
Allows internal (CPU) program memory to be tested  
Provides a positive affirmation of properly functioning video circuitry  
Fast access to Self-Test (special DT-1 feature)  
Fast access to DT-1 Monitor (special DT-1 trace feature)

**DATA TERMINAL-1 OPERATION**

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First, insure that you have the proper cable interfacing the DT-1 and the Model II. The cable to be used is a Null Modem Adapter (26-1496), WITH a standard RS232 cable. Connect one end to channel A of the Model II and the other end to the inner-most DB25 on the bottom-side of the DT-1.

You should next view the 'SET UP' configuration of the DT-1 exactly as shown in this manual, appendix A. To do this type:

**<CTRL><SHIFT><ENTER>** simutaneously on the DT-1

To change any of the options, simply type in a <1> or a <0> at the proper location after moving the cursor with the arrows on the keypad. Once the 'SET UP' is in order, as on page 2, type <ENTER>.

The DT-1 will ask if you want to store permanently.  
Type <N>

Now type <SHIFT/BREAK> together. A Bell will sound and a blinking-block cursor will appear at home position. The DT-1 is now ready. If trouble should arise while performing this, refer to the 'SET UP' instructions of the DT-1 owners' manual.

**LOADING & EXECUTING DT1DIAG**

---

Now turn on the Model II. Upon the prompt, 'INSERT DISKETTE', insert the TRSDOS / DT1DIAG diskette in Drive Ø. After entering the date and time type the following on the Model II:

**<SETCOM A=(9600,8,N,1)> <ENTER>**

After the prompt is displayed type in;

**<HOST ON> <ENTER>**

The Model II will ask if you want to disable the remote break. Type in <Y> or <N>.

\*\* NOTE \*\* The BREAK key on the DT-1 will temporarily pause the video on the DT-1, it will NOT break a TRSDOS execution, but a <CTRL><C> when typed on the DT-1 will.

You have now completed all keyboard entry required at the Model II.

From this point on ALL entries to the program should be made on the DT-1 to insure proper serial data transmission from the DT-1 to the Host. Be sure the <CAPS LOCK> is down

Type the following on the DT-1:

<BASIC DT1DIAG> <ENTER>

DT-1 Display Format

---

The following should be displayed on the DT-1. If it is NOT then try lowering the BAUD rates of both the Model II & the DT-1. Refer to Model II 'Setcom' instructions and the DT-1 'SET UP' instructions in their respective owner manuals.

DATA TERMINAL 1 TEST

Testing for visual attributes via RS232. The test is self-prompts with menu features. It will print a display, then prompt the Mode in which it printed along with further instructions.

Hit <ENTER> to continue ?

After typing <ENTER> the following menu will be displayed in reverse video. If there is NO reverse video (a white screen) a possible problem may be present with U25, an EEPROM. If the display has double ASCII characters, go back to the 'SET UP' and insure that the F/H (full duplex) is <Ø>.

Menu Display

---

	DT1 TEST
1	NORMAL
2	INVISIBLE
3	BLINK
4	INVISIBLE
5	REVERSE
6	INVISIBLE BLINK
7	REVERSE BLINK
8	REV INV BLINK
9	UNDERLINE
10	INV UNDERLINE
11	BLINK UNDERLINE
12	INV BLINK UNDERLINE
13	REV UNDERLINE
14	INV REV UNDERLINE
15	REV BLINK UNDERLINE
16	INV REV BLINK UNDERLINE
17	1/2 INTENSITY TEST
18	CURSOR ON/OFF TOGGLE TEST
77	RUN COMPLETE TEST
19	TURN ON DT1 **MONITOR** FEATURE
99	EXIT DT1 TEST?

Simply enter the number of the test you wish to perform and DT1DIAG will prompt you with any further instructions.

(example) <3> <ENTER>

\*\* NOTE \*\* The prompt at the bottom of the screen;  
'HIT <ENTER> to check if BLINK video is OK ?'

\*\*\*\*\*  
\*  
\* THE SCREEN SHOULD IMMEDIATELY RETURN \*  
\* to a NORMAL video after <ENTER> \*  
\*  
\*\*\*\*\*

## MODULE DESCRIPTION

- 
- <1> Will fill the screen with the word 'NORMAL' .
  - <2> The cursor will move across the screen printing non-visibly the word 'INVISIBLE'. To insure the video suppression output of the 8276 CRTC (U7), functional, perform this test. Again, hit <ENTER> to check if 'INVISIBLE' was indeed placed into the 2114's (video RAMS).
  - <3> Video should be filled with the word 'BLINK' and also should be blinking. This is caused by the General Purpose output of U7 to U2 latching dot information of U9.
  - <4> Same as menu item 2, but a different code was issued.
  - <5> The word 'REVERSE' repeated in Black-On-White is caused by U10 & U3 logic, originated white by U7 and the black printing caused by BOW from U12.
  - <6> A plain white video screen. ASCII was suppressed by signal, VSP of U7 & its associated logic.
  - <7> A white screen with ASCII blinking on/off.
  - <8> ASCII blanked,white screen.
  - <9> Video is normal with UNDERLINE underlined.
  - <10> Underlining performed with suppressed ASCII.
  - <11> ASCII written to normal video with underlining.
  - <12> Underlining is blinking with no visible ASCII.
  - <13> A white screen with ASCII and underlining.
  - <14> A white screen with NO ASCII but with underlines.
  - <15> A white screen with both ASCII & the underlines blinking.
  - <16> A white raster with blinking underlines but no visible ASCII, until <ENTER> is depressed.
  - <17> This is a test of changing the amplitude of the video signal, therefore allowing a grey/white or a dimmed ASCII display. This is caused by adding a portion of a logic 0 at the time of video dot output. If no apparent difference, check U11; U1.
  - <18> Toggles the cursor OFF or ON.
  - <19> \*\*At this entry, the DT-1 will NOT perform any of its unique attributes, but will rather inform you of EVERY code it received through RS232. from the HOST. Use this test to check internal ROM programming of the 8051 CPU in case some of the previous tests worked and some did not. Check the codes received against the codes in the owners manual.  
(displayed)< G4> should turn Reverse video on.

If you did receive the proper codes and they were not performed correctly then either the 8051 or U25 or associated circuitry should be suspected at fault.

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MEMORY MAP DECODING for DT1

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External to the CPU memory (4Kx8 ROM) is a total of 2K RAM (four 2114-type ICs) used for Video RAM, a EEPROM (X2210 non-volatile) which are all accessable only by the CPU for reads or writes. These memory locations are memory mapped. Address decoding is accomplished by U16 (a 1 of 8 decoder). Decoding is segmented into 1K byte pages. Address lines A10 thru A13 are monitored by U16. NOTE: The line A13 must be high while addressing any memory external to the CPU.

A13	A12	A11	A10	DECODED MEMORY SUBSECTIONS
1	Ø	Ø	Ø	Low Video memory U26 & U28
1	Ø	Ø	1	High Video memory U27 & U29
1	Ø	1	Ø	Non-volatile memory X22101 U25
1	Ø	1	1	Keyboard Read select to U6
1	1	Ø	Ø	Keyboard RS232C input Read U23
1	1	Ø	1	Non-volatile RAM WRITE select (U11)
1	1	1	Ø	NOT USED
1	1	1	1	CRT (8276) controller select

## APPENDIX A

## DATA TERMINAL 1 SET UP

SET UP							
TC1	TCØ	EM1	EMØ	REV	DTR	DSR	DCD
Ø	Ø	Ø	Ø	Ø	1	1	1
STB	O/E	PAR	WDL	BR3	BR2	BR1	BRØ
Ø	Ø	Ø	Ø	1	1	1	1
			ALF	AWP	F/H	CT1	CTØ
			Ø	1	Ø	Ø	Ø

## MNEMONIC

## DESCRIPTION OF TABLE

TC1 TCØ Selects TERMINATING CHARACTER

1	Ø	CARRIAGE RETURN
Ø	1	CARRIAGE RETURN/LINE FEED
1	Ø	END OF TEXT
1	1	END OF TRANSMISSION

EM1 EMØ Selects EMULATION MODE

Ø	Ø	TELEVIDEO 91Ø
Ø	1	LEAR SIEGLER ADM-5
1	Ø	ADDS 25
1	1	HAZELTINE 141Ø

REV	REVERSE VIDEO	( IF SET TO <1> )
DTR	DATA TERMINAL READY	( <1> = CONNECTED )
DSR	DATA SET READY	( <1> = CONNECTED )
DCD	DATA CARRIER DETECT	( <1> = CONNECTED )
STB	STOP BITS	( Ø=1 bit 1=2 bits)
O/E	ODD or EVEN PARITY	( Ø=odd 1=even)
PAR	PARITY SELECT	( <1> = SELECTED )
WDL	WORD LENGTH	( Ø=8 bit 1=7 bit)

BR3 BR2 BR1 BR0      Selects BAUD rate of RS232 I/O

0	0	0	0	9600
0	0	0	1	75
0	0	1	0	110
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	2400
1	0	0	0	4800
1	0	0	1	9600
1	0	1	0	19200 (HIGHER COUNT DEFAULTS TO 9600)

ALF                    AUTOMATIC LINE FEED <1>

AWP                    AUTOMATIC WRAP <1>

F/H                    FULL DUPLEX (0)        HALF DUPLEX (1)

CT1 CT0      Select CURSOR type

0	0	Blinking block
0	1	Blinking underline
1	0	Steady block
1	1	Steady underline

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## APPENDIX B

## DT-1 CABLE INTERFACING

Data Terminal 1 (DB25)                          Host computer (DB25)

PIN #	PIN #
<hr/>	
1 PGND	1 PGND
2 TD	3 RD
3 RD	2 TD
4 RTS	5 CTS
5 CTS	4 RTS
6 DSR	8 CD
6 to 2Ø -- tie DSR & DTR --	6 to 2Ø
7 SGND	7 SGND
8 CD	6 DSR

## NOTE:

The Null Modem Adapter (Radio Shack Catalog number 26-1496) totally eliminates the need to rewire and RS232 cables or adapters. Use it whenever connecting a DT1 directly to HOST computer.

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## APPENDIX C

## PROGRAM LISTING

```

100 ' ****
110 ' * DT1 DIAGNOSTIC *
120 ' * for Model II TRSDOS 2.0a *
130 ' * March 15, 1982 *
140 ' ****
150 CLS:CLEAR(1500):DIMV$(30)
160 ' *** INITIALIZE DT1 CODES ***
170 B$=CHR$(7):PRINT"BELL !!";B$
180 CL$=CHR$(27)+CHR$(42):'CLEAR SCREEN (w/NULLS)
190 RV$=CHR$(27)+CHR$(71)+CHR$(52):'REVERSE VIDEO
200 MT$=CHR$(27)+CHR$(85):'MONITOR ON
210 CI$=CHR$(27)+CHR$(46):'CURSOR INVISIBLE
220 NV$=CHR$(27)+CHR$(71)+CHR$(48):'NORMAL VIDEO
230 HC$=CHR$(30):'HOME CURSOR
240 ST$=CHR$(27)+CHR$(86):'SELF TEST
250 HI$=CHR$(27)+CHR$(29):'1/2 INTENSITY ON
260 IO$=CHR$(27)+CHR$(28):'1/2 INTENSITY OFF
270 BL$=CHR$(27)+CHR$(71)+CHR$(54):'REVERSE BLINK VIDEO
280 F=0:'Set 'F' flag null for 1st run
290 ' OUTPUT PROGRAM DISPLAY PROMPT
300 PRINTCLS:;PRINT,, "DATA TERMINAL 1 TEST":PRINT,"Testing for visual
attributes via RS232. The test is self-prompt-ing with menu features. It ";
310 PRINT"will print a display, then prompt the MODE in which it printed
along with further instructions.":PRINT:INPUT" Hit [ENTER] to continue
";Z$
320 FORI=1 TO 16:READV$:V$(I)=V$:NEXT
330 W=0:IFF=1 THEN J=48:T=J-47:GOTO450
340 PRINTCLS:;PRINTRV$:PRINT,"DT1 TEST":FORM=1 TO 16:PRINT,M,V$(M):NEXTM:T=0
350 PRINT," 17"," 1/2 INTENSITY TEST":PRINT," 18"," CURSOR ON/OFF TOGGLE
TEST"
360 PRINT," 77"," RUN COMPLETE TEST"
370 PRINT," 19"," TURN ON DT1 **MONITOR** FEATURE":PRINT," 99"," EXIT DT1
TEST";
380 INPUTT:J=T+47:F=0:IFT=99THEN710
390 PRINTNV$;CL$;:IFT<=0THEN340
400 IFT=19THENPRINTCLS:PRINTMT$:PRINT"*****TO EXIT THIS MODE HIT
[SHIFT/BREAK]*****":T=0:PRINT"THEN [ENTER] ":GOTO340
410 IFT=77THENF=1:GOTO330
420 IFT=18THENPRINTCI$:;GOTO340
430 IFT=17THEN590
440 IFT>19THEN340
450 PRINTCLS:;PRINTCHR$(27)+CHR$(71)+CHR$(J);
460 M=1848/LEN(V$(T))

```

```

470 FORX=1 TO M:PRINTV$(T);:NEXTX:IF J=48 THEN 490
480 PRINTNV$;:PRINT" Hit [ENTER] to check if ";V$(T); " video ";
490 INPUT" OK ";Y:PRINTHC$;:PRINTNV$;" ";
500 FOR K=1 TO 1000:NEXTK:PRINTCL$;B$;
510 INPUT"Type [R] for a repeat of this mode or {ENTER} to continue ";Y$
520 IFY$="R"THEN PRINTCL$;:Y$="":GOTO450
530 IFF=1 THENJ=J+1:T=T+1
540 INPUT"Type [T] for {SELF-TEST} or [ENTER] to continue ";Y$
550 IFY$="T"THENPRINTST$:FORB=1 TO2000:NEXTB:PRINT"0";:Y$=""
560 IFF=1 THENIFJ<64 THEN450 IFJ<64 THEN450
570 GOTO340
580 PRINTCL$;:CLS:PRINT" BELL";B$:FORB=1 TO 500:NEXTB:PRINTCL$:W=0
590 PRINTCHR$(27);")";"THIS IS 1/2 INTENSITY {ON} ":W=W+1
600 PRINTCHR$(27);"( ";"THIS IS 1/2 INTENSITY {OFF}"
610 PRINTRV$;:PRINTCHR$(8);:IFW=1 THEN590
620 PRINTNV$;W=0:INPUT" Type [R] to repeat 1/2 intensity toggle
";Y$:IFY$="R"THENPRINT;:Y$="":GOTO590
630 GOTO330
640 PRINTCL$;:PRINTRV$;:PRINTBL$;
650 FOR E=1 TO 830:PRINT" ";:NEXTE:PRINT"DT1 TEST
COMPLETE";:FORB=1 TO3000:NEXTB:PRINT:PRINT:PRINT,NV$;
660 PRINT"[Q] to EXIT test & [ENTER] to REPEAT entire DT1 test
";:PRINTBL$;:INPUTY$;
670 IFY$="Q"THEN710 ELSE RESTORE:GOTO330
680 DATA" NORMAL"," INVISIBLE"," BLINK"," INVISIBLE"," REVERSE",
" INVISIBLE BLINK"," REVERSE BLINK"," REV INV BLINK"," UNDERLINE"
690 DATA" INV UNDERLINE"," BLINK UNDERLINE"," INV BLINK UNDERLINE"," REV
UNDERLINE"," INV REV UNDERLINE"," REV BLINK UNDERLINE"
700 DATA" INV REV BLINK UNDERLINE"
710 PRINTCL$;CI$:PRINTRV$:FORX=1 TO12:PRINTCHR$(10);:NEXT
720 FORY=1 TO32:PRINTCHR$(8);:NEXTY
730 BL$=CHR$(27)+CHR$(71)+CHR$(58)
740
FORP=1 TO18:READK$:PRINTBL$;:PRINTK$;:PRINTCHR$(8);CHR$(8);CHR$(8);:NEXTP
750 PRINTCI$;CHR$(10);";CHR$(11);RV$;
760 FORT=1 TO1800:NEXTT
770 DATAE,T,E,L,P,M,O,C, ,T,S,E,T, ,1,-,T,D
780 PRINTCL$:END

```

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**FDCALG**

**MODEL II/16  
FLOPPY DISK CONTROLLER BOARD ALIGNMENT PROGRAM**

**CHAPTER 4**

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FDCALG  
MODEL II/16  
FLOPPY DISK CONTROLLER BOARD ALIGNMENT PROGRAM

Materials needed:

35 MHz or greater oscilloscope  
(2) x10 oscilloscope probes  
Digital Voltmeter (DVM) and probes  
Small screwdriver  
MOD II extender board  
Extender cable  
Blank 8" diskette  
FDCALG alignment program

Before running FDCALG:

There are two different FDC boards used in the Model II, upgraded Model II, and Model 16 computers. The early style is characterized by having only one connector for the FDC-to-drive cable. The late style board has two connectors -- one for the internal drive(s) and one for the external drives. The alignment procedures are different for each board.

Remove the FDC board and the drive cable. Plug the FDC board into the extender board and plug the extender board / FDC board assembly into the motherboard. Take the extender cable and plug it into the FDC board and the internal disk drive. If the FDC board is a early version (only 1 drive connector on the FDC board) plug a terminator in the correct socket on the cable.

**ALIGNMENT PROCEDURE**

( Early Style Boards )

- (1) Connect channel A to TP 24, Channel B to TP 20. Timebase set to 1 us/div. Sync negative trigger on channel A. If the program is not in the FM mode set it to FM by pressing <ENTER>. Adjust the trigger level for a steady display.
- (2) Adjust R36 so that channel A displays a 50% duty cycle (1 division per 1/2 cycle) as shown in FIGURE 1 attached.
- (3) Adjust R32 so that channel B looks exactly like channel A (both signals should be in phase).
- (4) Invert channel B and add it to channel A. Adjust R32 & R36 to minimize the glitches on the display.
- (5) Select the MFM mode by pressing <ENTER> and set the time base to .5 us/div.
- (6) Adjust R37 for a display as close to FIGURE 2 as possible, again minimizing the glitches.
- (7) Press <F1> to continue on to the next step.
- (8) Connect channel A to pin 10 of U7, channel B to TP 10. Timebase set to 0.5 us/div. Sync positive trigger on channel A and adjust the trigger level for a steady display.
- (9) Adjust R5 so that the pulse on channel A ends at the same time as the first pulse on channel B (See FIGURE 4).

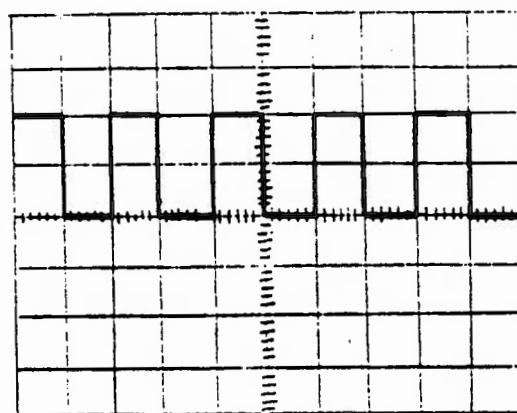
**ALIGNMENT PROCEDURE**

(Late Style Boards)

- (1) Adjust R2 to obtain 1.4 vdc at TP 25 when the FDC chip is inactive (when prompted by the menu).
- (2) Adjust R1 for a 4 MHZ square wave at pin 16 of U28 or pin 7 of U24.
- (3) Once these 2 steps have been completed press enter to have the FDC execute continuous writes on the diskette.
- (4) Set the scope to 200 ns/div. negative trigger on channel A. Adjust R3 for 250 ns pulses on TP 27 (see FIGURE 3).

FIGURE 1

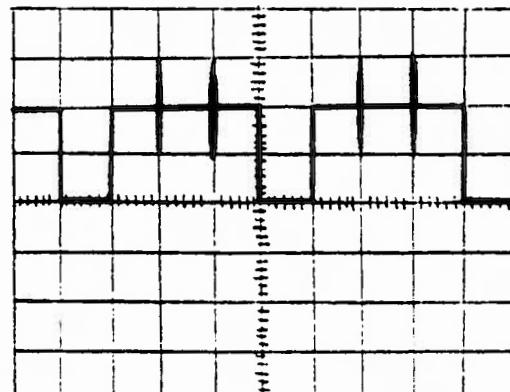
FM



Timebase 1  $\mu$ sec/div  
Channel A 2 V/div  
Adjust for 50% duty cycle

FIGURE 2

MFM



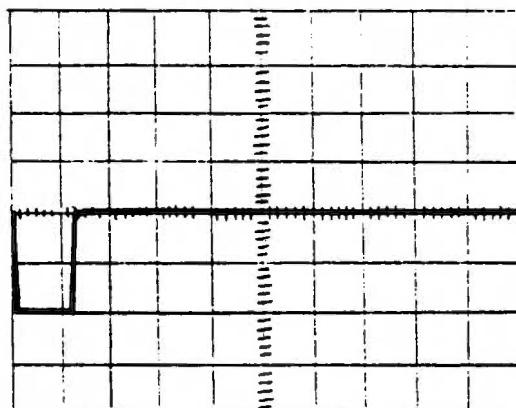
Timebase 1  $\mu$ sec/div  
Vertical 2 v/div  
Invert B and add to A  
Minimize the glitches.

---

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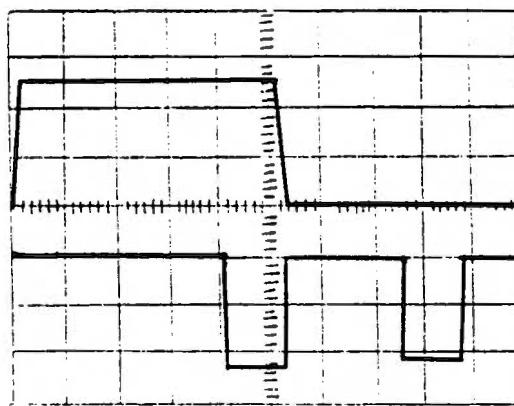
---

FIGURE 3  
Precomp adjustment



Timebase .2 μsec/div  
Channel A 2 V/div  
Adjust for 250 ns pulses

FIGURE 4  
Late Pulse Extension



Channel A

Channel B

Timebase 0.5 μsec/div  
Channel A 2 V/div  
Channel B 2 V/div

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**HIRES**

**VIDEO/GRAFICS BOARD DIAGNOSTIC AND SCREEN ALIGNMENT PROGRAM**

**CHAPTER 5**

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# HIRES

## VIDEO/GRAFICS BOARD DIAGNOSTIC AND SCREEN ALIGNMENT PROGRAM

## EQUIPMENT REQUIRED

Model II, Model 12, Model 16, or Model 16B Computer

## Video alignment tools

## **HIRES diagnostic program.**

Optional 26-4104 High Resolution Graphics board

## INTRODUCTION

Before turning on the computer install the board to be tested or aligned in the computer. Boot the diskette with the HIRES program and execute HIRES. After a few moments the menu should appear.

HIRES responds to the <BREAK> and <HOLD> keys at all times. <HOLD> 'freezes' the program and hold the display where it's at. Pressing the break key again will cause the program to continue execution. <BREAK> returns you to the previous menu, up to the very first menu that prompts for the <V>ideo or <G>raphics board test.

When the title first appears on the screen a menu will appear at the bottom. The tests that are available are <G>raphics section, <V>ideo section, <T>imer, or <Q>uit. Select <V> for the video board test or <G> for the graphics board test. <T>imer is used to select the time delay during the auto test. It can be set for 1 to 9 seconds and defaults to 2 seconds. If the screen needs to be aligned, and the High Resolution Graphics board is installed, select the <G>raphics board test. There is a very good test pattern in the graphics test. If <V> or <G> is selected the computer will ask if the information switch is to be turned on. With the switch on a small amount of additional information is about the test will be displayed before each test. It is best to use this option until the operator is familiar with the test and then leave it off.

```
*****
*                               IMPORTANT NOTICE
*
* All of these tests require you, the operator, to check the dis-
* play as part of the test. The only way to check the character
* generator is for the operator to check what is on the screen
* and verify that it is correct. The user should become familiar
* with the program by running the test on a known good computer.
*
*****
```

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**VIDEO BOARD TEST**  
-----

Video board test menu:

- <C> Clear Screen
- <F> Full Screen
- <W> Wait State on/off
- <A> Alpha/numeric Characters
- <G> Graphic Characters
- <V> Video Ram Test

The available test modes are:

<A> Auto Mode

Executes tests 1 through 6 in order and returns to the Menu.

<S> Single Mode

Executes the test one time and returns to the Menu.

<L> Loop Mode

Executes the test you chose and repeats that test until you press the <BREAK> key, which will return you to the Menu.

<Q> Quit

Returns to TRSDOS

**DESCRIPTION OF AVAILABLE TESTS**

<C> Clear screen test

This test will fill the display with blanks. The user should verify that there is nothing on the screen during this time.

<F> Full screen test

This test is used to check that all positions on the screen can be whited out and that all dots on the display are turned on.

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**<W> Wait state on/off test**

This section tests the video Real Time Clock timing circuitry. The first part of the test will fill the screen unsynchronized with the video display; this will cause 'hash' lines to appear on the screen. The second part of the test will fill the screen during vertical retrace. This is slower but there should be no small streaks or 'hash' on the screen. If you have streaks during the second part of the test there has been a failure in the RTC circuit.

The wait state test for the video waits for an interrupt from the Real Time Clock (RTC) which occurs at the start of vertical retrace. Once the interrupt occurs 8 characters are sent to the screen. This is done during retrace so no 'hashing' occurs on the screen. If no interrupt occurs then the program will lockup at this point. If the interrupt occurs at the wrong time then the writes will be out of sync and a small area of 'hash' will occur. If a constant interrupt occurs then the screen will be filled with 'hash' and it will be whited out much quicker than normal in this section.

**<A> Alpha/numeric characters test**

The character generator is checked during this test. This test produces the complete ASCII character set. The user should verify that all the characters listed in the Model II Owners Manual are displayed. This is useful if the computer is displaying incorrect characters.

**<G> Graphic characters test**

This test is similar to the alpha/numeric test except that all of the REGULAR Model II graphics characters are displayed on the screen and should be checked to see that they are all correct.

**<V> Video RAM test**

This completely tests the video memory with errors displayed on the bottom of the screen. After 12 errors the test stops and asks if you wish to quit or continue. This is the only video board test that the user does not have to visually verify. Just check to see which if any IC's are faulty.

**GRAPHICS BOARD TEST**  
-----

Graphics board test menu

- <C> Clear Screen
- <F> Full Screen
- <W> Wait State on/off
- <A> Alpha/numeric Characters with graphics background
- <G> Graphic characters with graphics background
- <C> Checker board
- <R> Sit/Run option test
- <E> Screen alignment test pattern
- <M> Graphics memory test

Available test modes are:

<A> Auto mode

Executes tests 1 through 9 in order and returns to the menu.

<S> Single Mode

Executes the test one time and returns to the Menu.

<L> Loop Mode

Executes the test you chose and repeats that test until you press the <BREAK> key, which will return you to the Menu.

<Q> Quit

Returns to TRSDOS

**DESCRIPTION OF AVAILABLE TESTS**

<C> Clear screen.

This test will black out the entire screen. Check for any pixels that may be 'stuck' on.

<F> Full screen.

This test will fully white out the screen using the graphics board. Check for any pixels or groups of pixels that may be 'stuck' off.

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**<W> Wait state on/off.**

During this test the video wait circuitry will be tested. The test will first fill the screen with the wait state turned off. This will cause streaks or 'hash' to appear on the screen. The test will then fill the screen with the wait states on. This is slower but there should be no streaks or 'hashing' on the screen.

The wait state test for the graphics board actually uses the wait line and depending on the failure there could be either 'hashing' on both screen fills or neither screen fills. If there is 'hashing' during the second part of the test, then there is a failure in the wait circuit. Trouble shooting here should start at pin 48 of J0 on the graphics board and work back into the graphics circuit.

**<A> Alpha/numeric characters with a graphics background.**

The Alpha/numeric characters with a graphics background module tests the ability of the video and graphics boards to display characters at the same time.

The first display shows alpha/numeric characters on the screen with the graphics board enabled but with all the pixels turned off. Next, the graphics board reverses the lower half of the display. This causes the characters on the bottom half of the screen to appear negative -- black on white instead of white on black. On the final screen the video board fills the screen with reverse characters that should look black on a white background. However, the graphics board is still reversing the bottom half of the screen causing it to appear normal.

If these patterns do not appear and all other tests are normal there is a interfacing problem between the graphics board and the video board, probably in the EXCLUSIVE-OR gates (U24 and U20) on the graphics board. The same holds true for the graphics characters test with graphics background.

**<G> Graphic characters with a graphics background.**

This test is the same as the previous test except that a graphics display is used instead of an alpha/numeric display.

**<C> Checker board test.**

The checker board test makes it easy to test the graphics memory visually. The checker board test turns on every other pixel on the screen. This is done because if only one pixel is missing on the screen it would be easy to overlook, however with this pattern one pixel missing causes a 'hole' to appear on the display. The reason for this is that the pixels surrounding the missing pixel are also off drawing more attention to the missing pixel. The pattern is then reversed so that the pixels that were turned off before are now turned on and may be verified.

**<R> Sit/Run test.**

In this test the Sit/Run registers of the graphics board are tested. The first half draws 8 lines to test all possible combinations of the registers. It then tests the memory to make sure that the lines were drawn correctly and displays any errors. The second half does the same thing but draws a cube.

The SIT/RUN test helps to check out the option latch (U27), and the up/down counters (U29, U30, U34, and U35) on the graphics board. A failure here could mean a faulty register in the option latch, or one of the counters may be counting in only one direction or not at all. The first half of this test will display errors on the screen because after writing using the SIT/RUN mode, it goes back and checks the RAM without using the RAM to make sure the data went to the right locations. In the second part (the cube) the program makes no checks and it is up to the operator to verify that the board is working properly.

**<S> Screen alignment test pattern**

This module gives the operator a test pattern to align the video display. The graphics board requires that the display have a much better alignment than previously required. The <HOLD> key will 'freeze' the display to aid in the alignment.

The screen should measure 8 inches by 6 inches and have 5 ROUND circles, one in the center and one in each of the corners. The markers on the edges should be at one inch intervals.

**<M> Graphic memory test**

The memory test checks all 19.2k bytes of RAM used by the graphics board. The method is the same as for the video RAM test except that during this test the status is printed on the display.

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**ARCTST**

**ARCNET™ SYSTEM DIAGNOSTIC TESTS**

**CHAPTER 6**

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**ARCTST**

ARCTST is a diagnostic program used to test the functions and interconnections of an ARCNET installation. The test is fast and simple, facilitating its use at each and every station as the station is installed.

ARCTST requires a minimum system of two computers. While most ARCNET systems will consist of more than two computers, the test procedure should be started as soon as two computers are on line. By testing each computer as it is brought on line, it will be much easier to isolate a troublesome unit, as each previously installed unit is tested and known to be good.

**OBJECTIVE**

The objective of ARCTST is quite simple -- to establish a working connection between two units.

ARCTST is a loopback type of test, similiar in many ways to the tests used to check RS232, modems, and telecommunications lines. The TEST unit generates a block of data and transmits a PACKET through the ARCNET system. The MASTER unit simply returns, or echoes, this PACKET without modification. The TEST unit then verifies that the PACKET it receives is the same as the PACKET it sent. If the verification produces no errors then the system consisting of the TEST unit, the MASTER unit, and any cables and hubs between the two units is functional.

**INSTALLING ARCTST**

For maximum efficiency, it will be necessary to have TWO copies of the ARCTST test diskette, one for the MASTER unit and one for the TEST unit. As well, if the units are more than a few feet apart, it is recommended that two technicians, or one technician and a knowledgeable helper, be present and in communication with each other.

Boot both units from their respective floppies, and at TRSDOS READY, type:

**ARCTST <enter>**

Note that ARCTST is identical for both machines. The MASTER or TEST functions will be selected when the program is running.

After the program is loaded, the screen should display the following:

POR-xxH-TYPE G TO CONTINUE

This message will appear ONLY the FIRST time ARCTST is run after the unit is booted or reset. This is indicated by the POR (Power On Reset). This number should match the switch settings of Z26 on the ARCNET board.

**NOTE: This number is guaranteed correct ONLY after a boot sequence.  
WRITE IT DOWN!!** Type <G> to continue to the test menu.

After typing <G> the following screen will appear:

ARC Net diagnostics version V.r

SID for this board is xxH  
WARNING! The SID may be incorrect

DID (HEX-2CHAR)=..

LDERR      ATTMP      ACKED      NOFRB      NODAT      BADAT      OVRWR      RECON

In the second line, SID (Source IDentification), the 'xx' will be replaced with the HEXADECIMAL ID number of the board installed in this unit. This number should match the switch settings of Z26 on the ARCNET board, and the number which appeared with the POR message. If the number is incorrect change it using the <S> option (page 4).

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The third line, DID (Destination IDentification), must be filled in with the HEXADECIMAL ID of the other unit to be used during the test. For example, if unit  $\emptyset 2H$  is to be used as the TEST unit, and unit  $\emptyset 6H$  is to be used as the MASTER unit, the the TEST unit should show the SID as  $\emptyset 2H$  and the DID should be entered as  $\emptyset 6$  (the 'H' is not necessary). The MASTER unit will have these entries reversed.

At this point, one of the computers must be designated as a MASTER unit, and the other designated as a TEST unit. The usual procedure would be to use the FILE PROCESSOR (FP) as the MASTER, and the newly installed APPLICATION PROCESSOR as the TEST.

As well, the individual ARCNET ID number of each unit must be known. This is, of course, the SID number given when ARCTST is loaded.

At the unit designated MASTER, enter the Destination ID (DID), or the ARCNET ID of the unit designated TEST. At the TEST unit, enter the DID of the MASTER unit. When the DID is fully entered the counters will be zeroed and the MENU will appear on the bottom line.

In the case of a two unit system, ARCTST should be run twice to let each unit act as the TEST and as the MASTER. In small systems, every unit should be tested with every other unit, with each unit being used as the TEST and as the MASTER.

In large systems, testing each individual interconnection will be very time consuming. In this case, install and THOROUGHLY check each unit to be used as a FILE PROCESSOR (FP). Then, install each APPLICATION PROCESSOR (AP) and check them to their associated FP(s) using the FP as the MASTER unit.

If all FPs can communicate between each other, and each AP can communicate with its FPs, then it is unlikely that an error exists.

#### RUNNING ARCTST

Once both the MASTER and TEST unit have been booted, ARCTST loaded, and the DIDs of both units properly set the test can be run.

At the MASTER unit, type <M> (for MASTER). At this point the MASTER unit may produce various errors since the TEST unit is not yet functioning. These errors may be disregarded.

At the TEST unit, type <T> (for test), then type <C> (for continue). Do not hit <ENTER>. With the TEST unit now functional, the ATTMP and ACKED counters should begin to count. There should be no counts accumulating in any of the other counters. If the other counters begin to register, see the INTERPRETING ERRORS section of this document.

#### CONTROLS

ARCTST is extremely simple to operate. It is only necessary to select the function, MASTER or TEST, of each unit. The three main selections are displayed on the screen.

<M> MASTER -- Puts this unit into the MASTER mode. The MASTER unit simply echoes the data packet back to the TEST unit without modification.

<T> TEST -- Puts this unit into the TEST mode. The TEST unit is actually the one being tested. It develops a data packet, transmits it to the MASTER unit specified during DID selection, receives the re-transmitted packet, and verifies that all data remains intact.

<Q> QUIT -- Return to TRSDOS.

There are also five secondary functions which are not displayed on the screen at any time:

<R> -- Functional only from the main menu (no test currently active). The cursor goes back to the DID selection area and you are allowed to change the DID. The DID can be changed without rebooting ARCTST.

<S> -- Functional only from the main menu (no test currently active). New instructions are added just above the main menu, and you can change the SID if you suspect it of being wrong.

<X> -- Functional only in the TEST or MASTER modes. The current test is terminated and the program returns to the TEST/MASTER/DOS menu.

<E> -- Functional only in the TEST mode. While in the TEST mode, pressing <E> will perform a SINGLE transmit/receive/verify test.

<C> -- Functional only in the TEST mode. While in the TEST mode, pressing <C> will perform CONTINUOUS transmit/receive/verify tests until <X> is pressed. Hitting ANY (except <X>) key will pause the test until <C> is hit again.

## COUNTERS

ARCTST keeps track of eight counters on screen. Below is an explanation of the uses of these counters.

**LDERR** -- LOAD ERROR. This indicates that there has been a read or write error between the computer and the ARCNET board. This counter has no meaning on the unit designated as MASTER.

**ATTMP** -- ATTEMPT. The TEST unit has attempted to send a packet. This is a normal condition.

**ACKED** -- ACKNOWLEDGED. Counts the number of properly received packets. This generally indicates proper operation.

**NOFRB** -- NO FREE BUFFER. Before the a unit transmits its packet, it asks the receiving unit if it has a free buffer to receive the packet. If negative acknowledges (NAK) are received for a time longer than approximately one second, the NOFRB is incremented.

**NODAT** -- NO DATA. This counter is incremented if a unit thinks it is to receive data, but no data comes in within approximately one second.

**BADAT** -- BAD DATA. The packet received from the MASTER unit was not the same as the packet transmitted from the TEST unit. This counter has no meaning on the unit designated as MASTER.

**OVRWR** -- OVER WRITE. Bad data was found outside of the ARCNET memory area reserved for the receive buffer. This counter has no meaning on the unit designated as MASTER.

**RECON** -- RECONFIGURATION. An attempt has been made to reconfigure the system, either by the TEST or MASTER units, or by another unit in the system.

## INTERPRETING ERRORS

Using the above counters it is possible to determine many common faults in the ARCNET system. The following are possible interpretations of various fault conditions. THIS LIST IS BY NO MEANS EXHAUSTIVE.

**Both ATTEMP and ACKED count increases.** No other counters are active.

This is proper operation of the system. The TEST unit, MASTER unit, and all cables and hubs in between are functioning properly.

**LDERR count increases.** The computer which registers the errors and its ARCNET board are not communicating properly. Possible ARCNET board failure, but CPU or memory board failure also possible.

**BADAT count increases.** Possible ARCNET board failure in either TEST or MASTER unit. Substitute known good ARCNET board into MASTER unit and try again. If both units can properly pass tests with other units in a multi-unit system, suspect cable and/or hubs between these two units.

**Both BADAT and LDERR count increases.** Possible CPU or memory fault in the computer registering the errors.

**Both RECON and NOFRB count increases.** Possible faulty cable, bad connection (broken or missing), or otherwise open line.

**RECON counts. Other counters may or may not function.** Other unit(s) have attempted to come "on line". Other units may be on or off line, but all units should be inactive during the testing procedure.

**ATTEMP counts in increments of 16.** No ARCNET board at location specified by DID. Unit may be non-functional, disconnected, or cabling may be faulty or mislabeled.

**ATTEMP is greater than ACKED by a factor of 16.** Unit specified by DID is not properly receiving the transmitted packets.

**ATTEMP, ACKED, and NODATA count increases.** BADAT may or may not count. Unit specified in DID is on line, but not running the proper program.

**NODAT only count increases.** Both units in MASTER mode. Make sure one unit is in TEST mode.

**NOFRB only count increases.** Both units in TEST mode. Make sure one unit is in MASTER mode.

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**8 MEGABYTE HARD DRIVE DIAGNOSTICS**

**CHAPTER 7**

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INTRODUCTION

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The following programs are provided to assist in alignment and troubleshooting of Model II/16 Eight Megabyte Hard Disk System:

HDVER

HDDIAG

HDIFAC

HDMENU

WARNING

```
*****
*** WARNING! WARNING! WARNING! WARNING! WARNING! ***
*****
*** THESE PROGRAMS CAN DESTROY DATA!!! BE CAREFULL ***
*** AND BE CERTAIN YOU UNDERSTAND HOW TO USE THEM ***
*** BEFORE ATTEMPTING TO USE THEM FOR DRIVE ***
*** VERIFICATION OR TROUBLESHOOTING!
***
```

---

## GENERAL DIAGNOSTICS PRECAUTIONS:

- 1) Do not attempt to transfer the diagnostics to TRSDOS 4.2 floppy or TRSDOS-HD! Boot the diagnostics on TRSDOS 2.0a by hitting the reset and holding down the <BREAK> and <REPEAT> keys simultaneously.
- 2) There will be some bad blocks on the Hard Drives. While the Operating System does not use and ignores them, they will be detected by the diagnostics! DO NOT ASSUME THE PLATTER IS DEFECTIVE BECAUSE THE DIAGNOSTICS DETECTS A BAD BLOCK! Check the chart supplied with the drive to verify which blocks are bad on the drive you are testing.

QUICK REFERENCE SECTION

---

**"WARNING"**

---

**Description**

Contains precaution messages for the proper care and handling of the Hard Disk unit. BEFORE ATTEMPTING AN INSTALLATION OR SERVICING, BE CERTAIN YOU UNDERSTAND THESE PRECAUTIONS.

**"HDVER"**

---

**Execution:**

1. In TRSDOS type <HDVER> and <ENTER>.
2. Answer "ENTER DRIVE SELECT PORT. <ENTER> - "C" .." prompt by typing <ENTER> (This maps the drive at port  $\emptyset C\emptyset$  hex to  $\emptyset CF$  hex).
3. Answer "ENTER DRIVE # TO TEST (4,5,6,7) ." with <4> and <ENTER>.

**OPTIONS:**

<W> Track 1 is reserved for use as a "diagnostics" track. No system information or data is maintained on this track. The <W> command will write, read and verify data on this track. This option may be safely used to insure proper write operation within limits.

<A> The "A" option will sequentially write, read and verify data ON ALL TRACKS!

\*\*\*\*\*  
\*\*\* WARNING! WARNING! WARNING! WARNING! \*\*\*  
\*\*\*\*\*  
\*\*\*  
\*\*\* THIS OPTION WILL DESTROY ANY DATA ON THE TRACKS \*\*\*  
\*\*\* IT WRITES. IT SHOULD ONLY BE USED BEFORE DATA \*\*\*  
\*\*\* IS ON THE DRIVE, OR FOR TROUBLESHOOTING WHEN \*\*\*  
\*\*\* THERE IS NO HOPE FOR RECOVERING DATA FROM THE \*\*\*  
\*\*\* THE DRIVE! AN ATTEMPT TO "SAVE" THE DATA ON \*\*\*  
\*\*\* THE HARD DRIVE SHOULD BE MADE BEFORE USING THIS \*\*\*  
\*\*\* OPTION. \*\*\*  
\*\*\*\*\*

---

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- <R> Reads all tracks sequentially and checks the status register for any errors. Errors will occur on bad blocks! Check the chart on the bottom of the drive, to ascertain which tracks have bad blocks. The blocks identified by the diagnostic should agree with the chart.
- <S> Quick version of the <R> command. Checks tracks 0000, 0124 (before precomp applied) and 0128, 0255 (precomp applied).
- <X> Generates a random track number, seeks the track, reads and checks status register for errors.
- <D> Selects drive to test.
- <Q> Exit to TRSDOS.

"HDIFAC"

---

Execution:

1. In TRSDOS type <HDIFAC> and <ENTER>.
2. Answer "ENTER DRIVE SELECT PORT. <ENTER> - "C" .." by typing <ENTER>.

OPTIONS:

- <A> Automatically runs tests 1-5.
- <L> Will continuously loop through any one of tests 1-5.
- <S> Will execute any test (1-5) once.
- <E> Exits to TRSDOS.
- <1> Will exercise a selected port. Valuable for port decoding troubleshooting.
- <2> Reads and displays the values of the interface DIP switches as seen by the system.
- <3> Writes and reads a walking binary pattern to the control register, and checks for errors.
- <4> Tests the Z80-CTC timer chip for proper timing operation, and verifies proper interrupts are being generated by the CTC.
- <5> RAM test for the interface board RAM.

---

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**"HDDIAG"**  
-----

Description: This program tests and manipulates various Hard Disk controller circuitry. One option (<A>) provides a method for adjusting the controller VCO, static error Amplifier, "DRUN", and dynamic error amplifier.

## Execution:

1. Type <HDDIAG> and <ENTER>
2. Type <ENTER> to map drive at Port 0Cx hex.
3. Select drive number to test.

## OPTIONS:

- <T> Writes and verifies data to the controller task register.
- <Ø> Restores the drive to track Ø (cylinder Ø, head Ø).
- <S> Allows user to seek a selected track with optional seek verification.
- <C> Allows user to step heads between two selected tracks.
- <L> Steps drive from outer-most to inner-most tracks in decreasing order.  
Exercises operation of step slew rate changes.
- <M> RAM test for static 2114 150ns RAMS on controller.
- <I> Seeks current track to generate an interrupt. Verifies that interrupt is received.
- <D> Selects drive number to test.
- <A> Self-prompting alignment procedure.
- <G> Reads and displays current controller status.
- <X> Generates random track number, reads track, and checks status register for errors.
- <R> Reads current track, checks status register for errors.

<W> Writes to currently selected track, checks for errors.

```
*****
*** WARNING! WARNING! WARNING! WARNING! WARNING!
*****
***      THIS OPTION WILL DESTROY CUSTOMER DATA      ***
***      IF A TRACK OTHER THAN THE DIAGNOSTIC TRACK    ***
***              (TRACK 1) IS WRITTEN.                  ***
*****
*****
```

<F> Formats Diagnostic Track (track 1) and checks for errors.

This test does not interfere with customer data providing head position and head select are functioning properly.

<E> Enable/disable interrupts. Option allows selection of interrupt status to facilitate fault isolation.

<Q> Exit to TRSDOS.

---

#### TECHNICAL SECTION

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#### History Table and Error Description

---

##### DRIVE NUMBER:

Specifies which drive the logged error occurred on.

##### CYLINDER NUMBER, HEAD NUMBER:

The cylinder number is analogous to a floppy disk drives "Track". There are 256 cylinders on the drive. Each cylinder consists of four media surfaces which may be accessed by one of four heads. The 256 cylinders times the 4 heads/cylinder yields 1024 tracks per drive. By observing logged errors, it is possible to determine if a fault may be caused by a defective head/head circuitry (all errors occur on a particular head), or if a platter has been damaged (all errors occur on a particular cylinder only).

**ID NOT FOUND:**

During initialization, an ID Field is written for each track and sector. This error occurs when the disk controller cannot lock onto the ID Field data, and as a result, cannot find the target sector to read or write data. Infrequent occurrences of this error may indicate that the "DRUN", "ERROR AMPS", or "VCO" require adjustment (using HDDIAG program).

Remember that some "media flaws" are inherent to the hard disk media and these will be detected by the diagnostic. Compare the logged faults with the "Media Error Map" which is on the bottom of the drive assembly to determine if there is a marked increase in the number of flaws. If an increase is noted, observe the conditions under which the faults are logged. A certain head or cylinder may be at fault.

**DATA CRC:**

During a read operation, some of the bits in the 512 bytes of data on the current sector were in error. Suspect the CRC Generator/checker chip (U14 WD1100-4) if this is a frequent error.

**ID CRC:**

During an attempted read or write operation, some of the bits in the ID field (containing sector location information) were incorrect. This may be due to flaws in the media or an operational failure. Consistant ID field CRC errors may be caused by the CRC Generator/checker chip (U14 WD1100-4) or misalignment of "VCO", "DRUN", or "Error Amp".

**BAD BLOCK:**

This error only occurs if the media was last formatted by the Shugart factory and indicates that a sector is unusable. TRSDOS does not mark faulty sectors with "Bad Block" marks. TRSDOS will log "Bad Blocks" as specific errors (ID NOT FOUND, ID CRC, etc.), and will not use those sectors of the Hard Disk. If the media has been initialized by TRSDOS, then HDVER will also log "Bad Blocks" by specific type errors.

**DAM NOT FOUND:**

Indicates that the data address mark (a unique byte that identifies the beginning of a data field) could not be found. This may be due to media, or point to a damaged AM Detector chip (U22 WD1100-03), or related circuitry.

## ABORTED COMMAND:

This is a major fault, and the disk controller will not accept a command if this occurs. Run "HDIFAC" or "HDDIAG" to obtain a better indication of the cause of this fault.

**"HDIFAC"**  
-----

Description: The Hard Disk Interface diagnostic consists of tests aimed at isolating faults on the Model II/16 Hard Disk interface circuit board. This provides a means of determining if a drive failure is due to the interface board or the controller assembly.

## Execution:

1. In TRSDOS type <HDIFAC> and <ENTER>.
2. Answer "ENTER DRIVE SELECT PORT. <ENTER> - "C" .." by typing <ENTER>.

## OPTIONS:

<A> Automatically runs tests 1-5.

<L> Will continuously loop through any one of tests 1-5.

<S> Will execute any test (1-5) once.

<E> Exits to TRSDOS.

<1> PORT TEST

Provides a way to easily exercise all of the I/O ports of the Hard Disk System. Options allow the port to be configured as either an input or output, and the address to be specified.

A new port may be defined by pressing the space-bar. <BREAK> returns the program to the menu.

**<2> "DID" REGS TEST**

This test determines if the interface can decode and read the switch configurations of switches "S1" and "S2". The purpose of the switches is to allow the operating system software to determine the configuration of the hardware. The user may change the configuration, should the need arise, without requiring modifications to the software.

With the "DID" test running in the <L>oop mode, the configuration of the switches will be displayed to the screen. If the switch setting is changed, but the value displayed does not change, then the port decoder is malfunctioning or the data bus is at fault.

**<3> CONTROL REGISTER TEST**

The Hard Disk control register consists of an eight bit latch (U16), and an eight bit tri-state buffer (U10). Various hardware functions are enabled/disabled by the data latched into this "control register".

The Control Register Test exercises the register by writing and reading a rotating "Logic 1" pattern across the data bus to see if each data line can be set high independently of the other lines. This test exercises the associated data lines as well as the register input and output port decoding. Note: After a system reset, all outputs of U16 should be "Logic 0" (reset should assert the clear input, pin 1).

**<4> CTC & INTERRUPT TEST**

The CTC and Interrupt test verifies that the system can write and read the Counter Timer Chip registers. If the registers function properly, then "CTC REGS ARE GOOD" is displayed. The test further verifies that all four CTC channels properly generate interrupts in the timer mode. Finally, the CTC is tested in the counter interrupt mode.

**<5> DYNAMIC RAM TEST**

The RAM test writes a binary incrementing pattern, followed by a "checker board" pattern. The "Pass Counter" indicates activity while the test is in progress. When an error is detected, the program will show the first page of failures and stop. Press any key to continue, <HOLD> to freeze the display.

**HDDIAG**  
-----

The Hard Disk Diagnostic Program consists of tests which exercise the Hard Disk controller and Drive assemblies. The flexibility of the tests provide a method for categorically isolating faults in the controller or drive assembly.

Features have been implemented to safeguard the customer's data. Track 1 on each drive is designated as a "Diagnostic Track". Read and write loop testing may be done on this track without concern for the customer's data. In the event that a fault causes the destruction of the diagnostic track ID field, the <F> option allows reconstructing the diagnostic track.

Even with these features, ALWAYS BE CERTAIN THAT THE CUSTOMER HAS BACKED UP THE DATA FILES IF IT IS AT ALL POSSIBLE before servicing the drive!

**Options:****<T> TASK REGISTER TEST**

The Task Register Test provides several modes of operation. The Single test mode allows the test to run through once, while the Loop Test Mode allows continuous exercising of the test for signal tracing with a scope.

The Task Registers are located in the "8X300" CPU. Data is written to, read, and checked to verify proper register operation.

The registers are addressed by CA-CE hex. The logic pattern which is written and read is a rotating "logic 1" in a field of "zeros", followed by a rotating "logic 0" in a field of "ones". This provides a means of testing the address lines "A0" thru "A2" ("A3" is always high). The input buffers for the read & write control functions, the data lines & data access lines internal to the controller board, and the chip enable function are all required to operate in order for this test to pass. The test will display "TASK REGISTER TEST PASSES" if all the required signal paths are good. If there is a mismatch of data written & read, then the difference is shown as the address and data byte, one error at a time. Pressing any key will advance the test.

If the task register or support circuitry is defective, then no commands required to operate the drive can be executed.

**<M> Static RAM Test**

The static RAMs (U-67, U-68) provide the I/O buffer for data transfers to/from the Hard Disk. The Hard Disk is formatted with 512 byte physical sectors, so 512 bytes of the static RAM are used to buffer the data between the host and the Hard Disk.

The Hard Disk host computer is not capable of keeping up with the high data rate required for Hard Disk read/write operations. For this reason the host computer interfaces through the static Ram buffer with the data to transfer. In addition, the "8X300" uses approximately 20 bytes of the RAM as a "scratchpad".

The Static RAM test exercises the buffer area of the RAM, but not the scratch space - it is not available to the host computer. Additionally, the RAMs are in parallel, and therefore affect each other. Due to these limitations in testing the RAMs, the test may not always detect a fault. If Static RAM problems are suspected, it may be wise to substitute known good RAMs (Remember - 150 nanosecond RAMs are required!).

**<I> Interrupt Test**

The interrupt test checks the ability of the controller to generate an interrupt upon completion of a command. The controller can be operated in an interrupt or poll status register mode. This mode may be controlled by toggling the <E> Enable/Disable Interrupts feature.

The current interrupt status is displayed on the right side of the status line. Note that the interrupt test enables the interrupt mode, runs the test, then restores the interrupt mode back to its initial condition.

The actual command executed to cause an interrupt is to seek the current track on which the selected Hard Disk is positioned. The CTC chip on the Hard Disk interface board is used to generate a "Vectored Interrupt" (Z80 mode 2 interrupt). The "HDBINTRQ" signal of channel 0 is responsible for triggering the vectored interrupt in the counter mode. The interrupt test fails if the interrupt service routine is not executed within several seconds, and an appropriate failure message is displayed on the video screen.

**<S> Seek Track**

The Seek Track option requires 4 digits for the track number in the range of 0000-1023. This is the track number and NOT the cylinder number. You may seek with a Read Verify to ensure that the drive found the target track, or select not to verify to determine if the drive can seek a track independent of a read operation. The default is No Verify.

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**<C> Carriage Step**

Carriage Step allows the entry of two track numbers to step between. Four digits are required, and you must enter the low track number first. The seeks are accomplished without a read verify. Note that seeking between tracks on the same cylinder will not cause a step - just an alternate head to be selected.

**<L> Slew Seek Test**

The Hard Drive employs slew seeking to optimize step rates. On long distance seeks, the step rate is actually done at a higher rate than for short seeks.

The test causes the head assembly to seek the extreme tracks, then moves toward the middle tracks, and then toward the extreme tracks again. This provides a method of exercising the slew seek feature of the drive and operates the circuitry for scope probing in the event of a failure in this area.

**<R> Read Current Track**

This command reads the current track on which the head is positioned, either in the interrupt or polled status mode. System software uses the polled status mode for the format routine only. All other Hard Disk I/O is accomplished using the interrupt mode.

The interrupt mode is faster than the polled status mode. If the interrupts are not functional, then the speed of reading the sectors will slow down and a "NO INTERRUPT RECEIVED" error message will be displayed. The speed of reading the track is proportional to the accuracy of the controller VCO tracking the data rate. The controller does 16 retries, auto restores at a slow step rate, then performs 16 more retries before exiting with an error status when invalid information is encountered.

**<W> Write Current Track**

The Write Current Track option writes 512 "B6" hex bytes on each of the 17 sectors of the track on which the head is positioned. The program warns of the possibility of destroying customer data, and requires a "Y" (yes) response to continue. The routine checks for the write protect condition and displays "WRITE PROTECTED DRIVE" if the drive is protected. The program will not normally allow a write on a drive with a write protect condition. **HOWEVER, IN A FAULT ENVIRONMENT THERE ARE NO GUARANTEES.** It is best to attempt a write on the "Diagnostic Track" (track 1) to check the write protect function.

## &lt;X&gt; Random Read

The Random Read test is the most demanding test among the options. The target track to be read is displayed on the video as the routine runs. Note that only the first sector of each track is read, and not all sectors nor random sectors.

---

**8 MEGABYTE HARD DISK ALIGNMENT PROCEDURE**

---

```
*****
* CAUTION! CAUTION! CAUTION! CAUTION! CAUTION! *
*****
* Some of the labels used for jumpers and test points are *
* used more than once. There are two test points labeled *
* 'R'. In the documentation jumpers will be referred to *
* as pairs, not as individual pins. This should leave no *
* confusion as to what pins are being referenced. *
*****
*****
```

**PC BOARD JUMPERS**

Before beginning the alignment procedures, be sure the controller board has been properly jumpered. The correct jumpers are:

U-V  
J-K  
Q-R if U4 is a WD1100-02  
S-R If U4 is a WD1100-12

There should be NO other jumpers on the board.

**CONTROLLER BOARD ADJUSTMENTS**

NOTE: Use the <A> option from the HDDIAG main menu.

There are three potentiometers on the controller board. They are located near the power switch and are numbered R1, R2, and R3. R1 adjusts the one shot used to start the reading of a track. R2 adjusts the bias on the error amplifier. R3 adjusts the free running frequency of the VCO.

Before starting this procedure, the drive should be turned on and running for approximately 5 minutes. As well, the unit should be checked to see that all modifications (see Technical Bulletin series HD) have been applied.

### 1. Voltage controlled oscillator (VCO) adjustment

Install a push-on jumper at test pins W-X located near U9 pin 14. Check TP1, near U1 pin 1, for a logic HIGH (+3.5 to +5 VDC). If TP1 is NOT a logic HIGH, proceed to Step 3.

If TP1 is at a logic HIGH, attach an oscilloscope probe to TP5 located between U11 and U12. Set the oscilloscope for 2 volts per division, DC coupled. Set the sweep speed for 100 nanoseconds (.1 microseconds) and adjust the trace for a stable display.

Adjust R3 so that the square wave at TP5 has a period of 115 nanoseconds (+/-5 nS).

Remove the push-on jumper at W-X.

### 2. Static error amplifier adjustment

Install a push-on jumper across test pins P-R located between U18 and U19. Install a push-on jumper across test pins S-T located next to Q1 near the front edge of the board.

Attach an oscilloscope probe to TP26 located near U1 pin 1. Set the oscilloscope for 20 millivolts per division, DC coupled. Set the sweep speed for comfortable viewing, LINE trigger. DO NOT use a voltmeter for this adjustment!

Adjust R2 so that the signal at TP26, located near U1 pin 1, is at 0 VDC, +/-20 millivolts. Note that the signal appearing on the oscilloscope will have much noise with it. The center of the 'noise band' needs to be as close to 0 VDC as possible.

Remove the push-on jumper at test pins P-R and move it to test pins M-N located near U17 pin 7.

Connect the oscilloscope probe to test pin W of the W-X pair. The voltage should be 0 VDC +/-50 millivolts. Adjust R2 until the signal at test pin W is 0 VDC +/-20 millivolts.

Remove the push-on jumpers at test pins S-T and M-N.

### 3. "DRUN" adjustment

The "DRUN" adjustment adjusts the one-shot that is used to start the reading of a track.

Connect the oscilloscope probe to TP9 located between U9 and U10. Set the oscilloscope for 2 volts per division, DC coupled. Set the sweep speed for 100 nanoseconds (.1 microseconds) per division, NEGATIVE INTERNAL trigger.

Adjust R1 so that a negative going pulse of 287 nanoseconds (+/-5 nS) is visible. It may be necessary to adjust the trigger level on the oscilloscope. Use the MIDDLE of the rising and falling edges of the waveform as measurement points. The signal after the 287 nanoseconds pulse may appear to be active, or both HIGH and LOW at the same time. This is normal.

It is CRITICAL that the 287 nanoseconds pulse be clean.

### 4. Dynamic error amplifier adjustment

Connect the oscilloscope probe to test point S of the S-T pair. Set the oscilloscope for 1 volt per division, DC coupled. Set the sweep for comfortable viewing, LINE trigger.

Adjust R3 for a -1 VDC signal. This may have to be mentally "averaged" due to normal signal changes above and below -1 volt.

Small pulses, both positive and negative, may be seen on the -1 VDC signal. Adjust R2 so that these pulses are as small as possible and the positive and negative pulses are equal in amplitude.

### 5. Fine tuning

Reformat the Diagnostic Track (track1) using HDDIAG option <F>. Repeat steps 1 through 4 until no further improvement can be made.

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**12 MEGABYTE HARD DRIVE DIAGNOSTICS**

**CHAPTER 8**

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**Radio Shack®**

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## HD Diagnostics

INTRODUCTION

---

The following programs are provided to assist in alignment and troubleshooting of the Twelve Megabyte Hard Disk System:

HDREL56

HDDIAG56

```
*****
*** WARNING!  WARNING!  WARNING!  WARNING!  WARNING! ***
*****  
***  
*** THESE PROGRAMS CAN DESTROY DATA!!! BE CAREFULL ***  
*** AND BE CERTAIN YOU UNDERSTAND HOW TO USE THEM ***  
*** BEFORE ATTEMPTING TO USE THEM FOR DRIVE ***  
***      VERIFICATION OR TROUBLESHOOTING! ***  
***  
*****
```

## GENERAL DIAGNOSTICS PRECAUTIONS:

1. Do not attempt to transfer the diagnostics to TRSDOS 4.2 floppy or TRSDOS-II! Boot the diagnostics on TRSDOS 2.0b by hitting the reset and holding down the <BREAK> and <REPEAT> keys simultaneously.
2. There will be some bad blocks on the Hard Drives. While the Operating System does not use and ignores them, they will be detected by the diagnostics! DO NOT ASSUME THE PLATTER IS DEFECTIVE BECAUSE THE DIAGNOSTICS DETECTS A BAD BLOCK! Check the chart on the bottom of the drive to verify which blocks are bad on the drive you are testing.

QUICK REFERENCE SECTION

---

**"HDREL56"**

---

**Execution:**

1. In TRSDOS type <HDREL56> and <ENTER>.
2. Answer "ENTER DRIVE SELECT PORT. <ENTER> - "C" .." prompt by typing <ENTER> (This maps the drive at port  $\emptyset C\emptyset$  hex to  $\emptyset CF$  hex).
3. Answer "ENTER DRIVE # TO TEST (4,5,6,7) ." with <4> and <ENTER>.

**OPTIONS:**

<W> Track 1 is reserved for use as a "diagnostics" track. No system information or data is maintained on this track. The <W> command will write, read and verify data on this track. This option may be safely used to insure proper write operation within limits.

<A> The "A" option will sequentially write, read and verify data ON ALL TRACKS!

```
*****
*** WARNING! WARNING! WARNING! WARNING! ***
*****
***      THIS OPTION WILL DESTROY ANY DATA ON THE TRACKS ***
***      IT WRITES. IT SHOULD ONLY BE USED BEFORE DATA ***
***      IS ON THE DRIVE, OR FOR TROUBLESHOOTING WHEN ***
***      THERE IS NO HOPE FOR RECOVERING DATA FROM THE ***
***      THE DRIVE! AN ATTEMPT TO "SAVE" THE DATA ON ***
***      THE HARD DRIVE SHOULD BE MADE BEFORE USING THIS ***
***                      OPTION. ***
*****
*****
```

- <R> Reads all tracks sequentially and checks the status register for any errors. Errors will occur on bad blocks! Check the chart on the bottom of the drive, to ascertain which tracks have bad blocks. The blocks identified by the diagnostic should agree with the chart.
- <S> Quick version of the <R> command. Checks tracks 0000, 0124 (before precomp applied) and 0128, 0255 (precomp applied).
- <X> Generates a random track number, seeks the track, reads and checks status register for errors.
- <D> Selects drive to test.
- <Q> Exit to TRSDOS.

**"HDDIAG56"**  
-----

Description: This program tests and manipulates various Hard Disk controller circuitry. One option (<A>) provides a method for adjusting the controller VCO, static error Amplifier, "DRUN", and dynamic error amplifier.

**Execution:**

1. Type <HDDIAG56> and <ENTER>
2. Type <ENTER> to map drive at Port 0Cx hex.
3. Select drive number to test.

**OPTIONS:**

- <T> Writes and verifies data to the controller task register.
- <0> Restores the drive to track 0 (cylinder 0, head 0).
- <S> Allows user to seek a selected track with optional seek verification.
- <C> Allows user to step heads between two selected tracks.
- <L> Steps drive from outer-most to inner-most tracks in decreasing order. Exercises operation of step slew rate changes.
- <M> RAM test for static 2114 150ns RAMS on controller.

- <I> Seeks current track to generate an interrupt. Verifies that interrupt is received.
- <D> Selects drive number to test.
- <A> Self-prompts alignment procedure (see page 12 for alignment procedure).
- <D> Reads and displays current controller status.
- <X> Generates random track number, reads track, and checks status register for errors.
- <R> Reads current track, checks status register for errors.
- <W> Writes to currently selected track, checks for errors.

```
*****
*** WARNING! WARNING! WARNING! WARNING! WARNING! ***
***** THIS OPTION WILL DESTROY CUSTOMER DATA ****
*** IF A TRACK OTHER THAN THE DIAGNOSTIC TRACK ***
*** (TRACK 1) IS WRITTEN. ***
*****
```

- <F> Formats Diagnostic Track (track 1) and checks for errors. This test does not interfere with customer data providing head position and head select are functioning properly.
- <E> Enable/disable interrupts. Option allows selection of interrupt status to facilitate fault isolation.
- <Q> Exit to TRSDOS.

TECHNICAL SECTION

---

---

History Table and Error Description

---

## DRIVE NUMBER:

Specifies which drive the logged error occurred on.

## CYLINDER NUMBER, HEAD NUMBER:

The cylinder number is analogous to a floppy disk drives "Track". There are 230 cylinders on the drive. Each cylinder consists of six media surfaces which may be accessed by one of six heads. The 230 cylinders times the 6 heads/cylinder yields 1380 tracks per drive. By observing logged errors, it is possible to determine if a fault may be caused by a defective head or head circuitry (all errors occur on a particular head), or if a platter has been damaged (all errors occur on a particular cylinder only).

## ID NOT FOUND:

During initialization, an ID Field is written for each track and sector. This error occurs when the disk controller cannot lock onto the ID Field data, and as a result, cannot find the target sector to read or write data. Infrequent occurrences of this error may indicate that the "DRUN", "ERROR AMPS", or "VCO" require adjustment (using HDDIAG56 program).

Remember that some "media flaws" are inherent to the hard disk media and these will be detected by the diagnostic. Compare the logged faults with the "Media Error Map" which is on the bottom of the drive assembly to determine if there is a marked increase in the number of flaws. If an increase is noted, observe the conditions under which the faults are logged. A certain head or cylinder may be at fault.

## DATA CRC:

During a read operation, some of the bits in the 512 bytes of data on the current sector were in error. Suspect the CRC Generator/checker chip (U6 WD1100-4) if this is a frequent error.

**ID CRC:**

During an attempted read or write operation, some of the bits in the ID field (containing sector location information) were incorrect. This may be due to flaws in the media or an operational failure. Consistant ID field CRC errors may be caused by the CRC Generator/checker chip (U6 WD1100-4) or misalignment of "VCO", "DRUN", or "Error Amp".

**BAD BLOCK:**

This error only occurs if the media was last formatted by the Shugart factory and indicates that a sector is unusable. TRSDOS does not mark faulty sectors with "Bad Block" marks. TRSDOS will log "Bad Blocks" as specific errors (ID NOT FOUND, ID CRC, etc.), and will not use those sectors of the Hard Disk. If the media has been initialized by TRSDOS, then HDREL56 will also log "Bad Blocks" by specific type errors.

**DAM NOT FOUND:**

Indicates that the data address mark (a unique byte that identifies the beginning of a data field) could not be found. This may be due to media, or point to a damaged AM Detector chip (U11 WD1100-03), or related circuitry.

**ABORTED COMMAND:**

This is a major fault, and the disk controller will not accept a command if this occurs. Run "HDIFAC" or "HDDIAG56" to obtain a better indication of the cause of this fault.

**HDDIAG56**  
-----

The Hard Disk Diagnostic Program consists of tests which exercise the Hard Disk controller and Drive assemblies. The flexibility of the tests provide a method for categorically isolating faults in the controller or drive assembly.

Features have been implemented to safeguard the customer's data. Track 1 on each drive is designated as a "Diagnostic Track". Read and write loop testing may be done on this track without concern for the customer's data. In the event that a fault causes the destruction of the diagnostic track ID field, the <F> option allows reconstructing the diagnostic track.

Even with these features, ALWAYS BE CERTAIN THAT THE CUSTOMER HAS BACKED UP THE DATA FILES IF IT IS AT ALL POSSIBLE before servicing the drive!

**Options:****<T> TASK REGISTER TEST**

The Task Register Test provides several modes of operation. The Single test mode allows the test to run through once, while the Loop Test Mode allows continuous exercising of the test for signal tracing with a scope.

The Task Registers are located in the "8X300" CPU. Data is written to, read, and checked to verify proper register operation.

The registers are addressed by CA-CE hex. The logic pattern which is written and read is a rotating "logic 1" in a field of "zeros", followed by a rotating "logic 0" in a field of "ones". This provides a means of testing the address lines "A0" thru "A2" ("A3" is always high). The input buffers for the read and write control functions, the data lines and data access lines internal to the controller board, and the chip enable function are all required to operate in order for this test to pass. The test will display "TASK REGISTER TEST PASSES" if all the required signal paths are good. If there is a mismatch of data written and read, then the difference is shown as the address and data byte, one error at a time. Pressing any key will advance the test.

If the task register or support circuitry is defective, then no commands required to operate the drive can be executed.

**<M> Static RAM Test**

The static RAMs (U-17, U-18) provide the I/O buffer for data transfers to/from the Hard Disk. The Hard Disk is formatted with 512 byte physical sectors, so 512 bytes of the static RAM are used to buffer the data between the host and the Hard Disk.

The Hard Disk host computer is not capable of keeping up with the high data rate required for Hard Disk read/write operations. For this reason the host computer interfaces through the static Ram buffer with the data to transfer. In addition, the "8X300" uses approximately 20 bytes of the RAM as a "scratchpad".

The Static RAM test exercises the buffer area of the RAM, but not the scratch space - It's not available to the host computer. Additionally, the RAMs are in parallel, and therefore affect each other. Due to these limitations in testing the RAMs, the test may not always detect a fault. If Static RAM problems are suspected, it may be wise to substitute "known good" RAMs (Remember - 150 nanosecond RAMs are required!).

**<I> Interrupt Test**

The interrupt test checks the ability of the controller to generate an interrupt upon completion of a command. The controller can be operated in an interrupt or poll status register mode. This mode may be controlled by toggling the <E> Enable/Disable Interrupts feature.

The current interrupt status is displayed on the right side of the status line. Note that the interrupt test enables the interrupt mode, runs the test, then restores the interrupt mode back to its initial condition.

The actual command executed to cause an interrupt is to seek the current track on which the selected Hard Disk is positioned. The CTC chip on the Hard Disk interface board is used to generate a "Vectored Interrupt" (Z80 mode 2 interrupt). The "HDBINTRQ" signal of channel 0 is responsible for triggering the vectored interrupt in the counter mode. The interrupt test fails if the interrupt service routine is not executed within several seconds, and an appropriate failure message is displayed on the video screen.

**<S> Seek Track**

The Seek Track option requires 4 digits for the track number in the range of 0000-1379. This is the track number and NOT the cylinder number. You may seek with a Read Verify to ensure that the drive found the target track, or select not to verify to determine if the drive can seek a track independent of a read operation. The default is No Verify.

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**<C> Carriage Step**

Carriage Step allows the entry of two track numbers to step between. Four digits are required, and you must enter the low track number first. The seeks are accomplished without a read verify. Note that seeking between tracks on the same cylinder will not cause a step - just an alternate head to be selected.

**<L> Slew Seek Test**

The Hard Drive employs slew seeking to optimize step rates. On long distance seeks, the step rate is actually done at a higher rate than for short seeks.

The test causes the head assembly to seek the extreme tracks, then moves toward the middle tracks, and then toward the extreme tracks again. This provides a method of exercising the slew seek feature of the drive and operates the circuitry for scope probing in the event of a failure in this area.

**<R> Read Current Track**

This command reads the current track on which the head is positioned, either in the interrupt or polled status mode. System software uses the polled status mode for the format routine only. All other Hard Disk I/O is accomplished using the interrupt mode.

The interrupt mode is faster than the polled status mode. If the interrupts are not functional, then the speed of reading the sectors will slow down and a "NO INTERRUPT RECEIVED" error message will be displayed. The speed of reading the track is proportional to the accuracy of the controller VCO tracking the data rate. The controller does 16 retries, auto restores at a slow step rate, then performs 16 more retries before exiting with an error status when invalid information is encountered.

**<W> Write Current Track**

The Write Current Track option writes 512 "B6" hex bytes on each of the 17 sectors of the track on which the head is positioned. The program warns of the possibility of destroying customer data, and requires a "Y" (yes) response to continue. The routine checks for the write protect condition and displays "WRITE PROTECTED DRIVE" if the drive is protected. The program will not normally allow a write on a drive with a write protect condition. **HOWEVER, IN A FAULT ENVIRONMENT THERE ARE NO GUARANTEES.** It is best to attempt a write on the "Diagnostic Track" (track 1) to check the write protect function.

**<X> Random Read**

The Random Read test is the most demanding test among the options. The target track to be read is displayed on the video as the routine runs. Note that only the first sector of each track is read, and not all sectors nor random sectors.

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**12 MEGABYTE HARD DISK ALIGNMENT PROCEDURE**

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The hard disk controller board adjustments need to be done only on the primary hard drive. The motor speed will need to be adjusted on each hard drive in the system.

**CONTROLLER BOARD ADJUSTMENTS**

There are three adjustments on the controller board. R1 adjusts the one shot used to start the reading of the track. R18 adjusts the bias on the error amplifier. C33 adjusts the free running frequency of the VCO.

Run the HDDIAG56 program and proceed to step 1 of the alignment procedure. Before starting this procedure, the drive should be running for about 2 minutes to allow it to come to its full final speed.

**1. Voltage controlled oscillator (VCO) adjustment.**

Check for a voltage from +2.4 to +3.0 VDC at pin 14 of U32. If the voltage is not within this range, check R22, R24, and U32.

Set channel A of the oscilloscope to 2 volts per division. Attach the Channel A test probe to TP9. TP9 is between U33 and U34.

Set Channel B to 1 volt per division, DC coupled, and attach it to TP8. TP8 is between the voltage regulator and U32.

Set the time base for 100 nanoseconds per division. The trigger should be on NORMAL and on channel A.

Adjust C33 to obtain exactly a 100 nanoseconds waveform on channel A. Adjust R18 for a +2.5 Vdc level on channel B.

When this has been done press enter to proceed on to the next step.

**2. "DRUN" adjustment**

DC couple channel A and connect the probe to TP1. TP1 is located between U1 and U2. Set the timebase to 50 nanoseconds per division. Set the trigger to NEGATIVE and NORMAL.

R1 should be adjusted so that channel A's waveform is clean, and low for 250 nanoseconds (+/- 5 nanoseconds). After the 250 nanoseconds, the signal will appear to be both high and low at the same time. This is normal.

**3. Error Amplifier Adjustment.**

This adjustment must be done during a continuous read. Since the DRUN adjustment also requires this, the Error Amplifier Adjustment should be done while the DRUN counter is running on the screen.

Set channel A to 1/2 volt per division and DC coupled. Connect the probe to TP8. Set the timebase to 20 microseconds per division. Set the trigger to NORMAL and adjust the level control for a steady display.

Use R18 to minimize the pulses going up and down on the oscilloscope. They should be as small as possible and the positive and negative pulses should be about equal in size.

Once the above steps have been completed track 1 should be reformatted and the above procedure should be repeated until R18 and C33 do not require any further adjustment.

**MOTOR SPEED ADJUSTMENTS**

Each motor speed board in the system should be aligned.

1. Set channel A to 100 millivolts per division and AC coupled. Connect the test probe to the lead of R26 closest to the power transistor leads. R26 is the large resistor next to the power transistors on the motor speed board. Set channel B to 1 volt per division, AC coupled, and connect the probe to TP3 on the drive logic board.

2. Set the time base for 2 milliseconds per division. Trigger on channel B. Adjust R5 so that the period of the channel B waveform is approximately 16.66 ms. Change the oscilloscope trigger to LINE and adjust R5 for a stable display. The oscilloscope in this case functions as sort of an "electronic strobe disk".

3. Trigger on channel A and adjust R23 so that the positive and negative voltage spikes shown on channel A are minimized.

4. Repeat steps 2 & 3 until no further improvement can be made.

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**68000 FAMILY DIAGNOSTIC TESTS**

**CHAPTER 9**

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## INTRODUCTION

The 68000 Diagnostic Software group contains several different diagnostic programs to check the Radio Shack Model 16 Microcomputer, as well as the 16-bit upgrade packages available for the Radio Shack Model II and Model 12 Microcomputers.

Included in the group are three memory tests, each with three versions. Each of the three memory tests uses a different algorithm, thereby testing as many different combinations as possible. Also included are four tests which check the 68000 memory system from the Z-80 processor.

Also in the group is a program for testing the interrupt structure of the 68000 system, and several support programs to allow the diagnostics to be run on both the Model 16 and the Model II/12 upgrades.

## HOW THE DIAGNOSTICS WORK

The Model 16 is actually two computers in one. The Z-80 based system is identical to the Model II, thereby allowing all Model II software to run. Before running the 68000 Diagnostics the Model II Diagnostic Software Group should be run to thoroughly check the Z-80 portion of the system.

The 68000 side of the system consists of the MC68000 processor, the associated memory board(s), and necessary support circuitry. It has no I/O devices (video, disk) of its own, THEREFORE RELYING ON THE Z-80 TO LOAD OR SAVE PROGAMS AND INFORMATION. If the Z-80 portion of the machine is not functioning properly, the diagnostics will have no access to the 68000 side of the system.

When running 68000 based programs the Z-80 is delegated to the "simple" tasks of disk I/O, video I/O, keyboard processing, etc. All programs loaded into the 68000 system are transferred from the disk, through the Z-80 system, and into the 68000 memory.

To do this a special program called RUN is used. RUN first loads into the Z-80 system and then loads the requested 68000 program into the 68000 memory. The syntax for RUN is:

**RUN [filespec]**

where [filespec] is one of the 68000 diagnostic programs. **ALL 68000 BASED PROGRAMS MUST BE LOADED IN THIS MANNER!**

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The programs in the 68000 Diagnostic Software group can be divided into two groups: 68000 based programs and Z-80 based programs. All 68000 programs end with either a "6" or a "68":

CHKR68      TINTEST6      QMAT68      (etc)

All 68000 based programs must be "RUN" (see above). The 68000 based programs use the MC68000 processor to execute the program, and therefore give the best indication of proper operation of the 68000 system.

All Z-80 based memory diagnostic tests start with "P" and end with "16":

PCHKR16      PREMEM16      (etc)

These programs exercise the 68000 memory by using the Z-80 processor. They are loaded in the normal manner:

[filespec]<ENTER>

These programs give a good indication of the ability of the Z-80 side to transfer information to the 68000 side -- a vital ability if the computer is to be able to load and run 68000 based programs.

All other programs on the diskette are Z-80 programs, and are loaded in the normal manner:

[filespec]<ENTER>.

There are four (4) different memory tests, and three (3) versions of each test. The first version is the "QUICK" version. Most of the memory test are relatively quick, but the MAT68 is very long, so a specific "quick test" (QMAT68) is supplied:

QMAT68      CHKR68      OFFLIM6      INTEST6

The second version is the "TIMED" version. Since most tests are rather short, a timed version is included to allow the test to run for a specified longer length of time. These tests are indicated by a "T" prefix:

TCHKR68      TOFFLIM6      TINTEST6

Since MAT68 is very long, the "quick" version is included but a "timed" version is not included.

The third version is the "CONTINUOUS" version. This version allows the test to run until terminated by the user. These tests are indicated by a "C" prefix:

CCHKR68      COFFLIM6      CINTEST6      CMAT68

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## OPERATING THE DIAGNOSTIC PROGRAMS

Before running the 68000 Diagnostic group, you must run the Model II Diagnostics to assure that the Z-80 sections of the computer are running properly.

Once the Z-80 sections are tested, boot the 68000 Diagnostic group in the normal manner. The Tandy Logo and copyright message should appear, along with TRSDOS READY.

All programs can be accessed from TRSDOS READY, but the diagnostics that will run from the 68000 sections must be loaded using the RUN program.

At TRSDOS READY, type:

**RUN [filespec] <ENTER>**

Where [filespec] is the name of one of the 68000 based diagnostics. Remember, all 68000 based diagnostics have either "6" or "68" as their last letter or letters.

When you hit <ENTER> the following messages should appear on the screen, one line at a time:

**XBOOTL version aa.bb  
Program Loaded  
IFC68 version yy.zz**

where aa.bb and yy.zz are version and release numbers of XBOOTL and IFC68, respectively.

The selected diagnostic program will now load and execute.

When loading Z-80 based diagnostics the process is the same as used to load any other program. At TRSDOS READY type:

**[filespec] <ENTER>**

where [filespec] is the name of one of the Z-80 based programs. Note that all Z-80 based memory diagnostics start with "P" and end with "16".

**MANY OF THE PROGRAMS IN THE MODEL 16 DIAGNOSTIC GROUP ARE RUN USING THE 68000 SYSTEM. PLEASE MAKE A CAREFUL NOTE OF WHICH PROGRAMS THAT ARE RUN UNDER THE Z-80 SYSTEM.**

## DISCUSSION OF THE PROGRAMS

**CHKR68**

This is a 68000 based program, and must be loaded using RUN.

CHKR68 uses a checkerboard type of pattern using test data of 00H, FFH, 55H, and AAH. CHKR68 runs ONE pass using all four patterns for a total of 4 passes.

**TCHKR68**

This is a 68000 based program, and must be loaded using RUN.

TCHKR68 is the timed version of CHKR68. It runs for 30 minutes. The number of completed passes is updated on the screen. To exit the program before the 30 minutes is up, type <BREAK>.

**CCHKR68**

This is a 68000 based program, and must be loaded using RUN.

This is the continuous version of CHKR68. The program will run until terminated by the user by typing <BREAK>. The number of completed passes is updated on the screen.

**OFFLIM6**

This is a 68000 based program, and must be loaded using RUN.

OFFLIM6 tests the memory offset and limit registers. It makes ONE pass before returning to TRSDOS. Note that this test logs any errors as they occur.

The memory offset registers are used to add a specific offset to a memory address. This is most often used in multiuser systems like XENIX. Each user is assigned an area in memory which becomes his "space". The lowest address of this space is assigned to his offset register. The offset is now added to each memory address this user produces to produce an absolute address.

User supplied address	Offset	Absolute Address
000000	+ 500000	= 500000
0032FE	+ 400000	= 4032FE

By using this scheme each user can be assigned a different space in memory without the user being aware that his program does not actually start at 0000 (or any specified address).

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The highest address assigned to a user's memory "space" is loaded into his limit register. If a user tries to address memory above his limit, an error is produced. This is approximately the same as an OM ERROR.

**TOFFLIM6**

This is a 68000 based program, and must be loaded using RUN.

This is the timed version of OFFLIM6, and runs 30 minutes. The number of passes is updated on the screen. Type <BREAK> to exit before the 30 minutes is up.

**COFFLIM6**

This is a 68000 based program, and must be loaded using RUN.

This is the continuous version of OFFLIM6, and runs until terminated by pressing <BREAK>. The number of passes is updated on the screen.

**INTEST6**

This is a 68000 based program, and must be loaded using RUN.

INTEST6 tests the interrupt structure of the 68000 system. It will make eleven (11) passes through the system. The results of the tests are written to the screen.

INTEST6 does not stop when it receives an error. Each pass MUST be visually checked for errors. The scrolling can be halted by pressing <HOLD>. Pressing <HOLD> a second time will continue the test. Press <BREAK> to exit the test and return to TRSDOS.

Note that if the <HOLD> key fails to function this may indicate a problem with the interrupt system.

**TINTEST6**

This is a 68000 based program, and must be loaded using RUN.

TINTEST6 is the timed version of INTEST6, and runs for approximately 30 minutes. It can be terminated before this time is up by pressing <BREAK>.

**CINTEST6**

This is a 68000 based program, and must be loaded using RUN.

CINTEST6 is the continuous version of INTEST6. Terminate the program by pressing <BREAK>.

**MAT68**

This is a 68000 based program, and must be loaded using RUN.

MAT68 is the Modified Address Test, similiar to the one used in MEMII for the Model II, but only tests the 68000 memory. MAT68 requires approximately 55 minutes to run, so there is NO timed MAT68 (TMAT68). The completed passes are logged on the screen.

MAT68 can be terminated by typing <BREAK>.

**CMAT68**

This is a 68000 based program, and must be loaded using RUN.

CMAT68 is the continous version of MAT68. It can be terminated by pressing <BREAK>.

**QMAT68**

This is a 68000 based program, and must be loaded using RUN.

QMAT68 is the quick version of MAT68. It is possible for QMAT68 to miss some errors that would have been caught by MAT68. Only two (2) passes are completed and logged.

**PREMEM16**

This is a Z-80 based test. DO NOT use "RUN".

PREMEM16 combines the MAT test and CHKR tests. The Z-80 is used to check the 68000 memory. You can return to TRSDOS by typing <BREAK>.

**PCMAT16**

This is a Z-80 based test. DO NOT use "RUN".

PCMAT16 is a continous version of MAT, but uses the Z-80 to exercise the 68000 memory. The test can be terminated by typing <BREAK>.

**PQMAT16**

This is a Z-80 based test. DO NOT use "RUN".

PQMAT16 is the quick version of MAT, and uses the Z-80 to check the 68000 memory. To terminate the test before completion, type <BREAK>.

**PCHKR16**

This is a Z-80 based test. DO NOT use "RUN".

PCHKR16 is the Z-80 based version of the CHKR test. The Z-80 is used to check the 68000 memory.

**AUTO16**

AUTO16 is a "DO" file. At TRSDOS ready type:

**DO AUTO16**

AUTO16 will automatically load and execute the quick versions of all the memory tests.

## OTHER PROGRAMS

There are other programs in the 68000 Diagnostic group which are not diagnostic programs, but are necessary to properly run the diagnostics. These programs are:

**RUN**

RUN is the "bootstrap" program necessary to load 68000 based programs into the 68000 memory. Although listed as a program, RUN is actually a command added to TRSDOS. Its syntax is:

RUN [filespec]

where [filespec] is the name of one of the 68000 based diagnostic programs.

**IFC68**

IFC68 is an auxiliary program called by RUN. The parameters used by IFC68 are set up by RUN, so IFC68 is useless without RUN.

IFC68 should never be executed by itself. Its only useful access is through RUN.

**BOTH**

DO NOT "DO BOTH" ON THE DIAGNOSTIC DISKETTE. ALWAYS MAKE A BACKUP FIRST, THEN PERFORM THE PATCHES ON THE BACKUP, NEVER ON THE ORIGINAL!

BOTH patches TRSDOS for the necessary wait to prevent the occurrence of ERROR 8, but does not patch the higher step rate used on the Model 12 and Model 16. This allows the diskette to work on Model II, Model 12, or Model 16 computers.

To use BOTH, at TRSDOS READY type:

DO BOTH <ENTER>

Note that if the diskette has previously had the BOTH patches applied STRING NOT FOUND - ABORT errors may be produced. If the diskette was previously patched, ignore these errors.

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**AUTOTND**

**8 INCH THINLINE™ DOUBLE SIDED DRIVE VERIFICATION PROGRAM**

**-- and --**

**AUTODRV8**

**8 INCH SINGLE SIDED DRIVE VERIFICATION PROGRAM**

**CHAPTER 10**

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AUTOTND - DOUBLE SIDED DISK DRIVE VERIFICATION PROGRAM  
AUTODRV8 - SINGLE SIDED DISK DRIVE VERIFICATION PROGRAM

**IMPORTANT NOTE:** AUTOTND was designed to verify double sided drives like the Tandon Thinline™. AUTODRV8 was designed to verify single sided drives like the CDC or TPI. The two tests function in an identical manner. Any differences will be noted.

#### INTRODUCTION

AUTOTND and AUTODRV8 are disk drive verification programs designed to verify operation of the various 8 inch drives. Both programs are similiar in function to the EXPTST program used on the Model II.

AUTOTND and AUTODRV8 now check for the number of VALID drives attached to the system. Each drive to be tested MUST have a blank diskette in it (single or double-sided as appropriate to the drive being tested) when the program prompts you to remove the system diskette. AUTOTND will checks both sides of the diskette.

#### RUNNING THE PROGRAMS

```
*****
*          !! WARNING !!
*
*      THIS TEST WILL DESTROY ANY DATA
*      ALREADY PRESENT ON THE TEST DISK
*      USE ONLY A BULK ERASED DISKETTE
*      TO PERFORM THIS TEST PROCEDURE
*****
*****
```

Boot the Diagnostic Diskette in the normal manner. At TRSDOS READY type:

**AUTOTND <ENTER>**

or

**AUTODRV8 <ENTER>**

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The program will load and display the following header. The single sided version will be only slightly different.

**MODEL 16 FLOPPY DISK DRIVE DIAGNOSTIC TEST  
FOR TANDON DOUBLE SIDED "THIN LINE" DRIVES  
(c)(p)1982 TANDY CORP. ALL RIGHTS RESERVED  
REV DATE xxxx y, zzzz**

**REMOVE SYSTEM DISKETTE, INSERT 2 SIDED ERASED DISKETTES IN DRIVES + CLOSE DOORS**

**HIT ANY KEY TO CONTINUE**

Where xxxx y, zzzz is the revision date in month-date-year form.

Insert KNOWN GOOD, ERASED diskettes in the drives to be tested. Be sure and use the proper type of diskette, single or double sided, for the drive(s) being tested. Close the doors and press any key to continue.

The screen should clear, and the following message should now appear:

**PLEASE WAIT: ANALYZING SYSTEM FOR 30 SECONDS**

(This message will not appear while AUTODRV8 is running)

The programs now checks system operation and jumper configuration. The CPU WAIT state jumpers and RTC interrupt jumper, the drive M2 jumper, the motor speed, and motor timeout are all checked. If an error occurs AUTOTND or AUTODRV8 will write an appropriate error message to the screen. If there are no errors the test will continue.

Once the system test is complete, and any errors have been corrected, the test will continue. For proper operation of the test, it is MANDATORY that you use KNOWN GOOD, ERASED diskettes. This will eliminate the possibility of media errors affecting the test results. If the drives under test show a high number of errors, first try using NEW diskettes. If this cures the problem the old diskettes are wearing out. They should be destroyed. Do not try to use the diskettes for another purpose, as this would be inviting further trouble due to media errors.

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The screen will clear and the following "menu" will appear:

"O":STEP OUT/"I":STEP IN/<ENTER>:ONE WR&RD/"C":LOOP WR&RD/"R":LOOP READ  
<BREAK>:END LOOP/"N":SELECT NEXT DRIVE/"T":SELECT SIDE x/"A":REPEAT WR&RD  
AUTODRV8 --/"X":EXCHANGE TEST/

[DONE]

TRACK	WRITE	READ	SEEK	HARD	TRACK
	RETRY	RETRY	ERROR	ERROR	TOTAL
0000	0000	0000	0000	0000	0000

AUTOTND and AUTODRV8 now enter the "A"utomatic mode. This mode writes four tracks on each selected drive. AUTOTND writes eight tracks, four on side zero and four on side one. Once all drives have been tested, press and hold <BREAK> until the "DONE" message appears.

#### COMMANDS

<O> STEP OUT

Step the head on the selected drive 1 track towards Track 00

<I> STEP IN

Step the head on the selected drive 1 track towards Track 76

<T> TOGGLE SIDE SELECT (AUTOTND only)

Toggle the side select option of the drive under test. The selected side will appear in the menu list:

"T":SELECT SIDE x                where "x" is the side selected (1 or Ø)

<X> EXCHANGE TEST (AUTODRV8 only)

Checks for disk drive reliability under both TRSDOS 2.0 format (256 bytes per sector) and TRSDOS 4.x format (512 bytes per sector).

This test will require TWO sets of disks -- One blank set and one set previously formatted under TRSDOS 4.2 or 4.3.

The user must exchange the diskettes when prompted by the program.

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**<ENTER> ONE WR/RD PASS**

Format, write sectors, read sectors, and verify the results on the selected track and side of the current drive under test. Effectively one diagnostic "pass".

**<C> CONTINUOUS WR/RD PASSES**

Same format, write, read, verify test as the <ENTER> option, but executes continuously until <BREAK> is pressed.

**<R> READ AND VERIFY**

Read and verify the selected track on the current drive.

**<BREAK> EXIT TEST**

Exit the test loop after the diagnostic "pass" in progress is finished.

**<N> NEXT DRIVE**

Select the next valid drive for testing.

**<A> AUTOMATIC MODE**

Format, write, read, and verify on tracks 00, 43, 44, and 76 on both sides of the currently selected drive.

As a note, if a "burn in" type of test is needed the best option would be to use the <C> command on Track 76 side 1 of the drive to be tested.

## STATUS DISPLAY

**TRACK**

Displays the track number currently being tested.

**WRITE RETRY**

Displays the number of FAILED write attempts.

**READ RETRY**

Displays the number of FAILED read attempts.

**SEEK ERROR**

Displays the number of seek errors reported by the FDC chip. A seek error is produced whenever the FDC chip can not read the correct track number from the ID field on the selected track.

**HARD ERROR**

Displays the number of errors that, had they been detected by TRSDOS, would have produced an error message. TRSDOS will normally try up to 16 times to complete a command. Therefore, hard errors are errors that occurred repeatedly for more than 16 times.

Soft errors are errors which occur only occasionally. A soft error will almost always be recovered by TRSDOS without any indication to the user. A small number of RETRY errors may indicate dirt (smoke, dust, hair) on the head or diskette. Larger numbers of RETRY errors, with no hard errors, may indicate diskette failure. Be sure and use a KNOWN GOOD, BULK ERASED diskette. Large number of RETRY errors, and possibly hard errors, may indicate a completely worn out disk. Try a KNOWN GOOD, BULK ERASED diskette before condemning the drive.

**TRACK TOTAL**

Displays the number of tracks tested.

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**TRS-80®**

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**TDCTL**

**8-INCH THINLINE™ DRIVE ALIGNMENT PROGRAM**

**CHAPTER 11**

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**Radio Shack®**

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**TDCTL - DRIVE CONTROLLER FOR TANDON 8-INCH THINLINE™ DRIVES****GENERAL DESCRIPTION**

TDCTL is designed to provide the control signals necessary to align and troubleshoot the TANDON Thinline™ 8-inch floppy drives currently used in the TRS-80 Model 12 or 16 Microcomputers. The program is completely menu driven with the flexibility to easily jump from one drive to another.

**FEATURES**

Instructions, test points, oscilloscope settings, and specifications listed with each test.  
Available tests: speed, carriage movement, head radial, head azimuth, index timing, head amplitude, raw data and track zero.  
Elastic stepping or single stepping.  
Program flow arranged to minimize changing of test probes and diskettes.  
Generous prompting to prevent errors and accidental damage of expensive alignment diskettes.

**EQUIPMENT REQUIRED**

TRS-80 Model 12 or 16  
35 MHz or better oscilloscope  
2 scope probes  
Cable for external sync to scope  
8-inch double sided alignment diskette  
8-inch double sided blank diskette  
Feeler gauges, Allen wrenches, and other tools  
TDCTL DIAGNOSTIC PROGRAM

## LOADING TDCTL

1. Power up the Expansion Bay (if available)
2. Power up the computer.
3. When "INSERT DISKETTE" message appears, insert the diskette containing the TDCTL program, and close the door.
4. When "TRSDOS READY" appears, type: TDCTL <ENTER>

## OPERATING TDCTL

TDCTL is completely menu driven and contains no "hidden" commands. This means that you will not need to refer to the operations manual once you become familiar with the program!

All keyboard entries by the technician are made with CAPITAL letters. This is most easily done by typing the <CAPS> key so that the red light remains on. All keyboard entries are now always capital letters without need for the <SHIFT> key.

## THE DISPLAY

When TDCTL finishes loading the menu page will appear on the screen. This menu will remain on screen at all times, even during testing.

The Menu consists of two parts: the status line and the selection listings. The status line is just above the selection listings, marked with three vertical lines at either end. The status line gives information on the current track, the selected drive number, and which side is presently in use. This information is updated as necessary to provide current status of the drive under test.

The selection listings are arranged in two columns. The left column is the actual test modules arranged in a logical alignment order to maximize efficiency and minimize time wasted changing probes and diskettes.

The right column contains the control functions. Each function is explained separately later.

While a test is running two additional sections appear on the screen. These sections provide pertinent information about each test and each drive.

Just below the menus appears the TEST SETUP INFORMATION. This section gives the necessary test points and equipment settings to perform the desired test on the selected drive.

Near the bottom of the screen, just below the test setup information, appears the SPECIFICATIONS LIST. This section details the proper specifications for the drive under test for the selected module.

#### SELECTING THE DRIVE

When TDCTL finishes loading the menu page will appear with a flashing cursor under the left hand column. At this time select a drive by typing: <D>

**SELECT DRIVE NUMBER (0-3)** will now appear in highlights. Select the appropriate drive number by typing that number.

After a drive has been properly selected the highlighted prompt will disappear.

#### THE MENUS

The two-part menu remains on screen while TDCTL is running. The left hand column contains the TESTS while the right hand column contains the CONTROL FUNCTIONS.

The tests are arranged in a logical alignment order so that probe and diskette changes are kept to a minimum. Each test can be individually selected by typing the appropriate number. As well, the test sequence can be stepped through in forward or reverse order, or an individual test can be repeated by using the control functions.

#### CONTROL FUNCTIONS

##### <BK> STOP TEST, DISPLAY MENU

<BK> is used to signify the BREAK key. When <BREAK> is pressed any test currently running is terminated, test information on the screen is erased, and the menus are displayed.

##### <Q> QUIT, GO TO TRSDOS

<Q> exits all tests and terminates the program. You are asked to reinsert the system diskette and type <ENTER>. TRSDOS then reboots.

**<R> RESTORE TO TRACK 00 ELASTIC**

If <R> is typed during any test the head is stepped out to Track 00 and then back to the selected track. This is most useful during head radial alignment.

**<S> STEP TO TRACK 76 ELASTIC**

If <S> is typed during a test the head is stepped in to Track 76 and then back to the selected track. This is most useful during head radial alignment.

**<N> NEXT MODULE**

Typing <N> terminates any current test and goes to the next test in sequence.

**<P> PREVIOUS MODULE**

Typing <P> terminates any current test and goes to the previous test in sequence.

**<T> TOGGLE SIDE SELECT**

<T> is used to toggle the side select option. Pressing <T> will select the side not presently in use. If the drive is presently using side 0, <T> will switch to side 1. If the drive is presently using side 1, <T> will select side 0. The presently selected side is indicated in the status line above the menu.

**<D> DRIVE SELECT**

Typing <D> puts the program into the drive select sequence already detailed.

**<O> SINGLE STEP OUT**

Typing <O> steps the head one track out toward track 00.

**<I> SINGLE STEP IN**

Typing <I> steps the head one track in toward track 76.

**<C> COMMAND REPEAT**

Typing <C> will restart any test.

**TEST DESCRIPTION**

FOR NORMAL DRIVE ALIGNMENT, ALL TESTS SHOULD BE EXECUTED IN ORDER, 1-8. MODULE 1 ( SPEED DEVIATION ) SHOULD NEVER BE BYPASSED.

The TESTS menu appears on the left side of the screen. Tests can be selected by typing the number of the desired test, or using <N>, <P>, or <C> keys if a test is already selected.

Each test module issues all necessary commands to the drive under test to accomplish the desired procedure. As well, each module provides prompts for inputs (if required), test equipment setup, test points, and specifications.

**<1> SPEED DEVIATION**

This test gives a visual readout of the speed of the disk drive motor.

After inserting a blank diskette and closing the door, the specifications and adjustment procedure appear on the screen and the actual speed of the drive under test appears shortly thereafter.

If the stated speed is grossly out of specification, but the drive appears to function normally, check the CPU wait state jumpers before assuming a faulty drive mechanism.

**<2> CARRIAGE MOVEMENT CHECK**

This test provides continuous movement of the head carriage assembly. The full movement of the carriage can be specified, or a narrow range of tracks can be selected.

After selecting this test the range select option appears. You are then asked to input a specific lower track limit. This must be a two digit decimal number in the range of 00 to 76. At this point, typing <ENTER> defaults to the full range of tracks 00 to 76 and the test begins. If you enter a specific track number you will then be asked to enter an upper track in the range of 00 to 76. <ENTER> defaults to track 76.

The carriage will continuously step between the two specified tracks so that the technician can check for obstructions, binding, etc.

**<3> HEAD RADIAL**

This test provides a means for checking proper head alignment.

After selecting this test you are asked to insert an ALIGNMENT DISKETTE. You MUST use a double-sided alignment diskette. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

After properly adjusting the head radial step the head to Track 00 and back using the <R>estore function. Step to Track 76 and back using the <S>tep track 76 function. Check for proper alignment after each step function. Repeat as necessary until the head radial alignment remains within specification and no longer changes after each step function.

Using the <T> option, select the other side of the diskette and repeat the above test. Both heads must remain within specifications.

**<4> HEAD AZIMUTH**

This test provides a means for checking the head azimuth.

After selecting this test you are asked to insert an ALIGNMENT DISKETTE. You MUST use a double-sided alignment diskette. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

Using the <T> option, select the other side of the diskette and repeat the above test. Check to make sure the readings of both heads meet or exceed the specifications. Repair as necessary to make the drive pass the test.

**<5> INDEX TIMING**

This test provides a means for checking proper adjustment of the Index Sector Assembly.

After selecting this test you are asked to insert an ALIGNMENT DISKETTE. You MUST use a double-sided alignment diskette. When you have the diskette inserted and the door closed, press <ENTER>. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

After properly adjusting the Index Sector Assembly remove and reinsert the Alignment Diskette several times, checking each time to be sure that the adjustment remains within specifications.

Using the <T> option, select the other side of the diskette and repeat the above test. Both heads must remain within specifications.

**<6> HEAD AMPLITUDE**

```
*****
*                               *
*           W A R N I N G ! !
*                               *
*   THIS TEST WILL DESTROY ANY DATA      *
*   ALREADY PRESENT ON THE TEST DISK      *
*   USE ONLY A BULK ERASED DISKETTE       *
*   TO PERFORM THIS TEST PROCEDURE        *
*                               *
*****
```

This test provides a means of checking head amplitude.

After selecting this test you are asked to insert a BLANK, DOUBLE-SIDED DISKETTE. Use only a fresh diskette that has been bulk erased. With the diskette inserted and the door closed, press <ENTER>. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

Check to make sure the amplitude from the drive under test meets or exceeds the given specifications. Should the drive fail this test, repeat the test (using the <C> option) with a NEW test diskette to eliminate the diskette as a possible cause.

Using the <T> option, select the other side of the diskette and repeat the above test. Both heads must remain within specifications.

Clean the heads, repair the drive PCB, or replace the heads as necessary to make the drive pass the test.

**<7> RAW DATA**

```
*****  
*  
*      W A R N I N G ! !  
*  
*      THIS TEST WILL DESTROY ANY DATA  
*      ALREADY PRESENT ON THE TEST DISK  
*      USE ONLY A BULK ERASED DISKETTE  
*      TO PERFORM THIS TEST PROCEDURE  
*  
*****
```

This test provides a means of checking for excessive electrical and mechanical jitter in the drive under test.

After selecting this test you are asked to insert a BLANK DOUBLE-SIDED DISKETTE. Use only a fresh diskette that has been bulk erased. With the diskette inserted and the door closed, press <ENTER>. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

Check to make sure that the pulse symmetry and jitter on both the second and third pulse does not exceed the maximum allowable limits. Check for worn belts, foreign material, or dirt causing excessive mechanical jitter. Do not dismiss the diskette as a possible cause of electrical jitter. Repair the drive PCB or suspect head magnetization in the case of excessive second pulse asymmetry.

Using the <T> option, select the other side of the diskette and repeat the above test. Both heads must remain within specifications.

**<8> TRACK 00 FLAG**

This test provides a means of producing control signals necessary to align the Track 00 flag.

After selecting this test, perform the necessary measurements and adjustments to make the drive under test meet or exceed specifications.

The head assembly can be stepped between the two necessary tracks by using the step <O>ut and step <I>n functions.

APPENDIX A: TDCTL PROGRAM USERS MANUAL

Disk drive specifications, test points, and jumpers

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## TANDON TM848-2

The TANDON TM848-2 is a double-sided drive that will be found in the TRS-80 Model 16 and 12 Microcomputers. Since the TANDON TM848-2 is a double-sided drive BOTH heads must exceed the following specifications:

DISK ROTATION SPEED.....	360 RPM +/- 4
HEAD AMPLITUDE.....	> 300 mv p.p.
INDEX PULSE WIDTH.....	1.5 msec +/- .5 msec.
INDEX TO BURST TIMING.....	200 usec +/- 100 usec
HEAD RADIAL ALIGNMENT.....	small / large >75%
RAW DATA JITTER.....	< 200 nsec on 3rd pulse < 250 nsec on 2nd pulse

Presently, TANDON is using two revisions of one style of PCB. Both boards have the same test points:

HEAD AMPLIFIER OUTPUT.....	TP 2,3
INDEX PULSE(single sided)....	end of R33 closest to DS2
INDEX PULSE(double sided)....	TP 12
RAW DATA OUTPUT.....	TP 9
TRACK 0 FLAG.....	TP 10
CIRCUIT GROUND.....	TP 1

The TANDON TM848-2 uses a termination resistor pack to properly terminate the signals. The resistor pack must be installed in the drive furthest from the FDC board. There must be ONE internal drive and ONE external drive terminated if the Expansion Bay is used. The resistor pack may have several pins lifted out of the socket or cut off of the IC.

## INTERNAL DRIVE FOR MODEL 16

Pins 1,2,4,6,7,8,9,10,11,13,15,16.....	Lifted or cut
Pins 3,5,12,14.....	Inserted

## EXTERNAL (BAY) DRIVE USED WITH MODEL 16

Pins 3,14.....	lifted or cut
Pins 1,2,4,5,6,7,8,9,10,11,12,13,15,16.....	Inserted

## INTERNAL DRIVE FOR MODEL 12 AND MODEL 16B

## EXTERNAL (BAY) DRIVE USED WITH MODEL 12 AND MODEL 16B

All pins .....	inserted
----------------	----------

TANDON uses the following push on jumpers and DIP shunts to properly configure the drive.

An appropriate jumper at DSx, just above the stepper motor.

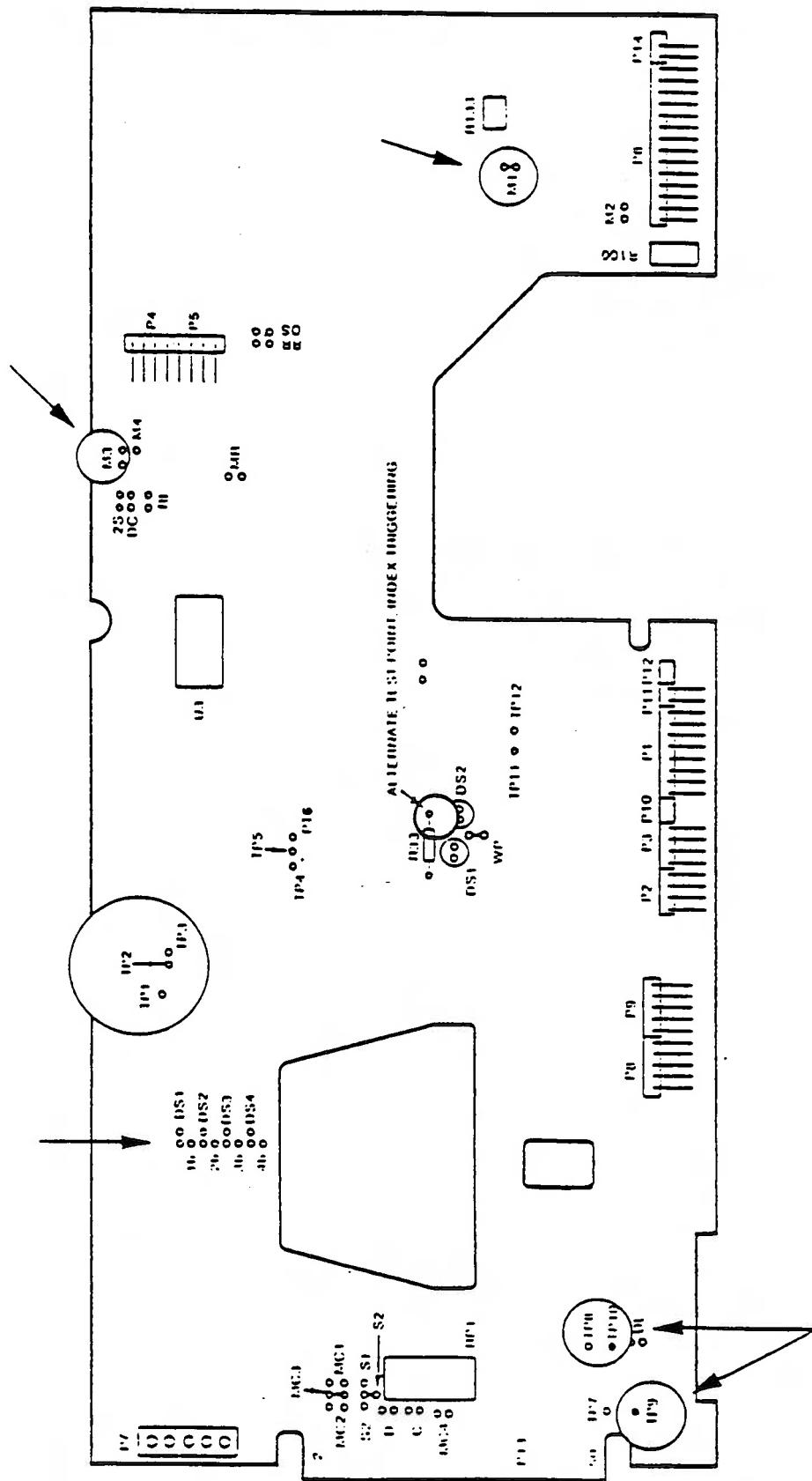
On DIP shunt U3 (may also be labeled HLL) the connection between pins 2 and 15 must be broken.

Push on jumper at M1 and M3 if possible. Early revision PCBs may have these points already wired.

There must be NO M2 JUMPER!!

APPENDIX B: TDCTL PROGRAM USERS MANUAL

Component and Test Point Locations



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APPENDIX C: TDCTL PROGRAM USERS MANUAL

Common waveforms during disk drive alignment

## NOTE:

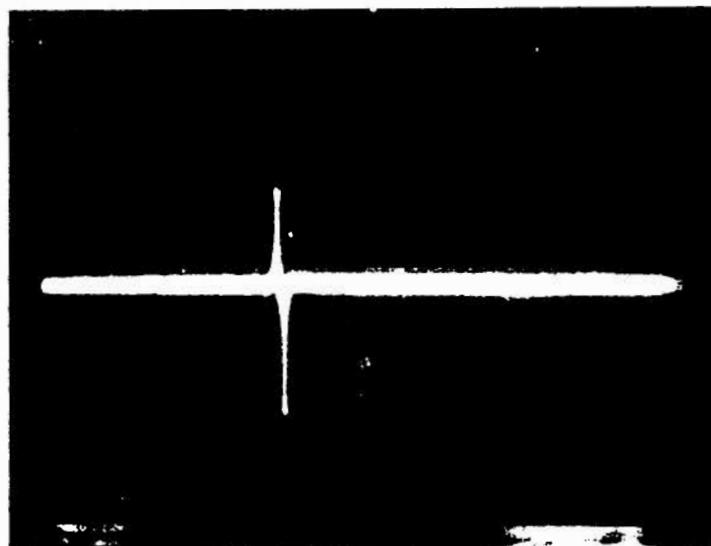
There are two different alignment diskettes available, SHUGART and DYMEK. While each one has all signals necessary to complete an alignment, the two diskettes differ slightly in the signal produced.

This is most noticeable during the Index Sector Timing tests. While the DYMEK diskette produces a signal burst to be measured, the SHUGART diskette produces only one cycle to be measured.

If the difference in the two diskettes will be apparent during a test two waveforms will be shown, one for each diskette.

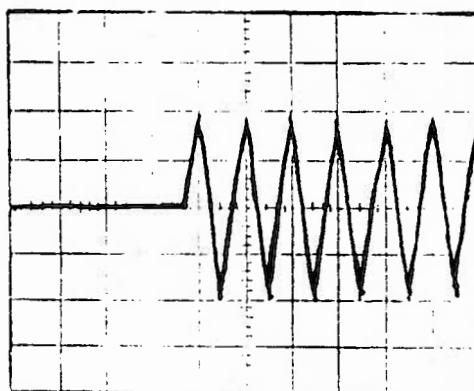
The following oscilloscope photographs and waveform drawings are taken from properly aligned drives, and should be considered "typical". They are "text book" cases and do not show extraneous noise or minor differences from unit to unit. While your readings may differ slightly in waveform or amplitude, they should still remain reasonably close to the following illustrations.

## INDEX SECTOR TIMING WAVEFORMS



50  $\mu$ sec/div horizontal  
500 mV/div vertical

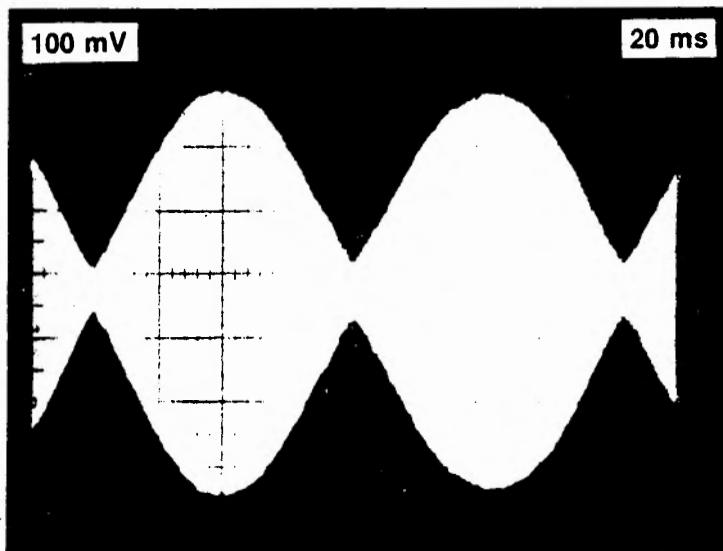
SHUGART ALIGNMENT DISKETTE



50  $\mu$ sec/div horizontal  
500 mV/div vertical

DYMEK ALIGNMENT DISKETTE

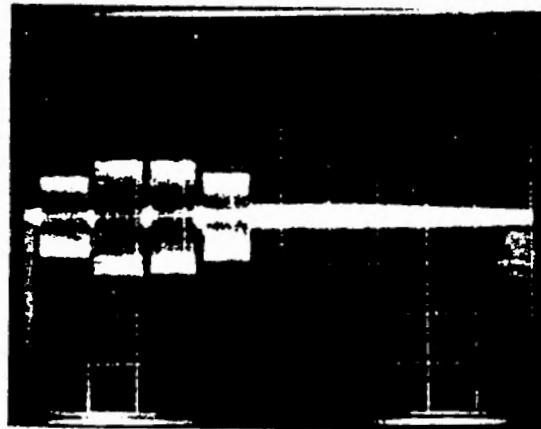
## HEAD RADIAL ALIGNMENT "CAT'S EYES" PATTERN



20 msec/div horizontal  
100 mV/div vertical

PATTERN AVAILABLE ON BOTH SHUGART AND DYMEK DISKETTES

HEAD AZIMUTH PATTERN



10 msec/div horizontal  
100 mV/div vertical

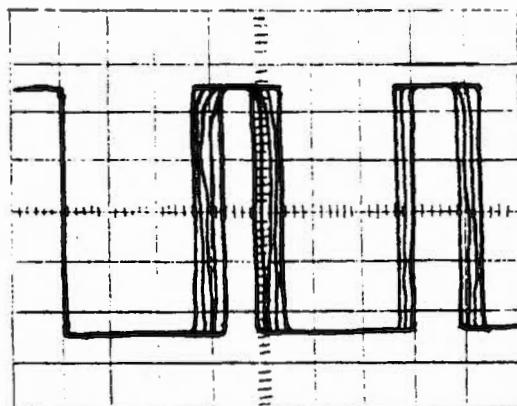
PATTERN AVAILABLE ON BOTH SHUGART AND DYMEX DISKETTES

---

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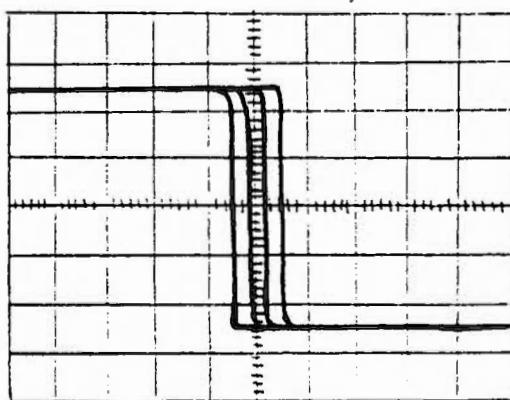
---

## RAW DATA ADJUSTMENT -- JITTER AND SYMMETRY



1  $\mu$ sec/div horizontal  
1 V/div vertical

NORMAL SWEEP



1  $\mu$ sec/div horizontal  
1 V/div vertical

EXPANDED SWEEP

---

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**TRS-80®**

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TDC

**8-INCH DRIVE ALIGNMENT PROGRAM**

**CHAPTER 12**

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**TDC - DRIVE CONTROLLER FOR ALL TRS-80 MODEL II 8-INCH DRIVES****GENERAL DESCRIPTION**

---

"TDC" is designed to provide the control signals necessary to align and troubleshoot all four types of 8-inch floppy drives currently used in the TRS-80 Model II Microcomputer. The program is completely menu driven with the flexibility to easily jump from one type of drive to another.

**FEATURES**

---

All four drive types easily selectable from one program.  
Instructions, test points, oscilloscope settings, and specifications listed with each test.  
Available tests: speed, carriage movement, head load timing, head radial, head azimuth, index timing, head amplitude, raw data and track zero.  
Elastic stepping or single stepping.  
Program flow arranged to minimize changing of test probes and diskettes.  
Generous prompting to prevent errors and accidental damage of expensive alignment diskettes.

**EQUIPMENT REQUIRED**

---

TRS-80 Model II  
35 MHz or better oscilloscope  
2 scope probes  
Cable for external sync to scope  
8-inch alignment diskette  
8-inch blank diskette  
Feeler gauges, Allen wrenches, and other tools  
"TDC" DIAGNOSTIC PROGRAM

## LOADING "TDC"

- 
1. Power up the Expansion Bay.
  2. Power up the computer.
  3. When "INSERT DISKETTE" message appears, insert the diskette containing the "TDC" program, and close the door.
  4. When "TRSDOS READY" appears, type: TDC <ENTER>

## OPERATING "TDC"

---

"TDC" is completely menu driven and contains no "hidden" commands. This means that you will not need to refer to the operations manual once you become familiar with the program!

All keyboard entries by the technician are made with CAPITAL letters. This is most easily done by typing the <CAPS> key so that the red light remains on. All keyboard entries are now always capital letters without need for the <SHIFT> key.

## THE DISPLAY

---

When "TDC" finishes loading the menu page will appear on the screen. This menu will remain on screen at all times, even during testing.

The Menu consists of two parts: the status line and the selection listings. The status line is just above the selection listings, marked with three vertical lines at either end. The status line gives information on the current track, the selected drive number, the status of the head load switch, and the selected drive type. This information is updated as necessary to provide current status of the drive under test.

The selection listings are arranged in two columns. The left column is the actual test modules arranged in a logical alignment order to maximize efficiency and minimize time wasted changing probes and diskettes.

The right column contains the control functions. Each function is explained separately later.

While a test is running two additional sections appear on the screen. These sections provide pertinent information about each test and each drive.

Just below the menus appears the TEST SETUP INFORMATION. This section gives the necessary test points and equipment settings to perform the desired test on the selected drive.

Near the bottom of the screen, just below the test setup information, appears the SPECIFICATIONS LIST. This section details the proper specifications for the drive under test for the selected module.

#### SELECTING DRIVE TYPE

---

When "TDC" finishes loading the menu page will appear with a flashing cursor under the left hand column. At this time select a drive by typing: <D>

"SELECT DRIVE TYPE <0-3>" will appear in highlights just below the left column. Select the appropriate type of drive you wish to check by typing the corresponding number.

Notice that the currently logged drive type is specified on the right end of the top row of the menu. This area changes as you select a new drive.

"SELECT DRIVE NUMBER (0-3)" will now appear in highlights. Select the appropriate drive number by typing that number.

After a drive has been properly selected the highlighted prompts disappear.

#### THE MENUS

---

The two-part menu remains on screen while "TDC" is running. The left hand column contains the TESTS while the right hand column contains the CONTROL FUNCTIONS.

The tests are arranged in a logical alignment order so that probe and diskette changes are kept to a minimum. Each test can be individually selected by typing the appropriate number. As well, the test sequence can be stepped through in forward or reverse order, or an individual test can be repeated by using the control functions.

#### CONTROL FUNCTIONS

---

<BK> STOP TEST, DISPLAY MENU

<BK> is used to signify the BREAK key. When <BREAK> is pressed any test currently running is terminated, test information on the screen is erased, and the menus are displayed.

<Q> QUIT, GO TO TRSDOS

<Q> exits all tests and terminates the program. You are asked to reinsert the system diskette and type <ENTER>. TRSDOS then reboots.

<R> RESTORE TO TRACK 00 ELASTIC

If <R> is typed during any test the head is stepped out to Track 00 and then back to the selected track. This is most useful during head radial alignment.

<S> STEP TO TRACK 76 ELASTIC

If <S> is typed during a test the head is stepped in to Track 76 and then back to the selected track. This is most useful during head radial alignment.

<N> NEXT MODULE

Typing <N> terminates any current test and goes to the next test in sequence.

<P> PREVIOUS MODULE

Typing <P> terminates any current test and goes to the previous test in sequence.

<H> HEAD LOAD SWITCH

<H> is used to alternately LOAD and UNLOAD the head load bail. The top line of the menu contains a "HEAD LOADED" message which changes to indicate the current state of the head load switch. The <REPEAT> key may be used with the <H> key to give an alternating head load cycle necessary for the Head Load Timing tests.

<D> DRIVE SELECT

Typing <D> puts the program into the drive select sequence already detailed.

<O> SINGLE STEP OUT

Typing <O> steps the head one track out toward track 00.

---

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**<I> SINGLE STEP IN**

Typing <I> steps the head one track in toward track 76.

**<C> COMMAND REPEAT**

Typing <C> will restart any test.

**TEST DESCRIPTION**  
-----

FOR NORMAL DRIVE ALIGNMENT, ALL TESTS SHOULD BE EXECUTED IN ORDER, 1-9.  
MODULE 1 ( SPEED DEVIATION ) SHOULD NEVER BE BYPASSED.

NOTE: IF YOU ARE ASKED TO INSERT A DISKETTE DURING ANY TEST, YOU MUST  
TYPE <ENTER> TO PROCEED WITH THE TEST.

The TESTS menu appears on the left side of the screen. Tests can be selected by typing the number of the desired test, or using <N>, <P>, or <C> keys if a test is already selected.

Each test module issues all necessary commands to the drive under test to accomplish the desired procedure. As well, each module provides prompts for inputs (if required), test equipment setup, test points, and specifications.

**<1> SPEED DEVIATION**

This test gives a visual readout of the speed of the disk drive motor.

After inserting a blank diskette and closing the door, the specifications appear on the screen and the actual speed of the drive under test appears shortly thereafter.

If the stated speed is grossly out of specification, but the drive appears to function normally, check the CPU wait state jumpers before assuming a faulty drive mechanism.

**<2> CARRIAGE MOVEMENT CHECK**

This test provides continuous movement of the head carriage assembly. The full movement of the carriage can be specified, or a narrow range of tracks can be selected.

After selecting this test the range select option appears. You are then asked to input a specific lower track limit. This must be a two digit decimal number in the range of 00 to 76. Typing <ENTER> defaults to track 00. You are then asked to input an upper track limit in the range of 00 to 76. <ENTER> at this point defaults to track 76.

The carriage will start to step between the two specified tracks so that the technician can check for obstructions, binding, etc.

Note that a diskette does NOT have to be installed for this test to function. No diskette means the head carriage is not hidden from view during testing.

**<3> HEAD LOAD TIMING**

This test provides a means for checking proper timing of the head load bail mechanism.

After selecting this test you are asked to insert an ALIGNMENT DISKETTE. When you have the diskette inserted and the door closed, press <ENTER>. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

The head can be alternately loaded or unloaded by use of the <H> key. Holding both <H> and <REPEAT> will produce an alternating head load which will produce a more usable oscilloscope display.

**<4> HEAD RADIAL**

This test provides a means for checking proper head alignment.

After selecting this test you are asked to insert an ALIGNMENT DISKETTE. When you have the diskette inserted and the door closed, press <ENTER>. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

After properly adjusting the head radial step the head to Track 00 and back using the <R>estore function. Step to Track 76 and back using the <S>tep track 76 function. Check for proper alignment after each step function. Repeat as necessary until the head radial alignment remains within specification and no longer changes after each step function.

**<5> HEAD AZIMUTH**

This test provides a means for checking the head azimuth.

After selecting this test you are asked to insert an ALIGNMENT DISKETTE. When you have the diskette inserted and the door closed, press <ENTER>. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

Check to make sure the readings meet or exceed the specifications. Repair as necessary to make the drive pass the test.

**<6> INDEX TIMING**

This test provides a means for checking proper adjustment of the Index Sector Assembly.

After selecting this test you are asked to insert an ALIGNMENT DISKETTE. When you have the diskette inserted and the door closed, press <ENTER>. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

After properly adjusting the Index Sector Assembly remove and reinsert the Alignment Diskette several times, checking each time to be sure that the adjustment remains within specifications.

**<7> HEAD AMPLITUDE**

```
*****  
*          *  
*      W A R N I N G ! !      *  
*          *  
*      THIS TEST WILL DESTROY ANY DATA      *  
*      ALREADY PRESENT ON THE TEST DISK      *  
*      USE ONLY A BULK ERASED DISKETTE      *  
*      TO PERFORM THIS TEST PROCEDURE      *  
*          *  
*****
```

This test provides a means of checking head amplitude.

After selecting this test you are asked to insert a BLANK DISKETTE. Use only a fresh diskette that has been bulk erased. With the diskette inserted and the door closed, press <ENTER>. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

Check to make sure the amplitude from the drive under test meets or exceeds the given specifications. Should the drive fail this test, repeat the test (using the <C> option) with a NEW test diskette to eliminate the diskette as a possible cause.

Replace the head load pad, clean the head, repair the drive PCB, or replace the head as necessary to make the drive pass the test.

#### <8> RAW DATA

```
*****
*          W A R N I N G ! !
*
*      THIS TEST WILL DESTROY ANY DATA
*      ALREADY PRESENT ON THE TEST DISK
*      USE ONLY A BULK ERASED DISKETTE
*      TO PERFORM THIS TEST PROCEDURE
*
*****
```

This test provides a means of checking for excessive electrical and mechanical jitter in the drive under test.

After selecting this test you are asked to insert a BLANK DISKETTE. Use only a fresh diskette that has been bulk erased. With the disk-ette inserted and the door closed, press <ENTER>. The proper test points and specifications for the selected drive will be displayed at the bottom of the screen.

Check to make sure that the pulse symmetry and jitter on both the second and third pulse does not exceed the maximum allowable limits. Check for worn belts, foreign material, or dirt causing excessive mechanical jitter. Adjust the required potentiometer to reduce remaining electrical jitter. Do not dismiss the diskette as a possible cause of electrical jitter. Repair the drive PCB or suspect head magnetization in the case of excessive second pulse asymmetry.

#### <9> TRACK 00 FLAG

This test provides a means of producing control signals necessary to align the Track 00 flag.

After selecting this test, perform the necessary measurements and adjustments to make the drive under test meet or exceed specifications.

The head can be stepped between the two necessary tracks by using the step <O>ut and step <I>n functions.

## A) SHUGART SA800

The Shugart SA800 drive will be found as Drive Ø in the TRS-8Ø Model II Microcomputer. When properly aligned and functioning, the drive should exceed the following specifications:

DISK ROTATION SPEED.....	36Ø RPM +/- 8
HEAD AMPLITUDE.....	>11Ø mv p.p.
INDEX PULSE WIDTH.....	1.7 msec +/- .5 msec
INDEX TO BURST TIMING.....	2ØØ usec +/- 1ØØ usec
HEAD LOAD TIMING.....	< 35 msec to 5Ø% ampl.
HEAD RADIAL ALIGNMENT.....	small / large >7Ø%
RAW DATA JITTER.....	< 2ØØ nsec on 3rd pulse < 25Ø nsec on 2nd pulse

Although the SHUGART SA800 drives presently use one of four different PC boards, all test point references remain the same. These test points are:

HEAD AMPLIFIER OUTPUT.....	TP 1,2
INDEX PULSE.....	TP 12
HEAD LOAD SIGNAL.....	TP 11
RAW DATA OUTPUT.....	TP 16
TRACK ØØ FLAG.....	TP 26
CIRCUIT GROUND.....	TP 5,6,7

To function correctly as drive Ø in a Model II system it must be properly terminated. This is done by a set of push-on jumpers and wire wrap connections on the board. The wire wrap is needed only with the old style FDC board (AXX-Ø5Ø5). A special wire jumper, part number AW-27Ø6, is available from National Parts. This jumper can be used ONLY on discrete and early LSI boards. The late LSI boards must be manually wire wrapped. It is important to check ALL boards from National parts, and any new units in for repairs to see that they have the proper jumpers installed.

Push-on connectors should be present on pins labeled;

A, B, C, DC, DS, DS1, T1, T2, Z, 8ØØ  
L (present only on discrete boards) (jumper vertical)

Wirewrap jumpers:

FROM	TO
J1-4	T6 ( on row farthest from connector )
J1-6	T5 ( " " " " " )
J1-8	T4 ( " " " " " )
J1-1Ø	T3 ( " " " " " )

## B) CONTROL DATA CORPORATION 9409-B

The CDC 9404-B will be found in the TRS-80 Model II Microcomputer Expansion Bay. When properly aligned and functioning, the drive should exceed the following specifications:

DISK ROTATION SPEED.....	360 RPM +/- 8
HEAD AMPLITUDE.....	> 200 mv p.p.
INDEX TO BURST TIMING.....	450 usec +/- 100 usec
HEAD LOAD TIMING.....	< 60 msec TO 50% ampl.
HEAD RADIAL ALIGNMENT.....	small / large >80%
RAW DATA JITTER.....	< 200 nsec on 3rd pulse < 250 nsec on 2nd pulse

CDC presently uses two styles of PCB, discrete and LSI. The test points differ between the two styles. Some test points do not have pins, and will require a wire to be soldered in to attach the probe.

DISCRETE	LSI
HEAD AMPLIFIER OUTPUT.....	TP 3,4
INDEX PULSE.....	TP 14
HEAD LOAD SIGNAL.....	J5-2
RAW DATA OUTPUT.....	TP 8
TRACK 00 FLAG.....	J3-2
CIRCUIT GROUND.....	TP 15
	C18 side farthest from the screw

A socket is provided for a modified termination resistor pack on each board. Only Drive 1 should be terminated.

DISCRETE BOARD..... Remove pin 14 from resistor pack  
 LSI BOARD..... Remove pin 9 from resistor pack

The LSI boards have an 8-pin socket for DRIVE SELECT jumpers. CDC numbers their devices 1-4, and TRS-80 convention is 0-3. To select Drive 1, short the jumper W2. Short only the jumper for the desired drive number.

The discrete board has one or two DIP packages switches installed. The 8-position S1 (under the termination socket) is Drive Select.

POS 1,2,3,4..... Drive Select - use ONLY one!  
 POS 5..... READY - always ON  
 POS 6,7,8..... spares - always OFF

The 7-position S3 may replace U20. If there is no IC in U20 then you will find either S3 or nothing at all. If there is nothing at all you must install a jumper wire.

POS 1,2,3,5,6,7..... All OFF  
 POS 4..... Switch ON, or jumper installed

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## C) TPI 8-INCH DRIVE

The TPI 8-inch drive can be found as any drive, 0 thru 3. All specifications remain the same, only drive configurations change. When properly aligned and functioning, the drive should exceed the following specifications:

DISK ROTATION SPEED.....	360 RPM +/- 8
HEAD AMPLITUDE.....	> 200 mv p.p.
INDEX TO BURST TIMING.....	200 usec +/- 100 usec
HEAD LOAD TIMING.....	< 35 msec TO 50% ampl.
HEAD RADIAL ALIGNMENT.....	small / large >80%
RAW DATA JITTER.....	< 200 nsec on 3rd pulse
	< 250 nsec on 2nd pulse

TPI is presently using one PCB. The test points are:

HEAD AMPLIFIER OUTPUT.....	TP 1,2
INDEX PULSE.....	TP 3
HEAD LOAD SIGNAL.....	TP 6
RAW DATA OUTPUT.....	TP 7
TRACK 00 FLAG.....	TP 5

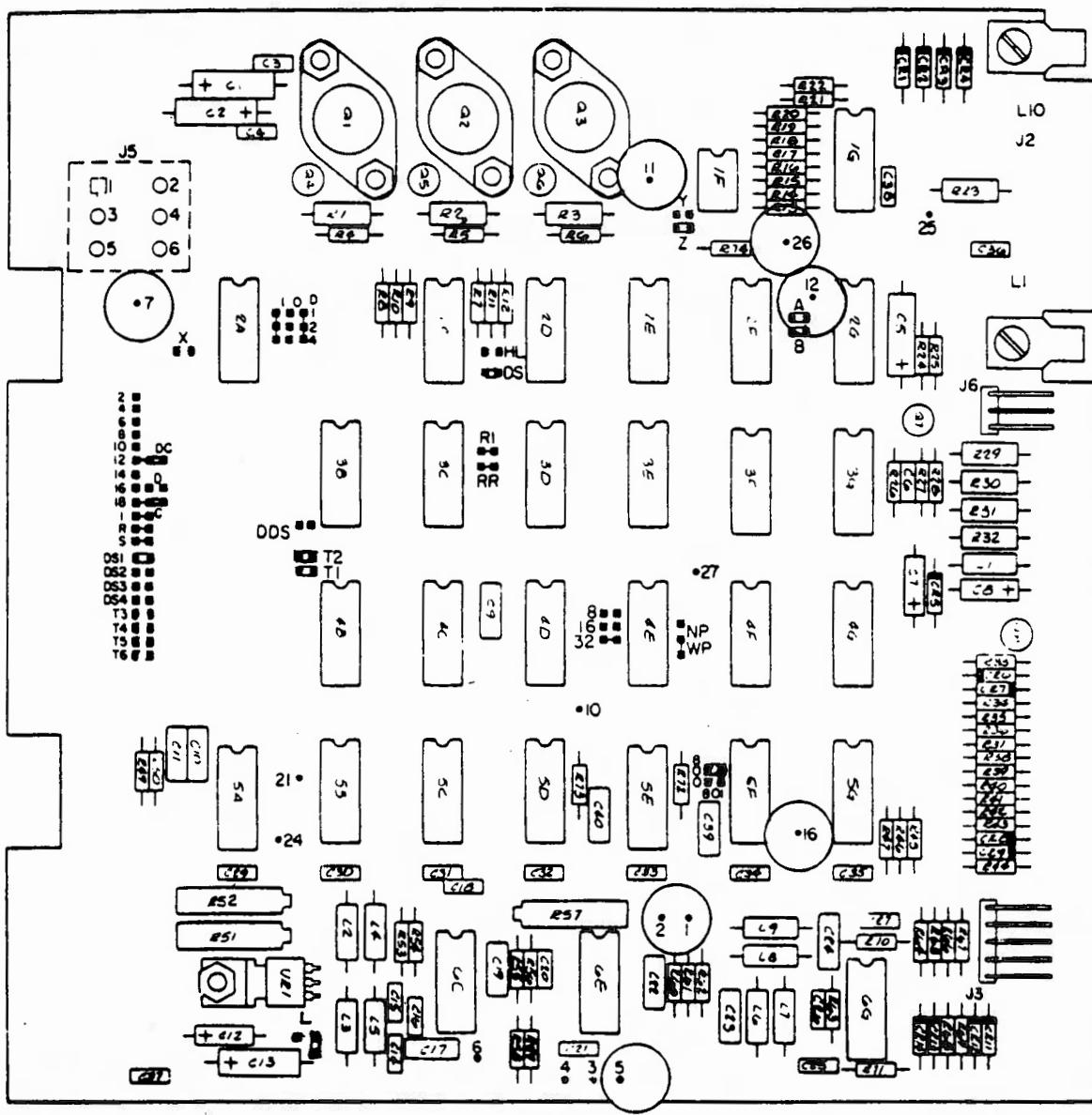
Like the Shugart, TPI uses push on jumpers to properly configure and terminate the drive. The following pins should have jumpers:

## TERMINATION

Drive 0	T1, T8
Drive 1	T3, T4, T5, T6, T7, T8

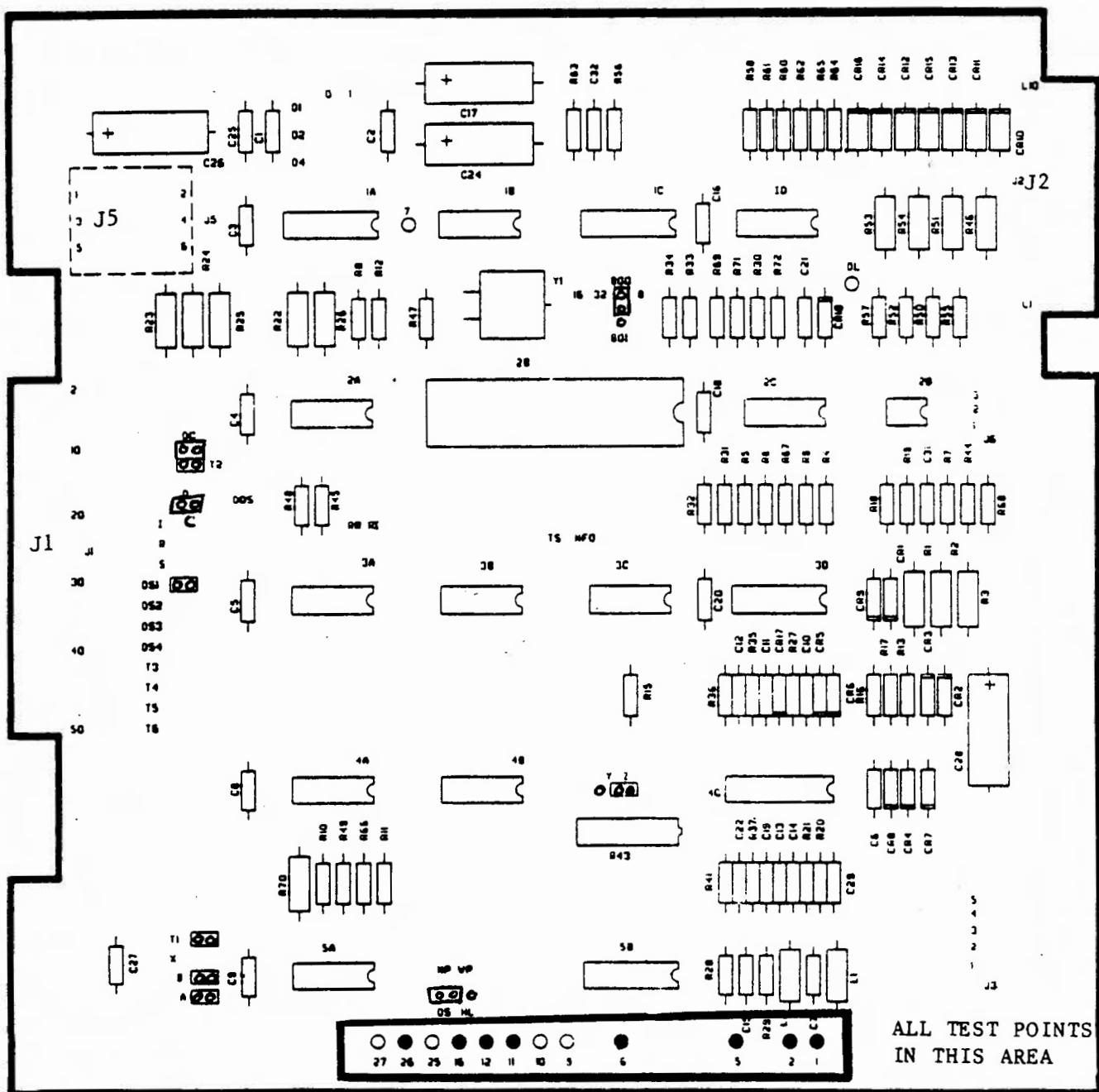
## DRIVE CONFIGURATION ON ALL DRIVES

E1-E2, E3-E4, and appropriate jumper at DSx to select the drive  
(boards are labeled DS1 to DS4)

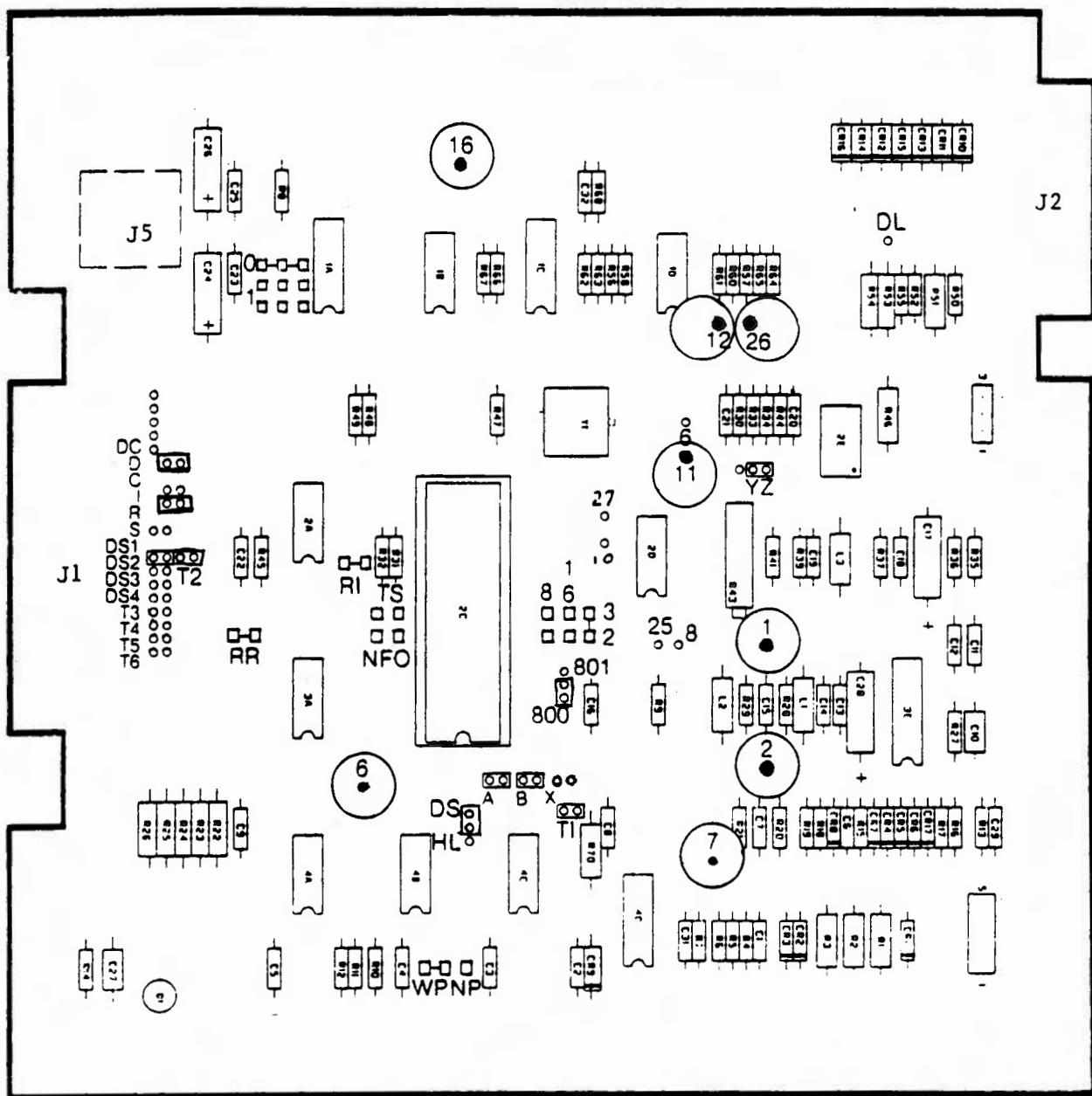


**SHUGART SA800  
Discrete PCB  
Test Point Locations**

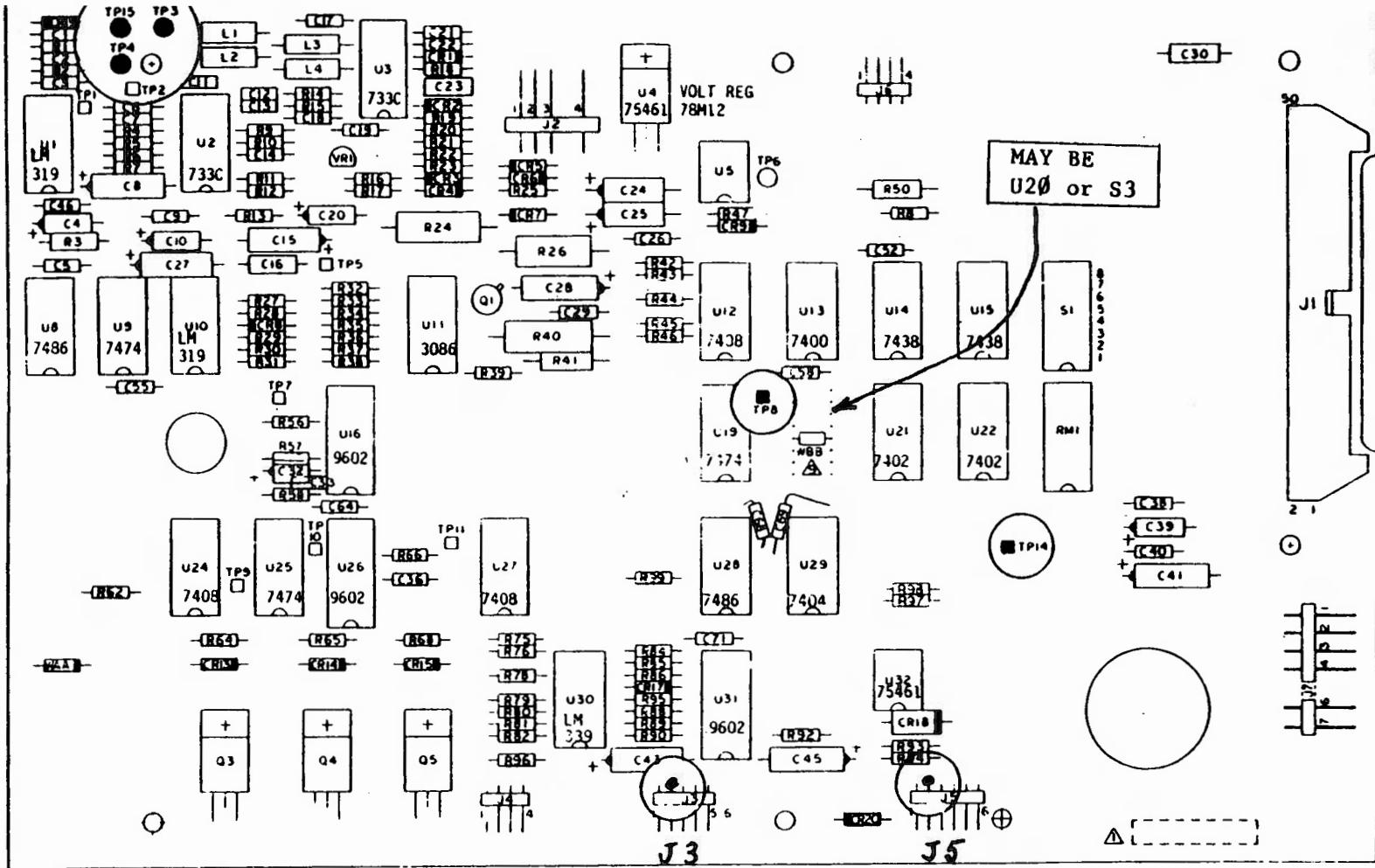
(Old style PCB shown.)  
(New style PCB Test Points are at same locations.)



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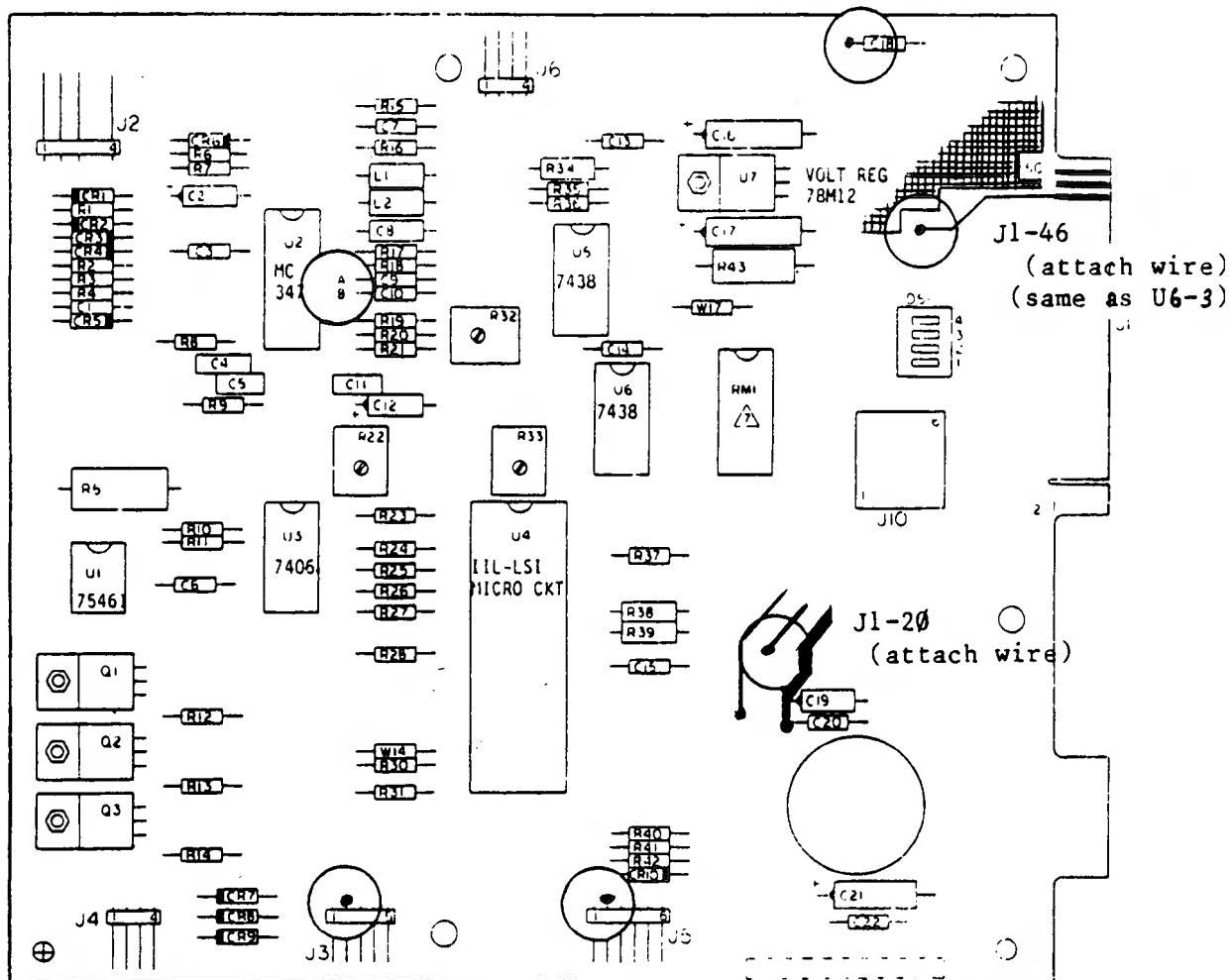


SHUGART SA800  
Test Point Locations

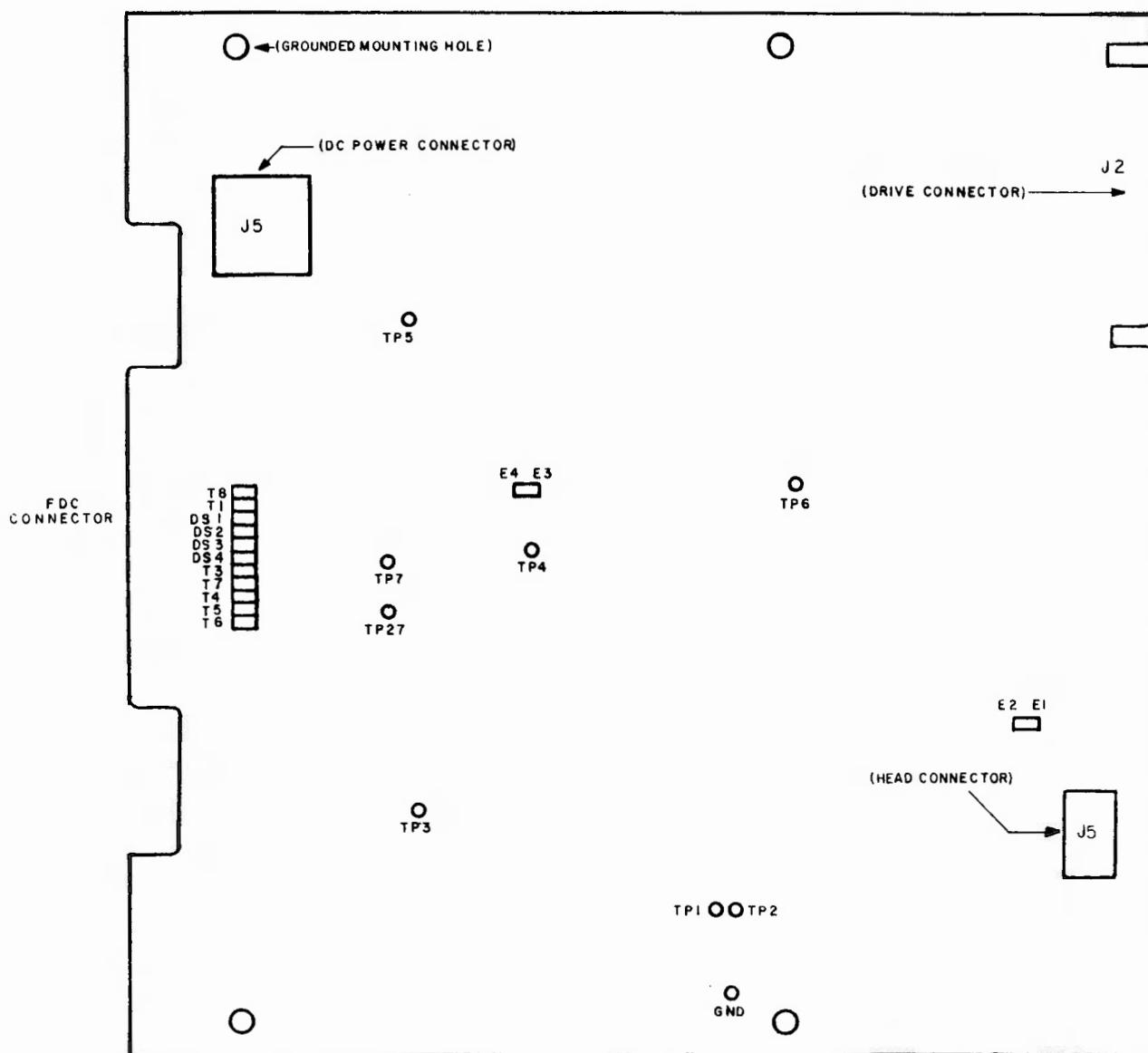


CDC 9404-B PCB  
Discrete Version  
Test Point Location

## CIRCUIT GROUND



CDC 9404-B  
LSI Version  
Test Point Location  
(NOTE: Board is upside down when viewed on chassis)



TPI  
TEST POINT LOCATION

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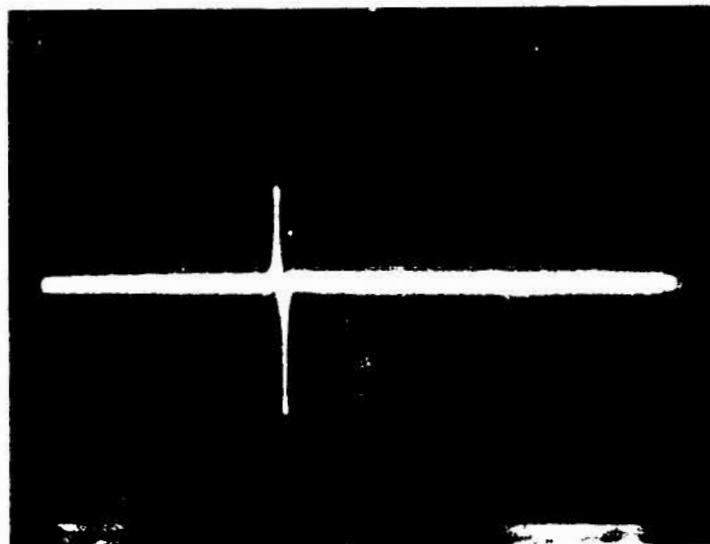
## NOTE:

There are two different alignment diskettes available, SHUGART and DYMEK. While each one has all signals necessary to complete an alignment, the two diskettes differ slightly in the signal produced.

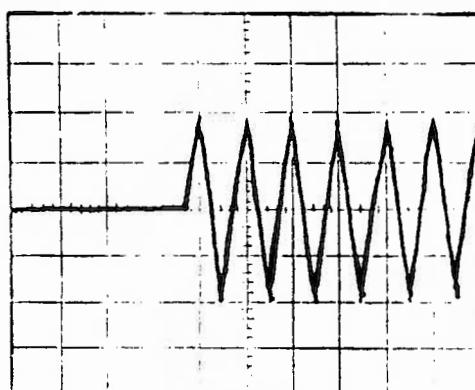
This is most noticeable during the Index Sector Timing tests. While the DYMEK diskette produces a signal burst to be measured, the SHUGART diskette produces only one cycle to be measured.

If the difference in the two diskettes will be apparent during a test two waveforms will be shown, one for each diskette.

The following oscilloscope photographs and waveform drawings are taken from properly aligned drives, and should be considered "typical". They are "text book" cases and do not show extraneous noise or minor differences from unit to unit. While your readings may differ slightly in waveform or amplitude, they should still remain reasonably close to the following illustrations.

INDEX SECTOR TIMING WAVEFORMS  
SHUGART, TPI, DRIVES50  $\mu$ sec/div horizontal  
500 mV/div vertical

SHUGART ALIGNMENT DISKETTE

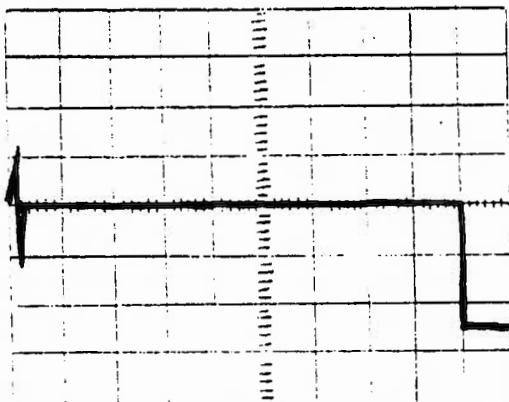
50  $\mu$ sec/div horizontal  
500 mV/div vertical

DYMEX ALIGNMENT DISKETTE

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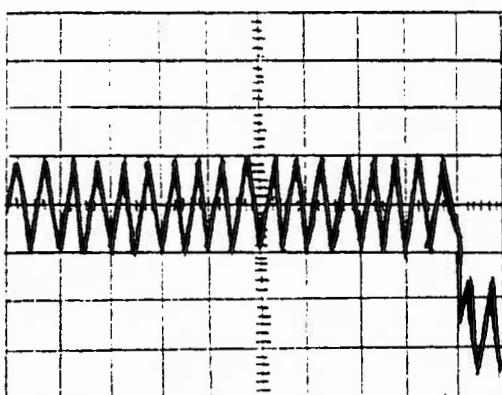
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INDEX SECTOR TIMING WAVEFORMS  
CDC DRIVES

50  $\mu$ sec/div horizontal  
Channel A 500 mV/div vertical  
Channel B 2 V/div vertical

SHUGART ALIGNMENT DISKETTE



50  $\mu$ sec/div horizontal  
Channel A 500 mV/div vertical  
Channel B 2 V/div vertical

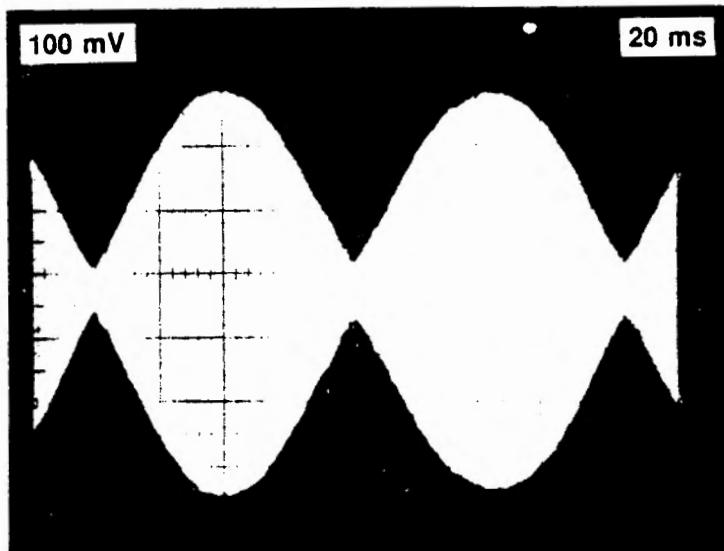
DYMEX ALIGNMENT DISKETTE

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HEAD RADIAL ALIGNMENT "CAT'S EYES" PATTERN  
ALL DRIVES



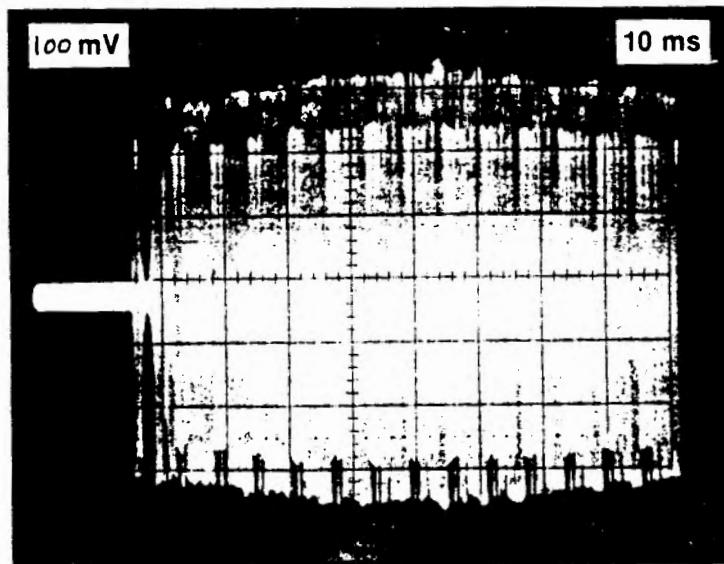
20 msec/div horizontal  
100 mV/div vertical

PATTERN AVAILABLE ON BOTH SHUGART AND DYMEK DISKETTES

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HEAD LOAD TIMING PATTERN  
ALL DRIVES

10 msec/div horizontal  
100 mV/div vertical

PATTERN AVAILABLE ON BOTH SHUGART AND DYMEK DISKETTES

PATTERN SHOWN TAKEN FROM SHUGART DRIVES  
TPI DRIVES IDENTICAL  
CDC DRIVES IDENTICAL WITH THE EXCEPTION OF TIMING SPECIFICATION

HEAD AZIMUTH PATTERN  
ALL DRIVES



10 msec/div horizontal  
100 mV/div vertical

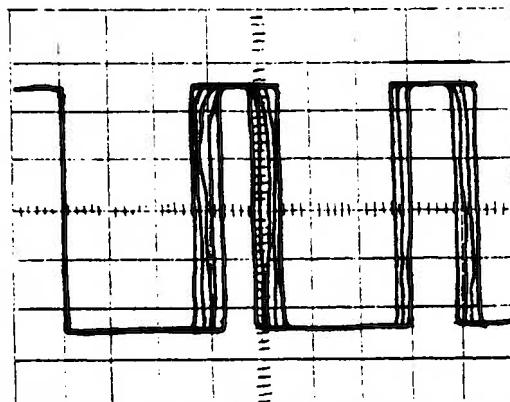
PATTERN AVAILABLE ON BOTH SHUGART AND DYMEK DISKETTES

PATTERN SHOWN TAKEN FROM SHUGART DRIVES  
CDC AND TPI DRIVES IDENTICAL

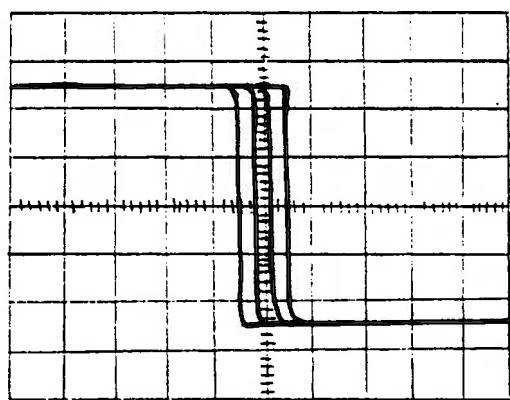
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RAW DATA ADJUSTMENT -- JITTER AND SYMMETRY  
ALL DRIVES

NOTE: Waveforms for CDC drives will be inverted from those shown

1  $\mu$ sec/div horizontal  
1 V/div vertical

NORMAL SWEEP

1  $\mu$ sec/div horizontal  
1 V/div vertical

EXPANDED SWEEP

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## **SERVICE POLICY**

Radio Shack's nationwide network of service facilities provides quick, convenient, and reliable repair services for all of its computer products, in most instances. Warranty service will be performed in accordance with Radio Shack's Limited Warranty. Non-warranty service will be provided at reasonable parts and labor costs.

Because of the sensitivity of computer equipment, and the problems which can result from improper servicing, the following limitations also apply to the services offered by Radio Shack:

1. If any of the warranty seals on any Radio Shack computer products are broken, Radio Shack reserves the right to refuse to service the equipment or to void any remaining warranty on the equipment.
2. If any Radio Shack computer equipment has been modified so that it is not within manufacturer's specifications, including, but not limited to, the installation of any non-Radio Shack parts, components, or replacement boards, then Radio Shack reserves the right to refuse to service the equipment, void any remaining warranty, remove and replace any non-Radio Shack part found in the equipment, and perform whatever modifications are necessary to return the equipment to original factory manufacturer's specifications.
3. The cost for the labor and parts required to return the Radio Shack computer equipment to original manufacturer's specifications will be charged to the customer in addition to the normal repair charge.

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