Radio Shack®

Service Manual

TRS-80®

Model 16

Catalog Number 26-6004/5/6

TRS-80®Model 16B/16B-HD Service Manual

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SERVICE MANUAL

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Contents   Page No.

List of Figures

List of Tables

1/ Introduction

The TRS-80 Model 16B/16B-HD Microcomputer is a powerful disk-based desk-top business computer with many advanced features. These features include portable software, 256K of memory expandable to 768K, detachable typewriter-format keyboard with numerical keypad and 8 programmable function keys, green CRT Monitor screen, and one parallel and two serial ports for external connection to a variety of printers and communications links.

Optional features include an extra internal floppy Disk Drive (Radio Shack Catalog Number 26-4167) or an external floppy Disk Bay Expansion Unit (1-drive unit 26-4165 or 2-drive unit 26-4166), a 12 Megabyte Hard Disk System (26-4152/3) for mass storage, an ARCNET™ system (26-6501/2) for local area communications network, a graphics board (26-4104) for video graphics capability, and a multi-terminal interface board.

This manual is intended as a guide to assist in the diagnosis of system problems to the subassembly level. It contains detailed instructions on disassembly and assembly of major subassemblies as well as some troubleshooting hints for the PCBs and subassemblies contained in the system. It also includes a section on the theory of operation that describes board operation and some individual component functions. It does not, however, provide a component by component analysis of the system.

The basic Model 16B Microcomputer is supplied with one floppy Disk Drive and five PCB assemblies; the Model 16B-HD is supplied with one floppy disk and on internal 15-meg hard disk. Two of the PCB assemblies are mounted in the Electronics Module, which is attached to the Base Assembly. These include the I/O Processor PCB and the Power Supply PCB. The Sound PCB, is mounted inside the Base Assembly at the left front corner. The CRT Monitor PCB mounted on the Bezel/Cover Assembly, is the electronics for the CRT assembly. The seven slot expansion unit plugs into the I/O Processor PCB, and the 16-bit CPU and memory board plug into the expansion unit along with the Video/Keyboard Interface PCB.

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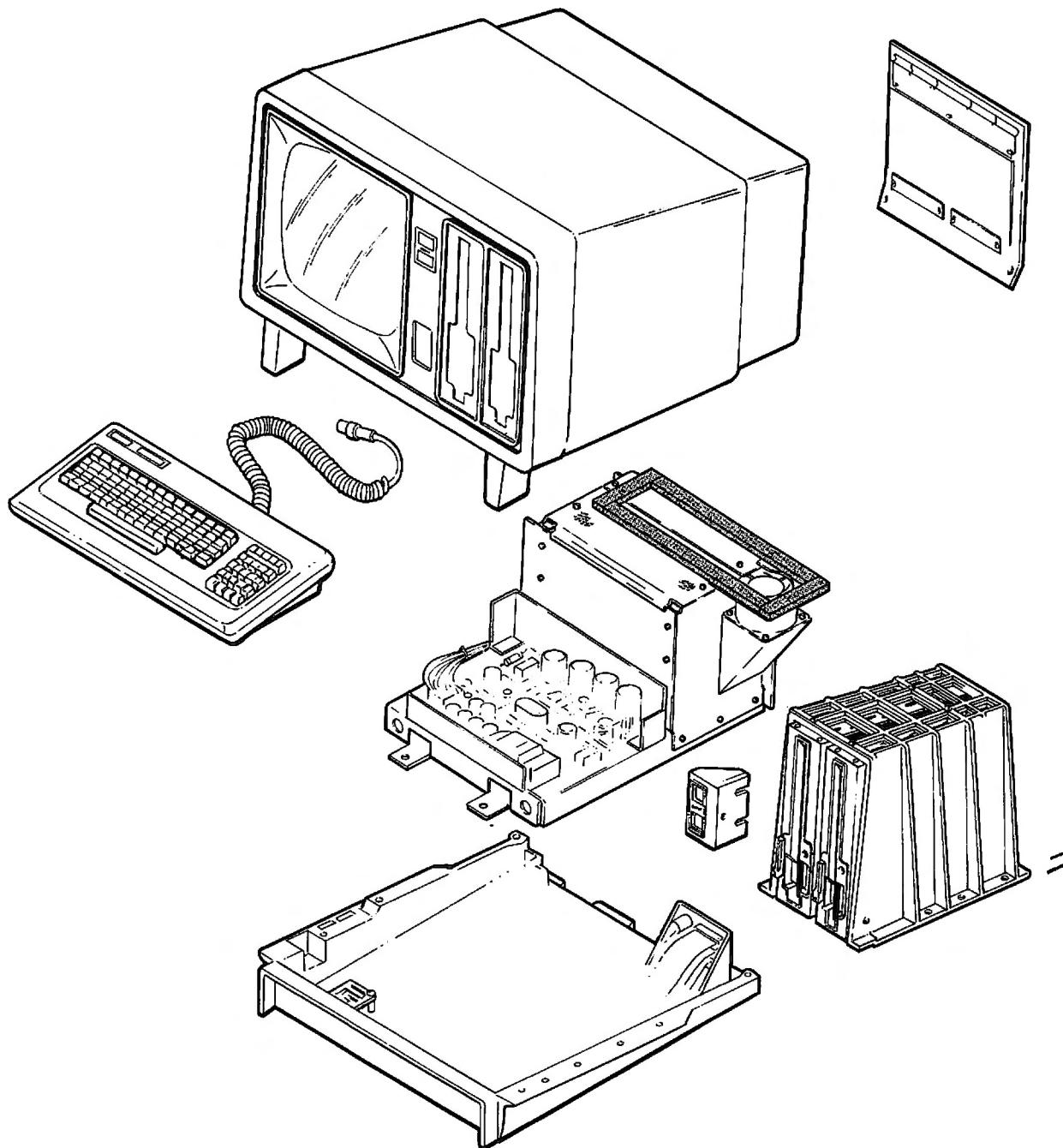
Figure 1-1.   Major Assemblies, Model 16B/16B-HD

A simplified exploded view of the Model 16B/16B-HD (Figure 1-1) helps locate major sub-assemblies as they are described in the following paragraphs. Disassembly procedures noted in Section 3 must be followed in the order presented due to the mounting locations of the individual components.

The major subassemblies that comprise the Model 16B/16B-HD include (1) the Base Assembly, (2) the Electronics Module, (3) the Reset/Power On Indicator Module with cable assembly, (4) the Disk Drive/Drive Support structure, (5) the Bezel/Cover Assembly, (6) Card Cage Assy, and (7) the Keyboard Assembly. The disassembly of each of these assemblies is discussed in Section 3. Care should be exercised in handling plastic components to prevent scratching or marring of the surface finish.

1.1 Base Assembly

The Base Assembly consists of the molded plastic base, power and signal I/O component mounting brackets, power ON/OFF switch, and Sound PCB that is responsible for generating an audible tone when key closure is achieved. The other assemblies of the Model 16B/16B-HD are mounted to the Base Assembly. The Base Assembly has rubber feet to protect the surface on which the Model 16B/16B-HD is placed for operation.

1.2 Electronics Module

The Electronics Module consists of a formed metal chassis, three component mounting brackets, two printed circuit boards, and a card cage assy with three additional boards. It is mounted to the instrument Base Assembly with four screws that are accessible when the Bezel/Cover Assembly is removed from the computer. When these screws and the electrical connections to the assembly are removed, the Electronics Module may be removed from the Base Assembly as a unit. The module mounts the I/O Processor PCB, the instrument cooling fan, the Video/Keyboard Interface PCB, 16-bit CPU/Memory PCBs, and the Power Supply PCB. Three ribbon cables connected to the I/O Processor Board exit the module through a slot in the right side of the chassis and connect to the rear terminal input connectors or the disk drive(s). The Power Supply Assembly covers the front half of the assembly. The Mother Board mounts vertically in the edge card connector in the middle of the I/O Processor Board. It is rigidly supported by the card cage sheet metal at the rear of the module.

1.3 Reset/Power On Indicator Module

The Reset/Power On Indicator module is mounted to the Drive
Support Structure and consists of the power ON/OFF
indicator, the reset switch, and cable assembly. The reset
switch, when pressed, blanks the screen and flashes the
command INSERT DISKETTE on the screen. To remove this
module from the unit, it is necessary to first remove the
Bezel/Cover Assembly. When reinstalling the assembly, it
must be properly positioned with respect to the Bezel/Cover
Assembly cutout.

1.4 Drive Support Structure

The Drive Support Structure is a rugged, formed sheet metal
design that is attached to the Base Assembly with six
mounting screws. Its design permits circulating air flow to
the disk drives for improved performance. It contains
shielding to protect the floppy disk drive electronics from
RF interference by the switching power supply or video
display. It mounts either one or two slim line floppy Disk
Drive assemblies (16B), or one slim line floppy Disk Drive
and one 15 Megabyte Hard Disk (16B-HD). The 16B drive
support structure is normally supplied with one disk
assembly in the left mounting position but a second may be
added if desired (see Installation Kit 26-4167). Cabling
for the additional floppy drive is already contained in the
wiring harness so that no cables have to be added or
replaced. The 16B-HD is supplied with one floppy disk and
one hard disk.

1.5 Bezel/Cover Assembly

The Bezel/Cover Assembly is a molded plastic cover that
contains the cathode ray tube (CRT), the CRT monitor PCB and
associated hardware. It is attached to the base with
mounting screws that are accessible from the underside of
the unit. There are three mounting screws on the right side
of the case, three on the left, one in the back, and three
at the front.
Once these are removed, the Bezel/Cover Assembly may be
tilted up and lifted off the Base Assembly.

CAUTION

The cables between the Video/Keyboard Interface
PCB, Power Supply and the Monitor PCB are short and
may be damaged if care is not exercised during the
removal. Exercise care to prevent damage to the
components mounted to either the Base Assembly or
the Bezel/Cover Assembly. Do not drop or otherwise
mishandle the Bezel/Cover Assembly as the CRT may
implode, causing harm to personnel and components.

Plug-in connectors attach the Bezel/Cover Assembly
electrically to the Base Assembly. To detach the
Bezel/Cover Assembly completely, disconnect these
connectors. Handle the assembly carefully to prevent
scratching or marring the cover surface.

The 12 inch CRT (Cathode Ray Tube) and Video Monitor PCB
form the Video Monitor Assembly for the TRS-80 Model
16B/16B-HD. The Video Monitor PCB is mounted on the inside
LH side of the Bezel/Cover Assembly. Signal and power
cables interconnect it with the Video/Keyboard Interface PCB
and Power Supply Assembly on the Electronics Module.

The Rear Door Assembly is a removable assembly that allows
easy access to the rear compartment and card cage (when
installed). It slides into a groove at the top of the
Bezel/Cover Assembly and is attached to the Base Assembly by
two thumb screws that secure it at the bottom.

1.6 Keyboard Assembly

The Keyboard Assembly is mechanically separate from the
Base/Bezel/Cover Assembly and is electrically connected
through a 5-pin DIN connector located on the front lower lip
of the Base Assembly. The two units are connected by a
coiled cable assembly attached to the Keyboard Assembly that
allows it to be moved up to 3 feet away from the Base
Assembly. A strain relief bushing provides protection for
the signal cable to prevent accidental pullout of the cable
from the Keyboard Assembly. The keyboard is a thin-line
design with standard typewriter key pad and numeric key pad.
Contained as part of the numeric key pad section are eight
function code buttons, F1 through F8, which allow
application dependant programmable functions to be selected.
Cork feet provide protection for the mounting surface on
which the Keyboard Assembly is mounted.

2/ Technical Specifications

2.1 Physical Characteristics

2.1.1 Case/Bezel/Base Assembly
```
Width   21.0 inches (53.3 cm)
Height  13.5 inches (34.3 cm)
Depth   20.5 inches (52.1 cm)
Weight  49.9 pounds (22.5 kgm)
```

2.1.2 Keyboard
```
Width   18.0 inches (45.7 cm)
Height   2.5 inches (6.4 cm)
Depth    7.5 inches (19.1 cm)
Weight   3.3 pounds (1.49 kgm)
```

2.2 System Operating Characteristics

	Min	Typ	Max	Units
Ambient Temperature	55	75	85	Degree F
	12	23	30	Degree C
Voltage Range (USA)	95	115	135	VAC
(Europe)	190	230	270	VAC
Current Drain	---	1.5	2.0	A
Line Frequency	47	50/60	63	Hz

2.3 Peripheral Interfaces

Serial Interface

Channel A allows asynchronous or synchronous communication.

Channel B allows asynchronous communication only.

Both channel A and B conform to the RS-232C Standard

Both use DB-25 connectors on the back of the display console. Pin-out connections are shown in Section 5, Cable Wiring/Pin Designations.

Parallel Interface

> Connects to a line printer via the 34-pin connector on
> the back of the display console. See Section 5, Cable
> Wiring/Pin Designations.
>
> Outputs 8 data bits in parallel. Inputs 4 data bits.
> All levels are TTL compatible

Multi-Slot Card Cage

> Provides four additional slots to accommodate hard disk
> drive interface, graphics board, 16-Bit memory board,
> multi-terminal interface board.

Kit 26-4167

> Adds disk drive to existing unit.

Disk Bay Expansion Unit

> Optional extra unit contains either one or two disk
> drives, 8" floppy diskette, 500K byte storage per
> diskette (single sided, double density or 1 megabyte
> with double sided, double density). Disk Bay Expansion
> Unit 26-4165 (1 drive) or 26-4166 (2 drive).

16-Bit CPU Board

> Provides 16-bit operation for high-level language tasks.
> Supports 8 levels of vectored interrupts, 4 levels of
> fixed priority bus arbitration, a Z80 to MC68000 memory
> interface controller, and direct access for up to 7
> megabytes of memory.
>
> The main components of this board are the MC68000 CPU
> and the AM9519A Interrupt Controller.

256K-Byte, 16-Bit Memory Board

> Offers optional byte parity checking and detection
> logic and selecting to map memory on any 256K boundry
> within 7-Meg memory space.

3/ Disassembly/Assembly Procedures

The Model 16B/16B-HD Microcomputer is designed for table-top operation. Dimensions of the main housing assembly and the keyboard assembly are given in Technical Specifications, Section 2. A desk assembly may be used (Radio Shack Catalog Number 26-4301) that allows mounting of optional extra disk drives used with the Model 16B/16B-HD system. Adequate space should be left around the unit to allow sufficient air flow to all components.

If the unit is to be disassembled for service or repair, follow the instructions contained in the following procedures. Exercise care in handling the Bezel/Case Assembly to prevent scratching or marring the surface finish.

3.1 Cover/Bezel Assembly

1. Remove all power from the unit by disconnecting the power cord. Remove peripheral cables (if required).

2. Remove from the disk drives, the cardboard inserts that protect the drive during shipment. (Save for later use.)

3. Remove the Rear Access Door by removing the screws at the bottom (non-captive screws) and pulling out and down on the door.

4. Place the unit upside down on a smooth, padded surface to prevent scratching the painted surfaces.

5. Remove ten (10) screws that attach the Cover/Bezel Assembly to the Base Assembly. There should be three screws on the right side, three screws on the left, one screw at rear, and three screws at the front. See Figure 3-1, which shows the location of the screws.

6. Hold the two assemblies together and turn the unit rightside up.

7. Tilt the Cover/Bezel Assembly toward the front until the rear of the case clears the input bracket, then slide the Cover/Bezel Assembly forward slightly. Spread the sides of the cover and then lift straight up, exercising care to prevent damage to components.

REAR

Cover/Bezel
Mounting Screws

Drive Mounting
Screws

FRONT

Cover/Bezel
Mounting Screws
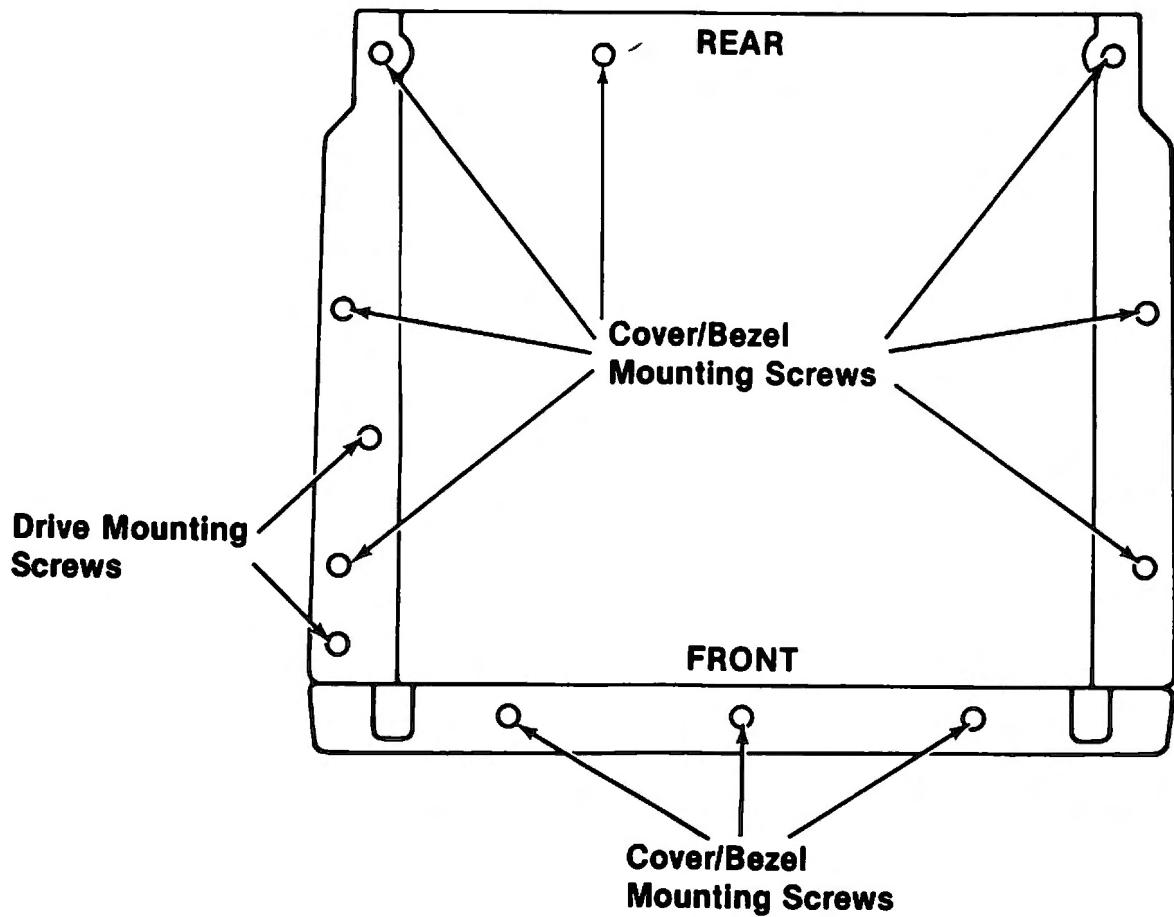
Figure 3-1. Cover/Bezel Assembly Mounting Screws

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8. Once the Bezel/Cover Assembly is clear, lay it off to the left side of the base unit. Separate the two units (Base and Cover/Bezel) by disconnecting the attaching harnesses (one to the Video/Keyboard Interface PCB, and an inline connector to the Power Supply Assembly).

9. Remove the ground wire spade lug terminal from the CRT Monitor PCB. This completely separates the Bezel/Cover Assembly from the Base Assembly.

3.2 CRT Removal

Note: The CRT and CRT Monitor PCB are replaced as a unit.

1. Disconnect the tube socket from the rear of the CRT.

2. Disconnect four wires (blue/green from left side and black/red from the right side) that are connected to the deflection coil.

CAUTION

Make sure the high voltage is discharged from the CRT (use grounded screwdriver to discharge).

3. Disconnect the high voltage clip.

4. Remove the lower right and upper left mounting nuts and washers. This will allow the grounding wire to be removed from around the rear of the CRT.

5. Remove the main connector P1 from the CRT Monitor PCB. Remove the remainder of the screws that attach the CRT Monitor PCB to the Bezel/Case Assembly and remove the board from the assembly.

6. Place the Bezel/Cover Assembly on its front surface (CRT face against the table) and remove the other two nuts and washers from the CRT. Carefully lift the CRT from the Bezel/Cover Assembly.

CAUTION

Handle the CRT very carefully to prevent injury due to CRT implosion. Do not handle tube using the neck of the tube. ALWAYS USE GOGGLES OR SAFETY GLASSES.

7. Assemble the Cover/Bezel Assembly in the reverse order
    of disassembly. Make sure that the grounding wire from
    the Electronics Module is connected to the lug on the
    CRT Monitor PCB lower rear mounting screw.

3.3 Brightness and Contrast Controls

1. The brightness and contrast controls are accessible
    after the Bezel/Cover Assembly has been removed from the
    Base Assembly.

2. Remove either control by loosening the attaching nut and
    sliding the control off the bracket to the front or
    rear.

3. The knobs are glued to the pot shaft. If pot
    replacement is required, the knob must be replaced also.

4. Remove the connector from the pot, noting the manner in
    which the connector is mounted. The connector is not
    keyed, so it would be possible to put it on backward
    when reassembling. The numbers on the connector should
    be down and not able to be read.

5. The brightness control (500K ohms) is to the front of
    the assembly, contrast control (500 ohms) is to the
    rear.

6. Reassemble in the reverse order, making sure the knobs
    are fully pushed onto the pot shafts to align with the
    cutout slots in the Base Assembly.

3.4 Bezel

The bezel may be detached from the case if either of the
parts needs to be replaced. Remove either the CRT or CRT
board (depending on which part is to be replaced). The
bezel is attached to the case with five screws. Loosen
these screws and the case may be lifted from the bezel.
When replacing the case, make sure the Tinnerman clips that
accept the screws from the Base Assembly are properly
inserted into the case.

3.5   Drive Support Structure

The Drive Support Structure is a formed sheet metal part that houses the thin line Disk Drive assemblies. It is attached to the Base Assembly with six screws, two of which are accessible from the righthand underside of the case. The other four screws are accessible only after the Cover/Bezel Assembly has been removed.

1.   Remove the Cover/Bezel Assembly (see Paragraph 3.1).

2.   Remove the power and signal connectors from the rear of the disk unit(s).

3.   Loosen the screws that mount the Reset/Power ON Module mounting bracket and remove the bracket by sliding it forward.

4.   Remove the Drive Support structure by removing the four screws at the left side of the structure and the two at the right (accessible from the underside of the RH lip of the Base Assembly).

5.   Remove the structure from the base.

6.   Remove the disk drive from the support structure by removing two screws at the top and two screws at the bottom of the Drive Support Assembly.

7.   Slide the disk drive forward to remove it from the support structure.

8.   If a drive is to be replaced, remove the front bezel by removing the mounting screws (two at the top and two at the bottom front lip).

9.   Reassemble in the reverse order of disassembly.

3.6   Electronics Module

The Electronics Module is mounted to the Base Assembly with
four screws that are accessible when the Bezel/Cover
Assembly is removed from the unit. The module may be
removed as a complete assembly or individual parts,
depending on which parts troubleshooting procedures indicate
may be faulty. Contained on this assembly are six PCB
assemblies (I/O Processor PCB Assembly, Video/Keyboard
Interface PCB Assembly, Mother Board, 16-bit CPU, 16-bit
Memory, and Power Supply PCB), and the instrument cooling
fan. Interconnection of the I/O Processor PCB and other
components is accomplished by the use of edge-card
connectors.

1. Remove the shield from the Power Supply Assembly by
    removing the attaching screws and clips.

2. Disconnect the plug from the sound board at the left
    front of the Base Assembly.

3. Disconnect the switched AC input (blue and brown wires)
    from the terminal strip at the left rear of the Power
    Supply Assembly. The wires going to the fan assembly
    may be left connected as they are part of the
    Electronics Module.

4. Remove the plugs from connectors J2 and J3 on the
    Video/Interface PCB.

5. Disconnect the inline connector to the CRT Monitor PCB
    (at left side of the Electronics Module).

6. Remove the wiring (brown and blue twisted pair) from
    clips on the front and right side of the electronics
    chassis.

7. Unplug the ground wire connected from the front of the
    Electronics Module to the Keyboard Assembly plug.

8. Disconnect the inline fuse to the Keyboard Assembly
    plug.
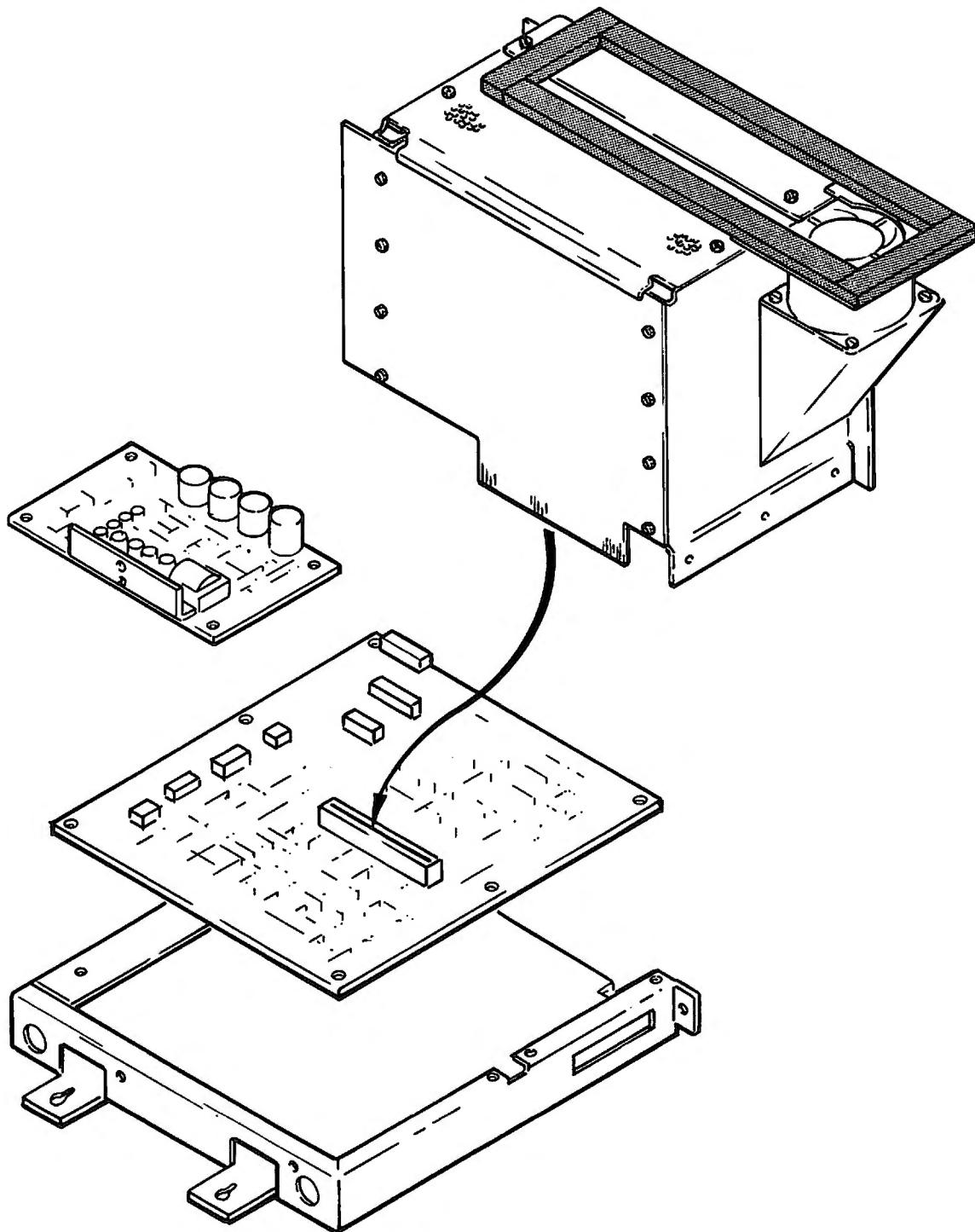
Figure 3-2.   Electronics Module Assembly

9. Disconnect the grounds from the two cables attached to the Video/Keyboard Interface PCB on the grounding lugs of the RH Board Retainer.

10. Remove the PC Board Retainers (one on each side) that secure the PCBs in the Mother Board assy.

11. Disconnect the Cover/Bezel cable assy connector and the Keyboard cable connector from the Video/Keyboard Interface Board.

12. Remove the boards from the Card Cage, making note of their position for re-assembly. Boards must be re-installed in the relative position listed below. The lowest slot os position 1.

Relative Board Position	Description	Priority
1	ARCNET	1 (lowest position)
2	Hard Disk Interface	2
3	Multi-Terminal Interface	3
4	Graphics	None
5	Video/Keyboard Interface	None
6	256K Memory Board	None
7	256K Memory Board	None
8	256K Memory Board	None
9	16-Bit CPU Board	None

All the listed boards might not be included in all units.

13. Unplug P5 from the J8 connector on the RH side of the Mother Board. Then remove the screws on the RH side of the Card Cage, which mount the Card Cage to the Electronics Module chassis.

14. Remove the four screws that hold the Card Cage Cover; remove the Cover.

15. Remove the screws that hold the Chassis Rear Panel; remove the Rear Panel.

16. Remove the three screws that hold the RH Card Cage Panel. The middle screw will release the grounding lug that goes to the CRT Monitor PCB.

17. Remove the three screws on the LH side of the chassis. The middle screw will release the ground wire.

18. Remove the Mother Board assy from the Electronics Module chassis.

19. Remove the Power Supply Assembly from the Electronics Module chassis by removing two screws at the left and right rear of the Power Supply and two screws at the front vertical lip.

20. Disconnect plug P5 from J5 on the I/O Processor PCB and lift the Power Supply Assembly out of the way. The fan and power connections to the disk drives should still be attached. Pull the cable to the Sound PCB through the hole in the chassis.

21. Unplug from the front of the I/O Processor PCB the connector and ground lug that go to the Reset Switch/Indicator Assembly.

22. Remove the seven Phillips machine thread screws that attach the I/O Processor PCB to the Electronics Module chassis (one attaches the ground lug at the front right side of the chassis).

    Note: Make sure that on reassembly the insulated standoffs are inserted between the I/O Processor PCB and the metal chassis.

23. Slide the I/O Processor PCB to the rear, exercising care to prevent damage to board components, and remove it from the bottom metal chassis bracket.

24. The three ribbon cable connectors may now be removed from the board. Note the manner in which the cables are routed to clear the connector for the Video/Keyboard Interface PCB. Make sure that on reassembly this routing is followed so that the connector (J0) on I/O Processor PCB is clear.

25. Reassemble in the reverse order, making sure that all cabling is clear and not pinched between any parts of the metal chassis brackets.

CAUTION

AC wiring should be routed according to Figure 5-2 to prevent electrical interference.

3.7 Keyboard

The Keyboard Assembly is a separate assembly that is attached to the main computer unit by a five-wire cable terminated in a DIN plug. A coiled cable assembly allows the keyboard to be separated from the main computer unit by up to three feet.

To disassemble the keyboard, proceed as follows:

1. Turn the keyboard upside down on a padded surface to prevent damage to the keypads.

2. Remove from the underside of the assembly the seven screws that tie the two halves of the keyboard together.

3. Hold the two halves together and turn them right-side up.

4. Lift off the top cover.

5. Lift off the black keyboard bezel.

6. Disconnect the connector from the PCB and remove the keyboard/PCB assembly from the keyboard base.

7. On reassembly, be sure that the pins on the keyboard/PCB assembly are properly seated in the four mounting bosses of the keyboard base before installing the top cover.

8. Reassemble in the reverse order of disassembly.

4/ Adjustments

The only adjustments on the Model 16B/16B-HD Microcomputer
are associated with the Floppy Disk Interface and are
required to be made only if disk drives are changed or
components have drifted due to aging. The adjustments are
located on the I/O Processor PCB and in the standard unit
are not accessible without removing the card cage assy. It
is not necessary to have the unit completely interconnected
in order to make these adjustments. The only requirement is
that power be supplied to the I/O Processor PCB. Follow the
procedure noted below to achieve the correct adjustments.

Exercise care in moving the cables that will run over the
components that require adjustment. Make sure that no
cables are pulled loose when gaining access for the
adjustments. (See Figure 4-1.)

1. Move the Video/Keyboard Interface PCB to the first
    unused slot below the 16-bit CPU and Memory Boards, or
    completely remove the PCB.

2. Turn power ON and engage the manual RESET on the front
    panel. Move the jumper from the storage position
    E31-E49 to the test position E30-E31.

3. Connect a scope to test point TP9 (located on the right
    side of the board looking from the rear of the unit) and
    verify the presence of a square wave pulse train.

4. Connect a frequency counter to TP9 and adjust C61
    (located in the middle of the board just to the left of
    jumper installed in Step 2) for a frequency of 265 KHz,
    if less than 60 seconds has elapsed since power was
    turned on. If more than 60 seconds has elspased since
    power was applied, wait at least eight minutes and
    adjust to 255 KHz.
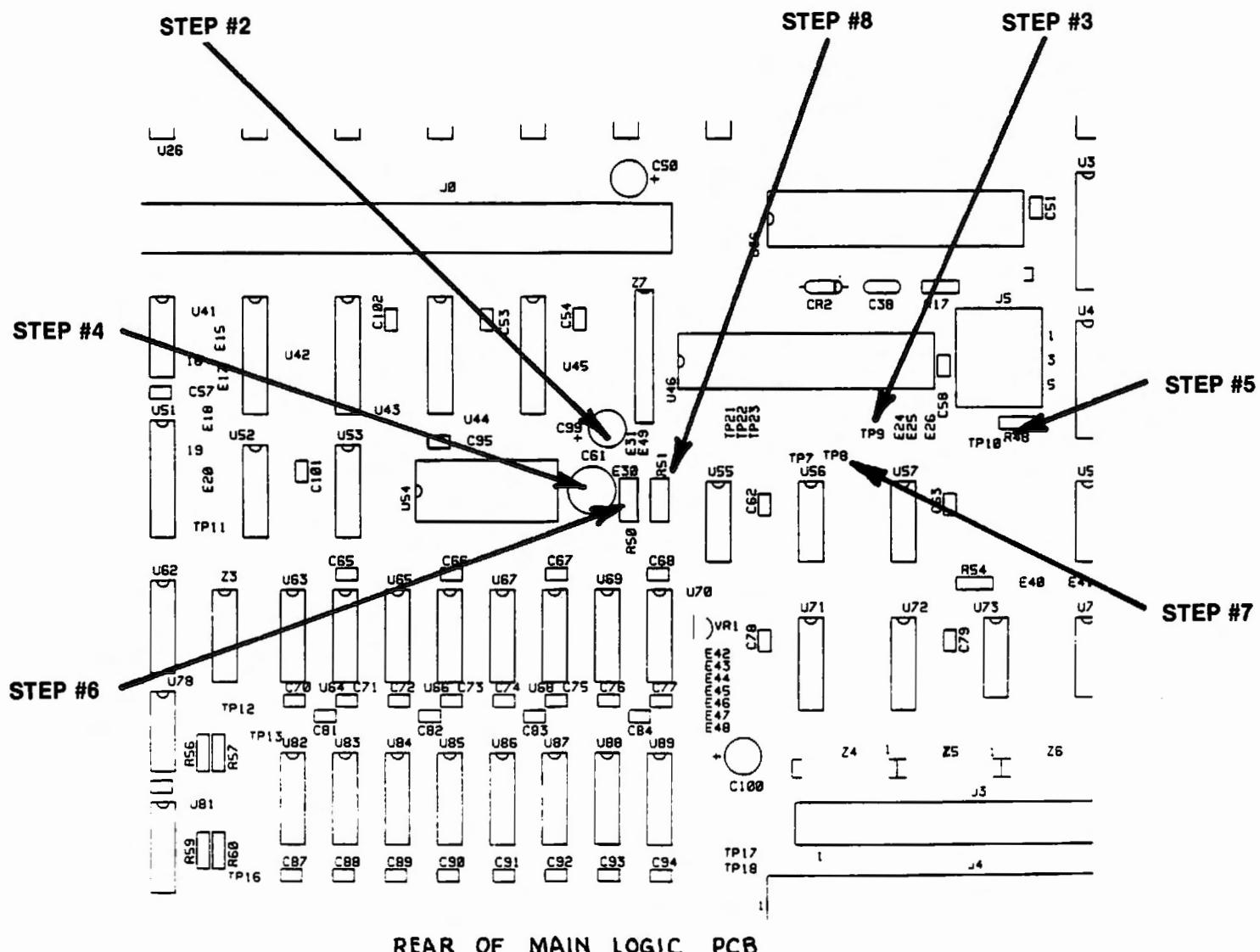
Figure 4-1. Adjustments

5. Connect the scope lead to test point TP10 (located just to the right of TP9 looking from the rear of the unit).

6. Adjust R50 (located just to the right of C61 looking from the rear of the unit) for a positive pulse width of 200 nanoseconds.

7. Connect the scope lead to test point TP8 (located just to the left of TP9 looking from the rear of the unit).

8. Adjust R51 (located just to the right of R50 looking from the rear of the unit) for a positive pulse width of 500 nanoseconds.

9. Remove the jumper installed between points E30 and E31 and reposition it between points E31 and E49.

10. Turn power OFF and ensure that all components of the Model 16B/16B-HD are electrically interconnected properly. It is not necessary at this time to mechanically reassemble the unit.

11. Turn the power ON. Re-install Video Board, if removed in step 1.

12. When the screen shows "INSERT DISKETTE", insert the test floppy diskette and boot up the system.

13. Run the following test to verify adjustments:

   AUTOTND (You will need one or two blank double-sided diskettes to run this rest.)

14. If the test is completed correctly, reassemble the Model 16B/16B-HD mechanical components in the reverse order of disassembly noted at the first part of this procedure or reinstall the cards removed.

To verify complete operation of the Model 16B/16B-HD, run the following tests:
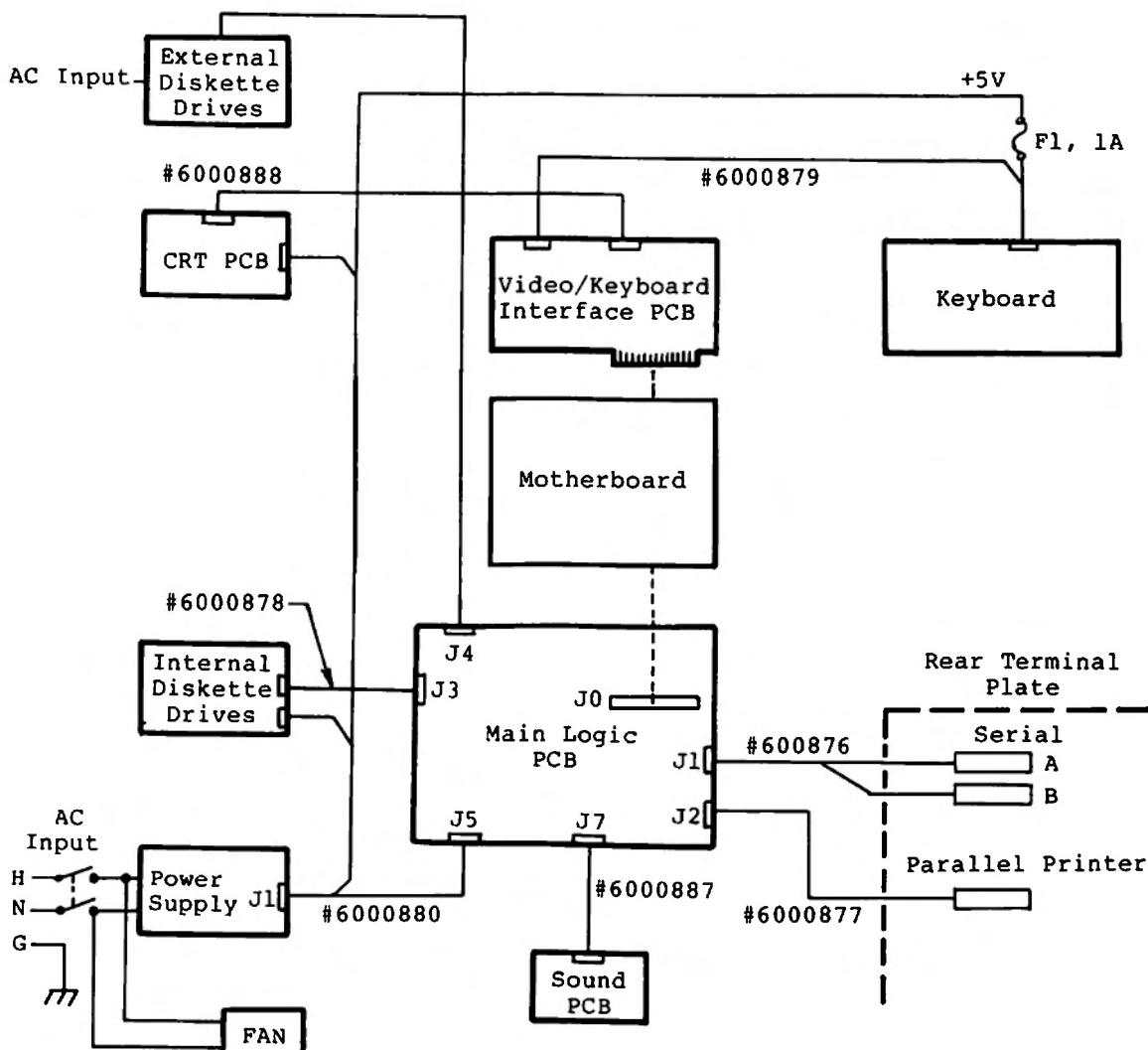
   SYSTEM (need serial loop-back and PRINTER-FDC EXT TEST cable)

   MEM II

   AUTOTND (One double-sided diskette per drive is required.)

5/ Cabling Diagrams/Pin Designations

Contained in this section is a cable block diagram of the
Model 16B/16B-HD System, cable wiring and routing, and pin
designations of all the connectors of the Model 16B/16B-HD.
The Video/Keyboard Interface PCB plugs into the Mother
Board. The Mother Board plugs into the I/O Processor PCB at
connector J0. All other connections are cable connectors
that plug into receptacles on the various boards of the
system. The cables are listed in numerical order by part
number noted on the overall cable/connector location
drawing, Figure 5-2 and 5-3.

Note: Position shown above does not indicate
       physical location on board. See Figure 5-2.

Figure 5-1. Cable Interconnection Layout
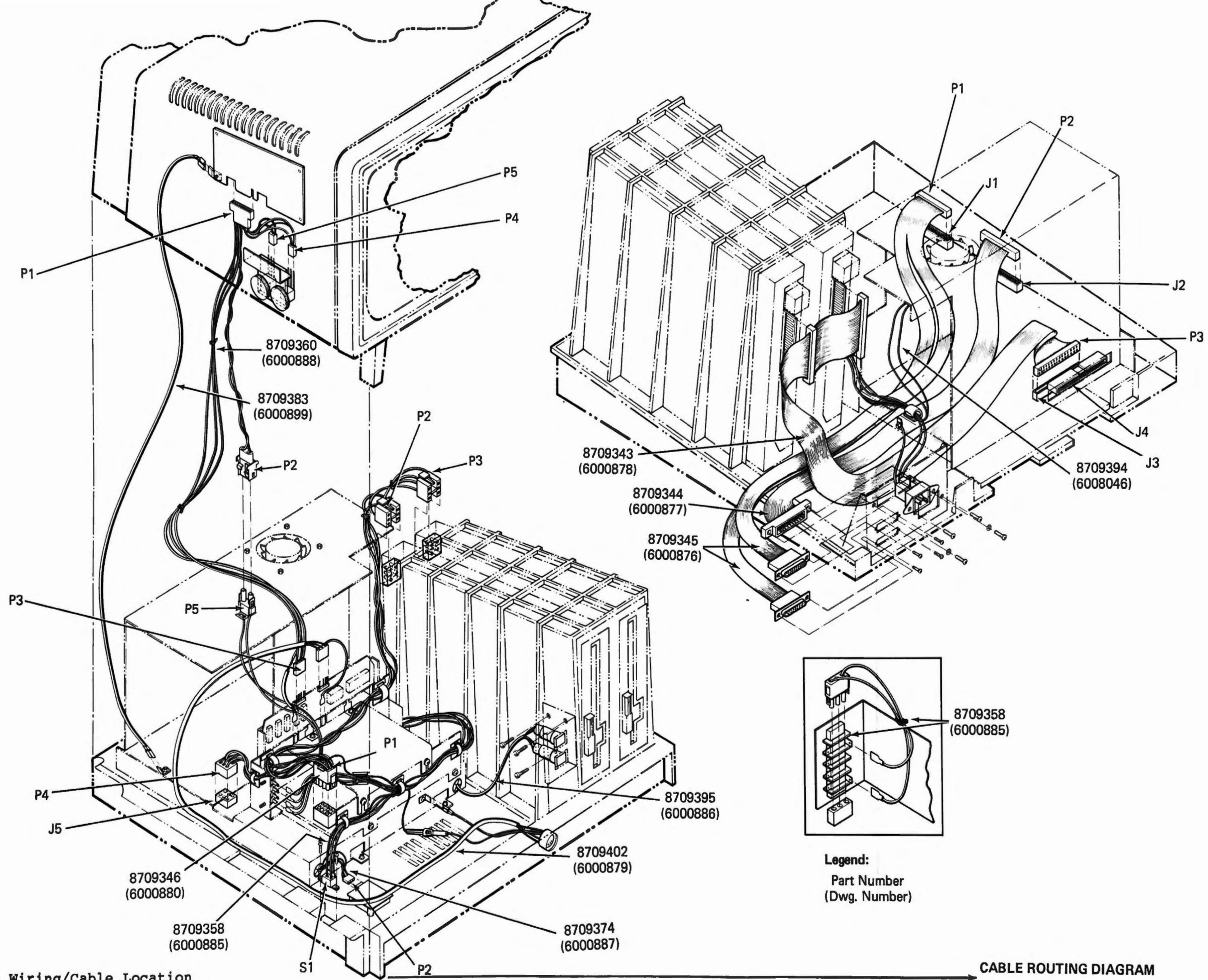
Figure 5-2. Cable Wiring/Cable Location

P1

P5

P4

8709360
(6000888)

8709383
(6000899)

P2

P2

P3

P3

P5

P4

J5

8709346
(6000880)

8709358
(6000885)

S1

P2

8709374
(6000887)

8709402
(6000879)

8709395
(6000886)

P1

P1

P2

J1

J2

P3

J4

J3

8709343
(6000878)

8709344
(6000877)

8709345
(6000876)

8709394
(6008046)

8709358
(6000885)

Legend:

Part Number
(Dwg. Number)

CABLE ROUTING DIAGRAM

- 23 -

Cable Assembly 8000876, RS-232 Serial Interface

Main PCB Connector P1/J1			Rear Input Channel A
Pin	Name	Description	Pin Number
1	GND	Power Ground	1
2	-	No Connection	14
3	TDCA	Transmit Data, Channel A	2
4	TSET	Transmit S.E.T.	15
5	RDCA	Received Data, Channel A	3
6	-	No Connection	16
7	RTSA	Request to Send, Channel A	4
8	RCLKA	Receiver Clock, Channel A	17
9	CTSA	Clear To Send, Channel A	5
10	-	No Connection	18
11	DSRA	Data Set Ready, Channel A	6
12	-	No Connection	19
13	GND	Power Ground	7
14	DTRA	Data Terminal Ready, Channel A	20
15	CDETA	Carrier Detect, Channel A	8
16-21		No Connection	
22	TCLKA	Transmit Clock, Channel A	24
23		No Connection	12
24		No Connection	25
25	-	GND	13
			Rear Input Channel B
26	GND	Power Ground	1
27	-	No Connection	14
28	TDCB	Transmit Data, Channel B	2
29	-	No Connection	15
30	RDCB	Received Data, Channel B	3
31	-	No Connection	16
32	RTSB	Request to Send, Channel B	4
33	RTCLKB	Rec/Transmit Clodk, Channel B	17
34	CTSB	Clear To Send, Channel B	5
35	DSRB	Data Set Ready, Channel B	18
36	-	No Connection	6
37	GND	Ground	19
38	GND	Power Ground	7
39	DTRB	Data Terminal Ready, Channel B	20
40	CDETB	Carrier Detect, Channel B	8

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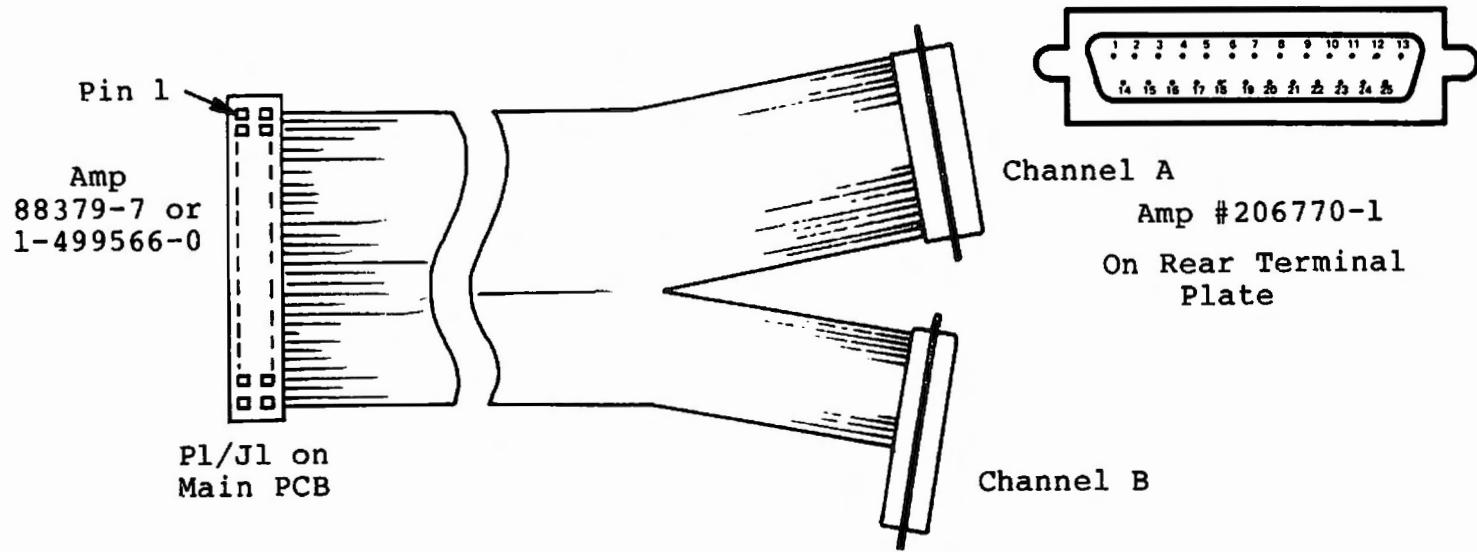
Figure 5-3. RS-232 Serial Interface Cable
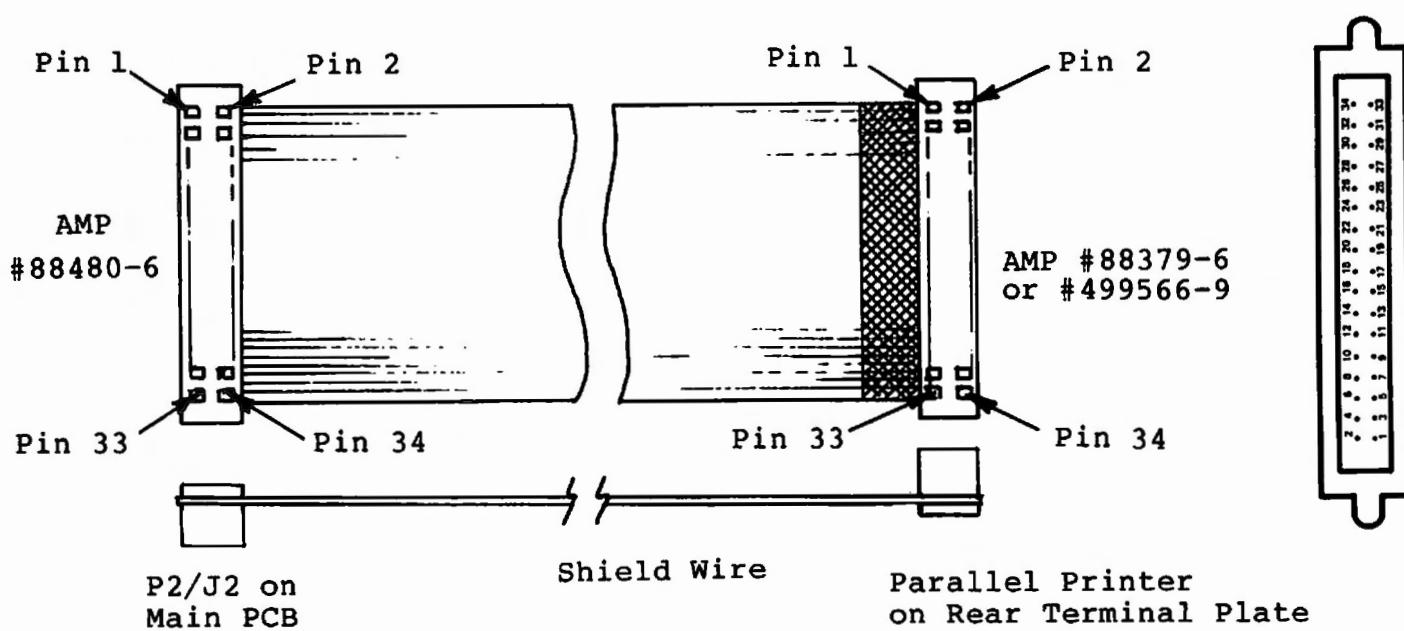
Figure 5-4. Line Printer/Parallel Output Cable

Cable Assembly 6000877, Line Printer/Parallel Output

Wiring for this cable is pin to pin from one connector to the other.

Main PCB P2/J2 to Rear Input Line Printer
===
Pin	Signal	Description
1	PSTB	Data Strobe
2	GND	Power Ground
3	PDAT0	Data Bit 0 to Printer
4	GND	Power Ground
5	PDAT1	Data Bit 1 to Printer
6	GND	Power Ground
7	PDAT2	Data Bit 2 to Printer
8	GND	Power Ground
9	PDAT3	Data Bit 3 to Printer
10	GND	Power Ground
11	PDAT4	Data Bit 4 to Printer
12	GND	Power Ground
13	PDAT5	Data Bit 5 to Printer
14	GND	Power Ground
15	PDAT6	Data Bit 6 to Printer
16	GND	Power Ground
17	PDAT7	Data Bit 7 to Printer
18	GND	Power Ground
19	PACK*	Printer Data Acknowledge
20	GND	Power Ground
21	BUSY	Printer Busy
22	GND	Power Ground
23	PE	Paper Empty
24	GND	Power Ground
25	PSEL	Printer Selected
26	PRIME	Printer Reset
27	GND	Power Ground
28	FAULT	Printer Fault
29	–	No Connection
30	–	No Connection
31	GND	Power Ground
32	–	No Connection
33	GND	Power Ground
34	–	No Connection

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Cable Assembly 6000878, FDC to Internal Drive

Wiring is pin to pin from one connector to the other.
Main PCB P3/J3 to Floppy Diskette Drive(s)
==

Pin	Name	Description
2	LOCURI*	Reduced Write Current
4,6,8	-	No Connection
10	TWOSIDI*	Two Sided Diskette Installed
12	DSKCHGI*	Drive Door Opened Since Last Select
14	SDSELI*	Side Select;low=side 0, high=side 1
16	-	No Connection
18	HLDI*	Head Load
20	IPI	Index Pulse
22	READYI	Drive Ready
24	-	No Connection
26	DS0I*	Drive Select Zero (Internal)
28	DS1I*	Drive Select One (Internal)
30	DS2E*	Drive Select Two (External)
32	DS3E*	Drive Select Three (External)
34	DIRI*	Step Direction
36	STEP1*	Step Head One Track
38	WDI*	Write Data
40	WGI*	Write Gate
42	TRK0I*	Track Zero Indication
44	WPRTI*	Write Protected Diskette
46	RDI*	Read Data
48,50	-	No Connection

*Inverted or active low. Power Grounds on odd terminals.

Internal   Internal   Main Logic PCB
Drive 0   Drive 1   P3/J3

AMP #499563-1   AMP #88379-8
                                                 or 1-4995676-2
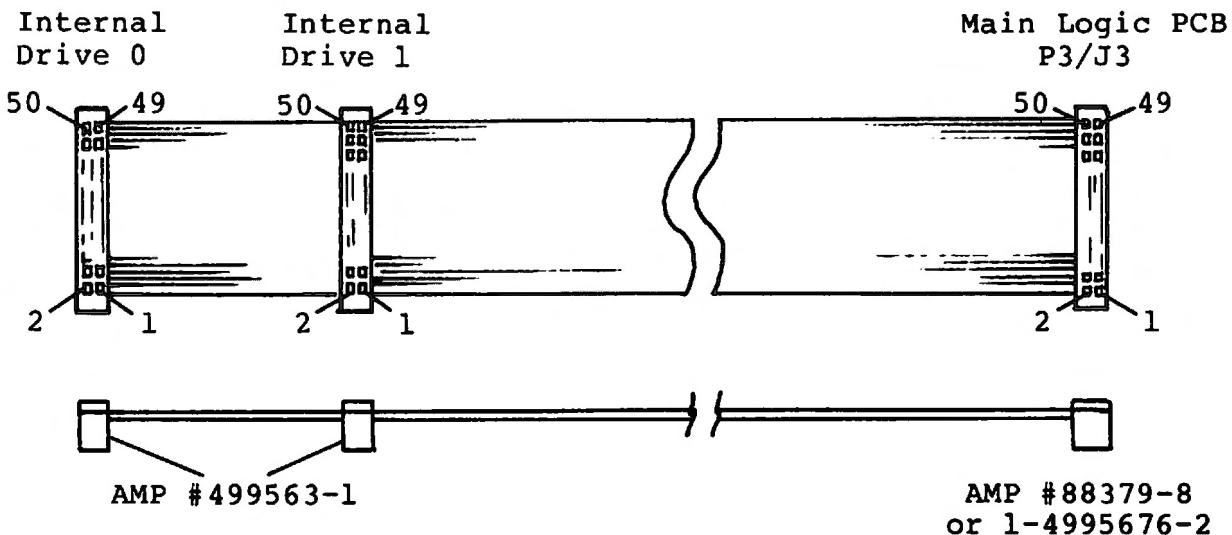
Figure 5-5. FDC to Internal Drive Cable

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Cable Assembly 6000879, Video/Keyboard PCB to Keyboard

Video/Keyboard Interface P2/J2			Keyboard Receptacle
Pin	Name	Description	Pin
1	DATA	Data from Keyboard	1
2	-	No Connection	-
3	CLOCK	Clock From Keyboard	2
4	BUSY	Busy to Keyboard	3
	-	+5 Volt	4
5	-	No Connection	-
6	GND	System Ground	5
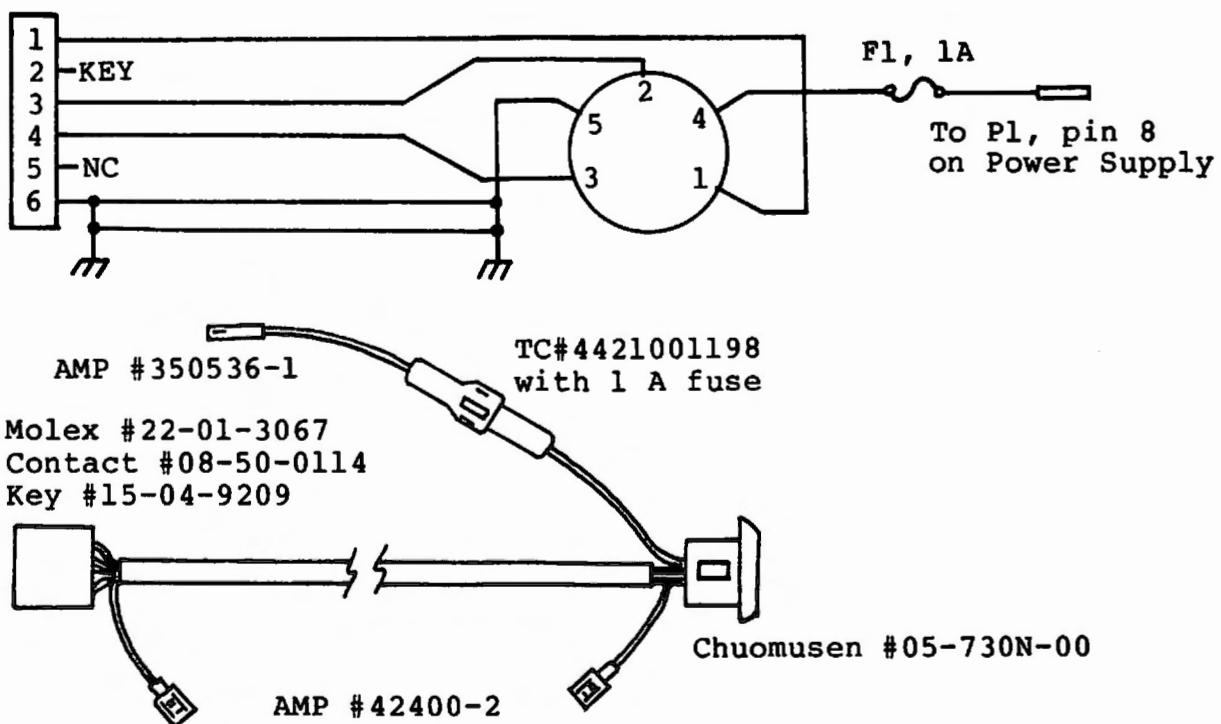
Figure 5-6. Video/Keyboard PCB to Keyboard Cable

Cable Assembly 6000880, DC Power to System

This cable supplies DC power from the Power Supply to the
Disk Drives, the CRT Monitor PCB, and the Mother Board. It
also supplies +5 volts (at pin 8) to the Keyboard via the
keyboard connector on the front panel of the Base Assembly.
This voltage is fused by a 1 ampere fuse. All wires in the
cable assembly are 18 gage except pins 9, 11, and 12, which
are 16 gage (+5 volt supply to Disk Drives and Mother Board.
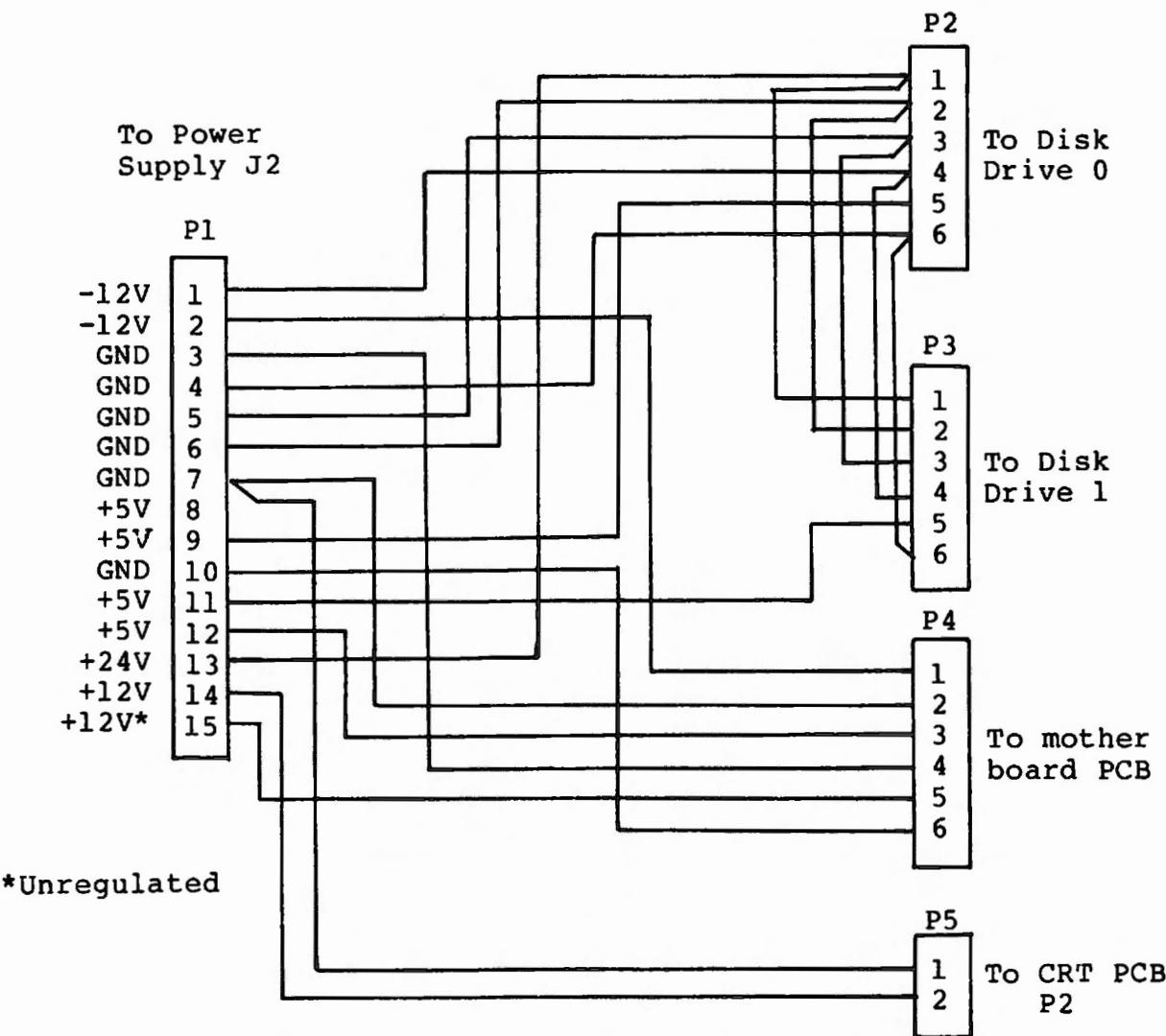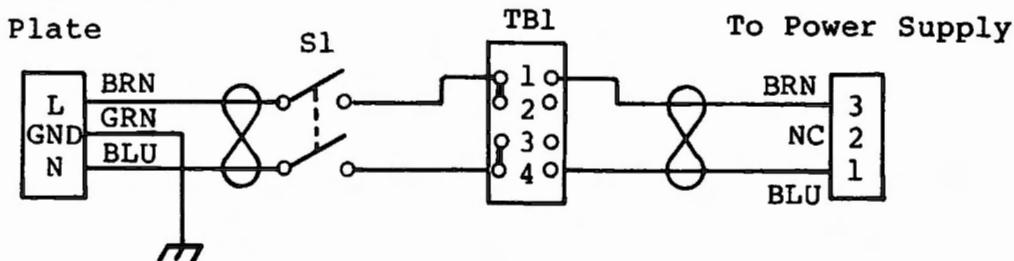
Figure 5-7.   DC Power Cable

Cable Assembly 6000885, AC Input

This cable assembly provides switched AC input from the rear
terminal panel of the Model 16B/16B-HD to the Power Supply
assembly. A terminal junction in the circuit after the
switch also supplies power to the cooling fan mounted on the
Card Cage. Input wiring is grounded through this cable by a
terminal at the rear input terminal panel. The AC wiring
from the rear panel is twisted to minimize the effect of
magnetic fields.

The terminal strip junction TB1 is mounted at the left side
of the Power Supply on the mounting bracket.

Figure 5-8. AC Input Cable

Cable Assembly 6000887, I/O Processor Board to Sound Board

This cable assembly interconnects the I/O Processor PCB to the Sound Board located at the left front corner of the Base Assembly. The cable is symmetrical and may be connected at either end to the Sound Board.
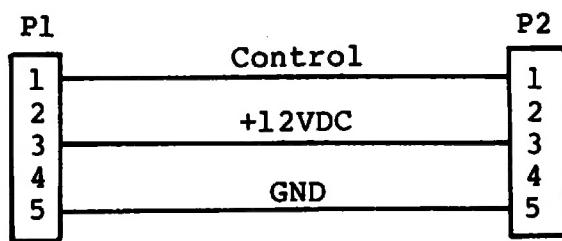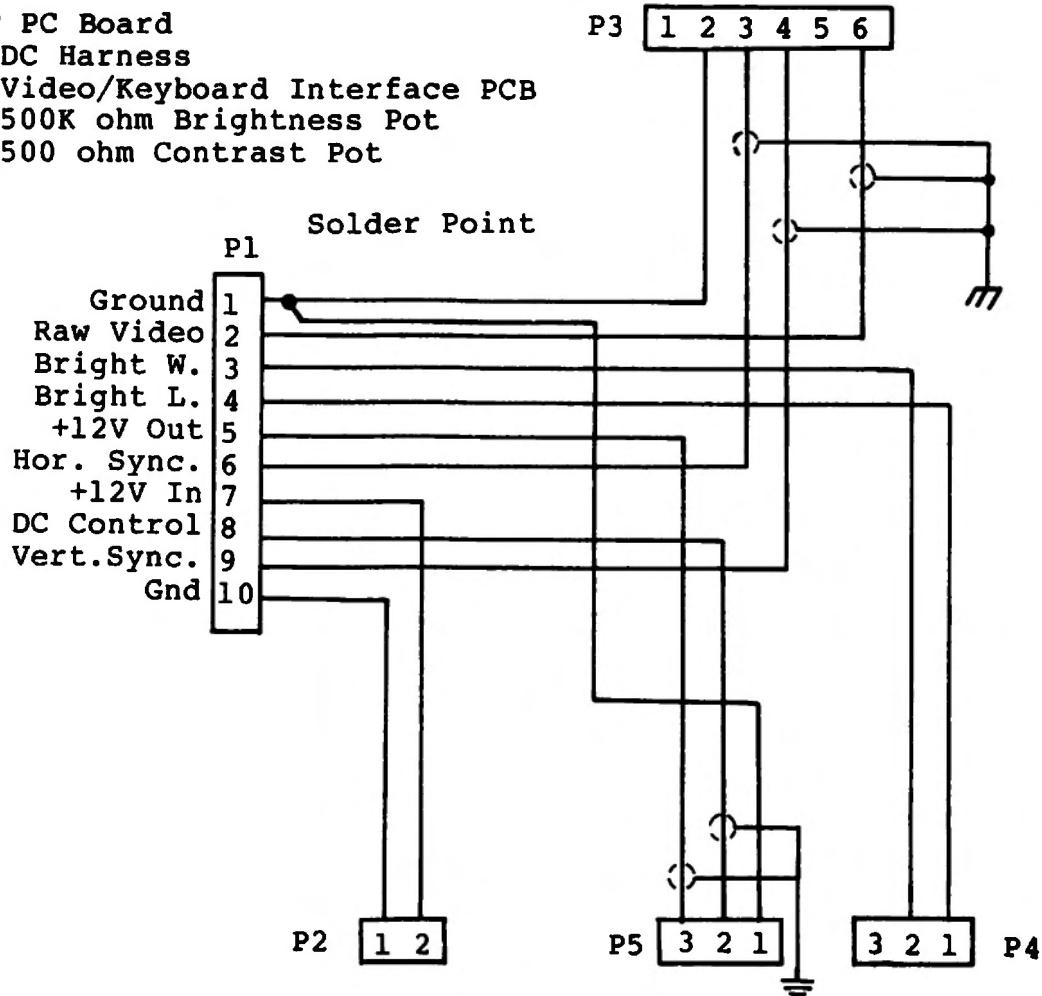
Figure 5-9. I/O Processor Board to Sound Board Cable

Harness Assembly 6000888, Video

The Video Harness contains the wiring that supplies +12 volts to the Video Monitor Assembly, wiring to the brightness and contrast controls mounted on the Cover/Bezel Assembly, and control circuitry from the Video/Keyboard Interface PCB.

P1 - CRT PC Board
P2 - To DC Harness
P3 - To Video/Keyboard Interface PCB
P4 - To 500K ohm Brightness Pot
P5 - To 500 ohm Contrast Pot

P3 | 1 2 3 4 5 6 |

Solder Point

| P1 |
Ground	1
Raw Video	2
Bright W.	3
Bright L.	4
+12V Out	5
Hor. Sync.	6
+12V In	7
DC Control	8
Vert.Sync.	9
Gnd	10

P2 | 1 2 | P5 | 3 2 1 | | 3 2 1 | P4

Figure 5-10. Video Cable

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Harness Assembly 6008046, Fan Power

The Fan Harness consists of a twisted pair that picks up AC power at the terminal strip on the Power Supply Assembly. It is controlled by the ON-OFF switch located at the left underside lip of the Model 16B/16B-HD. Routing of this cable is critical (see Figure 5-2 for routing).

Pin Designations, I/O Processor Board J0, and all Mother
Board Connector Positions

This connector accepts the Motherboard Assembly.

```
================================================================
Pin    Signal       Description
================================================================
1      68INTRQ      68000 to Z80 Interrupt Request
2      USER1        User Definable
3      GND          Power Ground
4      GND          Power Ground
5      +12V         Positive 12 Volt Power
6      +12V         Positive 12 Volt Power
7      GND          Power Ground
8      GND          Power Ground
9      +5V          Positive 5 Volt Power
10     +5V          Positive 5 Volt Power
11     INTRQ*       Maskable Interrupt Request (in)
12     NMIRQ*       Non-Maskable Interrupt Request (in)
13     IEIN         Interrupt Enable In (in)
14     IEOUT        Interrupt Enable Out (out)
15     BAKIN*       Bus Acknowledge In (in)
16     BAKOUT*      Bus Acknowledge Out (out)
17     BUSRQ*       Bus Request (in)
18     SYNC*        Z-80 M1 (indicates Op-Code Fetch) (out)
19     RD*          Read In Progress (out)
20     WR*          Write In Progress (out)
21     MEMCYC*      Z-80 MEMRQ (Memory Cycle In Progress) (out)
22     IOCYC*       Z-80 IORQ (I/O Cycle In Progress) (out)
23     A00*         Address Bit 0 Inverted (out)
24     A01*         Address Bit 1 Inverted (out)
25     A02*         Address Bit 2 Inverted (out)
26     A03*         Address Bit 3 Inverted (out)
27     A04*         Address Bit 4 Inverted (out)
28     A05*         Address Bit 5 Inverted (out)
29     A06*         Address Bit 6 Inverted (out)
30     A07*         Address Bit 7 Inverted (out)
31     A08*         Address Bit 8 Inverted (out)
32     A09*         Address Bit 9 Inverted (out)
33     A10*         Address Bit 10 Inverted (out)
34     A11*         Address Bit 11 Inverted (out)
35     A12*         Address Bit 12 Inverted (out)
36     A13*         Address Bit 13 Inverted (out)
37     A14*         Address Bit 14 Inverted (out)
38     A15*         Address Bit 15 Inverted (out)
39     RES          Reserved for System Expansion
40     DISRO*       Disable RAM Output (in)
```

Pin Designations, I/O Processor Board J0, and all Mother
Board Connector Positions

(con't)

Pin	Signal	Description
41	XFERRQ	DMA Transfer Request (in)
42	KBIRQ*	Keyboard Interrupt Request (in)
43	SELECT*	Keyboard Selected (out)
44	CLOCK	4MHz System Clock (out)
45	REFRSH*	Z-80 RAM Refresh Signal (out)
46	8MHz	Times Two System Clock (out)
47	RTC	Real Time Clock Heart Beat (30 or 60Hz)(out)
48	WAIT*	Z-80 Wait Request (in)
49	GND	Power Ground
50	GND	Power Ground
51	DAT0*	Data Bit 0 Inverted (input/output)
52	DAT1*	Data Bit 1 Inverted (input/output)
53	DAT2*	Data Bit 2 Inverted (input/output)
54	DAT3*	Data Bit 3 Inverted (input/output)
55	DAT4*	Data Bit 4 Inverted (input/output)
56	DAT5	Data Bit 5 Inverted (input/output)
57	DAT6*	Data Bit 6 Inverted (input/output)
58	DAT7*	Data Bit 7 Inverted (input/output)
59	DAT8*	Data Bit 8 Reserved for System Expansion
60	DAT9*	Data Bit 9 Reserved for System Expansion
61	DAT10	Data Bit 10 Reserved for System Expansion
62	DAT11*	Data Bit 11 Reserved for System Expansion
63	DAT12*	Data Bit 12 Reserved for System Expansion
64	DAT13*	Data Bit 13 Reserved for System Expansion
65	DAT14*	Data Bit 14 Reserved for System Expansion
66	DAT15*	Data Bit 15 Reserved for System Expansion
67	RESET*	System Reset (out)
68	HALT*	Z-80 Halt Indication (out)
69	GND	Power Ground
70	GND	Power Ground
71	+5V	Positive 5 Volt Power
72	+5V	Positive 5 Volt Power
73	GND	Power Ground
74	GND	Power Ground
75	-12V	Negative 12 Volt Power
76	-12V	Negative 12 Volt Power
77	+12V	Positive 12 Volt Power
78	+12V	Positive 12 Volt Power
79	GND	Power Ground
80	GND	Power Ground

Pin Designations, I/O Processor Board J4

Pin designations for this connector are the same as those
for cable assembly 6000878 except for the Name designations.
All references to I become E for this connector.

Example:

        LOCURI* is now LOCURE*
        TWOSIDI* is now TWOSIDE*, etc.

6/ Troubleshooting Procedures

6.1 Model 16B/16B-HD I/O Processor System

This section of the manual will guide service personnel through the system checkout procedure. The troubleshooting steps are organized in a flowchart manner. Following these steps will guide you to the faulty component or components. This procedure is intended to isolate only to the field replaceable units such as the power supply, i/o processor board, socketed ICs, etc. THe following sections describe the theory of operation and troubleshootng for the I/O Processor System. The 16-bit CPU and Memory Boards are covered in section 6.2.

6.1.1 Setup

First, disconnect the unit from the AC power scource. Next, seperate the Bezel/Cover Assembly from the Base Assembly. See Section 3 for complete instructions on disassembly. Verify the monitor remains electrically connected to the Video/Keyboard PCB and the Power Supply. Verify there are no disk(s) inserted in the drive(s). Verify that the power switch on the underside of the left lip is OFF, then connect the unit to the AC source and continue.

6.1.2 Power-on Diagnostics

When the power switch on the TRS-80 Model 16B/16B-HD is turned ON, the microprocessor starts executing the program in the BOOTSTRAP ROM. This program is divided into several sections that are executed in order if the previous section passed. These diagnostics are of a stair-step nature in that individual functions are tested before being put together to perform the complete task. This will be detailed in the following paragraphs.

1. Power ON. System RESET furnished by the hardware is applied. This causes the Z80 to begin executing program code from the BOOTSTRAP ROM at address 0000H.

2. The initilization of the system begins by disabling interrupts and deselecting all RAM memory but Page 0.

3. Initilize CRTC (CRT Controller). Specify horiziontal sync, vertical sync, enable video, select 80 character mode, white-out the entire screen.

4. Check ROM integrity by calculating checksum and
    comparing it against a value in the ROM. If it matches,
    continue. If there is a mismatch, the unit will print
    "BOOT ERROR CK" and stop.

5. Check integrity of Z80 registers by passing a specific
    bit pattern from register to register. If it passes
    unchanged, continue. If different, unit will print
    "BOOT ERROR Z8" and stop.

6. Check lower RAM (1000H to 7000H, i.e, above ROM) by
    reading a memory location, complement the data and write
    back into memory, compare memory with accumulator and
    then return memory location to original contents.

7. Flush the KEYBOARD of any/all extraneous characters due
    to power-up.

8. Initilize the HARD DISK (if available) and FLOPPY DISK
    systems. Software reset the controllers, seek track 5,
    then issue "restore" commands (set heads to track 0).

Now, the system is ready to boot the operating system. The
floppy disk controller is set to single density recording
mode. If the system is to boot from the FLOPPY DISK, the
words "INSERT DISKETTE" are printed in the middle of the
all-white screen. When a diskette is inserted and the drive
latch closed, the system begins to boot, indicated by a
"blank" screen with a blinking cursor in the middle.

The floppy disk drive controller commands the head to move
to Track 0. After a 3 second wait, a status is taken.

1. If the drive status is "busy", "not track 0", or "seek
    error", the message "BOOT ERROR DC" is displayed on the
    screen.

2. If the drive status is "not ready", the message "BOOT
    ERROR D0" is displayed.

If everything is in order, then the controller is directed
to read data from track 0 and place it in the RAM .

1. If a "record" is not found (no properly formated data
    was readable from disk), the message "BOOT ERROR TK" is
    displayed.

2. If all the records are not found, the message "BOOT
    ERROR LD" - lost data - is displayed.

3. If a CRC error occurs, the data from the floppy disk was
    read incorrectly and the message "BOOT ERROR SC" is
    displayed.

After the data is successfully loaded into RAM, then:

4. The data strings "BOOT" and "DIAG" are looked for. If
    both are found, the process continues. If these strings
    are not found, the screen will display the message "BOOT
    ERROR RS" - Not a Radio Shack diskette.

The data read in from the disk is a "diagnostic" routine
that tests the DMA, PIO functions and the RAM memory. (This
is all that is required to load the operating system using a
polled, non-interrupt method). The memory is tested from
2000H up to FFFFH. This is to determine if the system
memory size is 32k or 64k and operational. The following
error messages can occur:

       1. "BOOT ERROR DM" - DMA failed.
       2. "BOOT ERROR PI" - PIO failed.
       3. "BOOT ERROR LM" - lower memory failed.
       4. "BOOT ERROR HM" - higher memory failed.

Now if at least 32k of memory was found ok (i.e. memory
errors occured on a word boundary and above address 8000H),
the message "32K MEMORY" is displayed in the center of the
screen. If all 64K of memory responds, the message "64K
MEMORY" is displayed. Either of these messages indicates
the diagnostic has passed.

Next, the message "LOADING" or "INITIALIZING" is displayed
in the upper left corner of the screen indicating that a
"loader" routine is being read in to load the operating
system.

A word of caution. If the OS is TRSDOS 4.0 or later, then
an extra 16K of memory above 64K is required but not tested
for. As a result, if this memory

does not exist or is bad, the loading process may not be
completed and no error messages will be displayed. The
machine "hangs up" with "LOADING" message in the upper left
corner of the CRT. The extra memory required for the 4.X
operating system will be a 16K byte segment of Z80 memory
or the 16-bit CPU's memory.

A complete listing of the possible error messages that can
occur is tabulated below.

Hard Disk Errors

        HT   Timeout waiting for ready
        HC   CRC error - data
        HI   CRC error - ID
        HN   ID not found
        HA   Aborted command
        HO   Track 0 error
        HM   Data Address mark not found
        HD   Any other error

Floppy Disk Errors

        DC   FDC or drive error - busy not reset
        DO   Drive not ready
        SC   CRC error
        TK   Record not found reading track 0
        LD   Lost data on read from floppy
        RS   Not Radio Shack format disk

Other Errors

        CK   Bad ROM checksum
        Z8   CPU failure
        MF   RAM failure
        ML 01   Low RAM failure (0-3FF)
        MH 02   High RAM failure
        DM 03   DMA data failure
        DM 13   DMA - No interrupt
        DM 23   DMA - Extra interrupt
        PI 04   PIO data failure
        PI 14   PIO - No interrupt
        PI 24   PIO - Extra interrupt
        CT 05   CTC - No interrupt ch 0
        CT 15   CTC - No interrupt ch 1
        CT 25   CTC - No interrupt ch 2
        CT 45   CTC - Extra interrupt

TEST PROCEDURES

The following is a list of software routines that will thoroughly test the I/O Processor system.

1. SYSTEM - Version dated 11/29/1982, Tests SIO (serial channels A, B), PIO (printer I/F, external floppy I/F), DMA and Z80 interrupts and bus structure. Special loopback test cables required.

2. MEMII - Version 1.3. Video refresh RAM, Shadow ROM checksum, Checkerboard, Modified address and Coincidence RAM tests and Bank Select Tests.

3. AUTOTND - Version dated 07/22/1982. Thinline floppy drive tests.

4. DOVIDAL - Video alignment and centering test.

6.2   Model 16 CPU and 128K/256K Memory Board

In order to isolate a trouble in the Model 16B/16B-HD
boards, run all current Model II diagnostics. If any
failures are detected, refer to the Model II Technical
Reference Manual. If the Model 16B/16B-HD boards are
suspected as being at fault, remove the Model 16B/16B-HD CPU
and memory boards and rerun the Model II diagnostics to
verify the problem area.

If it is determined that the problem area is in the Model
16B/16B-HD MC68000 CPU or 128/256K Memory Board, use the
following troubleshooting chart for locating the trouble.

Run Diagnostics	Condition	Possible Fault	Recommended Action
16B/B-HD Memory Test (uses Z80A to test memory)	Test locked-up	Z80A to 68000 interface circuit	Check interface controller U36 and select logic
	Test locked-up	Bus arbitration circuit controller U6	Check latch U7 and bus arbitrator
	Test locked-up	Refresh logic	Check all logic in refresh circuit
	Bad RAM reported	Bad RAM	Calculate and replace bad RAM ICs
	Bad RAM reported	Z80A to MC68000 interface circuit	Check all logic in interface circuit
	Bad RAM reported	Memory board	Refer to Trouble Shooting the Model 16B/B-HD Memory Board
	No errors		Refer to Trouble Shooting the Model 16B/B-HD Memory Board

Run Diagnostics	Condition	Possible Fault	Recommended Action
Model 16B/B-HD Interrupt Test	Test locked up on software interrupt	Interrupt circuit	Check interrupt controller U15, ICs U34,40,26.
		MC68000 CPU	Replace MC68000
		Clock Logic	Check clock circuit
	Test locked up hardware interrupt	Interrupt circuit	Check interrupt controller U15 and all hardware interrupt inputs into U15
		MC68000 CPU	Replace MC68000
		Clock logic	Check clock circuit
	Software interrupt received was not interrupted generated	Interrupt controller	Replace interrupt controller U15
	Hardware interrupt received was not interrupt generated	Interrupt circuit	Check for shorts on interrupt input lines.
Model 16B/B-HD OBERROR in user Offset/Limit Test	Offset/Limit range	Check output registers	address lines for shorts
	Protected memory modified	U15, U41	Check listed ICs
	OBERROR not generated	4-bit full adders	Check U23, U24, U38

Run Diagnostics	Condition	Possible Fault	Recommended Action
Model 16B/B-HD Offset Limit Test	Random errors	I/O decoding and strobes	Check I/O and strobe circuit

Mother Board Troubleshooting

Run Diagnostics	Condition	Possible Fault	Recommended Action
Model 16B/B-HD Memory Modi-fied Address Test	Bad RAM reported	Bad RAM	Calculate and replace bad RAM ICs
		Data Buffers	Check buffers U5 - U8
		Address Buffers	Check U3, U4 and U9 for A17
		Memory Control	Check U9 and signal control logic and multiplexers

7/ Theory of Operation
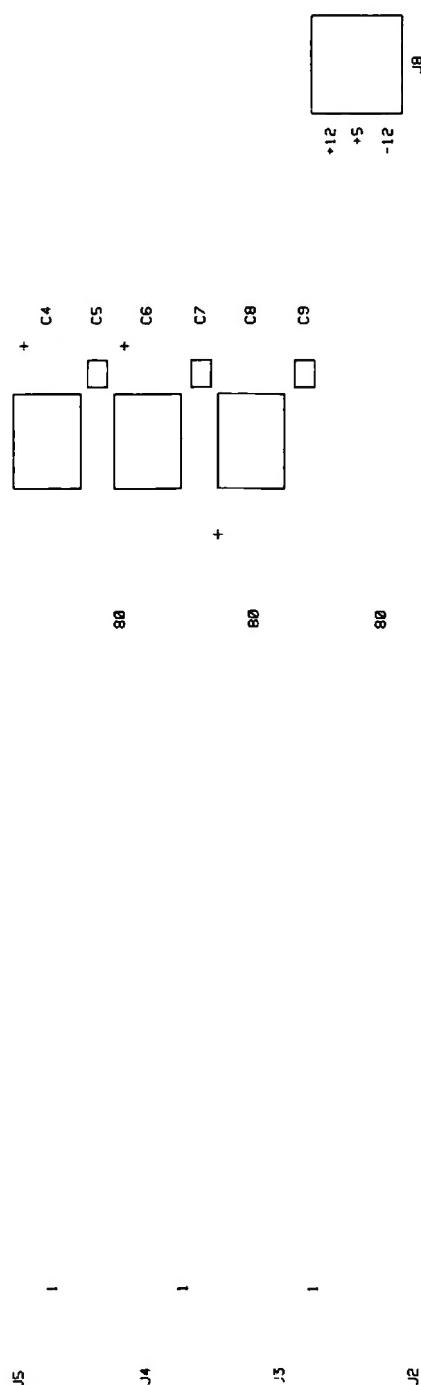
7.1 Mother Board

The mother board contains seven receptacles into which optional boards for the Model 16B/16B-HD are plugged. The connector receptacles are numbered from J1 through J7, beginning at the bottom of the board. The power supply input connector, P5, plugs into receptacle J8 at the RH side of the board.

Also included on the mother board are capacitors C4-C9, which serve to additionally filter the input voltage from the power supply. Other resistors and capacitors located at the top of the board serve as signal line terminators.
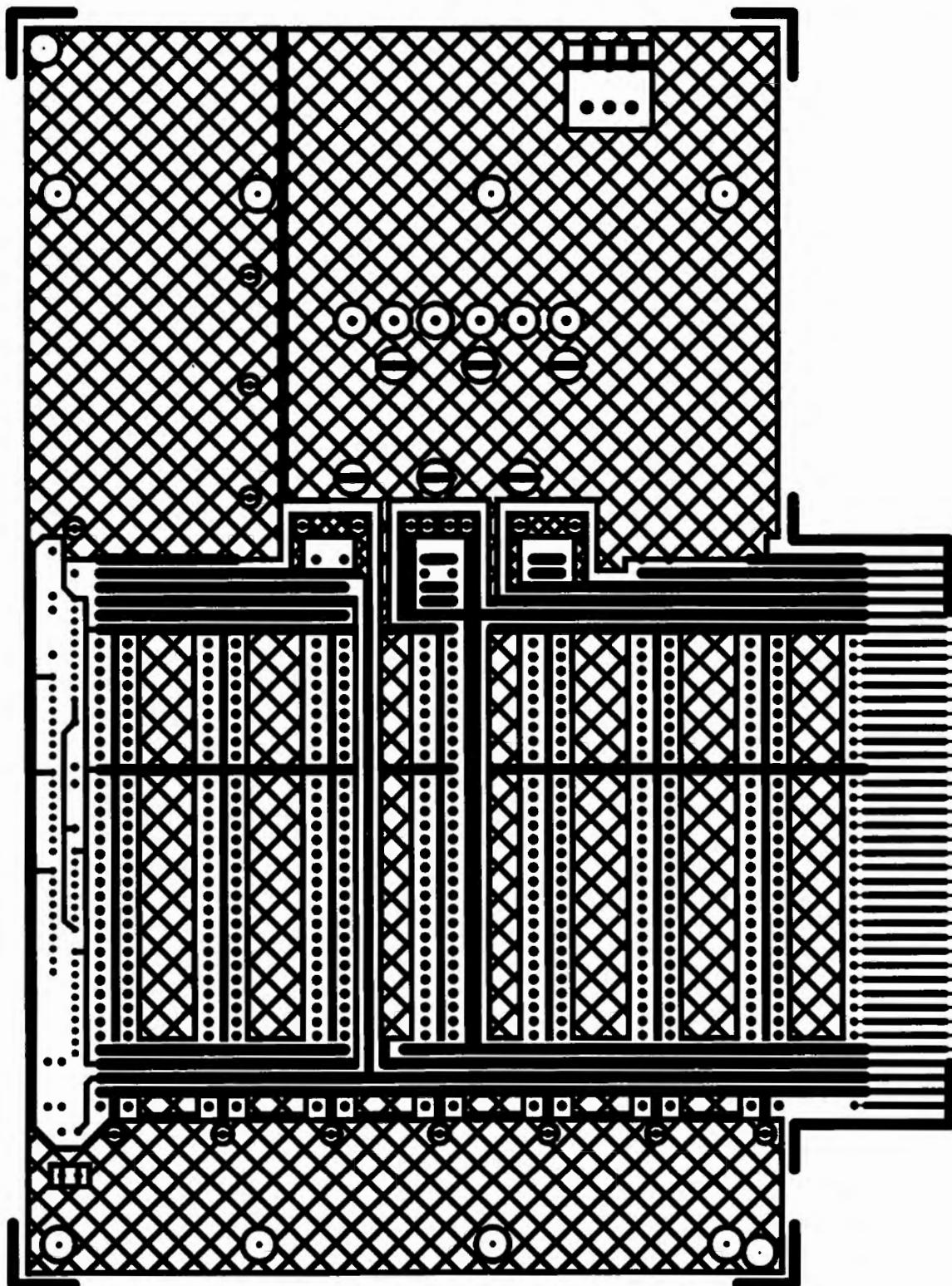
TANDY CORPORATION © 1982

MADE IN U.S.A.
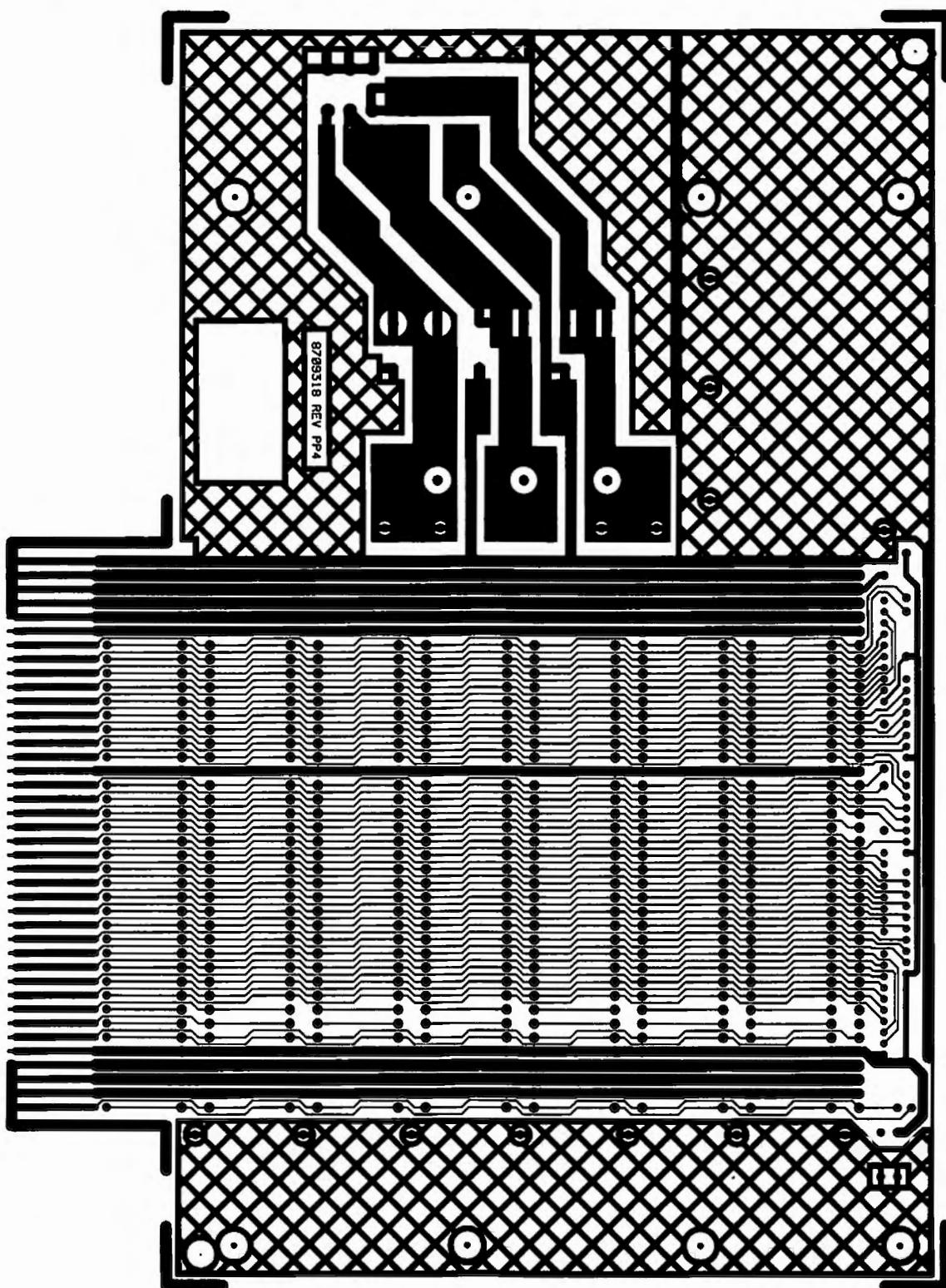
Component Location, Mother Board 8897701

Circuit Trace, Mother Board 8897701, Component Side

8709318 REV PP4

Circuit Trace, Mother Board 8897701, Solder Side

Parts List, Mother Board, 8897701

```
==================================================================
Ref No.    Description                                  Part No.
==================================================================


---        PCB, Mother Board                            8709318
```

Capacitors

Ref No.	Description	Part No.
C1	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C2	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C3	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C4	Capacitor, 470 uF, 16V, Elect, Axial	8317471
C5	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C6	Capacitor, 470 uF, 16V, Elect, Axial	8317471
C7	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C8	Capacitor, 470 uF, 16V, Elect, Axial	8317471
C9	Capacitor, 0.1 uF, 50V, Mono Axial	8374104

Connectors

Ref No.	Description	Part No.
J1	Connector, 80-pin Card Edge	8519014A
J2	Connector, 80-pin Card Edge	8519014A
J3	Connector, 80-pin Card Edge	8519014A
J4	Connector, 80-pin Card Edge	8519014A
J5	Connector, 80-pin Card Edge	8519014A
J6	Connector, 80-pin Card Edge	8519014A
J7	Connector, 80-pin Card Edge	8519014A
J8	Connector, 6-pin Power	8519015

Resistors

Ref No.	Description	Part No.
R1	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R2	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R3	Res. Network, 220/330 ohm, 10-pin, SIP	8290019
R4	Res. Network, 220/330 ohm, 10-pin, SIP	8290019
R5	Res. Network, 220/330 ohm, 8-pin, SIP	8290019
R6	Res. Network, 220/330 ohm, 8-pin, SIP	8290019
R7	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R8	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R9	Res. Network, 220/330 ohm, 8-pin, SIP	8290019
R10	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R11	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R12	Res. Network, 220/330 ohm, 10-pin, SIP	8290019

7.2 MC68000 CPU Board

The theory of operation for the MC68000 board has been
divided into several major sections, each corresponding to a
logical unit of LSI, MSI, and SSI parts on the CPU board.
They are as follows:

     Central Processing Unit (CPU)
     Interrupt Logic
     Z80A to MC68000 Memory Interface Circuitry
     Memory Management Circuitry
     Bus Arbitration Logic
     Data Transfer Acknowledge Logic
     MC68000 I/O Decoding and Strobes
     Clock Logic
     Refresh Logic
     Bus Error Logic

Note: The terms "assertion" and "negation" are used to
avoid confusion when talking about active-high or active-low
signals. "Assert" or "assertion" is used to indicate a true
or active state, regardless of its high or low potential.
"Negate" or "negation" indicates a false or inactive state.

7.2.1 Central Processing Unit (CPU)

The Model 16B/16B-HD CPU board uses the Motorola MC68000,
which contains 16 data lines, 23 address lines, and 20
control lines.

1. Data Lines

The data lines (KD0-KD15) are interfaced to the bus via
tranceivers U12 and U13 (AMD 8303s). When high, the CD
control line (pin 9) on the transceivers tri-states the data
bus. This signal is driven by Bus Grant Acknowledge
(BGACK), which indicates that a device other than the
MC68000 CPU is bus master.

The TR control line (pin 11 on the 8303) controls the
direction the transceiver is pointing and is driven by Data
Bus Transmit/Receive (DBTR). (See the upper left-hand
corner of sheet 3 of the CPU schematic.) The active-low
output DBTR from U9 pin 13 enables the data receivers during
an off-board interrupt acknowledge sequence (INTAKL6*) or
during a read from external memory.

The active-high state of DBTR enables the data drivers. It
follows, therefore, that the data receivers are disabled
when:

> A read or write is in progress from the Interrupt
>   Controller chip (INTCS*)
> A board interrupt acknowledge sequence is in progress
>   (PRIORINTAK*)
> A write to external memory (R/W*) occurs

It should be noted that the CD control line overrides the TR
control line, and that both drivers and receivers are
disabled (tri-stated) if BGACK is asserted.

2. Address Lines

The MC68000 address lines are interfaced to the address bus
via tranceivers U11, U28, and U30, which are the same type
used for the data lines. The CD control line is connected
directly to ground, which always enables address lines
KA1-KA11, KA12-KA19, and KA20-KA23 to the address bus unless
BGACK* is active. The direction control line (TR) is
switched by BGACK*, which indicates who has bus mastership.
If the MC68000 CPU is bus master, then BGACK* is negated and
the address lines are driven onto the bus. If an external
device is bus master, BGACK* will be asserted and the
address contained on the bus will be gated onto the CPU
address lines.

The CPU control lines may be divided into six major groups.
These are:

> Memory Access Control Lines
> Bus Arbitration Lines
> Interrupt Priority Lines
> Function Code Lines
> MC68000 Peripheral Interface Lines
> System Control Lines

Memory Access Control Lines

The memory access control lines include Address Strobe
(AS*), Lower Data Strobe (LDS*), Upper Data Strobe (UDS*),
Read/Write (R/W*), and Data Transfer Acknowledge (DTACK*).
AS* indicates there is a valid address on the address lines
of the MC68000 CPU and it is connected directly to the
MC68000 subsystem devices.

The Bus AS* (BAS*) depends on the state of the MC68000 CPU.
When the processor is in the user state, a delayed AS* is
required to allow the extra time needed for address checking
of the memory management unit. The logic described on sheet
3 of the CPU schematic (lower left-hand corner) steers AS*
or MAS (the delayed AS* for user state) to GAS*, which is
interfaced to the bus by U14.

LDS*, UDS*, and R/W* are directly interfaced to the bus
using non-inverting transceiver U14 (AMD8104). The control
lines are the same as described for the AMD 8303 (the
address and data transceivers). The TR input for U14 is
pulled up, which always enables the drivers. The CD input
is controlled by BGACK, which will disable (tri-state) the
drivers when an external device is bus master.

LDS* indicates that data bits BD0-BD7 are being accessed,
and UDS* indicates that data bits BD8-BD15 are being
accessed. If both are asserted at the same time, all 16
data bits are accessed. R/W* indicates whether the data bus
transfer is a read or write cycle. An active high indicates
a read cycle and an active low indicates a write.

Data Transfer Acknowledge (DTACK*) is the asynchronous
handshake signal used by memory and peripheral devices to
indicate that a bus cycle has been completed. DTACK* is
connected directly to the bus and becomes BDTACK*. For more
details, see Paragraph 7.1.6 Data Transfer Acknowledge
Logic.

Bus Arbitration Lines

The bus arbitration lines consist of Bus Request (BR*), Bus
Grant (BG*), and Bus Grant Acknowledge (BGACK*). BR* and
BGACK* are inputs to the MC68000 CPU and BG* is an output.
These signals are used to determine which device will be the
next bus master.

All three signals connect with the bus arbitration
controller chip U6. This chip interfaces with the bus to
provide four levels of bus requests and grants. For more
details, see Paragraph 7.1.5 Bus Arbitration Logic.

Interrupt Priority Lines

The Interrupt Priority Lines (IPL0*-IPL2*) are CPU inputs
that indicate the encoded priority of the
interrupt-requesting device. The highest priority is Level
7. Level 0 indicates that interrupts are not requested.

IPL0*-IPL2* are connected to the outputs of an 8-to-3 line priority encoder (U40) whose inputs are the interrupt sources. U40 is always enabled with pin 5 (EI) grounded. Level 5 interrupt is the only level currently used.

For more details on interrupt operation, see Paragraph 7.1.2 Interrupt Logic.

Function Code Lines

Function Code Lines (FC0, FC1, and FC2) are outputs from the processor chip that feed a 3-to-8 decoder (U34). U34 is used to detect accesses to User Space (either code or data) or to decode the Interrupt Acknowledge sequence (INTAK*).

Bus grant acknowledge (BGACK) disables the decorder to prevent the memory management unit from providing the memory protect function during bus cycles under external control (i.e., Z80A, CPU, or DMA transfers).

MC6800 Peripheral Interface Lines

The MC6800 Peripheral Interface Lines (E, VMA*, and VPA*) allow the CPU to interface easily to MC6800-type devices. The outputs (E and VMA*) are interfaced to the 16-bit bus. with a bidirectional transceiver U14. U14's enable is controlled by the BGACK signal.

The direction of the transciever is fixed to transmit to the bus. If BGACK is active, the transceiver is disabled and the outputs are tri-stated. Another device is then allowed to drive the bus control lines (i.e., Z80A, CPU, or DMA). The MC6800 Peripheral Interface lines are not currently implemented in the Model 16B/16B-HD operation.

System Control Lines

The System Clock input (CLK) to the MC68000 CPU is driven by a 6 MHz output of the clock logic (PCLOCK). The RESET*, HALT*, and BERR* lines are connected directly to the MC8600 bus. These lines are driven in a wire-OR fashion by open collector inverter U33. RESET* and HALT* are directly controlled by the Z80A CPU. This is done by setting or resetting latched bits in a special Z80A I/O port.

RESET* is a bidirectional signal allowing the Z80A I/O port latch or the MC68000 CPU to reset the MC68000 subsystem. For the MC68000 CPU to recognize the assertion of RESET*, HALT* must be asserted at the same time.

HALT* is also a bidirectional signal. When the Z80A I/O
port latch asserts HALT*, the MC68000 CPU will stop at the
end of the current bus cycle. If HALT* is asserted by the
MC68000 CPU, it indicates the processor has stopped, as in
the case of a double bus fault. See Paragraph 7.1.3 Z80A to
MC68000 Memory Interface Circuitry for more information.

Assertion of Bus Error (BERR*) to the MC68000 CPU indicates
that a major error has occurred during the current bus
cycle.

Errors can be a result of:

    A device that does not respond with BDTACK*.
    An attempt by the user to access memory outside the
        extents defined by the memory management unit.
    No interrupt vector received during an interrupt
        acknowledge sequence.

See Paragraph 7.2.10 Bus Error Logic for more information.

7.2.2   Interrupt Logic

The Interrupt Control function for the MC68000 subsystem is
implemented with an AM9519 interrupt controller. A single
AM9519 (U15) manages up to eight maskable interrupt request
inputs, resolves priorities, and supplies the vector number
response to the MC68000 CPU at interrupt acknowledge time.
When the AM9519 controller receives an unmasked interrupt
request, it issues a group interrupt request to the MC68000
CPU. When the interrupt is acknowledged, the controller
outputs the pre-programmed vector number corresponding to
the highest-priority unmasked interrupt request.

Operating Mode Register

The mode register in the AM9519 specifies the various
combinations of operating options that the programmer may
use. The following is a list of the operating options used
by the system.

Bit Number	Option
0	Priority Mode
1	Vector Selection
2	Interrupt Mode
3	GINT Polarity
4	IREQ Polarity
5	Selects internal register to be read on subsequent read operation
6	Selects internal register to be read on subsequent read operation
7	Master mask bit that enables or dis-ables all interrupts without modifying the interrupt mask register

Interrupt Request Inputs

Table 7-1 lists, in order from the highest to the lowest
priority, the interrupt inputs implemented in the MC68000
subsystem.

For more information, see the AM9519 data sheet section in
the AM9500 Peripheral Products Guide published by Advanced
Micro Devices.

7.2.3   Z80A to MC68000 Memory Interface Circuitry

Communication between the two CPUs is accomplished with the
Z80A CPU initiating interrupts to the MC68000, indicating
I/O completion, etc. The Z80A CPU can periodically poll an
MC68000 memory location to recognize requests for service
from the MC68000.

Optionally, the MC68000 can generate an interrupt to the
Z80A by accessing a decoded MC68000 memory location (not
available on Model II/16 upgrades). Once a request for
service has been recognized by the Z80A CPU, a descriptor
block is read into Z80A memory from MC68000 memory to
determine the specific service required.

Interrupt	Description	Vector Location
CONT4*	Initiated by the Z80A	234H
CONT5*	Initiated by the Z80A	238H
CONT6*	Initiated by the Z80A	23CH
ADERR*	Address error, generated by the memory management unit when a user attempts memory access outside the defined range.	240H
TIMERRI*	Time-out error, generated when no DTACK is received with the MC68000 as the bus master.	244H
TMERRE*	Time-out error, generated when no DTACK is received and the MC68000 is not the bus master.	248H
IPER*	Parity error, generated on a memory parity error when the MC68000 is the bus master.	24CH
EPER*	Parity error, generated on a memory parity error when the MC68000 is not the bus master.	250H

Table 7-1. Interrupt Inputs

Prior to attempting a memory transfer by the Z80A subsystem to or from the MC68000 memory, all Z80A memory pages must be deselected by resetting the lower nibble of port 0FFH. This implies that certain precautions must be observed. The stack and control program must be located in the lower 32K of the Z80A address space, since page zero cannot be disabled.

Additionally, two control ports must be initialized to
determine the addresses involved and the mode of the
transfer.

The two ports are described in the tables and text below.

Upper Address Latch (port 0DFH)

Description: Output only, latches the upper address bits
(A22-A15) for a Z80A transfer to or from MC68000 memory.

Data Bit	Function
7	A22
6	A21
5	A20
4	A19
3	A18
2	A17
1	A16
0	A15

Transfer Control Latch (port 0DEH)

Description: Output only, latches one address bit and seven
control outputs.

Data Bit	Function
7	A14
6	CONT6
5	CONT5
4	CONT4
3	RESET
2	HALT
1	CONT1
0	CONT0

Details of Control Outputs (port 0DEH)

CONT0
```
    0   =   If  Z80A   A0  =   0   asserts UDS*
            If  Z80A   A0  =   1   asserts LDS*
    1   =   If  Z80A   A0  =   0   asserts LDS*
            If  Z80A   A0  =   1   asserts UDS*
```

CONT1
```
    0   =   Enables Z80A to initiate memory transfers to or
            from MC68000 memory space
    1   =   Transfers by Z80A disabled
```

HALT
```
    0   =   MC68000 processor not halted
    1   =   Halts MC68000 processor
```

RESET
```
    0   =   RESET negated
    1   =   Asserts RESET to MC68000 processor
```

CONT4
```
    Interrupt to MC68000 processor
    Transition generates interrupt
```

CONT5
```
    Interrupt to MC68000 processor
    Transition generates interrupt
```

CONT6
```
    Interrupt to MC68000 processor
    Transition generates interrupt
```

7.2.4 Memory Management Circuitry

A fast memory management scheme provides two sets of offset
and limit registers. The offset and limit registers define
the relocation base address and the absolute limit address
allowed by the current user program. Providing two sets of
limit and offset registers allows all user programs to
access a common kernel of the operating system or the
run-time package.

Memory is allocated in 4K byte increments and relocation is
done on 4K byte boundaries. Memory management is not active
in system mode or during memory transfers initiated by bus
masters other than the MC68000 CPU.

Write protection for the memory outside a user's partition
is provided. Accesses outside of the user's defined
partition result in the generation of a bus error exception.
An interrupt can also be generated if the interrupt
controller is properly initialized.

There are two things that cause the generation of a bus
error:

    The user addresses outside his partition
    A bus time-out occurs

A bus time-out results when nonexistent memory or I/O
accesses are attempted. The source of the bus error can be
determined by reading the status register of the interrupt
controller.

The hardware that accomplishes the memory management
function works as described in the following paragraphs.

The MC68000 processor address bits A12 through A19 are added
to the 8-bit value that is stored in the active offset
register. The result of this addition is the effective
address that is presented to the address bus.

The effective address is compared to the 8-bit value that is
stored in the active limit register. If the effective
address is larger than the contents of the active limit
register, or if the addition results in a carry overflow
from the adder, a bus error is generated.

The MC68000 processor address A23 determines which set of
offset and limit registers are used. If A23 is high, then
offset and limit registers two will be active. If A23 is
low, then offset and limit registers one will be active.

Each of the two extents is implemented with an offset
register and a limit register, which are 74LS374 8-bit
D-type registers. The 8-bit value in the offset register is
added to the eight processor address lines (KA12 to KA19) to
form User Extent Address lines (UEA12 to UEA19).

The effective address is then compared with the value in the
limit register. If the EA is greater than the limit, an
out-of-bounds error is generated.

A carry out of the adder (LS283) also generates an OBERROR.
If OBERROR occurs when MMA and MAS are active, then an
Address Error is generated (ADERR). This signal (ADERR) is
one of the interrupt sources.

The source of the user extent address is selected by A23 and the signal MMA (memory management active) determines which set of buffers (U31 or U30) drive the address bus. If MMA is high, the user effective address is driven to the bus by U31. If MMA is low, the addresses directly from the 68000 are driven to the bus by U30.

For a one-megabyte memory space, eight bits of memory management allow 4K minimum granule sizes to be protected.

Note: KA22 asserted selects the I/O device address space. The I/O device strobe generation logic generates the I/O strobes necessary to communicate with interrupt controller and memory management registers by decoding KA21 and KA22.

7.2.5 Bus Arbitration Logic

Bus arbitration allows other devices capable of being bus master to request, be granted, and acknowledge bus mastership. The bus arbitration sequence is as follows:

1. The device asserts a Bus Request (BR*).

2. The MC68000 CPU asserts a Bus Grant (BG*) to indicate that the bus will be released at the end of the current bus cycle.

3. The device acknowledges the bus grant by asserting a Bus Grant Acknowledge (BGACK*) and assuming bus mastership. A requesting device should not assert BGACK* or assume bus mastership until the following conditions are met:

    A bus grant has been received

    BAS* has been negated, indicating that the CPU has completed the current bus cycle

    BDTACK* has been negated, indicating that memory or peripherals are not using the bus

    BGACK* has been negated, indicating that no other device still has bus mastership.

4. The device negates the Bus Request (BR*).

The bus arbitration control is performed by the bus arbitration controller chip U6. In addition to controlling the bus arbitration sequence, U6 manages four levels of bus requests and grants.

The sources for the four levels are Refresh Request
(REFRQ*), Bus Request 2 (BR2*), Bus Request 1 (BR1*), and
Bus Request 0 (BR0*), with REFRQ* having the highest
priority and BR0* the lowest. The bus requests are
pre-latched by a quad D-type latch U7 clocked at a 12 MHz
rate.

The bus request is latched at a Q output of U7 and asserts a
bus request input to U6 (pins 3-6). The bus arbitration
controller will, in turn, assert BR* to the MC68000 CPU.
After some internal synchronization time, the MC68000 will
assert BG* to U6, which indicates that it will release the
bus at the end of the current bus cycle.

When the current bus cycle has ended (i.e., when BAS* and
BDTACK* are negated), U6 will assert a bus grant to the
requesting device with the highest priority. The bus
arbitration controller U6 will also assert BGACK* and negate
BR* to the MC68000 CPU. BGACK* is inverted by 1/6th of U2
and both signals are used to indicate to other
bus-controlling circuitry that an external device has become
bus master.

The MC68000 CPU will negate BG* and wait until BGACK* has
been negated before reassuming bus mastership. The
requesting device can then assume bus mastership and perform
any data transfers needed.

When the current bus master is finished, it negates the bus
request to the bus arbitration controller through U7. Then,
if there is a bus request still pending, a bus grant will be
asserted to the next requesting device and BGACK* will
remain asserted until all pending bus requests have been
satisfied.

If no bus requests are pending, the bus arbitration
controller will negate BGACK* and allow the MC68000 CPU to
assume bus mastership. See Figure 7-1 for the timing
relationships of this circuit.
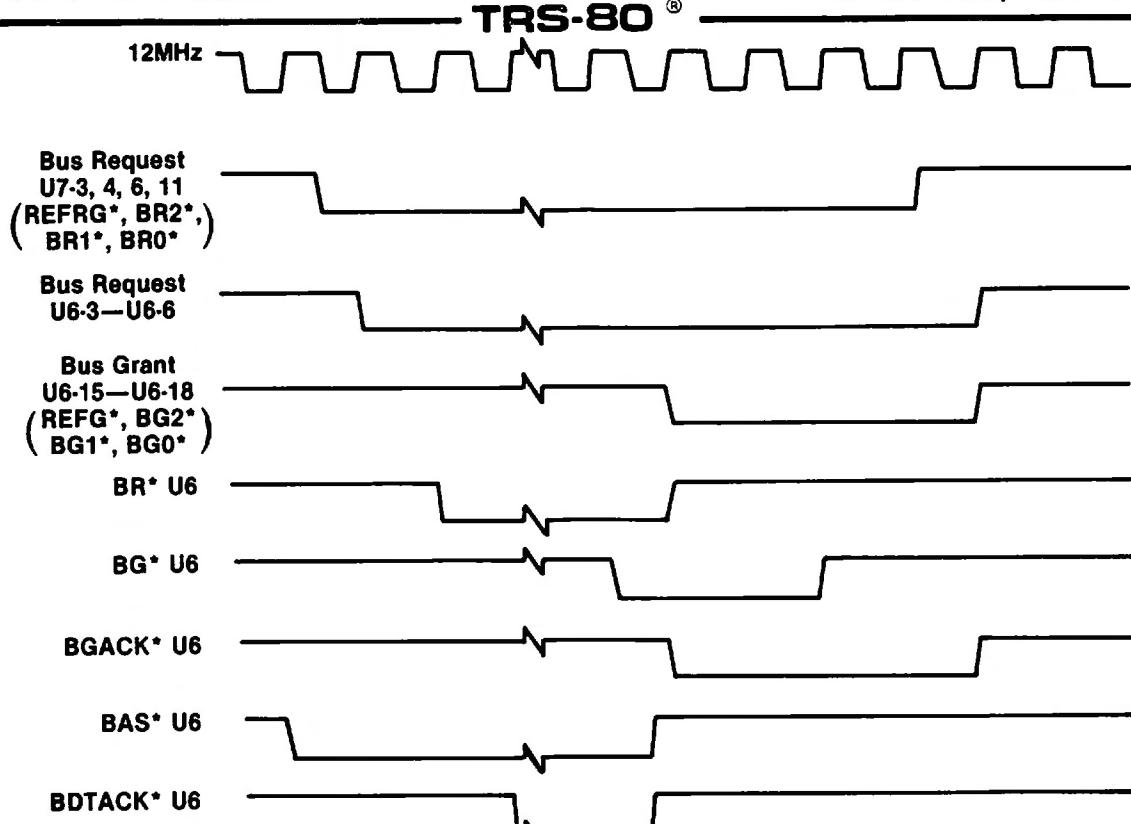
Figure 7-1. Bus Arbitration Circuit Timing

7.2.6 Data Transfer Acknowledge Logic

Data Transfer Acknowledge (DTACK*) is the asynchronous
handshake signal used by memory and peripheral devices to
complete a bus cycle. When BDTACK* is asserted during a
read bus cycle, the data is latched into the MC68000 CPU and
the bus cycle is terminated. Assertion of BDTACK* during a
write cycle causes the MC68000 CPU to terminate the bus
cycle.
There are two main sources of BDTACK* from the CPU's point
of view:

> Onboard devices, such as the AM9519 interrupt controller
> chip and the memory management registers.

> Offboard devices, such as memory or peripherals
> connected to the MC68000 bus.

Two signals can trigger the generation of an onboard BDTACK*
-- MIIDTACK* and RIP*.

If MIIDTACK* is asserted, a read or write to an onboard
device is in progress.

If RIP* is asserted, an interrupt acknowledge cycle is in
progress and the interrupt vector data is valid from the
interrupt controller chip U15.

MIIDTACK* and RIP* are ORed together at U8 pins 9 and 10 and
the resultant output at U8 pin 8 clocks a low into the D
flip-flop (1/2 of U49). This results in a high output at
U49 pin 6, which is inverted by 1/6th of U33 and used to
drive BDTACK* line low.

Address Strobe (AS) sets the flip-flop and negates BDTACK*
for the next bus cycle. Figure 7-2 shows the timing
relationships for onboard BDTACK* generation.
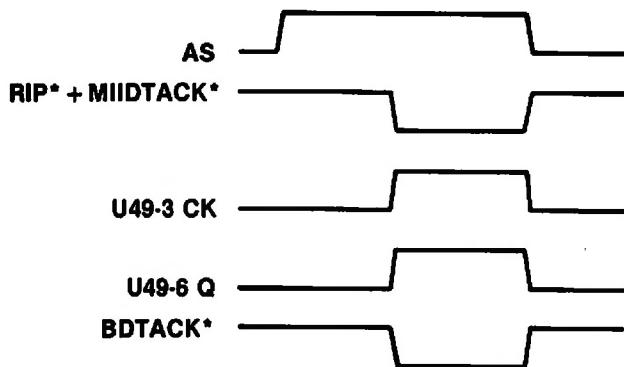
Figure 7-2. Onboard BDTACK Generation

Generation of BDTACK* from offboard devices is only from the
MC68000 memory boards. BDTACK* being asserted from an
MC68000 memory board indicates that the data transfer has
been completed.

During a read cycle, BDTACK* indicates that the data from
the data bus has been written into memory and has completed
the transfer. During a write cycle, BDTACK* indicates that
the data requested is present on the data bus. For more
details on memory BDTACK* generation, refer to Paragraph 7.2
Memory Board Theory of Operation.

BDTACK* is also generated for the time-out error logic
located in the middle and left of sheet 2 of the MC68000 CPU
schematic. BDTACK* is driven by 1/6th of U33 and is
generated by the Q output of U21 pin 9.

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The Q output of U21 pin 9 (TMERR) indicates that a
non-responding device has been accessed and a time-out error
has occurred.

7.2.7 MC68000 I/O Decoding and Strobes

The I/O devices in the MC68000 subsystem are memory-mapped
and consist of the:

> Interrupt controller chip
> Memory management registers
> Z80A interrupt (NOT implemented in the Model II
>   upgrades)

All other I/O devices and peripherals in the Model
16B/16B-HD are still controlled by the Z80A CPU.

The main I/O decoding is managed by chip U48, which is the
I/O controller. The I/O controller interfaces the MC68000
CPU to the MC68000 subsystem I/O devices, thereby providing
all necessary signals.

The right and top of sheet 2 of the MC68000 CPU schematic
should be referenced unless otherwise noted. The current
I/O devices are mapped at address locations 7800D0H to
7800D7H. Address bits KA20-KA22 are decoded by a 3 input
AND gate (1/3 of U10) that generates the signal VMIIAD.

VMIIAD and mIO (KA19) are connected to the I/O controller
and generate the I/O signals during access to the memory
space 780000H to 78FFFFH. When an I/O access is executed,
VMIIAD, mIO, AS*, and the 8 MHz CK (clock) start a 4 bit
internal counter. This counter is used to time the
assertion of BIORQ*, BRD*, and BWR*, and MIIDTACK*.

R/W* determines the assertion of BRD* or BWR*. BIORQ* is
used to enable a 1 of 8 decoder U41 that decodes address
bits KA1-KA7. Refer to the bottom right-hand corner of
sheet 3 of the MC68000 CPU schematic.

KA4, KA6, and KA7 are decoded by a 3-input AND gate, 1/3rd
of U27, and the output is connected to the active-high
enable input U41 pin 6. KA5 enables the third enable input
U41 pin 4 when an active low occurs.

KA1-KA3 are decoded to determine the output of U32 that
selects the I/O device. Table 7-2 outlines the
memory-mapped I/O locations currently implemented in the
MC68000 subsystem. See Figure 7-3 for the timing
relationships of the I/O controller U48.

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```
============================================================
Address      Function
------------------------------------------------------------
7800D0       Interrupt controller data register
7800D1       Interrupt controller command register

7800D2       Limit register two
7800D3       Offset register two

7800D4       Limit register one
7800D5       Offset register one

7800D6       Interrupt request to Z80A
7800D7       Interrupt request to Z80A
============================================================
```

Table 7-2. Memory-Mapped I/O Locations

Figure 7-3. I/O Controller Timing
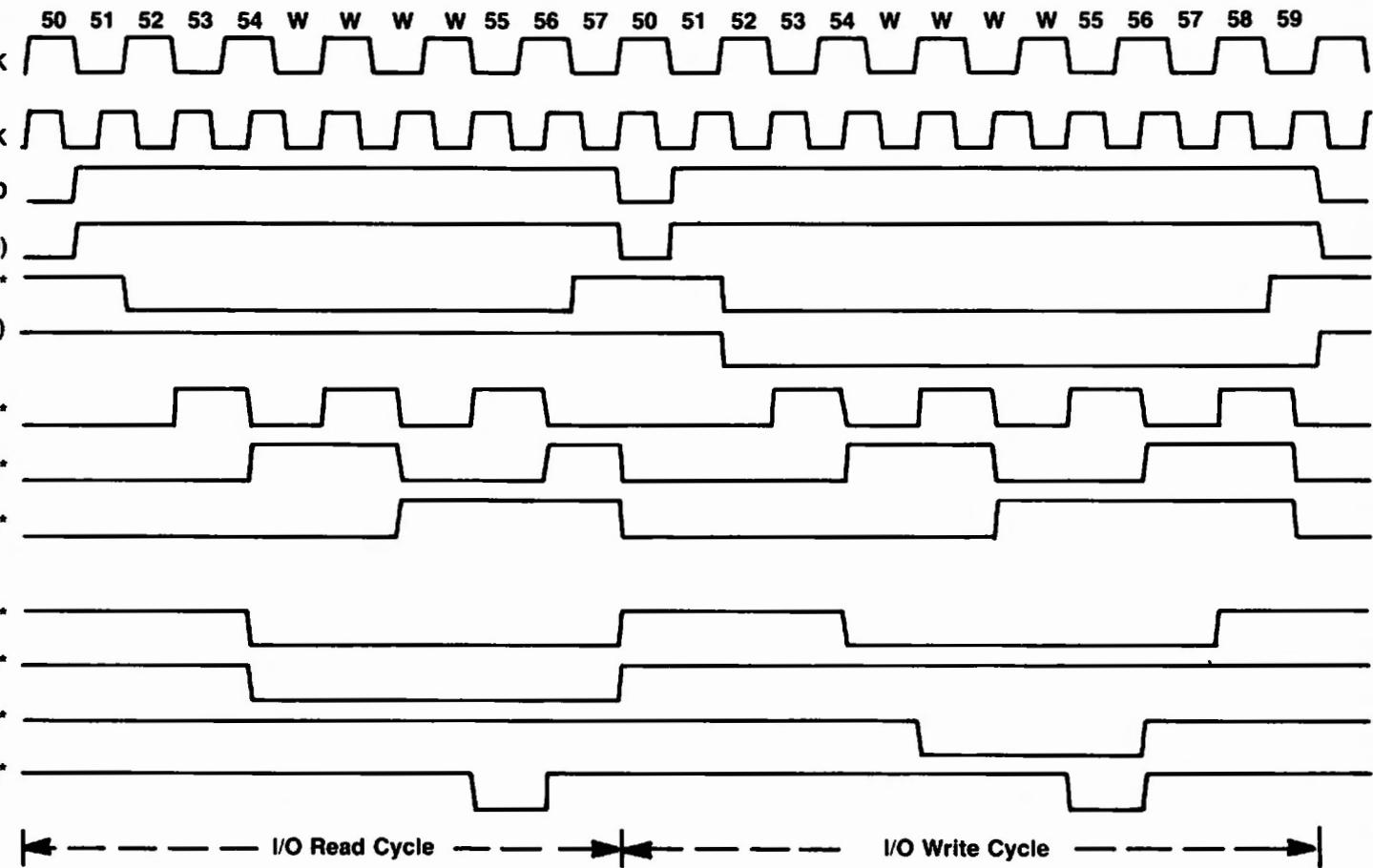
Figure 7-3. I/O Controller Timing

Table 7-3 outlines the memory map of the MC68000 subsystem:

SYSTEM RAM

Start Address	End Address	Total Bytes
Total Available RAM Space		
000000	6FFFFF	7 MEG
One 128K Memory Board Installed		
000000	01FFFF	128K
Two 128K (or one 256K) Memory Boards Installed		
000000	03FFFF	256K
One 256K and One 128K Memory Board Installed		
000000	05FFFF	384K
Two 256K Memory Boards Installed		
000000	07FFFF	512K
Three 256K Memory Boards Installed		
000000	09FFFF	768K

Table 7-3. Memory Map of the MC68000 Subsystem

7.2.8 Clock Logic

The clock logic provides the clocks and timing for the MC68000 subsystem. The heart of the clock logic is a 24 MHz crystal oscillator. (See the top left-hand corner of sheet 2 of the MC68000 CPU schematic.) The 24 MHz output of Y1 is input to pin 1 of U53. U53 is a PAL device that is programmed to: divide the 24 MHz input by 2 to produce a 12 MHz output at U53 pin 17; divide the 12 MHz output by 2 to produce a 6 MHz output at U53 pin 16; divide the 24 MHz by 3 to produce an 8 MHz output at U53 pin 19; and divide the 8 MHz output by 2 to produce a 4 MHz output at U53 pin 15. These various clock signals are used to time the operation of the Model 16B/16B-HD Microcomputer.

7.2.9 Refresh Logic

The refresh logic provides the necessary timing and control for generating the refresh pulses required for the dynamic RAMs on the MC68000 memory board(s). It provides refresh by becoming the bus master and supplying the refresh strobe REFRSH. The timing is generated by an LS393 counter (U39) and a PAL device (U46).

The timing logic generates a bus request (REFRQ*) every 15.5 or 31 usec, depending on the configuration of the jumper on E1, E2, and E3. If E1 and E2 are jumpered, U46 triggers the D flip-flop (1/2 of U25) on the count of 62, which equals 15.5 usec. This will meet the minimum requirement of 128 refreshes every 2 msec. If E2 and E3 are jumpered, the D flip-flop will be triggered on the count of 124, which will equal 31 usec. This configuration will generate less refresh bus request cycles, thus allowing more CPU running time. However, to meet the 2 msec refresh specification, two refresh pulses are generated during each refresh period.

The generation of the single- or double-refresh pulse is the function of a refresh state machine implemented with a PAL device, U46. Figure 7-4 shows the timing relationships of the refresh logic.

7.2.10 Bus Error Logic
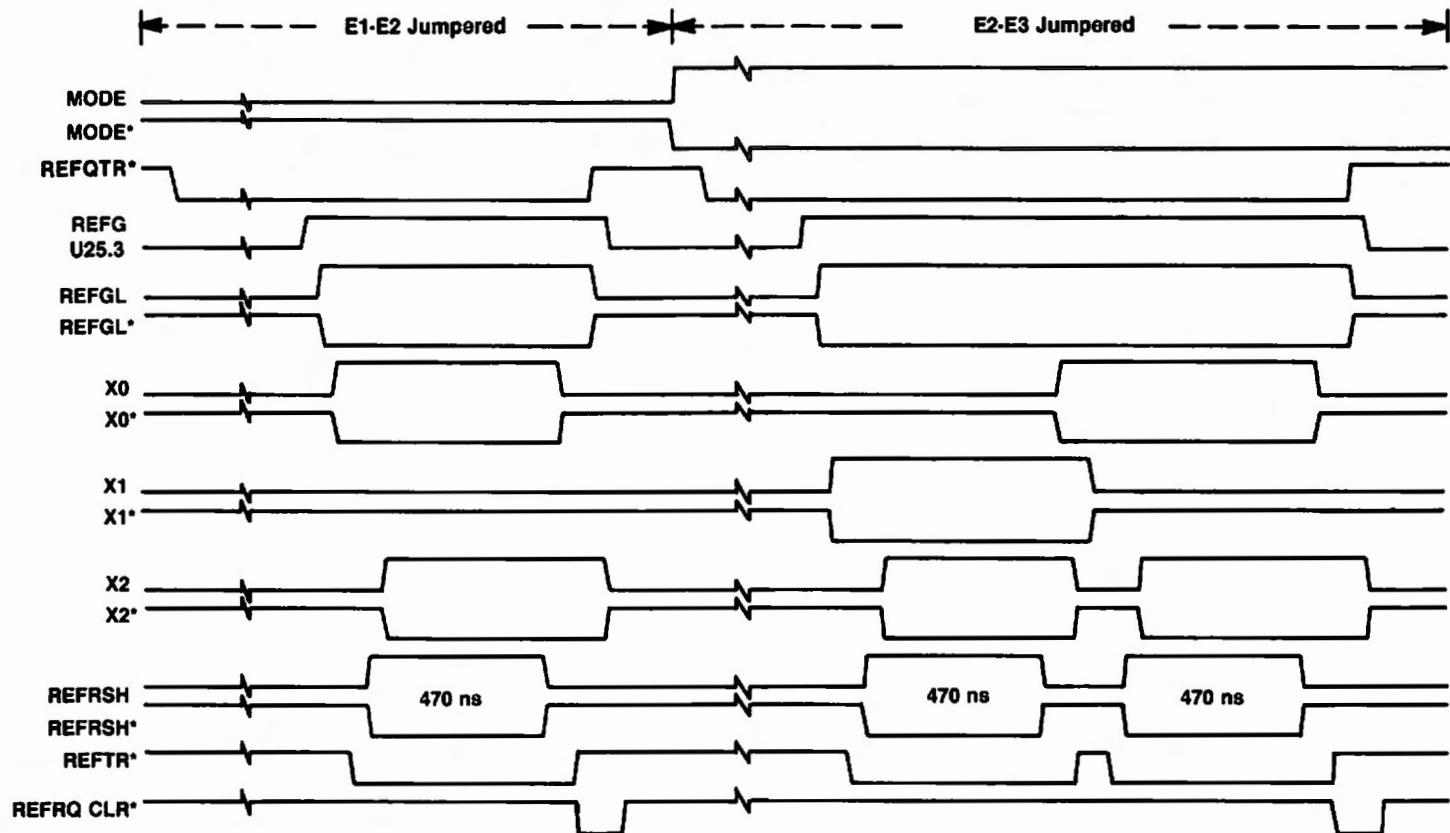
Bus error logic is driven low when one of three events noted below occurs:

.   An attempt by the user to access memory outside the extents defined by the memory management registers
.   A time-out error on an MC68000 memory access
.   A time-out error on a memory access by an external bus master, i.e. the Z80A CPU or DMA

The bus error signal also drives the MEMDIS* bus signal, which instructs the 16-bit memory board to abort a memory cycle. This provides a write-protect feature for accesses outside the user's defined extents. A 100 usec one-shot (1/2 of U32) is used to define the maximum time allowed for a memory cycle.
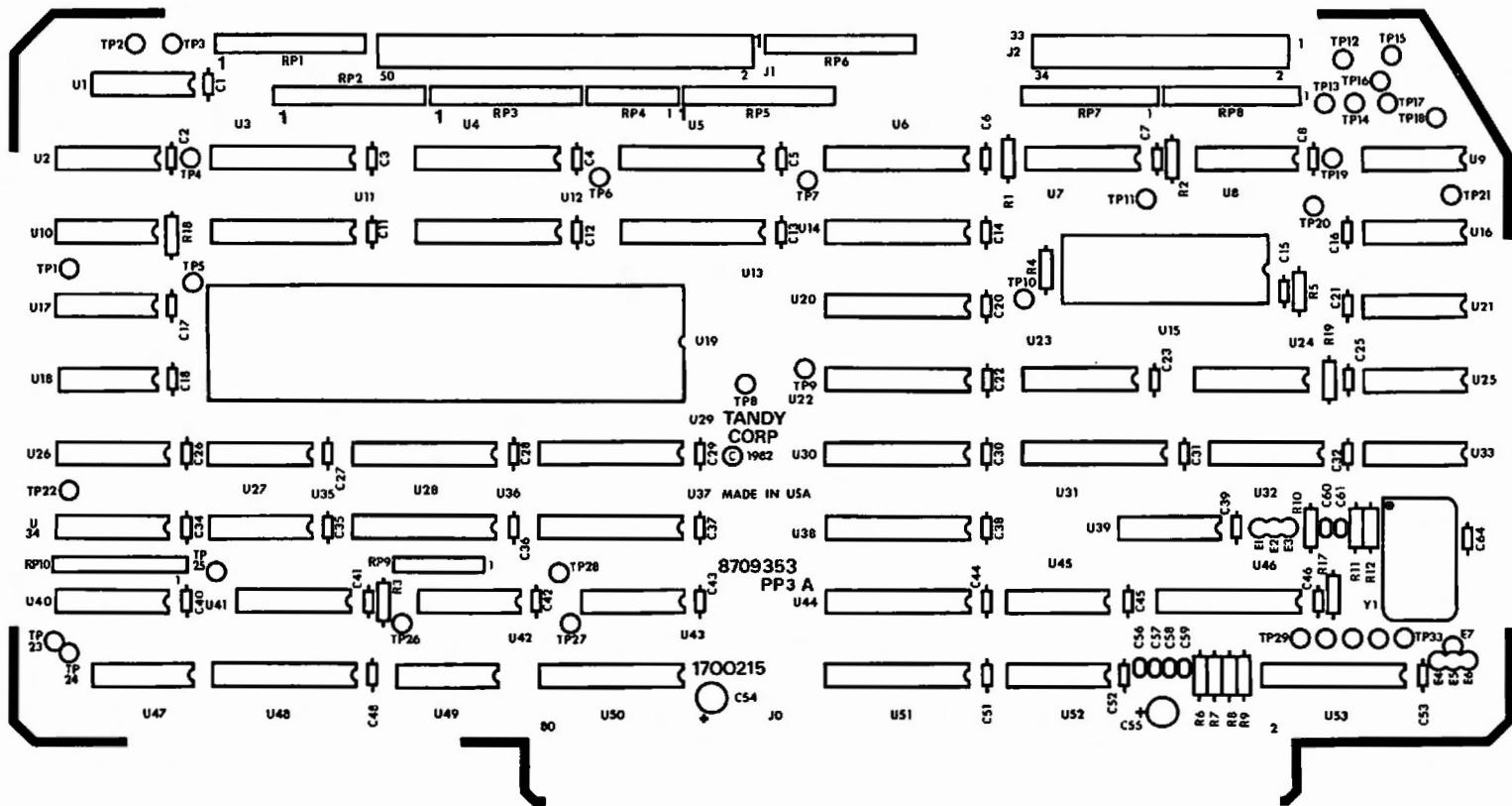
The bus Address Strobe (BAS*) is used to repeatedly trigger the one-shot. The active-low output of the one-shot is the clock input to a D flip-flop (1/2 of U21). If the one-shot ever times out, the rising edge of the active-low output will clock the state of BDTACK* into the D flip-flop.

The Q output of the flip-flop is inverted by an open collector device and drives the BDTACK* line. If, on a timeout, BDTACK* is high, indicating that the memory or I/O device did not respond, the BDTACK* is driven low by U33/ pin 12, which allows the cycle to complete. TMERR* is also driven by the Q-not output of the flip-flop. Thus, if a device on the bus fails to respond within the timespan allotted by the time-out circuit, a bus error will be generated.
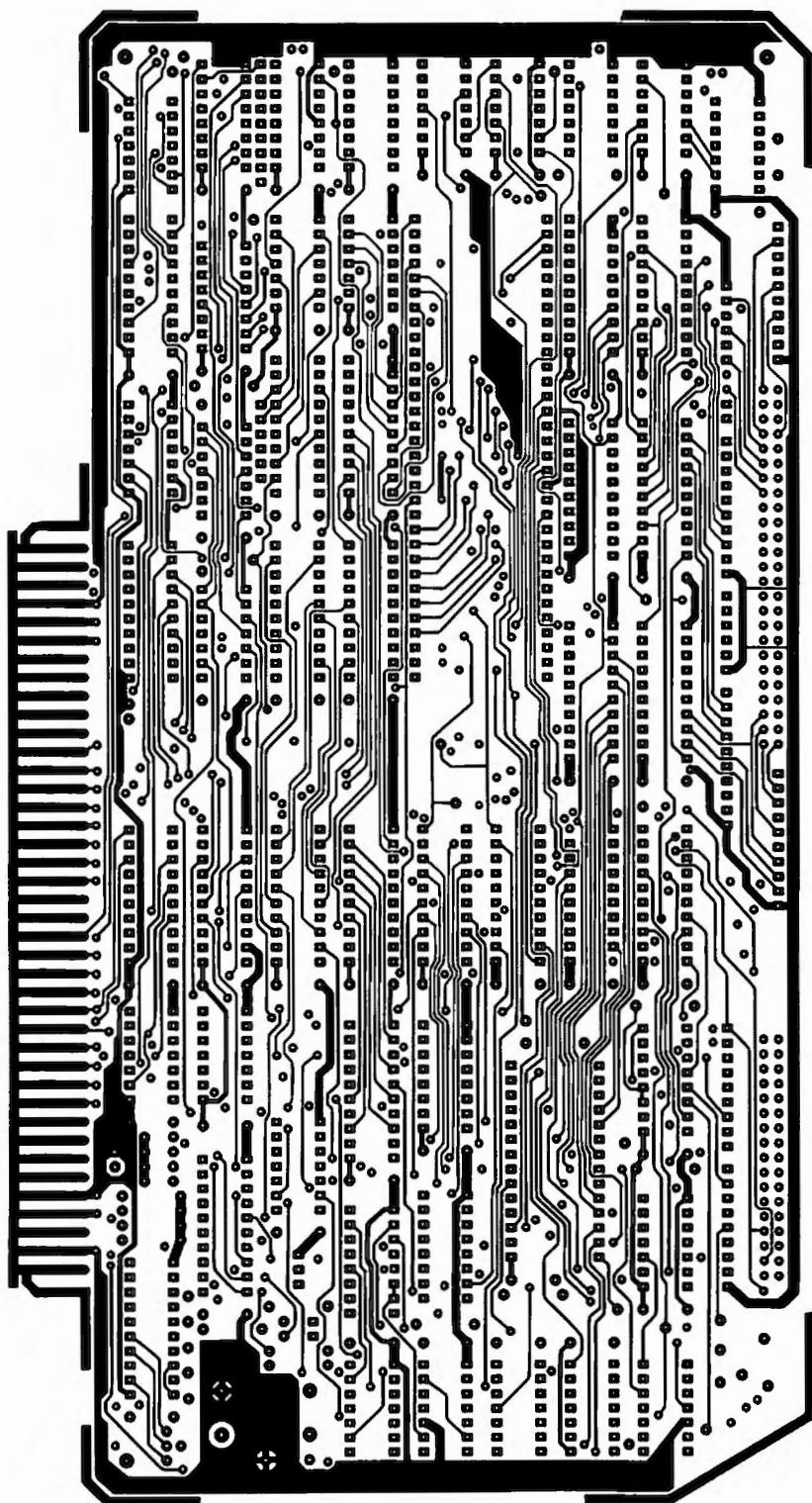
Note: Each block between signals equals one propagation delay.

Figure 7-4. Timing for Refresh Logic
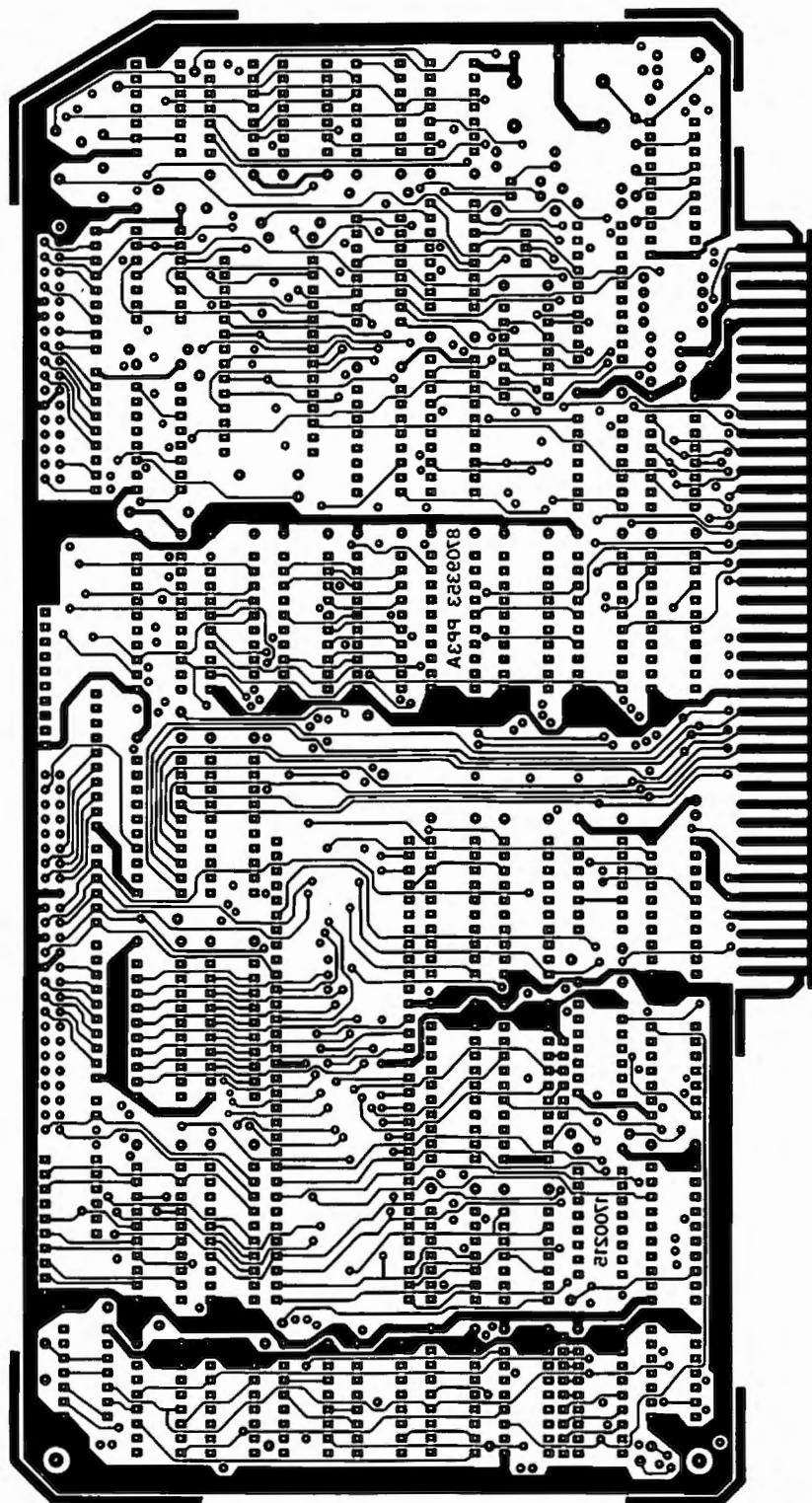
Component Layout, MC68000 CPU Board 8709353

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- 71 -

TP2 TP3
U1 C1 RP1
RP2 50 J1 RP6
U3 1 RP3 1 RP4 1 RP5 U6 C6 RP7 1 RP8
U2 C2 C3 U4 C4 U5 C5 C7 C8 U9
TP4 U11 TP6 U12 TP7 R1 U7 TP11 R2 U8 TP19 TP21
U10 R18 C9 U14 C14 R4 C15 C16 U16
TP1 TP5 U13 TP10 R5 C21 U21
U17 C17 U20 C20 U15 R19 C25
U19 U23 C23 U24 C25 U25
U18 C18 TP9 C22 U22
TP8 C30 C31 U32 U33
U29 TANDY CORP © 1982 U30 U31
U26 C26 C28 U37 MADE IN USA C39 U32 C60 C61
TP22 U27 U35 C27 U28 U36 U38 U39 U46 R17 R11 R12 C64
RP10 C4 C5 C6 C7 C44 U45 Y1
U40 U41 RP9 TP28 C43 U44 C45 C46 TP29 TP33 E7
TP23 TP25 R3 8709353 PP3 A
TP24 TP26 U42 TP27 U43 C56 C57 C58 C59
1700215 C52 C53
U47 U48 C48 U49 80 U50 C54 J0 U51 C51 U52 C55 R6 R7 R8 R9 2 U53

Circuit Trace, MC68000 CPU Board 8709353, Component Side

Circuit Trace, MC68000 CPU Board 8709353, Solder Side

Parts List, MC68000 CPU Board, 8898003

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Ref No.    Description                            Part No.
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Capacitors

Ref No.	Description				Part No.
C1	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C8	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C11	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C18	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C19	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C20	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C21	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C22	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C23	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C25	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C26	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C27	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C28	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C29	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C30	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C31	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C32	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C34	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C35	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C36	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C37	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C38	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C39	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C40	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C41	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C42	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C43	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C44	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C45	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C46	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C48	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C51	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C52	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C53	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104
C54	Capacitor,	100 uF,	16V,	Elect. Rad.	8327101
C55	Capacitor,	100 uF,	16V,	Elect. Rad.	8327101
C56	Capacitor,	68 pF,	50V,	C. Disk	8300683
C57	Capacitor,	68 pF,	50V,	C. Disk	8300683
C58	Capacitor,	68 pF,	50V,	C. Disk	8300683
C59	Capacitor,	68 pF,	50V,	C. Disk	8300683
C60	Capacitor,	0.001 uF,	Ceramic, 10%, Z5P		8302104
C61	Capacitor,	27 pF,	50V,	C. Disk, 5%	8300273
C64	Capacitor,	0.1 uF,	50V,	Mono-Axial	8374104

Parts List, MC68000 CPU Board, 8898003

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===============================================================
Ref No.   Description                                Part No.
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Resistors

Ref No.	Description	Part No.
R1	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R2	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R3	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R4	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R5	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R6	Resistor, 560 ohm, 1/4W, 5%	8207156
R7	Resistor, 560 ohm, 1/4W, 5%	8207156
R8	Resistor, 560 ohm, 1/4W, 5%	8207156
R9	Resistor, 560 ohm, 1/4W, 5%	8207156
R10	Resistor, 220 kohm, 1/4W, 5%	8207422
R11	Resistor, 30.1 kohm, 1/4W, 1%	8200330
R12	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R17	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R18	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R19	Resistor, 220 ohm, 1/4W, 5%	8207122

Resistor Paks

Ref No.	Description	Part No.
RP1	Res. Pak, 220-330 ohm SIP, 10-Pin	8290020
RP2	Res. Pak, 220-330 ohm SIP, 10-Pin	8290020
RP3	Res. Pak, 220-330 ohm SIP, 10-Pin	8290020
RP4	Res. Pak, 220 ohm SIP, 6-Pin	8290122
RP5	Res. Pak, 220-330 ohm SIP, 10-Pin	8290020
RP6	Res. Pak, 220-330 ohm SIP, 10-Pin	8290020
RP7	Res. Pak, 4.7k ohm SIP, 9-Pin	8292247
RP8	Res. Pak, 4.7k ohm SIP, 9-Pin	8292247
RP9	Res. Pak, 4.7k ohm SIP, 6-Pin	8293247
RP10	Res. Pak, 4.7k ohm SIP, 9-Pin	8292247

Intergrated Circuits

Ref No.		Description		Part No.
U1	IC,	74S00 Quad 2-IN NAND,	14-Pin	9010000
U2	IC,	74S04 Hex Inverter,	14-Pin	9010004
U3	IC,	MCM3482B 8-Bit Latch,	20-Pin	8051482
U4	IC,	74LS245 Octal Transceiver,	20-Pin	9020245
U5	IC,	74LS245 Octal Transceiver,	20-Pin	9020245
U6	IC,	PAL16R6 Custom Array,	20-Pin	8898489
U7	IC,	74LS174 Hex D-Type Flip-FLop,	16-Pin	9020174
U8	IC,	74S00 Quad 2-IN NAND,	14-Pin	9010000
U9	IC,	74LS02 Hex Inverter,	14-Pin	9020002
U10	IC,	74LS11 Triple #-IN AND,	14-Pin	9020011
U11	IC,	8303B 8-Bit Transceiver,	20-Pin	8060303
U12	IC,	8303B 8-Bit Transceiver,	20-Pin	8060303
U13	IC,	8303B 8-Bit Transceiver,	20-Pin	8060303
U14	IC,	8304B 8-Bit Transceiver,	20-Pin	8060304
U15	IC,	AM9519A Interrupt Controller,	28-Pin	8040519
U16	IC,	74S04 Hex Inverter,	14-Pin	9010004

Parts List, MC68000 CPU Board, 8898003
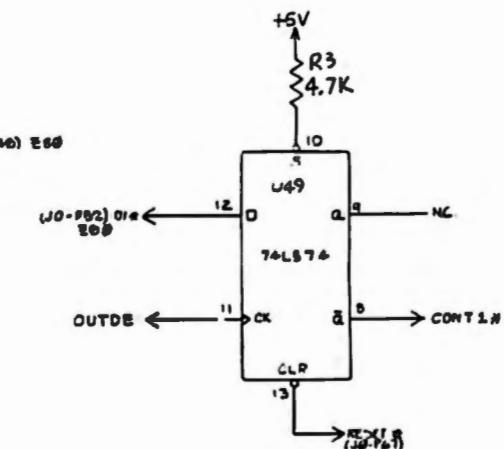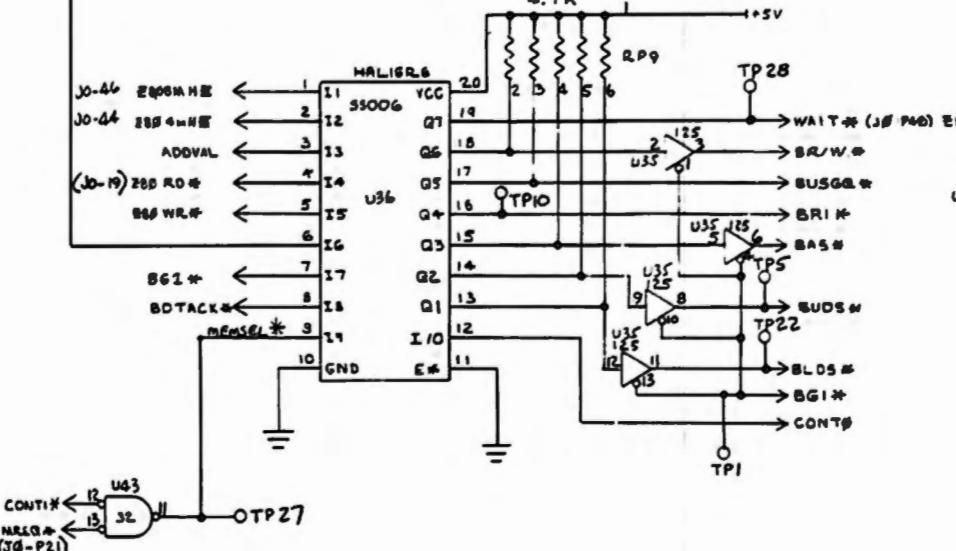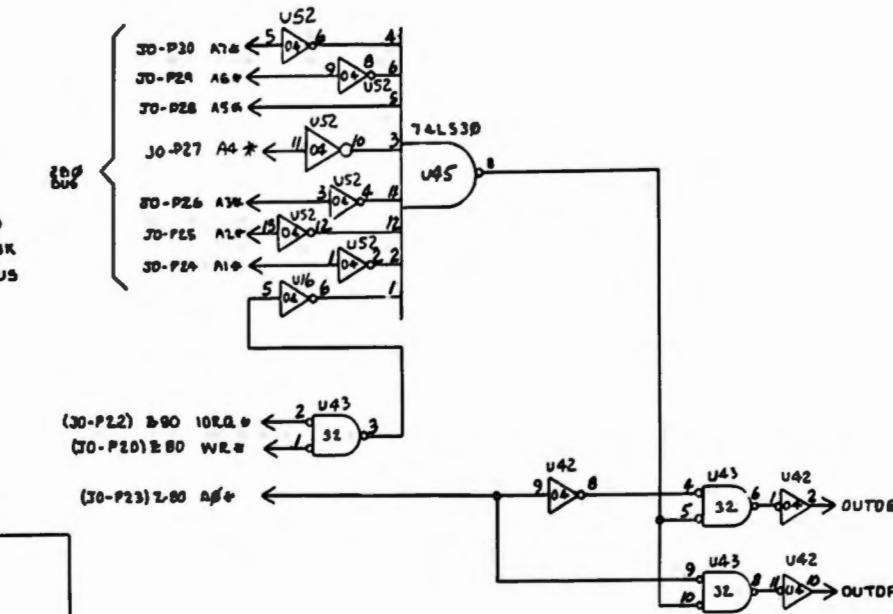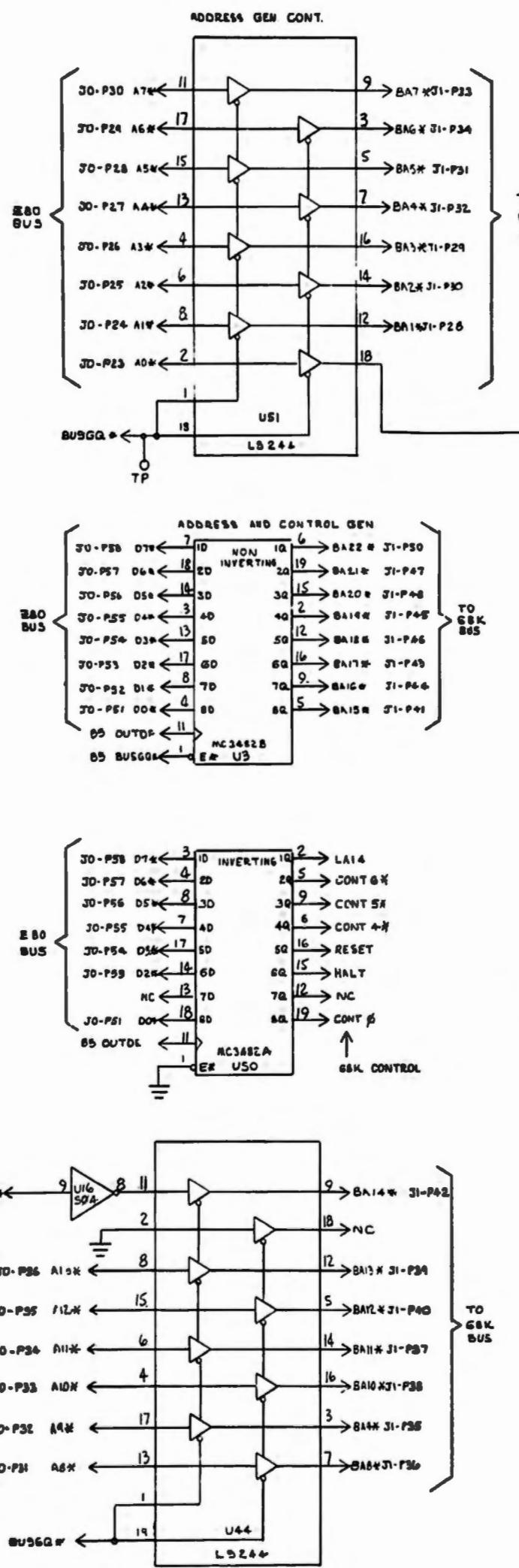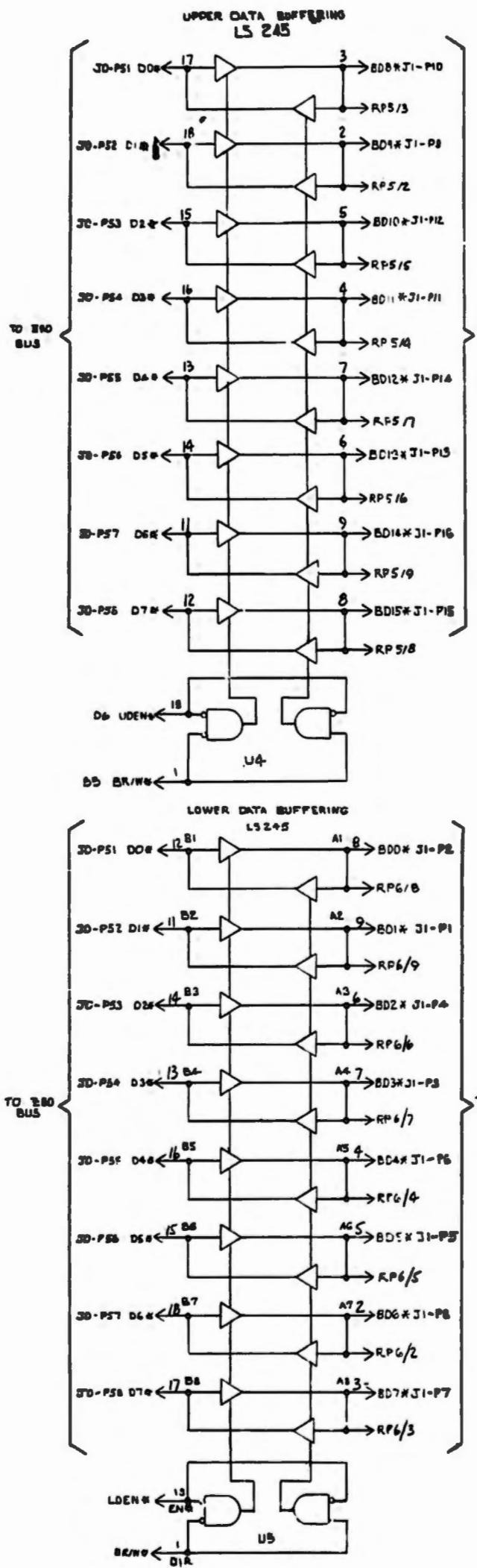
```
=================================================================
Ref No. Description                                    Part No.
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```

Intergrated Circuits

Ref No.	Description		Pin	Part No.
U17	IC,	74LS32 Quad 2-IN OR,	14-Pin	9020032
U18	IC,	74LS08 Quad 2-IN AND,	14-Pin	9020008
U19	IC, MCM68000		64-Pin	8040000
U20	IC,	74LS374 Octal Flip-Flop,	20-Pin	9020374
U21	IC,	74LS74 Dual Flip-Flop,	14-Pin	9020074
U22	IC,	74LS374 Octal Flip-Flop,	20-Pin	9020374
U23	IC,	74LS283 Binary Full Adder,	16-Pin	9020283
U24	IC,	74LS283 Binary Full Adder,	16-Pin	9020283
U25	IC,	74LS74 Dual Flip-Flop,	14-Pin	9020074
U26	IC,	74LS138 Decoder Mux,	16-Pin	9020138
U27	IC,	74LS11 Triple #-IN AND,	14-Pin	9020011
U28	IC,	8303B 8-Bit Transceiver,	20-Pin	8060303
U29	IC,	74LS374 Octal Flip-Flop,	20-Pin	9020374
U30	IC,	8303B 8-Bit Transceiver,	20-Pin	8060303
U31	IC,	74S240 8-Bit Buffer Inv,	20-Pin	9010240
U32	IC,	74LS123 Dual Mul.,	16-Pin	9020123
U33	IC,	7416 Hex Invert Buf Driv,	14-Pin	9000016
U34	IC,	74S138 Decoder Mux,	16-Pin	9010138
U35	IC,	74LS125 Tri-state Buffer,	14-Pin	9020125
U36	IC, PAL16R6A	Custom Array,	20-Pin	8898495
U37	IC,	74LS374 Octal Flip-Flop,	20-Pin	9020374
U38	IC,	74LS682 8-Bit Comparator,	20-Pin	9020682
U39	IC,	74LS393 4-Bit Binary Counter,	14-Pin	9020393
U40	IC,	74LS148 Encoder,	16-Pin	9020148
U41	IC,	74LS138 Decoder Mux,	16-Pin	9020138
U42	IC,74LS04NDS	Hex Inverter,	14-Pin	9020004
U43	IC,	74S32 Quad 2-IN OR,	14-Pin	9010032
U44	IC,	74S244 Octal Buffer,	20-Pin	9010244
U45	IC,	74LS30 8-IN NAND,	14-Pin	9020030
U46	IC, PAL16L8A	Custom Array,	20-Pin	8898493
U47	IC,	74LS164 Shift Register,	14-Pin	9020164
U48	IC, PAL16R6	Custom Array,	20-Pin	8898490
U49	IC,	74LS74 Dual Flip-Flop,	14-Pin	9020074
U50	IC, MCM3482A	8-Bit Latch,	20-Pin	8050482
U51	IC,	74S244 Octal Buffer	20-Pin	9010244
U52	IC,74LS04NDS	Hex Inverter,	14-Pin	9020004
U53	IC, PAL16R6A	Custom Array,	20-Pin	8898494

Parts List, MC68000 CPU Board, 8898003

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Ref No.    Description                           Part No.
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```
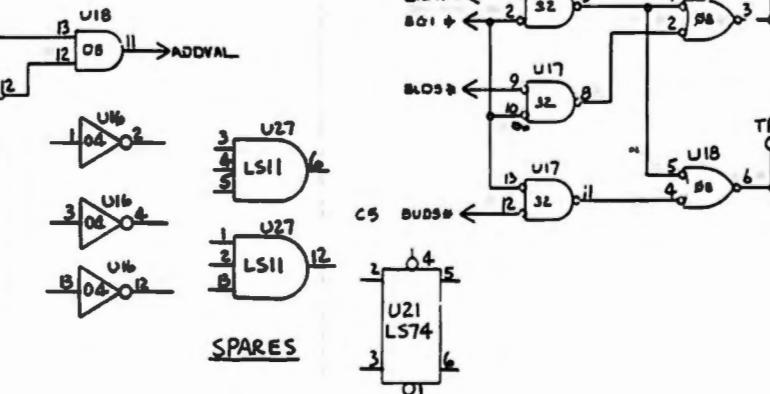
Sockets

Ref No.	Description	Part No.
---	Socket, 20-Pin (U3)	8509009
---	Socket, 20-Pin (U6)	8509009
---	Socket, 20-Pin (U11)	8509009
---	Socket, 20-Pin (U12)	8509009
---	Socket, 20-Pin (U13)	8509009
---	Socket, 20-Pin (U14)	8509009
---	Socket, 28-Pin (U15)	8509007
---	Socket, 64-Pin (U19)	8509014
---	Socket, 20-Pin (U28)	8509009
---	Socket, 20-Pin (U30)	8509009
---	Socket, 20-Pin (U36)	8509009
---	Socket, 20-Pin (U46)	8509009
---	Socket, 20-Pin (U48)	8509009
---	Socket, 20-Pin (U50)	8509009
---	Socket, 20-Pin (U53)	8509009

Staking Pins

Ref No.	Description	Part No.
E1	Staking Pin	8529014
E2	Staking Pin	8529014
E3	Staking Pin	8529014
E4	Staking Pin	8529014
E5	Staking Pin	8529014
E6	Staking Pin	8529014
E7	Staking Pin	8529014
TP1	Staking Pin	8529014
TP2	Staking Pin	8529014
TP3	Staking Pin	8529014
TP4	Staking Pin	8529014
TP5	Staking Pin	8529014
TP6	Staking Pin	8529014
TP7	Staking Pin	8529014
TP8	Staking Pin	8529014
TP9	Staking Pin	8529014
TP10	Staking Pin	8529014
TP12	Staking Pin	8529014
TP13	Staking Pin	8529014
TP14	Staking Pin	8529014
TP15	Staking Pin	8529014
TP16	Staking Pin	8529014
TP17	Staking Pin	8529014
TP18	Staking Pin	8529014
TP19	Staking Pin	8529014
TP20	Staking Pin	8529014
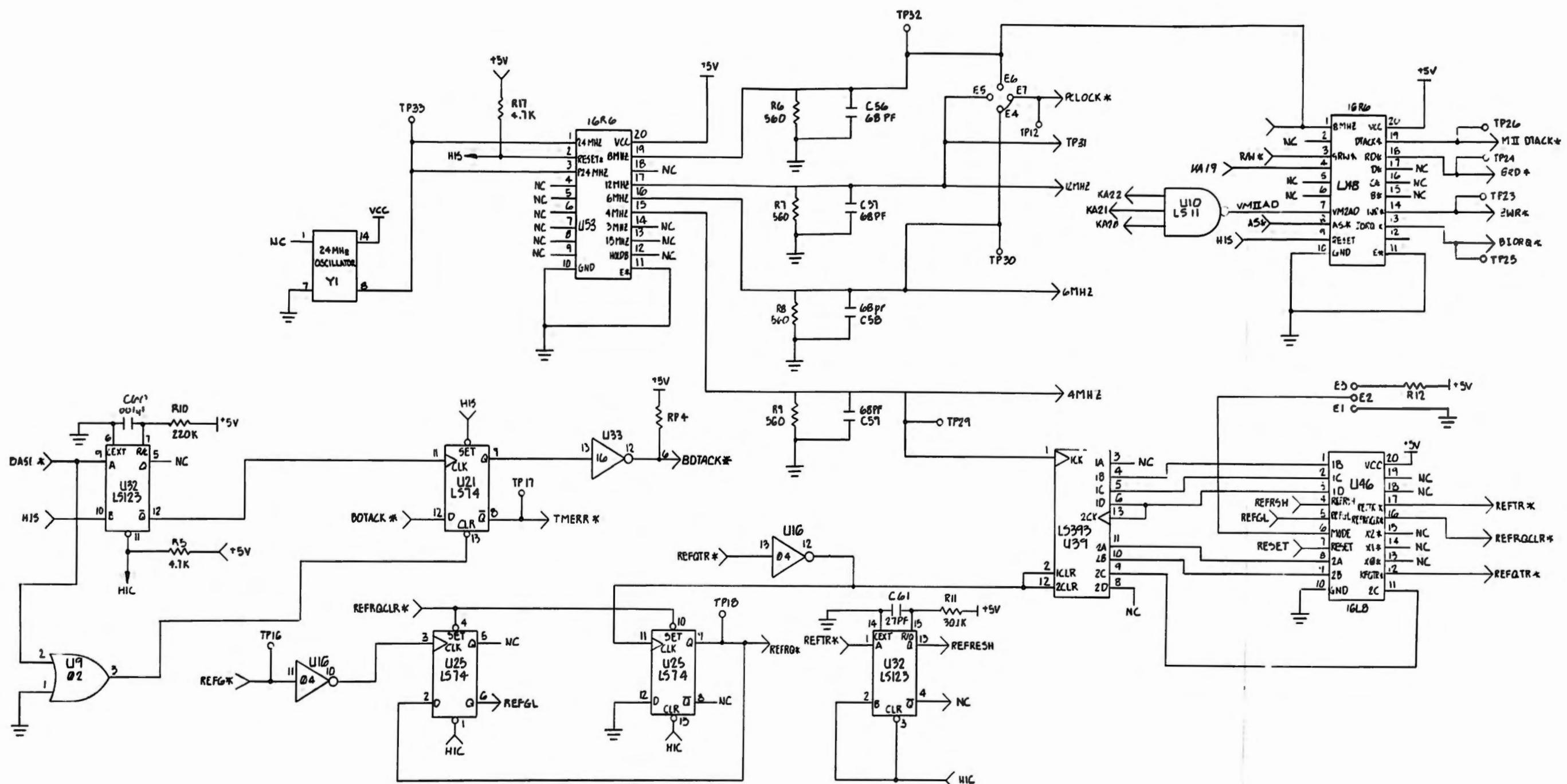
Radio Shack ®

Parts List, MC68000 CPU Board, 8898003

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Ref No.    Description                               Part No.
==============================================================
```

Staking Pin

Ref No.	Description	Part No.
TP21	Staking Pin	8529014
TP22	Staking Pin	8529014
TP23	Staking Pin	8529014
TP24	Staking Pin	8529014
TP25	Staking Pin	8529014
TP26	Staking Pin	8529014
TP27	Staking Pin	8529014
TP28	Staking Pin	8529014
TP28	Staking Pin	8529014
TP29	Staking Pin	8529014
TP30	Staking Pin	8529014
TP31	Staking Pin	8529014
TP32	Staking Pin	8529014
TP33	Staking Pin	8529014

Jumper Plugs

Ref No.	Description	Part No.
E2	Jumper Plugs	8519021
E3	Jumper Plugs	8519021
E4	Jumper Plugs	8519021
E5	Jumper Plugs	8519021
E6	Jumper Plugs	8519021
E7	Jumper Plugs	8519021

Miscellaneous

Ref No.	Description	Part No.
---	16-Bit CPU Board Main Assembly	8898003
---	PC Board, CPU (Rev PP3)	8709353
Y1	Oscillator, 24.0 MHz, 0.01%, HC-18	8409028
J1	Header, Dual 25-Pos. PCB MT.	9519117
J2	Header, Dual 17-Pos. PCB MT.	8519120
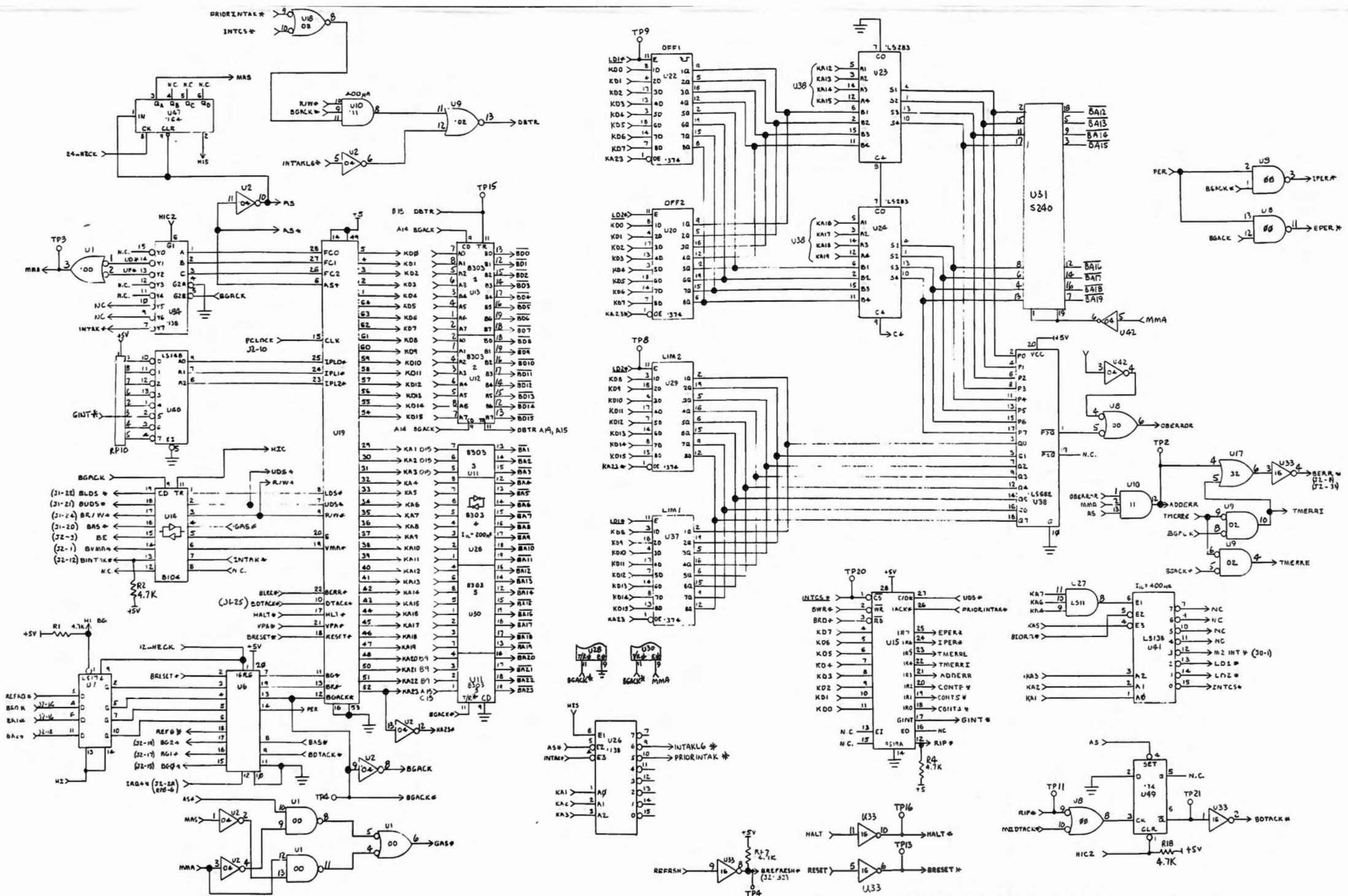
Schematic, MC68000 CPU Board, 8000181, Page 1 or 3

Schematic, MC68000 CPU Board, 8000181, Page 2 or 3

Schematic, MC68000 CPU Board, 8000181, Page 3 or 3

7.3 Memory Board

The Model 16B/16B-HD Memory board is a Random Access Memory
(RAM) with a total capacity of 128K words (256K bytes) of
data with optional byte parity for error detection. It is
designed for use with the MC68000 processor system. The
MC68000 has a 16-bit wide data bus and, therefore, the
memory is 16 bits wide.

Because the MC68000 needs to handle both 8- and 16-bit wide
data transactions, the memory is further divided into upper
and lower bytes (8-bit). Actually, all transfers to and
from memory are treated as byte transfers. If a full 16-bit
transfer is desired, an upper and lower byte transaction is
performed simultaneously. Thus, the memory is organized as
two parallel byte memories that share a common memory space.

Since parity is checked on all transfers, if the option is
enabled, the parity generating/checking has to be set up on
a byte basis. Therefore, each byte has a ninth bit added
called a parity bit. Parity is a scheme where the total
number of bits that equal one in every valid memory location
is either EVEN or ODD. The Model 16B/16B-HD memory uses
the ODD scheme. Thus, if the data has an even number of
bits equaling 1 (0, 2, 4, 6, or 8), the parity bit will
equal 1, making the total number of bits equal 1 or ODD
parity. Otherwise, the parity bit equals 0 or EVEN.

The Model 16B/16B-HD Memory Board can be functionally
divided into four main parts:

    Memory

    Address Circuits

    Control/Timing Circuits

    Parity Circuits

7.3.1 Memory

By understanding the requirements of the memory ICs, the
address and timing circuits are more easily understood. The
basic memory element is a DRAM (Dynamic Random Access
Memory) IC containing 65,536 (64K) single-bit locations.
Therefore, to store each byte with parity, nine ICs are
required.

Two particulars of dynamic RAMs are address multiplexing and
refresh. There are 16 address lines to access this amount
of memory. Address line A0, internal to the MC68000 CPU, is
used to distinguish between upper (if A0=1) and lower (if
A0=0) bytes. Since this least significant bit is used to
determine selection of the upper or lower byte, the address
is then contained in bits A1 through A16 rather than A0
through A15. To save pins and chip size, the ICs have only
8 address inputs.

Therefore, the address lines are loaded into memory in two
parts:

> First the Row address (A1-A8), by the Row Address
> Strobe (RAS)

> Second the Column address (A9-A16), by the Column
> Address Strobe (CAS)

Once the addresses are loaded, the memory alters or presents
the data at that location, depending on the state of the
Read/Write (R/W*) signal. Refresh is required to maintain
the information stored in the RAMs.

Every 2 milliseconds the entire contents of the RAM must be
refreshed. This requires 128 refresh-only accesses every
2.0 msec, or one every 16.0 usec. The refresh cycle is the
same as a read cycle, except AMUX and CAS are not generated.

7.3.2 Address Circuits

Address lines BA1* through BA16* are routed to the board
through two-line receiver-inverting buffers U3 and U4
(74S240), which are permanently enabled. The lower eight
address lines (BA1-BA8) are multiplexed by U28 and U48 with
the eight refresh address bits from the refresh address
counter U14 becoming the eight memory row address bits.

The row address bits are then multiplexed with the column
address bits by U29 and U49 (address lines BA9-BA16) and
become the eight multiplexed memory address bits. The
memory address lines are routed to all 36 ICs through series
resistors to reduce ringing and overshoot.

Address line BA17* is routed to the memory board by
non-inverting buffer U9. A17 enables the steering AND gates
to generate the RAS signals for the lower or upper 128K
memory page. Address lines BA18-BA22 are used to enable the

memory board at a specific 256K location within the MC68000 subsystem memory map allocation.

These address lines are connected to an 8-bit magnitude comparator U2 (LS688) that compares two 8-bit inputs. The address lines are compared to a preset value by the use of DIP switch S1. If the address lines BA18-BA22 equal the preset value, the output of the comparator is asserted and enables the memory board. Refer to Table 7-4 for the proper setting of S1.

7.3.3 Control/Timing

The control and timing signals consist of Bus Address Strobe (BAS*), Bus Upper Data Strobe (BUDS*), Bus Lower Data Strobe (BLDS*), Bus Read/Write (BR/W*), Memory Disable (MEMDIS*, which is BERR*), and Bus Data Transfer Acknowledge (BDTACK*).

All signals, except BDTACK*, are input signals from the MC68000 CPU board and are interfaced to the memory board through U9 (S241). BDTACK* is an output control signal to the MC68000 CPU board and is driven by an open collector NAND gate U1 pin 3 (7438).

The output of U10 pin 8 (UDSG) represents the logical AND of AS*, UDS*, board select from U2 pin 19, and MEMDIS. U10 pin 6 (LDSG) represents the logical AND of AS*, LDS*, BDSEL*, and MEMDIS or REF* (refresh). These two outputs are ORed together by U11, so either one will initiate a memory request cycle.

The output of U11 pin 8 (MEMREQ) clocks the D flip-flop (1/2 of U12) to start a pulse down a delay line U13. The pulse output at the 40 nsec tap is RAS, at 80 nsec it is AMUX, at 120 nsec it is CAS, and at 200 nsec it is TERMinate, which clears the flip-flop U12 and limits the pulse to 200 nsec. RAS from the 40 nsec output enables the steering logic.

MEMDIS is a signal used by the Memory Management Unit to prevent access to memory, especially writes. In addition to being a term in MEMREQ, it is ORed together with TERM as extra insurance to prevent an access cycle. MEMDIS should be true before UDS*/LDS*. The signal RAS is ANDed with the four combinations of LDSG, UDSG, A17 and A17* at U24 and U25 to make four signals.

| | S1 | | | | | | | |
| | | | (B18) | | (B19) | (B22) | (B20) | (B21) |
	1	2	3	4	5	6	7	8
Disable Board	X	0	X	X	X	X	X	X
000000-03FFFF	X	1	0	X	0	0	0	0
040000-07FFFF	X	1	1	X	0	0	0	0
080000-0BFFFF	X	1	0	X	1	0	0	0
0C0000-0FFFFF	X	1	1	X	1	0	0	0
100000-13FFFF	X	1	0	X	0	0	1	0
140000-17FFFF	X	1	1	X	0	0	1	0
180000-1BFFFF	X	1	0	X	1	0	1	0
1C0000-1FFFFF	X	1	1	X	1	0	1	0
200000-23FFFF	X	1	0	X	0	0	0	1
240000-27FFFF	X	1	1	X	0	0	0	1
280000-2BFFFF	X	1	0	X	1	0	0	1
2C0000-2FFFFF	X	1	1	X	1	0	0	1
300000-33FFFF	X	1	0	X	0	0	1	1
340000-37FFFF	X	1	1	X	0	0	1	1
380000-3BFFFF	X	1	0	X	1	0	1	1
3C0000-3FFFFF	X	1	1	X	1	0	1	1
400000-43FFFF	X	1	0	X	0	1	0	0
440000-47FFFF	X	1	1	X	0	1	0	0
480000-4BFFFF	X	1	0	X	1	1	0	0
4C0000-4FFFFF	X	1	1	X	1	1	0	0
500000-53FFFF	X	1	0	X	0	1	1	0
540000-57FFFF	X	1	1	X	0	1	1	0
580000-5BFFFF	X	1	0	X	1	1	1	0
5C0000-5FFFFF	X	1	1	X	1	1	1	0
600000-63FFFF	X	1	0	X	0	1	0	1
640000-67FFFF	X	1	1	X	0	1	0	1
680000-6BFFFF	X	1	0	X	1	1	0	1
6C0000-6FFFFF	X	1	1	X	1	1	0	1

0 = Off = Open
1 = On = Closed
X = Don't Care

Table 7-4. Memory Map Select Table

These four signals are ORed together with REF at U23 to
generate RAS1L, RAS1U, RAS2L, RAS2U, a Row Address Strobe
for each memory byte section. The signal CAS is ANDed with
(disabled by) REF* to generate CASU* and CASL*, the Column
Address Strobe for each word section. The signal R/W* is
ANDed at U15 with UDSG to generate R/W* UPPER BYTE, and with
LDSG to generate R/W* LOWER BYTE write strobes.

The drivers for each of the signals RAS1L*, RAS1U*, RAS2L*,
RAS2U*, CASL*, CASU*, R/W* LOWER BYTE, and R/W* UPPER BYTE
are each passed through a series resistor to reduce ringing
and undershoot. The signal DTACK* originates from the D
flip-flop U12. The CAS pulse from the delay line sets the
signal and is reset at the end of MEMREQ. An inverter
buffers the signal to the MC68000 processor section.

7.3.4 Parity
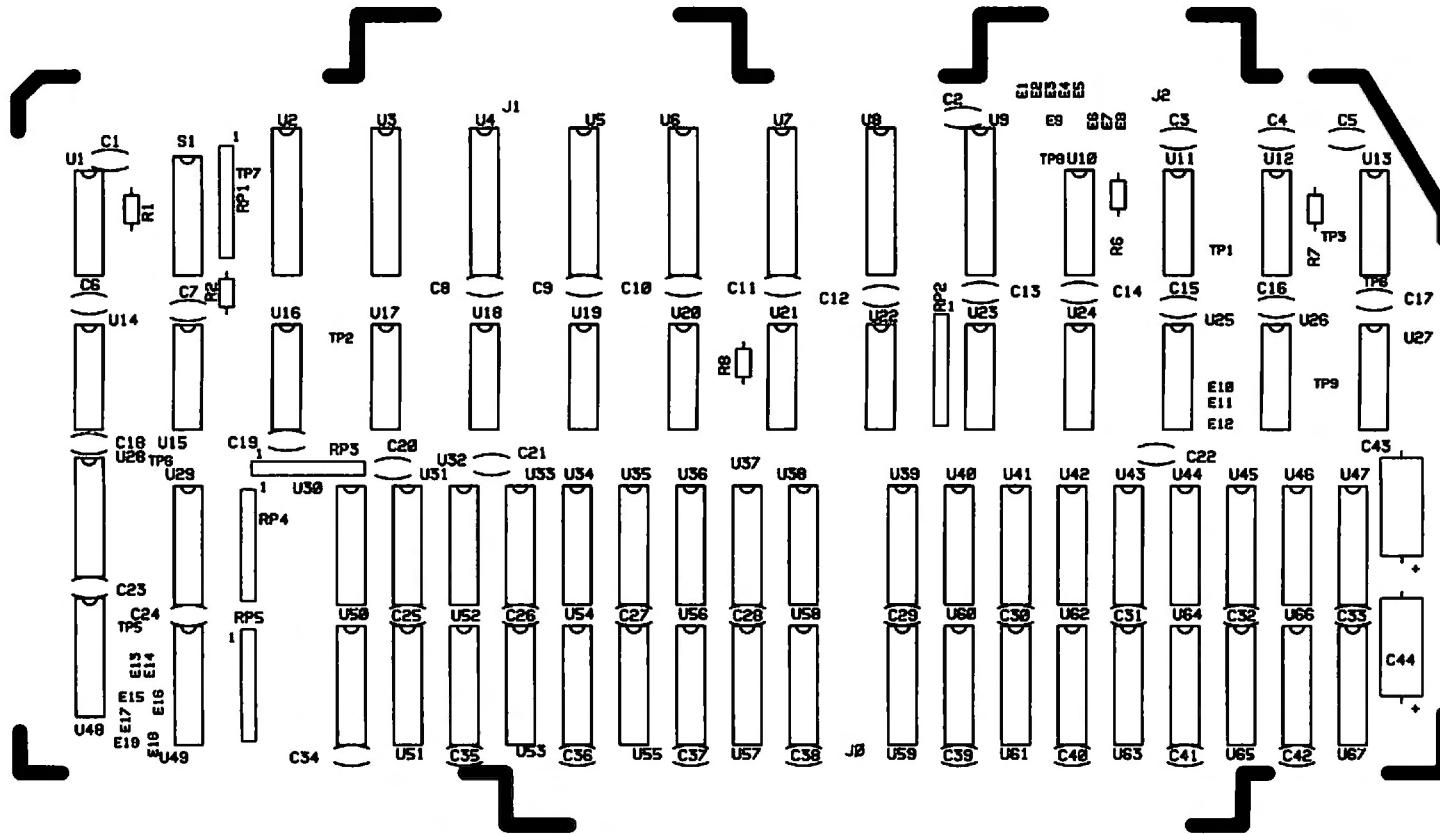
There are two parity circuits:

.   Input parity generators

.   Output parity checkers
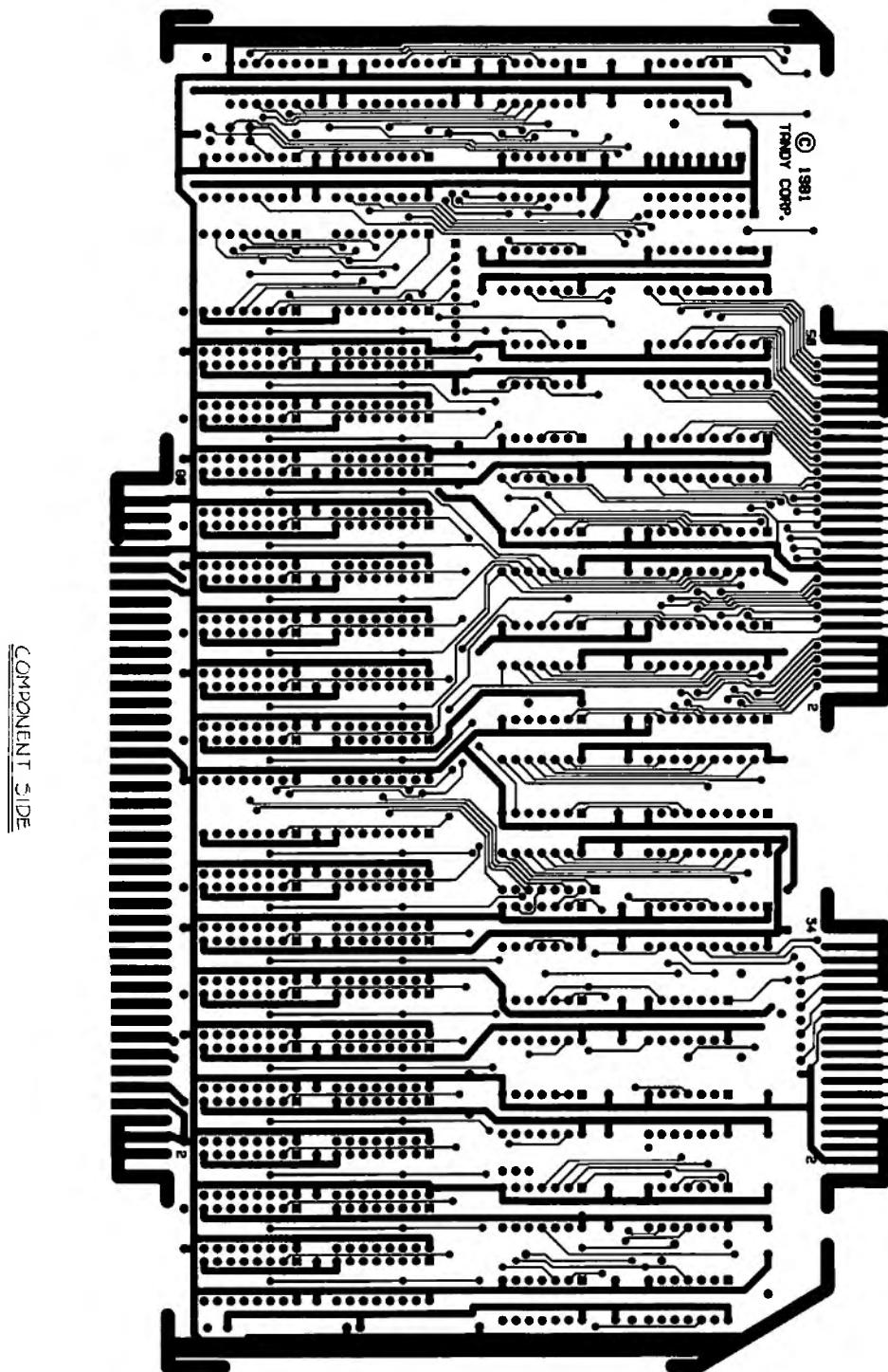
Since there is byte parity, there is one parity bit for each
byte. When data is being written to a memory location, the
data is monitored by the input parity generators.

The output of this generator is written into the same memory
location as the ninth or parity bit. When a byte is being
read from a memory location, all nine bits are monitored by
the output parity checkers (the parity bit is not passed on
to the bus). If the parity is correct, the output is a
logic 1.

If the parity is incorrect, a logic 0 is strobed into D
flip-flop U27 by AMUX. This signal is then routed to the
next selected system interrupt. The signal is cleared by
the next AS*. Parity is an optional feature. The lack of
it does not alter the memory operation.

U1 C1 S1 1 TP7 U2 U3 U4 J1 U5 U6 U7 U8 C2 U9 E9 J2 C3 C4 C5
R1 RP1 U13

C6 C7 R2 U16 TP2 U17 U18 C9 C10 C11 C12 RP2 C13 C14 U25 TP9
C8 U19 U20 U21 U23 U24 C16 U26 U27
U14 U22 C15 C17
TP8 U10 R6 U11 TP1 R7 TP3
C18 U15 C19 RP3 C20 U32 C21 U35 U36 U37 U38 C22 U39 U40 U41 U42 U43 U44 U45 U46 U47 C43
U28 TP6 U30 U51 U33 U34 E10
U29 RP4 E11
C23 E12
U48 RP5 C24
TP5 U49 C50 C25 U52 C26 U54 C27 U56 C28 U58 U29 U60 C30 U62 C31 U64 C32 U66 C33 C44
E13 E14
E17 E15 E16
E19 E18 U50
C34 U51 C35 U53 C36 U55 C37 U57 C38 J0 U59 C39 U61 C40 U63 C41 U65 C42 U67

R8

Circuit Trace, 128/256K Memory Board, Component Side

Circuit Trace, 128/256K Memory Board, Solder Side

Parts List, Memory Board, 8898002

```
==================================================================
Ref No.    Description                              Part No.
==================================================================
```
Capacitors

Ref No.	Description	Part No.
C1	Capacitor, 0.1 uF, Mono-Axial	8374104
C2	Capacitor, 0.1 uF, Mono-Axial	8374104
C3	Capacitor, 0.1 uF, Mono-Axial	8374104
C4	Capacitor, 0.1 uF, Mono-Axial	8374104
C5	Capacitor, 0.1 uF, Mono-Axial	8374104
C6	Capacitor, 0.1 uF, Mono-Axial	8374104
C7	Capacitor, 0.1 uF, Mono-Axial	8374104
C8	Capacitor, 0.1 uF, Mono-Axial	8374104
C9	Capacitor, 0.1 uF, Mono-Axial	8374104
C10	Capacitor, 0.1 uF, Mono-Axial	8374104
C11	Capacitor, 0.1 uF, Mono-Axial	8374104
C12	Capacitor, 0.1 uF, Mono-Axial	8374104
C13	Capacitor, 0.1 uF, Mono-Axial	8374104
C14	Capacitor, 0.1 uF, Mono-Axial	8374104
C15	Capacitor, 0.1 uF, Mono-Axial	8374104
C16	Capacitor, 0.1 uF, Mono-Axial	8374104
C17	Capacitor, 0.1 uF, Mono-Axial	8374104
C18	Capacitor, 0.1 uF, Mono-Axial	8374104
C19	Capacitor, 0.1 uF, Mono-Axial	8374104
C20	Capacitor, 0.1 uF, Mono-Axial	8374104
C21	Capacitor, 0.1 uF, Mono-Axial	8374104
C22	Capacitor, 0.1 uF, Mono-Axial	8374104
C23	Capacitor, 0.1 uF, Mono-Axial	8374104
C24	Capacitor, 0.1 uF, Mono-Axial	8374104
C25	Capacitor, 0.1 uF, Mono-Axial	8374104
C26	Capacitor, 0.1 uF, Mono-Axial	8374104
C27	Capacitor, 0.1 uF, Mono-Axial	8374104
C28	Capacitor, 0.1 uF, Mono-Axial	8374104
C29	Capacitor, 0.1 uF, Mono-Axial	8374104
C30	Capacitor, 0.1 uF, Mono-Axial	8374104
C31	Capacitor, 0.1 uF, Mono-Axial	8374104
C32	Capacitor, 0.1 uF, Mono-Axial	8374104
C33	Capacitor, 0.1 uF, Mono-Axial	8374104
C34	Capacitor, 0.1 uF, Mono-Axial	8374104
C35	Capacitor, 0.1 uF, Mono-Axial	8374104
C36	Capacitor, 0.1 uF, Mono-Axial	8374104
C37	Capacitor, 0.1 uF, Mono-Axial	8374104
C38	Capacitor, 0.1 uF, Mono-Axial	8374104
C39	Capacitor, 0.1 uF, Mono-Axial	8374104
C40	Capacitor, 0.1 uF, Mono-Axial	8374104
C41	Capacitor, 0.1 uF, Mono-Axial	8374104
C42	Capacitor, 0.1 uF, Mono-Axial	8374104

Parts List, Memory Board, 8898002

```
==================================================================
Ref No.   Description                                   Part No.
==================================================================
```

Resistors

Ref No.	Description	Part No.
R1	Resistor, 1 kohm, 1/4W, 5%	8207210
R2	Resistor, 1 kohm, 1/4W, 5%	8207210
R3	Resistor, 1 kohm, 1/4W, 5%	8207210
R4	Resistor, 1 kohm, 1/4W, 5%	8207210
R5	Resistor, 1 kohm, 1/4W, 5%	8207210
R6	Resistor, 1 kohm, 1/4W, 5%	8207210

Resistor Paks

Ref No.	Description	Part No.
RP1	Network, 4.7 kohm, Common SIP	8292246
RP2	Network, 33 ohm, Series SIP	8295003
RP3	Network, 33 ohm, Series SIP	8295003
RP4	Network, 33 ohm, Series SIP	8295003
RP5	Network, 33 ohm, Series SIP	8295003

Integrated Circuits

Ref No.	Description	Part No.
U1	IC, 7438, Quad 2-IN NAND, Oprn-C,14-Pin	9000038
U2	IC, 74LS688, 8-Bit Comparator, 20-Pin	9020688
U3	IC, 74S240, Octal Bus Line Dirver, 20-Pin	9010240
U4	IC, 74S240, Octal Bus Line Dirver, 20-Pin	9010240
U5	IC,MCM3482A, 8-Bit Latch, 20-Pin	8050482
U6	IC,MCM3482A, 8-Bit Latch, 20-Pin	8050482
U7	IC,MCM3482A, 8-Bit Latch, 20-Pin	8050482
U8	IC,MCM3482A, 8-Bit Latch, 20-Pin	8050482
U9	IC, 74S241, Octal Bus Line Driver, 20-Pin	9010241
U10	IC, 7525, Dual 4-IN NOR, 14-Pin	9000025
U11	IC, 74LS32, Quad 2-IN OR, 14-Pin	9020032
U12	IC, 74S74, Dual JK Flip-Flop, 14-Pin	9010074
U13	IC,DDU4-5200, Delay Line(200ns) 14-Pin	8429010
U14	IC, 74LS393, Dual 4-Bit Binary Counter	9020393
U15	IC, 74S37, Quad 2-IN NAND Buffer,14-Pin	9010037
U16	IC, 74S04, Hex Inverter, 14-Pin	9010004
U17	IC, 74S00, Quad 2-IN NAND, 14-Pin	9010000
U18	IC, 74S00, Quad 2-IN NAND, 14-Pin	9010000
U23	IC, 74S08, Quad 2-IN AND, 14-Pin	9010008
U24	IC, 74S10, Triple 3-IN NAND, 14-Pin	9010010
U25	IC, 74S10, Triple 3-IN NAND, 14-Pin	9010010
U26	IC, 74S04, Hex Inverter, 14-Pin	9010004
U27	IC, 74S74, Dual JK Flip-Flop, 14-Pin	9010074
U28	IC, 74S157, Quad 2-IN MUX, 16-Pin	9010157
U29	IC, 74S157, Quad 2-IN MUX, 16-Pin	9010157
U48	IC, 74S157, Quad 2-IN MUX, 16-Pin	9010157
U49	IC, 74S157, Quad 2-IN MUX, 16-Pin	9010157
U50	IC, MCM6665, Dynamic RAM (200ns), 16-Pin	8040665
U51	IC, MCM6665, Dynamic RAM (200ns), 16-Pin	8040665

Parts List, Memory Board, 8898002

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================================================================
Ref No.   Description                                  Part No.
================================================================
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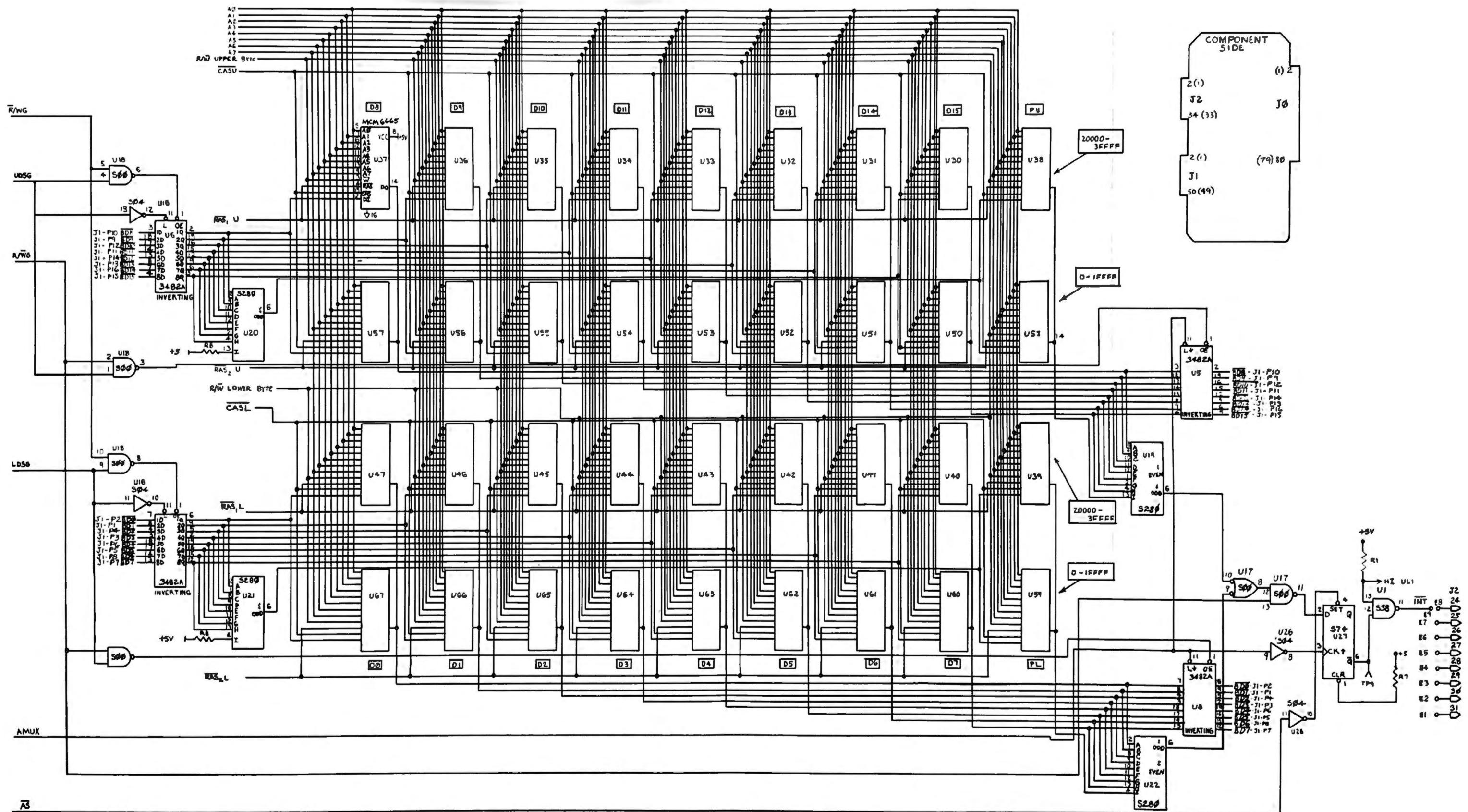
Integrated Circuits

Ref No.	Description		Part No.
U52	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U53	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U54	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U55	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U56	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U57	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U60	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U61	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U62	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U63	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U64	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U65	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U66	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665
U67	IC, MCM6665, Dynamic RAM (200ns),	16-Pin	8040665

Jumper Plugs

Ref No.	Description	Part No.
E1	Jumper Plug	8519021
E2	Jumper Plug	8519021
E13	Jumper Plug	8519021
E14	Jumper Plug	8519021
E16	Jumper Plug	8519021
E17	Jumper Plug	8519021
E18	Jumper Plug	8519021
E19	Jumper Plug	8519021
E20	Jumper Plug	8519021
E21	Jumper Plug	8519021
E22	Jumper Plug	8519021
E23	Jumper Plug	8519021

Sockets

Ref No.	Description	Part No.
---	Socket, 20-Pin (U5)	8509009
---	Socket, 20-Pin (U6)	8509009
---	Socket, 20-Pin (U7)	8509009
---	Socket, 20-Pin (U8)	8509009
---	Socket, 14-Pin (U19)	8509008
---	Socket, 14-Pin (U20)	8509008
---	Socket, 14-Pin (U21)	8509008
---	Socket, 14-Pin (U22)	8509008
---	Socket, 16-Pin (U30)	8509003
---	Socket, 16-Pin (U31)	8509003
---	Socket, 16-Pin (U32)	8509003
---	Socket, 16-Pin (U33)	8509003
---	Socket, 16-Pin (U34)	8509003
---	Socket, 16-Pin (U35)	8509003

Radio Shack ®

Parts List, Memory Board, 8898002

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================================================================
Ref No.    Description                              Part No.
================================================================
```
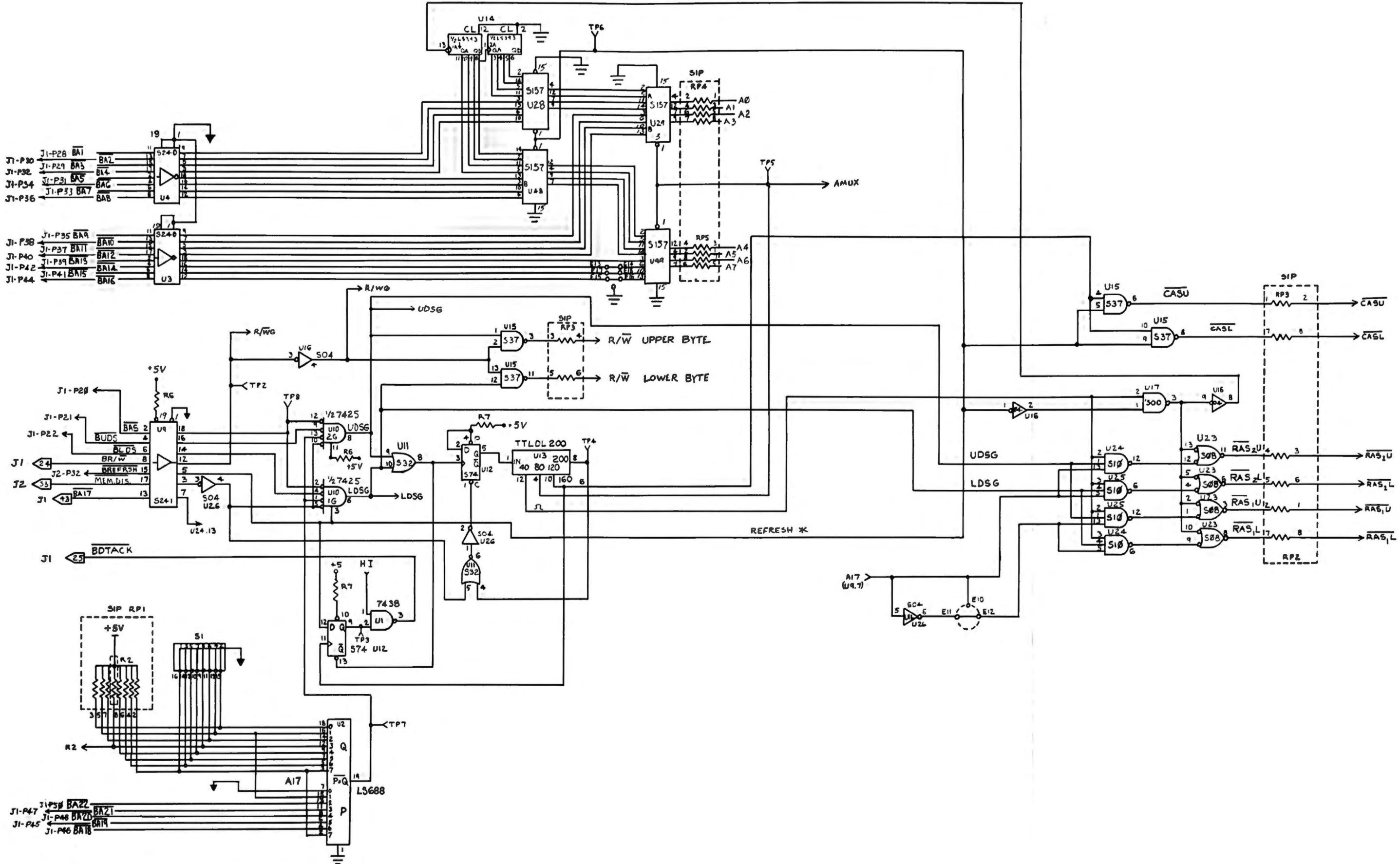
Sockets

Ref No.	Description	Part No.
---	Socket, 16-Pin (U36)	8509003
---	Socket, 16-Pin (U37)	8509003
---	Socket, 16-Pin (U38)	8509003
---	Socket, 16-Pin (U39)	8509003
---	Socket, 16-Pin (U40)	8509003
---	Socket, 16-Pin (U41)	8509003
---	Socket, 16-Pin (U42)	8509003
---	Socket, 16-Pin (U43)	8509003
---	Socket, 16-Pin (U44)	8509003
---	Socket, 16-Pin (U45)	8509003
---	Socket, 16-Pin (U46)	8509003
---	Socket, 16-Pin (U47)	8509003
---	Socket, 16-Pin (U50)	8509003
---	Socket, 16-Pin (U51)	8509003
---	Socket, 16-Pin (U52)	8509003
---	Socket, 16-Pin (U53)	8509003
---	Socket, 16-Pin (U54)	8509003
---	Socket, 16-Pin (U55)	8509003
---	Socket, 16-Pin (U56)	8509003
---	Socket, 16-Pin (U57)	8509003
---	Socket, 16-Pin (U58)	8509003
---	Socket, 16-Pin (U59)	8509003
---	Socket, 16-Pin (U60)	8509003
---	Socket, 16-Pin (U61)	8509003
---	Socket, 16-Pin (U62)	8509003
---	Socket, 16-Pin (U63)	8509003
---	Socket, 16-Pin (U64)	8509003
---	Socket, 16-Pin (U65)	8509003
---	Socket, 16-Pin (U66)	8509003
---	Socket, 16-Pin (U67)	8509003

Miscellaneous

Ref No.	Description	Part No.
---	16-Bit, 128K Memory Board Main Ass'y	8898004
---	PC Board, Memory 128/256 K Rev (PP2)	8709236
S1	Switch, DIP, 16-Pin	8489004
---	Cable, 34 Pos, Int. Bus. Ext. II	8709278
---	Cable, 50 Pos, Int. Bus. Ext. II	8709279

Schematic, Memory Board, 8000127, Page 1 of 2

7.4   I/O Processor I/O Processor Board

The I/O Processor I/O Processor Board is a complete
eight-bit microprocessor system minus the video interface.
The board features the Z80A family of ICs which provides two
serial communications channels (RS-232), a printer interface
(parallel) and DMA capability. Additionally, it has two
Floppy Disk interfaces and 64K bytes of RAM memory
expandable to 128K bytes. The system is functionally
equivalent and software compatible with the TRS-80 MODEL II.

A block diagram of the board is shown in Figure 7-5. From
this diagram, it can be seen that the board is divided
functionally into three sections; CPU, MEMORY and
PERIPHERAL. The CPU section consists of a Z80A
micro-processor, Z80A DMA, and the support circuitry to
control the bus. The MEMORY section consists of 64K/128K of
dynamic RAM, 2K of ROM, and the necessary timing control
circuity. The PERIPHERAL section consists of a Z80A CTC,
SIO (serial), PIO(printer), a FLOPPY DISK CONTROLLER and a
sound circuit interface.

7.4.1   CPU Section

1.   Processor
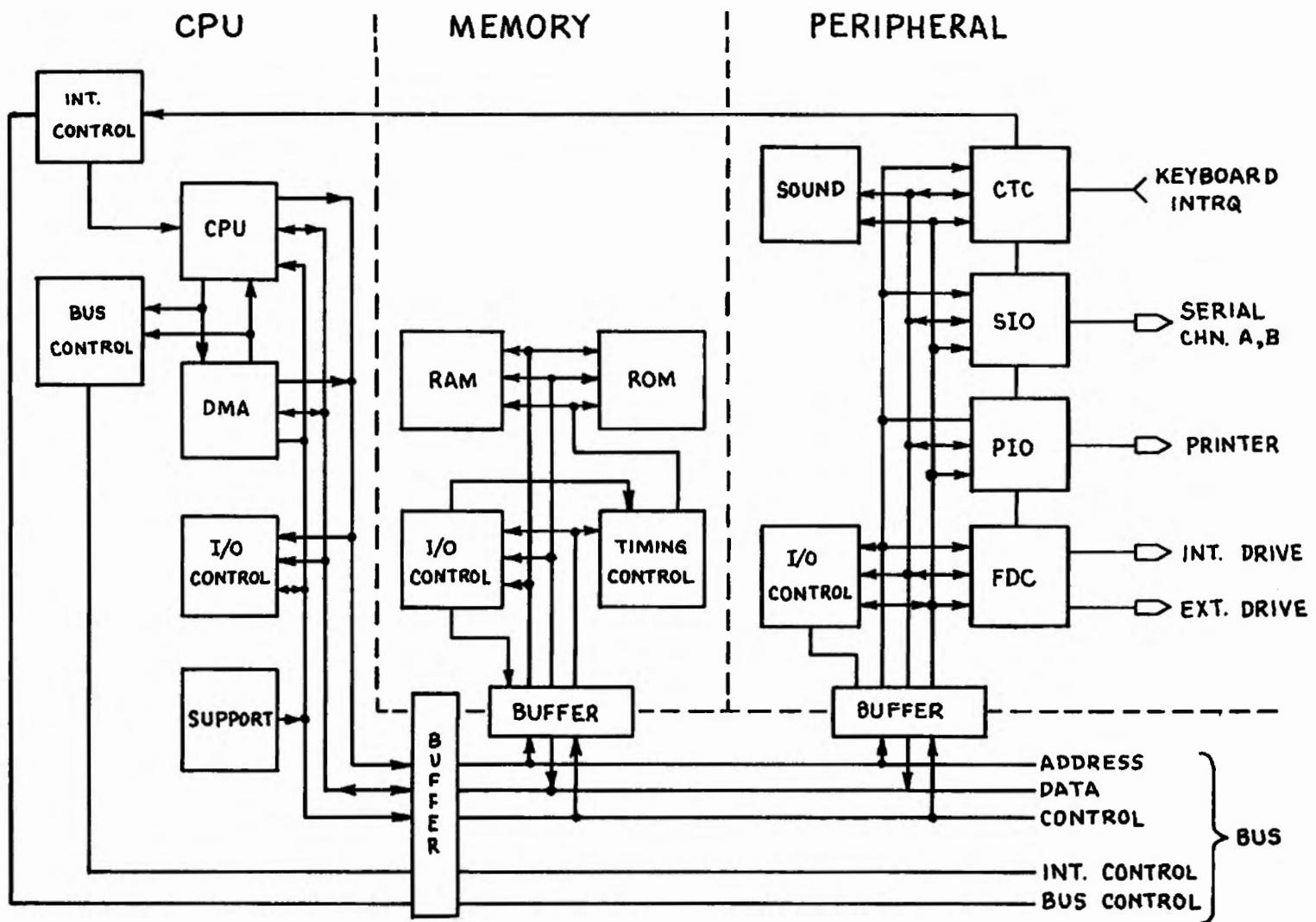
The PROCESSOR subsection consists of the Z80A CPU and DMA
VLSI ICs. For particular details, refer to the
manufacturer's specifications for these parts in Appendix A.
The Z80A CPU operational particulars are 4.0 MHz clock
rate, Mode 2 interrupt processing and control of memory
refresh. The DMA and the CPU are both 'bus masters' and
share the same bus support and buffer circuity.

2.   Support

The SUPPORT subsection consists of the Reset, Clock and Wait
circuits.

*RESET (schematic, sheet 2)- consists of two parts -
"power-on" and "manual". Before power is applied, all
capacitors are discharged. Upon power application, the
first comparator (1/4 of U4, output pin 14) waits until the
+5 VDC has risen above +4 V at which time it triggers (pin 8
is reference input 4V determined by CR1). C24 slows +5V
input into pin 9, starting the charging of C3. The   second

CPU

MEMORY

PERIPHERAL

INT. CONTROL

CPU

BUS CONTROL

DMA

I/O CONTROL

SUPPORT

BUFFER

RAM

ROM

I/O CONTROL

TIMING CONTROL

BUFFER

SOUND

CTC

KEYBOARD INTRQ

SIO

SERIAL CHN. A,B

PIO

PRINTER

I/O CONTROL

FDC

INT. DRIVE

EXT. DRIVE

BUFFER

ADDRESS

DATA

CONTROL

INT. CONTROL

BUS CONTROL

BUS

Figure 7-5. I/O Processor PCB Block Diagram

comparator triggers when C3 is charged to generate a pulse of at least 100 microseconds. On a "manual" reset (front panel switch), a third comparator generates a pulse longer than the (normal) switch bounce. The trailing edge of this pulse triggers a one-shot pulse of at least 50 microseconds. The two pulses -- "power on" and "manual" -- are logically ORed together to make the system reset signal RST/.

*CLOCK (schematic, sheet 2)- consists of an oscillator (half of U13), a divider (U6) and a buffer (half of U13). The oscillator frequency is 8.00 MHz and is crystal-controlled for stability. It is connected to the frequency divider by jumper E4-E5, which is provided to isolate the clock for testing purposes. The divider converts the 8.0 MHz into a 4 MHz clock and a 2 MHz clock that are then buffered by TTL gates for system use. In addition, the 4 MHz clock is also applied to a special buffer to generate the Z80 family high level clock. This special buffer uses a transistor (Q1) with a low Vce saturation as an active pull-up to obtain the required Voh of +4.6/5.2 V. The '04 TTL gate provides the Vol of +0.8/-0.3 V and switches the transistor on/off through the resistor network (R19,R20,C6).

*WAIT (schematic,sheet 1) - consists of two parts; a "fixed" wait circuit and an "user" wait circuit. The "fixed" wait circuit (U3) generates a "wait" request signal under two conditions. The first is when the boot ROM is enabled. The ROM has an access time longer than a normal CPU memory cycle and therefore it is necessary to insert a "wait" cycle for every memory access cycle. The second condition is when the ROM is disabled. The fetch (M1) cycle of every memory access is followed by a memory refresh cycle. To ensure sufficient dynamic RAM precharge time, a "wait" is inserted each time. The "user" wait circuit receives the signal EWAIT/ from any user on the BUS that requires longer access times than the CPU normally provides (example is the Video /Keyboard Interface PCB). Each user has an open-collector buffer for a wire-OR connection to the BUS. The CPU section simply provides the pull-up for the common output. For the CPU, the "fixed" and the "user" wait signals are ORed together and applied directly to the CPU. For the DMA, the "wait" and "chip select" signals share the same IC pin. These two signals are logically combined with BUSACK and BAO to choose between F8 (chip select) and EWAIT/. If BUSACK/ is false, F8 is applied. If BUSACK/ and BAO are true, the DMA is the bus master and EWAIT/ is applied. The DMA uses only the "user" wait signal EWAIT/.

3. Buffers

The CPU and DMA are bus masters; they transmit the address and control signals onto the bus. Data is both transmitted and received by all entities on the bus.

*Address buffers (U24,U25)- Disabled only if external bus master has control (BAO = lo)

*Control buffers (U26,U27)- Disabled only if external bus master has control (BAO = lo).

*Data transceiver (U30)- directional control signals IN (read), OUT (write). OUT is the defaulted direction; disabled if external bus master has control. IN equals CPU/DMA READ unless:

    1. CPU I/O read of DMA (DMARD) = lo

    2. CPU reading the DMA interrupt vector (INACKOFF/) = lo.

4. I/O Control

The I/O Control decodes the address and control signals to create the CPU section port read/write strobes MEMCFG/, SYSCFG/, OPSCFG/ and F8 plus the logic discretes F8IO and DMARD. The decoder is U10, a custom logic array. See Table 7-5 for a listing of each port strobe and its use.

5. Bus Control

The Bus Control circuity receives the "bus requests" from the DMA and other bus masters on the BUS and provides the logic for arbitrating the "bus grant" from the CPU. The Bus Control circuit has two parts, input and output. The input circuit ORs the "bus request" signals BUSREQ/ (from the DMA) and BUSREQ* (from the BUS) for the CPU. Each bus master is connected to the BUS through an open-collector buffer to wire-OR all requests. The CPU provides the common pull-up for the output. The output circuit buffers the DMA daisy-chain acknowledge signal BAO onto the BUS for any external bus master (none at present).

PORT	STROBE NAME	READ	WRITE
FF	MEMCFG/	Bits 7-0: 7=KBIRQ, 6=BLANK VIDEO, 5=RTC EN, 4=80 CHAR, 3 2 1 0=DON'T CARE. (6,5,4 = ON VIDEO BD)	Bits 7-0: 7=VIDEO ENABLE, 6=BLANK VIDEO, 5=RTC EN, 4=80 CHAR, 3=BANK SEL C, 2=BANK SEL B, 1=BANK SEL A, 0=PAGE SEL. (7,6,5,4 = ON VIDEO BD)
F9	SYSCFG/	NO FUNCTION	Bits 7-0: 7 6 5 4 3 2 1=DON'T CARE, 0=ROM ENABLE
F8	F8/	DMA STATUS	DMA COMMAND
F4-F7	SIOCE/	SIO STATUS AND DATA	SIO COMMAND AND DATA
FØ-F3	CTCCE/	CTC	CTC
EF	DRVSEL/	NO FUNCTION	Bits 7-0: 7=DOUBLE DENSITY, 6=SIDE SELECT, 5=DON'T CARE, 4=DRIVE 3 SEL, 3=DRIVE 2 SEL, 2=DRIVE 1 SEL, 1=DON'T CARE, 0=DRIVE Ø SEL

Table 7-5.   Input/Output Port Map

E8	SOFTMR/	NO FUNCTION	FDC RESET
E4-E7	FDCCE/	FDC STATUS AND DATA	FDC COMMAND AND DATA
EØ-E3	PIOCE/		PIO COMMAND AND DATA
EØ		*(bits 7–0: PRINTER BUSY, OUT OF PAPER, PRINTER SELECT, PRINTER FAULT, DON'T CARE, DOOR OPEN, 2 SIDE DISK, FDC INT)*	*(bits 7–4 DON'T CARE, bit 3 PRINTER RST, bits 2–0 DON'T CARE)*
A8	OPSCFG/	NO FUNCTION	*(bits 7–1 DON'T CARE, bit 0 LOW MEMORY PAGE)*
AØ	SNDCE/	NO FUNCTION	*(bits 7–1 DON'T CARE, bit 0 SOUND ON)*

Table 7-5. Input/Output Port Map (con't)

6. Interrupt Control

The CPU has two types of interrupts; maskable (INT/) and
non-maskable (NMI/). The non-maskable interrupt (bus name
NMIRQ*) is a Method 1 type interrupt (see Z80
specification). The sources for this signal are on the BUS
only. Like the "wait" and "bus request" signals, the
sources apply their signal onto the bus through an
open-collector buffer and the CPU section provides the
pull-up resistor for the wire-OR output. At present, the
only source for this signal is the REAL TIME CLOCK on the
Video/Keyboard Interface PCB. The maskable interrupt
(INTRQ/) is a Mode 2 type interrupt. All sources are on a
daisy-chain priority scheme where interrupt requests from
all sources are ORed together but who gets to make the
request is established by the acknowledge from the CPU being
passed from the highest priority IC down until the requestor
stops it, preventing lower priority ICs from responding
(IEI,IEO). The requestors are divided into two groups;
internal (INTRQ/) from the BOARD, and external (INTRQ*) from
the bus. The priority scheme has the four Z80A functions on
the board assigned the highest priority with a descending
priority of CTC, SIO, DMA and PIO. The bus continues the
priority scheme and establishes priority by position
(provided a back plane with connectors is present) by
daisy-chaining the acknowledges IEIN* (IEI), IEOUT* (IEO).
If a board slot is empty, that stops the chain.

7.4.2 Memory Section

1. RAM

The RAM memory section consists of two sets of 8 dynamic RAM
ICs and an address multiplexer. The first or base set of
RAM (U82-U89) is 64K in size; the second set (U63-U70) is
either 16K or 64K in size. The RAM memory is divided into
32K size groups called Pages of which there can be as many
as 16 (0-15). See Table 7-6 for a memory map. Page 0 is
called the Base Page and is always available at address
0-32K (if LOW PAGE = low; if LOW PAGE = hi, address
32K-64K). The other Pages are selected one at a time by a
value (01-0F) at port FF and respond in the address range
32K-64K (if LOW PAGE = low; if = hi address 0-32K). The
addresses for dynamic RAMs require multiplexing. This is
done by U52, U53, and U79. The upper address bits are
combined with the lower address in pairs to form RAC*s.

PAGE   0 1 0 1
BANK   0 0 7 7

ROM

0000
0FFF

4K

U82-U89
(ALL)

A15=0
0000-7FFF

ROM 0000-0FFF

7FFF

8000

U82-U89

BANK∅

A15=1
8000-FFFF

VIDEO F800-FFFF

F800
FFFF

VIDEO

0000

16K

BANKSEL

32K

U63-U70

3FFF

7800
7FFF

8000

U63-U70

Z80 ADDRESS

PHYSICAL ADDRESS

F800
FFFF
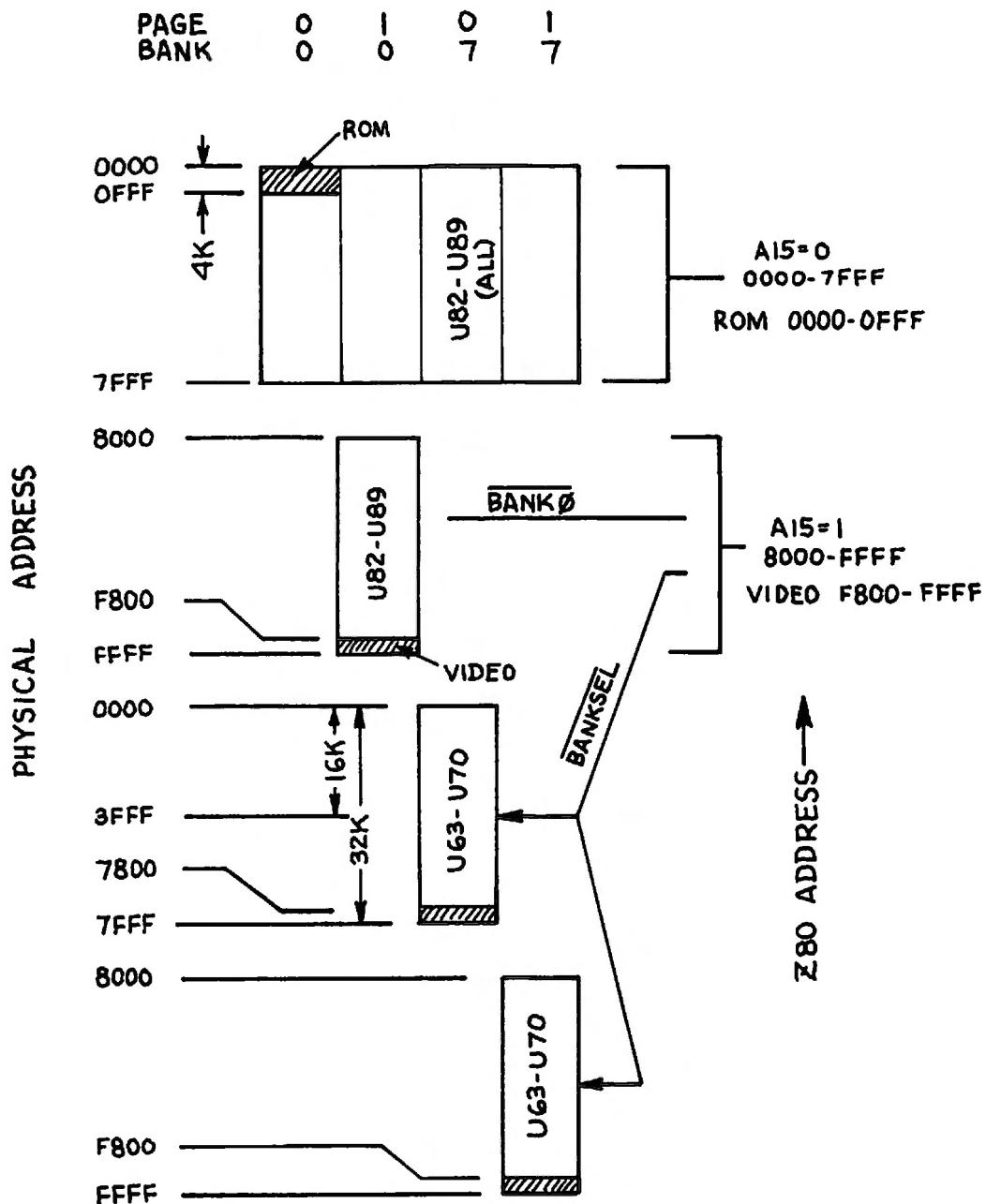
Table 7-6.   Memory Map

RAC0 through RAC5 are usable for 16K and 64K RAMs, both
banks. Unique address combinations are 16RAC6 (16K only,
address bit 6), 64RAC6 (64K only, address bit 6), L64RAC7
(lower 64K address bit 7), and U64RAC7 (upper 64K address
bit 7). Jumper options in the RAM section allow different
configurations to be selected. See Table 7-7 for details.

Timing signals come from the TIMING/CONTROL section, which
will be covered later.

2. ROM

The ROM memory subsection consists of U54, a 2K x 8 PROM
called the BOOT ROM. This ROM memory shadows the RAM memory
address space in the range 0-2K. This memory is available
only if the discrete signal ROM from the port F9 is true.
When the BOOT ROM is enabled, the shadowed RAM memory is
write only (read disabled). An option to upgrade to a 4K x
8 part is provided by a jumper option for the address bit
11. Timing signals come from the TIMING/CONTROL
section, which will be covered later.

3. I/O Control

The I/O CONTROL consists of a latch U51. The data is
stored in the latch by the I/O Port strobe MEMCFG/ from the
CPU Section. The outputs PAGE, BASEL, BBSEL, BCSEL are
converted to BANK0 (Page 0, 1) and BANKSEL (Page 2,3 OR 4,5
OR....14,15) by U61. See Table 7-7 for page select jumper
options. The VIDEO discrete enables the video RAM
memory, which shadows the memory address range F800-FFFF.
The I/O port discretes ROM and LOW PAGE originate from a
latch in the CPU section.

E18, E19, E20	ROM SIZE OPTION	
★	E18-E19	2K×8 ROM A11 = +5V
	E19-E20	4K×8 ROM A11 = A11
E24, E25, E26	FLOPPY DRIVE HEAD LOAD DELAY OPTION	
★	E24-E25	NO DELAY
	E25-E26	60 MILLISECOND DELAY
E27, E28, E29	FLOPPY DRIVE SIGNAL "READY" SOURCE	
★	E27-E28	FROM FLOPPY DRIVE
	E28-E29	SELECT LOGIC
E30, E31, E49	FLOPPY CONTROLLER TEST MODE	
	E30-E31	TEST
	E31-E49	NORMAL
<u>E40, E41</u>	INTERNAL FLOPPY DRIVE OPTION	
★	E40-E41	1 INTERNAL DRIVE (∅)
	OPEN	2 INTERNAL DRIVES (∅,1)
E42, E43, E44, E45, E46, E47, E48	RAM U63-U70 CONFIGURATION OPTION	
	FOR 16K (PIN 4116)	
★	E42-E45	−5VDC TO PIN 1
	E44-E45	−12VDC TO PIN 8 (NO CONNECTION TO E48)
	E46-E47	+5VDC TO PIN 9
	FOR 64K (PIN 6665)	
	E45-E46	+5VDC TO PIN 8
	E47-E48	URAC7 TO PIN 9 (NO CONNECTION TO E42, E43, E44)
E32 THRU E39	RAM BANK SELECTION OPTION, U63-U70	
	E32-E39	BANKSEL = PAGE 2,3
★	E38-E39	BANKSEL = PAGE 15,16
		(E33 THRU E37 NOT INSTALLED)

★ FACTORY SETTING

IF DRIVE 1 IS NOT PRESENT INTERNALLY YOU MUST DRIVE SELECT EXTERNAL DRIVES FOR DRIVE 2 + 3 ONLY DRIVE 1 IS SEEN INTERNALLY ONLY.

Table 7-7. Jumper Options

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E1, E2, E3	RAM WAIT STATE OPTIONS	
★	E1-E2	WAIT STATE INSERTED DURING M1 CYCLE
	E2-E3	NO WAIT STATES
E4, E5	CLOCK OSCILLATOR OPTION	
★	E4-E5	8 MHZ OSCILLATOR CONNECTED TO CLOCK DIVIDER
	OPEN	NO CONNECTION
E6, E7, E8	OPTIONS FOR SERIAL CHANNEL B BAUD CLOCK	
★	E7-E8	INTERNAL (CTC) CLOCK SOURCE
	E6-E7	EXTERNAL CLOCK SOURCE
E9, E10, E11, E12	OPTIONS FOR SERIAL CHANNEL A BAUD CLOCK	
★	E10-E11	INTERNAL (CTC) CLOCK SOURCE
	E11-E12	EXTERNAL CLOCK SOURCE
	E9-E10	INTERNAL CLOCK ROUTED TO EXTERNAL- IN ADDITION TO E10-E11
E13, E14	PRINTER INTERFACE SIGNAL "PRIME" OPTION	
	E13-E14	CONNECTED
★	OPEN	NO CONNECTION
E15, E16, E17	RAM ADDRESS BIT 6 OPTION, U62- U69	
	E15-E16	16K OPERATION: 16RAC6
	E16-E17	64K OPERATION: 64RAC6

★ FACTORY SETTING

Table 7-7.   Jumper Options (con't)

E50, E51, E52	RAM UPPER BANK SIZE OPTION	
	E50-E52	64K SIZE
	E51-E52	16K SIZE
E53, E54, E55	OPTIONS FOR SERIAL CHANNEL A RECEIVE BAUD CLOCK	
*	E53-E54	INTERNAL (CTC) CLOCK SOURCE
	E53-E55	EXTERNAL CLOCK SOURCE

* FACTORY SETTING

Table 7-7. Jumper Options (con't)

4. TIMING/CONTROL

The TIMING/CONTROL subsection (schematic, sheet 5, 6) provides the necessary signals to access the memory and control the data transceiver. This circuitry includes the memory controller U50, RAM timing generator circuit U39, U62, U80, U81 and ROM timing and data transceiver control U60, U49. The memory controller U50 decodes the addresses A11-A15, memory configuration discretes ROM, VIDEO, BANK0, BANKSEL, LOW PAGE and 16K to determine if a memory access should be in progress and, if it is, whether it is for ROM or for RAM. For ROM (ROM = hi, address range 0000-0FFF), the outputs ROMSEL and ROMAD are true (hi). If for RAM, BANK0 = lo, PAGE = hi (address 0000-FFFF unless VIDEO = hi, then address 0000-F800), the outputs RASEN0, CASEN are set true (hi). If for RAM, BANKSEL = lo (address 8000-FFFF unless VIDEO = hi, then address 8000-F800 unless 16K = hi then address 8000-BFFF) RASEN1, CASEN are set true (hi). If for Video memory, (VIDEO = hi, address F800-FFFF), the outputs are all false (lo). The input REFRESH sets all the outputs false during its true time. The AND-OR gate U39 is the RAM memory access decoder generating MEMREQ/, which triggers the RAS-CAS timing sequencer U61, U80, and U81. The equation for U39 is (MREQ*WRITE + MREQ*ROM*ROMAD*READ + MREQ*RAM*READ). Basically, this allows write access to the RAM memory for all addresses but limits the read accesses to only those addresses not shadowed by the ROM memory if ROM is true.

The RAM timing sequencer generates the RAS, CAS and MUXSEL to read, write and refresh the dynamic RAM ICs. For the lower memory bank RAS0, MUXSEL and CAS are required; for the upper bank RAS1, MUXSEL and CAS are needed. (RASEN0 and RASEN1 never occur together). The fixed timing sequence is generated by the delay line U80. When MEMREQ/ goes true (lo), (and for instance, RASEN0, CASEN are true) U81.6, U62.6 are set lo, and U81.7 stays hi. U81.6 sets RAS0P lo and U62.6 starts a negative level through the delay line. The 150 nanosecond tap clears U62.6, thereby creating a 150 ns negative pulse. This pulse, delayed 30 ns, = MUXSEL/, which switches the address multiplexer from the row address to the column address. The pulse delayed 60 ns sets U62.7 or CASP lo. The pulse delayed 240 ns clears RAS0P (U62.7). CASP flip-flop U81.7 is cleared by the trailing edge of MEMREQ/. This establishes a minimum length RAS* (240 ns) to insure the minimum pre-charge time for the RAS only REFRESH cycle to follow (if M1 cycle). Now, RASP (RAS Prime) is ORed with (MREQ*REFRESH) (RAS refresh) and applied to U82-U89 through damping resistor R60. CASP (CAS Prime) is buffered to U63-U89 through damping resistor R59.

The ROM timing sequence is simply (MREQ*ROMSEL) = ROMCE/;
chip select and (ROMSEL*READ) = ROMOE/; output enable.
REFRESH clears ROMSEL during refresh.

5. BUFFERS

The address buffers U42-43 receive the addresses from the
BUS and apply them to the multiplexers, ROM and the memory
controller.

The data transceiver is U44. Directional control is
provided by logic gates U41, U49 and U60. The signals IN/
and OUT/ are normally off (hi) unless access is being made
to the memory. U60 ORes the five signals that define the
timing windows for this access - [(RAS0P*CASP + RAS1P*CASP)
+ ROMCE/ + MEMCFG/]. A disable signal DISO* (DISable Output,
not presently used) negates the enable of U60.

7.4.3 Peripheral

1. CTC

The CTC is the Z80A COUNTER/TIMER CIRCUIT. It has two
functions. One, it is used as a baud rate generator for the
SIO function. Here channel 0 and 2 are tied together to
provide a square wave clock for both channels of the SIO
serial interface. Second, it is an interrupt processor for
two interrupt signals; one from the keyboard KBIRQ* and
USEIRQ* a growth input on the BUS. See schematic, sheet 3.

2. SIO

The SIO is the Z80A SERIAL INPUT/OUTPUT CONTROLLER. It
provides two channels of serial (RS-232-C) communication.
The two channels are labeled Channel A and Channel B.
Channel A can be either synchronous or asynchronous.
Channel B can be asynchronous only. They are available
through flat ribbon cables at connectors at the rear of the
chassis. The serial input/ output interface of the SIO is
buffered by U7, U8, U14, U15 and U23 - line drivers and
receivers operating from +12/-12VDC. Jumper options allow
either external or internal (CTC) clocks for operation. See
Table 7-7 for jumper details. See schematic, sheet 3. See
Section 5 for a description of the SIO connector pin
designations.

3.   PIO

The PIO is the Z80A PARALLEL INPUT/OUTPUT CONTROLLER.   It
provides two parallel data interfaces; one is used as the
data port for the printer and the other is used as an input
port for status from the Floppy Disk Drive and Printer.
Since both ports are interrupt driven, the second port (B)
is used as an interrupt controller by the Floppy Disk
Controller for data transfers.   The printer interface (B),
uses the output ready signal BRDY to trigger a one-shot to
provide a 2.0 microsecond pulse for the printer handshake.
See schematic, sheet 4.   See Section 5 for a description of
the PIO connector pin designations.

4.   FDC

The FDC is the FLOPPY DISK CONTROLLER function.   This
circuit is designed to read and write an 8" Floppy Disk
Drive (FDD) using single or two sided media in both single
and double density formats.   The major component in this
circuit is the WD 2793 VLSI IC.   This part synchronizes,
reconstructs and reads the data, reads/writes status and
provides write data in the proper format for a floppy disk
drive.   Additionally, it communicates with the CPU as an I/O
device.   Interface circuity is provided to interface with
two sets of FDDs - 1 or 2 internal drives (in chassis) and 1
or 2 external expansion drives.   Since the FDDs in a set are
connected in parallel, only one set of drivers and receivers
is required for each, the internal and the external set.
The drivers are open-collector inverter gates designed to
drive into a 150 ohm load to +5 vdc provided by one of the
FDDs in a set.   The receivers are 2:1 multiplexers - one
channel for internal, one for external.   The board provides
the 150 ohm pull-up for the FDDs.   FDD drive select logic is
provided by programmable logic array U47.   Here, the CPU via
I/O port EF elects a single drive it wishes to communicate
with, selects data density - single or double, and
determines which channel of the input status mux to select.
The head load timing circuit is provided for FDDs that have
a seperate circuit for this function that times out the
mechanical bounce.   (In some newer FDDs, the head is loaded
when the disk is installed but the motor is turned ON/OFF.)
The one-shot is set-up for 3.0 milliseconds.   See Table 7-7
for jumper options.   See schematic, sheet 4.   See Section 5
for a description of the FDC connector pin designations.

See Disk Drive Manual for alignment instructions.

5. SOUND
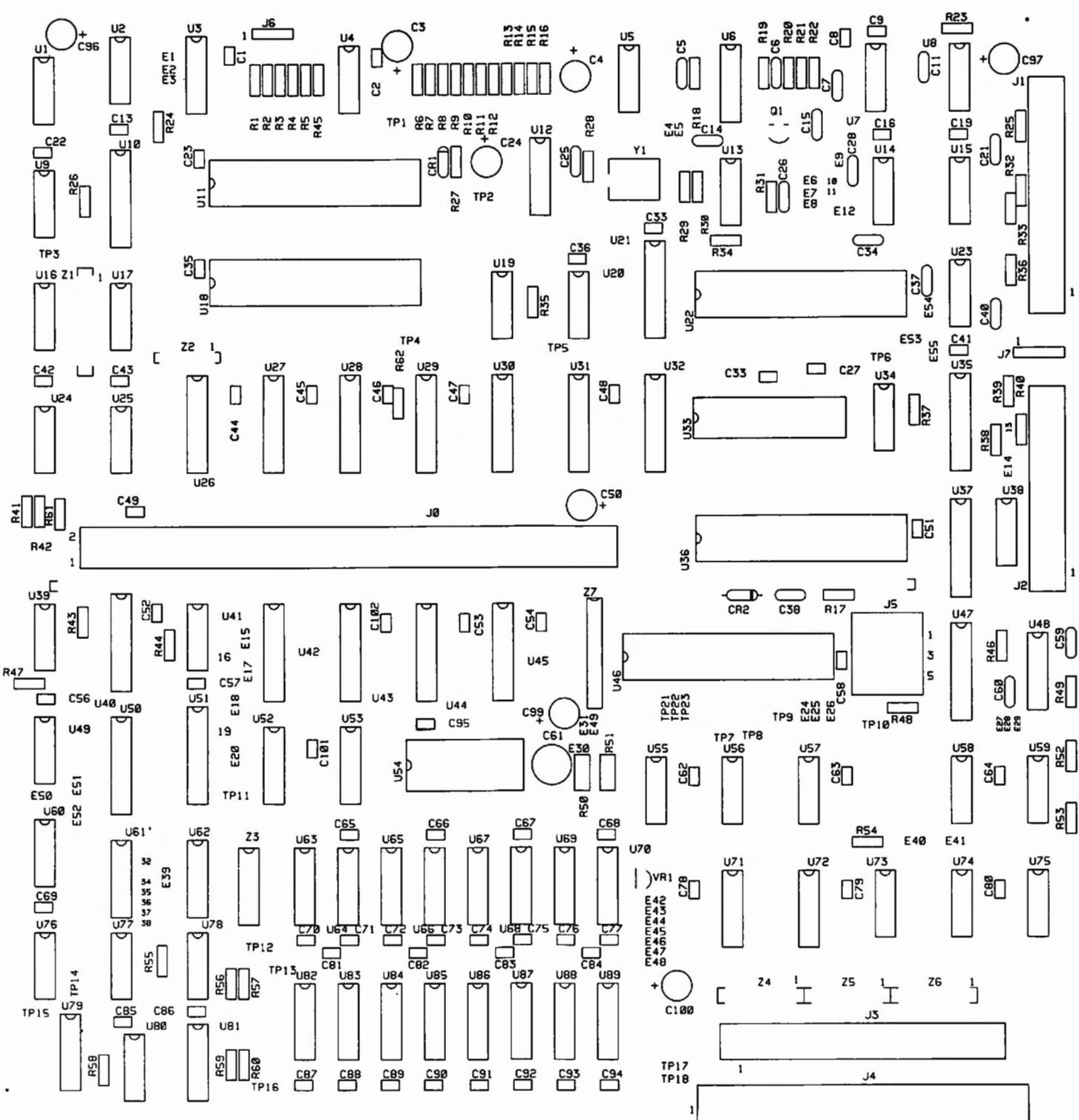
The SOUND function is an oscillator of fixed frequency and variable duration under software control. The oscillator is located on a separate satellite board. Power and tone duration control are provided by the I/O Processor PCB. The tone control circuit is 1/2 of D flip-flop U38. The sound is enabled as long as the signal SOUND = low. SOUND is the complement of U38.6, which is equal to CPU data bit 0 when I/O port strobe SNDCE/ (A8) is applied. See schematic, sheet 2 for the oscillator and sheet 4 for the control circuit.

6. I/O CONTROL

The I/O CONTROL circuit for the Peripheral section is U21, a programmable logic array. See Table 7-5 for address and function of the I/O ports CTCCE/, SIOCE/, PIOCE/, FDCCE/, SNDCE/, DRVSEL, SOFTMR/ and PGSEL/.
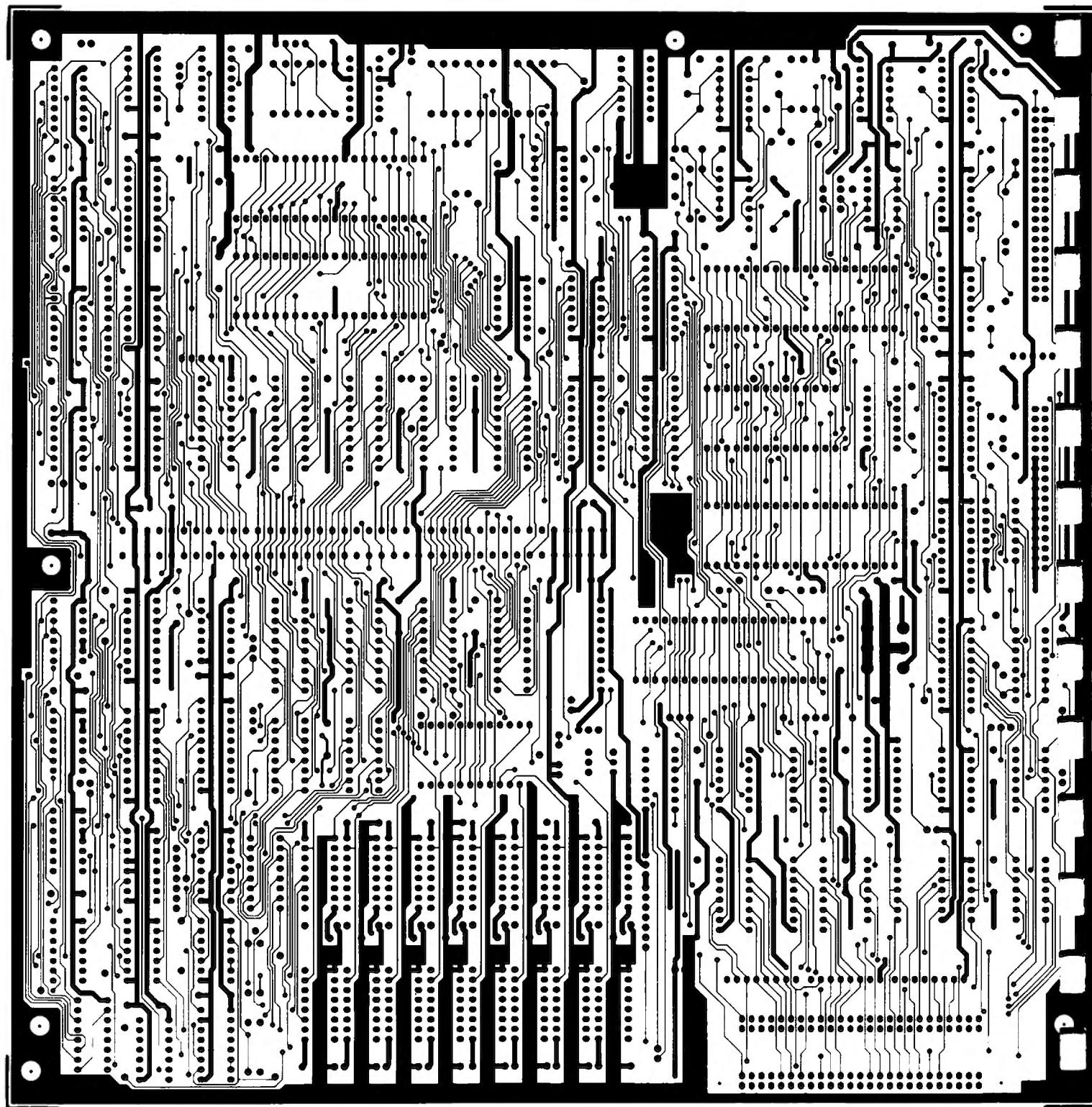
7. BUFFERS

The address and control buffers U31, U32, U56 are straight-forward, simple line receivers. The data transceiver control circuitry -- U5, 20, 29, 55 -- determines the direction of data flow. The default direction is in or write. To switch to read (drive the BUS), two conditions must occur. The first is that {PGSEL*READ} is true (low). (PGSEL is true if any of the other outputs of U47 is true). The second condition is that one of the three functions CTC, SIO or PIO has an interrupt acknowledge pending. See schematic, sheet 3.
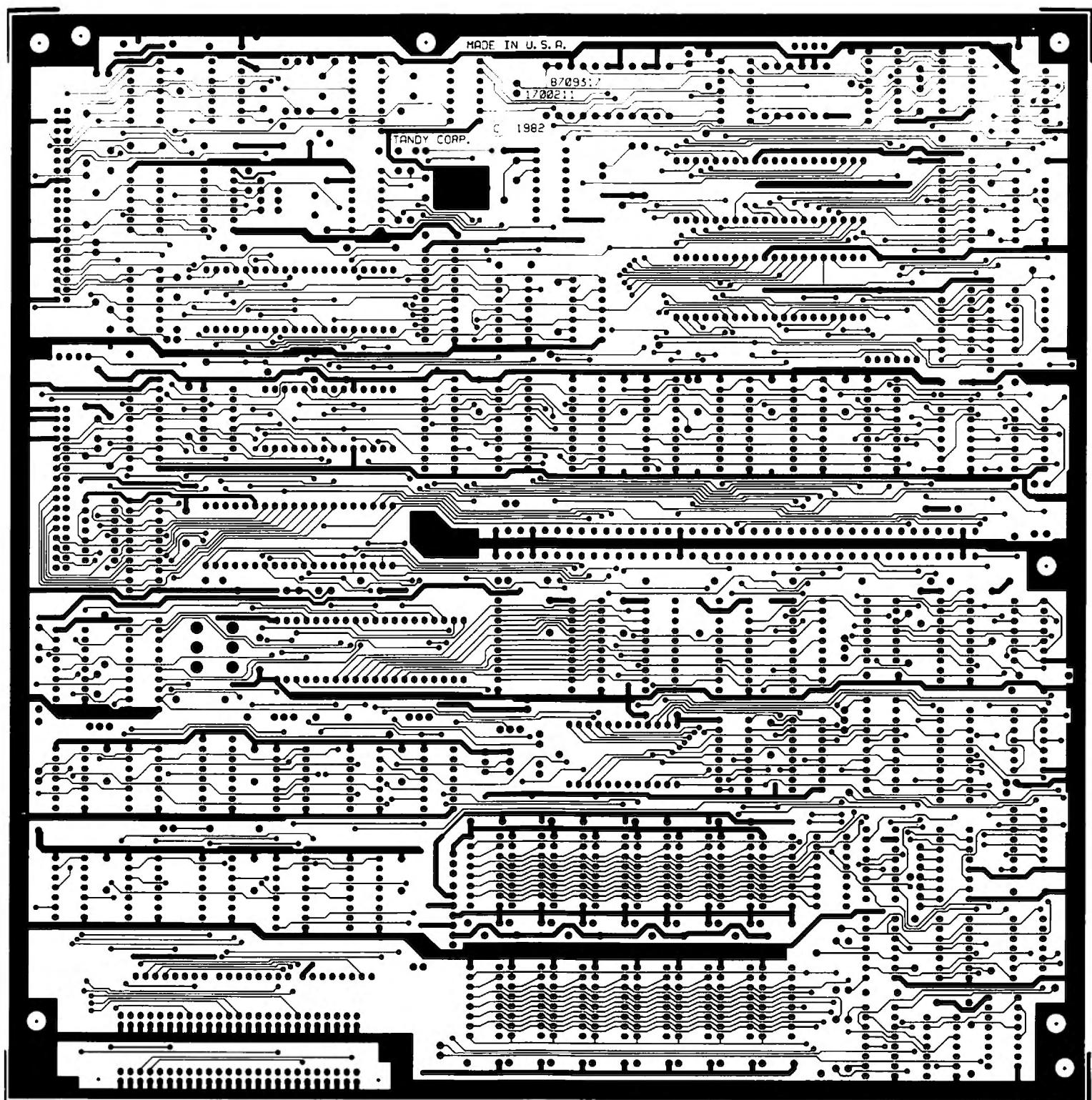
Component Layout, I/O Processor PCB 8898423

Circuit Trace, I/O Processor PCB 8898423, Component Side

Circuit Trace, I/O Processor PCB 8898423, Solder Side

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
C1	Capacitor, 0.1 uF, 50V	8374104
C2	Capacitor, 0.1 uF, 50V	8374104
C3	Capacitor, 1 uF, 16V, Elec Rad	8325101
C4	Capacitor, 10 uF, 16V, Elec Rad	8326101
C5	Capacitor, 100 pF, 50V, C Disk	8301104
C6	Capacitor, 33 pF, 50V, C Disk	8300334
C7	Capacitor (For future design use)	-------
C8	Capacitor, 0.1 uF, 50V	8374104
C9	Capacitor, 0.1 uF, 50V	8374104
C10	Not Used	
C11	Capacitor (For future design use)	-------
C12	Not Used	
C13	Capacitor, 0.1 uF, 50V	8374104
C14	Capacitor, 470 pF, 50V, C Disk	8301474
C15	Capacitor, 100 pF, 50V, C Disk	8301104
C16	Capacitor, 0.1 uF, 50V	8374104
C17	Not Used	
C18	Not Used	
C19	Capacitor, 0.1 uF, 50V	8374104
C20	Not Used	
C21	Capacitor (For future design use)	-------
C22	Capacitor, 0.1 uF, 50V	8374104
C23	Capacitor, 0.1 uF, 50V	8374104
C24	Capacitor, 1 uF, 16V, Elec Rad	8325101
C25	Capacitor, 1000 pF, 50V, C Disk	8302105
C26	Capacitor, 100 pF, 50V, C Disk	8301104
C27	Capacitor, 0.1 uF, 50V	8374104
C28	Capacitor (For future design use)	-------
C29	Not Used	
C30	Not Used	
C31	Not Used	
C32	Not Used	
C33	Capacitor, 0.1 uF, 50V	8374104
C34	Capacitor (For future design use)	-------
C35	Capacitor, 0.1 uF, 50V	8374104
C36	Capacitor, 0.1 uF, 50V	8374104
C37	Capacitor (For future design use)	-------
C38	Capacitor, 0.1 uF, 63V, 10%, Mtl Flm	8394103
C39	Not Used	
C40	Capacitor (For future design use)	-------
C41	Capacitor, 0.1 uF, 50V	8374104
C42	Capacitor, 0.1 uF, 50V	8374104
C43	Capacitor, 0.1 uF, 50V	8374104
C44	Capacitor, 0.1 uF, 50V	8374104
C45	Capacitor, 0.1 uF, 50V	8374104

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Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description				Part No.
C46	Capacitor,	0.1 uF,	50V		8374104
C47	Capacitor,	0.1 uF,	50V		8374104
C48	Capacitor,	0.1 uF,	50V		8374104
C49	Capacitor,	0.1 uF,	50V		8374104
C50	Capacitor,	10 uF,	16V,	Elec Rad	8326101
C51	Capacitor,	0.1 uF,	50V		8374104
C52	Capacitor,	0.1 uF,	50V		8374104
C53	Capacitor,	0.1 uF,	50V		8374104
C54	Capacitor,	0.1 uF,	50V		8374104
C55	Not Used				
C56	Not Used				
C57	Not Used				
C58	Not Used				
C59	Capacitor,	200 pF,	NPO,	C Disk	8301203
C60	Capacitor,	0.68 uF,	35V,	Tant.	8334683
C61	Capacitor,	5-60 pF,	NPO,	Trim	8360550
C62	Capacitor,	0.1 uF,	50V		8374104
C63	Capacitor,	0.1 uF,	50V		8374104
C64	Capacitor,	0.1 uF,	50V		8374104
C65	Capacitor,	0.1 uF,	50V		8374104
C66	Capacitor,	0.1 uF,	50V		8374104
C67	Capacitor,	0.1 uF,	50V		8374104
C68	Capacitor,	0.1 uF,	50V		8374104
C69	Capacitor,	0.1 uF,	50V		8374104
C70	Capacitor,	0.1 uF,	50V		8374104
C71	Capacitor,	0.1 uF,	50V		8374104
C72	Capacitor,	0.1 uF,	50V		8374104
C73	Capacitor,	0.1 uF,	50V		8374104
C74	Capacitor,	0.1 uF,	50V		8374104
C75	Capacitor,	0.1 uF,	50V		8374104
C76	Capacitor,	0.1 uF,	50V		8374104
C77	Capacitor,	0.1 uF,	50V		8374104
C78	Capacitor,	0.1 uF,	50V		8374104
C79	Capacitor,	0.1 uF,	50V		8374104
C80	Capacitor,	0.1 uF,	50V		8374104
C81	Capacitor,	0.1 uF,	50V		8374104
C82	Capacitor,	0.1 uF,	50V		8374104
C83	Capacitor,	0.1 uF,	50V		8374104
C84	Capacitor,	0.1 uF,	50V		8374104
C85	Capacitor,	0.1 uF,	50V		8374104
C86	Capacitor,	0.1 uF,	50V		8374104
C87	Capacitor,	0.1 uF,	50V		8374104
C88	Capacitor,	0.1 uF,	50V		8374104
C89	Capacitor,	0.1 uF,	50V		8374104
C90	Capacitor,	0.1 uF,	50V		8374104

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
C91	Capacitor, 0.1 uF, 50V	8374104
C92	Capacitor, 0.1 uF, 50V	8374104
C93	Capacitor, 0.1 uF, 50V	8374104
C94	Capacitor, 0.1 uF, 50V	8374104
C95	Capacitor, 0.1 uF, 50V	8374104
C96	Capacitor, 33 uF, 16V, Elec Rad	
C97	Capacitor, 33 uF, 16V, Elec Rad	
C98	Not Used	
C99	Capacitor, 10 uF, 16V, Elec Rad	8326101
C100	Capacitor, 33 uF, 16V, Elec Rad	
C101	Capacitor, 0.1 uF, 50V	8374104
C102	Capacitor, 0.1 uF, 50V	8374104

Connectors

J0	Connector, 80-Pin, Edge Card	8519014A
J1	Connector, 40-Pin, Vertical Hood	8519159
J2	Connector, 34-Pin, Vertical Hood	8519158
J3	Connector, 50-Pin, Vertical Hood	8519160
J4	Connector, 50-Pin, Rt. Angle	8519164
J5	Connector, 6-Pin, Power	8519015
J6	Connector, 4-Pin, Rt. Anlge	8519053
J7	Connector, 5-Pin, Straight	8519161

Diodes

CR1	Diode, 1N5222, 2.5V Zener	8150222
CR2	Diode, 1N914	8150148

Integrated Circuits

---	IC, DDU-7J-300, Delay Line	8429017
---	IC, Z80A, SIO/O	8047884
---	IC, 2716, EPROM	8040716
U1	IC, 74LS74 Dual Flip-Flop	9020074
U2	IC, 74S10 Triple3-In NAND	9010010
U3	IC, 74LS175 Quad Flip-Flop	9020175
U4	IC, LM339 Linear Quad Comparator	9050339
U5	IC, 74LS04 Hex Inverter	9020004
U6	IC, 74LS161 Counter	9020161
U7	IC, MC1488 Quad Line Driver	9050188
U8	IC, MC1489 Quad Line Receiver	9050189
U9	IC, 74LS00 Quad 2-In NAND	9020000
U10	IC, PAL12L6	8040126
U11	CI, Z80A CPU	8047880
U12	IC, 74LS123 Multivibrator	9020123
U13	IC, 7404 Hex Inverter	9000004
U14	IC, MC1488 Quad Line Driver	9050188

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Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
U15	IC, MC1489 Quad Line Receiver	9050189
U16	IC, 74LS04 Hex Inverter	9020004
U17	IC, 7407 Hex Buffer	9000007
U18	IC, Z80A DMA	8047883
U19	IC, 74LS20 Dual 4-In NAND	9020020
U20	IC, 74LS08 Quad 2-In AND	9020008
U21	IC, PAL16L8	8041168
U23	IC, MC1489 Quad Line Receiver	9050189
U24	IC, 74S08 Quad 2-In AND	9010008
U25	IC, 74LS32 Quad 2-In OR	9020032
U26	IC,74ALS244 Octal Buffer	9025244
U27	IC,74ALS240 Octal Buffer, Inv.	9025240
U28	IC,74ALS240 Octal Buffer, Inv.	9025240
U29	IC,74ALS244 Octal Buffer	9025244
U30	IC, AMD8307 Transceiver	8060307
U31	IC,74ALS244 Octal Buffer	9025244
U32	IC,74ALS240 Octal Buffer, Inv.	9025240
U33	IC, Z80A CTC	8047882
U34	IC, 74LS04 Hex Inverter	9020004
U35	IC,74ALS244 Octal Buffer	9025244
U36	IC, Z80A PIO	8047881
U37	IC,74ALS244 Octal Buffer	9025244
U38	IC, 74LS74 Dual Flip-Flop	9020074
U39	IC, 74S64 ADN-OR	9010064
U40	IC,74ALS240 Octal Buffer, Inv.	9025240
U41	IC, 7407 Hex Buffer	9000007
U42	IC,74ALS240 Octal Buffer, Inv.	9025240
U43	IC,74ALS240 Octal Buffer, Inv.	9025240
U44	IC, AMD8307 Transceiver	8060307
U45	IC, AMD8307 Transceiver	8060307
U46	IC, WD2793 FDC Control	8040793
U47	IC, PAL16R6	8040166
U48	IC, 74LS123 Multivibrator	9020123
U49	IC, 74LS00 Quad 2-In NAND	9020000
U50	IC, 82S153	8040153
U51	IC, 74LS273 Octal Flip-Flop	9020173
U52	IC, 74LS157 Multiplexer	9020157
U53	IC, 74LS157 Multiplexer	9020157
U55	IC, 74LS32 Quad 2-In OR	9020032
U56	IC, 7407 Hex Buffer	9000007
U57	IC, 74LS125 Quad Buffer	9020125
U58	IC, 74LS04 Hex Inverter	9020004
U59	IC, 7407 Hex Buffer	9000007
U60	IC, 74LS30 8-In NAND	9020030
U61	IC, 74LS138 Decoder	9020138

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

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=============================================================
Ref.No.      Description                          Part No.
=============================================================
U62          IC,  74S112 Flip-Flop                9010112
U63          IC, 16K DRAM                         8040016
U64          IC, 16K DRAM                         8040016
U65          IC, 16K DRAM                         8040016
U66          IC, 16K DRAM                         8040016
U67          IC, 16K DRAM                         8040016
U68          IC, 16K DRAM                         8040016
U69          IC, 16K DRAM                         8040016
U70          IC, 16K DRAM                         8040016
U71          IC, 74LS158 Multiplexer              9020158
U72          IC, 74LS157 Multiplexer              9020157
U73          IC,    7416 Hex Driver               9000016
U74          IC,    7416 Hex Driver               9000016
U75          IC,    7407 Hex Buffer               9000007
U76          IC, 74LS04 Hex Inverter              9020004
U77          IC,   74S00 Quad 2-In NAND           9010000
U78          IC,   74S08 Quad 2-In AND            9010008
U79          IC, 74LS157 Multiplexer              9020157
U81          IC,  74S112 Flip-Flop                9010112
U82          IC, 64K DRAM                         8040655
U83          IC, 64K DRAM                         8040655
U84          IC, 64K DRAM                         8040655
U85          IC, 64K DRAM                         8040655
U86          IC, 64K DRAM                         8040655
U87          IC, 64K DRAM                         8040655
U88          IC, 64K DRAM                         8040655
U89          IC, 64K DRAM                         8040655
```

Resistors

```
R1           Resistor,  10k ohms, 1/4W,  5%       8207310
R2           Resistor,  15k ohms, 1/4W,  5%       8207315
R3           Resistor, 4.7k ohms, 1/4W,  5%       8207247
R4           Resistor,  56k ohms, 1/4W,  5%       8207356
R5           Resistor,  22k ohms, 1/4W,  5%       8207322
R6           Resistor,  51k ohms, 1/4W,  5%       8207351
R7           Resistor, 4.7k ohms, 1/4W,  5%       8207247
R8           Resistor,  150 ohms, 1/4W,  5%       8207115
R9           Resistor,  10k ohms, 1/4W,  5%       8207310
R10          Resistor,   2k ohms, 1/4W,  5%       8207220
R11          Resistor,  10k ohms, 1/4W,  5%       8207310
R12          Resistor,  15k ohms, 1/4W,  5%       8207315
R13          Resistor,  56k ohms, 1/4W,  5%       8207356
R14          Resistor, 4.7k ohms, 1/4W,  5%       8207247
R15          Resistor,  22k ohms, 1/4W,  5%       8207322
R16          Resistor,   1k ohms, 1/4W,  5%       8207210
```

Radio Shack ®

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
R17	Resistor, 1k ohms, 1/4W, 5%	8207210
R18	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R19	Resistor, 1.2k ohms, 1/4W, 5%	8207212
R20	Resistor, 220 ohms, 1/4W, 5%	8207122
R21	Resistor, 10k ohms, 1/4W, 5%	8207310
R22	Resistor, 560 ohms, 1/4W, 5%	8207156
R23	Resistor, 10k ohms, 1/4W, 5%	8207310
R24	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R25	Resistor, 10k ohms, 1/4W, 5%	8207310
R26	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R27	Resistor, 7.5k ohms, 1/4W, 5%	8207275
R28	Resistor, 160k ohms, 1/4W, 5%	8207416
R29	Resistor, 680 ohms, 1/4W, 5%	8207168
R30	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R31	Resistor, 560 ohms, 1/4W, 5%	8207156
R32	Resistor, 10k ohms, 1/4W, 5%	8207310
R33	Resistor, 10k ohms, 1/4W, 5%	8207310
R34	Resistor, 22 ohms, 1/4W, 5%	8207022
R35	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R36	Resistor, 10k ohms, 1/4W, 5%	8207310
R37	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R38	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R39	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R40	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R41	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R42	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R43	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R44	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R46	Resistor, 390k ohms, 1/4W, 5%	8207349
R48	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R49	Resistor, 20k ohms, 1/4W, 5%	8207320
R50	Trim Pot, 50k ohms, 3-Pin	8289351
R51	Trim Pot, 50k ohms, 3-Pin	8289351
R52	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R53	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R54	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R55	Resistor, 51 ohms, 1/4W, 5%	8207051
R56	Resistor, 51 ohms, 1/4W, 5%	8207051
R57	Resistor, 51 ohms, 1/4W, 5%	8207051
R58	Resistor, 51 ohms, 1/4W, 5%	8207051
R59	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R60	Resistor, 51 ohms, 1/4W, 5%	8207051
R61	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R62	Resistor, 4.7k ohms, 1/4W, 5%	8207247

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

```
===============================================================
Ref.No.    Description                              Part No.
===============================================================
```

Resistor Paks

Ref.No.	Description	Part No.
Z1	Resistor Pak, 2.2k ohms, SIP 10-Pin	8290031
Z2	Resistor Pak, 10k ohms, SIP 6-Pin	8290032
Z3	Resistor Pak, 56k ohms, DIP	8290034
Z4	Resistor Pak, 150 ohms, SIP 8-Pin	8293316
Z5	Resistor Pak, 150 ohms, SIP 8-Pin	8293316
Z6	Resistor Pak, 150 ohms, SIP 8-Pin	8293316
Z7	Resistor Pak,220/330 ohms, SIP 10-Pin	8290020

Staking Pins

Ref.No.	Description	Part No.
TP6	Staking Pin	8529014
TP8	Staking Pin	8529014
TP8	Staking Pin	8529014
TP9	Staking Pin	8529014
TP10	Staking Pin	8529014
TP21	Staking Pin	8529014
TP22	Staking Pin	8529014
TP23	Staking Pin	8529014
E1	Staking Pin	8529014
E2	Staking Pin	8529014
E4	Staking Pin	8529014
E5	Staking Pin	8529014
E6	Staking Pin	8529014
E7	Staking Pin	8529014
E8	Staking Pin	8529014
E9	Staking Pin	8529014
E10	Staking Pin	8529014
E11	Staking Pin	8529014
E12	Staking Pin	8529014
E15	Staking Pin	8529014
E16	Staking Pin	8529014
E17	Staking Pin	8529014
E18	Staking Pin	8529014
E19	Staking Pin	8529014
E24	Staking Pin	8529014
E25	Staking Pin	8529014
E27	Staking Pin	8529014
E28	Staking Pin	8529014
E30	Staking Pin	8529014
E31	Staking Pin	8529014
E32	Staking Pin	8529014
E38	Staking Pin	8529014
E39	Staking Pin	8529014
E40	Staking Pin	8529014

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
Staking Pins		
E41	Staking Pin	8529014
E42	Staking Pin	8529014
E43	Staking Pin	8529014
E44	Staking Pin	8529014
E45	Staking Pin	8529014
E46	Staking Pin	8529014
E47	Staking Pin	8529014
E48	Staking Pin	8529014
E49	Staking Pin	8529014
E50	Staking Pin	8529014
E51	Staking Pin	8529014
E52	Staking Pin	8529014
E53	Staking Pin	8529014
E54	Staking Pin	8529014
E55	Staking Pin	8529014
Transistors		
Q1	Transistor, 2N3906	8100906
Miscellaneous		
Y1	Crystal, 8.0000MHz	8409006
VR1	Voltage Regulator, 79L05	8051905
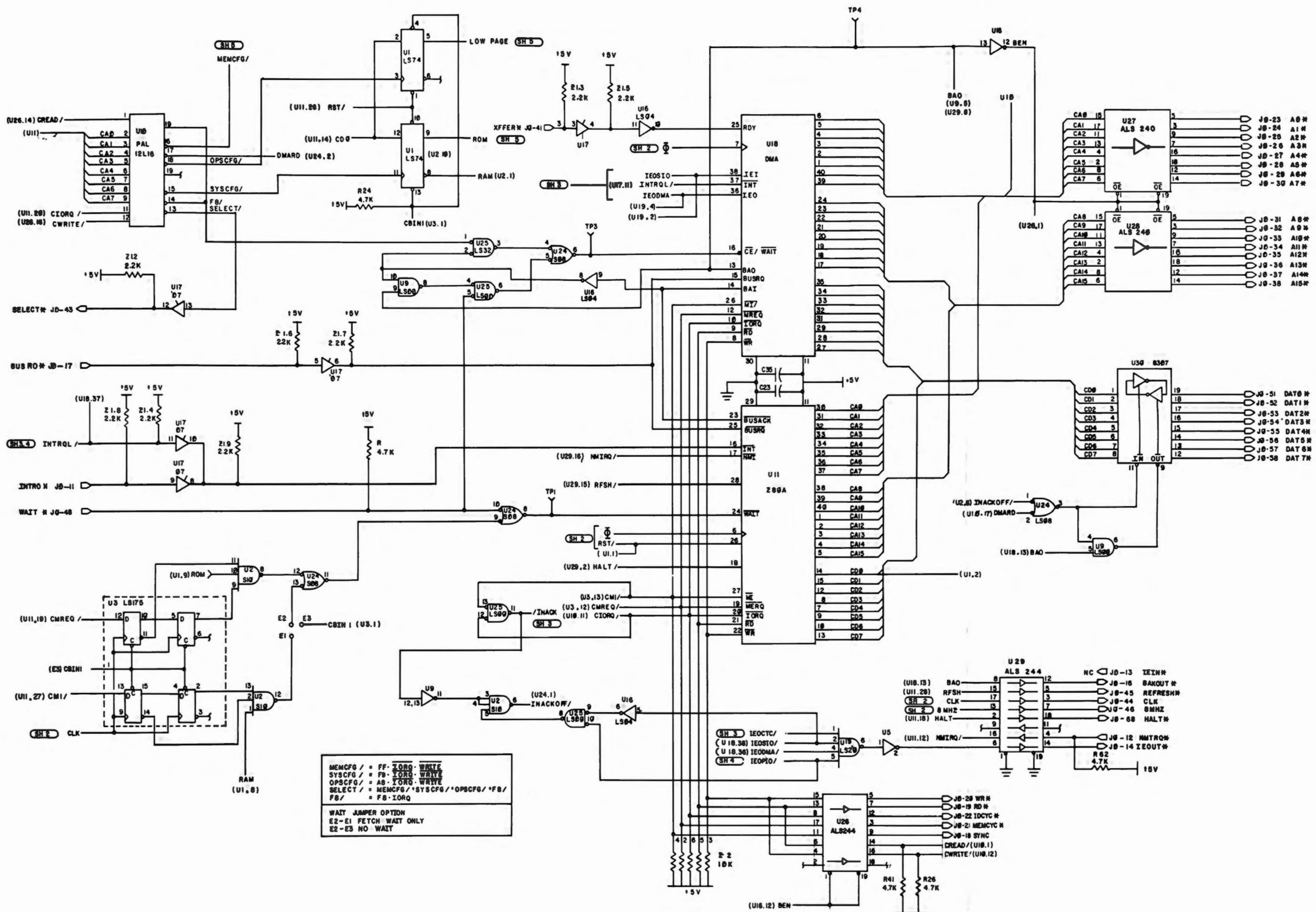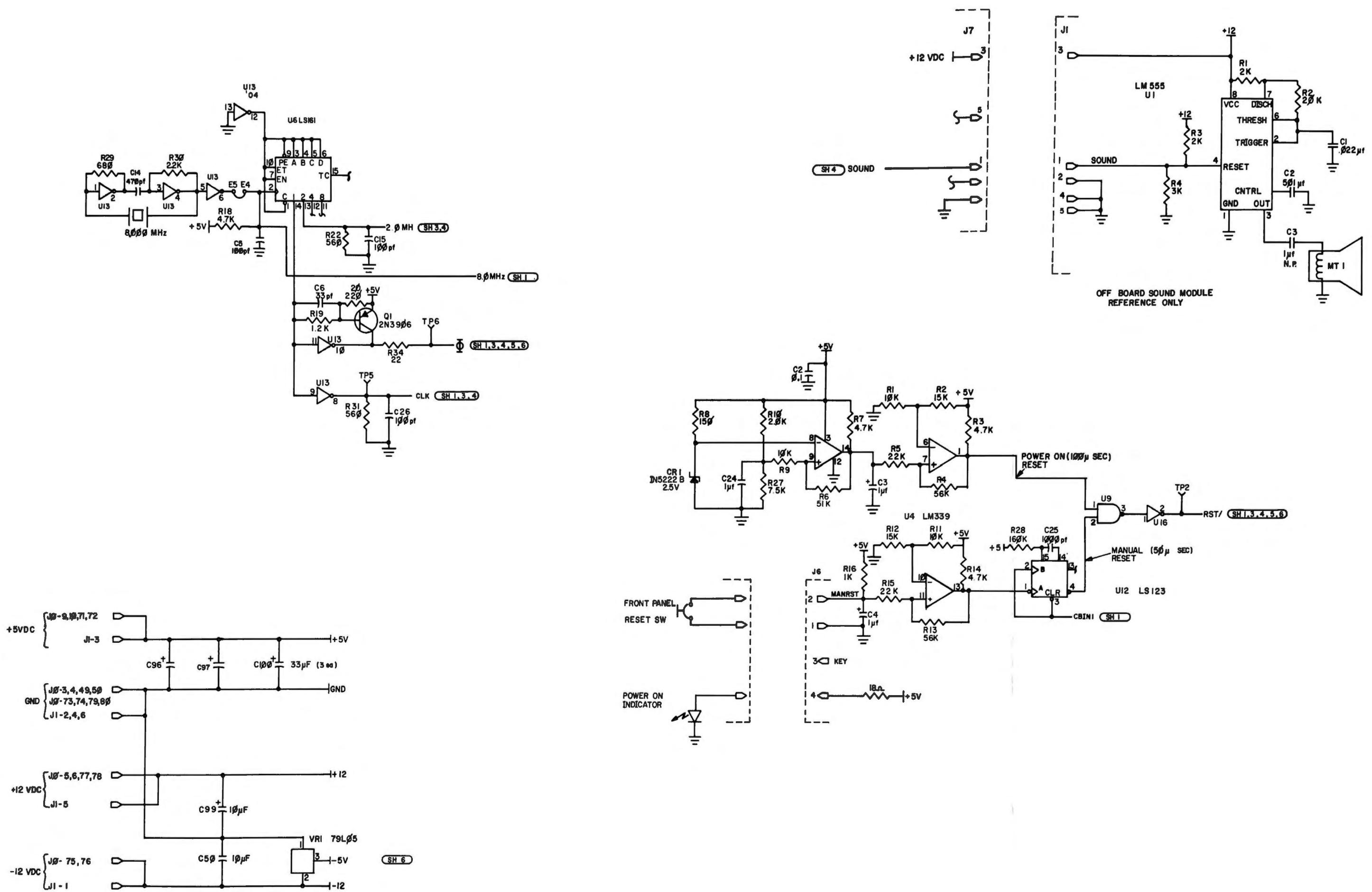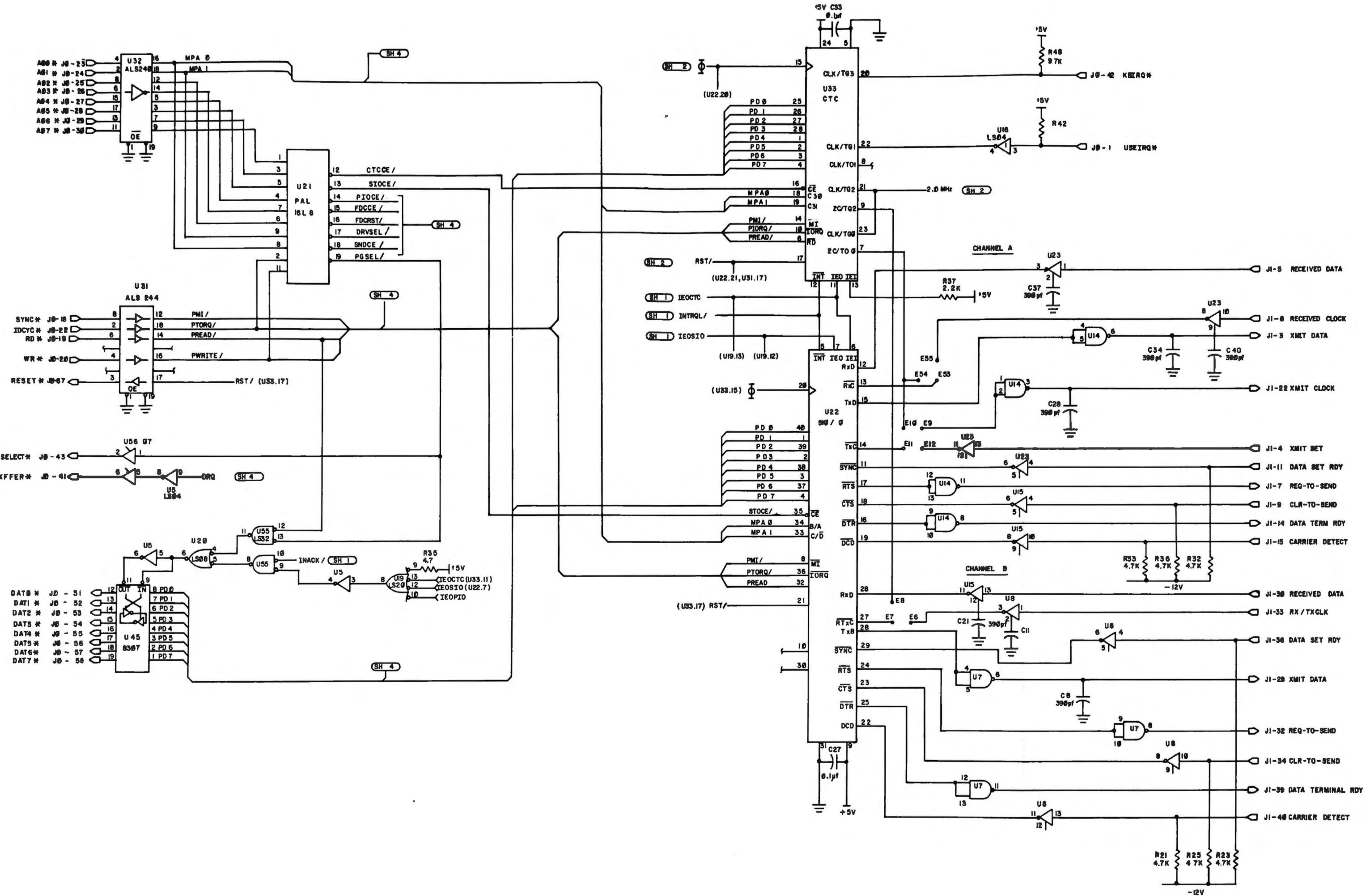
Quanity	Description	Part No.
1	Bus Bar, 8.5"	8439008
1	Printed Circuit Board	8709317
16	Socket, 16-Pin	8509003
18	Socket, 20-Pin	8509009
1	Socket, 24-Pin	8509001
1	Socket, 28-Pin	8509007
5	Socket, 40-Pin	8509002
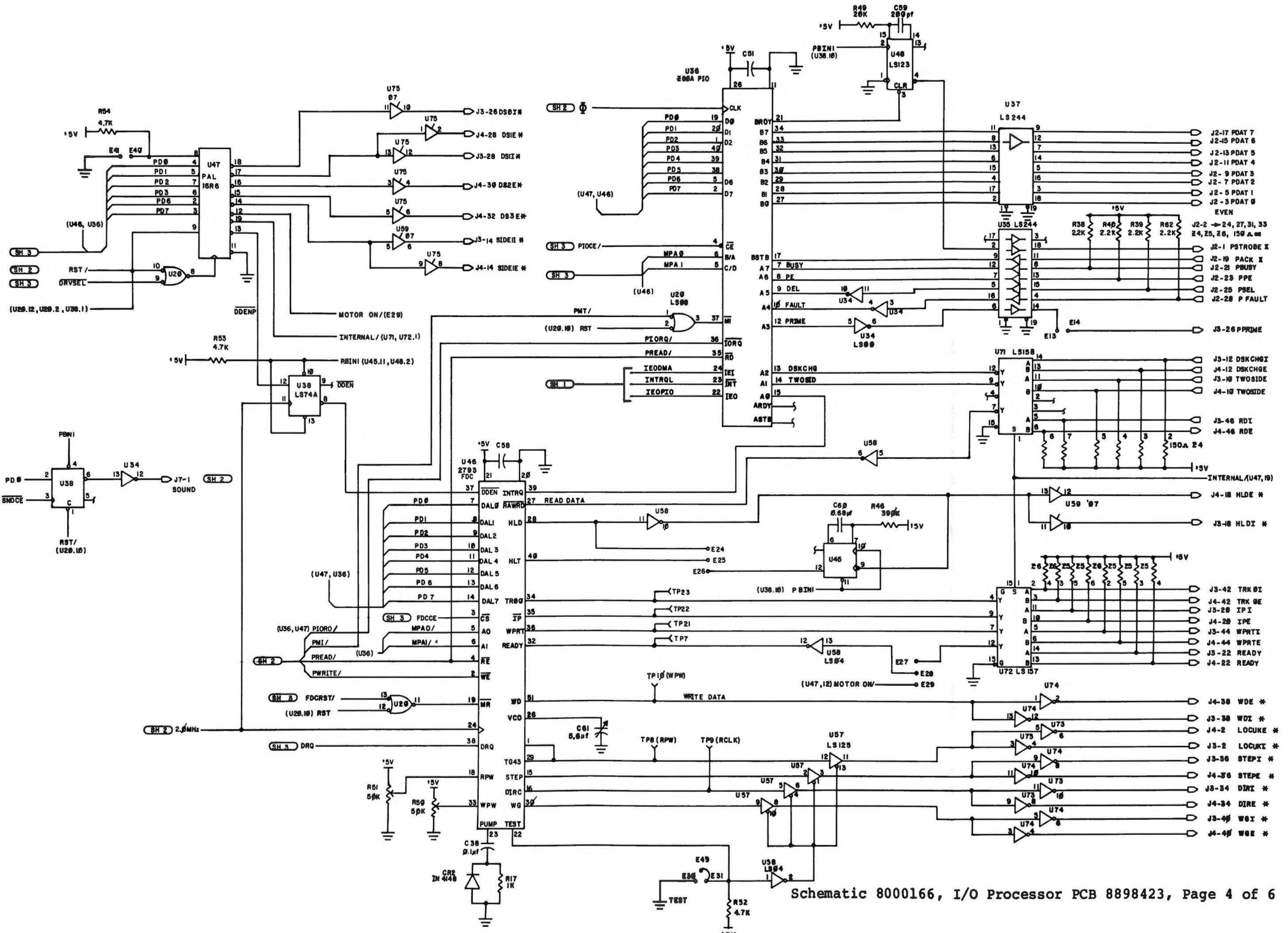
Schematic 8000166, I/O Processor PCB 8898423, Page 1 of 6
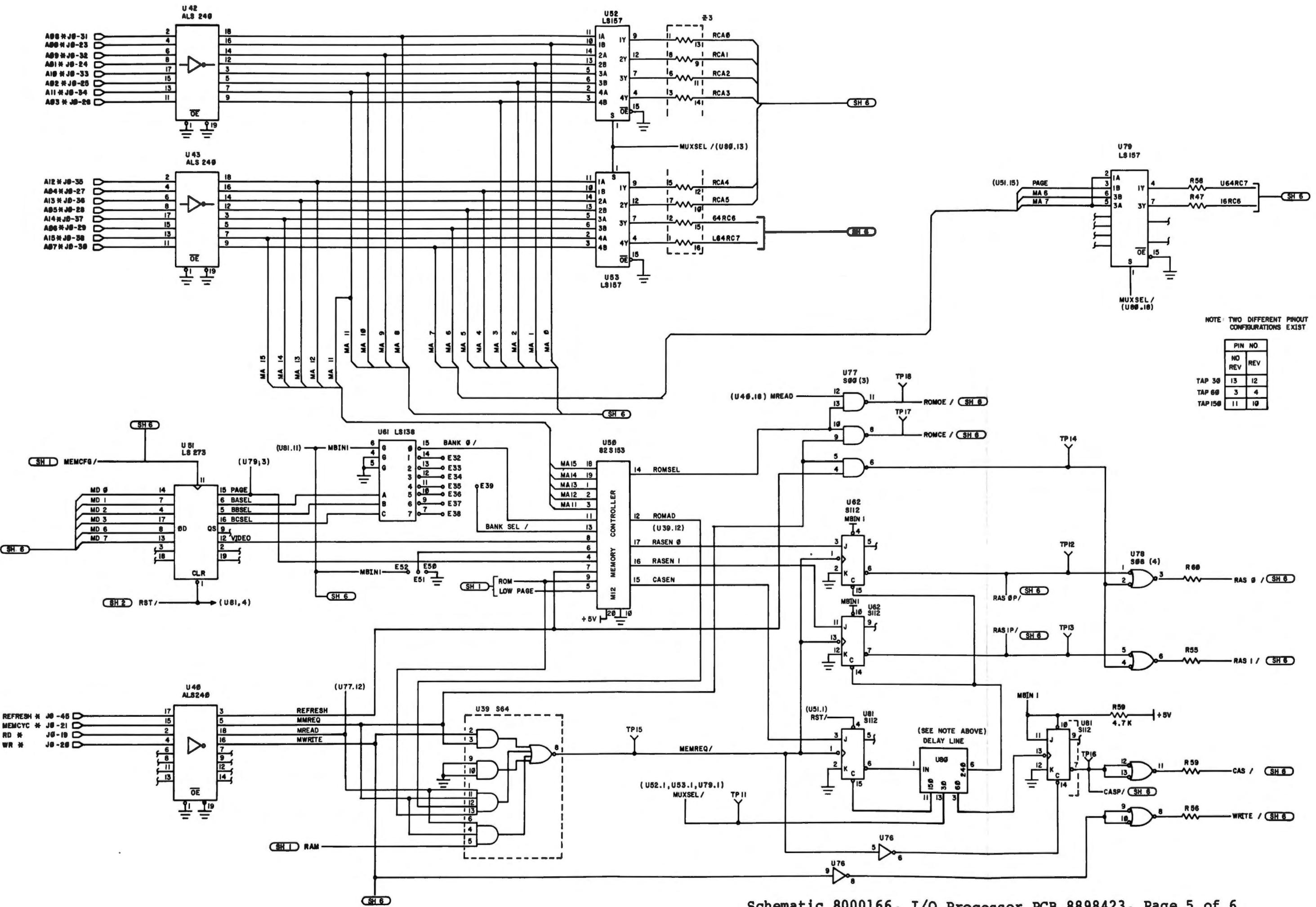
OFF BOARD SOUND MODULE
REFERENCE ONLY
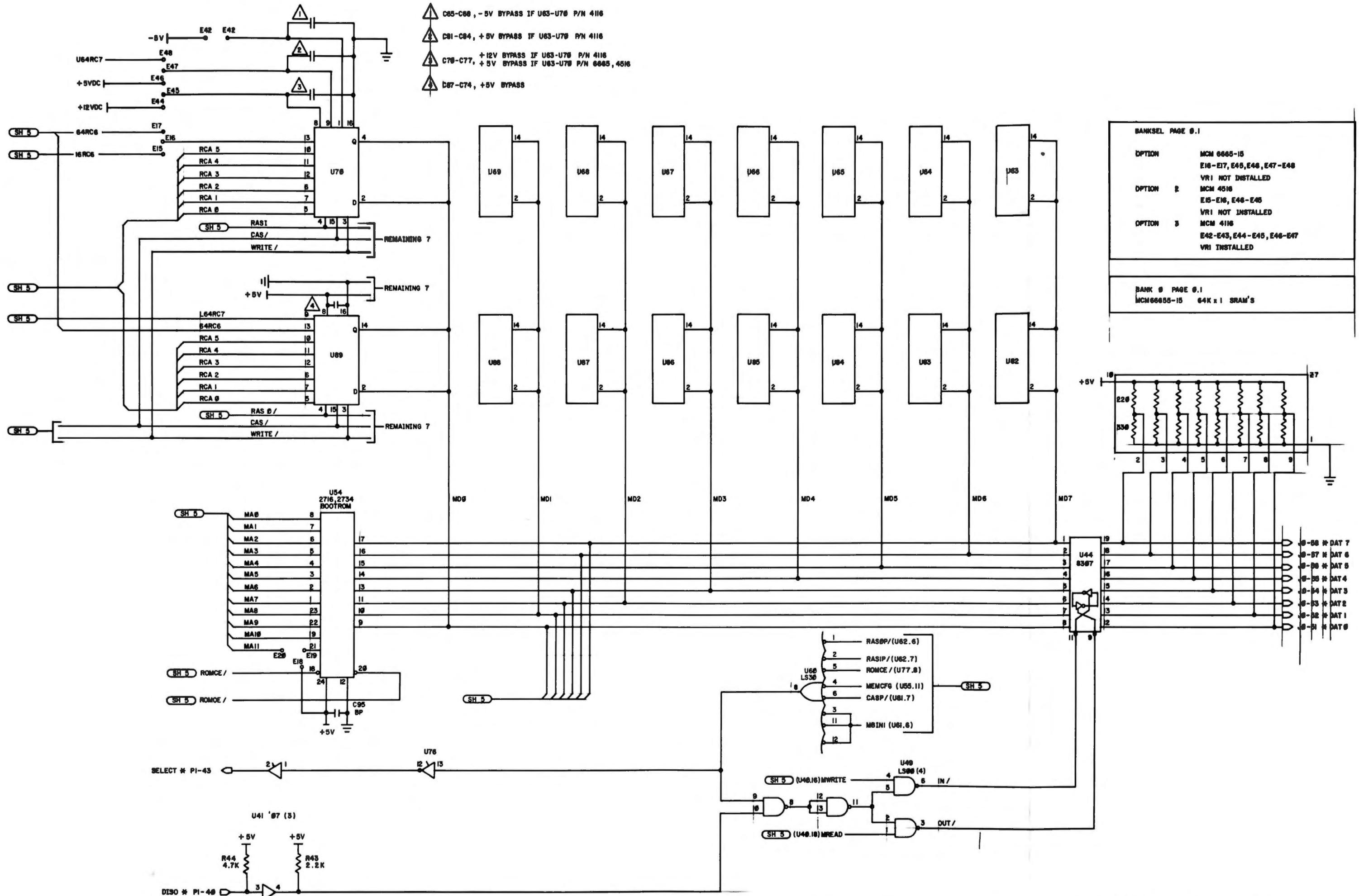
Schematic 8000166, I/O Processor PCB 8898423, Page 3 of 6

Schematic 8000166, I/O Processor PCB 8898423, Page 5 of 6

Schematic 8000166, I/O Processor PCB 8898423, Page 6 of 6

7.5   Video/Keyboard Interface Board

The Video/Keyboard Interface board has two major functions.
One is to control a built-in, high-resolution video monitor
capable of displaying 24 lines of either 80 normal
characters or 40 expanded characters in both upper and lower
cases. The other is to control a keyboard that includes the
normal set of key functions plus eight software-programmable
function keys.

Figure 7-6 shows a block diagram of this PCB assembly. It
includes a high speed oscillator (U1) whose frequency
(12.48Hz) is the rate at which information is shifted to the
CRT and video dots are written, and a CRT controller
providing diversified functions such as video timing and
display refresh memory addressing. A multiplexer switches
the control of the Display RAM address source to either the
CRTC or the CPU, depending on the RAM/Video RAM Logic
Selection. The block diagram also shows a video-board
select logic which controls a 3-state buffer, the keyboard
control, and enables the video and Real Time Clock. Data is
latched from the Display RAM into a ROM character generator,
then shifted to the video output to finally appear on the
display monitor.

Figure 7-6 includes as many blocks as possible for clarity.
For example, the pulse-width adjuster block in the block
diagram is simply an MSI monostable multivibrator with
Schmitt-trigger inputs. Its main function is to provide
noise immunity and pulse width stability to the horizontal
sync signal, which is one of the CRTC ouputs. Also, the
vertical sync goes through the RTC & NMIRQ* Logic to
generate a Real Time Clock signal (30 or 60 Hz) and a
non-maskable interrupt request signal.

All the different blocks describing the control system
(Video/Keyboard) are described in the following sections.

7.5.1.   Theory of Operation

1.   High Speed Timing (refer to Video/Keyboard schematic)

The timing for the system is derived from a crystal
oscillator. This oscillator is shown in the upper LH corner
of the schematic. It consists of a 12.48 MHz
fundamental-cut crystal in a parallel resonant circuit that
is composed of two inverters (part of U1) that are biased
into their linear region by resistors R2 and R3 (470 ohms
each).
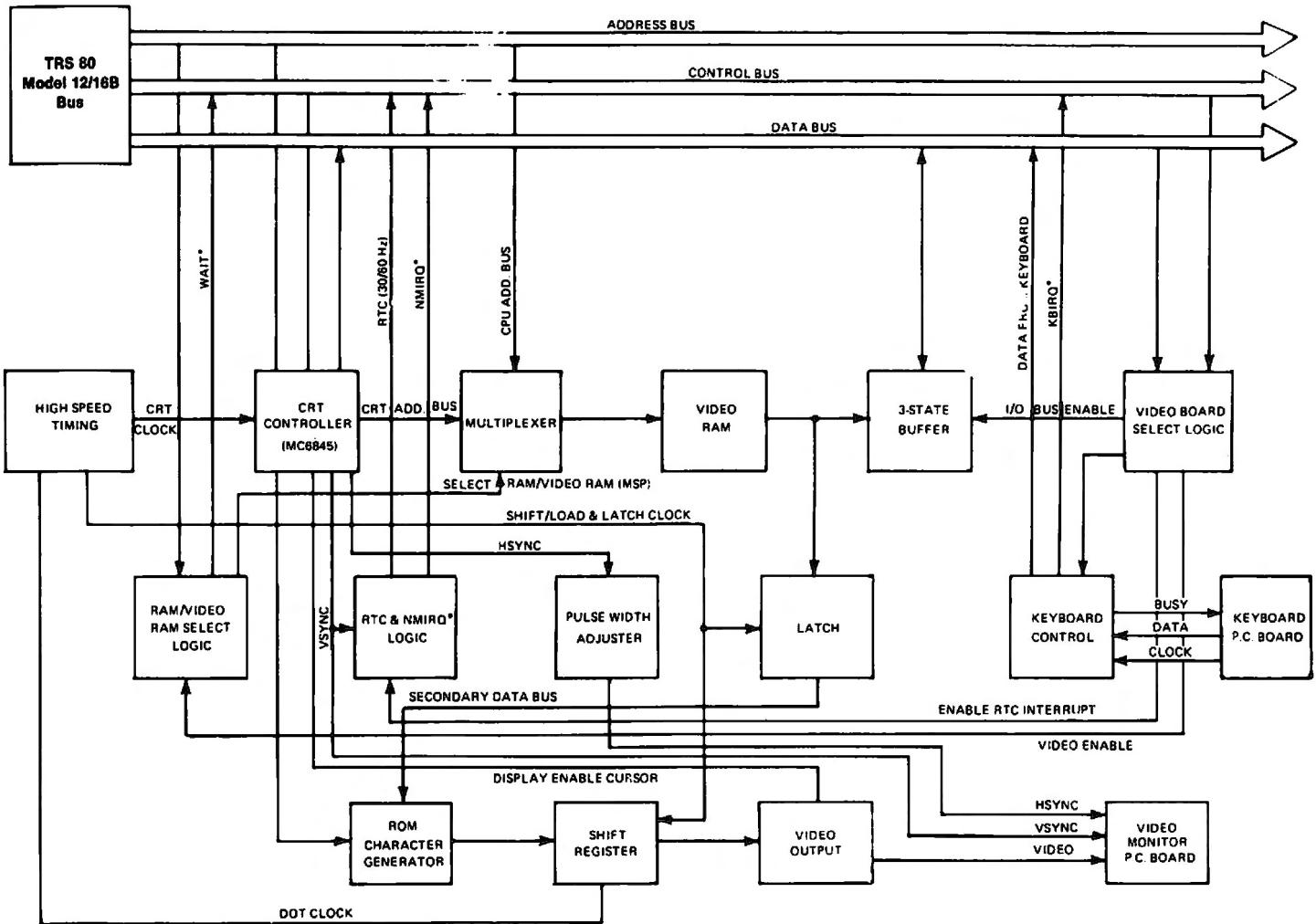
Figure 7-6.   Video/Keyboard Interface PCB Block Diagram

The waveform at pin 8 of Ul resembles a "raw" square wave
with a frequency of approximately 12.48 MHz.

At pin 2 of the same chip, the signal appears more like a
"clean" square wave. It is labeled RCLOCK and is fed
through inverter Ul pin 13 and exits pin 12 as RCLOCK*. The
asterisk indicates that the signal is an active low, i.e. if
RCLOCK is normally an active high, RCLOCK* will be an
active low.

At pin 3 of Ul, RCLOCK* goes through an inverter to give
RCLOCKP (RCLOCK prime) and through a second inverter to
yield RCLOCKP*. Up to this point, all clock pulses have the
same frequency (12.48 MHz) but different phases.

All these different clock pulses are generated to provide
the timing to synchronize the various activities of the
video system. Some activities should take place before
others while some should occur three or four times as often
as others. RCLOCK is divided by 2 by a D Flip-Flop, pins 3
and 5 of Ul7. This provides a frequency of 6.24 MHz, which
is then NANDed with the 80*/40 character Enable. When this
signal is low (active), 80 characters per line will be
displayed on the screen. When the signal is high, only 40
characters will appear on the screen.

CLOCK (at pin 6 of U28, test point TP26) is either 12.48 MHz
(for 80 characters) or 6.24 MHz (for 40 characters). Note
that the NAND gate (U28 pins 1, 2, and 3) is used here as an
inverter. CLOCK goes through inverter U33 (pins 1 and 2) to
become DCLK, which is the DOT CLOCK. Its frequency (either
6.24 or 12.48 MHz) is the rate at which video information is
shifted to the CRT.

CLOCK, which is a phase-shifted DOT CLOCK, is divided by the
4-bit counter (U26) to produce the character-rate clock
labeled as CCLK with a frequency of 1.56 MHz (for 80
characters) or 0.78 MHz (for 40 characters). This 4-bit
counter (LS163) is synchronous (all its flip-flops are
clocked simultaneously) so that the outputs change
coincident with each other when instructed by the
count-enable inputs and internal gating. The DOT CLOCK
triggers the four flip-flops on the rising edge of its wave
form. The count is accomplished as follows (in HEX): 0, 9,
A, B, C, D, E, F, 0, 9, A, B, C,...etc. This is best
described by the timing diagram in Figure 7-7. Notice that
both 40 and 80 character modes are represented here and that
the signals TCLK* and PLCLK* are also shown on this diagram.
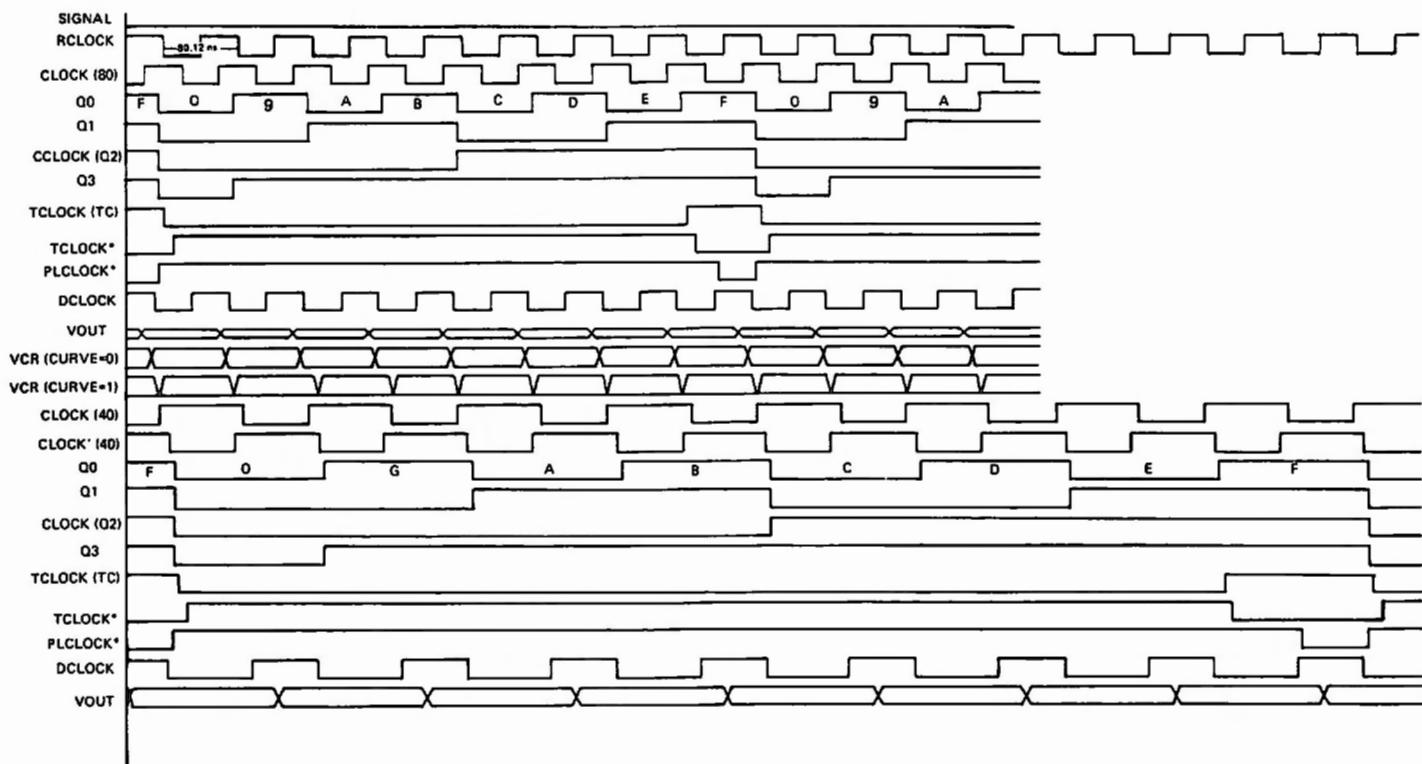
Figure 7-7. Timing Diagram

All these different signals are needed to allow the proper
synchronization of the functions. The diagram represents
accurately the propagation delay times provided by the
different gates.

An example of this follows: the CCLK triggers the MC6845
CRT controller that, if enabled, sends an address to the
video RAM requesting data to be sent to the Latch (U8)
inputs. TCLK* then latches it into the character ROM that,
at its turn, would send the appropriate dots to the shift
register U10. PLCLK* then shift loads them in parallel into
the 8-bit shift register (U10) and DCLK shifts them out
serially toward the Video.

2. Cathode Ray Tube Controller (CRTC)

The video monitor display uses the Motorola Controller
MC6845, a reliable processor that controls the monitor with
no CPU intervention until the video memory receives new data
to be processed.

The MC6845 simplifies not only the design and the
architecture, but also the troubleshooting of the video
control board. It sharply reduces the number of IC chips
normally required. This CRTC commands the interface to
raster scan the CRT display. It also provides video timing
and refresh memory addressing. The CRTC is a collection of
registers, counters and comparators that time all logic
activities as the interfaced raster scan proceeds. Its
logic consists of programmable horizontal and vertical
timing generators, linear register, cursor logic, light-pen
capture register and control circuitry for interfacing to a
processor bus. The CRTC permits easy timing and
synchronization of signals. It also handles raster graphics
as well as alphanumeric applications. It is fully
programmable through the CPU data bus, thus generating
timing for almost any alphanumeric screen density.
Therefore, it is up to the designer to choose any screen
density desired, for instance 80 x 24, 132 x 20, etc.

In the Model 16B/16B-HD, either an 80 x 24 or a 40 x 24
character screen density is used. This can be set by
programming the registers of the CRTC. The CPU communicates
with the CRT controller through a buffered 8-bit data bus by
reading or writing into the 18 registers of the CRTC.

Other functions of the CRT controller are to generate
refresh addresses, row addresses, video monitor timing
(horizontal and vertical sync), cursor and display enable.

The best way to describe the MC6845 controller is to refer to pin descriptions as noted in Figure 7-8. The following paragraphs describe the function of each pin on the CRTC chip. The MC6845 is identified as U11 on the schematic.
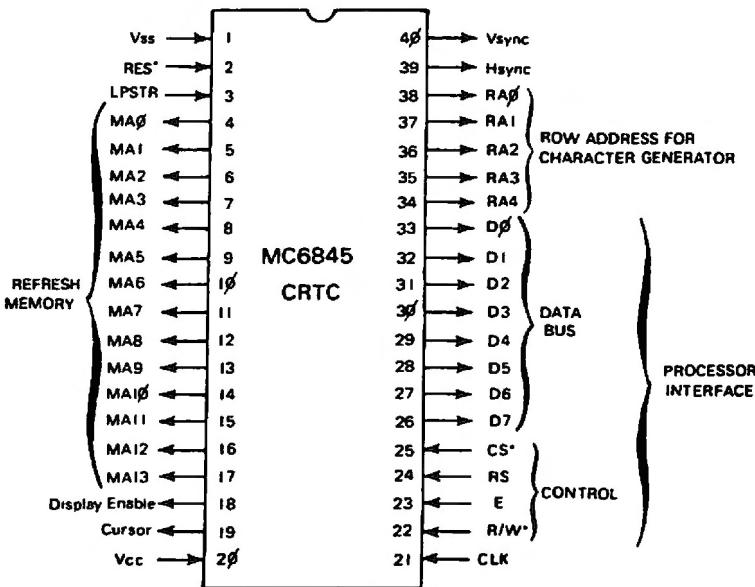
Figure 7-8. MC6845 Pin Identification

Processor Interface

The CRTC interfaces to the processor bus on the bidirectional data bus (D0-D7) using CS*, RS, E and R/W* for control signals. The data bus lines are used for data transfers between the CRTC internal register file and the processor.

The enable signal (pin 23) of U11 is a high impedance TTL/MOS compatible input that enables the data bus input/output buffers and clocks data to and from the CRTC. In the schematic, the CRTC is enabled by either the RD* or WR* (U42, pins 11, 12, and 13). The high-to-low transition is its active edge.

The chip select (CS*), when low, selects the CRTC to read or write the internal register file. It is active (low) only when there is a valid stable address being decoded from the

processor. It is active when either I/O port FC* or FD* is
active (U31, pins 6 and 7). The register select line (RS)
is an input that selects either the address register (RS=0)
or one of the data registers (RS=1) of the internal register
file. The read/write signal (R/W*) determines whether the
internal file gets written (signal low) or read (signal
high).

CRT Control

The CRTC provides horizontal sync (HS), vertical sync (VS),
and Display Enable signals. The vertical sync is an active
high signal that drives the monitor. It determines the
vertical position of the displayed data. The horizontal
sync is also an active high signal that drives the monitor
to determine the horizontal position of the displayed data.

The Display Enable is an active high signal that indicates
the CRTC is providing addressing in the display area.

Refresh Memory/Character Generator Addressing

The CRTC provides memory addresses (MA0-MA13), which scan
the refresh RAM. Only MA0 through MA10 are used, since the
video memory capacity is only 2K bytes. Also provided are
Raster addresses (RA0-RA4) for the character ROM. The
refresh memory addresses (MA0-MA10) are used to refresh the
CRT screen with pages of data located in the 2K block of
Display RAM.

The raster addresses (RA0-RA4) determine the row of a
character in the character ROM.

Other Pins

The clock input is used to synchronize all CRT control
signals. This signal is the character-rate clock CCLK
(1.56/0.78 MHz). The active transition is high to low.

The Light Pen Strobe (LPSTR) is not used in the Model
16B/16B-HD. The cursor, which is an active high signal,
indicates cursor display to external video processing logic.

The Reset (RES*) input is used to reset the CRTC. It is an active low. When this signal is active, the CRTC is forced into the following status:

    All the counters in CRTC are cleared and the device stops the display operation.

    All the outputs go to a low level.

    The control registers of the CRTC are not affected.
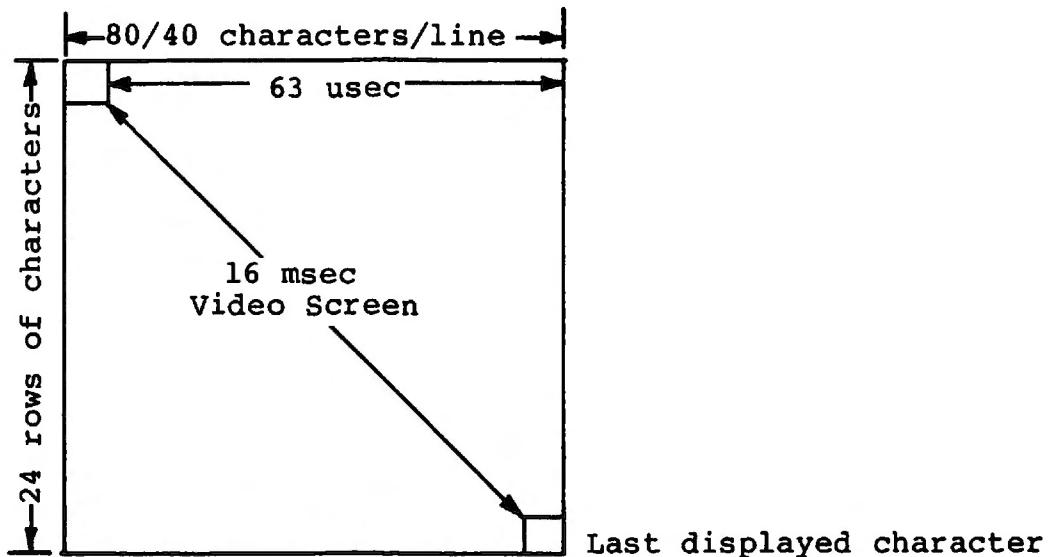
Display Refresh

The CRTC internal register file is programmed to display either a 80 x 24 or 40 x 24 alphanumeric character format. The address of each of these characters is stored in the display memory. That is why only 2K of Video RAM is required (just enough to store the entire screen density). Everything that is displayed on the screen must be refreshed continuously or it will fade and disappear. Each character is a dot matrix of 8 x 10 cells and every cell is refreshed approximately 60 times a second. The CRT beam scans the screen from top to bottom, refreshing every dot whose location is indicated by the coordinates that the display memory and the character ROM receive from the CRTC (memory refresh address and Row address).

The CRTC takes care of this particular chore while the CPU takes care of other more important tasks. However, every time the CPU addresses its upper 2K bytes of memory, it automatically takes control of the Video RAM. The reason is that these 2K bytes, locations F800H through FFFFH, overlap the video memory in its entirety. Thus the display RAM can be accessed by either the CPU or the CRTC, but not by both at the same time.

The processor (CPU) gets priority access anytime, but is synchronized by an interrupt to perform accesses only during the vertical retrace time. The vertical retrace time is defined as the time it takes the CRT beam to return from the end of the very last scan line back to the start of the very first one. The CRT beam is shut off during the retrace time.

The CRTC sends its addresses as follows: The first set of address lines, consisting of MAO through MA10, cycles binarily through the display memory and is incremented with each clock pulse (CCLK), one per character displayed. The second set (RA0-RA4) addresses the row-address select lines

First displayed character

Video Screen density: 80/40 x 24 characters.

Only $(1920)_{10}$ locations are displayed of the 2K RAM contents
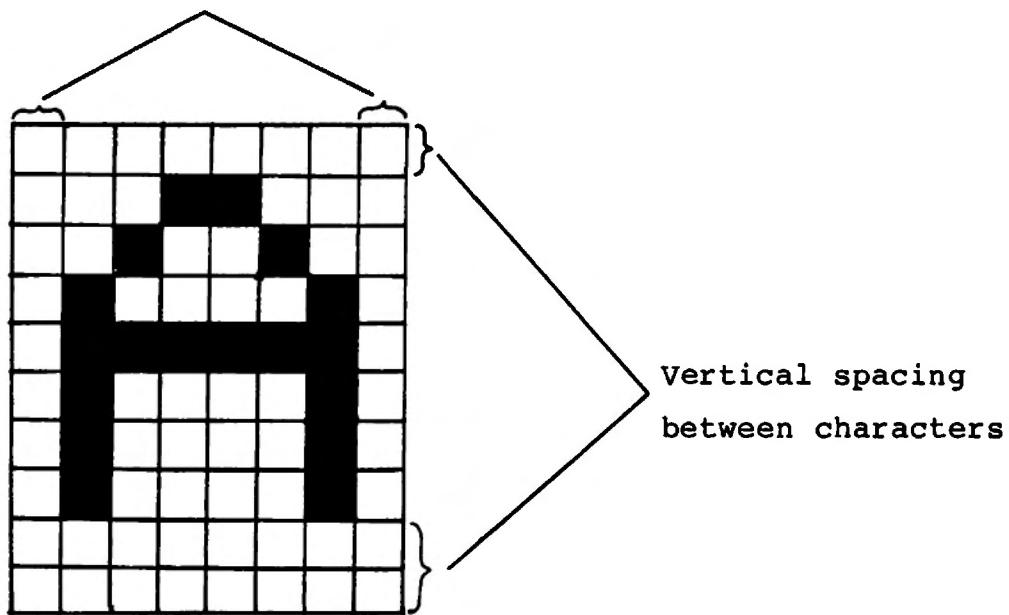
Horizontal spacing between characters

Figure 7-9. Character Dot Pattern

of the character generator. These also cycle binarily, but
are incremented with each horizontal retrace time. The
horizontal retrace time is the period in which the CRT beam
returns from the end of a scan line back to the beginning of
the next one.

The CTRC's linear address generator repeats the same
sequence of character addresses for each scan line within
the same character row.

The character block in our case is 10 rows high, so it takes
10 separate accesses of a given character to write its 10
dot-rows on the screen. Putting 80 x 24, or 1920,
characters on the screen requires 10 x 1920, or 19200,
character accesses 60 times every second.

Multiplexers

As you can see in the schematics, LS157 multiplexers (U23,
24, and 25) are used for multiplexing refresh memory
addresses between the processor and the CRTC.

The processor is in control when the select inputs (pin 1 of
each chip) are high. When these inputs are low, the control
of the display is switched to the CRTC. MSP, the signal
that controls multiplexing, is derived from the RAM/VIDEO
RAM Select Logic block.

RAM/VIDEO RAM Select Logic

The block labeled RAM/VIDEO RAM Select Logic on the diagram
in Figure 7-9 is a decoder. That is, when the CPU is
addressing its upper 2K bytes of memory located at F800H
through FFFFH, address lines AD11 through AD15 become high
(active). Also, the Memory request signal or memory cycle
(MEMCYC) is activated by the CPU. This signal is activated
every time the CPU addresses any part of its memory.
Another important signal is the input to pin 4 of NAND gate
LS30, U41. This signal is used to enable the CPU to access
the Video RAM only if the software says to. That time is
when Port FFWR* is activated and bit 7 (D2 of U18) is set to
1. If all these conditions are met, then pin 8 of U41 goes
low and MSEL (U30 pin 6) becomes high.

MSEL is ANDed with MSLP (U13 pins 1, 2, & 3) to finally give
MSP, the select input to the multiplexers. When this MSP
signal is high, the Video RAM is under the processor
control. Note that when the RESET* button is pressed (U32
pin 8), the CPU loses that control (MSP becomes low).

Since the CRTC clock CCLK and the processor (Z80) clock are
asynchronous, there must be some way to resolve conflict
between the CRTC and the CPU for Display RAM access. This
is done by MSEL* creating a WAIT* request to the CPU.

This is one of two configurations as set by jumpers E1-E2-E3
and E4-E5-E6.

E1-E2, E5-E6

This configuration allows the CPU access whenever requested
(CCLK is low). MSEL* sets WAIT*. MSEL is not created until
CCLK goes low, which holds off MSP. When MSP goes true,
false MSP ANDed with Q1 clears WAIT*. When the CPU access
is over, the control is returned to the CRTC on the next
CCLK high period.

E2-E3, E4-E5

This configuration allows the CPU access only during
vertical and horizontal retrace periods as defined by the
CRTC signal DISPEN. Thus, if the CPU makes an access
request, WAIT* is created as before by MSEL but MSELP is not
allowed to become true until DISPEN is true.

Video Board Select Logic

This part of the system is called the port addressing block.
It uses the lower eight lines of the address bus as shown
by U27 (LS30) for the dual 2 to 4 line decoder (U31 LS155).
One of the decoders is enabled only by Read NANDed with I/O
Cycle signal (IOCYC) to give 3 Read ports (FCRD*, FERD*, and
FFRD* pins 9, 11, and 12). The other is enabled only by the
IOCYC signal and its outputs could actually be used for Read
or Write ports. In our design, either one of the FC* or FD*
ports could chip select the MC6845 controller. Port FF*
NANDed with WR* gives FFWR* (U3 pins 11, 12, and 13). Also,
the Input/Output address select (U27 pin 8 and U33 pins 5
and 6) is ANDed with IOCYC to give the I/O Select (IOSEL) to
enable the 3-state buffers (U34 and U35) to either Read from
the CRTC (IOBIE:I/O Bus Input Enable) or Write into it
(IOBIE*:I/O Bus Output Enable). Note that test points TP22
(U13 pin 6) and TP21 (U2 pin 11) will show us if we are
reading from or writing into the CRTC. The following table
shows the port addressing and the function of every port.

PORT ADDR.	READ FUNCTION	WRITE FUNCTION
FC	Read Keyboard data Clear Keyboard Interrupt	Load CRTC address Register
FD	Read CRTC Data Register	Load CRTC data Register
FE	Clear Real Time clock (RTC) interrupt	
FF	Read Non-maskable Interrupt Register and Non-maskable Interrupt Mask Register.	Load Memory Bank Select Register and load Non-maskable Interrupt Mask Register and Video enable.

Table 7-8. Port Addressing

For example, Port FF is used as follows:

Non-maskable Interrupt Mask Register and Bank Select
Register: Write only.

D7   D6   D5   D4   D3   D2   D1   D0

Bit 7 (D7)

- if set (1), enables the 2K bytes RAM, disables the upper 2K bytes of the Bank's RAM (F800H to FFFFH)

- if reset (0), disables Video RAM, enables Bank RAM F800H to FFFFH.

Bit 6 (D6)

- if 0, enables Video display (on)
- if 1, Video display off

Bit 5 (D5)

- Set (1), enables the Real Time Clock (RTC) interrupt
- Reset (0), disables the RTC interrupts

Bit 4 (D4)
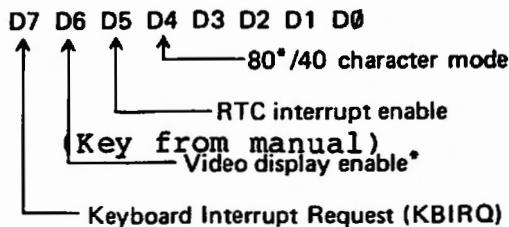
- 1, enables the 40 character mode and disables the 80 character mode
- 0, enables the 80 character mode and disables the 40 character mode.

Bit 3 through 0 (D3 - D0)

- Selects 1 of 16 memory banks. Note that if we hit the Reset, the RTC interrupt is disabled.

Non-maskable Interrupt mask Register:
    Read only

D7 D6 D5 D4 D3 D2 D1 D0

└─ 80*/40 character mode

└─ RTC interrupt enable

(Key from manual)
└─ Video display enable*

└─ Keyboard Interrupt Request (KBIRQ)

Bit 7 (D7)

- 1, Keyboard interrupting
- 0, No Keyboard interrupting

Bit 6 (D6)

- 1, Video Display disabled
- 0, Video Display enabled

Bit 5 (D5)

- RTC interrupt enable

Bit 4 (D4)

- 80*/40 character mode*

Bits 3 through 0 (D3-D0)

- They are "don't care" bits (not used)

Now that we know how these different ports will be used, we can set the control bits, say in Port FF, the way we want to. This means that we will be writing into Port FF. Therefore, the FFWR* signal is activated. If, for example, we set bit 7 to 1, bit 6 to 0, bit 5 to 1, and bit 4 to 0, FFWR* will latch this data vector into our system and the following results will be obtained:

Pin 11 of U41 will be high, thus enabling the 2K byte Video RAM. BLNKVID*, Q3 (pin 14 of U18), will go high and disable the blank Video (Video on).

The Real Time Clock (RTC), U18 pin 3, is enabled. This produces a low (0) at U18 pin 7. This generated signal is what we previously called the 80*/40 character mode. In this case, the 80* character mode is enabled (low). It is inverted at U30 pins 1, 2, and 3 and NANDed with RCLOCK* to appear at the output of the NAND gate U28, pins 8, 9, and 10 as CLOCK (TP26).

Note that the OR gate (U3 pins 4, 5, and 6) is drawn as a NAND gate.

This gate A,B ⟩C is the same as this gate A,B ⟩o-C

Figure from Model II manual

The OR gate is sometimes shown as above because we are using mostly active low signals. You can go from one gate to another by using DeMorgan's Theorem.

For the above example, the following equation applies:

$$\overline{\overline{A}\,\overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B = C$$

If we want to Read the Status of Port FF, we activate the FFRD* signal to enable the 3-state buffers LS240, U38. This will produce the status of the KBIRQ*, the BLNKVID*, the 80*/40 character mode*, and the ENABLE RTC INT* as shown at the inputs 2, 4, 6, and 8 of U38.

Other Blocks

The 3-state Buffers (U36, U37) are enabled by either the Video Read (VRD) or Write* (WR*). VRD is the result of the RD signal ANDed with MSP (U13 pins 11, 12, and 13). VWR* is the output of WR NANDed with MSP (U2 pins 11, 12, and 13).

When the CPU wants to write data into the Video RAM, WR* goes low (U36, U37 pin 1). When it does, a reading from the Video RAM, VRD (high) is active (pin 15 of U36, U37). Test points TP2 and TP24 will help detect if data is read from or written into the Display RAM by the CPU.

The keyboard control consists of an LS74 Flip-Flop (U17, pins 9, 11, and 12) showing the keyboard mode. That is, when data is being clocked in from the keyboard, a busy signal is sent to the system bus at the end of every word (8 bits of data). A busy (active low) signal goes from pin 9 of U17 back to the keyboard processor, telling it to stop sending data. Also, the same signal goes toward the CPU under the name of Keyboard Interrupt Request (KBIRQ*), telling it that a word of data is ready to be read. Data is clocked serially out of the keyboard into the shift register (U6) and then latched into the system data bus when FCRD* port is activated. Note that when FCRD* is activated (low), the Flip-Flop (U17 pins 11 and 12) becomes set and the KBIRQ* or BUSY* signal goes high (disable). Now that the keyboard logic does not receive the active busy signal, it will start sending data again.

The timing diagram of Figure 7-10 shows how data leaves the keyboard in serial fashion. Notice the narrower pulse labeled End Of Data pulse. It is generated at the end of an 8 data bit sequence. Its rising edge latches a low to the output of U17 pin 9. This low signal (KBIRQ* or BUSY*) informs the CPU that a word is ready to be read. It also prevents the keyboard from sending more data until the
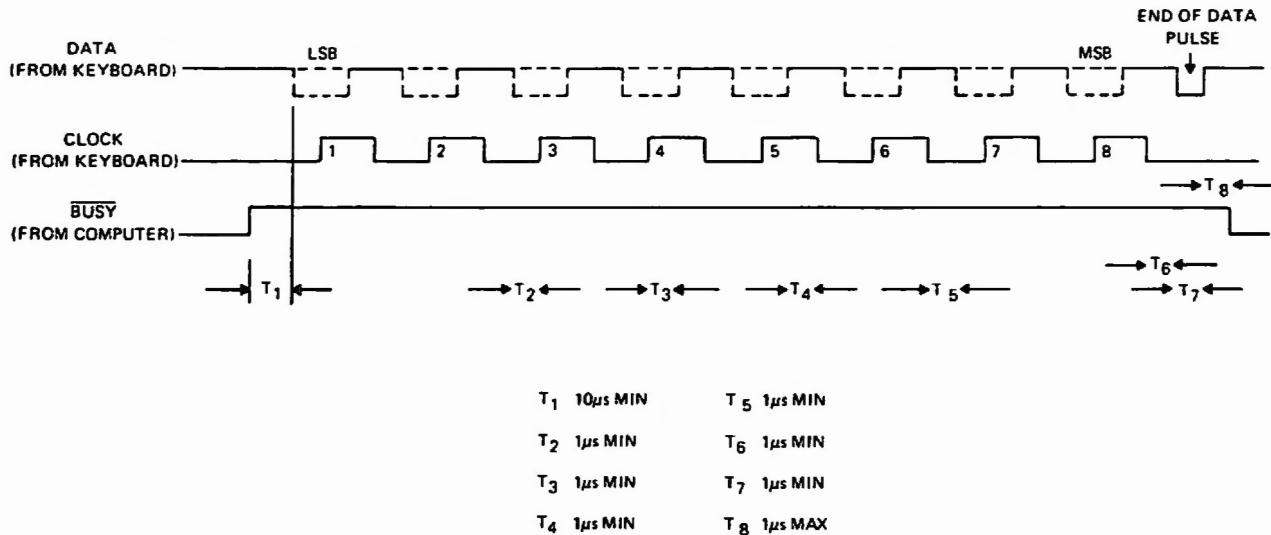
Figure 7-10. Keyboard Timing Diagram

actual 8 bit word at the output of the shift register (U6) is buffered into the data bus (in other words, read by the CPU).

The RTC and NMIRQ* logic block takes the VSYNC signal, divides it by 2 (U16 pins 8, 9, 11, and 12) to yield a 30 Hz RTC. The 60/30 Hz RTC signal clocks a high into the output of U16 pin 5 to generate an RTC interrupt (RTCINT) signal that is ANDed with ENABLE RTC INT (U29 pins 1 and 2). The output of U29 (pin 13) is then inverted and sent to the system bus as a Non-maskable Interrupt Request (NMIRQ*). Note that this signal is cleared by activating Port FERD* (Flip-Flop U16 pin 1).

The pulse-width adjuster is as defined in the earlier section of this text. It consists of a monostable multivibrator with Schmitt-trigger inputs that provide noise immunity and pulse-width stability to the horizontal sync signal (U5, 74121). The remaining parts of the system block diagram, such as the Latch, the character ROM, the Shift Register, etc., can be better defined by tracing the data path as follows:

The CPU writes a word of data into the Video RAM. The CRT
controller, which automatically displays the information
represented by Video RAM contents on the Video screen, moves
that word and stores it temporarily in the Latch. The Latch
will retain the byte for processing so that the RAM can get
ready to send the next byte. The Latch is an LS273. When
activated (by TCLK*), U8 latches the data. This data, along
with RA0-RA3 from the CRTC, constitute an address for the
ROM. The data from Memory (U8) specify a character. The
RA0-RA3 specifies the row of the character matrix to be
displayed in ASCII form. Note that the 8th bit is used as a
Reverse Video signal (REVID). U9 is the character
generator. The seven-bit ASCII word applied to its inputs
would address a certain area in it. These ASCII inputs are
considered the higher seven bits of an address. The lower
part of the address comes from the CRTC (RA0-RA4). This
lower part selects the row position of the addressed dot
pattern.

Each character consists of a dot matrix, 8 dots wide and 10
dots high. Since each character consists of a pattern of
dots, there must be some method to determine which dot
should be on and which dot should be off to form any one
character. The character generator controls the dot
patterns on the screen.
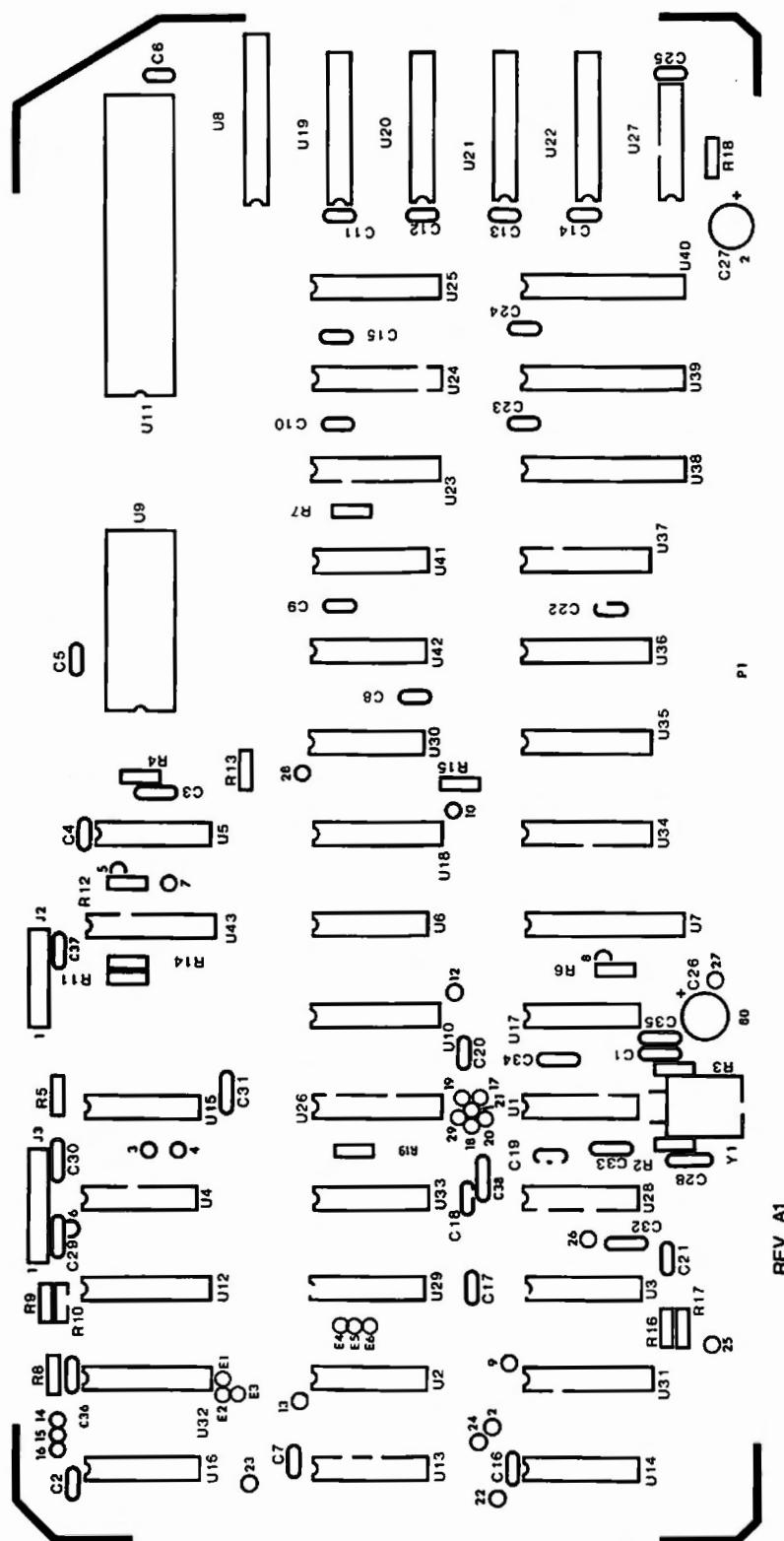
U9 outputs 8 dots (on or off) at the same time. RA0 through
RA4 selects the row of the addressed pattern. The character
generator must output 10 times to build one character.

Here is how a typical character line is written:

Assume an ASCII word is in the Latch. The electron beam is
on the first scan line of the character. Therefore, the row
address is binary "0". That is, RA0 through RA4 are low, U9
outputs the first dot pattern for that particular ASCII
character. The next ASCII character is applied to U9. At
the same time, the row address is incremented. It is now
binary "1" pointing to the second scan line. Keep in mind
that the electron beam does not stop at the last dot of the
first pattern, but continues scanning the rest of the entire
scan line. By the time the second dot pattern goes out, the
third ASCII word comes in. This process goes on until the
entire character (10 rows) is written on the screen.
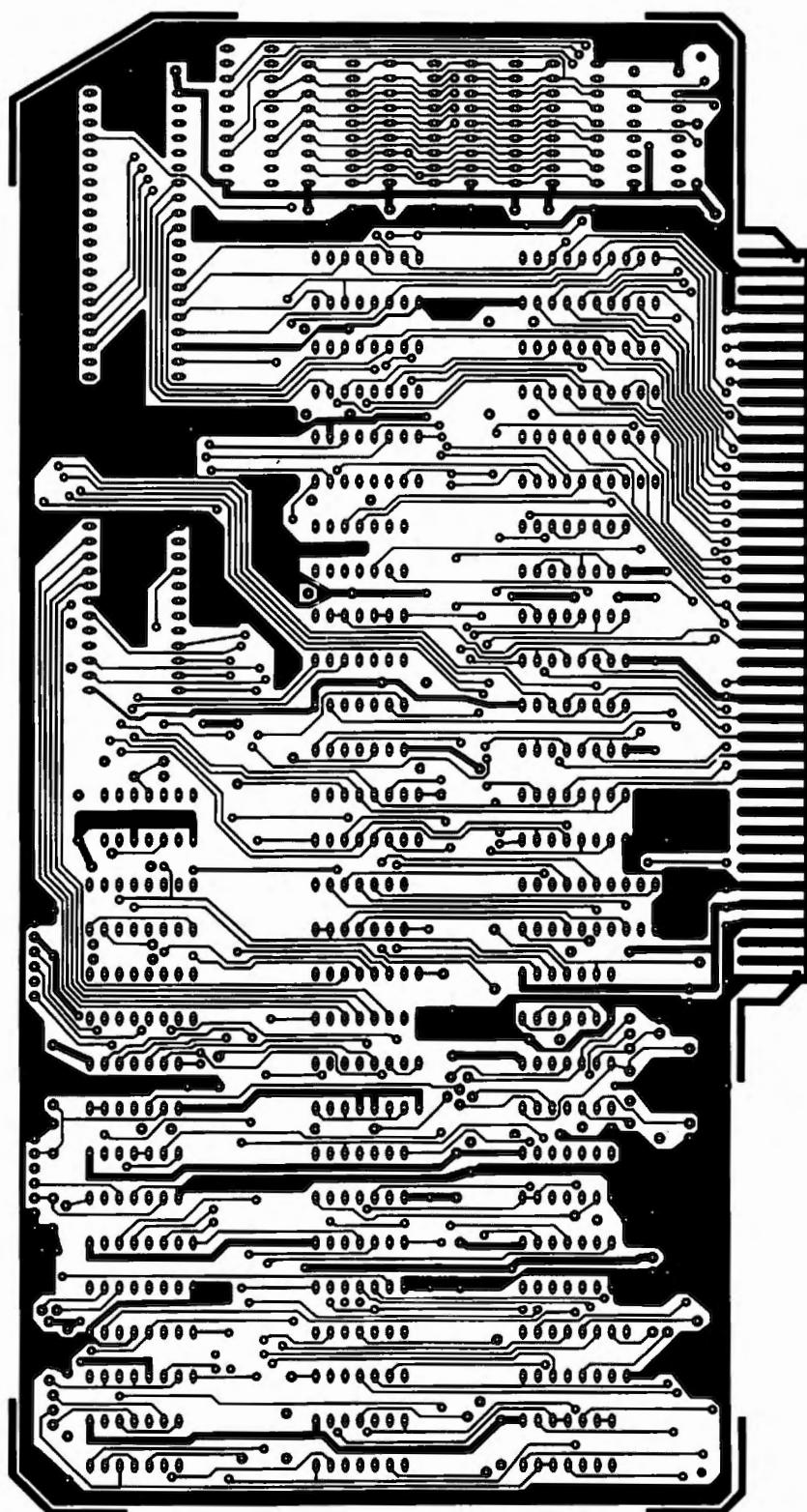
The various dot patterns are loaded into the shift register
U10 in parallel and are shifted out of it serially. All of
this is done so fast that it seems that the entire character

is displayed "not in pieces" but as a single entity. After
the eight dot scans are output, the electron beam is turned
off and two rows (the 9th and 10th) of blank dots are
output. This provides separation between character lines.
Once these two rows are output, the system is ready to
output the first row of the second character line.
Following the path the data goes through before being output
at pin 9 of U10 (Vout), the Vout signal is delayed quite a
bit with respect to the Display Enable and Cursor signals.
For this reason, the two signals are delayed by two TADCLK
cycles and Reverse Video (REVID) is delayed by one TADCLK
cycle with respect to the Vout signal. This is shown by
U12. Note how the delayed cursor and DREVID are exclusive
ORed (U4 pins 12 and 13). The resulting signal at pin 11 of
U4 is also exclusive ORed with Vout (U4 pins 9 and 10).
Either the cursor, the Reverse Video or the Video will be
displayed in a character location, but not two of them at
the same time. The signal output at pin 8 of U4 is finally
enabled by the Display enable and either one of the RCLOCK,
RCLOCK*, RCLOCKP, or RCLOCKP* signals. One of these signals
is chosen to achieve the best result. The final signal at
pin 12 of U15 is simply called VIDEO. The VIDEO, HSYNC, and
VSYNC signals are separately shielded and sent to the CRT
Logic board (ground signals are wrapped around them).

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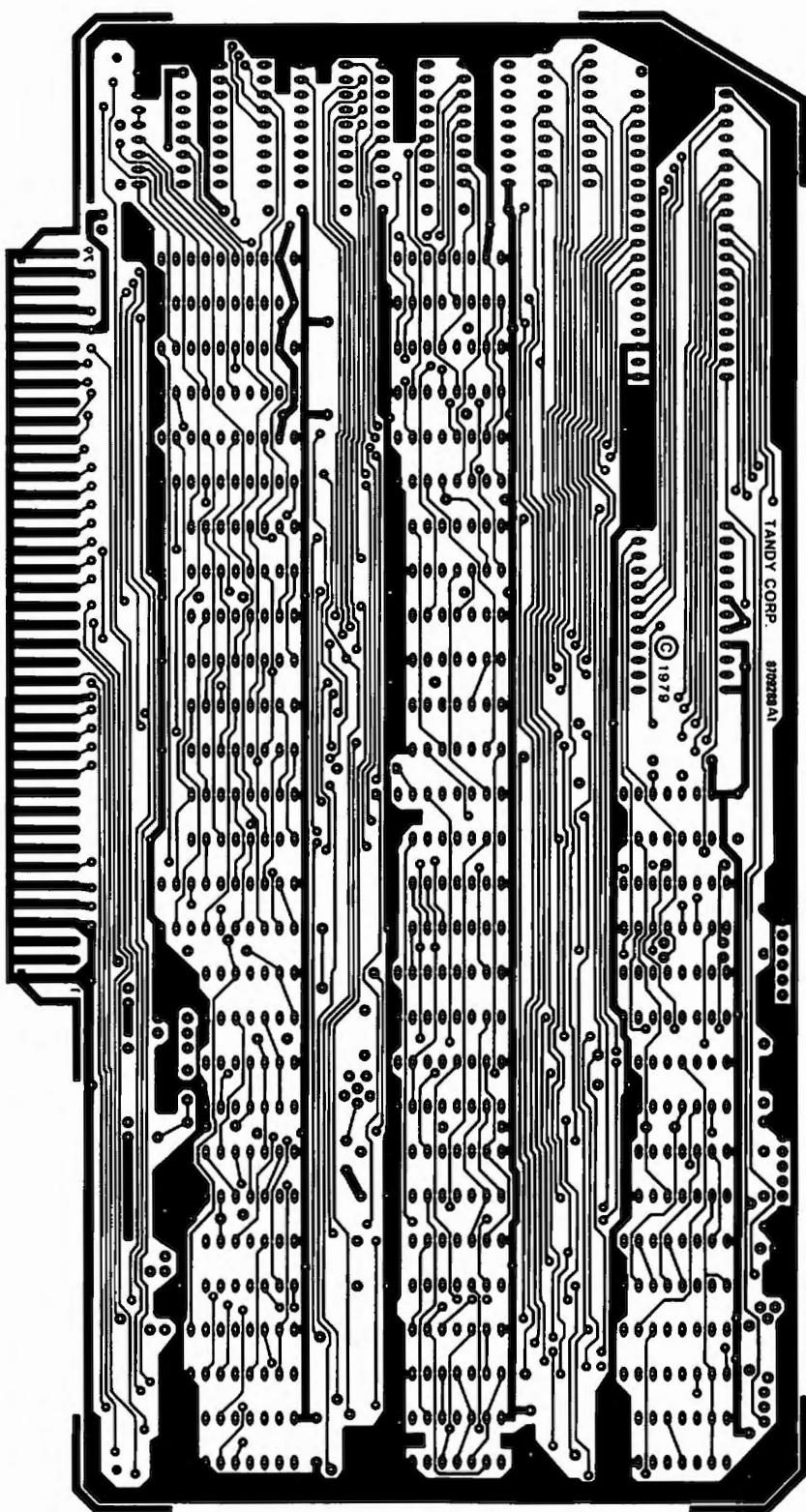
Component Layout, Video/Keyboard PCB 8898022

Circuit Trace, Video/Keyboard PCB 8898022, Component Side

Circuit Trace, Video/Keyboard PCB 8898022, Solder Side

Parts Lists, Video/Keyboard Interface, 8898022

```
=======================================================================
Ref. No.   Description                              Part No.
=======================================================================
```

Capacitors

Ref. No.	Description				Part No.
C1	Capacitor,	0.01	uF	50V	8303102
C2	Capacitor,	0.1	uF,	50V	8374104
C3	Capacitor,	1000	pF,	50V	8302104
C4	Capacitor,	0.1	uF,	50V	8374104
C5	Capacitor,	0.1	uF,	50V	8374104
C6	Capacitor,	0.1	uF,	50V	8374104
C7	Capacitor,	0.1	uF,	50V	8374104
C8	Capacitor,	0.1	uF,	50V	8374104
C9	Capacitor,	0.1	uF,	50V	8374104
C10	Capacitor,	0.1	uF,	50V	8374104
C11	Capacitor,	0.1	uF,	50V	8374104
C12	Capacitor,	0.1	uF,	50V	8374104
C13	Capacitor,	0.1	uF,	50V	8374104
C14	Capacitor,	0.1	uF,	50V	8374104
C15	Capacitor,	0.1	uF,	50V	8374104
C16	Capacitor,	0.1	uF,	50V	8374104
C17	Capacitor,	0.1	uF,	50V	8374104
C18	Capacitor,	0.1	uF,	50V	8374104
C19	Capacitor,	0.1	uF,	50V	8374104
C20	Capacitor,	0.1	uF,	50V	8374104
C21	Capacitor,	0.1	uF,	50V	8374104
C22	Capacitor,	0.1	uF,	50V	8374104
C23	Capacitor,	0.1	uF,	50V	8374104
C24	Capacitor,	0.1	uF,	50V	8374104
C25	Capacitor,	0.1	uF,	50V	8374104
C26	Capacitor,	33	uF,	16V	8326331
C27	Capacitor,	33	uF,	16V	8326331
C28	Capacitor,	15	pF,	50V	8300154
C29	Capacitor,	100	pF,	50V	8301104
C30	Capacitor,	150	pF,	50V	8301154
C31	Capacitor,	100	pF,	50V	8301104
C32	Capacitor,	100	pF,	50V	8301104
C33	Capacitor,	100	pF,	50V	8301104
C34	Capacitor,	220	pF,	50V	8301223
C35	Capacitor,	100	pF,	50V	8301104
C36	Capacitor,	0.1	uF,	50V	8374104
C37	Capacitor,	0.1	uF,	50V	8374104
C38	Capacitor,	100	pF,	50V	8301104

Connectors

Ref. No.	Description	Part No.
J2	Connector, RT Angle, 6-Pin	8519017
J3	Connector, RT Angle, 7-Pin	8519022

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Parts Lists, Video/Keyboard Interface, 8898022

```
=====================================================================
Ref No.   Description                                        Part No.
=====================================================================
```

Resistors

Ref No.	Description	Part No.
R2	Resistor, 470 ohm, 1/4W 5%	8207147
R3	Resistor, 470 ohm, 1/4W 5%	8207147
R4	Resistor, 39k ohm, 1/4W 5%	8207339
R5	Resistor, 4.7k ohm, 1/4W 5%	8207247
R6	Resistor, 4.7k ohm, 1/4W 5%	8207247
R7	Resistor, 4.7k ohm, 1/4W 5%	8207247
R8	Resistor, 4.7k ohm, 1/4W 5%	8207247
R9	Resistor, 2.2k ohm, 1/4W 5%	8207222
R10	Resistor, 2.2k ohm, 1/4W 5%	8207222
R11	Resistor, 15 ohm, 1/4W 5%	8207015
R12	Resistor, 180 ohm, 1/4W 5%	8207118
R13	Resistor, 2.2k ohm, 1/4W 5%	8207222
R14	Resistor, 180 ohm, 1/4W 5%	8207118
R15	Resistor, 2.2k ohm, 1/4W 5%	8207222
R16	Resistor, 2.2k ohm, 1/4W 5%	8207222
R17	Resistor, 2.2k ohm, 1/4W 5%	8207222
R18	Resistor, 4.7k ohm, 1/4W 5%	8207247
R19	Resistor, 8.2k ohm, 1/4W 5%	8207282

Integrated Circuits

Ref No.	Description	Part No.
U1	IC, SN74LS04NDS	9020004
U2	IC, SN74LS00NDS	9020000
U3	IC, SN74LS32NDS	9020032
U4	IC, SN74LS86NDS	9020086
U5	IC, N7412NB	9000121
U6	IC, SN74LS164NDS	9020164
U7	IC, SN74LS244NDSW	9020244
U8	IC, SN74LS273NDS	9020273
U9	IC, 2316	————
U10	IC, SN74LS165NDS	9020165
U11	IC, 6845	————
U12	IC, SN74LS174NDS	9020174
U13	IC, SN74LS08NDS	9020008
U14	IC, SN74LS33NDS	9020033
U15	IC, SN74LS11NDS	9020011
U16	IC, SNB74LS74ANDS	9020074
U17	IC, SNB74LS74ANDS	9020074
U18	IC, SN74LS175NDS	9020175
U19	IC, 21L14	————
U20	IC, 21L14	————
U21	IC, 21L14	————
U22	IC, 21L14	————
U23	IC, SN74LS157NDS	9020157
U24	IC, SN74LS157NDS	9020157

Parts Lists, Video/Keyboard Interface, 8898022

Ref No.	Description	Part No.
U25	IC, SN74LS157NDS	9020157
U26	IC, SN74LS161NDS	9020161
U27	IC, SN74LS30NDS	9020030
U28	IC, SN74LS00NDS	9020000
U29	IC, SN74LS08NDS	9020008
U30	IC, SN74LS04NDS	9020004
U31	IC, SN74LS155NDS	9020155
U32	IC, SN74LS76NDS	9020076
U33	IC, SN74LS04NDS	9020004
U34	IC, MC8T26APDS	9060026
U35	IC, MC8T26APDS	9060026
U36	IC, MC8T26APDS	9060026
U37	IC, MC8T26APDS	9060026
U38	IC, SN74LS240NDS	9020240
U39	IC, SN74LS240NDS	9020240
U40	IC, SN74LS240NDS	9020240
U41	IC, SN74LS30NDS	9020030
U42	IC, SN74LS00NDS	9020000
U43	IC, 74LS367	9020367

Miscellaneous

Item	Qty	Description	Part No.
PCB	1	Video/Keyboard Interface	8709288A
Socket	1	24-pin DIP (for U9)	8509001
Socket	1	40-pin DIP (for U11)	8509002
Socket	4	18-pin DIP (for U19-U22)	8509006
Y1	1	Crystal, 12.48 MHz	8409004

7.6 Power Supply Board

7.6.1 Functional Specifications

The Power Supply Assembly for the TRS-80 Model 16B/16B-HD is
a 140 watt switching power supply. The Printed Circuit
Board is mounted to the electronic chassis bracket. Line
input to the power supply module is made through an amp
wafer with locking 3-pin socket header.

        Pin 1   Line - Neutral
        Pin 2   Blank
        Pin 3   Line - High

Outputs are taken from an amp wafer with locking 15-pin PCB
socket header.

        Pin 1   -12 V   Pin 9 +5 V
        Pin 2   -12 V   Pin 10 Common
        Pin 3   Common   Pin 11 +5 V
        Pin 4   Common   Pin 12 +5 V
        Pin 5   Common   Pin 13 +24 V
        Pin 6   Common   Pin 14 +12 V
        Pin 7   Common   Pin 15 +12 V
        Pin 8   +5 V

In theory, the power supply rectifies the AC line to DC,
then chops it at 20 kHz. The chopped DC voltage is then
transformed to the required output voltages and rectified to
low voltage isolated DC. Feedback loops are provided for
voltage regulation and over-current protection.

The power supply may be jumper selected for either of the
following ratings:

        Vin -- 95 to 135 VAC @ 47 to 63 Hz input frequency
          or   190 to 270 VAC @ 47 to 63 Hz input frequency

The Power Supply Assembly can withstand the following
maximum ratings:

        Vin (AC continuous) -- 140 V (input select 115 V)
                    or   -- 280 V (input select 230 V)

        Short Circuit, any output -- indefinite

		Min	Typ	Max	
Output Voltages	VO1	4.95	5.00	5.25	V
	VO2	11.40	12.00	12.60	V
	VO3	See Note 1			
	VO4	21.20	24.00	26.40	V
	VO5	-11.40	-12.00	-12.60	V

VO4, no load tolerance

Note: VO1/VO2 specified for balanced loads. All voltages measured at connector.

		Min	Typ	Max	
Output Loads	IO1	3.0	4.3	13.36	A
	IO2	0.25	0.50	0.75	A
	IO3	0.10	1.0	1.5	A
	IO4	0	1.3	2.0	A
	IO5	0.05	0.1	0.2	A

		Min	Typ	Max	Units
OCP, Current Limit	ICL1	14.0	15.0	16.0	A
	ICL2	1.1	1.6	2.0	A
	ICL3	1.6	2.3	3.0	A
	ICL4	2.1	2.5	3.0	A
	ICL5	---	1.0	2.0	A

Note: VO5 is a thermally protected IC regulator.

		Min	Typ	Max	
OVP, Crowbar VCB1		5.94	6.25	7.00	V

		Min	Typ	Max	
Output Noise	VO1	---	---	50	mV p-p
	VO2	---	---	100	mV p-p
	VO3	---	---		mV p-p
	VO4	---	---	250	mV p-p
	VO5	---	---	50	mV p-p

Efficiency	70	80	---	%
Load Transient VOS	---	0.3	---	V
VO1, 25% to 75% TROS	---	1.0	---	mSec
Load Step VUS	---	0.3	---	V
TRUS	---	1.0	---	mSec

	Min	Typ	Max	
Hold Up Time:				
Full Load Lo Line	10	18	---	mSec
Full Load Nom Line	16	30	---	mSec
Insulation Resistance				
Input to Output	100	1000	---	M ohm
Input to Ground	100	1000	---	M ohm
Output to Ground	100	1000	---	M ohm
Isolation				
Input to GND and Op	4.24	---	---	KVDC
Line Conducted EMI (Reference VDE 0875)				
0.15 to 0.5 MHz	---	1.0	---	mV
0.5 to 5 MHz	---	0.5	---	mV
5 to 50 MHz	---	0.5	---	mV

7.6.2. Equipment for Test Set-Up

1. Isolation Transformer (minimum of 500 VA rating)

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. 0-140 V Variable Transformer (Variac) -- used to vary the input voltage. Recommend 10 amp, 1.4 KVA rating, minimum.

3. Voltmeter -- Need to measure DC voltages to 50 VDC and AC voltages to 200 VAC. Recommend two digital multimeters.

4. Oscilloscope -- Need X10 and X1 probes.

5. Load board with connectors -- See Table 7-5 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

    Note: Because of its design, this power supply must have a load present or damaging oscillations may result. Never test the power supply without at least the minimum load shown in Table 7-5.

6. Ohmmeter

7.6.3 Set-Up Procedure

1. Set up as shown in Figure 7-11. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 V output, with DVMs. Also monitor the +5 V output with the oscilloscope using 50 mV/div sensitivity. The DVM monitoring the +5 V output can also be used to check the other outputs. See Paragraph 7.3.4 for test points within the power supply.

Output	Min Load Amps	R for Min Load	Max Load Amps	R for Max Load	J2 Pins
+5V V01	3.0	1.66 ohm 30 W	13.36	.34 ohm 130 W	8,9, 11,12
+12 V02	.25	48 ohm 6 W	.75	16 ohm 20 W	15
+12 V03	.10	120 ohm 4 W	1.5	8 ohm 40 W	14
+24 V04	0	Infinity	2.0	12 ohm 100 W	13
-12 V05	.05	2.4 ohm 1 W	.2	60 ohm 5 W	1,2

Table 7-9.   Power Supply Voltage Chart
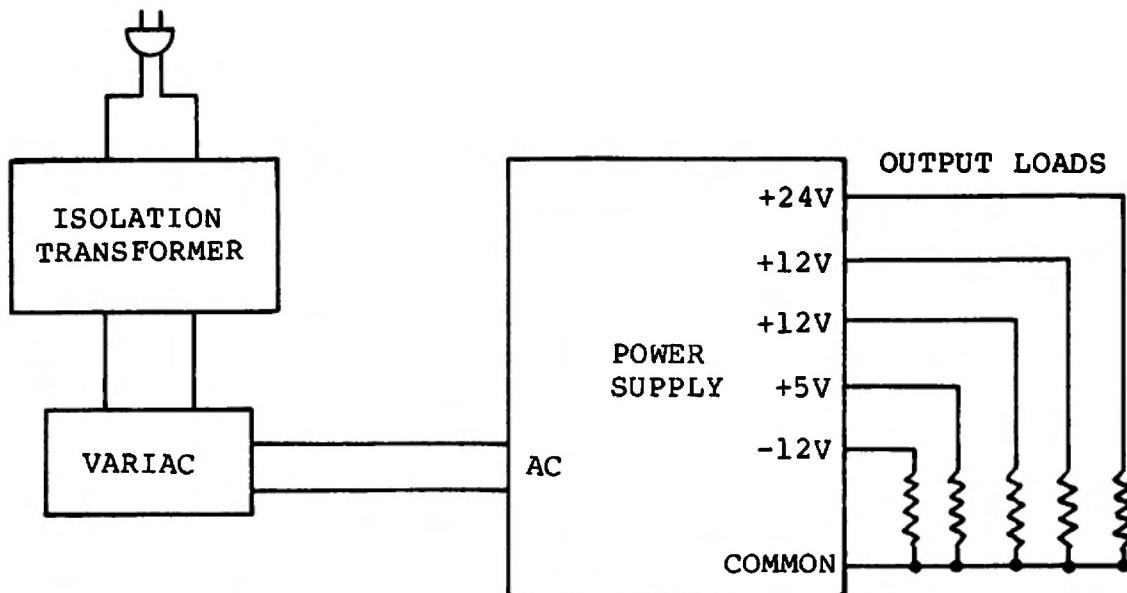
Figure 7-11.   Test Layout, Power Supply

2. Visual Inspection

    Check power supply for any broken, burned, or obviously
    damaged components. Visually check the fuse. If any
    questions, check with an ohmmeter.

3. Start-Up

    Load power supply with minimum load as specified in
    Table 7-5. Bring up power slowly with the variable
    transformer while monitoring the +5 V output with the
    oscilloscope and DVM. The power supply should start
    with approximately 40-60 volts applied, and should
    regulate when 95 VAC is reached. If the output has
    reached 5 volts, complete a performance test as shown in
    Section 7.3.5. If there is no output, refer to Section
    7.3.4.

4. Bracket Removal

    The main PCB is held to the bracket with screws and uses
    spacers to separate the PCB from the bracket. An
    insulator is inserted between the PCB and the mounting
    bracket to ensure that the bracket cannot short any of
    the pins of the PCB.

7.6.4. No Output

1. Check Fuse

    If a fuse is blown, replace it but do not apply power
    until the cause of the failure is found.

2. Preliminary Check on Major Primary Components

    Check diode bridge (DB1), power transistor (Q7), and
    catch diode (Q7) for shorted junctions. If any
    component is found shorted, replace it.

3. Preliminary Check of Major Secondary Components

    Use an ohmmeter to check for shorted outputs on the
    various output lines. If the +5 V output is shorted,
    check also crowbar SCR (SCR1) and zener diode (Z1).

4. Check for B+

    Set up power supply and attach the X10 scope probe
    ground to the cathode side of D5. Slowly turn up the
    power and check for B+ on the cathode side of D9. With
    an input of 95 VAC, this point should be betweeen 130
    and 170 VDC. If this is not correct, check DB1, the
    fuse (F1), and if necessary, R5, D12, and D13. Also
    check input capacitors C5, C6, C7 and C8.

                         CAUTION

              Your scope should be powered by
              an isolation transformer.

5. Check Q1 Waveforms

    Using X10 probe on the case of TO-3 package of Q7, check
    the collector waveform. The transistor should be
    switching. The correct waveform is shown in Figure
    7-12. If switching is not present, check for shorted
    junctions on Q7. If Q7 is not shorted, check the base
    waveform.

    The base of Q7 (looking under the PCB) is the pin from
    the center of Q7 closest to the PCB edge. The correct
    waveform is shown in Figure 7-13. If the waveform is
    there, the problem is on the secondary side of the
    supply. If the wave form is not correct, the problem is
    in the control section of the supply and the supply
    should be returned to the repair depot.

100V/Div   2V/Div
100 uSec/Div   10 uSec/Div
Input-95VAC
Load-minimum
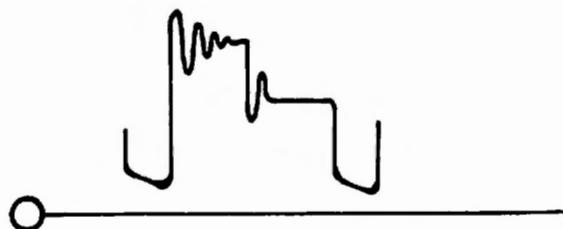
Figure 7-12.   Q7 Collector   Figure 7-13.   Q7 Base
           Waveform   Waveform
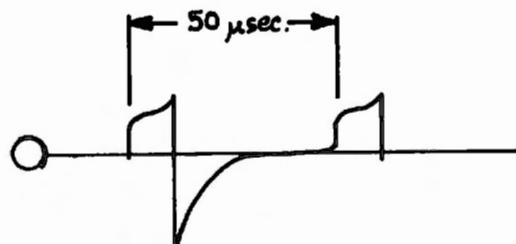
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7.6.5 Performance Test

Each of these test conditions should be set up and noted to
be within the limits specified in Table 7-6.

Test	Input	+5 Load	+12 Load	+24 Load	-12 Load
1	95 VAC	Max	Max	Max	Max
2	135 VAC	Max	Max	Max	Max
3	*135 VAC	Max	Max	Max	Max
4	135 VAC	Min	Min	Min	Min
5	95 VAC	Min	Min	Min	Min

*On Test 3, input voltage should be varied over the full
range to search for instability after correct outputs
are noted at 135 VAC.

Output	Min	Max	No Load	Ripple
V01/+5 Volt	4.90V	5.10V	-	50 mV P-P
V02/+12 Volt	11.40V	12.60V	-	100 mV P-P
V03/+12 Volt	See Note 1	See Note 1	-	100 MV P-P
V04/+24 Volt	21.20V	26.40V	30.0V	250 mv P-P
V05/-12 Volt	-11.40	-12.60V	-	50 mV P-P

Table 7-10. Voltage and Ripple Specifications
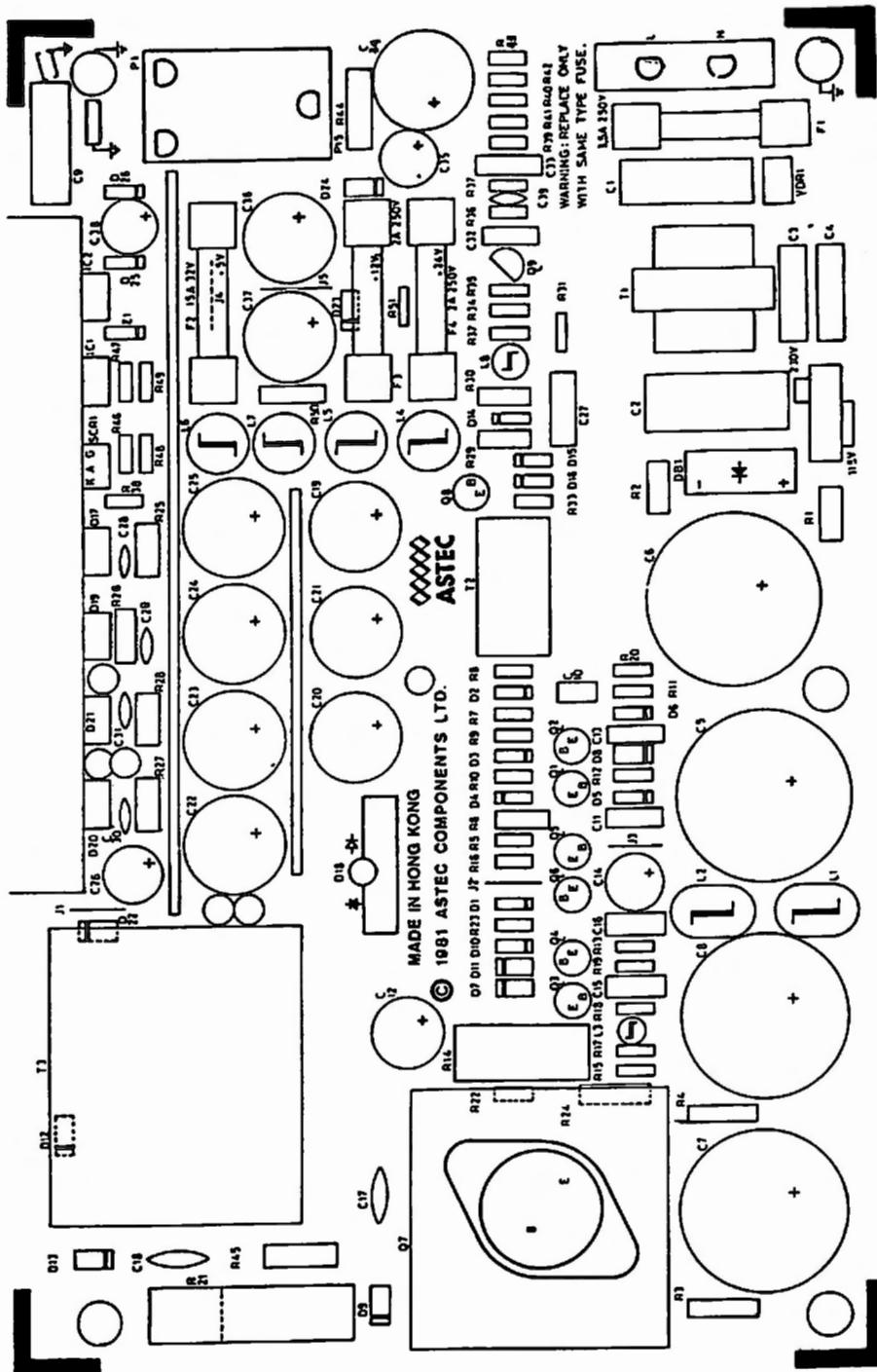
Notes:

1. V03 must not change from its initial value by more than
    +/- 100 mV under the following load conditions on the
    V04 output.

    A step increase in output current from 0.0A to 2.5A
    maximum decaying to 0.92A total within 350 ms.

    A step increase in output current from .55A to 3.05A
    maximum decaying to 1.45A total within 350 ms.

2. V03 output voltage may vary +/-5% under all other
    conditions of rated line load and temperature.

Component Layout, Power Supply 8790047

Parts List, Power Supply 8790047 (Astec Components AA11082)

```
===================================================================
Ref No.    Description                            Mfr. Part No.
===================================================================
```

Capacitors

Ref No.	Description				Mfr. Part No.
C1	Capacitor,	0.1 uF,	250VAC,	20%	068-10400010
C2	Capacitor,	0.22 uF,	250VAC,	10%	068-22400010
C3	Capacitor,	2200 pF,	400VAC,	20%4)	055-22220001
C4	Capacitor,	2200 pF,	400VAC,	20%	055-22220001
C5	Capacitor,	220 uF,	250V,	+100/-10%	057-22120200
C6	Capacitor,	220 uF,	250V,	+100/-10%	057-22120200
C7	Capacitor,	220 uF,	250V,	+100/-10%	057-22120200
C8	Capacitor,	220 uF,	250V,	+100/-10%	057-22120200
C9	Capacitor,	0.01 uF,	250VAC,	20%	068-10300010
C10	Capacitor,	2200 pF,	50V,	10%	058-22200020
C11	Capacitor,	0.047 uF,	250V,	10%	058-47300090
C12	Capacitor,	330 uF,	25V,	20%	057-33120160
C13	Capacitor,	0.22 uF,	100V,	10%	058-22400120
C14	Capacitor,	220 uF,	10V,	20% SxA	059-22120300
C15	Capacitor,	0.22 uF,	100V,	10%	058-22400120
C16	Capacitor,	0.1 uF,	100V,	10%	058-10400110
C17	Capacitor,	1000 pF,	3KV,	20% Z5P	055-10267728
C18	Capacitor,	0.01 uF,	1KV,	20% Z5V	055-10368925
C19	Capacitor,	470 uF,	35V,	20% SxA	057-47120230
C20	Capacitor,	470 uF,	25V,	20% SxA	057-47120220
C21	Capacitor,	470 uF,	25V,	20% SxA	057-47120220
C22	Capacitor,	2200 uF,	25V,	20% SxA	057-22220130
C23	Capacitor,	2200 uF,	25V,	20% SxA	057-22220130
C24	Capacitor,	2200 uF,	25V,	20% SxA	057-22220130
C25	Capacitor,	2200 uF,	25V,	20% SxA	057-22220130
C26	Capacitor,	100 uF,	25V,	20% SxA	057-10120270
C27	Capacitor,	0.22 uF,	100V,	10%	058-22400120
C28	Capacitor,	1000 pF,	100V,	10%	055-10250528
C29	Capacitor,	0.01 uF,	100V,	+80/-20%	055-10382125
C30	Capacitor,	0.01 uF,	100V,	+80/-20%	055-10382125
C31	Capacitor,	0.01 uF,	100V,	+80/-20%	055-10382125
C32	Capacitor,	0.022 uF,	100V,	20%	058-22300080
C33	Capacitor,	0.022 uF,	100V,	10%	058-22400120
C34	Capacitor,	1000 uF,	35V,	20% SM	057-10220190
C35	Capacitor,	100 uF,	25V,	20% SxA	057-10120270
C36	Capacitor,	1000 uF,	16V,	20% SxA	057-10220180
C37	Capacitor,	470 uF,	25V,	20% SxA	057-47120220
C38	Capacitor,	100 uF,	25V,	20% SxA	057-10120270
C39	Capacitor,	1000 pF,	100V,	10%	055-10250528

Coils

Ref No.	Description	Mfr. Part No.
L1	Toroid	124-00000110
L2	Toroid	124-00000110
L3	Choke, 1.5 mH	328-00100010

Parts List, Power Supply 8790047 (Astec Components AA11082)

Ref No.	Description	Mfr. Part No.

Coils (con't)

Ref No.	Description	Mfr. Part No.
L4	Choke Coil Assy	852-20100010
L5	Choke Coil Assy	852-20100010
L6	Filter Choke Coil Assy	852-20100220
L7	Filter Choke Coil Assy	852-20100220

Diodes

Ref No.	Description	Mfr. Part No.
D1	Diode, 1N4606	212-10700210
D2	Diode, 1N4606	212-10700210
D3	Diode, 1N4606	212-10700210
D4	Diode, 1N4606	212-10700210
D5	Diode, 1N4606	212-10700210
D6	Diode, 1N4606	212-10700210
D7	Rectifier, 1N4001GP	226-10400080
D8	Diode, 1N4606	212-10700210
D9	Rectifier, RGP10J	226-10400060
D10	Diode, 1N4606	212-10700210
D11	Rectifier, 1N4001GP	226-10400080
D12	Rectifier, RGP10J	226-10400060
D13	Rectifier, RGP10J	226-10400060
D14	Diode, 1N4606	212-10700210
D15	Diode, 1N4606	212-10700210
D16	Diode, 1N4606	212-10700210
D17	Rectifier, S6K20	226-11300010
D18	Rectifier, RG3B	226-10700010
D19	Rectifier, S6K20	226-11300010
D20	Diode, SCK S10SC3M	211-10300210
D21	Diode, SCK S10SC3M	211-10300210
D22	Rectifier, RGP10B	226-10400070
D23	Rectifier, 1N4001GP	226-10400080
D24	Rectifier, 1N4001GP	226-10400080
D25	Rectifier, 1N4001GP	226-10400080
D26	Rectifier, 1N4001GP	226-10400080
DB1	Bridge Rectifier, KBL08	226-30800010
Z1	Diode, Zener, 5.6V, 5%, 40mA	222-56086002

Fuses

Ref No.	Description	Mfr. Part No.
F1	Fuse, 3.5A, 250V, 3AG	084-00300110
F2	Fuse, 15A, 32V	084-00400020
F3	Fuse, 2A, 250V, 3AG	084-00300020
F4	Fuse, 2A, 250V, 3AG	084-00300020

Parts List, Power Supply 8790047 (Astec Components AA11082)

Ref No.	Description			Mfr. Part No.
Jumpers				
J1	Jumper Wire, 12.7 mm			358-80800001
J2	Jumper Wire, 12.7 mm			358-80800001
J3	Jumper Wire, 12.7 mm			358-80800001
J4	Jumper Wire, 17 mm			358-80800001
J5	Jumper Wire, 17 mm			358-80800001
Integrated Circuits				
IC1	Regulator, LM317T			211-10300100
IC2	Regulator, MC7912			211-10300210
Resistors				
R1	Thermistor,	4 ohm,	10%	258-40970015
R2	Thermistor,	4 ohm,	10%	258-40970015
R3	Resistor,	100K ohm,	5% 1W	248-10406052
R4	Resistor,	100K ohm,	5% 1W	248-10406052
R5	Resistor,	10 ohm,	5% 1/4W	240-10006022
R6	Resistor,	470 ohm,	5% 1/2W	240-47106033
R7	Resistor,	68 ohm,	5% 1/4W	240-68006022
R8	Resistor,	1K ohm,	5% 1/4W	240-10206022
R9	Resistor,	150 ohm,	5% 1/4W	240-15106022
R10	Resistor,	100 ohm,	5% 1/4W	240-10106022
R11	Resistor,	470 ohm,	5% 1/4W	240-47106022
R12	Resistor,	470 ohm,	5% 1/4W	240-47106022
R13	Resistor,	220 ohm,	5% 1/4W	240-22106022
R14	Resistor,	27 ohm,	5% 5W, WW	257-27006120
R15	Resistor,	1K ohm,	5% 1/4W	240-10206022
R16	Resistor,	18 ohm,	5% 1/4W	240-18006022
R17	Resistor,	10 ohm,	5% 1/4W	240-10006022
R18	Resistor,	56 ohm,	5% 1/4W	240-56006022
R19	Resistor,	47 ohm,	5% 1/4W	240-47006022
R20	Resistor,	100 ohm,	5% 1/4W	240-10106022
R21	Resistor,	510 ohm,	5% 5W	257-51106120
R22	Resistor,	10 ohm,	5% 1/4W	240-10006022
R23	Resistor,	270 ohm,	5% 1/4W	240-27106022
R24	Resistor,	0.47 ohm,	5% 2W	247-04786065
R25	Resistor,	10 ohm,	5% 1/2W	240-10006033
R26	Resistor,	10 ohm,	5% 1/2W	240-10006033
R27	Resistor,	10 ohm,	5% 1/2W	240-10006033
R28	Resistor,	10 ohm,	5% 1/2W	240-10006033
R29	Resistor,	270 ohm,	5% 1/2W	240-27106033
R30	Resistor,	560 ohm,	5% 1/2W	240-56106033
R31	Resistor,	39 ohm,	5% 1/4W	240-39006022
R32	Resistor,	12 ohm,	5% 1/4W	240-12006022
R33	Resistor,	330 ohm,	5% 1/4W	240-33106022

Radio Shack ®

Parts List, Power Supply 8790047 (Astec Components AA11082)

===
| Ref No. | Description | | | | | Mfr. Part No. |
===

Resistors (con't)

Ref	Description	Value				Mfr. Part No.
R34	Resistor,	56 ohm,	5%	1/4W		240-56006022
R35	Resistor,	47 ohm,	5%	1/4W	*	240-47006022
R36	Resistor,	12K ohm,	5%	1/4W		240-12306022
R37	Resistor,	470 ohm,	5%	1/4W		240-47106022
R38	Resistor,	12 ohm,	5%	1/4W		240-12006022
R39	Resistor,	2.7K ohm,	2%	1/4W		247-27015022
R40	Resistor,	2.7K ohm,	2%	1/4W		247-27015022
R41	Resistor,	100K ohm,	5%	1/4W		240-10406022
R42	Resistor,	100K ohm,	5%	1/4W		240-10406022
R43	Resistor,	100K ohm,	5%	1/4W		240-10406022
R44	Resistor,	330 ohm,	5%	2W		248-33106063
R45	Resistor,	0.47 ohm,	5%	1W		247-04786054
R46	Resistor,	15K ohm,	5%	1/4W		240-15306022
R47	Resistor,	220 ohm,	2%	1/4W		247-22005022
R48	Resistor,	220K ohm,	5%	1/4W		240-22406022
R49	Resistor,	2.2K ohm,	1%	1/4W		247-22014022

Transformers

Ref	Description	Mfr. Part No.
T1	Transformer Assy	852-10200680
T2	Transformer Assy	852-10200680
T3	Transformer Assy, Power	852-10201300

Transistors

Ref	Description	Mfr. Part No.
Q1	Transistor, NPN, SD467	209-11700460
Q2	Transistor, PNP, SB561	210-11700350
Q3	Transistor, PNP, SB561	210-11700350
Q4	Transistor, NPN, SD467	209-11700460
Q5	Transistor, PNP, SB561	210-11700350
Q6	Transistor, NPN, SD467	209-11700460
Q7	Transistor, NPN, 2SC1325A	209-10200040
Q8	Transistor, PNP, SB561	210-11700350
Q9	IC, TL431CLP	211-10800100

Miscellaneous

Ref	Description	Mfr. Part No.
SCR1	SCR, C1 2u	227-13000010
VDR1	VDR, 260VAC	256-26100014

7.7 Sound Board
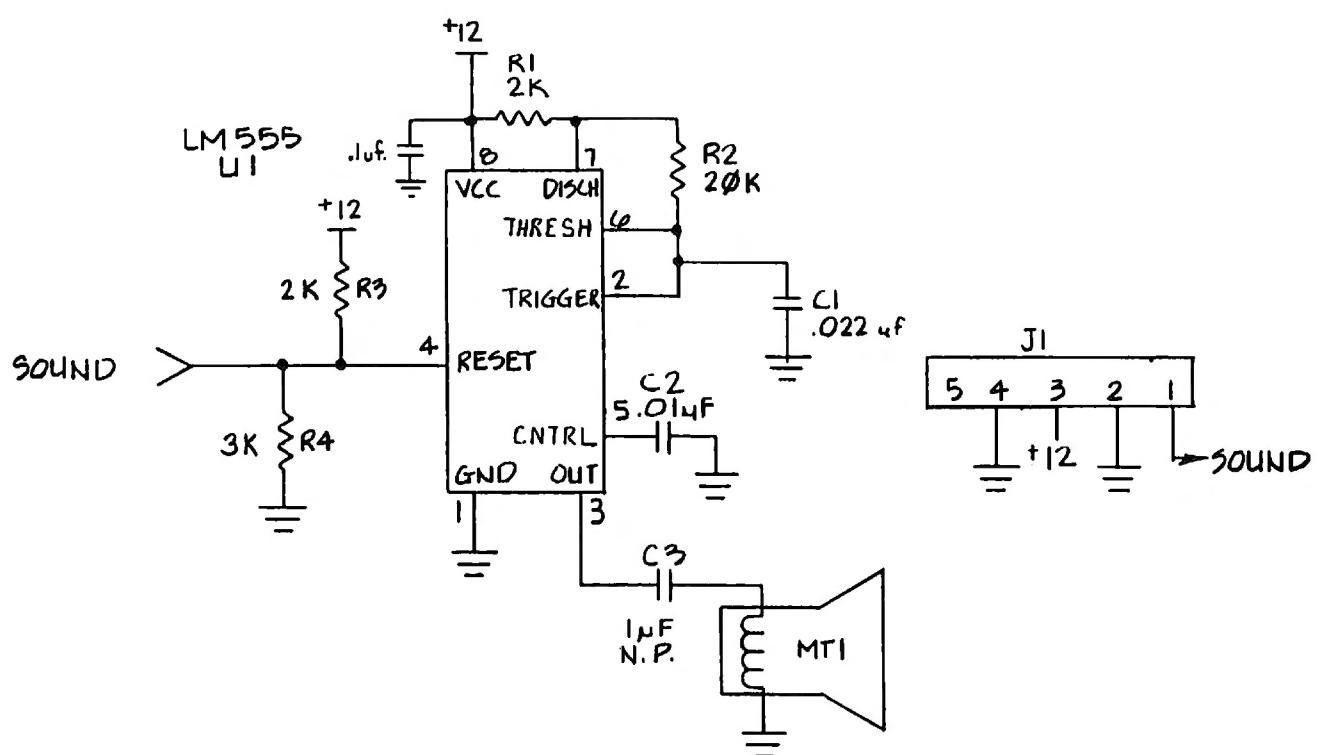
The Sound PCB is a small board located in the front left
corner of the Base Assembly; it is accessible when the
Cover/Bezel Assembly is removed from the Base Assembly (see
Section 3 for disassembly procedures). It is connected to
the I/O Processor PCB by a cable that has a connector on
either end.

The function of the Sound PCB is to generate an audible
signal whenever a key is depressed on the keyboard.

Contained on this board is an LM555 timer/oscillator that
generates a 1558 Hz tone when a pulse is received from the
computer. The voltage required to operate the circuit is 12
volts supplied from the computer at pin 3 of the input jack
J1. The frequency of the device is controlled by R1, R2,
and C1. There is no provision for varying the volume of the
tone generated by the Sound PCB.

Parts List, Sound PCB, 8898429

```
========================================================================
Ref No.    Description                                    Part No.
========================================================================
C1         Capacitor, .022 mF, 50V, +50/-10%              8353224
C2         Capacitor, 0.01 mF, 50V                        8303104
C3         Capacitor,    1 mF, 16V Elec Axial             8395111
C4         Capacitor,  0.1 mF, 50V Mono                   8374104
C5         Capacitor,   10 mF, 16V Elec Radial            8326101

J1         Connector, 5-pin                               8519162

---        PCB, Sound, Rev PP1                            8709368

R1         Resistor,  2K ohm, 1/4W 5%                     8207220
R2         Resistor,  3K ohm, 1/4W 5%                     8207230
R3         Resistor,  2K ohm, 1/4W 5%                     8207220
R4         Resistor, 20K ohm, 1/4W 5%                     8207320

MT1        Transducer, QMB-12, 12V                        8490002

U1         IC, NE555N                                     8050555
```

Schematic 8000165, Sound Board 8898429

7.8   CRT Assembly

The CRT Assembly on the Model 16B/16B-HD is supplied from
several different manufacturers. The assembly consists of
the CRT, the CRT Monitor PCB, which is mounted to the inside
of the Cover/Bezel Assembly, and the associated mounting
hardware. Information concerning each of these assemblies
is contained in the Appendix Section at the rear of this
manual. This information includes a theory of operation of
the CRT Assembly, schematic diagrams of the various
configurations, and parts lists.

Disassembly procedures for the CRT Assembly are contained in
Section 3 of this manual. Exercise care when handling the
CRT as improper handling may cause personal injury.

When replacing the CRT, it must be replaced as an assembly,
i.e., both the CRT and the CRT Monitor PCB must be replaced
at the same time. Adjustment procedures, where applicable,
are noted in the sections contained in the Appendix.

7.9 Keyboard Assembly

The keyboard of the TRS-80 Model 16B/16B-HD is an 82-key, low profile capacitive keyboard that utilizes an 8021 microprocessor chip.

The microprocessor and its associated circuitry scan the key matrix, convert switch closures to an 8-bit digital code and then transmits that code serially to the keyboard interface on the Video/Keyboard Interface PCB.
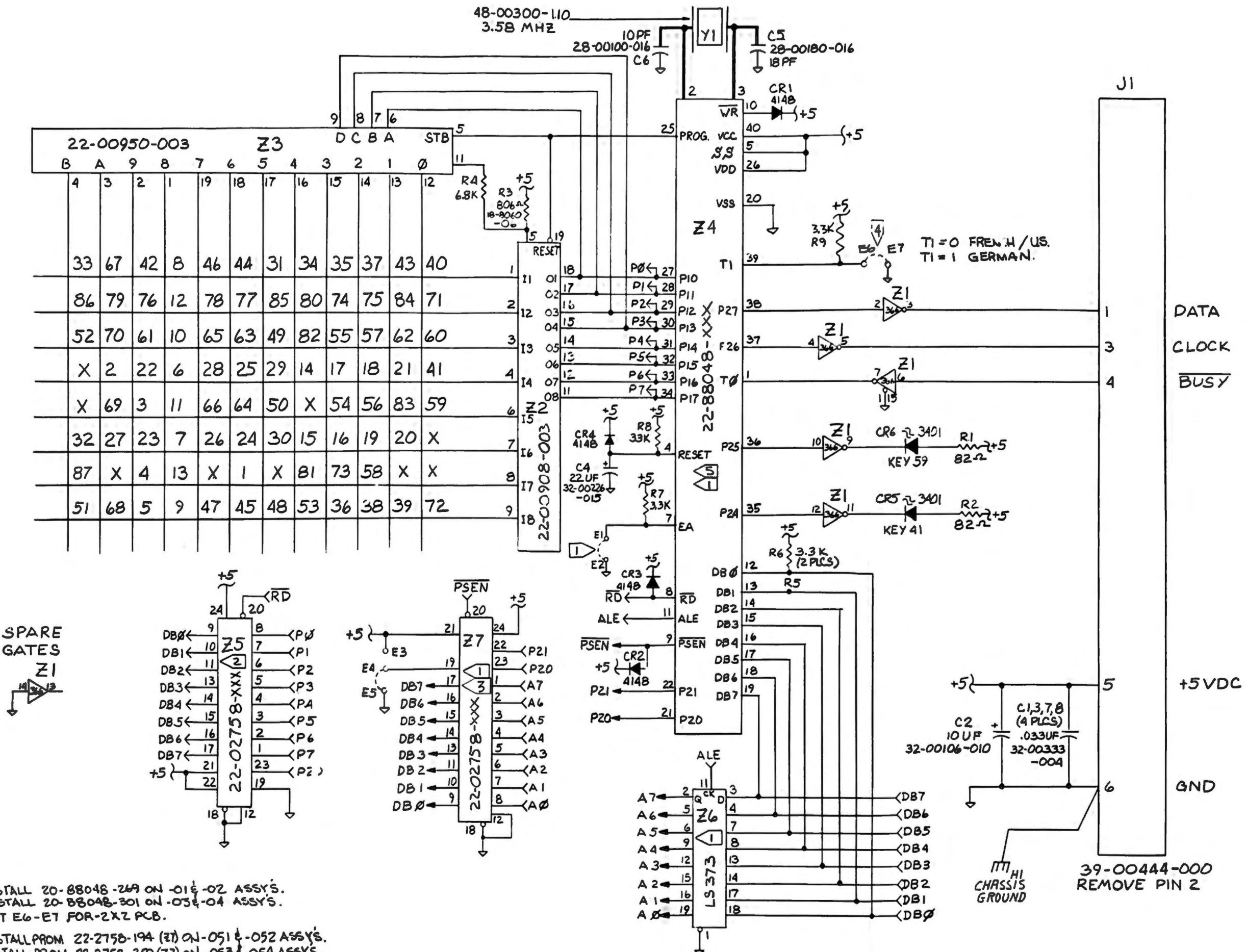
The keyboard is connected to the main console by a built-in cable that plugs into a connector mounted on the front surface of the Base Assembly. The interconnecting mating cable assembly is shown in Figure 5-6.

Parts List, Low Profile Keyboard 8790522

Ref No.	Description	Mfr. Part No.
Capacitors		
C1	Capacitor, C .033 uF, 25V	32-00333-004
C2	Capacitor, T 10 uF, 10V	32-00106-010
C3	Capacitor, C .033 uF, 25V	32-00333-004
C4	Capacitor, T 22 uF, 15V	32-00226-015
C5	Capacitor, C 18 pF, 50V	28-00180-016
C6	Capacitor, C 10 pF, 50V	28-00100-016
C7	Capacitor, C .033 uF, 25V	32-00333-004
C8	Capacitor, C .033 uF, 25V	32-00333-004
---	PCB, 1/16	01-02424-201
Diodes		
CR1	CRO, IN4148	21-04148-000
CR2	CRO, IN4148	21-04148-000
CR3	CRO, IN4148	21-04148-000
CR4	CRO, IN4148	21-04148-000
CR5	LED, 3401 RD LT	21-03401-001
CR6	LED, 3401 RD LT	21-03401-001
Integrated Circuits		
Z1	IC, 74366N	22-74366-001
Z2	IC, 908	22-00908-003
Z3	IC, 950	22-00950-003
Z4	Mup, masked	20-88048-269
Resistors		
R1	Resistor, 82 ohms, 5% 1/4W	25-00820-000
R2	Resistor, 82 ohms, 5% 1/4W	25-00820-000
R3	Resistor, 806, 1% 1/4W	18-08060-006
R5	Resistor, 3.3k ohms, 5% 1/4W	25-00332-000
R6	Resistor, 3.3k ohms, 5% 1/4W	25-00332-000
R7	Resistor, 3.3k ohms, 5% 1/4W	25-00332-000
R8	Resistor, 33K ohms, 5% 1/4W	25-00333-000
R4	Resistor, 6.8K ohms, 5% 1/4W	25-00682-000
Connector, Right Angle 6 (J1)		39-00444-000
Mount, S/B LP		44-00102-000
Bar, S/B 30mm		44-00173-000
Leg, S/B 30mm		44-00174-000
Spring, 1.5 oz, 30mm, yellow		45-00053-015
Spring, 3 oz		45-00053-030
Screw, PH 4-40 .250		47-00008-002
Screw, #2 high/low		47-00368-000

Parts List, Low Profile Keyboard 8790522

```
=====================================================================
XTAL, 3.58 MHz, Dip (Y1)                            48-00300-110
Mounting Plate                                       49-01143-000
Switch, 30mm Capacitor Assy                          61-04024-001
Switch, 30mm Capacitor Assy Lt                       61-04024-002
Switch, Capacitor 30mm                               61-04031-001
Switch, Capacitor 30mm                               61-04031-002
KYTP Set
```

Schematic Diagram 8000196, Keyboard Assembly 8790522

NOTES:

1. ON -050 SERIES ASSYS. ONLY, INSTALL 20-88035-000 AT Z4, INSTALL Z6 & Z7, PER NOTE 3 DELETE CONNECTION E1 TO E2.

2. DO NOT INSTALL.

3. INSTALL PROM 22-2758-194 (Z7) ON -051 & -052 ASSYS. INSTALL PROM 22-2758-259 (Z7) ON -053 & -054 ASSYS.

4. CUT E6-E7 FOR 2X2 PCB.

5. INSTALL 20-88048-269 ON -01 & -02 ASSYS. INSTALL 20-88048-301 ON -03 & -04 ASSYS.

7.10   Hard Disk Controller

7.10.1   System Overview

The Model 16B with built in hard disk (Cat. No. 26-6006) is
identical to the standard 16B (Cat. No. 26-6004), except for
the addition of a 15-megabyte (formatted) hard disk drive,
controller PC board, drive power supply, and associated
cables. The drive is mounted next to the existing floppy
drive in place of a second internal floppy. The power
supply for the hard disk is mounted to the outside of the
drive mounting tower. The controller PC board is located in
the bottom slot of the card cage. There are two cables
connecting the controller and the internal hard drive.
There are also connectors on the controller for adding a
secondary, external hard drive. The extra power supply is
used to power the internal hard drive and a small cooling
fan located under the drive tower. The controller PC board
is powered from the main card cage.

7.10.2   Hard Drive Controller Board

The hard drive controller (HDC) board is a two sided PC
board with the same form and size as those used in the Model
II and Model 16. This board is designed to provide all
control and data signals for connecting one internal and one
external 5.25" Winchester technology drives.

1.   Host System Interface

The HDC is connected to the 16B motherboard via an
80-position card edge connector, J1. Data lines are passed
through an AMD 8303 inverting transceiver, U39. Eight
address lines are buffered by a 74LS240, U40. Most control
signals are buffered by another 74LS240, U41. This board
uses the Z80 interrupt priority daisy chain, so the board
must be placed in either the bottom card slot, or the next
one up, if the system also has an Arcnet board installed.

2.   Port Decoding

The HDC uses a range of 16 consecutive eight bit port
locations with the standard range being C0 to CF. Decoding
of the correct range is done by U33, a 74S138 using the
upper 4 address lines and M1 and IORQ*. A 4 position jumper
enables changing of the range to be recognized. For normal
use, the jumper should be installed between E1 and E2. See
the following table for other configurations.

Jumper Location	Port Range Decoded
E1 to E2	C0 to CF Hex
E1 to E3	70 to 7F HEX
E1 to E4	60 to 7F HEX
E1 to E5	50 to 5F HEX

Table 7-11.   Port Decoding

Further decoding is done by U34, a 74S139 that determines
one of four 4 byte ranges. The first range is indicated by
the signal SELDIR*, which indicates a select of ports C0-C3.
This signal enables one half of another 74S139, U42,
depending on a read or write operation. Only two outputs of
U42 are used, those being WRDIR1* and RDDIR1*. WRDIR1* is
used to clock data onto an octal latch, U12, and RDDIR1* is
used to enable a read from that latch by turning on U21.

Normally the host data bus transceiver is turned to pass
data to the controller board by the state of the signal
M2DEN.   A multiple and-nor gate, U15, is used to determine
one of the following conditions and switch the direction of
data flow toward the host system.   The conditions are: a
read from a port in the selected range, a read of one of the
onboard CTC channels, or an interrupt acknowledge cycle.

The individual ports and their functions will now be listed
referenced to the standard C0-CF range. A more detailed
description will be given later.

Port Address	Description/Use
C0	Write protect status--read only
C1	Control-enable--write/read.
C2	Not used
C3	Not used
C4	CTC channel 0 control
C5	CTC channel 1 control
C6	CTC channel 2 control
C7	CTC channel 3 control
C8	Drive data register
C9	Read--drive error register
	Write--write precompensation
CA	Sector count register
CB	Sector number register
CC	Cylinder LSB register
CD	Cylinder MSB register
CE	SDH register
CF	Read--drive status register
	Write-- command register

Table 7-12.   Ports and Functions

3. Drive Control and Interface

The main device on the controller board is the Western
Digital WD1010 (U26). This is a MOS/LSI part that performs
the function of drive controller/formatter. The WD1010 is
software compatible with WD1000 series controllers with
certain minor differences.

The WD1010 has an 8-bit bi-directional data bus through
which it communicates with the host bus transceivers.
Selection of the internal registers is accomplished by
activating the appropriate address lines (A0-A2) and the
chip select (CSI) line along with either read or write.
The signals WR*IB and RD*IB are passed through a 74LS368
(U38) to the WD1010,the WD1100-11, and the sector buffer.
This is done because the WD1010 uses CSI (U26-8) as a
bi-directional signal. When the WD1010 is reading or
writing data to the sector buffer it activates the signal
BCS* (U26-1). This signal in the active high state, called
DISHDB, is used to isolate the read and write lines from the
rest of the board. DISHDB is also fed to the data bus
transceiver (U39-9) to isolate the internal data bus from
that of the system. Should the host attempt an access of
the controller status register while the WD1010 is using the
internal bus, the host will see a busy condition and should
not attempt to issue any commands until the bus is free.

The WD1100-11 is essentially a gate array device that serves
multiple functions on the controller board. First, it
provides the drive and head select output lines to the drive
interface. Also, it has two internal 1-shots -- one is used
to shape the incoming drive data pulses to a specified
width, the other is used to provide the signal DRUN, which
tells the WD1010 when to begin attempting an ID read.
Finaly, the WD1100-11 is the sector buffer managing device
that handles the transfer of data, through the WD1010,
between the host and the drive.

The sector buffer, U28, is a 2K x 8-bit static RAM with an
access time of 150 nsec or faster. Data from the drive is
loaded into it by the WD1010 and WD1100-11 for the host
system to read. Data that is to be written onto the drive
is placed into the sector buffer by the host, where the
WD1010 will access it as needed.

The WD1010 and WD1100-11 provide a drive interface
compatible with seagate ST506 type drives. Each drive has a
separate data and control cable. The data and control
signals for the internal primary drive are routed through
connectors J4 and J5. For the external secondary drive,

data and control signals appear at connectors J3 and J2. By
utilizing separate control output signal drivers for each
drive, the need to terminate only the last logical drive has
been eliminated. All drive terminators are left in.
However, control signals coming into the controller board
are fed from both drives into a 741S14 (U19) and then to the
WD1010. Drive select outputs determine which drive is
producing these control input signals. Read and write data
lines are transferred between drives and controller by means
of an RS-422 standard driver-receiver pair, (U4 and U5).

4. Data Recovery

a. System Clock Oscillator

The fundamental clock frequency for the controller board is
provided by a 20 MHz crystal oscillator, U2. One-half of U3
divides this down to a 10 MHz square wave signal called
2XDR, which is 2 times the drive data transfer rate. This
clock is again divided down by U18 to provide a 5 MHz clock
called WCLK, which is used to run the WD1010.

b. Phase Comparator

The phase comparator circuitry is comprised of a PAL16R6A
(U18), a 60 nsec delay line (U37), and 3 D-type flip-flops
(U1 and U7). When data is being inspected from the drive,
its phase relationship must be determined with respect to
the Vco clock. The function of the circuitry is to provide
windows during which the leading edge of the incoming data
is compared to the leading edge of the Vco. The windows are
approximately 50 nsec in width. The window is initiated by
the leading edge of any data bit as it enters U7-3 (INDATA).
The window is terminated by the same data bit, delayed by 60
nsec, at U7-11 (DLYDATA) or by the Vco output (OSC*) at
U1-3. When both DLYDATA and the nearest OSC* edge arrive at
the detector, the detector is reset (by U17-6) until the
next data bit arrives. DLYDATA sets its detector latch to
produce a pump-up condition at the error amplifier, while
the Vco (OSC*) sets its detector latch to produce a
pump-down condition at the error amplifier.

c. Error Amplifier and Vco

The error amplifier is comprised of a transistor pack, U30,
and a low pass filter. U30 is wired as a balanced current
mirror device that sources or sinks current to the filter
stage. Whenever the Vco is running slower than the incoming
data stream, the error amp receives pump-up pulses. The
filter integrates these pulses to provide an average

increase in the voltage reference to Vco (TP 3), causing the
Vco to speed up. Whenever the Vco is running too fast,the
error amp receives pump-down pulses and provides the Vco
with an average decrease in control voltage (TP 3) which in
turn slows down the Vco. The Vco is a 74S124, U16, which is
initially set by C11 to a free running frequency of 10 MHz.
Supply voltage for the Vco and error amplifier circuits is
provided by a 78M05 +5 volt regulator (VR1). This insures
noise isolation from TTL devices using the system +5 volt
bus.

d. Write Precompensation

Write precompensation is accomplished by two means. First
by the activation of the signal RWC which is produced by the
WD1010 and driven onto the drive control interface. The
WD1010 activates this signal whenever the heads are
positioned at or inside of a pre-determined cylinder of the
drive. The drive uses this signal to reduce the current
flow through the heads while writing data. The other means
of precomping is done by writing data either 12 nsec early
or late when the heads are in the precomp area. The WD1010
continually puts out the signals EARLY* and LATE*, which are
fed into U18 along with RWC. When RWC is active the PAL,
U18, outputs a delayed and latched (by 2XDR) version of
EARLY* and LATE* called EELD and LELD. When RWC is not
active, the signal is not output by U18. These three
signals are used as enables for U31 to pass one of three
WDATA signals, which are separated 12 nsec by the delay
line, through to the RS-422 driver, U4. The PAL output
INDATA will be either RDATA or WDATA depending upon the
signal WGATE.

5. Controller Alignment

The controller alignment should be done after any servicing
to the board or drive components.

1. Move jumper plug from E6-E7 position to E7-E8 position.
   This feeds a 4 MHz clock into the read-data path so the
   drive does not have to be connected (but may be) at this
   time.

2. Adjust R3 until a high going pulse of 75-80 nsec is seen
   on the DLYDATA signal. This signal is available on
   U26-37 for PP-2 boards or on test point 8 for rev A or
   later boards.

3. Adjust R2 until the DRUN signal just begins to toggle.
    DRUN may be found on U27-15 for rev A boards or on test
    point 7 for all other board revisions. This is only a
    preliminary adjustment and does not need to be exact at
    this time.

4. Replace jumper to position E6-E7 and be sure the primary
    drive is connected and powered on.

5. Adjust trim capacitor C11 until a 100 nsec square wave
    (10 MHz) signal is seen at TP 6 and the DC level of TP 3
    is between 2 and 3 volts.

6. Using a diagnostic, such as HQII, format track 1
    (diagnostic track).

7. Next, do a continuous track read of the diagnostic
    track.

8. Set the scope for 2 msec sweep and trigger one channel
    on index (active high) at U19-6. Place the other
    channel on DRUN. You should see two index pulses spaced
    16.67 msec apart.

9. Adjust R2 until you can define seventeen separate low
    pulses on DRUN between the two index marks. By
    adjusting R2 in both directions you can find the
    location where the pulses on DRUN are distinguished most
    clearly. The diagnostic should be incrementing the pass
    counter without error.

10. Next recheck the 10 MHz signal at TP 6 and the Vco
    reference at TP 3 and readjust C11, if needed for a
    stable setting.

11. If drive has a good format on it, execute random reads
    and check for proper operation.

12. If drive does not have a good format (ie. a new drive),
    format the entire drive and then execute a random read
    test.

6. Register specifications

The important controller ports will now be listed in
greater detail. For more information on controller register
functions and programming, see the WD1010 specification
booklet.

1. C0 -- Write Protect Register
   This port is for read only use and only bits D7 and D6
   should be looked at. A logic one in location D7
   indicates the primary drive is write protected and a
   logic one in D6 indicates the secondary drive is write
   protected.

2. C1 -- Control Enable Register
   This port is a write/read register which enables certain
   functions of the controller board.

D0	Logic one enables dma operation
D1	Logic one enables interrupts
D2	Not used
D3 -- DEVEN	Logic one enables access to the WD1010
D4 -- SFTRST	Logic one triggers a 10 usec reset one-shot
D5	Not used
D6	Not used-must be written as 0
D7	Not used-must be written as 0

3. C8 -- Data Register
   Data to and from drive passes through this port.

4. C9
   Write -- This value in hex is the cylinder divided by 4
   where write precompensation starts.

   Read -- This is the controller error register.

D0	Not used-forced to zero
D1	Logic one indicates track 0 was not located when expected
D2	Aborted command
D3	Not used-forced to zero

D4	ID not found-set to one if desired cylinder,head,sector, or size cannot be found after 8 disk revolutions or if a CRC error was encountered in the desired ID field
D5	Not used-forced to zero
D6	When set to one indicates a CRC error was encountered in a data field or if a data address mark was not found
D7	This bit is set when an ID field is encountered with a bad block mark used for bad sector mapping

5. CA -- Sector Count
    This register contains the number of sectors to be transferred. It is used only when multiple sector reads or writes are used.

6. CD -- Sector Number
    This register holds the number of the desired sector to be accessed during read or write sector commands. This must be loaded with the number of bytes to be used for gaps 1 and 3, during a format track command.

7. CC -- Cylinder LSB
    Contains the LSB of the desired cylinder to be accessed.

8. CD -- Cylinder MSB
    Contains the MSB of the desired cylinder to be accessed; only bits D0 and D1 may be used.

9. CD -- SDH register
   This is loaded with the desired sector size, drive
   number, and head number parameters using the following
   form.

Bits 6 5	Sector Size	Bits 2 1 0	Head Selected
0 0	256	0 0 0	HD 0
0 1	512	0 0 1	HD 1
1 0	1024	0 1 0	HD 2
1 1	128	0 1 1	HD 3
		1 0 0	HD 4
Bits 4 3	Drive Select	1 0 1	HD 5
		1 1 0	HD 6
0 0	Drive 0	1 1 1	HD 7
0 1	Drive 1		

   Location D7 should be written as a zero always.

10. CF -- Command/Status
    Write -- The desired command is loaded here, see the
    WD1010 manual for available commands.

    Read -- Controller Status Register

    D0   When set indicates an error has
                occurred; error register should then be
                checked.

    D1   When set indicates a command is still in
                progress and no new command should be
                issued.

    D2   Not used - forced to zero.

    D3   This bit is set whenever the sector
                buffer should be written to or read from
                by the host, depending upon the command.

    D4   This bit reflects the state of the seek
                complete line from the drive.

    D5   This bit reflects the state of the write
                fault line from the drive.
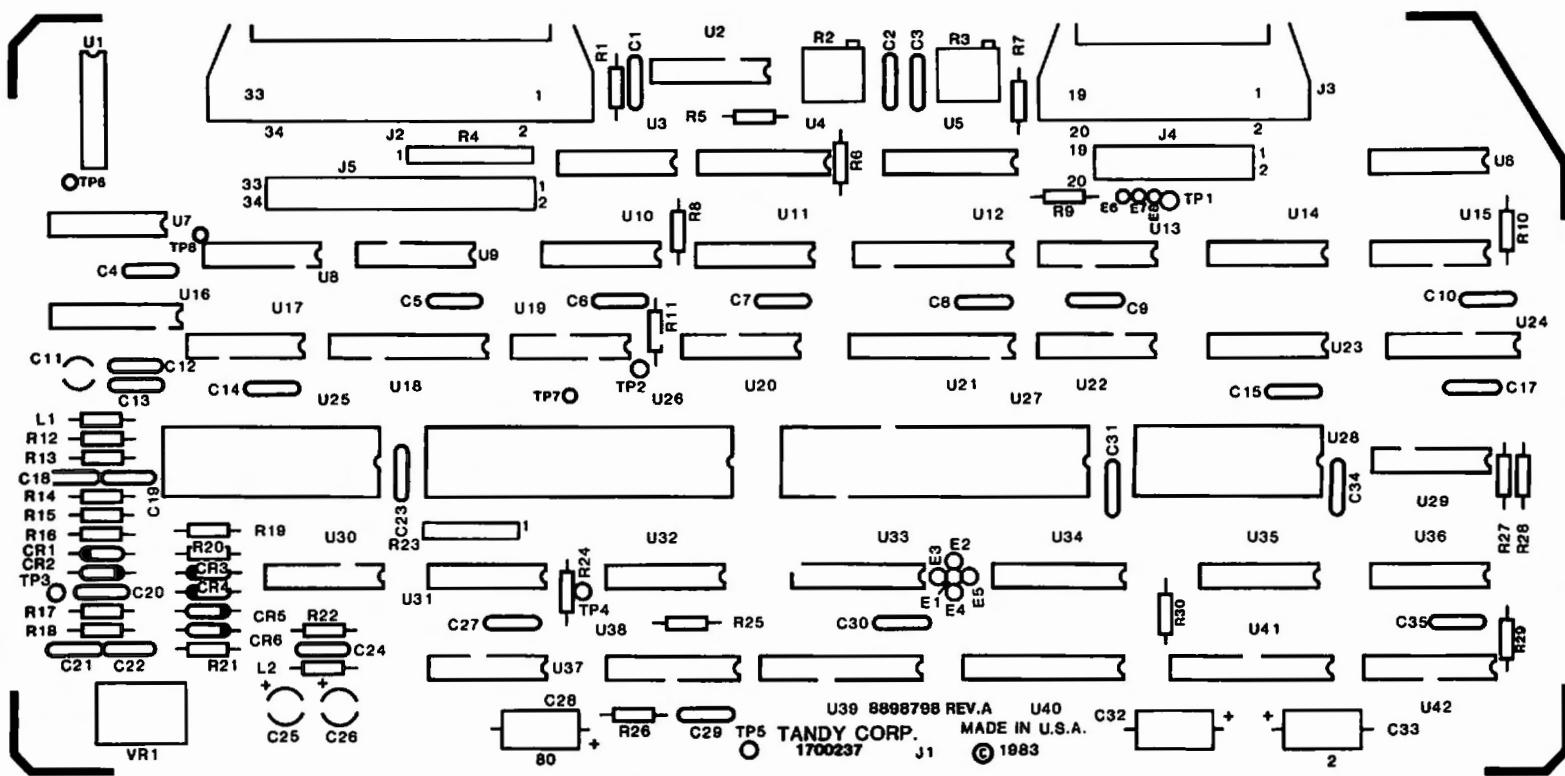
D6   This bit reflects the state of the ready
                            line from the drive. Upon an interrupt
                            for an error this bit is frozen until
                            the status register is read.

D7   This bit is set whenever the WD1010 is
                            busy accessing the drive or the sector
                            buffer.

7.10.3 Hard Disk Drive
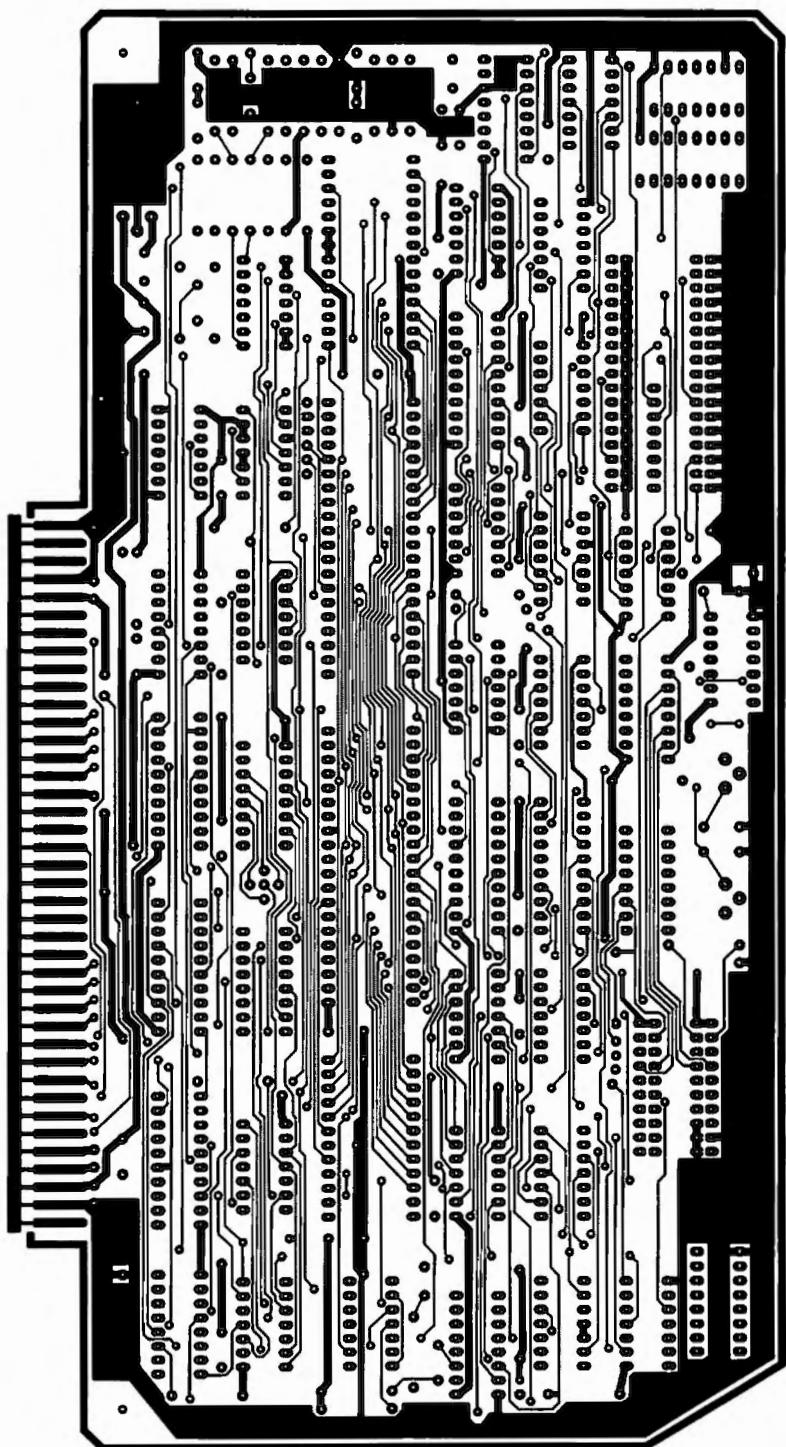
The hard disk that is installed in the Model 16B is a
15-megabyte Tandon TM503. It has 3 5.25" Platters, each
with 2 read/write surfaces for a total of 6 recording
surfaces. Each surface has a dedicated read/write head
attached to a common stepper arm mechanism. Each surface
has a total of 306 cylinders giving a total track count of
1836. For more detailed information on this drive and its
servicing, refer to the Tandon TM500-Series manual.

7.10.4 Hard Disk Power Supply

The power supply that is used to run the Tandon drive is a
38 watt Aztec switching power supply, Model Number AA 11330.
This supply also powers a 12 volt DC ventilation fan located
under the drive mounting tower. For service information of
the power supply refer to the appropriate enclosed manual.
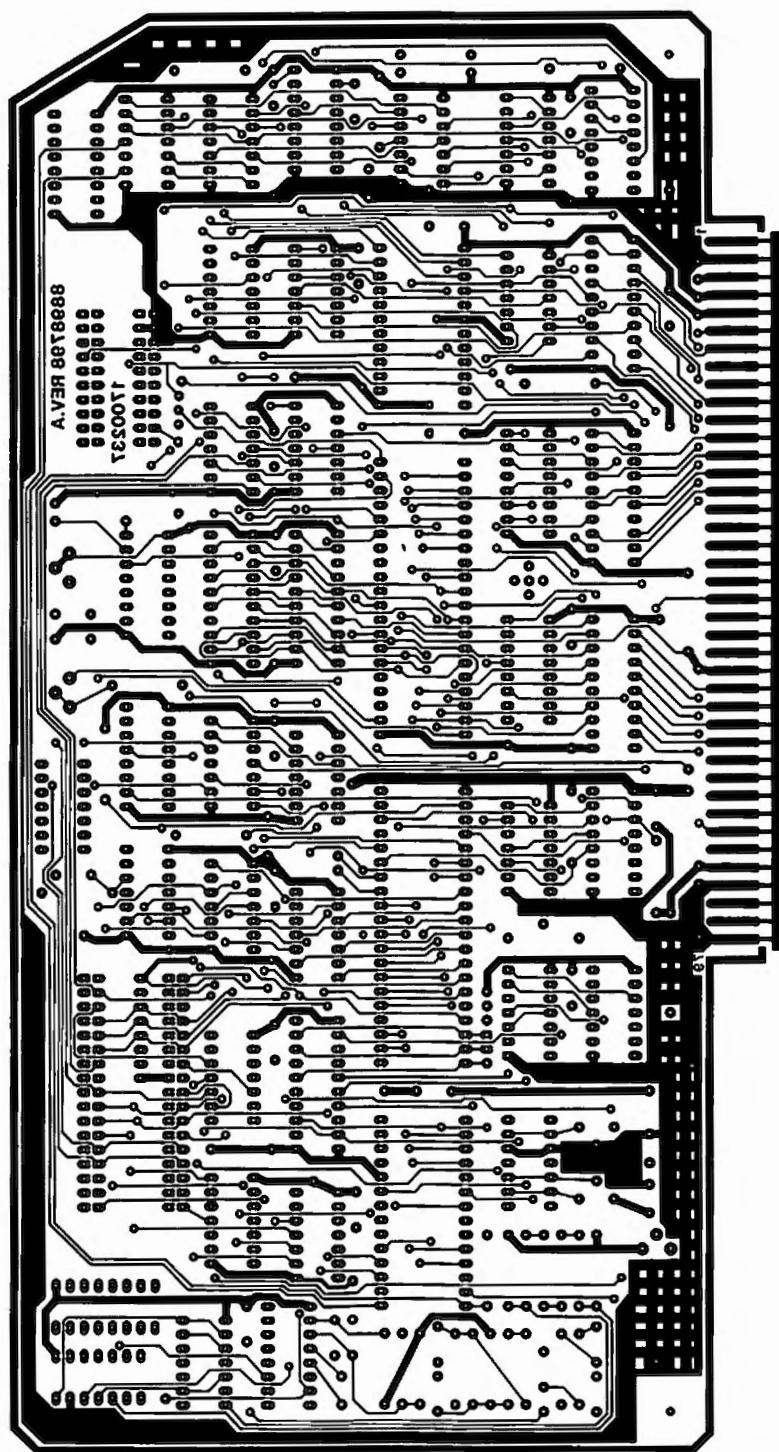
Circuit Trace, Hard Disk Controller 8898798 Rev. A,
Component Side

Circuit Trace, Hard Disk Controller 8898798 Rev. A, Solder
Side

Parts List, Hard Disk Controller PCB, 8898798 Rev. A

```
===========================================================
Ref No. Description                               Part No.
===========================================================
```

Capacitors

Ref No.	Description				Part No.
C1	Capacitor,	100 pF,	50V,	C. Disk	8301104
C2	Capacitor,	100 pF,	50V,	C. Disk, NPO	8301103
C3	Capacitor,	100 pF,	50V,	C. Disk, NPO	8301103
C4	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C5	Not Used				
C6	Not Used				
C7	Not Used				
C8	Not Used				
C9	Not Used				
C10	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C11	Capacitor,	7-60 pF,	Trim		8360607
C12	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C13	Not Used				
C14	Not Used				
C15	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C16	Not Used				
C17	Capacitor,	0.001 uF,	50V,	C. Disk, 10%	8302104
C18	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C19	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C20	Capacitor,	330 pF,	50V,	C. Disk, NPO	8301332
C21	Capacitor,	150 pF,	50V,	C. Disk, NPO	8301153
C22	Capacitor,	0.0068 uF,	50V,	C. Disk, 10%	8302684
C23	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C24	Capacitor,	0.1 uF,	50V,	C. Disk, 10%	8304104
C25	Capacitor,	10 uF,	16V,	Elect. Rad.	8326101
C26	Capacitor,	0.47 uF,	16V,	Elect. Rad.	8324471
C27	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C28	Capacitor,	100 uF,	16V,	Elect. Arial	8317101
C29	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C30	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C31	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C32	Capacitor,	100 uF,	16V,	Elect. Arial	8317101
C33	Capacitor,	100 uF,	16V,	Elect. Arial	8317101
C34	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104
C35	Capacitor,	0.1 uF,	50V,	Mono Axial	8374104

Connectors

Ref No.	Description	Part No.
J2	Connector, 34-Pos. Shrouded Rgt. Ang.	8519196
J3	Connector, 20-Pos. Shrouded Rgt. Ang.	8519197
J4	Connector, 20-Pos. Straight Header	8519121
J5	Connector, 34-Pos. Straight Header	8519120

Parts List, Hard Disk Controller PCB, 8898798 Rev. A

===
Ref No. Description   Part No.
===

Diodes
CR1	Diode,	1N4148				8150148
CR2	Diode,	1N4148				8150148
CR3	Diode,	1N4148				8150148
CR4	Diode,	1N4148				8150148
CR5	Diode,	1N4148				8150148
CR6	Diode,	1N4148				8150148

Resistors
R1	Resistor,	560	ohm,	1/4W,	5%		8207156
R2	Pot.,	10	kohm				8279312
R3	Pot.,	10	kohm				8279312
R4	Res. Pak,	220/330	ohm				8290019
R5	Resistor,	470	ohm,	1/4W,	5%		8207147
R6	Resistor,	1	kohm,	1/4W,	5%		8207210
R7	Resistor,	100	ohm,	1/4W,	5%		8207110
R8	Resistor,	4.7	kohm,	1/4W,	5%		8207247
R9	Resistor,	100	ohm,	1/4W,	5%		8207110
R10	Resistor,	1	kohm,	1/4W,	5%		8207210
R11	Resistor,	4.7	kohm,	1/4W,	5%		8207247
R12	Resistor,	5.6	kohm,	1/4W,	5%		8207256
R13	Resistor,	4.7	kohm,	1/4W,	5%		8207247
R14	Resistor,	2.43	kohm,	1/4W,	1%,	MF	8200224
R15	Resistor,	200	ohm,	1/4W,	1%,	MF	8200120
R16	Resistor,	2.43	kohm,	1/4W,	1%,	MF	8200224
R17	Resistor,	680	ohm,	1/4W,	5%		8207168
R18	Resistor,	330	ohm,	1/4W,	5%		8207133
R19	Resistor,	1	kohm,	1/4W,	5%		8207210
R20	Resistor,	274	ohm,	1/4W,	1%,	MF	8200427
R21	Resistor,	274	ohm,	1/4W,	1%,	MF	8200427
R22	Resistor,	261	ohm,	1/4W,	1%,	MF	8200126
R23	Res. Pak,	1	kohm,	6-Pin SIP			8290210
R24	Resistor,	1	kohm,	1/4W,	5%		8207210
R25	Resistor,	4.7	kohm,	1/4W,	5%		8207247
R26	Resistor,	1	kohm,	1/4W,	5%		8207210
R27	Resistor,	16	kohm,	1/4W,	5%		8207316
R28	Resistor,	4.7	kohm,	1/4W,	5%		8207247
R29	Resistor,	4.7	kohm,	1/4W,	5%		8207247
R30	Resistor,	22	ohm,	1/4W,	5%		8207022

Intergrated Circuits
| U1* | IC, | 74F74, Dual Flip-Flop, | 14-Pin | 8015074 |
| U2 | IC, | Osc., 20 MHz | 14-Pin | 8409029 |

* Note: 74S74 may be substituted for 74F74

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Parts List, Hard Disk Controller PCB, 8898798 Rev. A

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=====================================================================
Ref No. Description                                    Part No.
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Integrated Circuits

Ref No.		Description		Part No.
U3*	IC,	74F74, Dual Flip-Flop,	14-Pin	8015074
U4	IC,	MC3487, Line Driver,	16-Pin	8050487
U5	IC,	MC3486, Line Receiver,	16-Pin	8050486
U6	IC,	74S04, Hex Inverter,	14-Pin	8010004
U7*	IC,	74F74, Dual Flip-Flop,	14-Pin	8015074
U8	IC,	7407, Hex Buffer,	14-Pin	8000007
U9	IC,	7407, Hex Buffer,	14-Pin	8000007
U10	IC,	7438, Quad 2-IN NAND,	14-Pin	8000038
U11	IC,	7438, Quad 2-IN NAND,	14-Pin	8000038
U12	IC,	74LS273, Octal Flip-Flop,	20-Pin	8020273
U13	IC,	7416, Hex Inverter,	14-Pin	8000016
U14	IC,	74LS293, Binary Counter,	14-Pin	8020293
U15	IC,	74S64, AND OR Invert,	14-Pin	8010064
U16	IC,	74S124, Oscillator,	16-Pin	8010124
U17	IC,	74S00, Quad 2-IN NAND,	20-Pin	8010000
U19	IC,	74LS14, Hex Inverter,	14-Pin	8020014
U20	IC,	74LS04, Hex Inverter,	14-Pin	8020004
U21	IC,	74LS244, Octal Buffer,	20-Pin	8020244
U22	IC,	74LS04, Hex Inverter,	14-Pin	8020004
U23	IC,	74LS02, Quad 2-IN NOR,	14-Pin	8020002
U24	IC,	74LS221, Multivibrator,	16-Pin	8020221
U29	IC,	74S08, 2-IN AND,	14-Pin	8010008
U30	IC,	MPQ6700, Transistor Array,	14-Pin	8180700
U31	IC,	74S64, AND OR Invert,	14-Pin	8010064
U32	IC,	74LS02, Quad 2-IN NOR,	14-Pin	8020002
U33	IC,	74S138, Decoder,	16-Pin	8010138
U34	IC,	74S139, Decoder,	16-Pin	8010139
U35	IC,	74S04, Hex Inverter,	14-Pin	8010004
U36	IC,	74S32, Quad 2-IN OR,	14-Pin	8010032
U37	IC,	Delay Line (60 ns)		8429016
U38	IC,	74LS368, Hex Bus Driver	16-Pin	8020368
U39	IC,	AM8303, Bus Transceiver,	20-Pin	8060303
U40	IC,	74LS240, Octal Buffer,	20-Pin	8020240
U41	IC,	74LS240, Octal Buffer,	20-Pin	8020240
U42	IC,	74S139, Decoder,	16-Pin	8010139
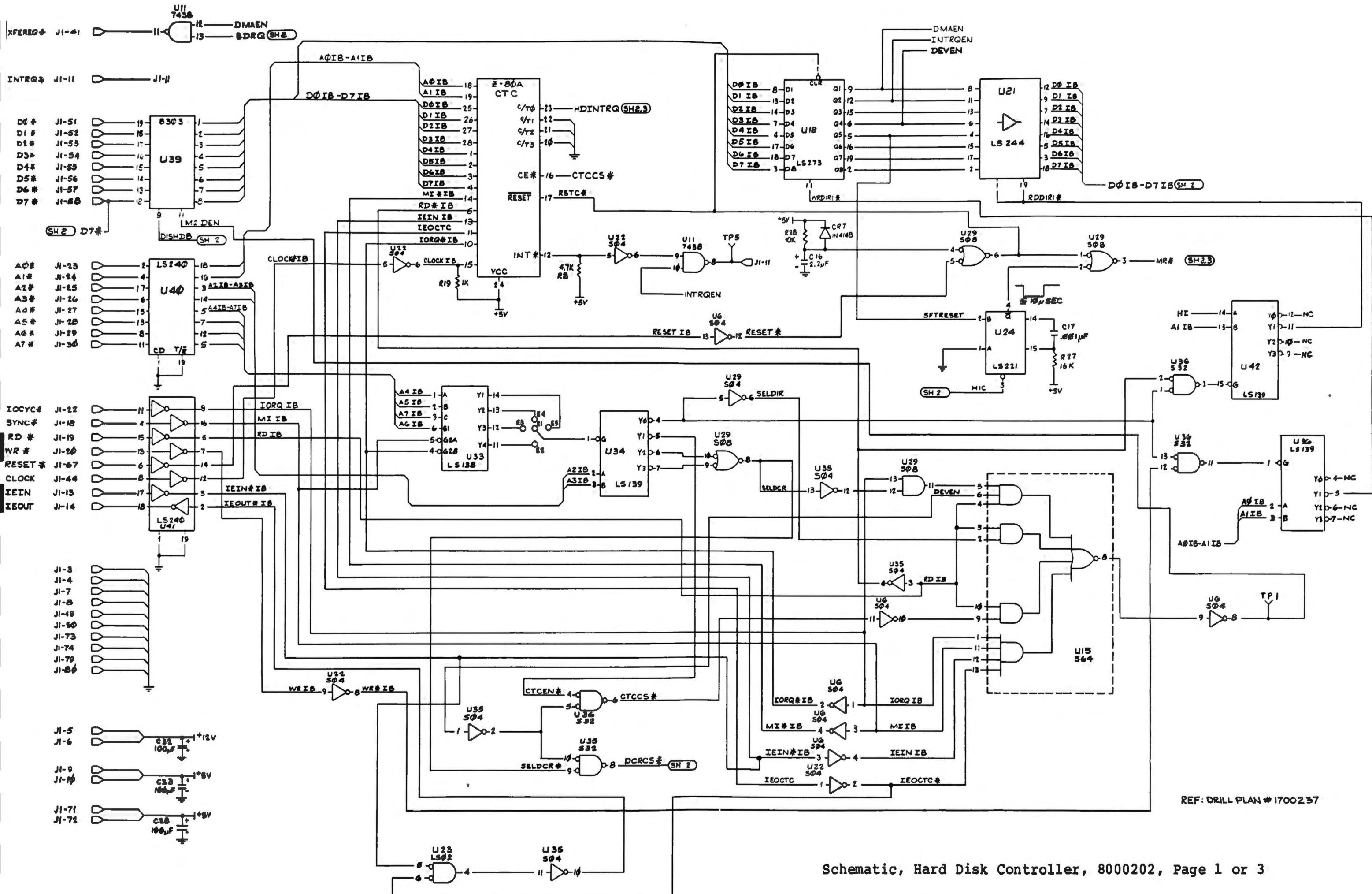
* Note: 74S74 may be substituted for 74F74

Sockets
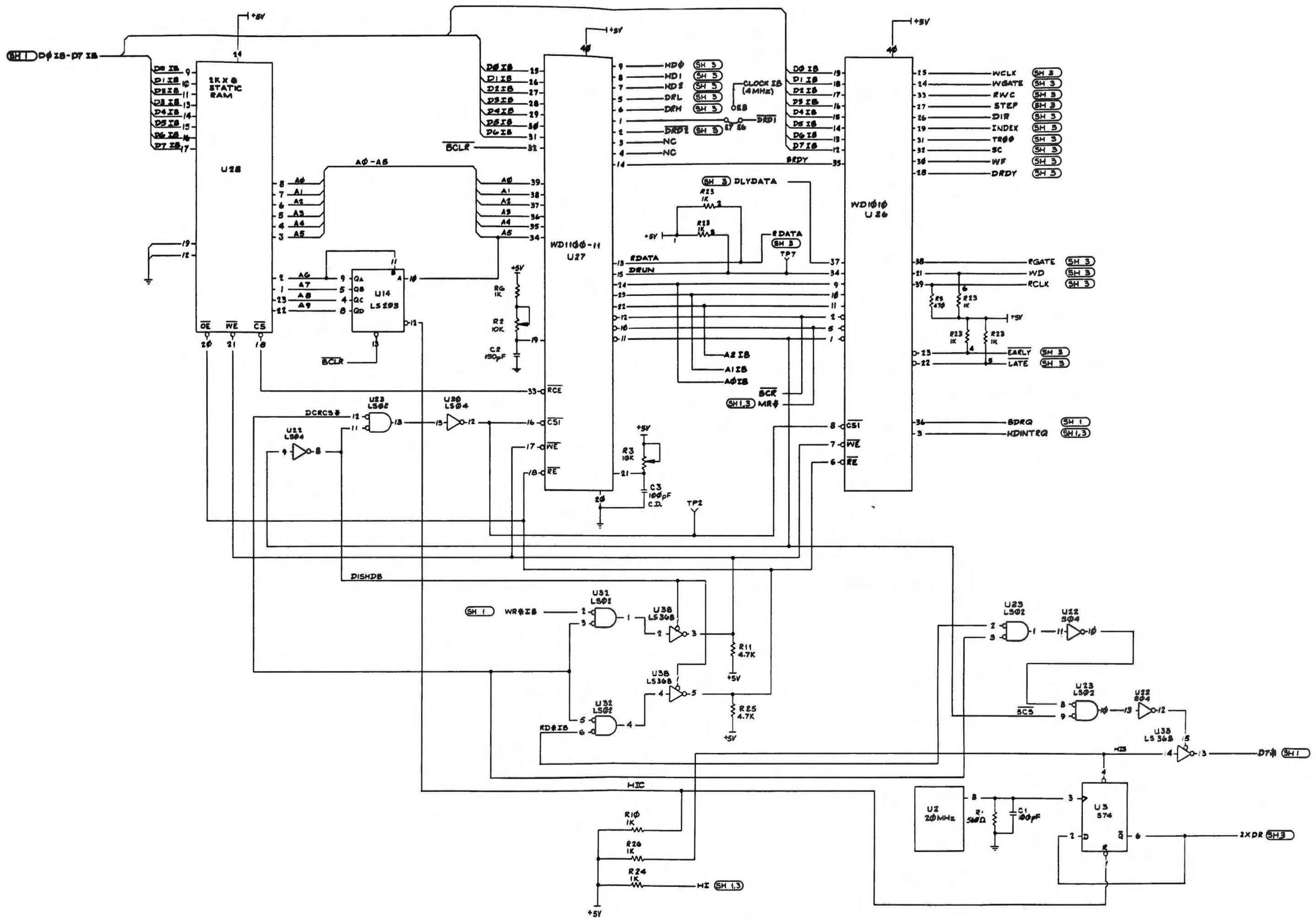
Ref No.	Description	Part No.
U18	Socket, 20-Pin DIP	8509009
U25	Socket, 28-Pin DIP	8509007
U26	Socket, 40-Pin DIP	8509002
U27	Socket, 40-Pin DIP	8509002
U28	Socket, 24-Pin DIP	8509001
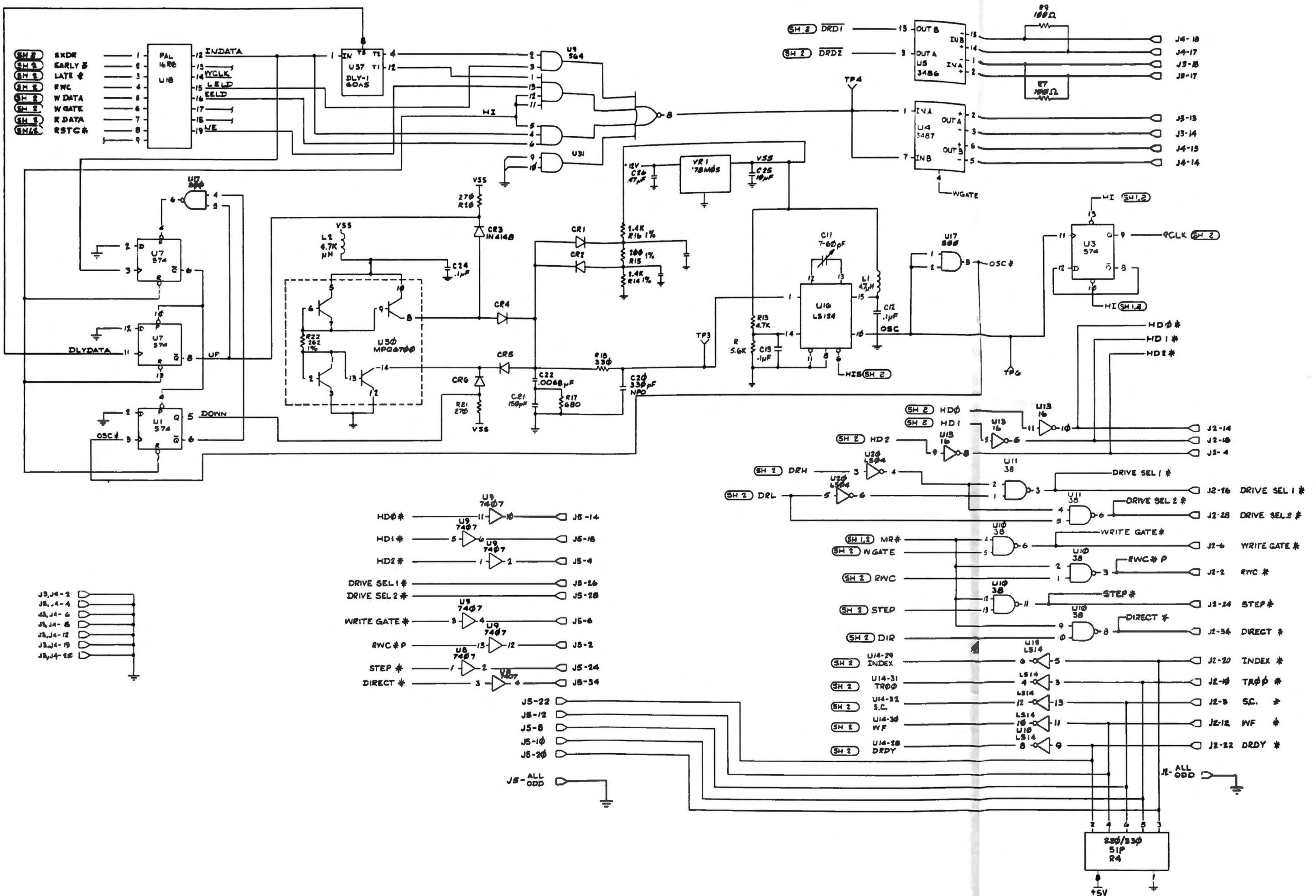
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Parts List, Hard Disk Controller PCB, 8898798 Rev. A

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==================================================================
Ref No. Description                                     Part No.
==================================================================
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Staking Pins

Ref No.	Description	Part No.
TP1	Staking Pin	8529014
TP2	Staking Pin	8529014
TP3	Staking Pin	8529014
TP4	Staking Pin	8529014
TP5	Staking Pin	8529014
TP6	Staking Pin	8529014
TP7	Staking Pin	8529014
E1	Staking Pin	8529014
E2	Staking Pin	8529014
E3	Staking Pin	8529014
E4	Staking Pin	8529014
E5	Staking Pin	8529014
E6	Staking Pin	8529014
E7	Staking Pin	8529014
E8	Staking Pin	8529014

Miscellaneous

Ref No.	Description	Part No.
---	PCB Logic Board Rev.	8709474
L1	Inductor, 4.7 uH, 10%	8419017
L2	Inductor, 4.7 uH, 10%	8419017
VR1	Regulator, 78M05	8051805

Schematic, Hard Disk Controller, 8000202, Page 1 or 3

REF: DRILL PLAN # 1700237

Schematic, Hard Disk Controller, 8000202, Page 3 or 3

8/ Parts Lists/Exploded Views

Contained in this section are the parts lists and exploded
views for the various subassemblies of the Model 16B/16B-HD.
Some parts are noted but may not be available as individual
items. Consult the factory for replacement part
availability.

8.1 Bottom Case S/A 8898531, Model 16B/16B-HD Computer

Item	Quan	Description	Part No.
1	1	Base, Computer	8719302
2	4	Feet, Bumpon	8590128
3	1	Panel, Rear Connector	8729152
4	1	Connector, Power Cord	8519013
5	2	Screw, #4-40 x 1/2" PPH	8569033
6	2	Nut, KEPS Lock #4-40	8579003
7	1	Plug, Hole (ARCNET)	8729125
8	2	Clip, Tinnerman	8559045
9	1	PCB, Sound	8898429
10	2	Screw, #6 x 1/4" Zinc	8569077
11	3	Clip, Tinnerman	8559049
12	3	Screw, #8 x 1" PPH	8569172
13	3	Washer, #8 Internal Star	8589088
14	1	Cable, Keyboard Interface	8709402
15	2	Screw, #8-32 x 3/8"	8569030
16	1	Clamp, 50-Pin Ribbon Cable	8559050
17	3	Screw, #8-32 x 1/4" Hex	8569036
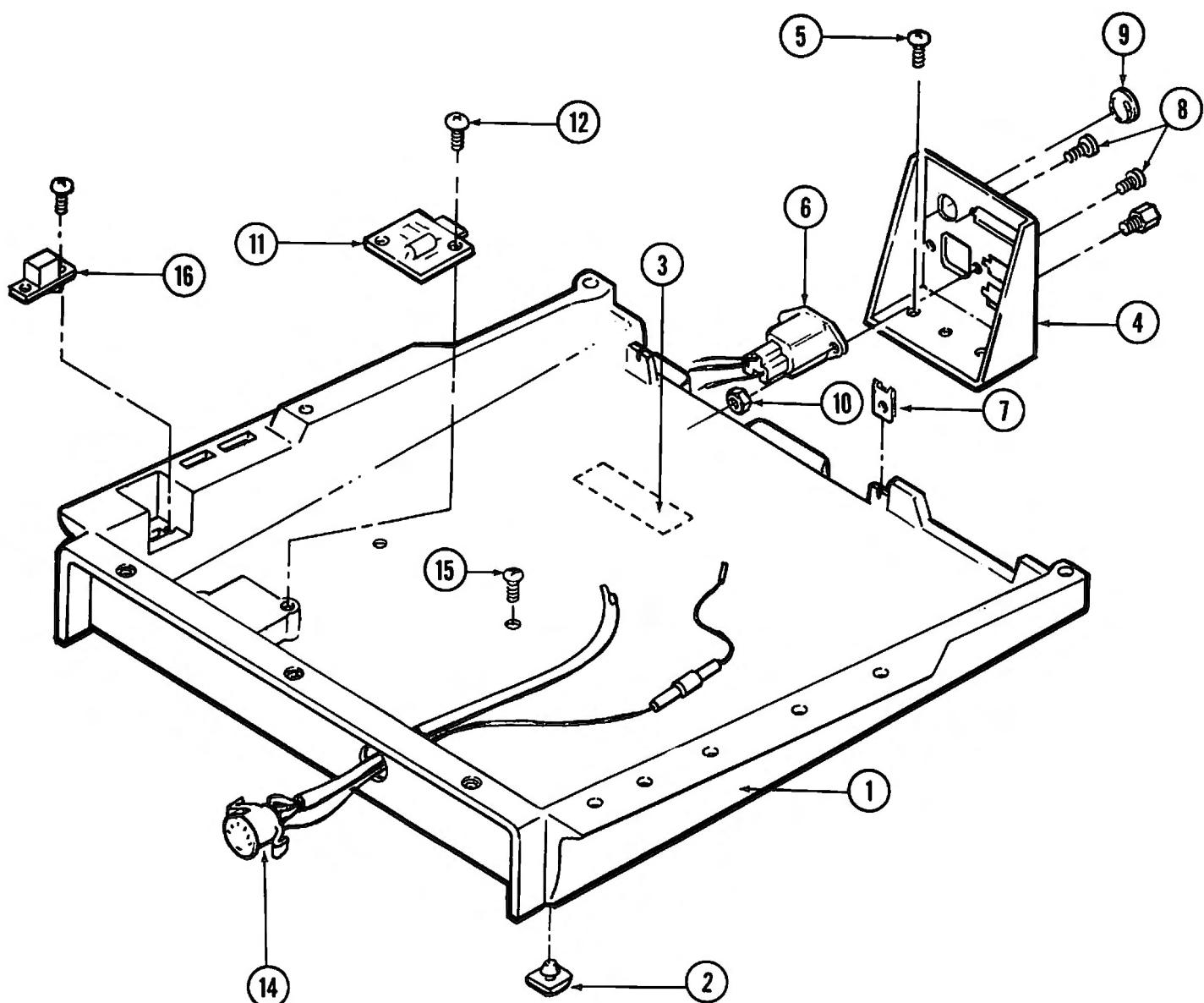
Figure 8-1. Exploded View, Base Assembly

8.2 Electronics Module

```
=================================================================
Item Qty  Description                        Part No.
=================================================================
1    1    Chassis, Main PCB                  8729142
2    2    Strain Relief                      8559046
3    1    Support, Video Board               8719253
4    1    Shield, Rear                       8729174
5    1    Fan Assembly, Cooling              8898519
6    4    Screw, #6-32 x 2" Hex              8569052
7    4    Nut, #6-32 KEPS                    8579004
8    1    I/O Processor PCB Assembly         8898423
9    1    Video/Keyboard PCB Assembly        8898022
10   1    Power Supply PCB Assembly          8790040
11   1    Shield, Power Supply               8729185
12   1    Cover, Power Supply                8898544
13   9    Screw, #6-32x 1/4 Hex              8569168
```
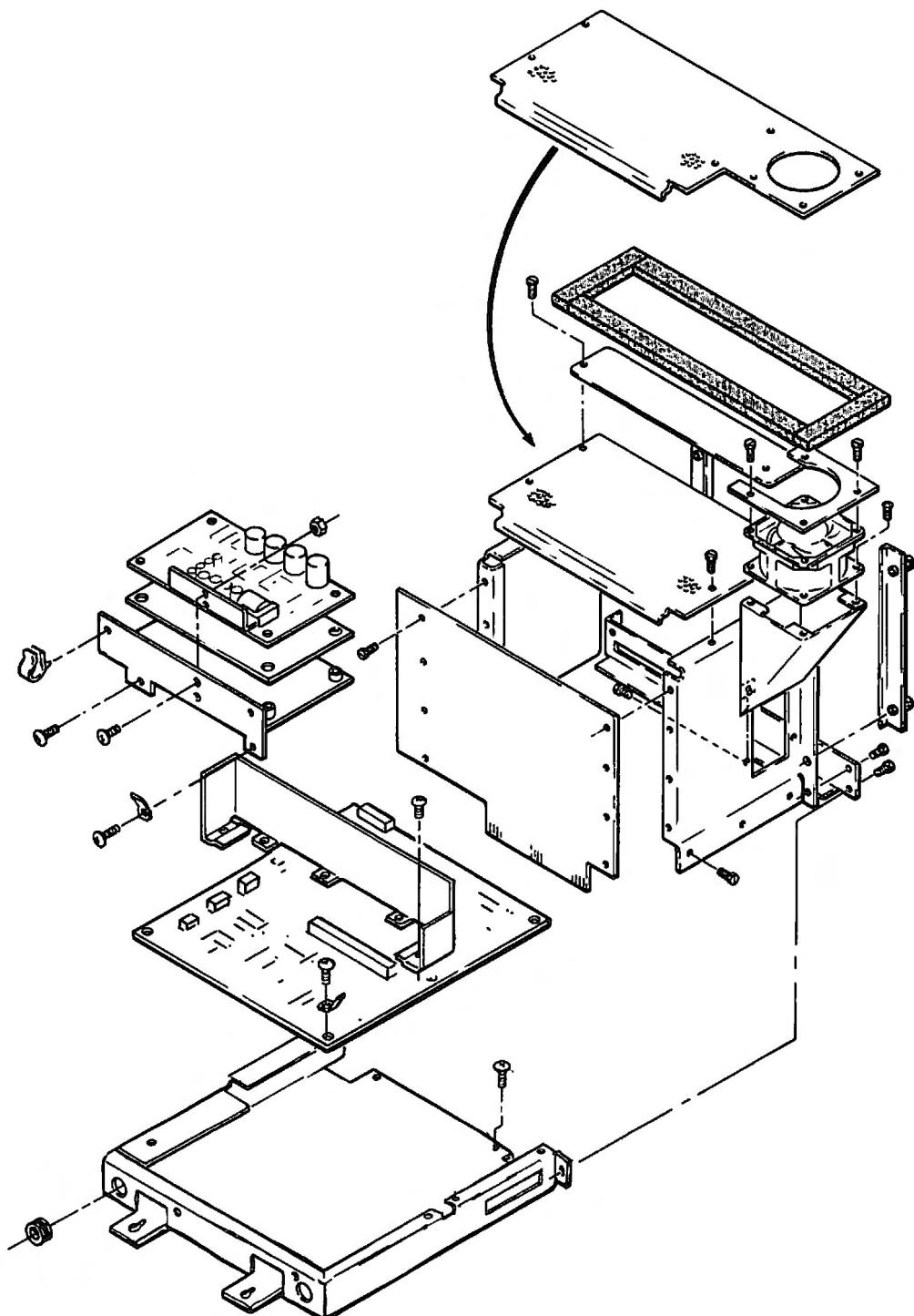
Figure 8-2.   Exploded View, Electronics Module

8.3 Reset/Power On Indicator Module

```
============================================================
Item Qty  Description                          Part No.
============================================================
1    1    Bezel, Switch                        8719255
2    1    Indicator, Power On                  8469011
3    1    Switch, Reset                        8489056
4    1    Cable, Reset Switch                  8709395
```
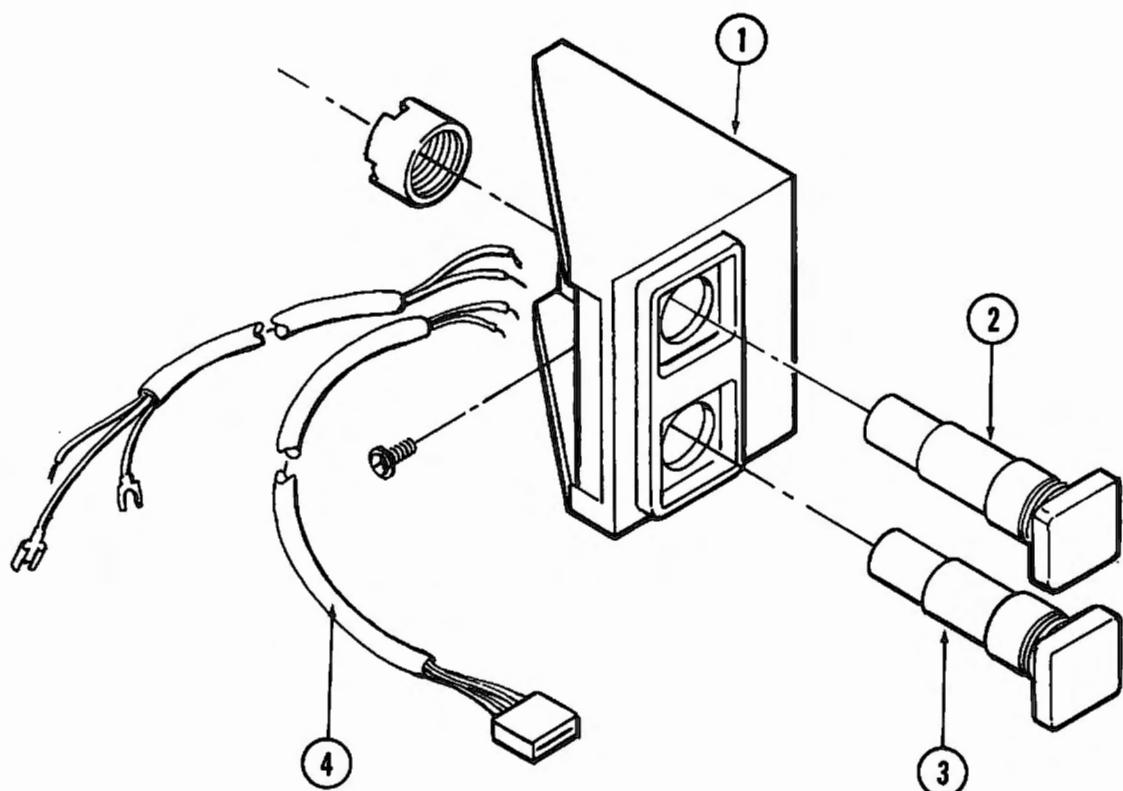
Figure 8-3.   Reset/Power ON Indicator Module

8.4 Drive Support Assembly

```
================================================================
Item Qty  Description                         Part No.
================================================================
1    1    Mount, Disk Drive                   8719252
2    1    Lens, LED                           8719294
3    1    Bezel, Drive                        8719295
4    1    Disk Drive Assembly                 8790119
5    2    Bracket, Bottom Mounting            8729151
6    4    Screw, #6-32 x 3/4" Flat Head       8569162
7    1    Shield                              8729189
8    8    Screw, #8-32 x 3/4" Hex Head        8569097
9    4    Screw, #8-32 x 1/2" Hex Head        8569078
10   2    Screw, #8-32 x 3/8" Hex Head        8569030
```
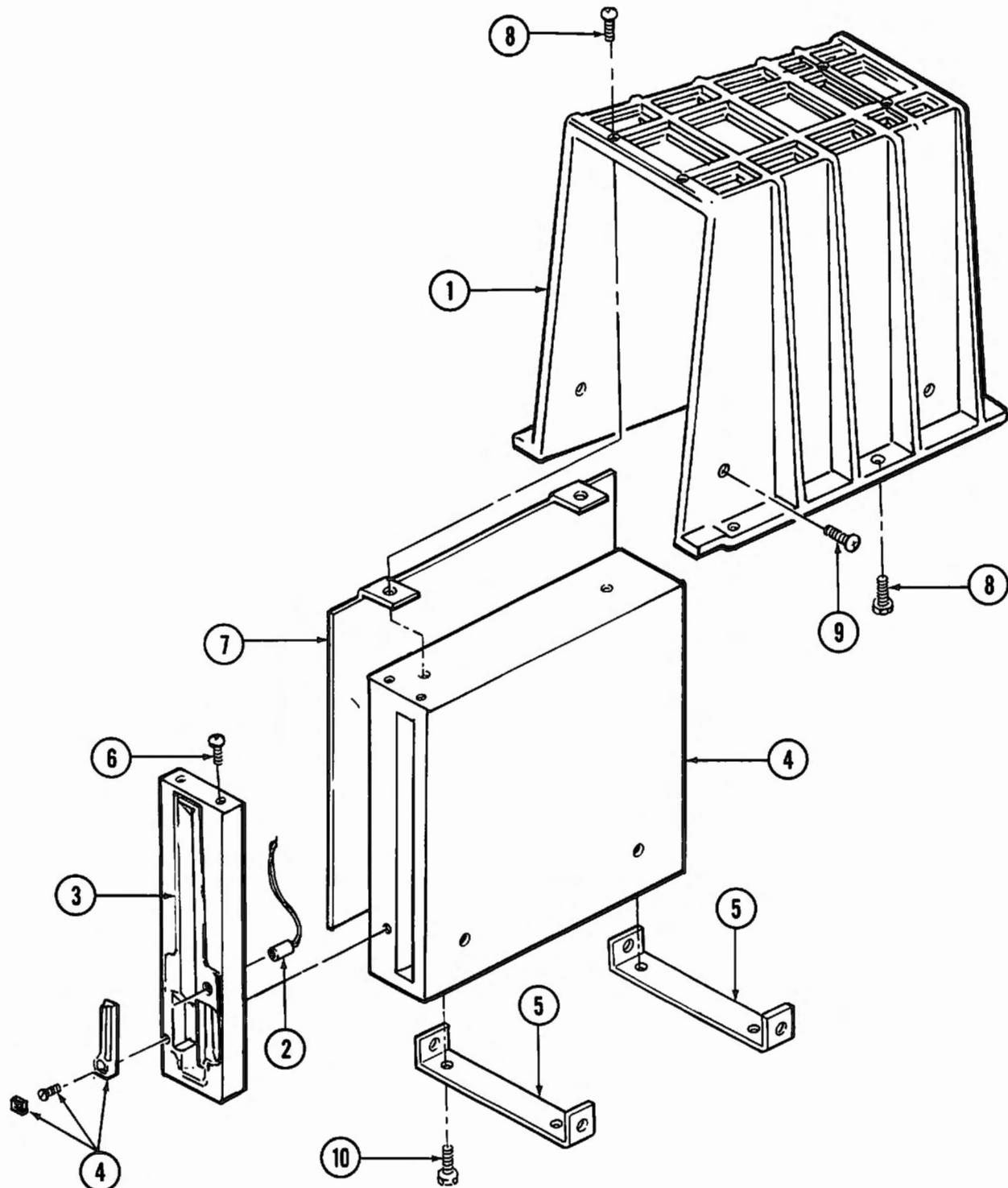
Figure 8-4.   Exploded View, Drive Support Assembly

8.5 Cover/Bezel Assembly

Item	Qty	Description	Part No.
1	1	Bezel, Front	8719251
2	1	Bezel Overlay	8719238
3	2	Clip, Tinnerman	8729107
4	1	Case, Top	8719244
5	1	CRT Assembly, (Motorola)	8790606
		CRT Assembly, (TCE)	8790607
		CRT Assembly, (RCA)	
6	4	Washer	8589055
7	4	Nut, #10-24 KEPS	8579030
8	1	Tab, .25 Faston	8529038
9	1	Cable Assembly, CRT PCB Gnd	8709383
10	1	Harness, Video	8709360
11	1	Pot, 500K (Brightness)	8262450
12	1	Pot, 500 ohm (Contrast)	8261150
13	2	Knob, Thumbwheel	8719112
14	1	Nameplate	8719257
15	3	Gasket, Fan	8719293
16	1	Shield, Video Board	8729198
17	6	Clip, Tinnerman	
18	1	Washer, #6 Star	8589029
19	1	Door, Rear	8719248
20	1	Spring, Bar	8729158
21	2	Bracket, Strain Relief	8729150
22	7	Screw, #6 x1/4" Zinc	8569077
23	2	Screw, Thumb	8569174
24	5	Screw, #8 x 1/2" Hex Head	8569163
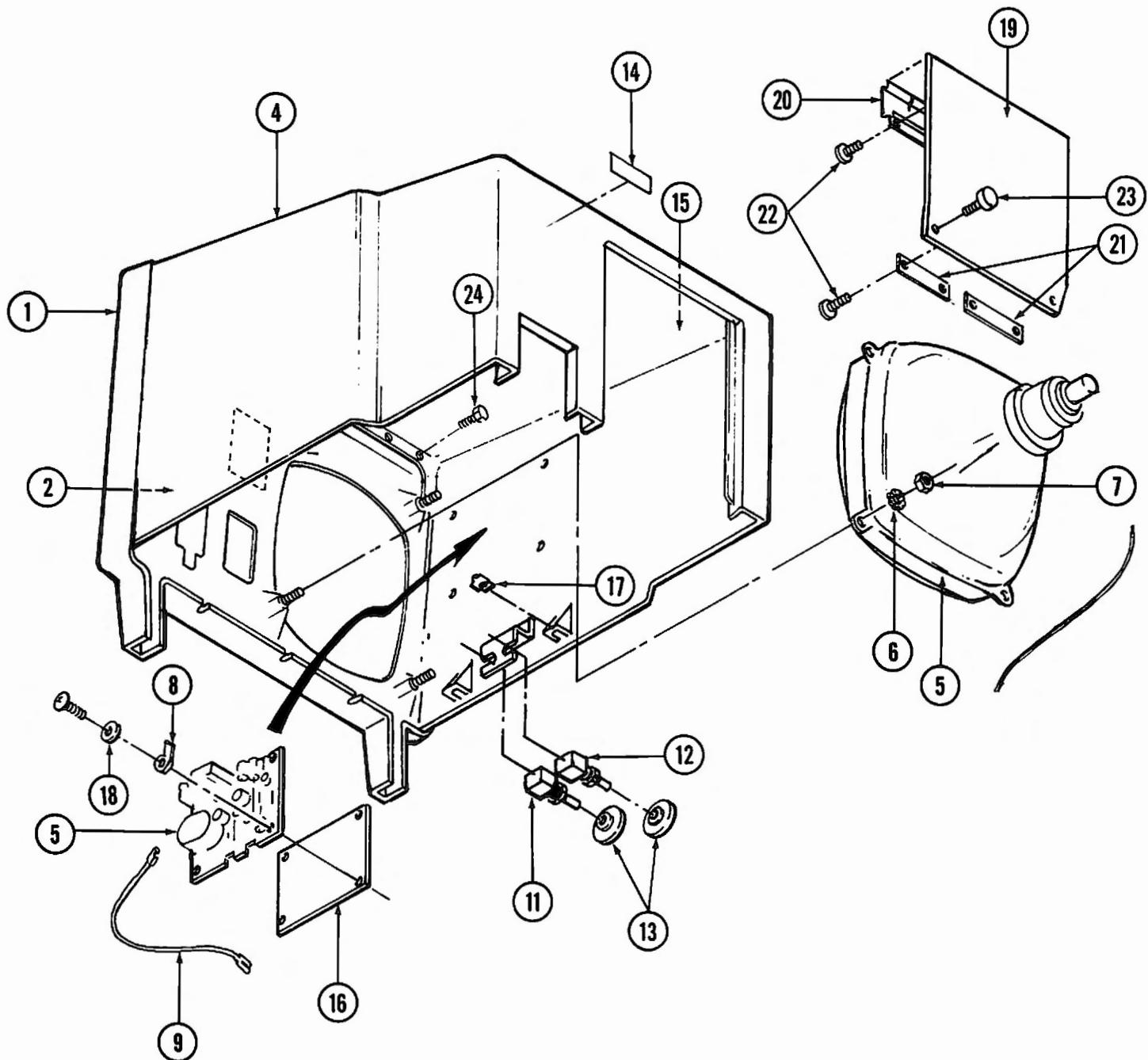
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Figure 8-5. Exploded View, Cover/Bezel Assembly

8.6 Keyboard Assembly

Item	Qty	Description	Part No.
1	1	Base, Keyboard	8719246
2	1	Bushing	8719258
3	1	Cable, Keyboard	8709396
4	1	Keyboard, Low Profile	8790522
5	1	Bezel, Keyboard	8719247
6	1	Logo, Keyboard	8719254
7	1	Cover, Keyboard	8719245
8	7	Screw, #6 x 1/2" Plastite	8569152
9	2	Feet, Bumpon	8590128
10	1	Label, Keyboard ID	8789839
11	4	Feet, Cork	8591001
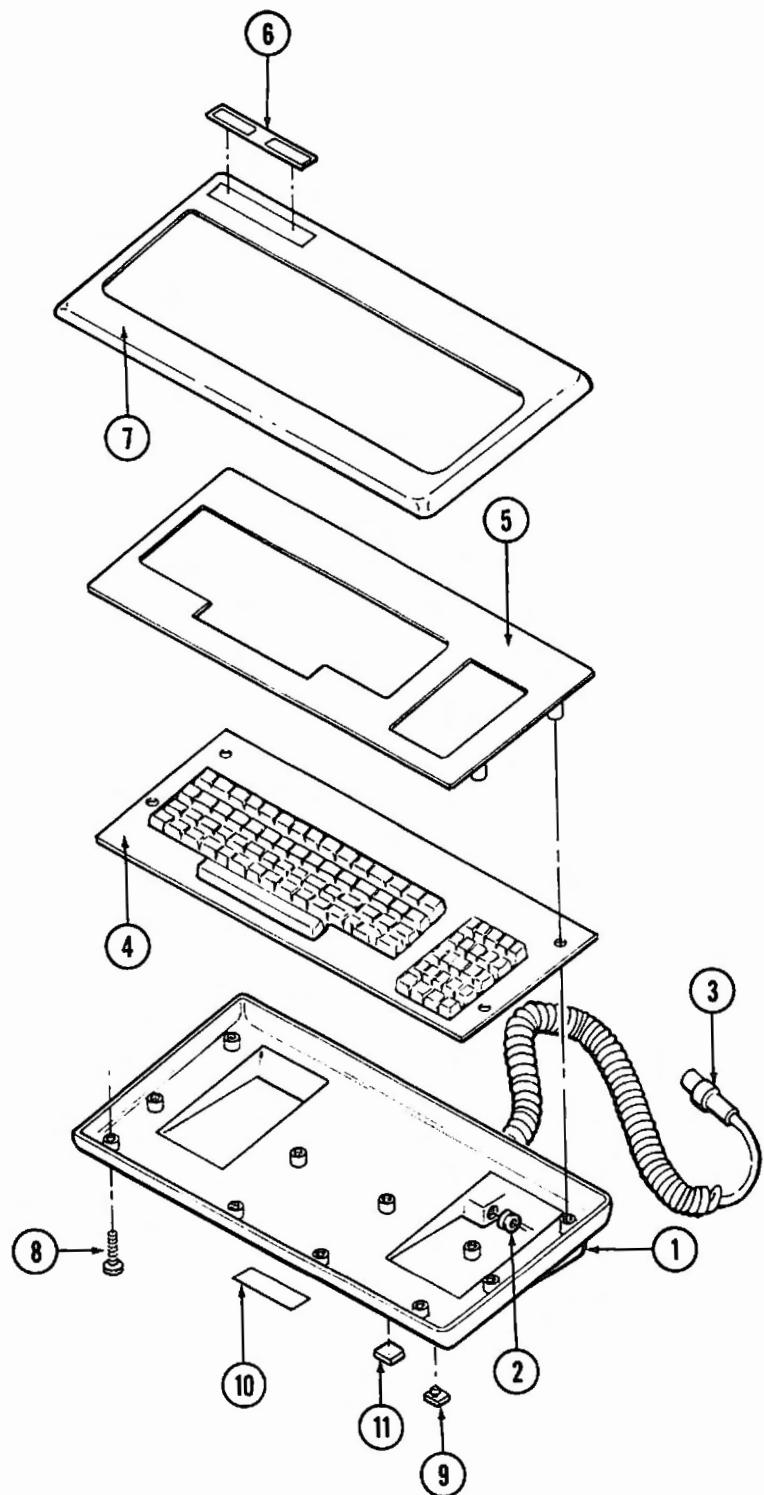
Figure 8-6. Keyboard Assembly

8.7 Hard Disk Drive Assembly

```
================================================================
Item Qty   Description                             Part No.
================================================================
  1   1    Mount, Disk Drive                       8729261
  2   1    Drive, 15 Meg Hard Disk                 8790205
  3   1    Bracket, Lower Hard Disk                8729259
  4   1    Bracket, Upper Hard Disk                8729260
  5   5    Spacer, Antivibration                   8589096
  6   1    Bar, Front Mounting                     8729263
  7   1    Bar, Rear Mounting                      8729262
  8   1    Mount, Fan                              8729285
  9   1    Fan, DC Motor                           8790407
 10   1    Power Supply, 38W                       8790025
 11   1    Cable Assembly, AC Wiring               8709486
 12   1    Cable Assembly, 20-Pin Connector        8709489
 13   1    Cable Assembly, DC Wiring               8709487
 14   1    Cable Assembly, 34-Pin Connector        8709490
 15   1    PCB Assembly, Hard Disk Controller      8898809
 16   1    Terminal Block                          8529045
 17   1    Bezel Overlay                           8719379
 18   2    Wing Clips, Bezel Overlay               8559057
 19   2    Spacer, Plastic                         8589097
 20   1    *Cover, Card Cage                       8729267
 21   1    *Panel, Card Cage Left (from rear)      8729286
 22   1    *Gasket, Foam                           8719384
 23   8    Screw, Hex Head, #8-32 x 3/8"           8569030
 24   6    Screw, Hex Head, #8-32 x 1/4"           8569036
 25   6    Screw, Pan Head, #6-32 x 1/4"           8569158
 26   6    Washer, Lock, #6                        8589018
 27   2    Nut, KEPS, Lock #8-32                   8579028
 28   5    Nut, Hex, #6-32                         8579004
      1    Cable Assembly, Ground (not shown)      8709488
      1    Label, IC U54                           8789914
      1    Label, Warning, UL                      8789090
      1    Label, Upgrade                          87891039
      1    Map, Media Error                        8759252
      1    Holder, Plastic w/adhesive              8590109
    U54    IC, 2716, Boot ROM                      8040716
      1    Label, IC, 2716, Boot ROM
```

*   These three pieces, if needed, will be found in the
Model 12 HD Seven Slot Expansion Unit (kit) Catalog Number
26-6017.
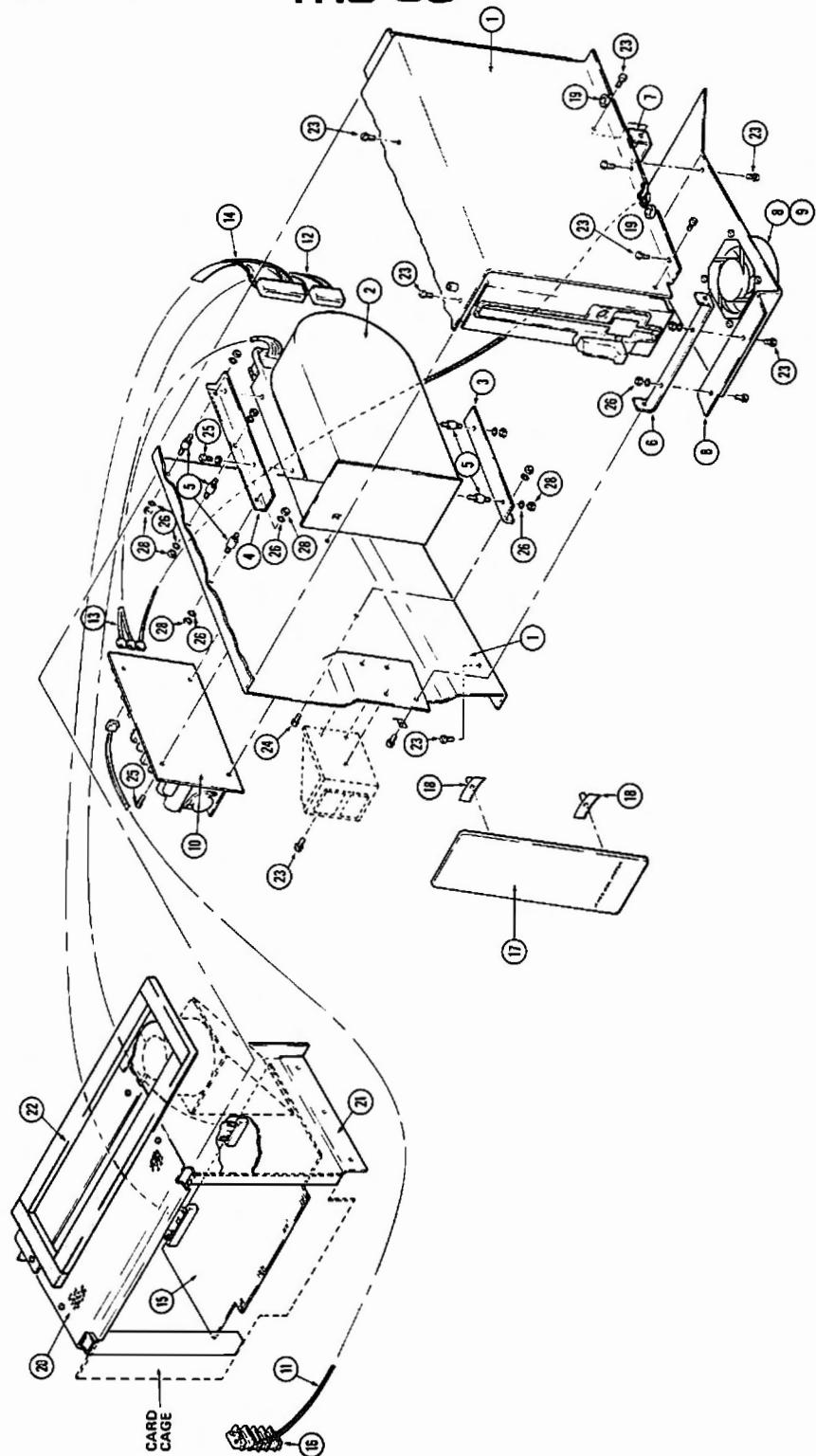
Figure 8-7. Hard Disk Drive

APPENDIX VIDEO MONITOR ASSEMBLIES

Video Monitor Assembly 87900608 (RCA)

Ref. No.	Description			Part No.
Coils				
L502	Bead Choke Assy			1479981
L504				2871650
Ferrite Beads				
FB501	Bead, Ferrite			2843117
FB502	Bead, Ferrite			2843117
FB503	Bead, Ferrite			2843117
FB504	Bead, Ferrite			2843117
FB505	Bead, Ferrite			2843117
FB506	Bead, Ferrite			2843117
FB601	Bead, Ferrite			1443391
Capacitors				
C501	Capacitor,	1000 pF,	50V	2841253
C502	Capacitor,	0.1 uF,	25V	1490938
C503	Capacitor,	0.1 uF,	25V	1490938
C504	Capacitor,	0.68 uF,	50V	2813835
C505	Capacitor,	0.01 uF,	50V	2813835
C506	Capacitor,	.0056 uF,	50V	2813835
C507	Capacitor,	1200 pF,	250V	1490135
C508	Capacitor,	100 uF,	16V	1490306
C509	Not Used			
C510	Capacitor,	2700 pF,	50V	2841254
C511	Capacitor,	4.7 uF,	35V	2841273
C512	Capacitor,	0.01 uF,	50V	2841255
C513	Not Used			
C514	Capacitor,	470 pF,	1KV	945304
C515	Capacitor,	470 pF,	1KV	945304
C516	Capacitor,	0.01 uF,	50V	2841255
C517	Capacitor,	0.01 uF,	1KV	945304
C518	Capacitor,	180 pF,	1KV	945304
C519	Capacitor,	1 uF,	350V	1490001
C520	Not Used			
C521	Capacitor,	0.01 uF,	350V	945304
C522	Not Used			
C523	Capacitor,	30 uF,	100V	984655
C524	Capacitor,	0.1 uF,	150V	2841518
C525	Capacitor,	390 pF,	500V	945802
C526	Capacitor,	56 uF,	50V	1446667

Video Monitor Assembly 87900608 (RCA)

Ref. No.	Description	Part No.
C527	Capacitor, 1000 pF, 500V	1420193
C528	Capacitor, 1000 pF, 500V	1420193
C529	Capacitor, 680 pF, 500V	1420193
C530	Capacitor, 0.01 uF, 250V	1490136
C531	Capacitor, 0.01 uF, 250V	1490136
C532	Capacitor, 470 uF, 25V	1490306
C533	Capacitor, 330 uF, 25V	1490306
C534	Capacitor, 0.1 uF, 25V	1490938
C535	Capacitor, 1 uF, 50V	2841273
C536	Capacitor, 180 pF, 250V	1490134
C537	Capacitor, 0.01 uF, 1KV	945304
C538	Capacitor, 0.47 uF, 200V	2871197
C539	Capacitor, 0.47 uF, 200V	973991
C540	Capacitor, 5600 pF,1000V	945304
C541(on yoke)	Capacitor, 33 uF	-------
C542	Not Used	
C543	Capacitor, 1000 pF, 50V	2841253
C603	Capacitor, 0.01 uF, 50V	2841255
C604	Capacitor, 0.033 uF, 50V	2813835
C605	Capacitor, 220 uF, 16V	1490306
C606	Capacitor, 220 uF, 16V	1490306
C607	Capacitor, 5600 pF, 50V	2813835
C608	Capacitor, 47 uF, 10V	2841274
C609	Capacitor, 0.1 uF, 50V	2813835
C610	Capacitor, 0.60 uF, 80V	984655
C611	Capacitor, 3300 pF, 500V	1420193
C702	Capacitor, 270 pF, 50V	2841253

Diodes

Ref. No.	Description	Part No.
CR504	Diode	1476171
CR505	Not Used	
CR506	Diode	1476171
CR507	Diode	1476171
CR508	Diode	1471872
CR509	Diode, Zener, 18V	99201
CR510	Diode, Zener, 11V	99201
CR511	Diode	1471872
CR606	Diode	1471872
CR607	Diode	1471872
CR608	Diode	1471872
CR609	Diode	1471872
CR610	Diode	1471872

Video Monitor Assembly 87900608 (RCA)
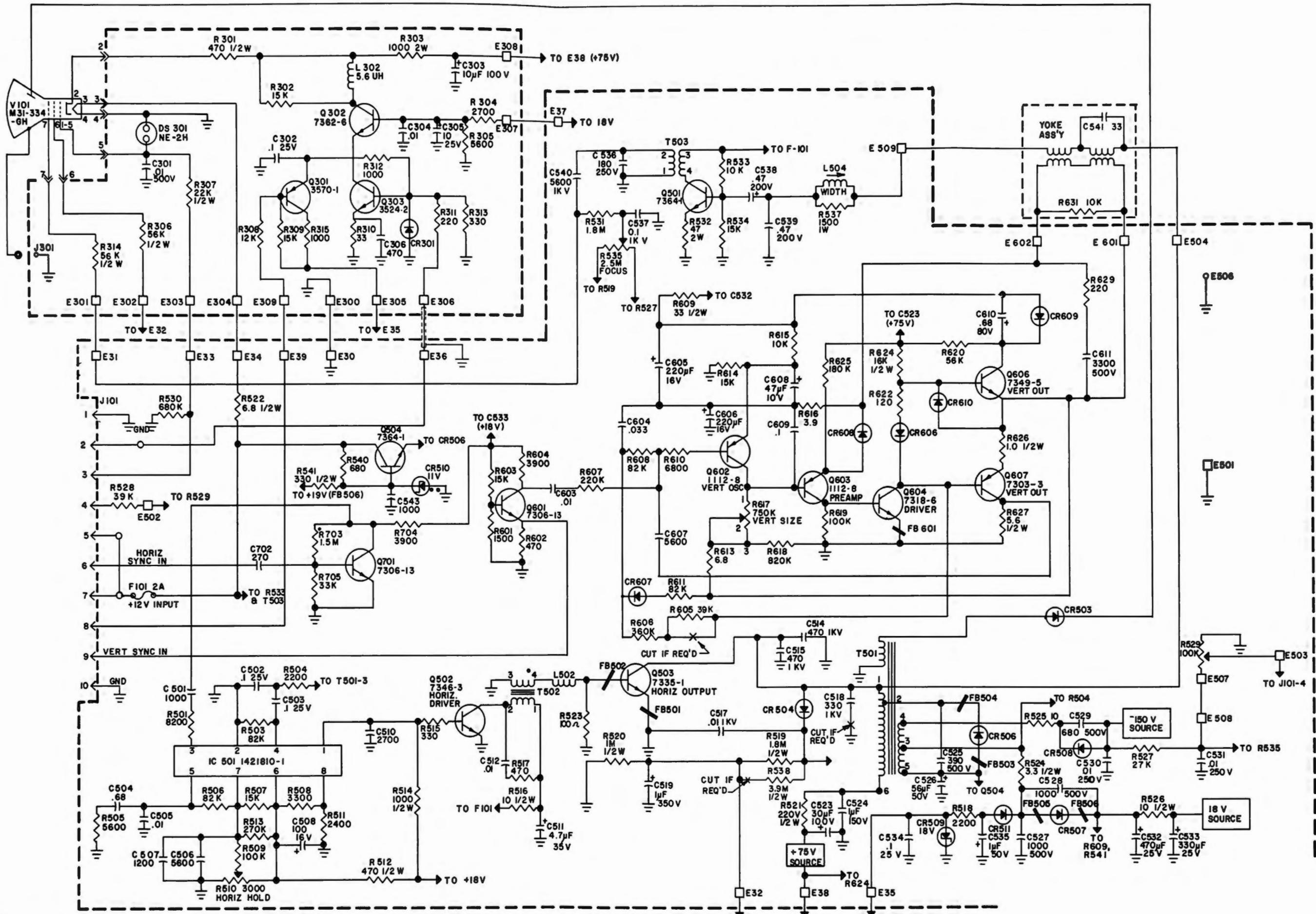
Ref. No.	Description	Part No.
Fuses		
F101	Fuse, 2A, 250V	1479891
Integrated Circuits		
IC50	IC	1421810
Resistors		
R501	Resistor, 8.2k ohms, 1/4W	993218
R502	Not Used	
R503	Resistor, 82k ohms, 1/4W	993218
R504	Resistor, 2.2k ohms, 1/4W	993218
R505	Resistor, 5.6k ohms, 1/4W	993218
R506	Resistor, 82k ohms, 1/4W	993218
R507	Resistor, 15k ohms, 1/4W	993218
R508	Resistor, 2.7k ohms, 1/4W	993218
R509	Resistor, 100k ohms, 1/4W	993218
R510	Resistor, 3k ohms, Variable	2871647
R511	Resistor, 2.4k ohms, 1/4W	993218
R512	Resistor, 470 ohms, 1/2W	993273
R513	Resistor, 270k ohms, 1/4W	993218
R514	Resistor, 1k ohms, 1/2W	993210
R515	Resistor, 330 ohms, 1/4W	993218
R516	Resistor, 10 ohms, 1/2W	993273
R517	Resistor, 470 ohms, 1/4W	993218
R518	Resistor, 2.2k ohms, 1/4W	993218
R519	Resistor, 1.8M ohms, 1/2W	993210
R520	Resistor, 2.2M ohms, 1/2W	993210
R521	Resistor, 220 ohms, 1/2W	993273
R522	Resistor, 6.8 ohms, 1/2W	993273
R523	Resistor, 18 ohms, 1/4W	993218
R524	Resistor, 3.3 ohms, 1/2W	993273
R525	Resistor, 10 ohms, 1/4W	993272
R526	Resistor, 10 ohms, 1/2W	993273
R527	Resistor, 47k ohms, 1/4W	993218
R528	Resistor, 390k ohms, 1/4W	993218
R529	Resistor, 750k ohms, Variable	1473359
R530	Resistor, 680k ohms, 1/4W	993218
R531	Resistor, 1.8M ohms, 1/4W	993218
R532	Resistor, 47 ohms, 2W	1491351
R533	Resistor, 10k ohms, 1/4W	993218
R534	Resistor, 15k ohms, CF	-------
R535	Resistor, 2.5M ohms, Variable	1473359
R537	Resistor, 1.5k ohms, 1W	1423327

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Video Monitor Assembly 87900608(RCA)

Ref. No.	Description	Part No.
R538	Not Used	
R539	Not Used	
R540	Resistor, 680 ohms, 1/4W	993218
R541	Resistor, 2.2k ohms, 1/4W	993218
R601	Resistor, 1.4k ohms, 1/4W	993218
R602	Resistor, 2.2k ohms, 1/4W	993218
R603	Resistor, 15k ohms, 1/4W	993218
R604	Resistor, 3.9k ohms, 1/4W	993218
R605	Resistor, 18k ohms, 1/4W	993218
R606	Resistor, 390k ohms, 1/4W	993218
R607	Resistor, 220k ohms, 1/4W	993218
R608	Resistor, 82k ohms, 1/4W	993218
R609	Resistor, 33 ohms, 1/2W	993273
R610	Resistor, 6.8k ohms, 1/4W	993218
R611	Resistor, 82k ohms, 1/4W	993218
R612	Not Used	
R613	Resistor, 6.8M ohms, 1/4W	993218
R614	Resistor, 15k ohms, 1/4W	993218
R615	Resistor, 10k ohms, 1/4W	993218
R616	Resistor, 3.9 ohms, 1/4W	993272
R617	Resistor, 750k ohms, Variable	1473359
R618	Resistor, 820k ohms, 1/4W	993218
R619	Resistor, 100k ohms, 1/4W	993218
R620	Resistor, 56k ohms, 1/4W	993218
R621	Not Used	
R622	Resistor, 120 ohms, 1/4W	993218
R623	Not Used	
R624	Resistor, 16k ohms, 1/2W	993210
R625	Resistor, 180k ohms, 1/4W	993218
R626	Resistor, 1.0 ohm, 1/2W	993273
R627	Resistor, 5.6 ohms, 1/2W, CFFB	-------
R628	Not Used	
R629	Resistor, 220 ohms, 1/4W	993218
R703	Resistor, 1.5M ohms, 10%, 1/4W	993218
R704	Resistor, 3.9k ohms, 1/4W	993218
R705	Resistor, 33k ohms, 1/4W	993218

Transformers

T501	Transformer, High Voltage	2830604
T502	Transformer, Horizontal Driver	1479977
T503	Transformer,	1479977
----	Transformer, Rectifier Assy.	1465974

Video Monitor Assembly 87900608 (RCA)

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=================================================================
Ref. No.          Description                      Part No.
=================================================================
```

Transistors

Ref. No.	Description	Part No.
Q501	Transistor, NPN	1417364
Q502	Transistor, NPN	1417364
Q503	Transistor, NPN	1417355
Q504	Transistor, NPN	1417364
Q601	Transistor, NPN	1417306
Q602	Transistor, PNP	1471112
Q603	Transistor, PNP	1471112
Q604	Transistor, NPN	1417318
Q605	Not Used	
Q606	Transistor, NPN	1417349
Q607	Transistor, PNP	1417303
Q701	Transistor, NPN	1417306

Mechanical Parts

Description	Part No.
Heat Sink	1491335
Heat Sink	2840062
Label, Warning	1423349
Screw, Hex HD .138(6)-.20 x .312LG	93603
Sleeving, 1.38"	2010722
Terminal Wire (.45SQ x .44LG)	938391
Terminal Bead Chain	1471828

Schematic, Monitor Chassis(RCA), 8000184

Video Monitor Assembly 8790608 (TCE)

```
================================================================
Ref. No.   Description                            Part No.
================================================================
```

Capacitors

Ref. No.	Description				Part No.
C101	Capacitor,	4.7 uF,	50V,	20%	CE04(RB)475M
C102	Capacitor,	180 pF,	50V,	10%	CK45B1H181K
C103	Capacitor,	0.1 uF,	50V,	10%	CQ92M1H104K
C104	Capacitor,	22 uF,	100V,	20%	CE04C226M
C105	Capacitor,	2200 pF,	500V,+100-0%		CK45E2H222P
C201	Capacitor,	0.022 uF,	50V,	10%	CQ92M1H223K
C202	Capacitor,	0.022 uF,	50V,	10%	CQ92M1H223K
C203	Capacitor,	0.01 uF,	50V,	10%	CQ92M1H103K
C204	Capacitor,	0.33 uF,	50V,	10%	CE04(RB)334K
C205	Capacitor,	4.7 uF,	35V,	20%	CS15E475M
C206	Capacitor,	4.7 uF,	35V,	20%	CS15E475M
C207	Capacitor,	33 uF,	16V,	20%	CE04C336M
C208	Capacitor,	33 uF,	16V,	20%	CE04C336M
C209	Capacitor,	1000 uF,	16V,	20%	CE04C108M
C210	Capacitor,	0.033 uF,	50V,	10%	CQ92M1H333K
C211	Capacitor,	220 uF,	16V,	20%	CE04C227M
C212	Capacitor,	100 uF,	16V,	20%	CE04C107M
C301	Capacitor,	220 pF,	50V,	10%	CK45B1H221K
C302	Capacitor,	0.47 uF,	50V,	10%	CE04(RB)474K
C303	Capacitor,	100 pF,	50V,	10%	CK45B1H101K
C304	Capacitor,	0.022 uF,	50V,	10%	CQ92M1H223K
C305	Capacitor,	0.018 uF,	50V,	10%	CQ92M1H183K
C306	Capacitor,	0.018 uF,	50V,	10%	CQ92M1H183K
C307	Capacitor,	4.7 uF,	50V,	20%	CE04C475M
C308	Capacitor,	0.01 uF,	50V,	10%	CQ92M1H103K
C309	Capacitor,	220 uF,	16V,	20%	CE04C227M
C310	Capacitor,	56 pF,	50V,	5%	CC45CH1H560J
C311	Capacitor,	4700 pF,	50V,	5%	CQ92P1H472J
C312	Not Used				
C313	Capacitor,	1000 uF,	25V,	20%	CE04C108M
C314	Capacitor,	0.033 uF,	400V,	5%	CQ92P2G333J
C315	Capacitor,	0.047 uF,	400V,	10%	CQ92P2G473K
C316	Capacitor,	1 uF,	250V,	20%	CE04C105M
C317	Capacitor,	0.01 uF,	630V,	10%	CQ92P2J103K
C318	Capacitor,	0.01 uF,	630V,	10%	CQ92P2J103K
C319	Capacitor,	4700 pF,1000V,+100-0%			CK45E3A472P
C320	Capacitor,	2200 pF,	500V,+100-0%		CK45E2H222P
C321	Capacitor,	2200 pF,1000V,+100-0%			CK45E3A222P
C322	Capacitor,	15 uF,	25V,	20%	CE04(RP)A01M
C323	Capacitor,	2200 pF,	500V,+100-0%		CK45E2H222P
C324	Capacitor,	2200 pF,	500V,+100-0%		CK45E2H222P

Video Monitor Assembly 8790608 (TCE)

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==================================================================
Ref. No.     Description                            Part No.
==================================================================
C401         Capacitor,   220 uF,  16V, 20%        CE04C227M

C501         Capacitor,  1000 pF,1000V,+100-0%     CK45E3A102P

Coils
L301         Coil, Linearity                       143410020A
L302         Coil, Width                           143310140A

Diodes
D101         Diode, Si 10E-1                       -----------

D201         Diode, Si 10E-1                       -----------
D202         Diode, Si VD1221                      -----------
D203         Diode, Si VD1221                      -----------

D301         Diode, Si RGP25D                      -----------
D302         Diode, Si BBT4                        -----------
D303         Diode, Si BBT4                        -----------
D304         Diode, Si BBT4                        -----------
D305         Diode, Si BBT10                       -----------
D306         Diode, Si BBT4                        -----------

Fuses
FU401        Fuse, 2A, 250V                        251000790A

Integrated Circuits
IC201        IC, AN5763, V-Process                 -----------
IC301        IC, AN5753, H-Process                 -----------

Resistors
R101         Resistor,   470 ohms, 1/4W, 5%        RD1/4MZ(S)471J
R102         Resistor,   15k ohms, 1/4W, 5%        RD1/4MZ(S)153J
R103         Resistor,    1M ohms, 1/4W, 5%        RD1/4MZ(S)105J
R104         Resistor,   220 ohms, 1/4W, 5%        RD1/4MZ(S)221J
R105         Resistor,    33 ohms, 1/4W, 5%        RD1/4MZ(S)330J
R106         Resistor,   100 ohms, 1/4W, 5%        RD1/4MZ(S)101J
R107         Resistor,   47k ohms, 1/4W, 5%        RD1/4MZ(S)473J
R108         Resistor,    1k ohms, 1/4W, 5%        RD1/4MZ(S)102J
R109         Resistor,    1k ohms, 1/4W, 5%        RD1/4MZ(S)102J
R110         Resistor,  1.5k ohm,    3W, 5%        RSM3P1152J

R201         Resistor,  4.7k ohms, 1/4W, 5%        RD1/4MZ(S)472J
R202         Resistor,  4.7k ohms, 1/4W, 5%        RD1/4MZ(S)472J
R203         Resistor,   100 ohms, 1/4W, 5%        RD1/4MZ(S)101J
R204         Resistor,   56k ohms, 1/4W, 5%        RD1/4MZ(S)563J
```
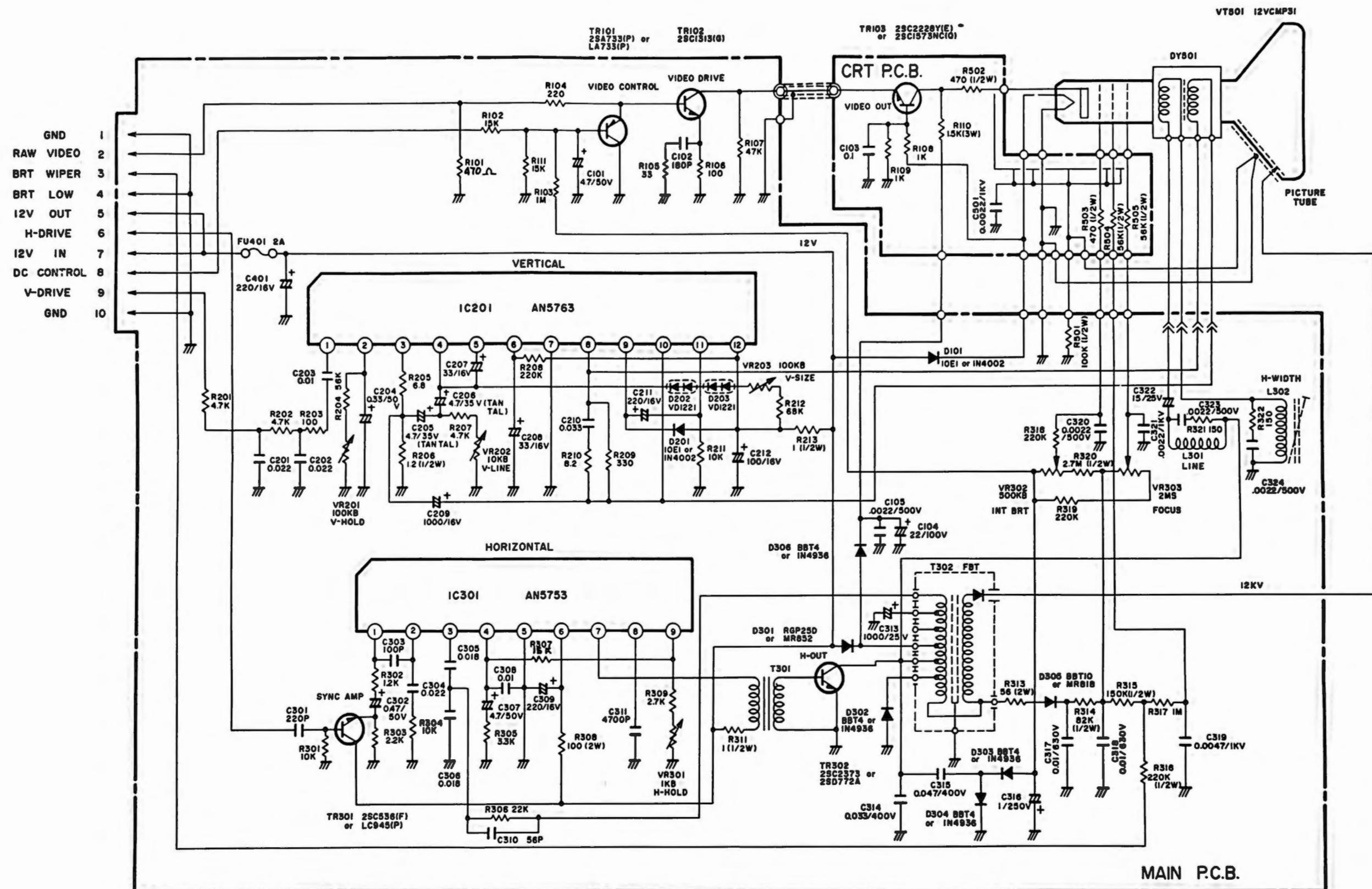
Radio Shack®

Video Monitor Assembly 8790608 (TCE)

Ref. No.	Description,	Part No.
R205	Resistor, 6.8 ohms, 1/4W, 5%	RD1/4MZ(S)6R8J
R206	Resistor, 1.2 ohms, 1/4W, 5%	RD1/4MZ(S)1R2J
R207	Resistor, 4.7k ohms, 1/4W, 5%	RD1/4MZ(S)472J
R208	Resistor, 220k ohms, 1/4W, 5%	RD1/4MZ(S)224J
R209	Resistor, 330 ohms, 1/4W, 5%	RD1/4MZ(S)331J
R210	Resistor, 8.2 ohms, 1/4W, 5%	RD1/4MZ(S)8R2J
R211	Resistor, 10k ohms, 1/4W, 5%	RD1/4MZ(S)103J
R212	Resistor, 69k ohms, 1/4W, 5%	
R213	Resistor, 1 ohm, 1/2W, 5%	RD1/2MZ(S)1R0J
R302	Resistor, 1.2k ohms, 1/4W, 5%	RD1/4MZ(S)122J
R303	Resistor, 2.2k ohms, 1/4W, 5%	RD1/4MZ(S)222J
R304	Not Used	
R305	Resistor, 3.3k ohms, 1/4W, 5%	RD1/4MZ(S)332J
R306	Resistor, 22k ohms, 1/4W, 5%	RD1/4MZ(S)223J
R307	Not Used	
R308	Resistor, 100 ohms, 2W, 5%	RSM2P 560J
R309	Resistor, 2.7k ohms, 1/4W, 5%	RD1/4MZ(S)272J
R310	Not Used	
R311	Resistor, 1 ohm, 1/2W, 5%	RD1/2MZ(S)1R0J
R313	Resistor, 56 ohms, 2W, 5%	RSM2P 560J
R314	Resistor, 82k ohms, 1/2W, 5%	RD1/2MZ(S)823J
R315	Resistor, 150k ohms, 1/2W, 5%	RD1/2MZ(S)154J
R316	Resistor, 220k ohms, 1/2W, 5%	RD1/2MZ(S)224J
R317	Resistor, 1M ohms, 1/4W, 5%	RD1/4MZ(S)105J
R318	Resistor, 220k ohms, 1/4W, 5%	RD1/4MZ(S)24J
R319	Not Used	
R320	Resistor, 2.7M ohms, 1/2W, 5%	RD1/2MZ(S)275J
R321	Resistor, 150 ohms, 1/4W, 5%	RD1/4MZ(S)151J
R322	Resistor, 150 ohms, 1/4W, 5%	RD1/4MZ(S)151J
R323	Not Used	
R324	Not Used	
R325	Not Used	
R326	Not Used	
R327	Not Used	
R328	Not Used	
R329	Resistor, 220k ohms, 1/4W, 5%	RD1/4MZ(S)24J
R501	Resistor, 100k ohms, 1/2W,10%	RC1/2GF104K
R502	Resistor, 470 ohms, 1/2W,10%	RC1/2GF471K
R503	Resistor, 470 ohms, 1/2W,10%	RC1/2GF471K
R504	Resistor, 56k ohms, 1/2W, 5%	RC1/2GF563K
R505	Resistor, 56k ohms, 1/2W, 5%	RC1/2GF563K

Video Monitor Assembly 8790608 (TCE)

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Ref. No.    Description,                          Part No.
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Variable Resistors

Ref. No.	Description	Part No.
VR201	Variable Resistor, 100k ohms	176910730A
VR202	Variable Resistor, 20k ohms	176910710A
VR203	Variable Resistor, 100k ohms	176910730A
VR301	Variable Resistor, 1k ohms	176910670A
VR302	Variable Resistor, 500k ohms	176910750A
VR303	Variable Resistor, 2M ohms	176910640A

Transformers

Ref. No.	Description	Part No.
T301	Transformers, Drive	10851001MA
T301	Transformers, Flyback	10801003YA

Transistors

Ref. No.	Description	Part No.
TR101	Transistor, PNP, 2SA733(P)	--------
TR102	Transistor, NPN, 2SC1313(G)	--------
TR103	Transistor, NPN, 2SC2228Y(E)	--------
TR301	Transistor, NPN, 2SC536(F)	--------
TR302	Transistor, NPN, 2SC2373	--------

Miscellaneous

Ref. No.	Description	Part No.
VT501	Cathode Ray Tube	559010030A
VT501	Deflection Yoke	581510020A
	Clip, Fuse	197303080A
	Connector, 4-Pin	194110780A
	Socket, 4-Pin	194010370A
	Sockey, Cylindrical	196310010A
	Spring Tension, Ground Wire	434010020A
	Wire Ground, (Code Terminal)	316010110A

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