

Carnegie Mellon University

# ADVANCED DATABASE SYSTEMS

Parallel Join Algorithms (Sorting)

@Andy\_Pavlo // 15-721 // Spring 2018

## ADMINISTRIVIA

Code Review Submission: April 11th

Project Status Meetings: April 11th

Project #3 Status Updates: April 16th



#### TODAY'S AGENDA

SIMD Background

Parallel Sort-Merge Join

Evaluation

Project #3 Code Review Guidelines



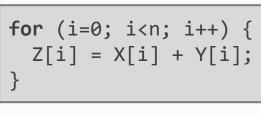
# SINGLE INSTRUCTION, MULTIPLE DATA

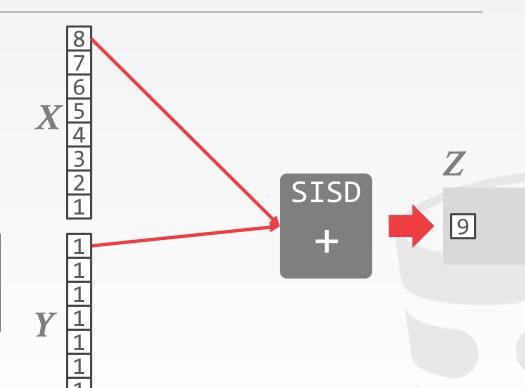
A class of CPU instructions that allow the processor to perform the same operation on multiple data points simultaneously.

Both current AMD and Intel CPUs have ISA and microarchitecture support SIMD operations.

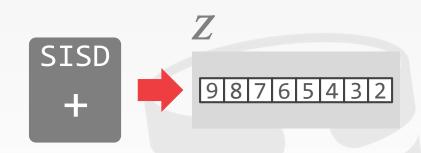
→ MMX, 3DNow!, SSE, SSE2, SSE3, SSE4, AVX

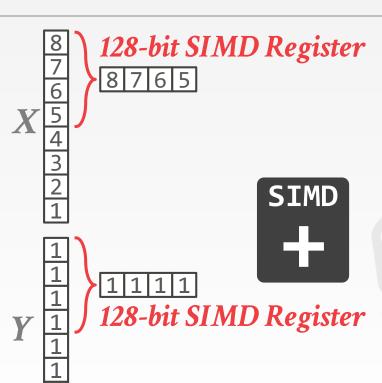














$$\begin{array}{c}
X + Y = Z \\
\begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_n \end{bmatrix} + \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_n \end{bmatrix} = \begin{bmatrix} X_1 + y_1 \\ X_2 + y_2 \\ \vdots \\ X_n + y_n \end{bmatrix} \\
X = \begin{bmatrix} X_1 \\ 5 \\ 4 \\ 3 \\ 2 \\ 1 \end{bmatrix}$$

$$\begin{array}{c}
X + Y = Z \\
X = \begin{bmatrix} X_1 \\ Y_2 \\ \vdots \\ X_n + y_n \end{bmatrix} \\
X = \begin{bmatrix} X_1 + y_1 \\ X_2 + y_2 \\ \vdots \\ X_n + y_n \end{bmatrix}$$

$$\begin{array}{c}
X = \begin{bmatrix} X_1 \\ Y_2 \\ \vdots \\ X_n + y_n \end{bmatrix} \\
Y = \begin{bmatrix} X_1 + y_1 \\ \vdots \\ X_n + y_n \end{bmatrix}$$

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#### SIMD TRADE-OFFS

#### Advantages:

→ Significant performance gains and resource utilization if an algorithm can be vectorized.

#### Disadvantages:

- → Implementing an algorithm using SIMD is still mostly a manual process.
- → SIMD may have restrictions on data alignment.
- → Gathering data into SIMD registers and scattering it to the correct locations is tricky and/or inefficient.



#### Phase #1: Sort

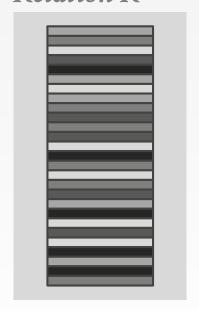
 $\rightarrow$  Sort the tuples of **R** and **S** based on the join key.

#### Phase #2: Merge

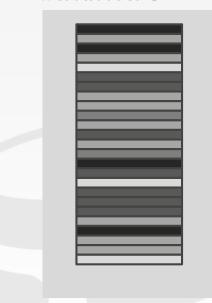
- $\rightarrow$  Scan the sorted relations and compare tuples.
- $\rightarrow$  The outer relation **R** only needs to be scanned once.



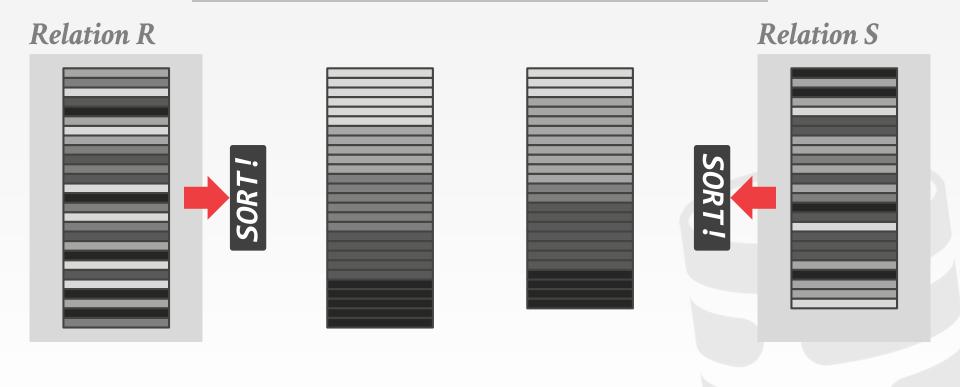
#### Relation R



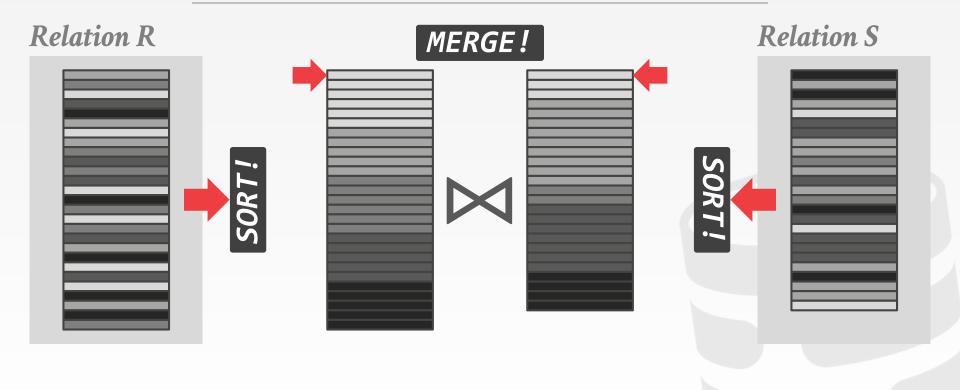
#### Relation S













#### PARALLEL SORT-MERGE JOINS

Sorting is always the most expensive part.

Use hardware correctly to speed up the join algorithm as much as possible.

- → Utilize as many CPU cores as possible.
- → Be mindful of NUMA boundaries.
- $\rightarrow$  Use SIMD instructions where applicable.



# PARALLEL SORT-MERGE JOIN (R⋈S)

#### Phase #1: Partitioning (optional)

 $\rightarrow$  Partition **R** and assign them to workers / cores.

#### Phase #2: Sort

 $\rightarrow$  Sort the tuples of **R** and **S** based on the join key.

#### Phase #3: Merge

- $\rightarrow$  Scan the sorted relations and compare tuples.
- $\rightarrow$  The outer relation R only needs to be scanned once.



#### PARTITIONING PHASE

## **Approach #1: Implicit Partitioning**

- → The data was partitioned on the join key when it was loaded into the database.
- $\rightarrow$  No extra pass over the data is needed.

### **Approach #2: Explicit Partitioning**

- → Divide only the outer relation and redistribute among the different CPU cores.
- → Can use the same radix partitioning approach we talked about last time.



#### SORT PHASE

Create <u>runs</u> of sorted chunks of tuples for both input relations.

It used to be that Quicksort was good enough.
But NUMA and parallel architectures require us to be more careful...



#### Level #1: In-Register Sorting

 $\rightarrow$  Sort runs that fit into CPU registers.

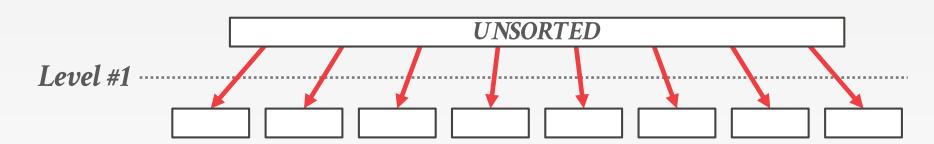
#### Level #2: In-Cache Sorting

- → Merge Level #1 output into runs that fit into CPU caches.
- → Repeat until sorted runs are ½ cache size.

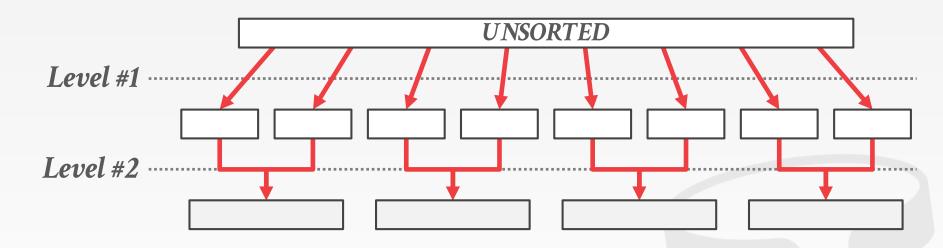
#### Level #3: Out-of-Cache Sorting

 $\rightarrow$  Used when the runs of Level #2 exceed the size of caches.

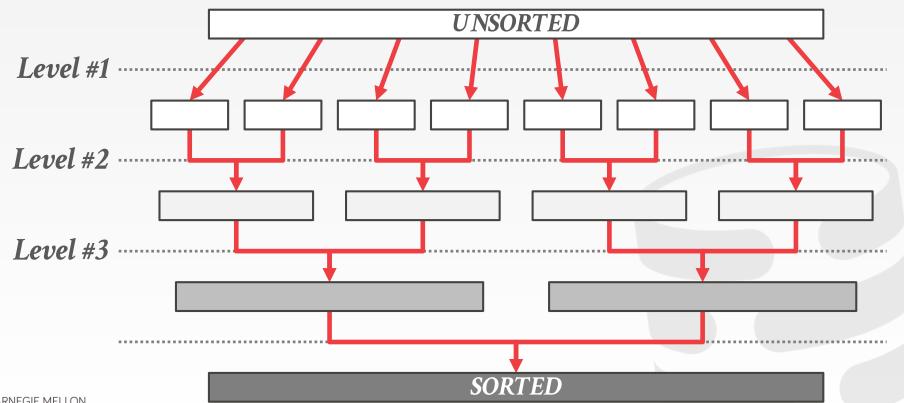






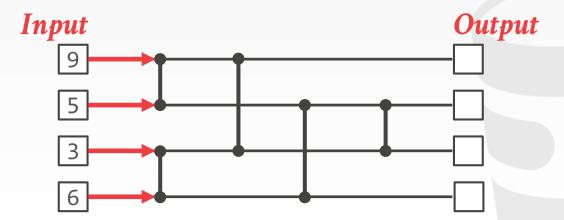






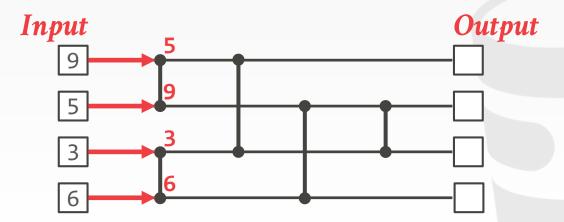


- → Always has fixed wiring "paths" for lists with the same number of elements.
- → Efficient to execute on modern CPUs because of limited data dependencies and no branches.



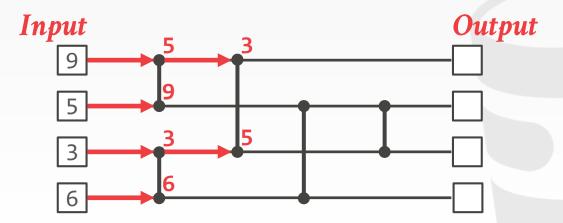


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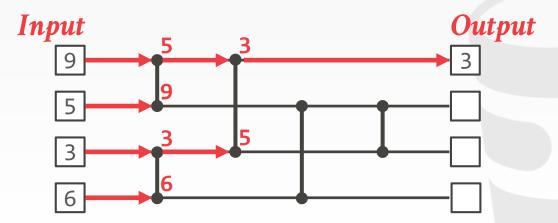


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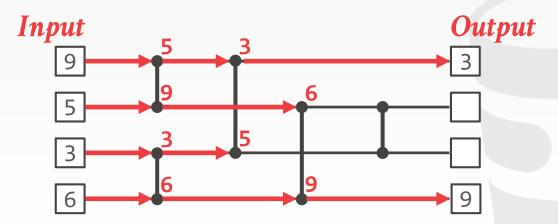


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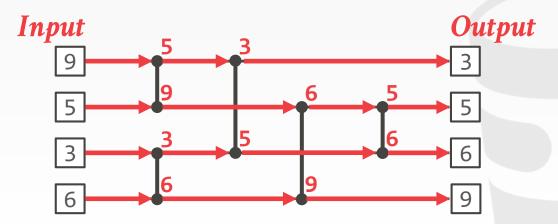


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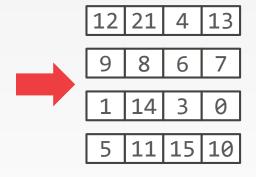




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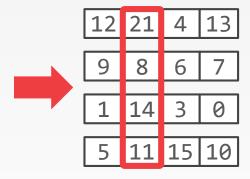


Instructions:

 $\rightarrow$  4 LOAD



#### Sort Across Registers

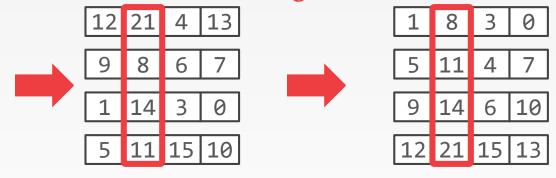


**Instructions:** 

 $\rightarrow$  4 LOAD



#### Sort Across Registers



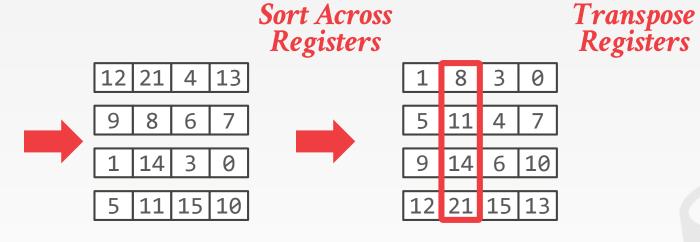
Instructions:

 $\rightarrow$  4 LOAD

Instructions:

 $\rightarrow$  10 MIN/MAX





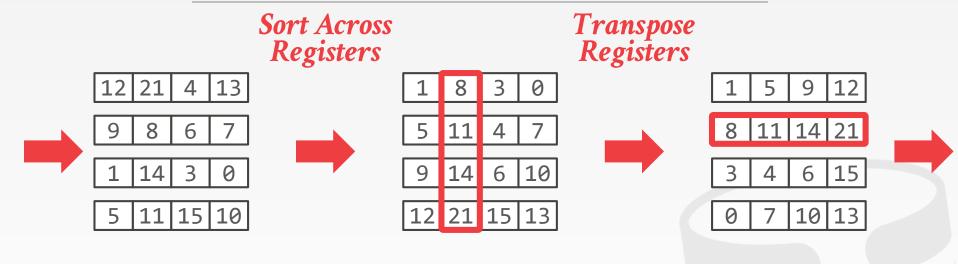
Instructions:

 $\rightarrow$  4 LOAD

Instructions:

 $\rightarrow$  10 MIN/MAX





Instructions:

 $\rightarrow$  4 LOAD

Instructions:

 $\rightarrow$  10 MIN/MAX

**Instructions:** 

→ 8 SHUFFLE

 $\rightarrow$  4 STORE



#### LEVEL #2 - BITONIC MERGE NETWORK

Like a Sorting Network but it can merge two locally-sorted lists into a globally-sorted list.

Can expand network to merge progressively larger lists (½ cache size).

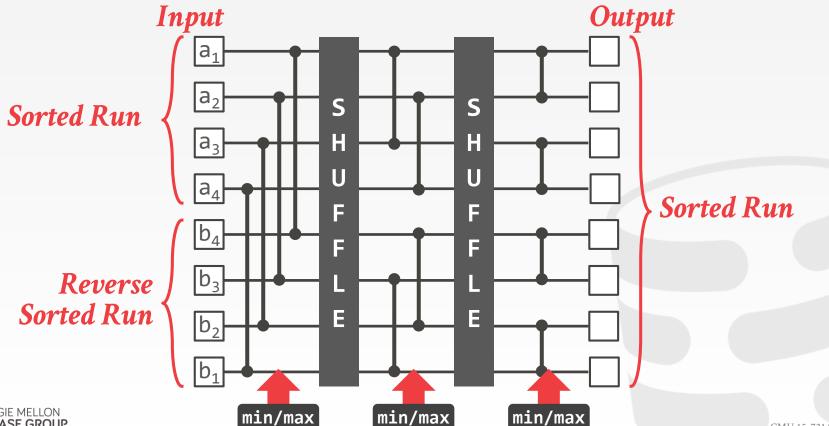
Intel's Measurements

 $\rightarrow$  2.25–3.5x speed-up over SISD implementation.



ATABASE GROUP

#### LEVEL #2 - BITONIC MERGE NETWORK



#### LEVEL #3 - MULTI-WAY MERGING

Use the Bitonic Merge Networks but split the process up into tasks.

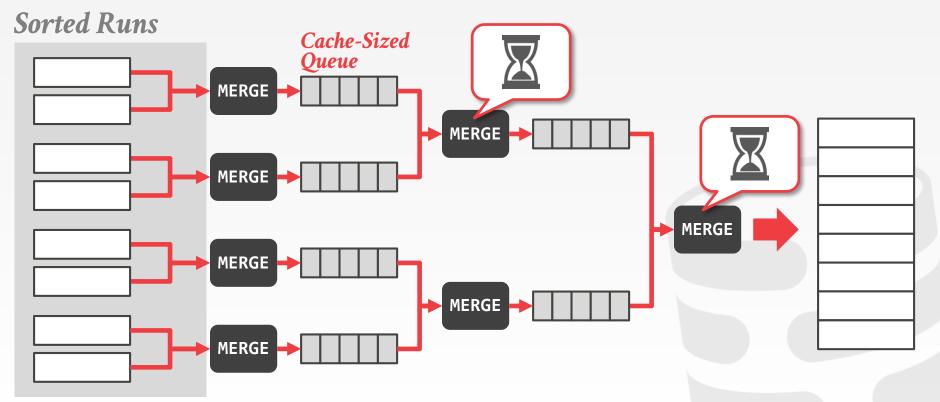
- $\rightarrow$  Still one worker thread per core.
- → Link together tasks with a cache-sized FIFO queue.

A task blocks when either its input queue is empty or its output queue is full.

Requires more CPU instructions, but brings bandwidth and compute into balance.



#### LEVEL #3 - MULTI-WAY MERGING



#### MERGE PHASE

Iterate through the outer table and inner table in lockstep and compare join keys.

May need to backtrack if there are duplicates.

Can be done in parallel at the different cores without synchronization if there are separate output buffers.



## SORT-MERGE JOIN VARIANTS

Multi-Way Sort-Merge (M-WAY)

Multi-Pass Sort-Merge (M-PASS)

Massively Parallel Sort-Merge (MPSM)



#### **Outer Table**

- $\rightarrow$  Each core sorts in parallel on local data (levels #1/#2).
- → Redistribute sorted runs across cores using the **multi- way merge** (level #3).

#### Inner Table

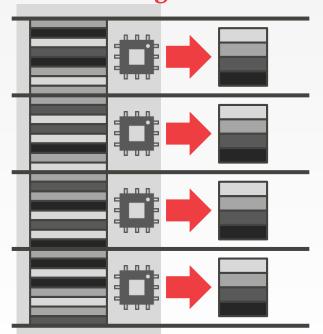
 $\rightarrow$  Same as outer table.

Merge phase is between matching pairs of chunks of outer/inner tables at each core.

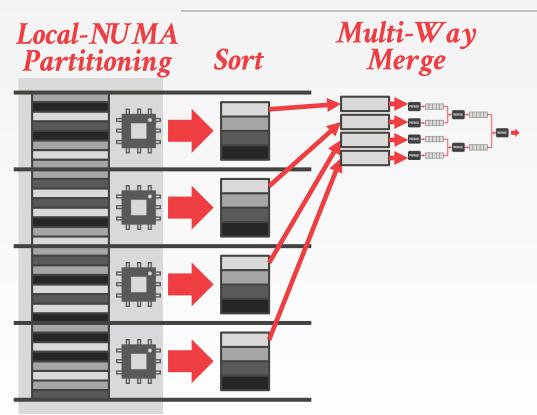


#### Local-NUMA Partitioning

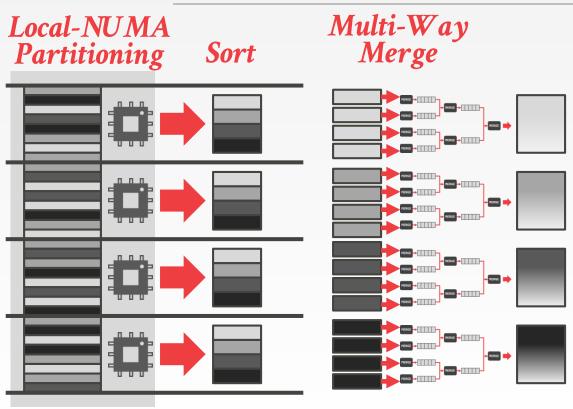
#### Sort



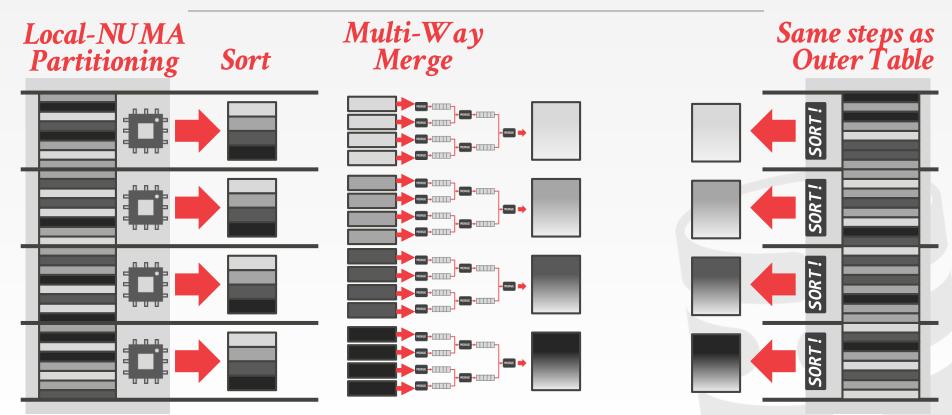




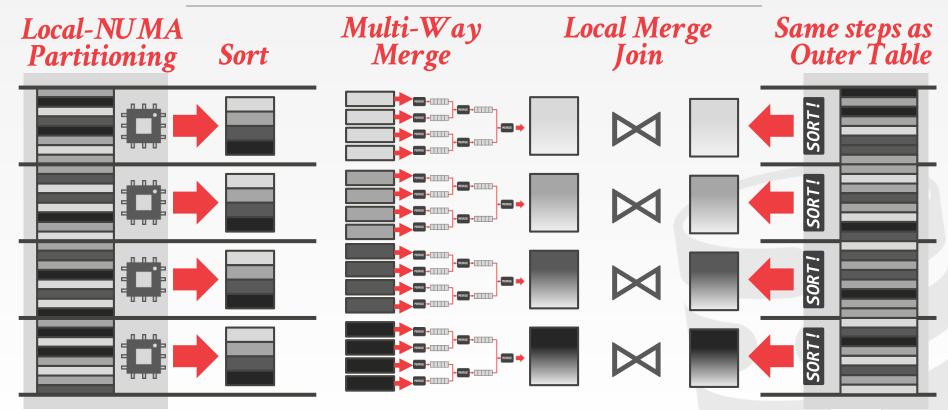




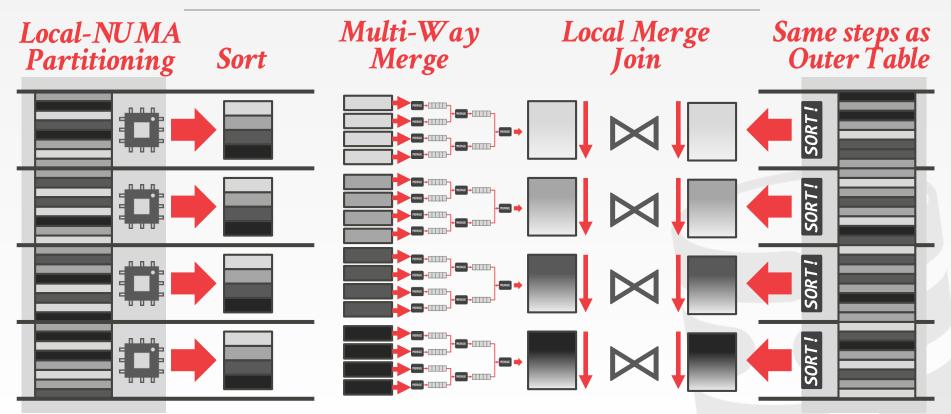














## MULTI-PASS SORT-MERGE

#### **Outer Table**

- $\rightarrow$  Same level #1/#2 sorting as Multi-Way.
- → But instead of redistributing, it uses a <u>multi-pass naïve</u> merge on sorted runs.

#### Inner Table

 $\rightarrow$  Same as outer table.

Merge phase is between matching pairs of chunks of outer table and inner table.



#### **Outer Table**

- → Range-partition outer table and redistribute to cores.
- $\rightarrow$  Each core sorts in parallel on their partitions.

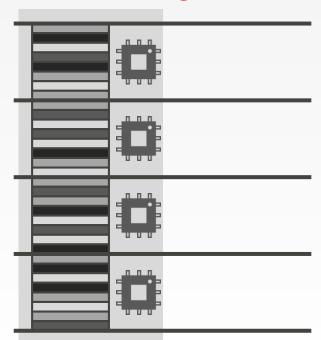
#### Inner Table

- → Not redistributed like outer table.
- $\rightarrow$  Each core sorts its local data.

Merge phase is between entire sorted run of outer table and a segment of inner table.

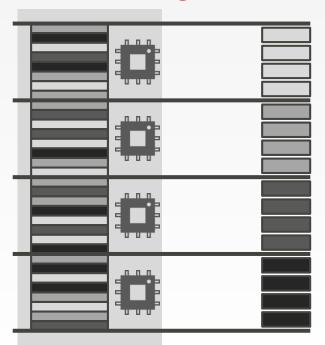


## Cross-NUMA Partitioning

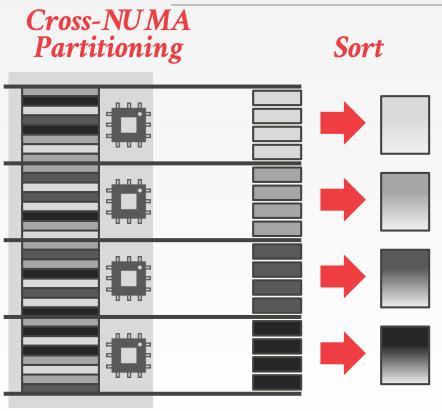




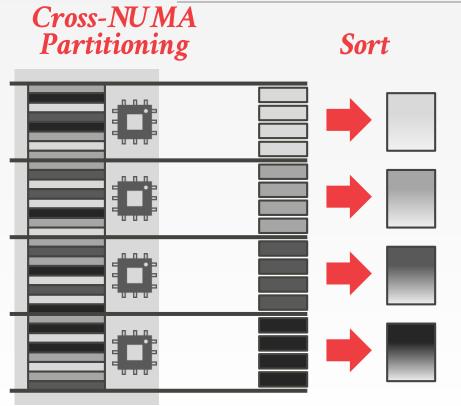
## Cross-NUMA Partitioning

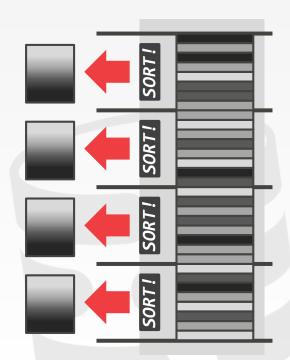




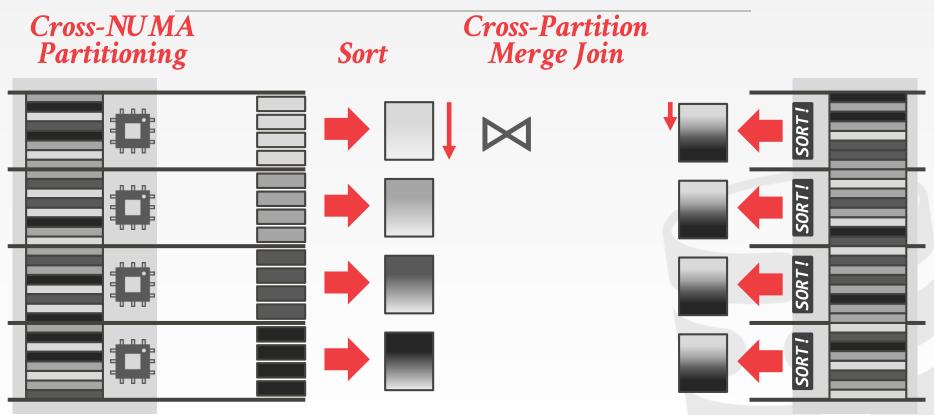




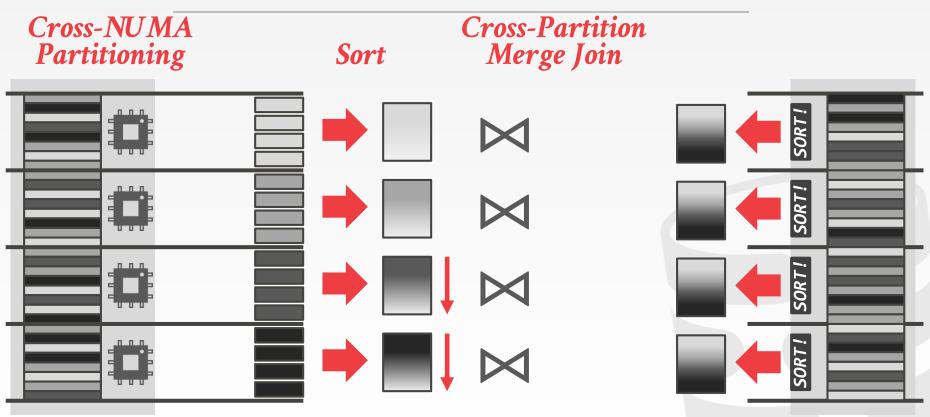














#### HYPER'S RULES FOR PARALLELIZATION

# Rule #1: No random writes to non-local memory

→ Chunk the data, redistribute, and then each core sorts/works on local data.

# Rule #2: Only perform sequential reads on non-local memory

→ This allows the hardware prefetcher to hide remote access latency.

#### Rule #3: No core should ever wait for another

→ Avoid fine-grained latching or sync barriers.



## EVALUATION

Compare the different join algorithms using a synthetic data set.

- → **Sort-Merge:** M-WAY, M-PASS, MPSM
- → **Hash:** Radix Partitioning

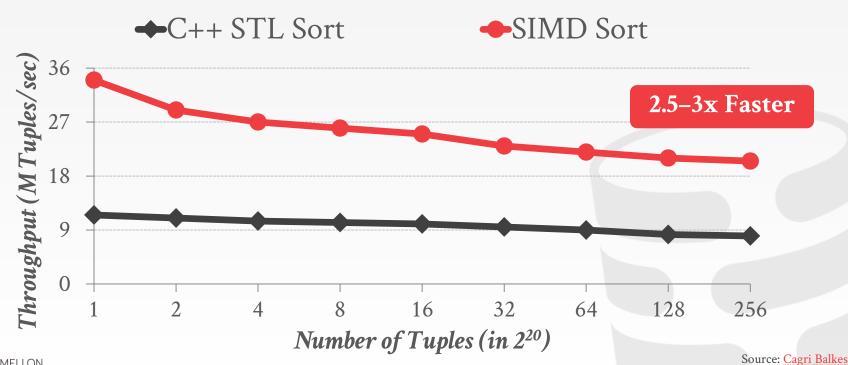
#### Hardware:

- → 4 Socket Intel Xeon E4640 @ 2.4GHz
- → 8 Cores with 2 Threads Per Core
- $\rightarrow$  512 GB of DRAM



#### RAW SORTING PERFORMANCE

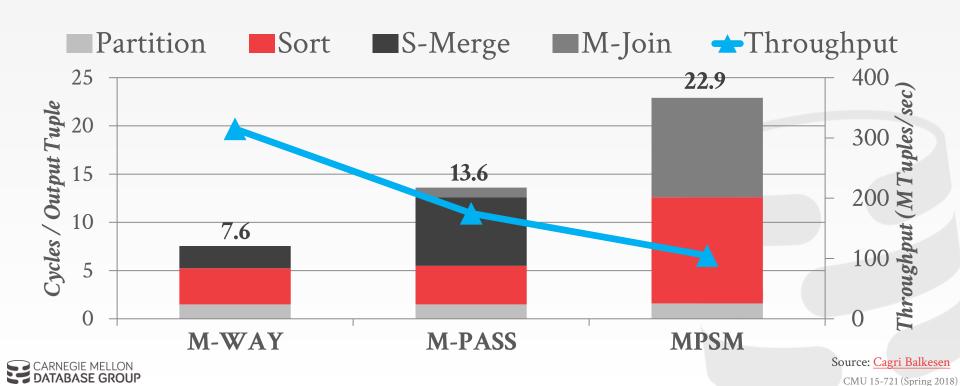
#### Single-threaded sorting performance





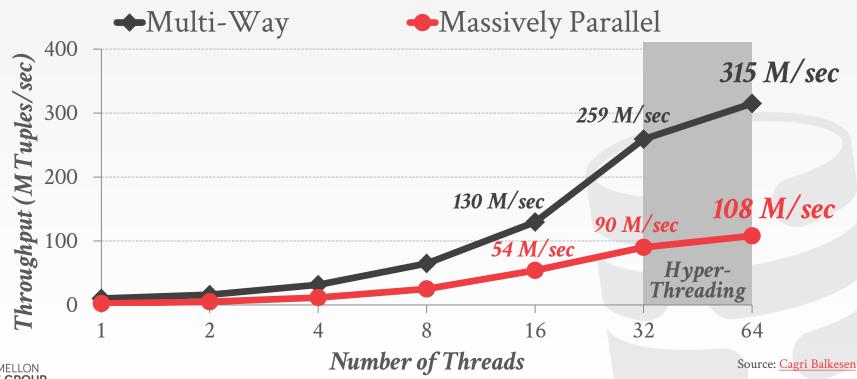
#### COMPARISON OF SORT-MERGE JOINS

#### Workload: $1.6B \bowtie 128M$ (8-byte tuples)



## M-WAY JOIN VS. MPSM JOIN

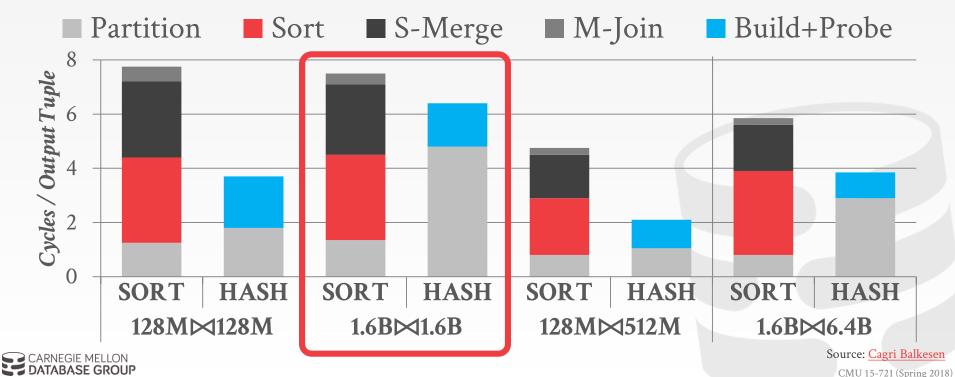
#### Workload: $1.6B \bowtie 128M$ (8-byte tuples)





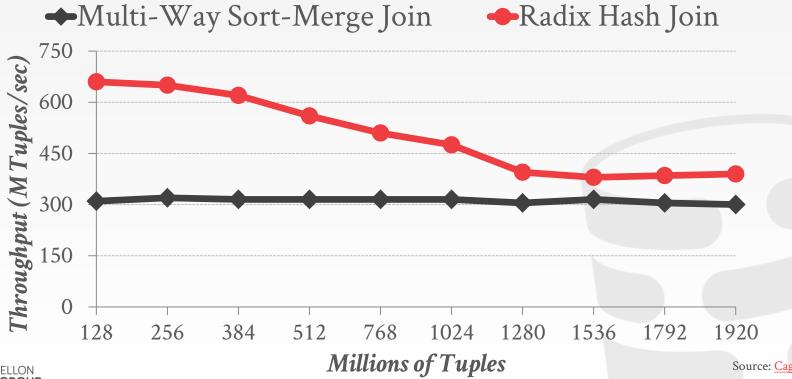
## SORT-MERGE JOIN VS. HASH JOIN

4 Socket Intel Xeon E4640 @ 2.4GHz 8 Cores with 2 Threads Per Core



## SORT-MERGE JOIN VS. HASH JOIN

#### Varying the size of the input relations





#### PARTING THOUGHTS

Both join approaches are equally important. Every serious OLAP DBMS supports both.

We did not consider the impact of queries where the output needs to be sorted.



#### CODE REVIEWS

Each group will send a pull request to the CMU-DB master branch.

- $\rightarrow$  This will automatically run tests + coverage calculation.
- → PR must be able to merge cleanly into master branch.
- → Reviewing group will write comments on that request.
- → Add the URL to the Google spreadsheet and notify the reviewing team that it is ready.

Please be helpful and courteous.



#### GENERAL TIPS

The dev team should provide you with a summary of what files/functions the reviewing team should look at.

Review fewer than 400 lines of code at a time and only for at most 60 minutes.

Use a **checklist** to outline what kind of problems you are looking for.



## CHECKLIST - GENERAL

Does the code work?

Is all the code easily understood?

Is there any redundant or duplicate code?

Is the code as modular as possible?

Can any global variables be replaced?

Is there any commented out code?

Is it using proper debug log functions?



## CHECKLIST - DOCUMENTATION

Do comments describe the intent of the code?

Are all functions commented?

Is any unusual behavior described?

Is the use of 3rd-party libraries documented?

Is there any incomplete code?



## CHECKLIST - TESTING

Do tests exist and are they comprehensive?
Are the tests actually testing the feature?
Are they relying on hardcoded answers?
What is the code coverage?



## NEXT CLASS

No lecture on Wednesday April 11<sup>th</sup>.

Reminder: First Code Review

April 11<sup>th</sup> @ 11:59pm

