Time				
			100 sec	
clk				
rstn				
vector_instruction[31:0]	xxxxxxxx		02A28A57	
rs1[4:0]	xx	00	05	
rs2[4:0]	xx	00	0A	
rd[4:0]	xx	00	14	
ALU_op_from_decoder[2:0]	xxx	000		
address_s1_from_decoder[4:0]	xx	00	05	
address_s2_from_decoder[4:0]	xx	00	0A	
address_destination_from_decoder[4:0]	xx	00	14	
vsew[2:0]	xxx	000		
is_alu_op				
is_load_store_op				
is_vlen_op				