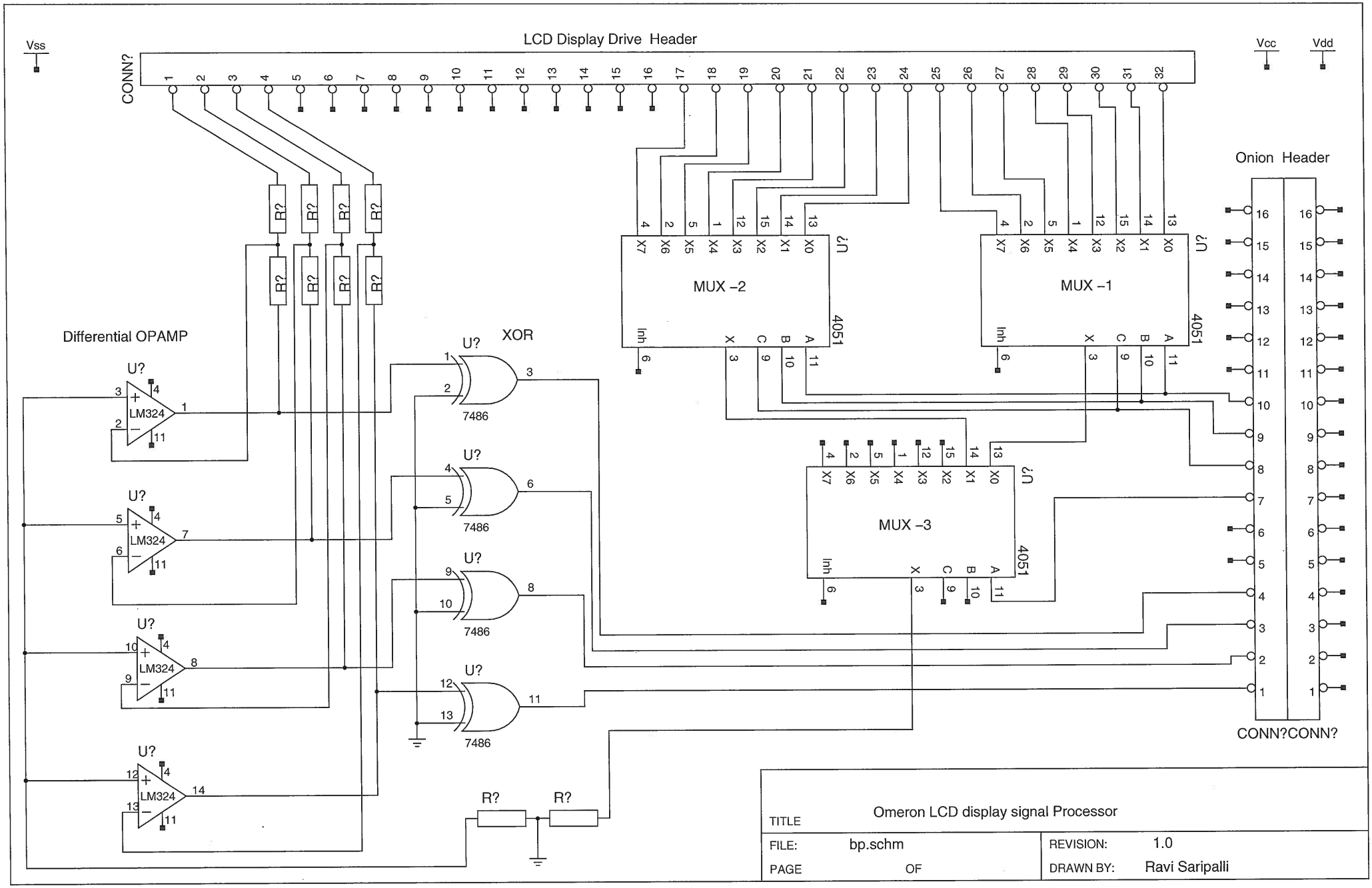

LCD Display Drive Header
CONN?
Vss
Vcc
Vdd
Onion Header
MUX –2
MUX –1
MUX –3
4051
Differential OPAMP
LM324
XOR
7486
R?
U?
CONN?CONN?
TITLE
Omeron LCD display signal Processor
FILE:
bp.schm
PAGE
OF
REVISION:
1.0
DRAWN BY:
Ravi Saripalli

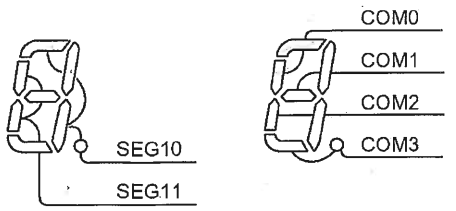


Figure 15-5 Example of COM, SEG Pin Connection (1/4 duty)

Table 15-5 Example of Display Data (1/4 duty)

No.	Display	Display data	No.	Display	Display data
0		11011111	5		10110101
1		00000110	6		11110101
2		11100011	7		00000111
3		10100111	8		11110111
4		00110110	9		10110111

Example (2) Table 15-6 shows an example of display data which are displayed using 1/2 duty LCD in the same way as Table 15-5. The connection between pins COM and SEG are the same as shown in Figure 15-6.

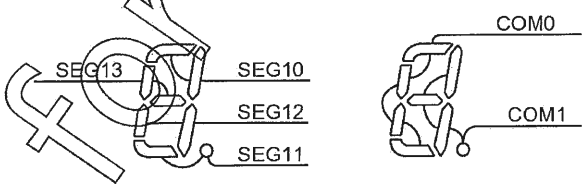
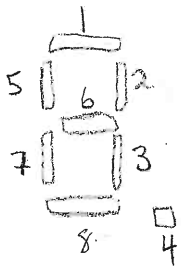


Figure 15-6 Example of COM, SEG Pin Connection



Check 5 ... 10110101 ✓
Check 1 ... 00000110 ✓

8 7 6 5 (4) 3 2 1 ✓
Decimal

National Semiconductor

February 1988

CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

General Description

The EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

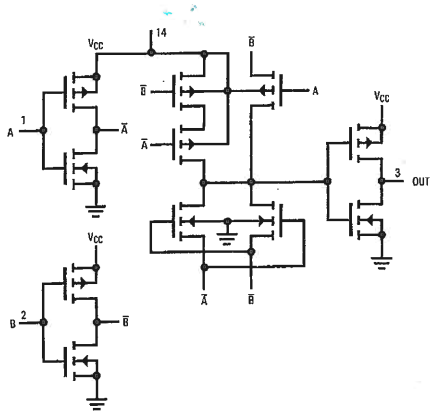
Features

■ Wide supply voltage range	3.0V to 15V
■ Low power	100 nW (typ.)
■ Medium speed operation	$t_{PHL} = t_{PLH} = 40$ ns (typ.) at $C_L = 15$ pF, 10V supply
■ High noise immunity	0.45 V_{CC} (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

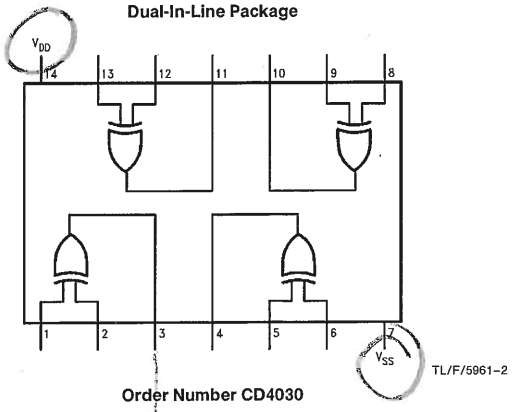
Schematic Diagram



TL/F/5961–1

Connection Diagram

Dual-In-Line Package



TL/F/5961–2

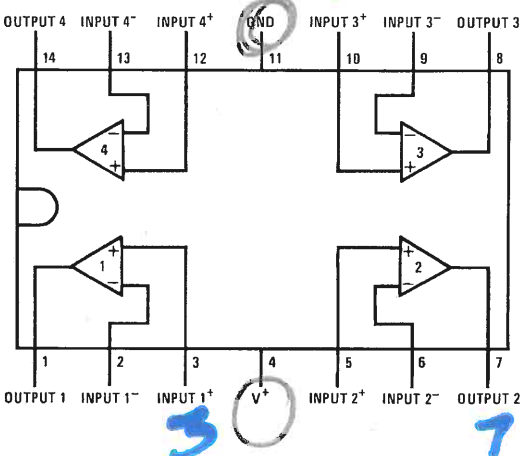
Order Number CD4030

RRD-B30M105/Printed in U. S. A.

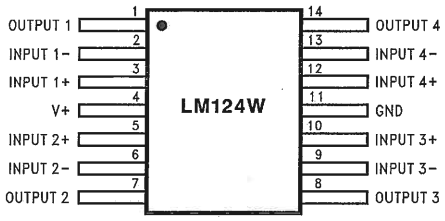
output 3, 4, 10, 11

5 Pin Configuration and Functions

J Package
14-Pin CDIP
Top View



D Package
14-Pin SOIC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUTPUT1	1	O	Output, Channel 1
INPUT1-	2	I	Inverting Input, Channel 1
INPUT1+	3	I	Noninverting Input, Channel 1
V+	4	P	Positive Supply Voltage
INPUT2+	5	I	Nonnverting Input, Channel 2
INPUT2-	6	I	Inverting Input, Channel 2
OUTPUT2	7	O	Output, Channel 2
OUTPUT3	8	O	Output, Channel 3
INPUT3-	9	I	Inverting Input, Channel 3
INPUT3+	10	I	Noninverting Input, Channel 3
GND	11	P	Ground or Negative Supply Voltage
INPUT4+	12	I	Noninverting Input, Channel 4
INPUT4-	13	I	Inverting Input, Channel 4
OUTPUT4	14	O	Output, Channel 4

MUX 74 (2) SN 74HC151N
MUX 138 (1) SN 74HC138N

SN54HC151, SN74HC151
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS110C – DECEMBER 1982 – MAY 1997

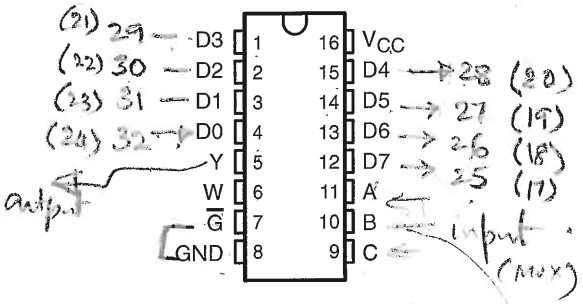
- **8-Line to 1-Line Multiplexers Can Perform as:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

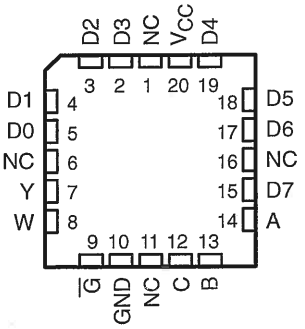
These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe ($\overline{G}$) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

The SN54HC151 is characterized for operation over the full military temperature range of –55°C to125°C. The SN74HC151 is characterized for operation from –40°C to 85°C.

SN54HC151 . . . J OR W PACKAGE
SN74HC151 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC151 . . . FK PACKAGE
(TOP VIEW)



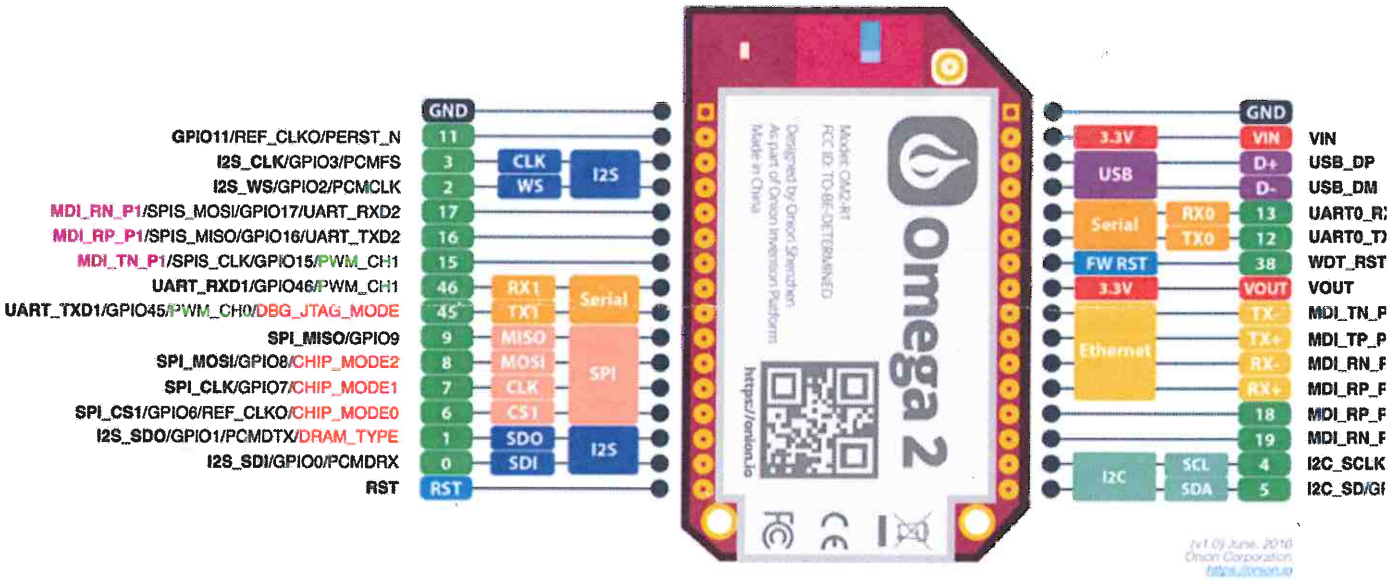
NC – No internal connection

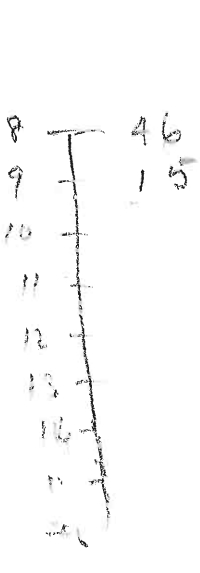
FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE $\overline{G}$	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1 . . . D7 = the level of the respective D input

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265


GND
GPIO11/REF_CLKO/PERST_N
I2S_CLK/GPIO3/PCMFS
I2S_WS/GPIO2/PCMCLK
MDI_RN_P1/SPIS_MOSI/GPIO17/UART_RXD2
MDI_RP_P1/SPIS_MISO/GPIO16/UART_TXD2
MDI_TN_P1/SPIS_CLK/GPIO15/PWM_CH1
UART_RXD1/GPIO46/PWM_CH1
UART_TXD1/GPIO45/PWM_CH0/DBG_JTAG_MODE
SPI_MISO/GPIO9
SPI_MOSI/GPIO8/CHIP_MODE2
SPI_CLK/GPIO7/CHIP_MODE1
SPI_CS1/GPIO6/REF_CLKO/CHIP_MODE0
I2S_SDO/GPIO1/PCMDTX/DRAM_TYPE
I2S_SDI/GPIO0/PCMDRX
RST
CLK
WS
I2S
RX1
TX1
Serial
MISO
MOSI
CLK
CS1
SPI
SDO
SDI
I2S
Omega 2
3.3V
USB
Serial
FW RST
3.3V
Ethernet
I2C
RX0
TX0
SCL
SDA
VIN
D+
D-
VOUT
TX-
TX+
RX-
RX+
VIN
USB_DP
USB_DM
WDT_RST
VOUT
I2C_SCLK
PWM outputs




RST
MUX