




















Mini DP Source connector			Mini DP to Mini DP Cable assembly			Mini DP Sink connector		
Signal Type	Pin Name	Pin	Plug Pin		Plug Pin	Pin	Pin Name	Signal Type
GND	GND	1	1		8	8	GND	GND
Out	ML_Lane 0 (p)	3	3		12	12	ML_Lane 0 (p)	In
Out	ML_Lane 0 (n)	5	5		10	10	ML_Lane 0 (n)	In
GND	GND	7	7		13	13	GND	GND
Out	ML_Lane 1 (p)	9	9		17	17	ML_Lane 1 (p)	In
Out	ML_Lane 1 (n)	11	11		15	15	ML_Lane 1 (n)	In
GND	GND	13	13		7	7	GND	GND
Out	ML_Lane 2 (p)	15	15		11	11	ML_Lane 2 (p)	In
Out	ML_Lane 2 (n)	17	17		9	9	ML_Lane 2 (n)	In
GND	GND	19	19		19	19	GND	GND
In	Hot Plug Detect	2	2		2	2	Hot Plug Detect	Out
CFG	CONFIG1	4	4		4	4	CONFIG1	CFG
CFG	CONFIG2	6	6		6	6	CONFIG2	CFG
GND	GND	8	8		1	1	GND	GND
Out	ML_Lane 3 (p)	10	10		5	5	ML_Lane 3 (p)	In
Out	ML_Lane 3 (n)	12	12		3	3	ML_Lane 3 (n)	In
GND	GND	14	14		14	14	GND	GND
I/O	AUX_CH (p)	16	16		16	16	AUX_CH (p)	I/O
I/O	AUX_CH (n)	18	18		18	18	AUX_CH (n)	I/O
PWR Out	DP_PWR	20	20	(no connection)	20	20	DP_PWR	PWR Out

Title		
Size A4	Number	Revision
Date:	5.30.2024	Sheet 1 of 1
File:	D:\PCB\...\M2male_M2female_miniDP_SchDown By: CME	



open source
hardware



29.05.2024

M.2 PCIe x2 to miniDP and M.2 female

J1

PERSTF
CKRQF
WAKEF

CLK_P

CLK_N

PERST2

WAKE2

J3

J2

M.2 M KEY

github.com/rick-heig/nvme_csd

HH
GHI
REDS_D

