---------- Forwarded message ----------
From: pppaaarrriiitttyyy@lycos.com
Date: Aug 26, 2013
Subject: shift register noise sources
To: riphers@gmail.com

Hello!

The computer runs for moments at a time. Makes assembling and posting an email a bit of a race.

I'll be able to look tomorrow, Monday, for the files.

There is a thing called the shift-register noise source.
It is a shift-register with some bits exclusive-or'ed together and fed-back to make the input.
A string of ones and zeros lies within a strand of flip-flops. At the clock-edge,
they all move to the next step along the strand.
The new bits comming in are made by exclusive-oring some of the other bits already in play.

Everyone is generally concerned with the maximal length sequence: how to get the longest run of "shhhhhhhhh" before it repeats. When it repeates, you can hear it.

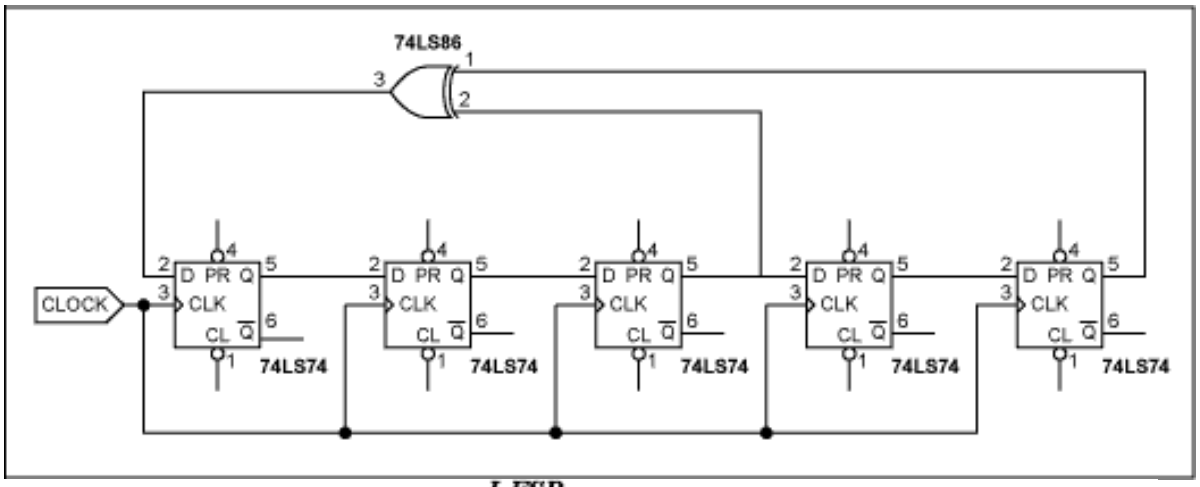
The 19-bit generator in the attachment ought to be pretty good. It must be started with something in it, not "0". It will hit every number that can be represented with 19 bits. The repeats won't become obnoxious untill the clock frequency is raised really high.

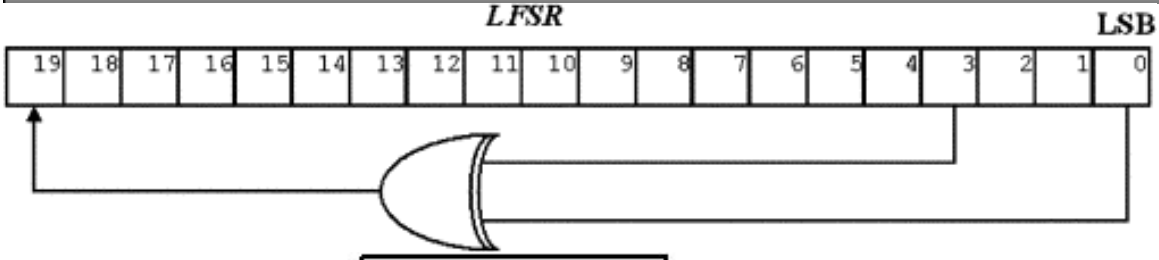
The white noise can be band-swept by sweeping the clock frequency.

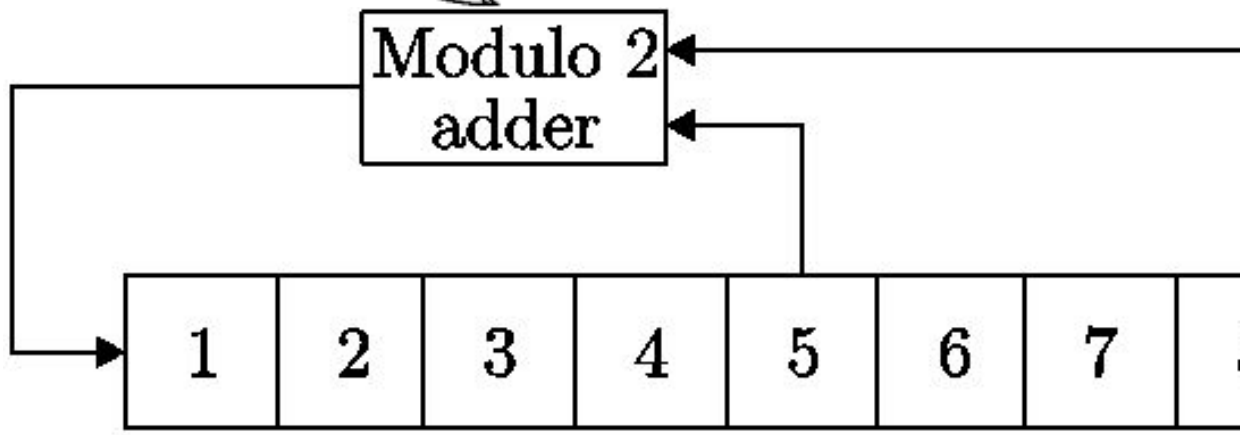
But, if you just make a strand of flip-flops and feed them back willy-nilly, there will be hidden pockets of numbers that circulate among themselves. These shorter and distinct sounding sub-sequences are stable unless they are disturbed out of their turf ((hand me that exclusive-or gate)) in which case the numbers of another sub-sequence will find expression.

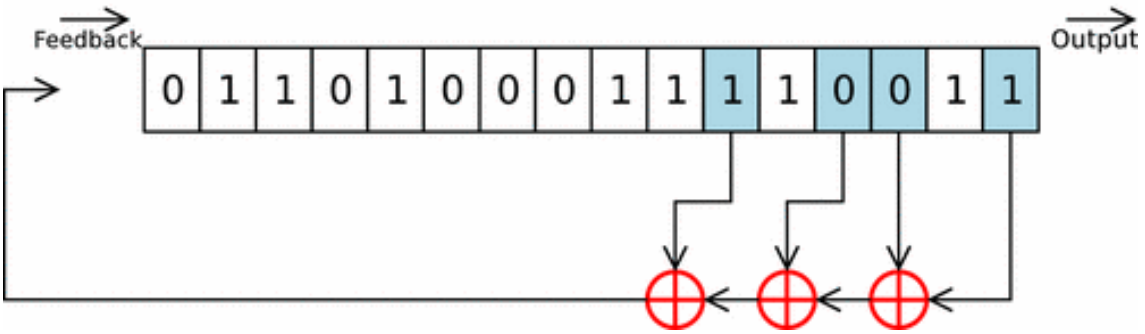
A shift register can be made of flip-flops, shift-register chips, or counter chips set to paralell-load on every clock. The counter implementation could be disturbed by switching from "load" to "count".

(Shifting a base-10 number one step to the right divides it by it by 10: "946.0" becomes "94.60".)


74LS86
CLOCK
D PR Q
CLK
CL Q
74LS74


LFSR
LSB
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0


Modulo 2
adder
1
2
3
4
5
6
7


Feedback
Output
0 1 1 0 1 0 0 0 1 1 1 1 0 0 1 1

turns, in particular a single turn only; no extra clock phases beyond the four discussed here are needed, and there is no dependence on the set-threshold property.

The flux-doubling scheme could be arrived at by a more radical structural alteration of the network of Fig. 17(c) than any of the structural variations considered in Section 3.3. However, this particular scheme derivation is more readily visualized in terms of surgery on the toroid-wire circuit of Fig. 18(c).

As mentioned near the end of Section 3.3, equalization of the sizes of cores B and M in Fig. 18(c) would help minimize the problem of back transfer. Assuming that this is done, the circuit is redrawn with the solid-line coupling loops in Fig. 20(a). The turns N_4 and N_5 [the Cl M and Cl B windings of Fig. 18(c)] are adjusted so as to equalize as much as possible the net mmf's on Cores M_O and B_O at Clear O time.

Now note that input conditions for Cores M_E and B_E are very similar, M_E being set by a counterclockwise current at $O \rightarrow E$ drive time and B_E by a comparable magnitude of clockwise current at Clear O drive time. In order to prevent M_E from being cleared by the latter loop current, a positive bias winding has been added to the Clear O line on B_E.

Unlike input conditions for cores M_E and B_E, conditions are still very different as far as output is concerned. For any flux switched in M_E is coupled on ahead, whereas flux switched into B_E "dead ends" there, being used merely to balance the $\Delta\phi$ in M_E (when the latter is cleared out) so as to prevent back transfer. The question arises as to whether we can make B comparable to M relative to output in addition to input, i.e., make B a data coupling core also. This can in fact be done. All that is required is to thread the transmitting ends of the coupling loops through the B as well as the M cores, as indicated by the dashed lines in Fig. 20(a) and by the solid lines in Fig. 20(b), where the circuit is redrawn. Since loop current at $O \rightarrow E$ time negatively links B_O in addition to M_O, B_O (like M_O) is positively biased to oppose the tendency of loop current to clear these cores.

To verify that flux doubling actually occurs in the circuit of Fig. 20(b), let us review the sequence of flux transfers during a half cycle of operation during transfer of a *one*, assuming single-turn windings in the coupling loops. Let us suppose that we initially have one unit of set flux stored in each of the cores B_O and M_O and two units in Core C_O, and suppose that these quantities represent less than half the capacities for each of the cores. The $O \rightarrow E$ drive causes the two units of flux in C_O to be transferred to M_E. Then the Clear O drive causes the two units of flux stored in B_O and C_O together to be transferred to B_E. During both of these two phases the flux switched in M_E and B_E is coupled additively into C_E via a small output-loop current, resulting in four units of flux being set into C_E. (Note

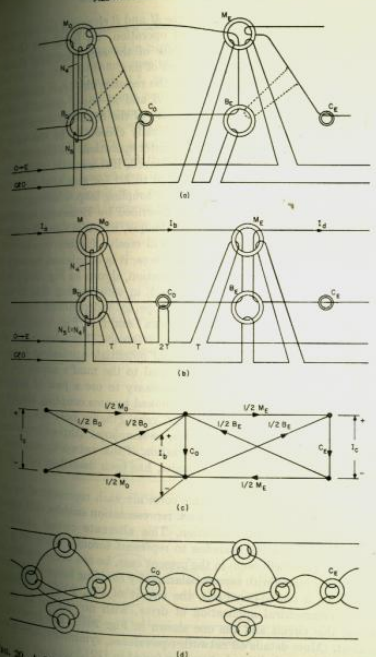
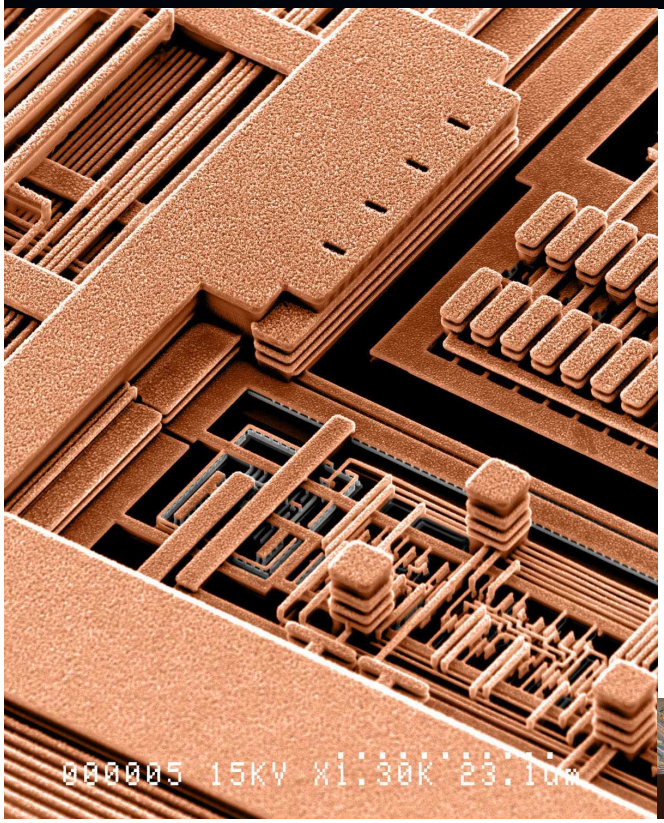


FIG. 20. A flux-doubling scheme. (a,b) Conversion of the circuit of Fig. 18(c) to a flux-doubling scheme. (c) A network form of the circuit. (d) An alternate physical realization of the network of (c). The circuits of parts (b) and (d) are operationally equivalent.


000005 15KV X1,30K 23.1um