EE 214A Design Project

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Parameter	Given Specification	Achieved Specification
Power dissipation	$\leq$ 3mW	1.5667 mW
Small-signal transresistance gain	$\geq$ 20KΩ	20.148 kΩ
$-$3dBBandwidth	$\geq$ 90MHz	90.041MHz
Common mode output voltage	-0.5 to 0.5V	-0.1714

Table 1: Specifications.

Part of Circuit	Area in μm^2
Core	132.8
NMOS-bias	40
Bias generator circuit*	8

Table 2: Area of different parts of the circuit. * Without resistor element

Section	% of Core Circuit
NMOS-bias	30.12
Bias generator circuit	6.02

Table 3: Relative area breakdown.

1 Design Outline

Our project was to design the three stage amplifier in figure 2 to the specifications listed in table 1. The common gate stage buffers the input and converts the current signal into a voltage signal, the common source stage amplifies the voltage signal, and the common drain stage buffers the output. Additionally, we designed a current mirror circuit and bias generator circuit to power the amplifier's stages. We first designed the core circuit assuming ideal current sources and then designed the biasing circuits to supply the requisite current for each stage of the amplifier. To simplify the NMOS-Bias circuit dimension calculations, we set the overdrive voltage of the NMOS-Bias circuit to 1V. As a result, we had to design our bias generator circuit to output 1.5V. The bias generator circuit was modeled on the magic battery circuit discussed in lecture.

When designing our core circuit, we started with specifications and technology parameters as inputs. To reduce the number of free parameters we decided set all channel lengths to the minimum length. This also reduced capacitances by minimizing the MOSFET areas, thereby increasing our 3dB bandwidth. Our core circuit design flow is shown in figure 1 and centers on estimating the 3dB bandwidth with ZVTC analysis. We found that the circuit divided into 4 nodes (i.e. time constants) – two nodes between stages and nodes at the input and output. Furthermore, we found that the input and output time constants could be analyzed as functions of two free parameters each: V_{OV} and I_D. Subsequently, the time constants between stages could also be parameterized by two free parameters: A_{V2} and V_{OV2}. It was not sufficient to minimize time constants stage-by-stage as this would leave insufficient current for the last stage analyzed, so we swept over V_{OV1}, I_{D1}, V_{OV3}, I_{D3}, A_{V2}, and V_{OV2} simultaneously and selected instances that met specification. We then scaled our power, bandwidth and gain requirements in Matlab until we found the minimum power design that allowed us to meet the specifications in SPICE.

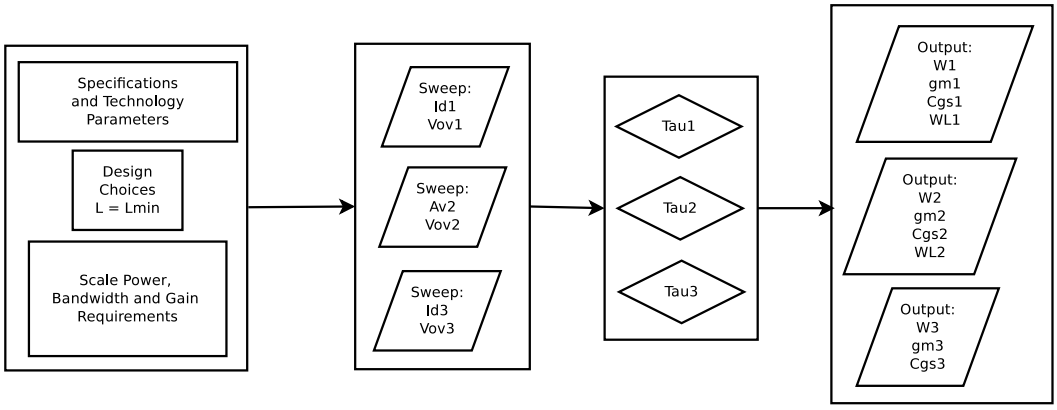

Figure 1: Core Circuit Design Process.

We found a steep bandwidth-power trade off at the common drain stage due to the large output capacitance $C_{out} \sim$ O(pF) and a power-gain tradeoff at the common source stage. The common drain stage required more current and therefore power to counteract the high capacitance of C_{out}. The common source stage was used as a voltage amplifier and the more current it consumed, the higher its gain. To optimize for power, we leveraged the conservative estimate that ZVTC provides for the 3dB bandwidth to relax the constraint on f3dB in our Matlab script so that we could lower the power consumption of our final circuit. We also adjusted our gain requirement until our SPICE result just met the requirements while consuming the least power.

2 Schematic

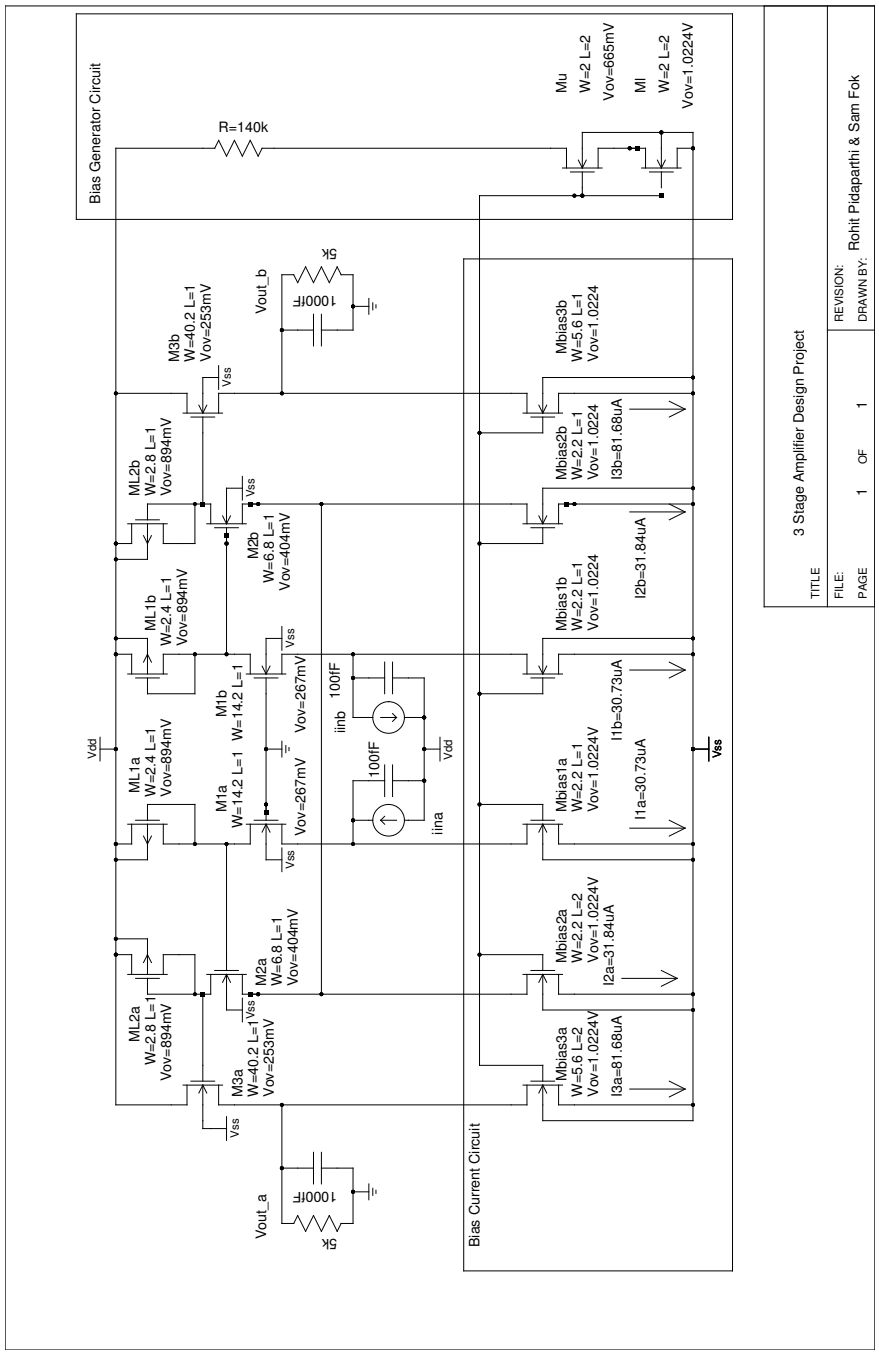

Figure 2: Schematic of our design.

3 Design Parameter Calculations

Our design flow hinges upon estimating the ZVTCs associated with each node of the amplifier. As derived in the appendix,

$$\tau_1 = \frac{V_{ov1}}{2I_{D1}}C_{in} + 1.33\frac{2}{3}\frac{L_1^2}{\mu_n Vov_1} \quad (1)$$

$$\tau_2 = \frac{R_m g_{mL2}}{0.8}(1 + 0.25(1 + A_{v2}))\frac{2}{3}\frac{L_2^2}{\mu_n V_{OV2}} \quad (2)$$

$$\tau_3 = 0.58A_{v2}\frac{2}{3}\frac{L_2^2}{\mu_n V_{OV2}} + 1.33\frac{2}{3}\frac{L_{L2}^2}{\mu_p(1 - V_{OV3})} + 0.41C_{gs3}\frac{1 - V_{OV3}}{2I_{D2}} \quad (3)$$

$$\tau_4 = \frac{1}{1.2}\frac{V_{OV3}}{I_{D3}}C_{out} + \frac{1.33}{1.2}\frac{2}{3}\frac{L_3^2}{\mu_n V_{OV3}} \quad (4)$$

(1) depends only free parameters V_{OV1} and I_{D1}, and (4) takes the same form with V_{OV3} and I_{D3} . Since we picked minimum channel length, the second terms of the sums do not contribute much and τ_1 and τ_4 are minimized by by maximizing I_D and minimizing V_{OV} (see Figure 3).
From sweeping I_{D1} and V_{OV1} and picking τ_1 with (1), we extract:

$$W_1 = \frac{2I_{D1}L_1}{KP_n V_{OV1}}$$

$$g_{m1} = \frac{2I_{D1}}{V_{OV1}}$$

$$C_{gs1} = \frac{\tau_1 g_{m1} - C_{in}}{1.33}$$

Similarly, sweeping I_{D3} and V_{OV3} and picking τ_4 with (4), we can extract:

$$W_3 = \frac{2I_{D3}L_3}{KP_n V_{OV3}}$$

$$g_{m3} = \frac{2I_{D3}}{V_{OV3}}$$

$$C_{gs1} = \frac{1.2\tau_4 g_{m3} - C_{out}}{1.33}$$

With I_{D1}, I_{D3}, and a fixed total power, we can set:

$$g_{mL2} = \frac{2I_{D2}}{V_{OVL2}}$$

$$W_{L2} = \frac{2I_{D2}L_{L2}}{KP_P V_{OVL2}^2}$$

Where $I_{D2} = I_{total} - I_{D1} - I_{D3}$ from the power constraint and $V_{OVL2} = 1 - V_{OV3}$ from the constraint that the common mode output voltage be between -0.5 and $0.5V$ (derivation in appendix). For a given total power, $I_{D1}$and I_{D3}, I_{D2} is fixed, so (2) and (3) depend only on free parameters A_{v2} and V_{OV2}, so we consider their sum in Figure 4. From V_{OV2} and A_{v2}:

$$W_2 = \frac{2I_{D2}L_2}{KP_n V_{OV2}^2}$$

$$g_{m2} = A_{v2}g_{mL2}$$

$$g_{mL1} = \frac{0.8A_{v2}}{R_m}$$

$$V_{OVL1} = \frac{2I_D}{g_{mL1}}$$

$$W_{L1} = \frac{2I_{D1}L_{L1}}{KP_p V_{OVL1}^2}$$

A minimum power circuit can then be found by incrementally decreasing our total power (hence current) and shrinking our solution space until finding an optimal power circuit.

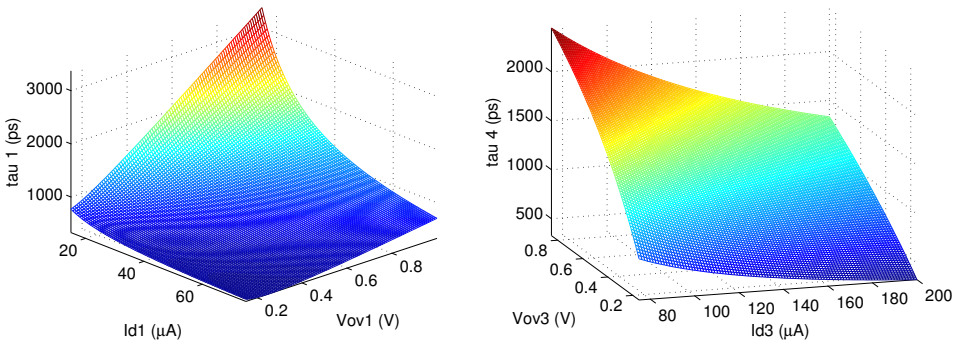

Figure 3: τ_1 and τ_4 take on the same form and both are minimized by maximixing current and minimizing overdrive voltage. We require a large I_{D3} to compensate for the large C_{out}. In addition, V_{OV3} is restricted from being too small by the specification that common mode output voltage be between -0.5 and $0.5V$. Although we could pick I_D and V_{OV} to minimize τ_1 and τ_4, this would not yield a globally optimal solution as τ_2 and τ_3 are dependent parameters set in picking τ_1 and τ_4.

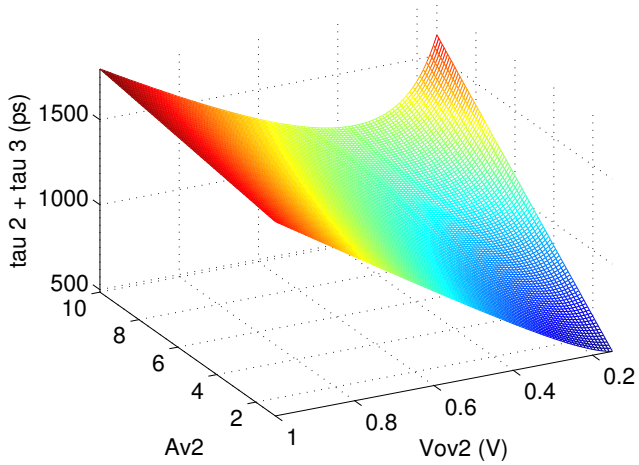

Figure 4: $\tau_2 + \tau_3$ is a convex surface that increases monotonically with A_{v2}. As A_{v2} increases, the range of feasible V_{OV2} becomes more restricted.

SPICE Results and Comparison with Hand Calculations

Comparisons between hand calculated values and SPICE results are listed in Tables 4 and 5. When we calculated gain, 3dB bandwidth and power consumption by hand, we knew that our 3dB bandwidth would be lower than the SPICE result because ZVTC provides a conservative approximation of 3dB. Therefore, we relaxed the 3dB bandwidth requirement to trade 3dB bandwidth for gain and power. This accounts for the discrepencies between our hand calculations and our final spice bandwidth.

Bias Circuit Calculations

The bias circuit shown in Figure 2 was created using the magic battery technique of Lecture 13. In order to determine the parameters for the bias circuit, we can use the following equation derived in the lecture:

Calculation	Gain($k\Omega$)	BW (Hz)	Power (mW)
Hand	21.949	80.13	1.45
SPICE	20.148	90.041	1.5667
%Difference hand and SPICE	8.2	-12.4	21.5

Table 4: Gain, 3dB bandwidth, and power comparison between hand calculations and SPICE.

	Hand Calculations			Spice Results			% difference		
Mosfet	$g_m(\mu S)$	$I_D(\mu A)$	$V_{OV}(V)$	$g_m(\mu S)$	$I_D(\mu A)$	$V_{OV}(V)$	g_m	I_D	V_{OV}
M1	274	35.6	0.52	230	30.73	0.27	16	13.7	48.5
M2	142	32	0.91	157	31.84	0.40	-10.6	0.6	55.4
M3	795	77.6	0.34	645	81.68	0.25	18.9	-5.3	25.3
ML1	94.9	-35.2	1.5	64.96	-30.73	0.95	31.5	13.7	36.9
ML2	113.3	-32	1.13	71.27	-31.84	0.89	37.1	0.6	21
Mbias1	142.4	35.6	1	60.12	30.73	1.02	57.8	13.7	-2.2
Mbias2	128.2	32	1	62.29	31.84	1.02	51.4	0.6	-2.2
Mbias3	269.5	77.6	1	159.8	81.68	1.02	40.7	-5.3	-2.2

Table 5: Hand calculations vs SPICE simulation results of MOSFET parameters.

$$V_B = \sqrt{\frac{(k+1)\cdot 2I_{bias}}{\frac{W}{L}\cdot KP}} + V_t \tag{5}$$

we can then rearrange to solve for I_{bias} to get:

$$I_{bias} = \frac{(V_B - V_t)^2(\frac{W}{L}\cdot KP)}{2\cdot(k+1)} \tag{6}$$

From project specifications we have the constraint that $W_{min} = 2\mu$m. We then replace W in the equation above with $k \cdot W_{min}$ to get:

$$I_{bias} = \frac{(V_B - V_t)^2(\frac{kW_{min}}{L}\cdot KP)}{2\cdot(k+1)} \tag{7}$$

From this equation, power is minimized if we pick k=1 because $\frac{k}{2\cdot(k+1)} = \frac{1}{4}$ wheras if k increases $\frac{k}{2\cdot(k+1)} = \frac{1}{2}$. In our design, we chose to create an overvoltage of 1V so we needed to produce a target bias voltage $V_B$of 1.5V. These choices for k and $V_B$give us a bias current I_{bias}. We can then use Ohm's law to determine R_B, the resistor we need :

$$R_B = \frac{V_{DD} - V_{ss} - V_{bias}}{I_{bias}} \tag{8}$$

4 Bode Plot

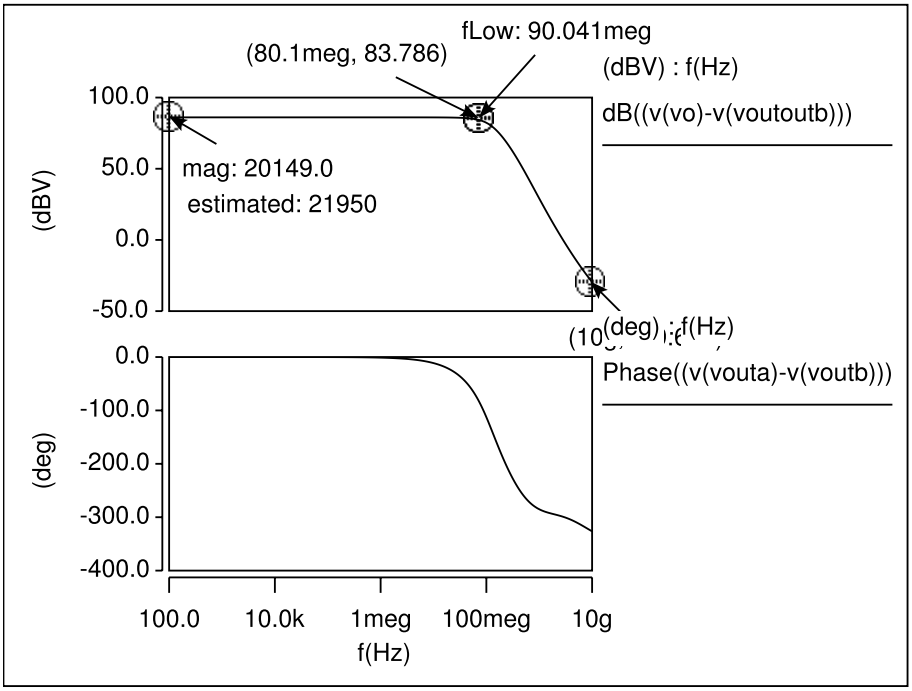

Figure 5: Bode Plot

As expected, our hand calculated 3dB bandwidth was lower than the spice result because ZVTC conservatively estimates the bandwidth. Interestingly, the two closely spaced kinks in phase plot around 3g with little corresponding change in the magnitude plot suggest that there is a closely spaced pole-zero pair around 3g.

5 Transient Simulation

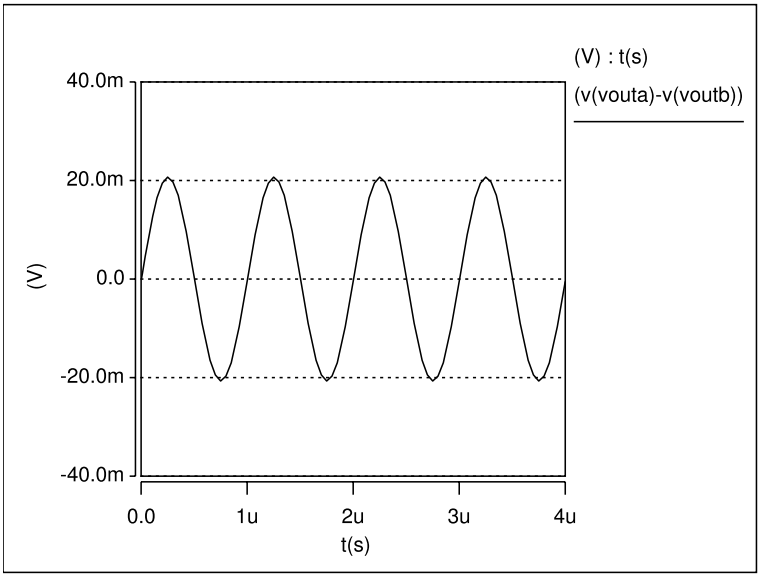

Figure 6: Transient Simulation. Input is 1MHz, 0.5μA differential sine wave. Slightly greater than 20kΩ gain observed with no distortion.

6 Conclusion

We designed and simulated a differential, three stage amplifier with bias circuitry that met the specifications and minimized power.

We learned to reduce a potentially very high dimensional problem of sizing a multistage circuit to a managable, lower dimensional space using assumptions about the relative scale of factors and simplifying design choices. Being more familiar with the relative scales and contributions of circuit parameters such as capacitances and conductances would have certainly expedited the design process.

As our first circuit design project, we were tripped up by things we had not encountered before. Having not worked with differential circuits before, we did not discover a bug from not connecting the sources of our differential common source stages in our SPICE deck for days.

7 Appendix

We consider four capcitances for each MOSFET: C_{gs}, C_{gd}, C_{db}, and C_{sb}. For ZVTC analysis, the resistances as seen from each capacitance are listed in (Table 6). To further simplify, we assume that:

$$\begin{aligned} C_{gd}/C_{gs} &= 0.25 \\ C_{db}/C_{gs} &= 0.33 \\ C_{sb}/C_{gs} &= 0.33 \\ g_{mb}/g_m &= 0.2 \end{aligned} \tag{9}$$

We will also use:

$$\frac{C_{gs}}{g_m} = \frac{2}{3}\frac{L^2}{\mu V_{OV}} \tag{10}$$

,

$$\begin{aligned} R_m &= \frac{1}{g_{mL1}}\frac{g_{m2}}{g_{mL2}}A_{v3} \\ &= \frac{1}{g_{mL1}}\frac{g_{m2}}{g_{mL2}}0.8 \\ R_m &= \frac{1}{g_{mL1}}A_{v2}0.8 \end{aligned} \tag{11}$$

Where we assume $A_{v3} = 0.8$ since M_3 is in common drain configuration.

	M_1	M_{L1}	M_2	M_{L2}	M_3
C_{gs}	$\frac{1}{g_{m1}}$	$\frac{1}{g_{mL1}}$	$\frac{1}{g_{mL1}}$	$\frac{1}{g_{mL2}}$	$\frac{R_{out}}{1+g_m' R_{out}} + \frac{1}{6}\frac{1}{g_{mL2}}$
C_{gd}	$\frac{1}{g_{mL1}}$	shorted	$\frac{1}{g_{mL2}} + \frac{1}{g_{mL1}} + A_{v2}\frac{1}{g_{mL1}}$	shorted	$\frac{1}{g_{mL2}}$
C_{db}	$\frac{1}{g_{mL1}}$	$\frac{1}{g_{mL1}}$	$\frac{1}{g_{mL2}}$	$\frac{1}{g_{mL2}}$	$\frac{R_{out}}{1+g_m' R_{out}}$
C_{sb}	$\frac{1}{g_{m1}}$	shorted	shorted	shorted	$\frac{R_{out}}{1+g_m' R_{out}}$

C_{in}	$C_{out} = 2C_L$
$\frac{1}{g_{m1}}$	$\frac{R_{out}}{1+g_m' R_{out}}$

Table 6: Resistances seen by Capacitances. R_{Cgd_M2} follows from CS configuration, and R_{Cgs_M3} was derived following HW4P3. Also note that $R_{out} = R_L/2$.

From Table 6, we can divide the time constants of the circuit into four groups according to the resistances seen by the capacitors. τ_1 consists of the capacitors that see resistance $\frac{1}{g_{m1}}$:

$$\begin{aligned} \tau_1 &= \frac{1}{g_{m1}}(C_{in} + C_{gs1} + C_{sb1}) \\ &= \frac{1}{g_{m1}}(C_{in} + 1.33C_{gs1}) \\ &= \frac{1}{g_{m1}}C_{in} + 1.33\frac{C_{gs1}}{g_{m1}} \\ \tau_1 &= \frac{V_{ov1}}{2I_{D1}}C_{in} + 1.33\frac{2}{3}\frac{L_1^2}{\mu_n V ov_1} \end{aligned}$$

The second line follows from (9) and the fourth line follows from (10). τ_2 consists of the capacitors that see resistance $R_{L1} = \frac{1}{g_{mL1}}$:

$$\begin{aligned}
\tau_2 &= \frac{1}{g_{mL1}}(C_{gs2} + (1 + A_{v2})C_{gd2}) \\
&= \frac{1}{g_{mL1}}(1 + 0.25(1 + A_{v2}))C_{gs2} \\
&= \frac{R_m}{A_{v2}0.8}(1 + 0.25(1 + A_{v2}))C_{gs2} \\
&= \frac{R_m g_{mL2}}{0.8}(1 + 0.25(1 + A_{v2}))\frac{C_{gs2}}{g_{m2}} \\
\tau_2 &= \frac{R_m g_{mL2}}{0.8}(1 + 0.25(1 + A_{v2}))\frac{2}{3}\frac{L_2^2}{\mu_n V_{OV2}}
\end{aligned}$$

The second line follows from (9), the third line follows from (11), and the fifth line follows from (10). τ_3 consists of the capacitors that see resistance $\frac{1}{g_{mL2}}$:

$$\begin{aligned}
\tau_3 &= \frac{1}{g_{mL2}}(C_{db2} + C_{gd2} + C_{gsL2} + C_{dbL2} + C_{gd3} + \frac{1}{6}C_{gs3}) \\
&= \frac{1}{g_{mL2}}(0.58C_{gs2} + 1.33C_{gsL2} + 0.41C_{gs3}) \\
&= 0.58A_{v2}\frac{C_{gs2}}{g_{m2}} + 1.33\frac{C_{gsL2}}{g_{mL2}} + 0.41C_{gs3}\frac{V_{OVL2}}{2I_{D2}} \\
&= 0.58A_{v2}\frac{2}{3}\frac{L_2^2}{\mu_n V_{OV2}} + 1.33\frac{2}{3}\frac{L_{L2}^2}{\mu_p V_{OVL2}} + 0.41C_{gs3}\frac{1 - V_{OV3}}{2I_{D2}} \\
\tau_3 &= 0.58A_{v2}\frac{2}{3}\frac{L_2^2}{\mu_n V_{OV2}} + 1.33\frac{2}{3}\frac{L_{L2}^2}{\mu_p(1 - V_{OV3})} + 0.41C_{gs3}\frac{1 - V_{OV3}}{2I_{D2}}
\end{aligned}$$

Note that $V_{OVL2} = 1 - V_{OV3}$ from the constraint that the common mode output voltage be between -0.5 and $0.5V$. If we set $V_{out} = 0V$, we have that $V_{sb3} = 2.5V$ so $V_t(V_{sb3}) = V_{t0} + \gamma(\sqrt{2\phi_f + V_{sb3}} - \sqrt{2\phi_f}) \approx 1V$ for the given technology parameters

$$\begin{aligned}
V_{OV3} &= V_{gs3} - V_t(V_{sb3}) \\
&= V_{g3} - V_{out} - 1V \\
V_{OV3} &= V_{g3} - 0V - 1V
\end{aligned} \tag{12}$$

$$\begin{aligned}
V_{OVL2} &= V_{sgL2} - V_{tL2} \\
&= V_{DD} - V_{g3} - V_{tL2} \\
&= 2.5V - V_{g3} - 0.5V \\
V_{OVL2} &= 2V - V_{g3}
\end{aligned} \tag{13}$$

Adding (12) to (13) yields

$$V_{OV3} + V_{OVL2} = 1V \tag{14}$$

As $R_{out} = 5\text{k}\Omega$and $\frac{1}{g'_{m3}} = \text{O}(1\text{k}\Omega)$, we can approximate $\frac{R_{out}}{1+g'_m R_{out}}$ with $\frac{1}{g'_{m3}}$, soτ_4 follows the same steps as τ_1:

$$\begin{aligned}
\tau_4 &= \frac{1}{g'_{m3}}(C_{out} + C_{gs3} + C_{sb3}) \\
&= \frac{1}{1.2g_{m3}}(C_{out} + 1.33C_{gs3}) \\
&= \frac{1}{1.2}\frac{1}{g_{m3}}C_{out} + \frac{1.33}{1.2}\frac{C_{gs3}}{g_{m3}} \\
\tau_4 &= \frac{1}{1.2}\frac{V_{OV3}}{I_{D3}}C_{out} + \frac{1.33}{1.2}\frac{2}{3}\frac{L_3^2}{\mu_n V_{OV3}}
\end{aligned}$$

```
* Design Problem, ee114/214A- 2012
* Please fill in the specification achieved by your circuit
* before your submit the netlist.
************************************************************
* The specifications that this script achieves are:
* sunetid = rohitpid, samfok
* Power  = 1.5667 mW
* Gain   = 20.148 K
* BandWidth = 90.041  MHz
************************************************************


** Including the model file
.include /usr/class/ee114/hspice/ee114_hspice.sp

* Defining Top level circuit parameters
.param Cin = 100f
.param CL  = 500f
.param RL  = 10K

* defining the supply voltages

vdd vdd 0 2.5
vss vss 0 -2.5

* Defining the input current source

** For ac simulation uncomment the following 2 lines**
 Iina           iina    vdd     ac      0.5
 Iinb           vdd     iinb    ac      0.5

** For transient simulation uncomment the following 2 lines**
*Iina           iina    vdd     sin(0 0.5u 1e6)
*Iinb           vdd     iinb    sin(0 0.5u 1e6)

* Defining Input capacitance

Cina    vdd     iina 'Cin'
Cinb    vdd     iinb 'Cin'

* Defining the differential load

RL      vouta           voutb           'RL'
CL      vouta           voutb           'CL'

*** Your Trans-impedance Amplifier here ***
**nmos***
*name drain gate source bulk type parameters*
M1a  node_1a 0 iina vss nmos114 w=14.2u l=1u
M1b  node_1b 0 iinb vss nmos114 w=14.2u l=1u
M2a  node_2a node_1a ibias2 vss nmos114 w=6.8u l=1u
M2b  node_2b node_1b ibias2 vss nmos114 w=6.8u l=1u
M3a  vdd node_2a vouta vss nmos114 w=40.2u l=1u
M3b  vdd node_2b voutb vss nmos114 w=40.2u l=1u

**pmos***
*name drain gate source bulk type parameters*
ML1a node_1a node_1a vdd vdd pmos114 w=2.4u l=1u
ML1b node_1b node_1b vdd vdd pmos114 w=2.4u l=1u
ML2a node_2a node_2a vdd vdd pmos114 w=2.8u l=1u
ML2b node_2b node_2b vdd vdd pmos114 w=2.8u l=1u

*** Your Bias Circuitry here ***
**nmos***
*name drain gate source bulk type parameters*
Mbias1a iina nbias vss vss nmos114 w=2.2u l=2u
Mbias1b iinb nbias vss vss nmos114 w=2.2u l=2u
```

```
Mbias2a ibias2 nbias vss vss nmos114 w=2.2u l=2u
Mbias2b ibias2 nbias vss vss nmos114 w=2.2u l=2u
Mbias3a vouta nbias vss vss nmos114 w=5.6u l=2u
Mbias3b voutb nbias vss vss nmos114 w=5.6u l=2u


*** nmos
*** drain gate source bulk mostype w_value l_value
Mu nbias nbias vx vss nmos114 w=2u l=1u
Ml vx nbias vss vss nmos114 w=2u l=1u

*Resistors
R vdd nbias 140k


* defining the analysis

.op
.option post brief nomod

** For ac simulation uncomment the following line**
.ac dec 100 100 10g
.measure ac gainmax max vdb(vouta)
.measure ac f3db when vdb(vouta)='gainmax-3'

** For transient simulation uncomment the following line **
*.tran 0.01u 4u

.end
```

```
****** HSPICE -- B-2008.09-SP1 32-BIT (Nov 24 2008) linux ******
******
* design problem, ee114/214a- 2012

 ******  operating point information tnom=  25.000 temp=  25.000 *****
***** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:ibias2  =-345.1616m 0:iina    =  -1.1166  0:iinb    =  -1.1166
+0:nbias   =-977.6485m 0:node_1a =   1.0540  0:node_1b =   1.0540
+0:node_2a =   1.1064  0:node_2b =   1.1064  0:vdd     =   2.5000
+0:vouta   =-171.4282m 0:voutb   =-171.4282m 0:vss     =  -2.5000
+0:vx      =  -2.2270


****  voltage sources

subckt
element  0:vdd      0:vss
 volts      2.5000    -2.5000
 current -313.3478u  313.3478u
 power    783.3695u  783.3695u

    total voltage source power dissipation=    1.5667m       watts



***** current sources

subckt
element  0:iina     0:iinb
 volts     -3.6166     3.6166
 current    0.          0.
 power      0.          0.


    total current source power dissipation=   0.            watts

**** resistors

subckt
element  0:rl       0:r
 r value   10.0000k  140.0000k
 v drop   832.6673a    3.4776
 current  8.327e-20   24.8403u
 power      0.        86.3860u



**** mosfets


subckt
element  0:m1a      0:m1b      0:m2a      0:m2b      0:m3a      0:m3b
model    0:nmos114. 0:nmos114. 0:nmos114. 0:nmos114. 0:nmos114. 0:nmos114.
region     Saturati   Saturati   Saturati   Saturati   Saturati   Saturati
 id        30.7312u   30.7312u   31.8399u   31.8399u   81.6826u   81.6826u
 ibs      -13.8338f  -13.8338f  -21.5484f  -21.5484f  -23.2857f  -23.2857f
 ibd      -35.5398f  -35.5398f  -36.0644f  -36.0644f  -50.0000f  -50.0000f
 vgs        1.1166     1.1166     1.3991     1.3991     1.2779     1.2779
 vds        2.1706     2.1706     1.4516     1.4516     2.6714     2.6714
 vbs       -1.3834    -1.3834    -2.1548    -2.1548    -2.3286    -2.3286
 vth      849.9200m  849.9200m  994.7223m  994.7223m    1.0246     1.0246
 vdsat    266.6980m  266.6980m  404.4160m  404.4160m  253.2614m  253.2614m
 vod      266.6980m  266.6980m  404.4160m  404.4160m  253.2614m  253.2614m
 beta     864.1122u  864.1122u  389.3546u  389.3546u    2.5470m    2.5470m
 gam eff  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m
```

```
 gm       230.4570u  230.4570u  157.4612u  157.4612u  645.0458u  645.0458u
 gds        2.5250u    2.5250u    2.7804u    2.7804u    6.4462u    6.4462u
 gmb       46.7893u   46.7893u   27.4807u   27.4807u  109.4054u  109.4054u
 cdtot     15.1944f   15.1944f    8.1767f    8.1767f   37.8570f   37.8570f
 cgtot     36.4525f   36.4525f   17.3665f   17.3665f  103.1510f  103.1510f
 cstot     39.0998f   39.0998f   19.2848f   19.2848f  103.5813f  103.5813f
 cbtot     18.6108f   18.6108f   10.3140f   10.3140f   40.2499f   40.2499f
 cgs       28.8734f   28.8734f   13.8267f   13.8267f   81.7403f   81.7403f
 cgd        7.1945f    7.1945f    3.4303f    3.4303f   20.4293f   20.4293f


subckt
element  0:ml1a     0:ml1b     0:ml2a     0:ml2b     0:mbias1a  0:mbias1b
model    0:pmos114. 0:pmos114. 0:pmos114. 0:pmos114. 0:nmos114. 0:nmos114.
region     Saturati   Saturati   Saturati   Saturati   Saturati   Saturati
 id       -30.7312u  -30.7312u  -31.8399u  -31.8399u   30.7312u   30.7312u
 ibs        0.         0.         0.         0.         0.         0.
 ibd       14.4602f   14.4602f   13.9356f   13.9356f  -13.8338f  -13.8338f
 vgs       -1.4460    -1.4460    -1.3936    -1.3936     1.5224     1.5224
 vds       -1.4460    -1.4460    -1.3936    -1.3936     1.3834     1.3834
 vbs        0.         0.         0.         0.         0.         0.
 vth     -500.0000m -500.0000m -500.0000m -500.0000m  500.0000m  500.0000m
 vdsat   -946.0234m -946.0234m -893.5570m -893.5570m    1.0224     1.0224
 vod     -946.0234m -946.0234m -893.5570m -893.5570m    1.0224     1.0224
 beta      68.6761u   68.6761u   79.7549u   79.7549u   58.8043u   58.8043u
 gam eff  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m
 gm        64.9692u   64.9692u   71.2655u   71.2655u   60.1187u   60.1187u
 gds        2.6849u    2.6849u    2.7946u    2.7946u    1.4372u    1.4372u
 gmb       21.7913u   21.7913u   23.9032u   23.9032u   20.1644u   20.1644u
 cdtot      4.7373f    4.7373f    5.3027f    5.3027f    4.5877f    4.5877f
 cgtot      6.1194f    6.1194f    7.1407f    7.1407f    9.0141f    9.0141f
 cstot      9.9800f    9.9800f   11.2934f   11.2934f   12.6067f   12.6067f
 cbtot      8.6553f    8.6553f    9.5262f    9.5262f    8.2778f    8.2778f
 cgs        4.8800f    4.8800f    5.6934f    5.6934f    7.8467f    7.8467f
 cgd        1.2106f    1.2106f    1.4120f    1.4120f    1.1187f    1.1187f


subckt
element  0:mbias2a  0:mbias2b  0:mbias3a  0:mbias3b  0:mu       0:ml
model    0:nmos114. 0:nmos114. 0:nmos114. 0:nmos114. 0:nmos114. 0:nmos114.
region     Saturati   Saturati   Saturati   Saturati   Saturati     Linear
 id        31.8399u   31.8399u   81.6826u   81.6826u   24.8403u   24.8403u
 ibs        0.         0.         0.         0.        -2.7295f    0.
 ibd      -21.5484f  -21.5484f  -23.2857f  -23.2857f  -15.2235f   -2.7295f
 vgs        1.5224     1.5224     1.5224     1.5224     1.2494     1.5224
 vds        2.1548     2.1548     2.3286     2.3286     1.2494   272.9544m
 vbs        0.         0.         0.         0.      -272.9544m    0.
 vth      500.0000m  500.0000m  500.0000m  500.0000m  584.8448m  500.0000m
 vdsat      1.0224     1.0224     1.0224     1.0224   664.5523m  272.9544m
 vod        1.0224     1.0224     1.0224     1.0224   664.5523m    1.0224
 beta      60.9258u   60.9258u  156.3000u  156.3000u  112.4940u  102.7295u
 gam eff  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m
 gm        62.2876u   62.2876u  159.7935u  159.7935u   74.7581u   28.0405u
 gds        1.4372u    1.4372u    3.6582u    3.6582u    2.2081u   79.4033u
 gmb       20.8919u   20.8919u   53.5964u   53.5964u   21.6516u    9.4051u
 cdtot      4.2679f    4.2679f    7.6382f    7.6382f    4.2969f    7.2545f
 cgtot      9.0245f    9.0245f   22.9775f   22.9775f    5.1045f    6.5858f
 cstot     12.6067f   12.6067f   27.4534f   27.4534f    8.2756f    8.1180f
 cbtot      7.9476f    7.9476f   12.3624f   12.3624f    7.5284f    8.8311f
 cgs        7.8467f    7.8467f   19.9734f   19.9734f    4.0667f    3.5180f
 cgd        1.1291f    1.1291f    2.8800f    2.8800f    1.0077f    3.0456f


******
```

```
* design problem, ee114/214a- 2012

 ******  ac analysis tnom=  25.000 temp=  25.000 *****
  gainmax=  8.0064E+01    at=  1.2882E+04
              from=  1.0000E+02    to=  1.0000E+10
  f3db=  9.0041E+07

         ***** job concluded
****** HSPICE -- B-2008.09-SP1 32-BIT (Nov 24 2008) linux ******
******
* design problem, ee114/214a- 2012

 ******  job statistics summary tnom=  25.000 temp=  25.000 *****

 ******  HSPICE Threads Information  ******
 Command Line Threads Count:                      0
 Available CPU Count:                             8
 Actual Model Evaluation(Load) Threads Count:     1
 Actual Solver Threads Count:                     1


 ******  Circuit Statistics  ******
 # nodes       =      14  # elements   =      27
 # resistors   =       2  # capacitors =       3  # inductors   =       0
 # mutual_inds =       0  # vccs       =       0  # vcvs        =       0
 # cccs        =       0  # ccvs       =       0  # volt_srcs   =       2
 # curr_srcs   =       2  # diodes     =       0  # bjts        =       0
 # jfets       =       0  # mosfets    =      18  # U elements  =       0
 # T elements  =       0  # W elements =       0  # B elements  =       0
 # S elements  =       0  # P elements =       0  # va device   =       0


 ******  Runtime Statistics (seconds)  ******

 analysis           time    # points   tot. iter  conv.iter
 op point           0.00           1           7
 ac analysis        0.02         801         801
 readin             0.00
 errchk             0.00
 setup              0.00
 output             0.00


          total memory used          184  kbytes
          total cpu time            0.02 seconds
          total elapsed time        0.09 seconds
          job started at     01:51:59 11/26/2012
          job ended   at     01:51:59 11/26/2012
```