Module 3: Memory Roadmap

In a nutshell: Having built the computer's ALU, this module we turn to building the computer's *main memory* unit, also known as *Random Access Memory,* or *RAM*. This will be done gradually, going bottom-up from elementary flip-flop gates to one-bit registers to *n*-bit registers to a family of RAM chips. Unlike the computer's processing chips, which are based on *combinational logic*, the computer's memory logic requires a clock-based *sequential logic*. We will start with an overview of this theoretical background, and then move on to build our memory chipset.

Key concepts: combinational vs sequential logic, clocks and cycles, flip-flops, registers, RAM units, counters.

WATCH:

- Unit 3.1: Sequential Logic
- Unit 3.2: Flip Flops
- Unit 3.3: Memory Units
- Unit 3.4: Counters
- Unit 3.5: Project 3 Overview
- Unit 3.6: Perspectives

DO:

- Project 3: Sequential Chips.
- **Submission instructions:** note that the project 3 files are located in two folders named 'a' and 'b'. This technical detail speeds up the simulation and testing of the project 3 chips. However, when you submit your work in a zip file, put all the files together, and not inside any folders.
- If you are taking the course as an auditor, you can check your work yourself, using the tests described here. If you are taking the certificate option, submit your project zip file here.

GET HELP:

Module 3 Discussion Forum