Freescale Semiconductor
Application Note

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Cookbook for SAR ADC Measurements

ADC measurements done properly

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Contents

1 Introduction

An analog to digital (A/D) converter cannot ensure ideal accuracy by itself. A number of parameters can affect the achievable accuracy of an A/D converter in an application.

For example:

- A/D conversion timing (that is, acquisition time, conversion time, sampling time, sampling jitter, and so on)
- Power supply characteristics (noise, internal impedance)
- Isolation between digital and analog portions of the data acquisition system
- Internal and external impedance matching
- I/O switching
- PCB layout

To achieve optimal performance, it is necessary to consider the overall A/D conversion system in the application design. This document gives comprehensive guidelines on how to correctly select and design the required external RC components for a SAR A/D input based upon a selected acquisition time and other converter parameters that can be found in the controller documentation.

This application note was written to address a number of similar requests from several customers. One customer reported having performed an investigation of the influence of the A/D during sampling, and also of the influence of different values of external RC components on performance. They

observed serious voltage disturbances (voltage drops/peaks) at the A/D input (see Figure 1). This disturbance was even worse in the case of sequential sampling, when the previously measured signal was grounded. The disturbance at the A/D input in this case results from the basic principle of operation of the sample and hold (S/H) circuit inherent in a SAR A/D. These disturbances do not have to introduce a loss of conversion accuracy as long as the A/D timing is set correctly. If appropriate precautions are not taken, a significant reduction in the accuracy of the digital result can occur during the conversion. This application note clearly shows how to avoid this situation by choosing the correct conversion time and external RC components. An example of a correct external RC component design is presented at the end of the application note. The example clearly demonstrates proper selection and design of external components and also mentions common mistakes related to incorrect selection of external resistance.

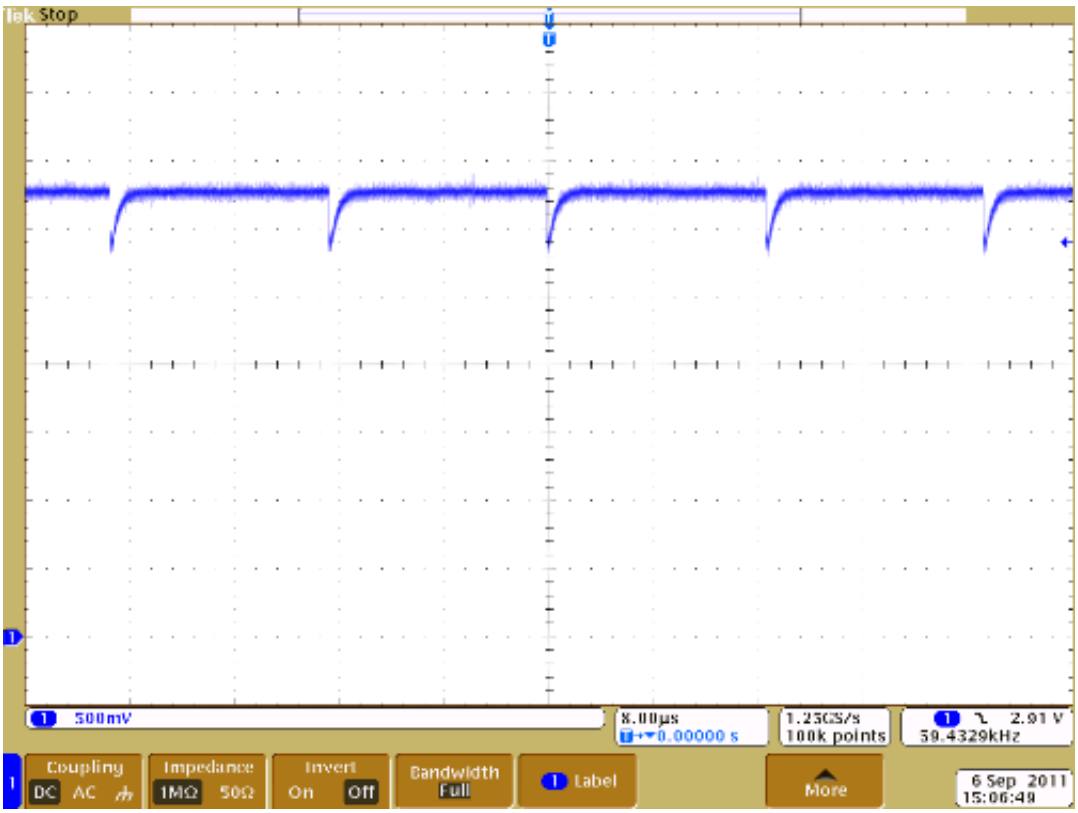

Figure 1. Voltage drops at A/D input during sampling process

2 Theoretical background

To achieve the best performance from an A/D, the overall system must be designed and configured correctly. The hardware setup must carefully follow data sheet recommendations, for example:

- Place 0.1 µF capacitor positioned as near as possible to the package power pins (one capacitor for each power pins pairs)
- Place approximately 100 µF capacitor to power pins
- PCB trace lengths should be minimal
- It is necessary to consider all parasitic passive components due to PCB traces in your application
- Special care must be taken to minimize noise levels on the analog power and reference pins
- Use separate power and ground planes for digital and analog supply pins
- If the analog and digital circuits are connected to the same power supply a small inductor (or ferrite) should be connected between digital and analog pins
- Separate analog components from noisy digital components by ground planes (not in parallel), and place the analog ground trace around the analog signal trace

In addition the aforementioned recommendations, special attention must be paid to the design and selection of the external RC components. Minimum values for the external RC components must be considered in final calculations. See *MC56F825x/ MC56F824x Digital Signal Controller* (document MC56F825X)

In the text below, the basic principle of the sample and hold circuit (S/H) that is inherently part of an A/D is described in detail. An equivalent sampling circuit considered to present the required background theory is shown in Figure 2. To simplify the sampling process all parasitic components are neglected.

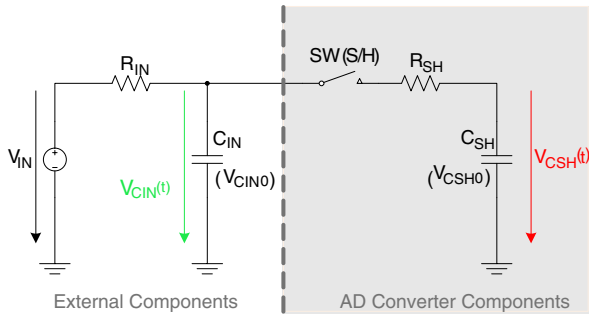

Figure 2. Equivalent sampling circuit

Considering the correct sampling process (including *Nyquist-Shannon* sampling theorem), it is possible to replace a measured input signal with a constant DC voltage source during the A/D conversion time. If the signal source is assumed to have a large input impedance ($R_{IN} >> R_{SH}$), two essentially different time intervals of sampling capacitance charging appears. This is not a common case, but a lot of designers use it (usually $R_{IN} \leq R_{SH}$). Time waveforms for the voltage across the sampling capacitor C_{SH} (red) and the voltage across the input capacitor C_{IN} (green) are shown in Figure 3.

NOTE

Figure 3 assumes that the initial voltage across the input capacitor C_{IN} is greater than the initial voltage across the sampling capacitor C_{SH} ($V_{CIN0} > V_{CSH0}$). In such a case, the voltage drop across the input capacitor appears (see Figure 3). In some cases this condition is not satisfied, that is $V_{CIN0} < V_{CSH0}$. In this case, a voltage peak across the input capacitor appears. The magnitude of the voltage drop/peak is defined by Eqn.6.

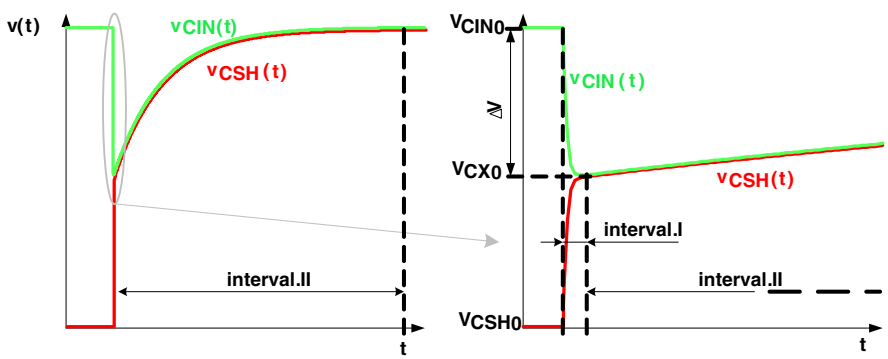

Figure 3. Example of time waveforms of voltage across sampling capacitor and voltage across input capacitor (b. in detail)

In Figure 3, the charging of the sampling capacitor C_{SH} should be divided into two time intervals (see Figure 2). In the case of high input impedance, the second interval is much slower than the first one. Taking these facts into account, the equivalent circuit from Figure 2 can be divided into two separate equivalent circuits as shown in Figure 4. The first (shorter) interval is represented by the circuit shown in fig. 4a. Solving a system of differential equations, it is possible to achieve mathematical representation of voltage time waveforms. The voltage across sampling capacitance is defined as:

Eqn.1

$$V_{CSH}(t) = \left(V_{CIN0} - V_{CSH0}\right)\frac{\alpha}{\alpha+1}\left(1 - e^{-\frac{t}{\tau_I}}\right) + V_{CSH0}$$

and the voltage across input capacitance as:

Eqn.2

$$V_{CIN}(t) = (V_{CIN0} - V_{CSH0})\left(\frac{\alpha}{\alpha+1} - \frac{1}{\alpha+1}e^{-\frac{t}{\tau_1}}\right) + V_{CSH0}$$

Where V_{CIN0} represents the initial voltage across input capacitance (this voltage is equal to the measured input voltage), V_{CSH0} represents initial voltage across input capacitance C_{IN}. The value of initial voltage across the sampling capacitor C_{SH} depends on the specific A/D converter input scheme. Usually when sequential sampling is used, the initial voltage V_{CSH0} is equal to a previous channel voltage conversion. If a pre-sampling circuit is used, the initial voltage can be equal to V_{REFL} or V_{REFH}. In some special cases this value can be set to $(V_{REFH} - V_{REFL})/2$ to ensure lower voltage stress of the capacitor. τ

The τ_I in Eqn. 2 represents time constant of the equivalent circuit, that is:

Eqn. 3

$$\tau_1 = R_{SH}(C_{IN} + C_{SH})$$

and symbol αrepresents:

Eqn. 4

$$\alpha = \frac{C_{IN}}{C_{SH}}$$

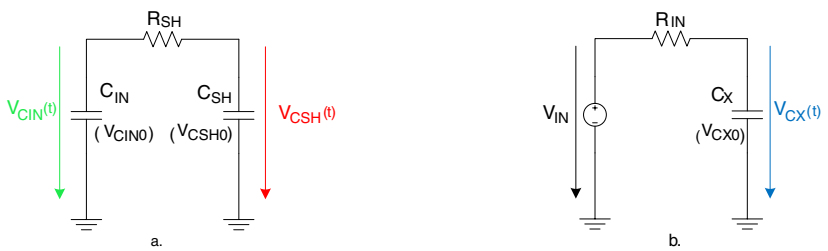

Figure 4. Equivalent circuits a.Interval I, b. Interval II

The voltage waveforms for the first interval are shown in Figure 5. The gray dashed line represents the real waveform of voltage across the input capacitor C_{IN}. This interval represents the charging of sampling capacitor C_{SH} by energy accumulated in the input capacitor (usually $V_{CIN0} = V_{IN}$). In a steady state, no energy is transferring; the current is zero, and voltages across both capacitors are equal. A mathematical expression of steady state voltage is defined using substitution $t \to \infty$ intoEqn.1 and 2:

Eqn. 5

$$v_{CX0} = (t) = (V_{CIN0} - V_{CSH0})\frac{\alpha}{\alpha+1} + V_{CSH0} = \frac{\alpha}{\alpha+1}V_{CIN0} + \frac{1}{\alpha+1}V_{CSH0}$$

From Eqn. 5 and Figure 5 it is possible to derive a magnitude of voltage drop (or peak) across the input capacitor during the first interval.

Eqn.6

$$\Delta V = V_{CIN0} - v_{CX0} = \frac{1}{\alpha+1}(V_{CIN0} - V_{CSH0})$$

Referring to Eqn.4, it can be seen that a higher ratio between input and sampling capacitance will produce a smaller voltage drop (or peak).

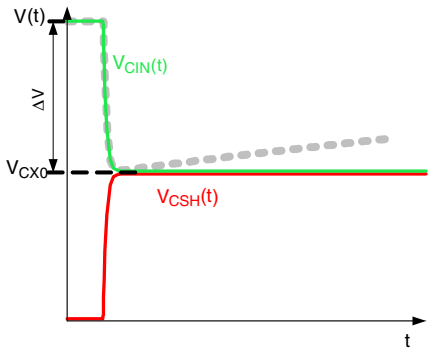

Figure 5. Time waveforms of voltages for interval I. of sampling capacitor charging

The equivalent circuit shown in fig. 4b represents the second interval of the sampling capacitor charging. Again, considering the case of a high input impedance ($R_{IN} >> R_{SH}$), and also assuming that the interval I voltage across the sampling capacitance V_{CSH} is equal to the voltage across input capacitance V_{CIN} during this time interval; the parallel connection of the input capacitor and sampling capacitor can be represented by the equivalent capacitance C_X. The initial voltage across C_X is given by the steady state voltage of the first interval, see Eqn. 5 . The time-domain waveform of the voltage across the equivalent capacitor $v_X(t)$ is shown in Figure 6 . The gray dashed line represents the real waveform of the input voltage.

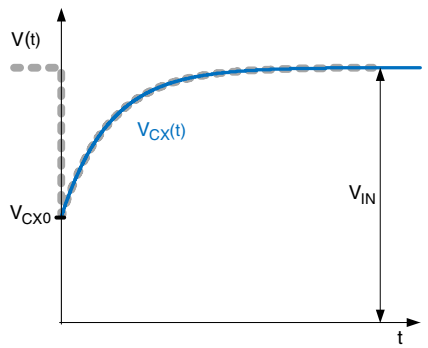

Figure 6. Time waveforms of voltage for interval II of sampling capacitor charging

A mathematical expression for the voltage across the equivalent capacitance $v_{CX}(t)$ (7) was derived by solving a system of differential equations (resulting from equivalent circuit).

eqn. 7

$$v_{CX}(t) = (V_{IN} - V_{CX0})(1 - e^{-\frac{t}{\tau_{II}}}) + V_{CX0}$$

where V_{CX0} represents the initial voltage across the equivalent capacitance, and τ_{II} represents time constant for second interval, that is:

Eqn. 8

$$\tau_{II} = R_{IN}(C_{IN} + C_{SH})$$

The basic requirement for the level of voltage across the sampling capacitance C_{SH} at the end of the sampling period (acquisition time) must be defined by following condition:

Eqn. 9

$$V_{IN} - v_{CX}(T_{AQ}) \leq \frac{V_{FSR}}{2^{(N+1)}}$$

Where T_{AQ} is an acquisition time, V_{FSR} is A/D full scale range voltage and N is the A/D resolution in number of bits. The expression on the right side of Eqn.9 represents the voltage error caused by ½ LSB of the A/D converter.

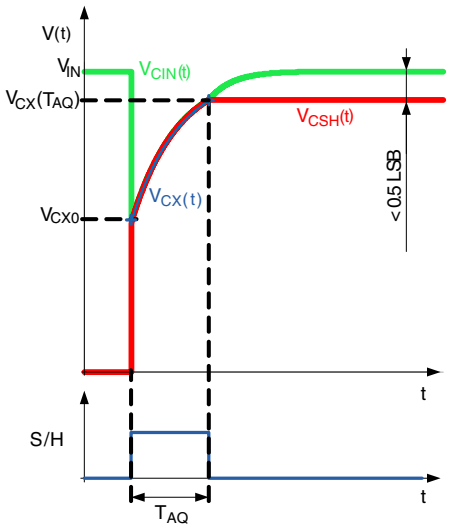

Figure 7. Voltage waveforms during acquisition time

To achieve an acceptable level of voltage across the sampling capacitance (loss of ½ LSB) the S/H switch must be switched on during acquisition time T_{AQ} given by the following equation (see also Figure 7):

Eqn.10

$$T_{AQ} \geq \tau_{11} \bullet \ln\left(\frac{(V_{IN}-V_{CSH0})}{(1+\alpha)V_{FSR}} \cdot 2^{(N+1)}\right)$$

On the other hand, when the value of input resistance is required and acquisition time is known:

Eqn. 11

$$R_{IN} \leq \frac{T_{AQ}}{(C_{IN}+C_{SH})\ln\left(\frac{(V_{IN}-V_{CSH0})}{(1+\alpha)V_{FSR}} \cdot 2^{(N+1)}\right)}$$

3 Example

In this example, the Freescale daughter board with the MC86F8257 was used and primarily intended for motor control applications. This example was set up to demonstrate proper selection and design of the external RC components required for A/D inputs. The daughter board power was supplied from a battery source. The analog and digital circuits were powered by the same power supply. Most of the recommendations were satisfied except for the inductor (or ferrite) connected between the digital and analog power pins.

NOTE

It will be necessary to allow some margin in the experimental results due to the tolerances of the passive components that were used with the neglected parasitic components.

For this example, three single-ended channels with sequential sampling mode were used. The first and the third channel inputs were grounded and the second channel was connected to 3.3 V. The PGA gain was set to 1. The conversion time was set to 2.05 us, this means that the core frequency = 60 MHz which then requires a divisor of 6 which makes an A/D clock = 10 MHz (0.1 us), that is conversion time is equal to 8.5*0.1µs+6*0.1 us+6*0.1 µs = 2.05 µs.

The conversion is initialized by a sync pulse originating from the timer every 16.67 us (sampling frequency is 60 kHz). According to the A/D timing block diagram. See, *MC56F825x/4x Reference Manual* (document number MC56F825XRM), the acquisition time of the sample and hold circuit is half of the A/D clock, that is T_{AQ} = 50 ns. The A/D resolution in number of bits is 12. Considering the worst case (the second channel), the measured input voltage V_{IN} is set to V_{REFH}, that is V_{IN} =

3.3 V and initial voltage across sampling capacitance is V_{REFL}, that is V_{CSH0} = 0V (from the previous measurement). The full scale range is equal to 3.3 V, that is V_{FSR} = 3.3 V. With respect to the data sheet *MC56F825x/MC56F824x Digital Signal Controller* (document MC56F825X) the capacitance of the sampling capacitor for 1x gain of PGA is 1.4 pF. Capacitance is directly proportional to the PGA gain. All other parasitic capacitances were neglected. Following the recommendation for correct operation of the controller, no less than 33 p capacitor must be connected at each of the used A/D inputs. In a calculation minimum recommended resistance 10Ω is considered.

In the aggregate:

- T_{AQ} = 50 ns
- C_{IN} = 33 pF (minimum)
- C_{SH} = 1.4 pF
- V_{IN} = 3.3 V
- V_{CSH0} = 0 V
- V_{FSR} = 3.3 V
- N = 12

Using Eqn.11 for this example input resistance R_{IN}must not exceed the value given by:

$$R_{IN} \leq \frac{50nf}{(33pF-1.4pF)In(\frac{1}{1+\alpha}2^{13})} = 250\Omega$$

The minimum recommended value of input resistance (10Ω) is satisfied. The value of α is given by Eqn. 4, That is:

$$\alpha = \frac{C_{IN}}{C_{SH}} = \frac{33}{1.4} = 23.6$$

The magnitude of the voltage drop (peak) across the input capacitor during sampling is defined by Eqn. 6 and in this case it is:

$$\Delta V = \frac{1}{\alpha+1}(V_{CIN0} - V_{CSH0}) = \frac{1}{\alpha+1}(3.3-0) = 134mV$$

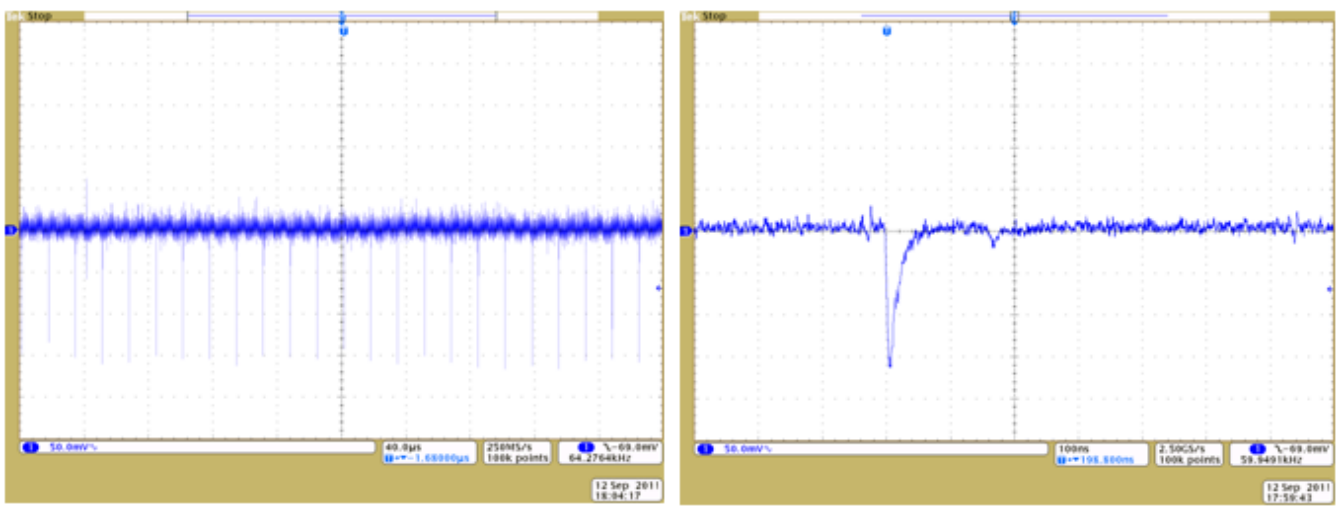

Figure 8. Correct acquisition time setting – digital result 4087 (time scale: left side 40 µs, right side 100 ns)

In Figure 8 the voltage drop across the input capacitor (taking into account the S/H circuit simplifications and all component tolerances) is big but does not cause any error in the digital output of the A/D. The digital result for the second channel measured by FreeMASTER is 4087.

A common mistake related to external RC component design is to increase input impedance by R_{IN} to reduce current or to make impedance isolation between the measured source and A/D. Now the same case is considered, except that the input resistance R_{IN} will be increased to10kΩ to demonstrate insufficient charging of sampling capacitor C_{SH} during the acquisition time. As can be seen in detail in Figure 9, the acquisition time of 50 ns is not sufficient to enable the sampling

capacitance to charge correctly. The condition defined in Eqn. 9 is not satisfied and consequently, a big error in the second channel A/D digital output should be expected. The digital result for the second channel measured by FreeMASTER in this case was 3780. The result represents significant inaccuracy in the measurement. To get correct results, it is necessary to follow Eqn.10 and set the acquisition time higher than:

$$T_{AQ} \geq t_{II} \cdot \ln\left(\frac{(V_{IN} - V_{CSH0})}{(1+\alpha)V_{FSR}} \cdot 2^{(N+1)}\right) \geq 2\mu s$$

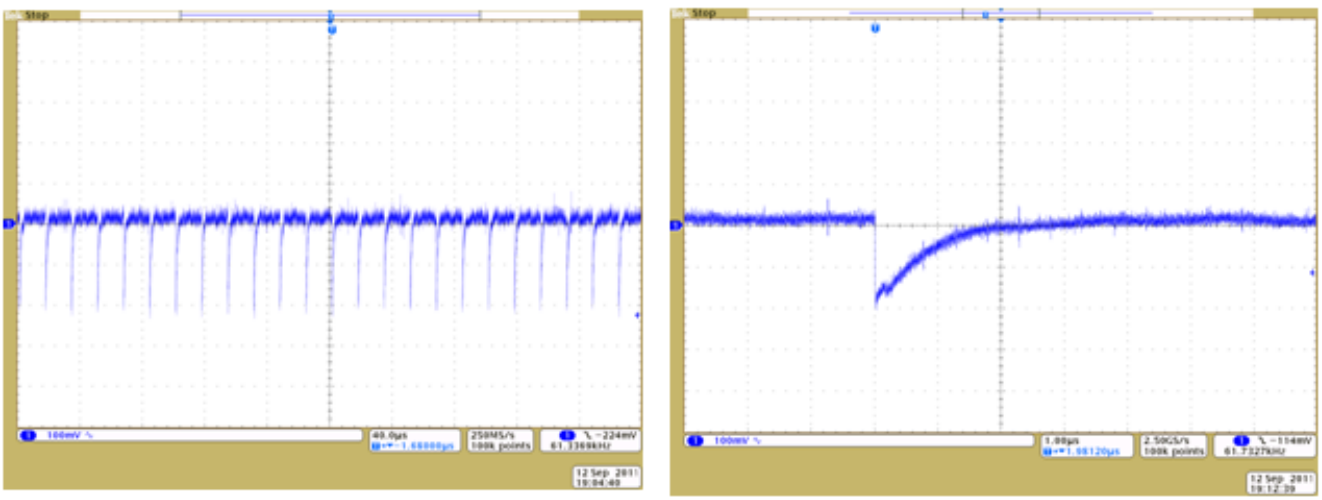

Figure 9. Incorrect acquisition time setting – digital result 3780 (time scale: left side 40 µs, right side 1 µs)

4 Conclusion

During the acquisition time T_{AQ}, the sampling capacitor C_{SH} must be charged to an acceptable minimal portion of the voltage level of the measured input voltage. In general, the deviation from the measured input voltage at the end of acquisition time must not exceed 0.5 LSB of the full scale range. If higher input impedance R_{IN} is used (high external component time constant) the sampling capacitor C_{SH} is quickly charged at first by the energy of the external input capacitor C_{IN} (much lower input components time constant). The process of charging the sampling capacitance causes a voltage drop (or peak) across external input capacitor C_{IN}. The subsequent process of charging the sampling capacitor is much slower due to this higher input impedance. The acquisition time must be properly set while considering the time constant of the sampling capacitor charging. Hence, the external RC components essentially affect the AD conversion accuracy. To achieve optimal performance from an A/D, special care must be taken to select and design appropriate external RC components, in addition to meeting all other requirements, see *MC56F825x/4x Reference Manual* (document number MC56F825XRM) and *MC56F825x/MC56F824xDigital Signal Controller* (document MC56F825X).

References

MC56F825x/4x Reference Manual (document number MC56F825XRM), Rev. 2, 10/2010.

MC56F825x/MC56F824x Digital Signal Controller technical data (document MC56F825X), Rev. 3.

Nyquist–Shannon sampling theorem

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