Basic Electronics Engineering (Spring 2024)

Resources of PPT:

- www.google.com

- Digital Design, 4th Edition
  M. Morris Mano and Michael D. Ciletti

Analog Electronics

Reference Book:

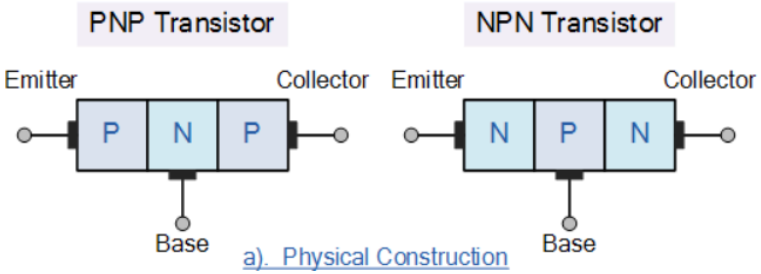
1. **R. BOYLESTAD and L. NASHELSKY, “Electronic Devices And Circuit Theory”, Prentice Hall.**
2. **Sedra and Smith, “Microelectronic Circuits”, Oxford University Press**

BJT

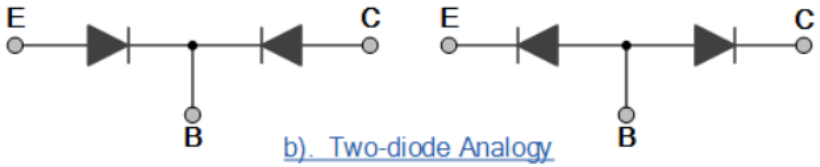
Forward Bias: + -

Reverse Bias: - +

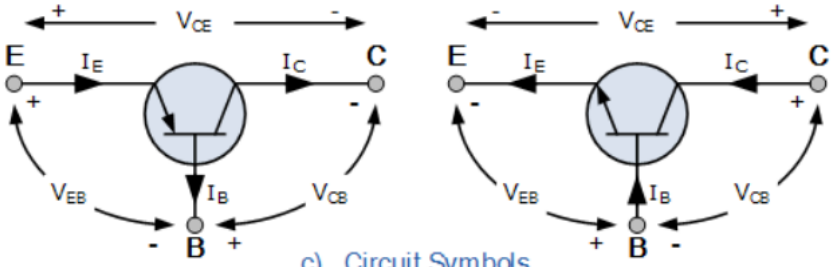
Bipolar Junction Transistor (BJT) Construction:



a). Physical Construction

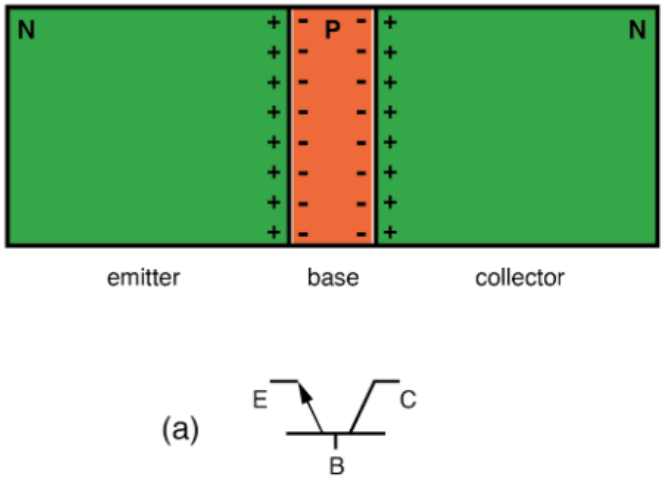


b). Two-diode Analogy

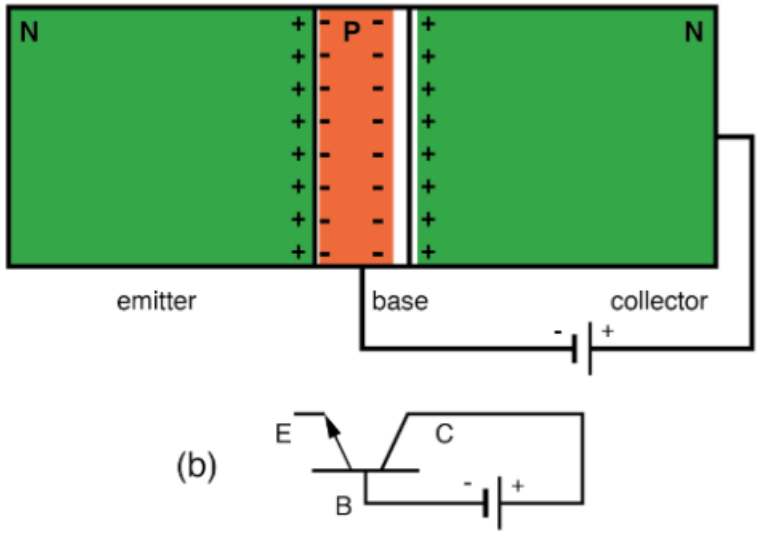


c). Circuit Symbols

BJT

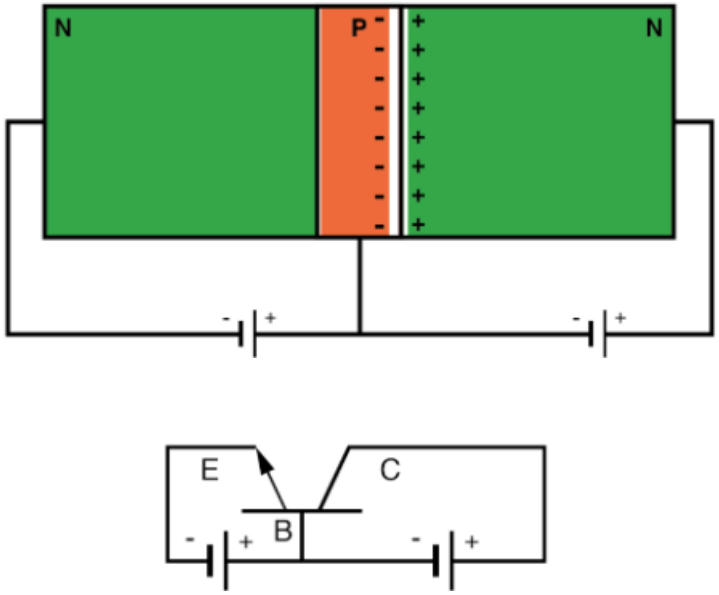


(a) NPN junction bipolar transistor with no bias voltage.

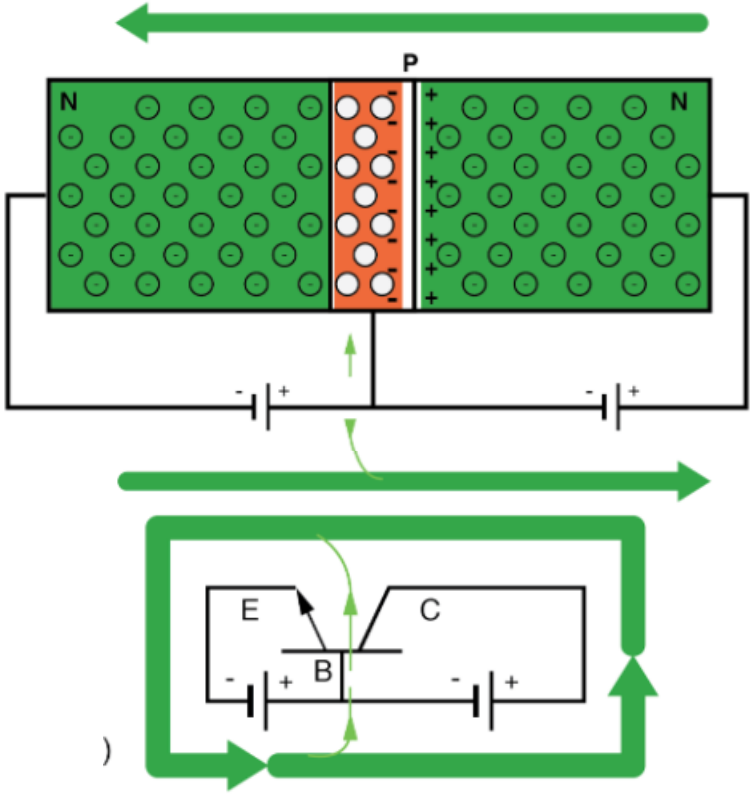


(b) Apply reverse bias to collector base junction.

BJT

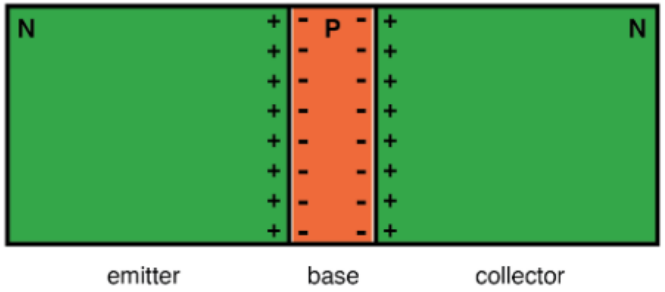


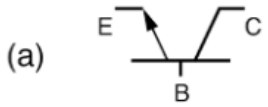
(c) Adding forward bias to base-emitter junction



(d) results in a small base current and large emitter and collector currents.

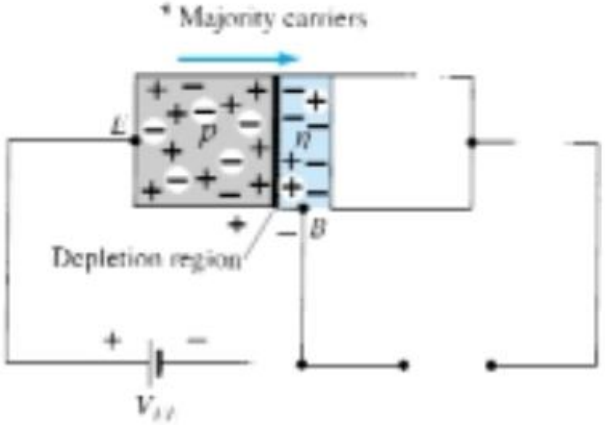
BJT



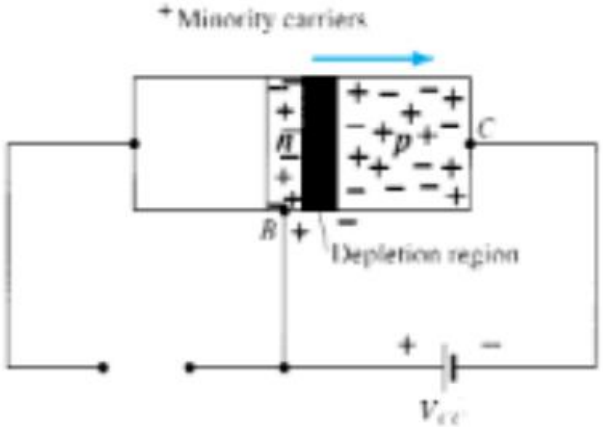


Junction type	Applied voltages	Junction bias		Mode
		B–E	B–C	
NPN	E < B < C	Forward	Reverse	Forward-active
	E < B > C	Forward	Forward	Saturation
	E > B < C	Reverse	Reverse	Cut-off
	E > B > C	Reverse	Forward	Reverse-active
PNP	E < B < C	Reverse	Forward	Reverse-active
	E < B > C	Reverse	Reverse	Cut-off
	E > B < C	Forward	Forward	Saturation
	E > B > C	Forward	Reverse	Forward-active

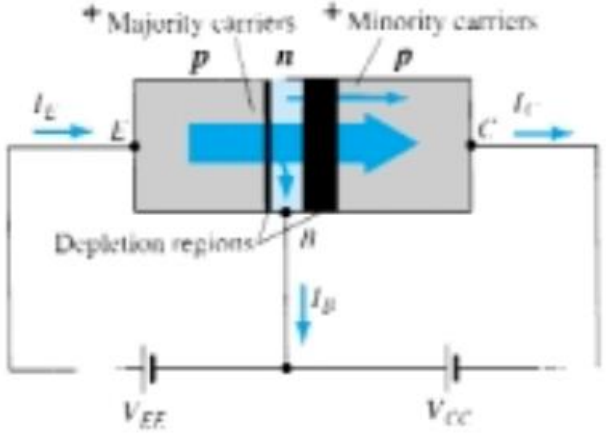
BJT in Common Base Configuration



(a) Forward-biased junction of a *pnp* transistor.



(b) Reverse-biased junction of a *pnp* transistor

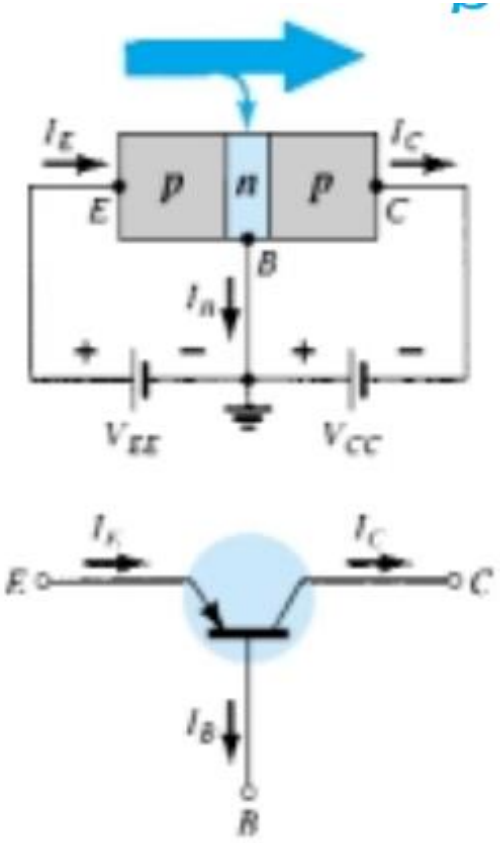


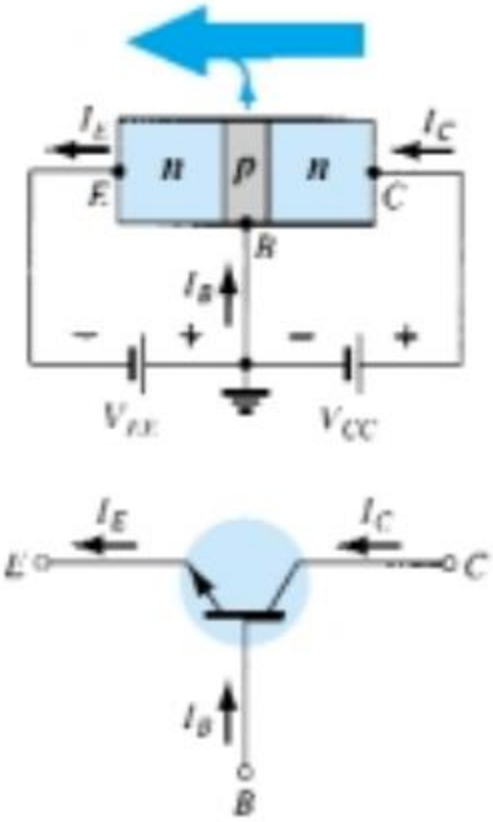
© Majority and minority carrier flow of a *pnp* transistor.

$$I_E = I_C + I_B$$

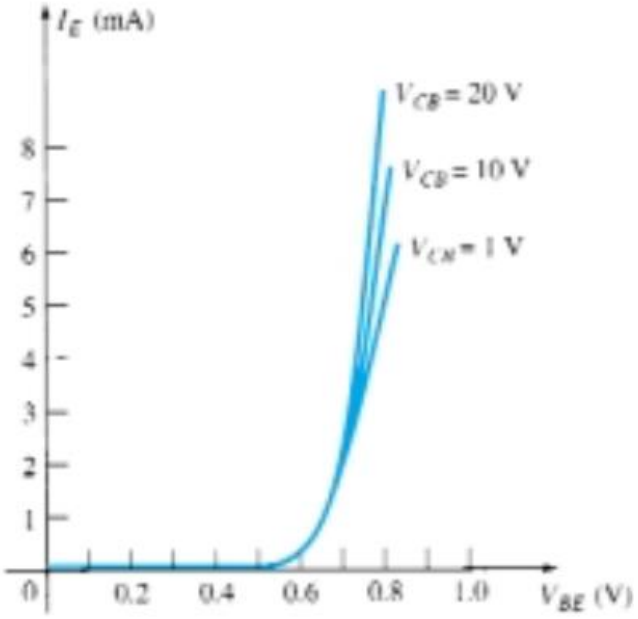
$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$$

BJT in Common Base Configuration

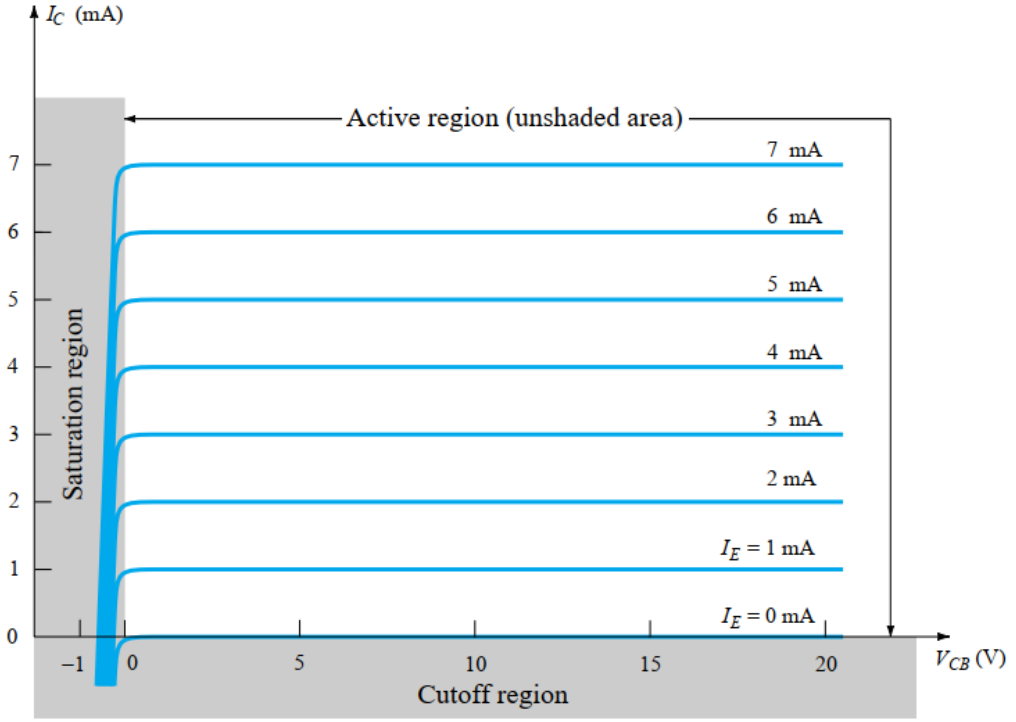




BJT in Common Base Configuration

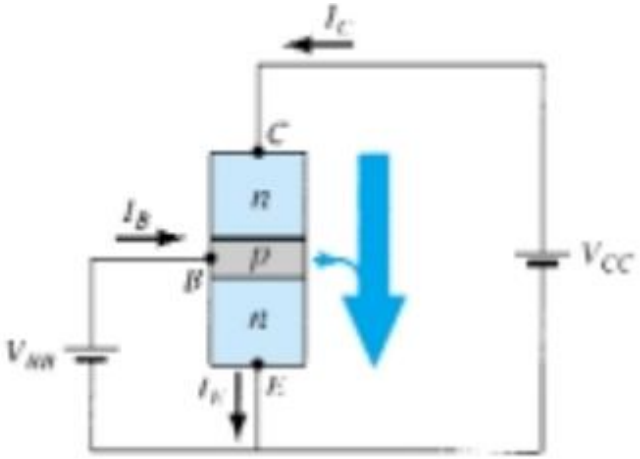


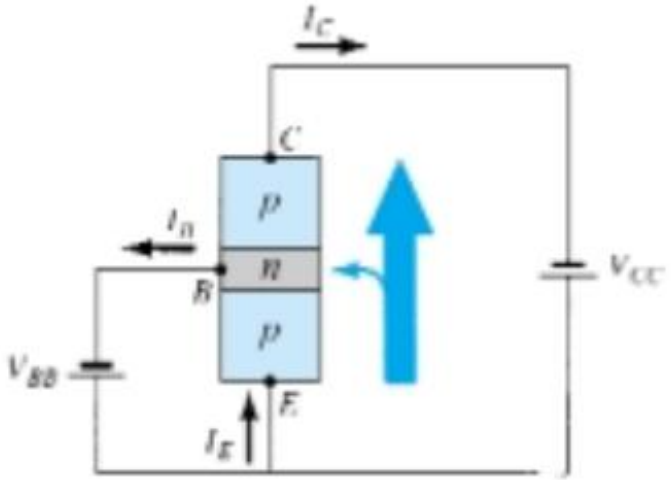
(a) Input or driving point characteristics for a common-base silicon transistor amplifier.

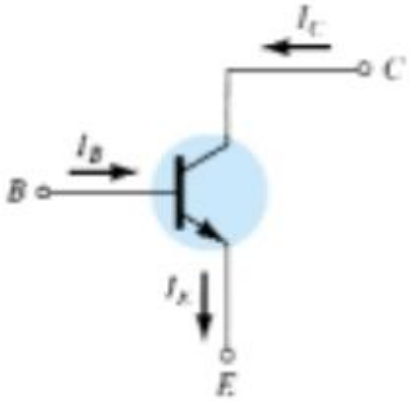


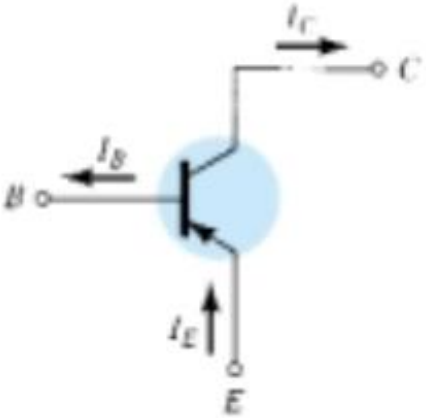
(b) Output or collector characteristics for a common-base transistor amplifier.

BJT in Common Emitter Configuration

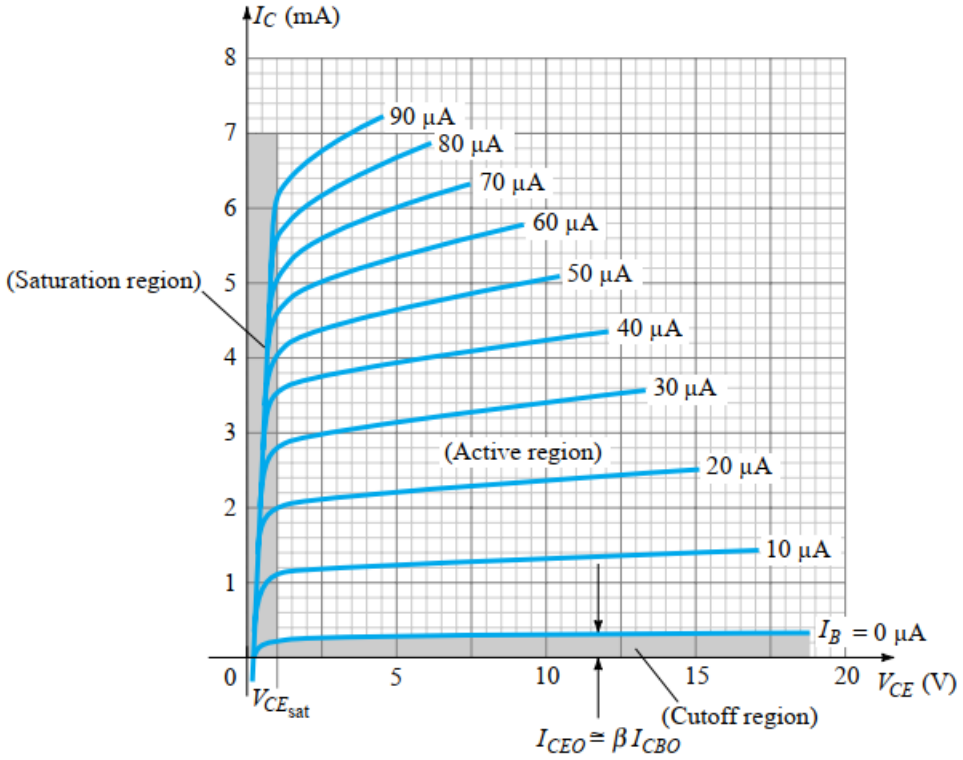


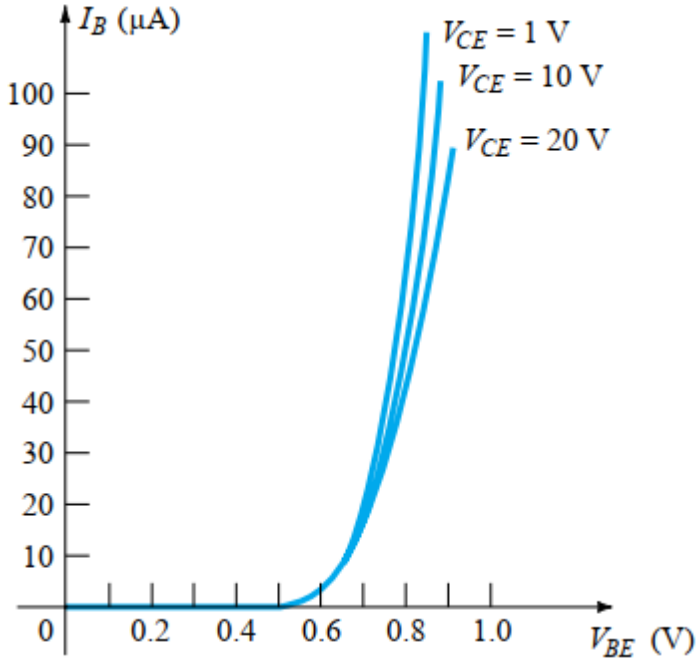




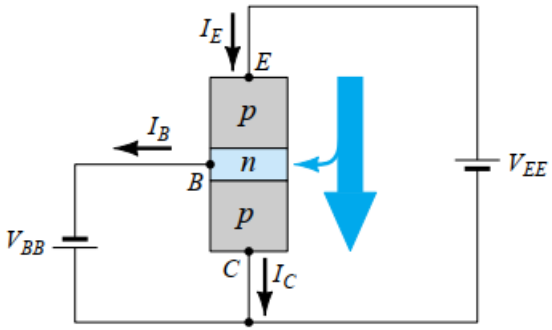


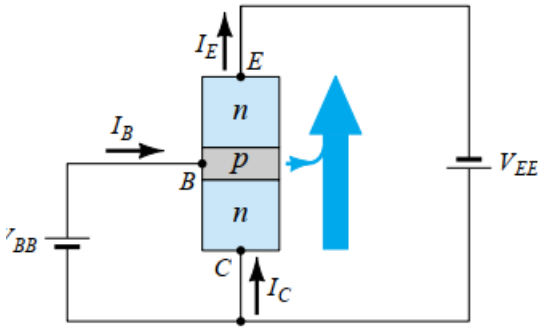
BJT in Common Emitter Configuration

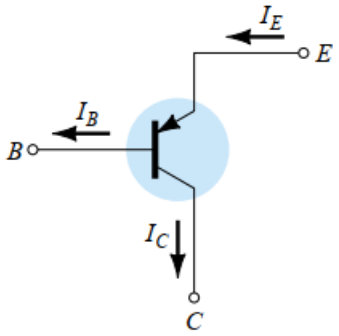


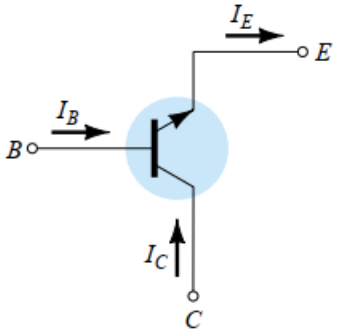


BJT in Common Collector Configuration

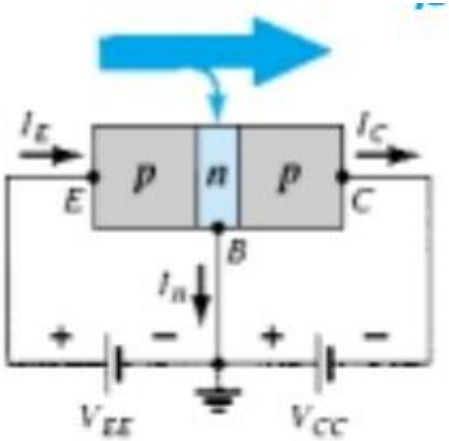




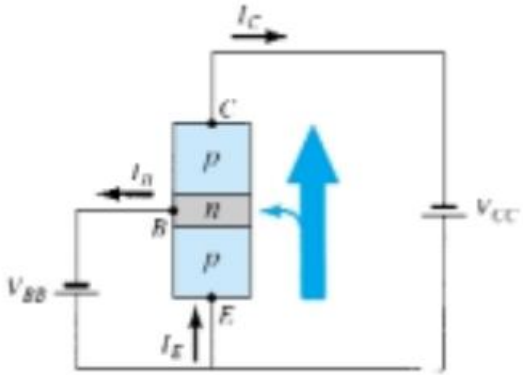




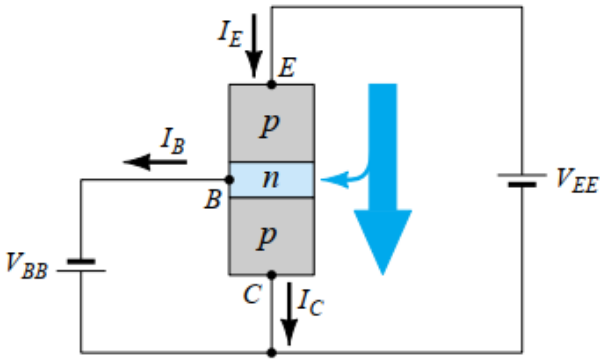
BJT in CB, CE and CC Configuration



(a) Common Base (CB)



(b) Common Emitter (CE)



(c) Common Collector (CC)

$$I_E = I_C + I_B$$

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

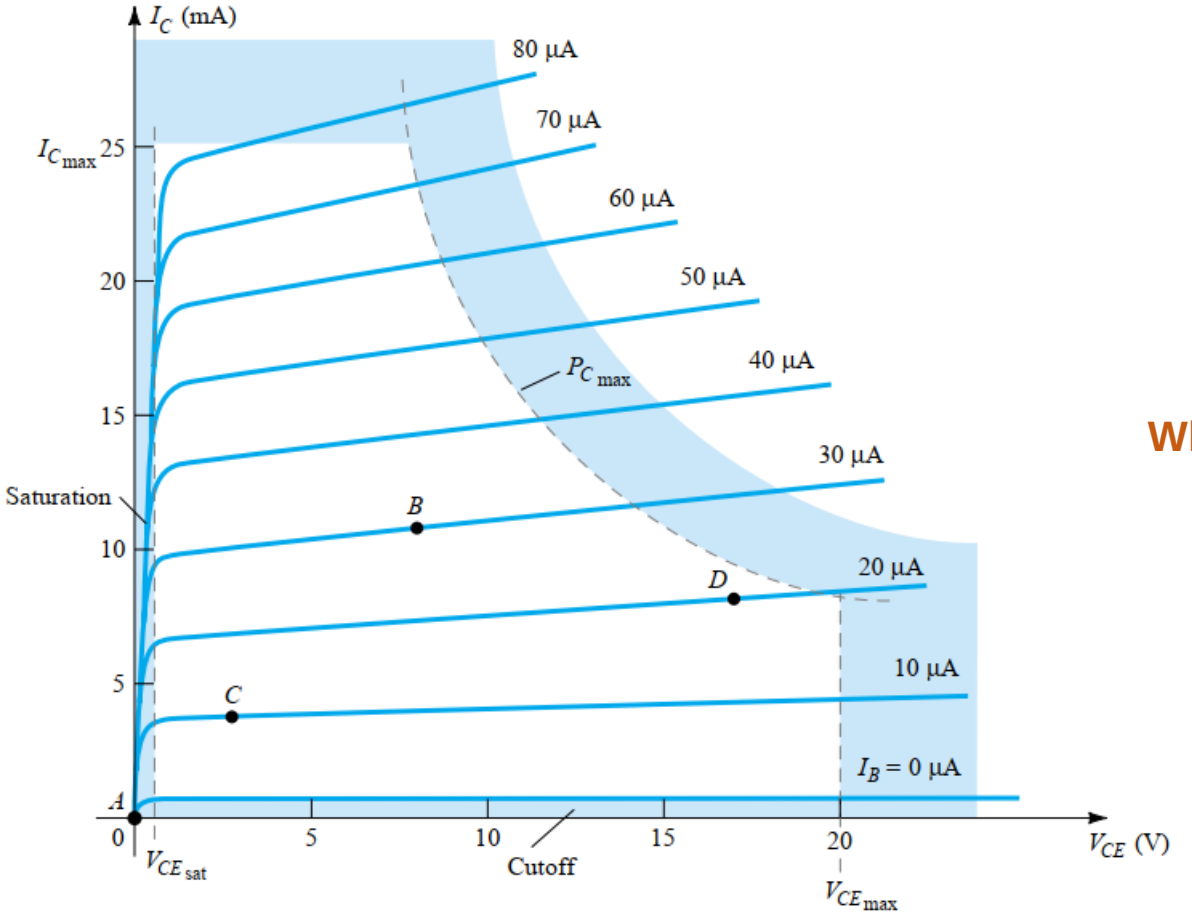
$$\alpha_{\text{dc}} = \frac{I_C}{I_E}$$

$$\alpha_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}\ =\ \text{constant}}$$

$$\beta_{\text{dc}} = \frac{I_C}{I_B}$$

$$\beta_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}}$$

BJT Biasing



Why Biasing is needed?

Fig.: Various operating points within the limits of operation of a transistor.

BJT FIXED-BIAS CIRCUIT

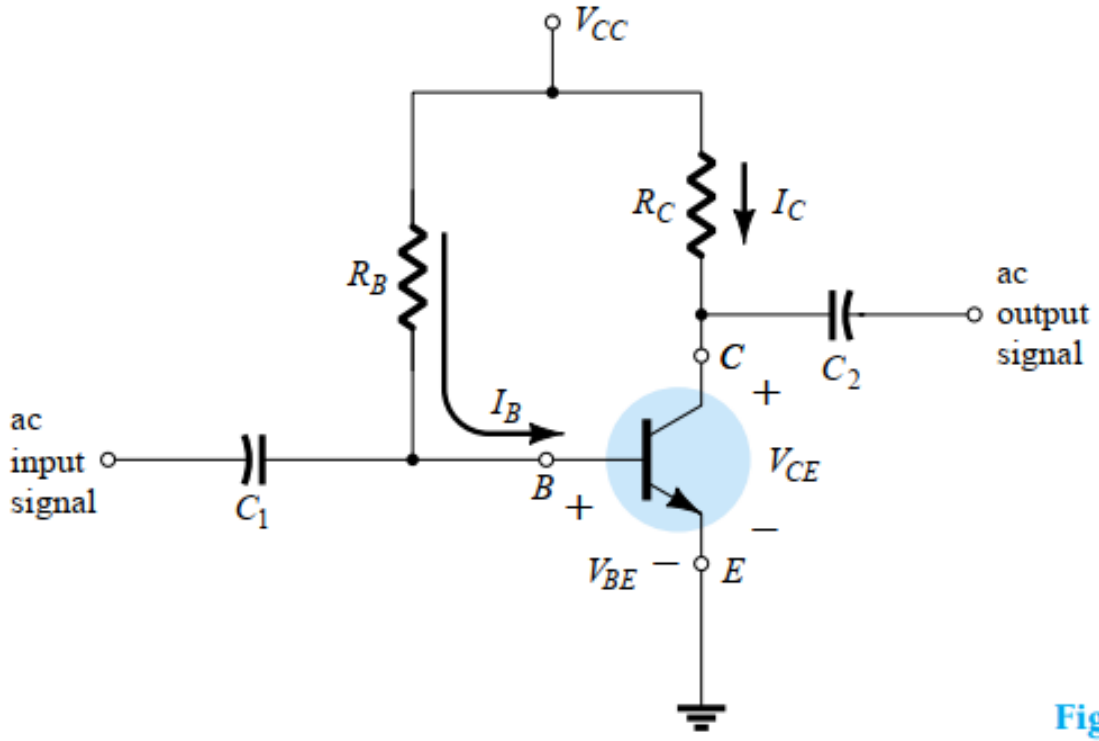


Figure 4.2 Fixed-bias circuit.

BJT FIXED-BIAS CIRCUIT

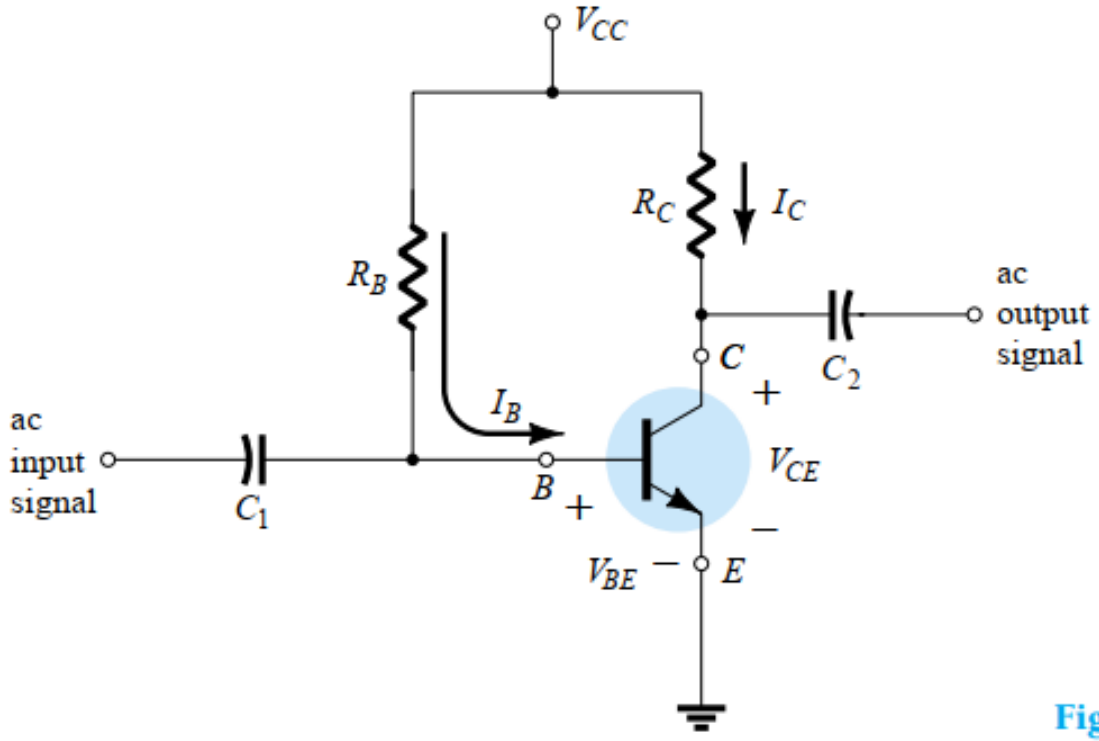


Figure 4.2 Fixed-bias circuit.

BJT FIXED-BIAS CIRCUIT

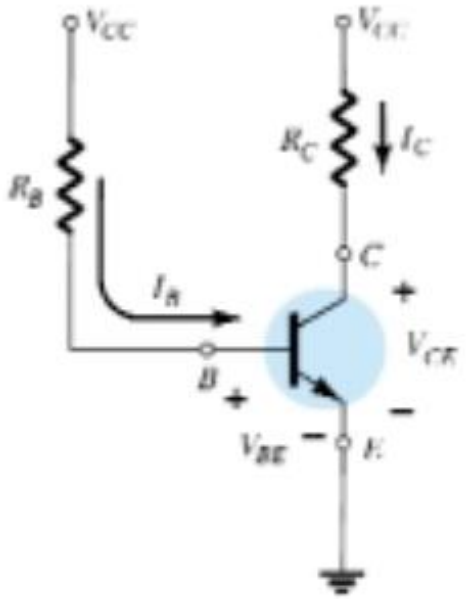


Fig.: dc equivalent circuit.

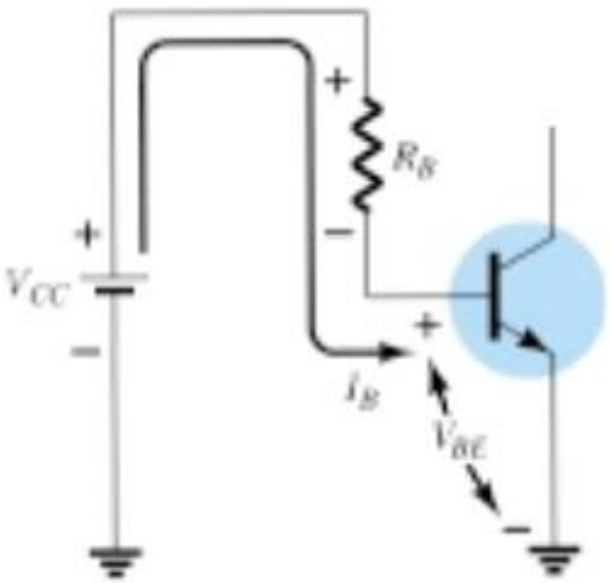


Fig: Base–emitter loop

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

BJT FIXED-BIAS CIRCUIT

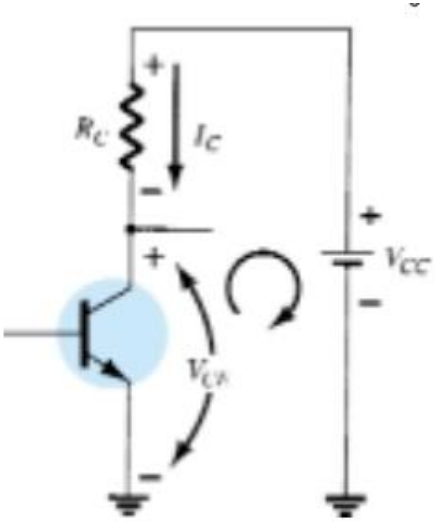
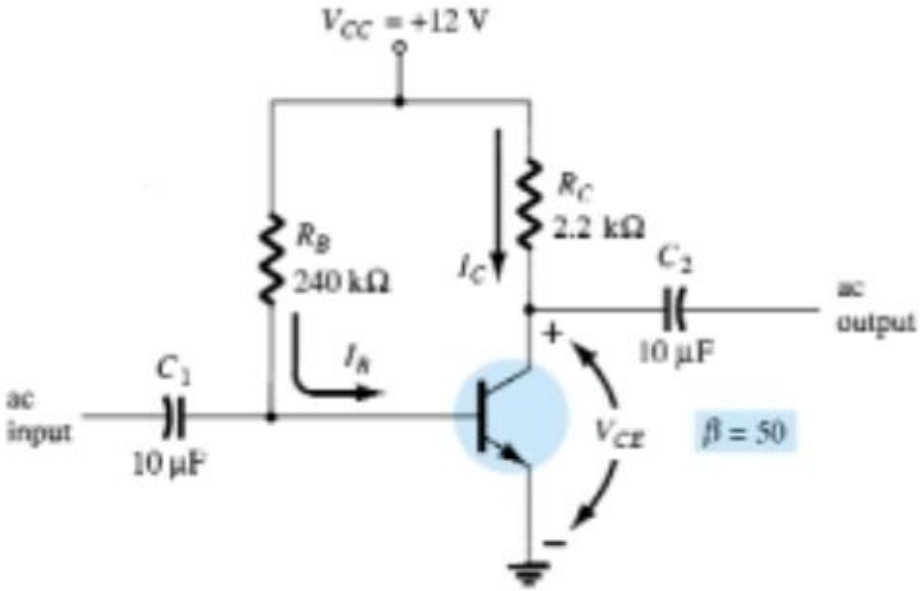


Fig: Collector–emitter loop.

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$



Determine the following

(a) I_{B_Q} and I_{C_Q}.

(b) V_{CE_Q}.

(c) V_B and V_C.

(d) V_{BC}.

BJT FIXED-BIAS CIRCUIT

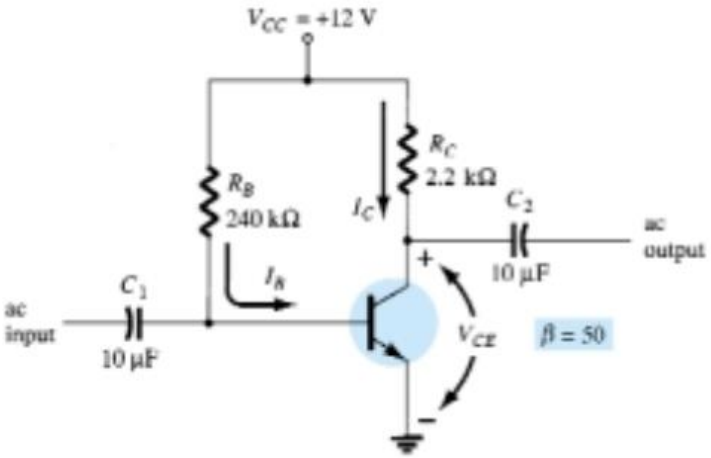


Figure 4.7 dc fixed-bias circuit for Example 4.1.

Solution

(a) Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

(b) Eq. (4.6): $$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

(c) $V_B = V_{BE} = \mathbf{0.7\ V}$

$V_C = V_{CE} = \mathbf{6.83\ V}$

(d) Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

BJT FIXED-BIAS CIRCUIT

Load-Line Analysis

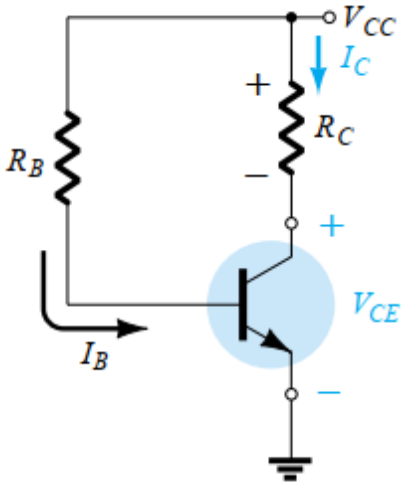
$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC} - (0)R_C$$

$$V_{CE} = V_{CC}\big|_{I_C = 0\ \text{mA}}$$

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{ce} = 0\ \text{V}}$$



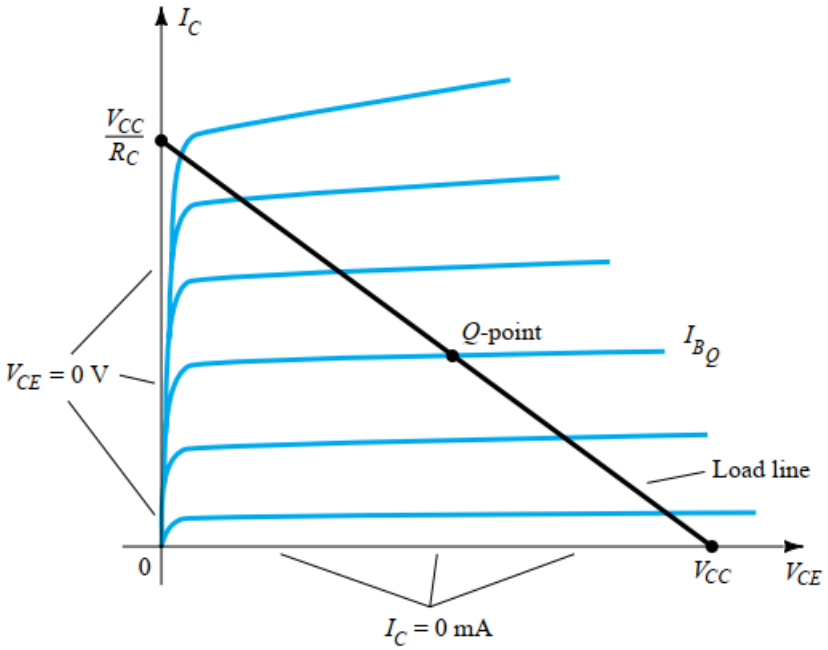


Fig: Fixed-bias load line

BJT EMITTER-STABILIZED BIAS

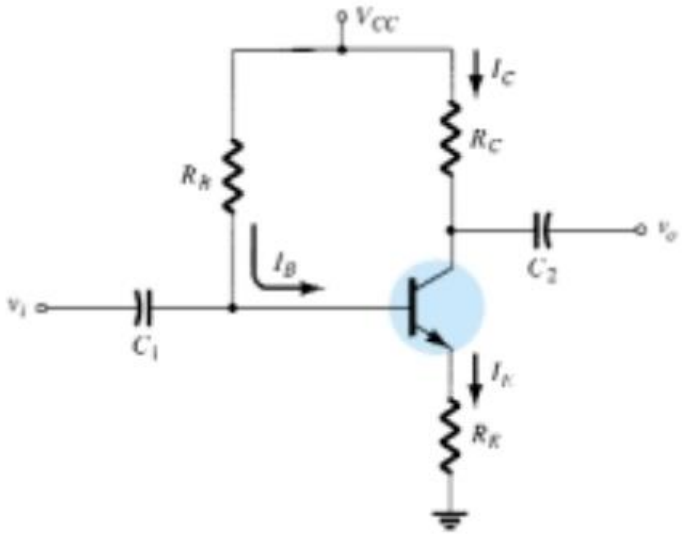


Fig: BJT bias circuit with emitter resistor.

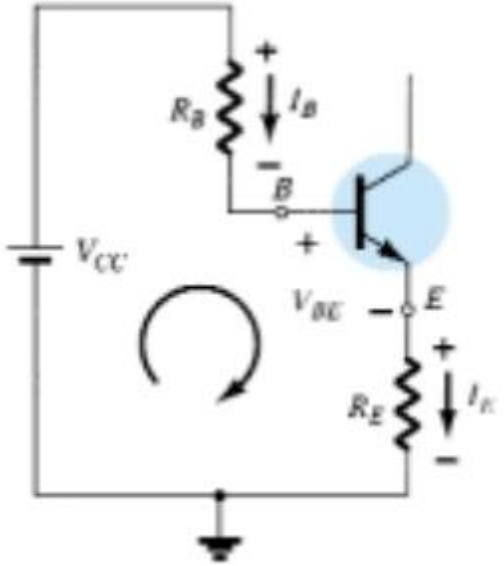


Fig: Base–emitter loop

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term ($1+\beta$)R_E.

BJT EMITTER-STABILIZED BIAS

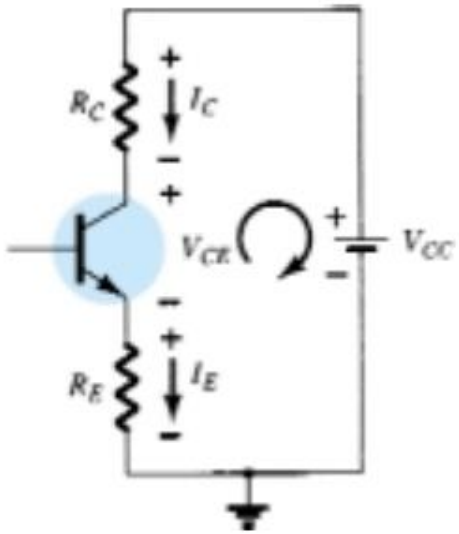


Fig: Collector–emitter loop

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E$$

$$V_C = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_B R_B$$

$$V_B = V_{BE} + V_E$$

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.

BJT EMITTER-STABILIZED BIAS

Load-Line Analysis

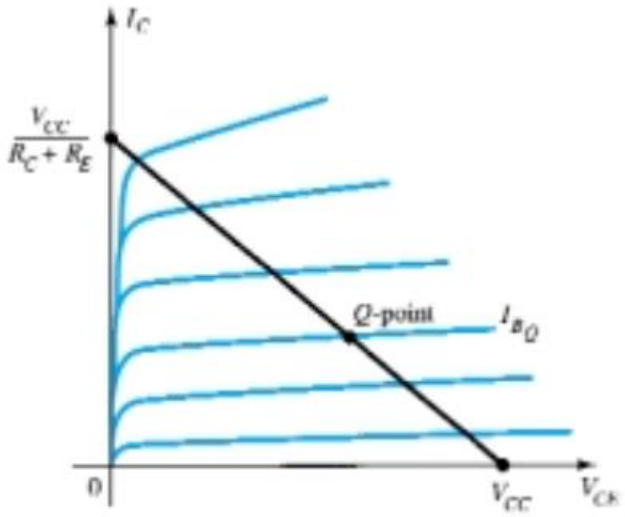


Fig: Load line for the emitter-bias configuration.

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = V_{CC}\big|_{I_C = 0\ \text{mA}}$$

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0\ \text{V}}$$

For the emitter bias network of Fig. 4.22, determine:

(a) I_B.
(b) I_C.
(c) V_{CE}.
(d) V_C.
(e) V_E.
(f) V_B.
(g) V_{BC}.

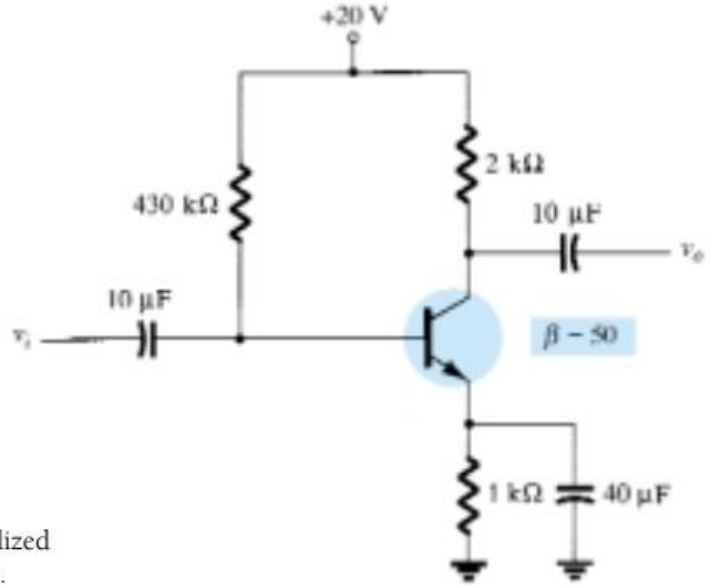


Figure 4.22 Emitter-stabilized bias circuit for Example 4.4.

BJT EMITTER-STABILIZED BIAS

(a) Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$

$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

(b) $$I_C = \beta I_B$$

$$= (50)(40.1\ \mu\text{A})$$

$$\cong \mathbf{2.01\ mA}$$

(c) Eq. (4.19): $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$

$$= \mathbf{13.97\ V}$$

(d) $$V_C = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$

$$= \mathbf{15.98\ V}$$

(e) $$V_E = V_C - V_{CE}$$

$$= 15.98\text{ V} - 13.97\text{ V}$$

$$= \mathbf{2.01\ V}$$

(f) $$V_B = V_{BE} + V_E$$

$$= 0.7\text{ V} + 2.01\text{ V}$$

$$= \mathbf{2.71\ V}$$

(g) $$V_{BC} = V_B - V_C$$

$$= 2.71\text{ V} - 15.98\text{ V}$$

$$= \mathbf{-13.27\ V}$$ (reverse-biased as required)

BJT Voltage Divider BIAS

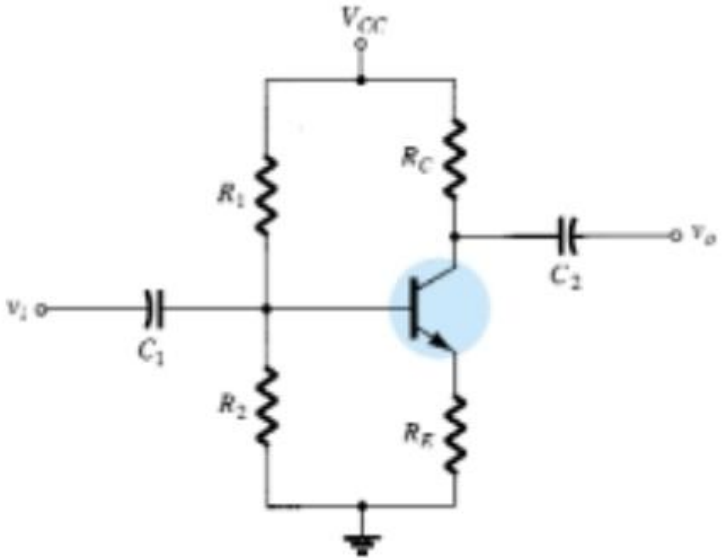


Figure 4.25 Voltage-divider bias configuration.

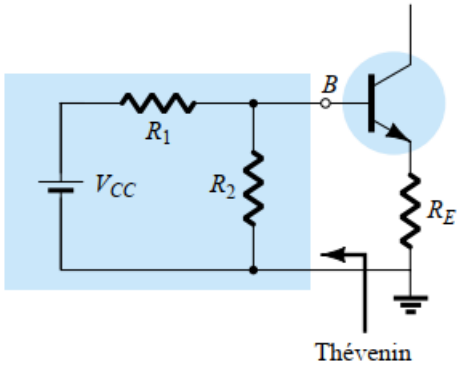
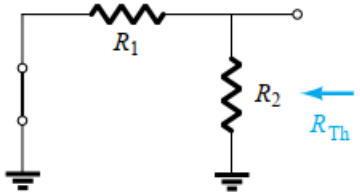
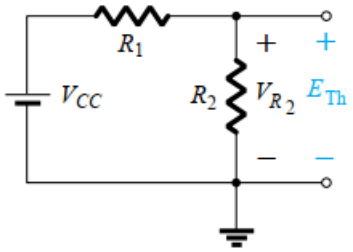


Figure 4.27 Redrawing the input side of the network of Fig. 4.25.

BJT Voltage Divider BIAS



$$R_{Th} = R_1 \| R_2$$



$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

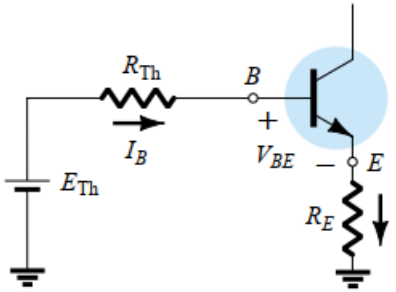


Figure 4.30 Inserting the Thévenin equivalent circuit.

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

BJT Voltage Divider BIAS

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE}=0\text{ V}}$$

$$V_{CE} = V_{CC}|_{I_C=0\text{ mA}}$$

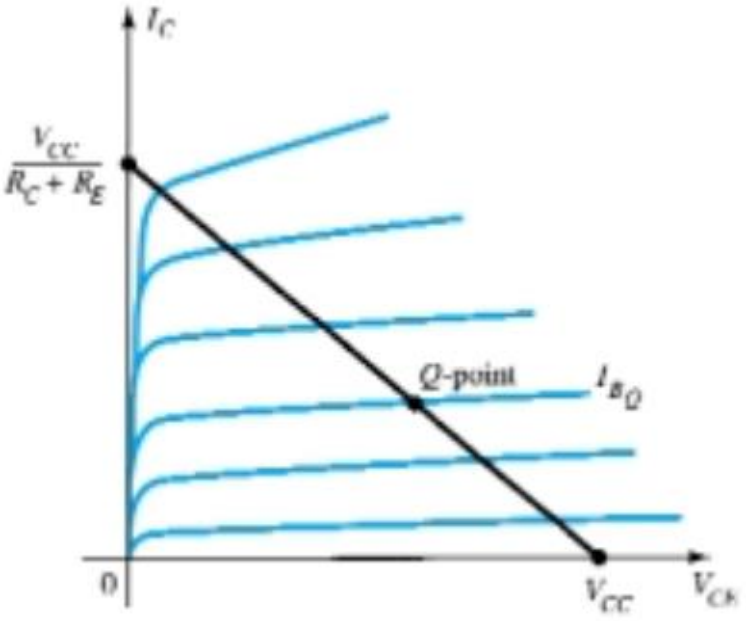


Figure 4.24 Load line for the emitter-bias configuration.

BJT VOLTAGE FEEDBACK BIAS

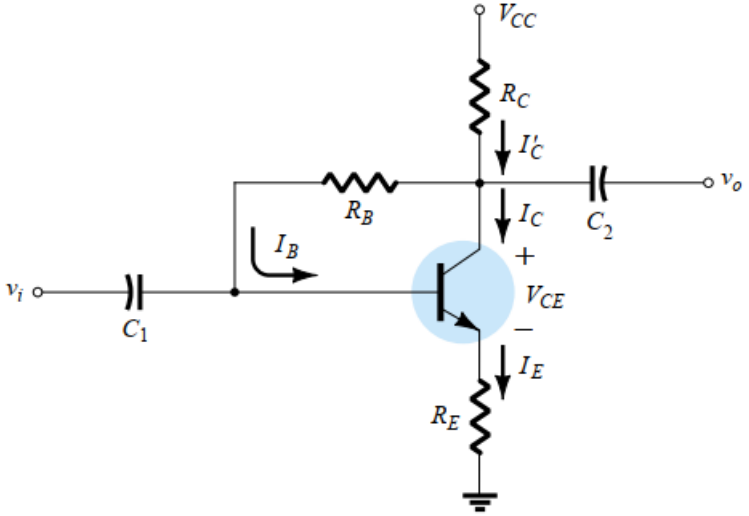


Fig: BJT with voltage feedback bias

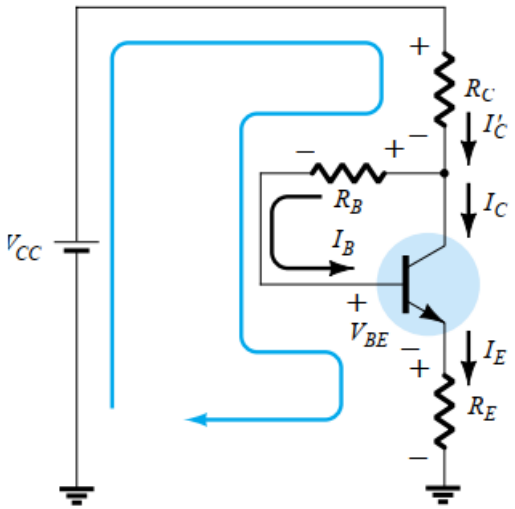


Fig: Base–emitter loop

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I'_C \cong I_C = \beta I_B \text{ and } I_E \cong I_C$$

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

BJT VOLTAGE FEEDBACK BIAS

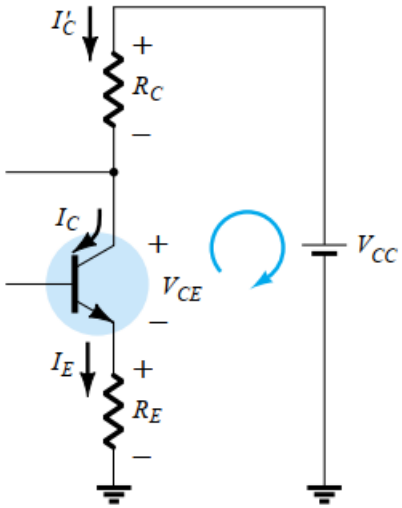


Fig: Collector–emitter loop

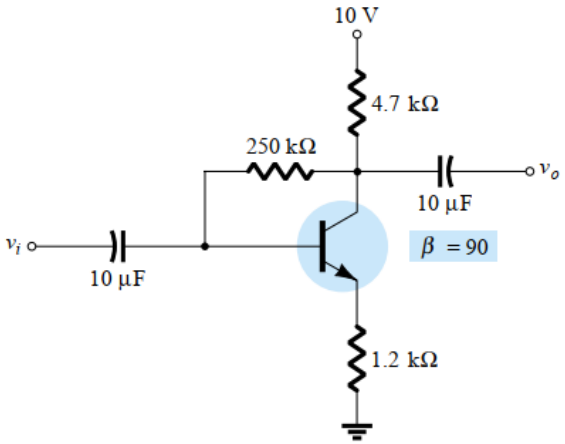
$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$



Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega}$$

$$= 11.91\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A})$$

$$= \mathbf{1.07\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 10\text{ V} - 6.31\text{ V}$$

$$= \mathbf{3.69\ V}$$

BJT Stability Analysis

Stability Factors, $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

$S(I_{CO})$: EMITTER-BIAS CONFIGURATION

For the emitter-bias configuration, an analysis of the network will result in

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{(\beta + 1) + R_B/R_E}$$

For the fixed-bias configuration,

$$S(I_{CO}) = \beta + 1$$

Voltage-Divider Bias Configuration

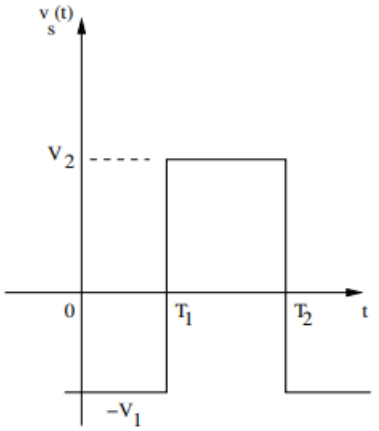
$$S(I_{CO}) = (\beta + 1)\frac{1 + R_{Th}/R_E}{(\beta + 1) + R_{Th}/R_E}$$

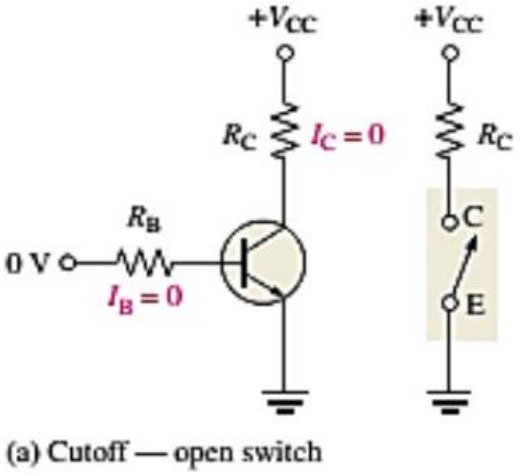
Feedback-Bias Configuration

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_C}{(\beta + 1) + R_B/R_C}$$

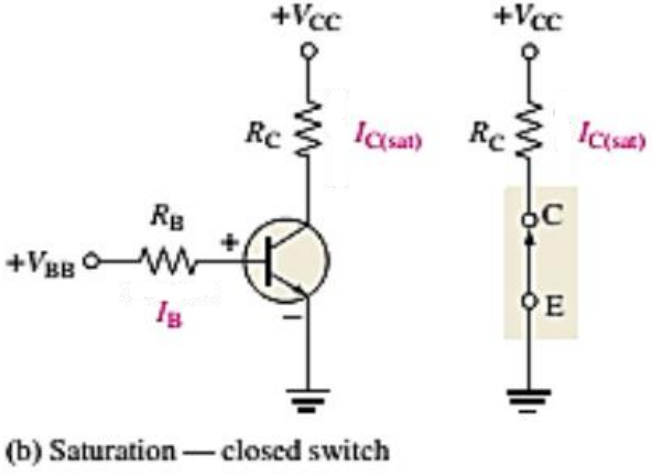
BJT AS SWITCHING CIRCUIT

A BJT can be used as a switching device in logic circuits to turn on or off current to a load. As a switch, the transistor is normally in either cutoff (load is OFF) or saturation (load is ON).

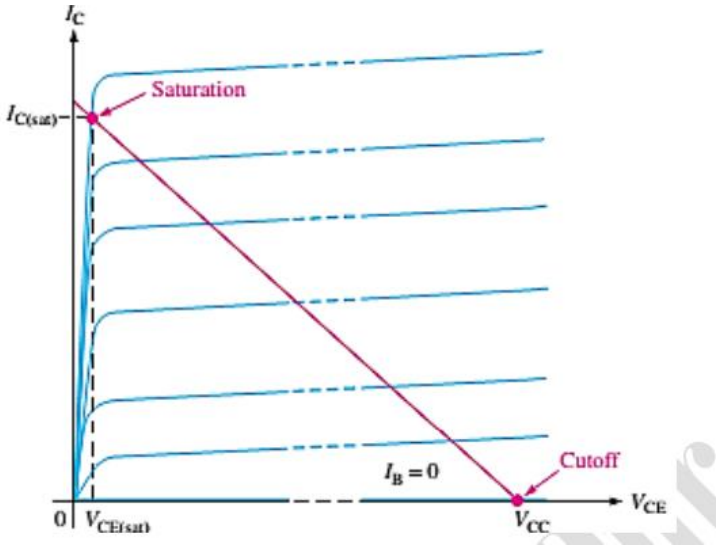




(a) Cutoff — open switch



(b) Saturation — closed switch

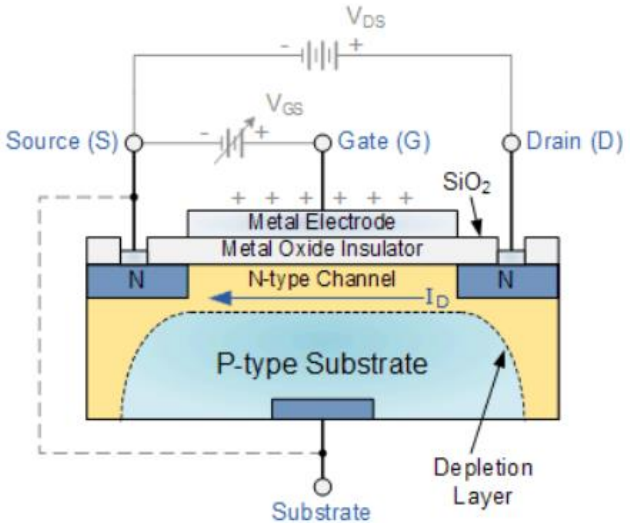


Switches between cut-off and saturation region.

MOSFET

MOSFET (*m*etal-*o*xide-*s*emiconductor-*f*ield-*e*ffect *t*ransistor) has four components:

- Source (S)
- Drain (D)
- Gate (G)
- Body (B) terminals



The body (B) is frequently connected to the source terminal, reducing the terminals to three. It works by varying the width of a channel along which charge carriers flow (electrons or holes).

The charge carriers enter the channel at the source and exit via the drain. The width of the channel is controlled by the voltage on an electrode called Gate which is located between the source and the drain. It is insulated from the channel near an extremely thin layer of metal oxide.

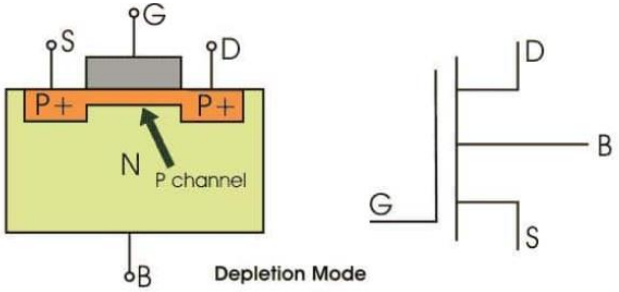
- Depletion Type – the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.

- Enhancement Type – the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.

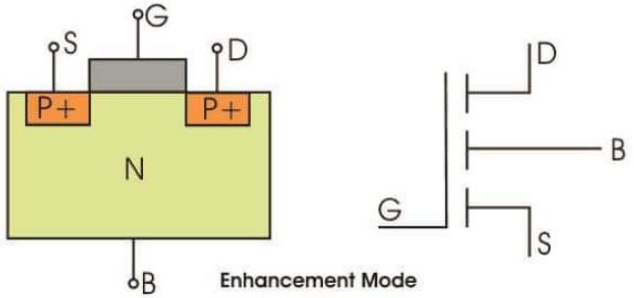
MOSFET

There are four types of MOSFET:

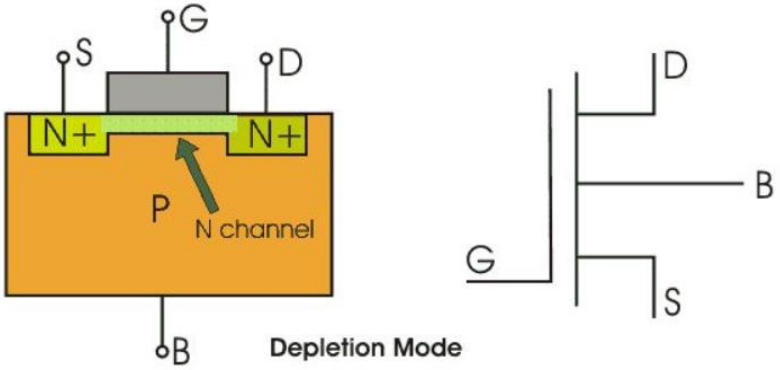
1. P-Channel Depletion MOSFET
2. P-Channel Enhancement MOSFET
3. N-Channel Depletion MOSFET
4. N-Channel Enhancement MOSFET Drain (D)



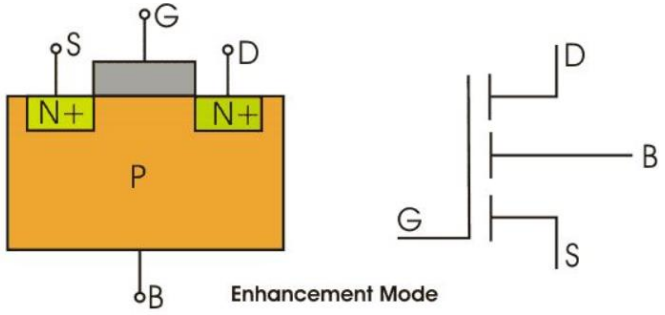
(a) P-Channel Depletion MOSFET



(b) P-Channel Enhancement MOSFET



(a) N-Channel Depletion MOSFET



(b) N-Channel Enhancement MOSFET

N-Channel Depletion MOSFET

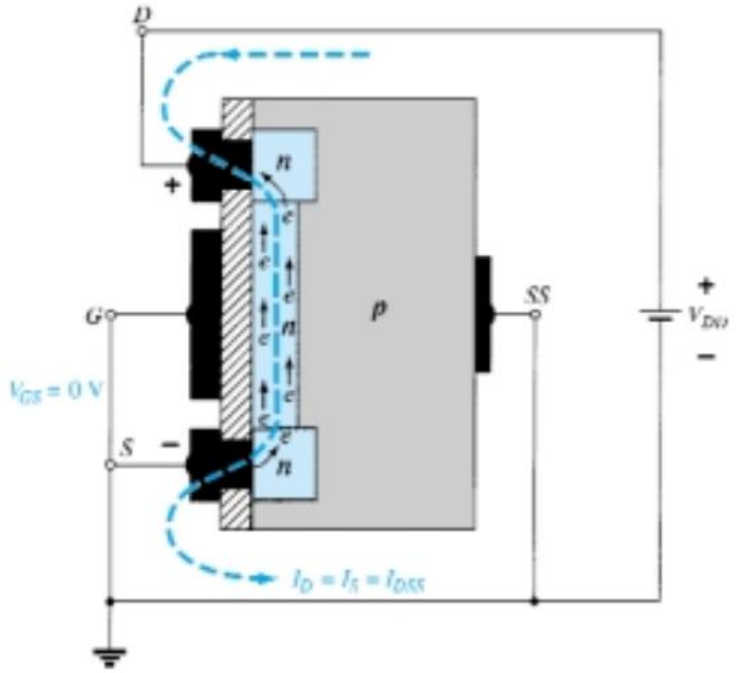


Fig: n-Channel depletion-type MOSFET with V_{GS}=0 V and an applied voltage V_{DD}

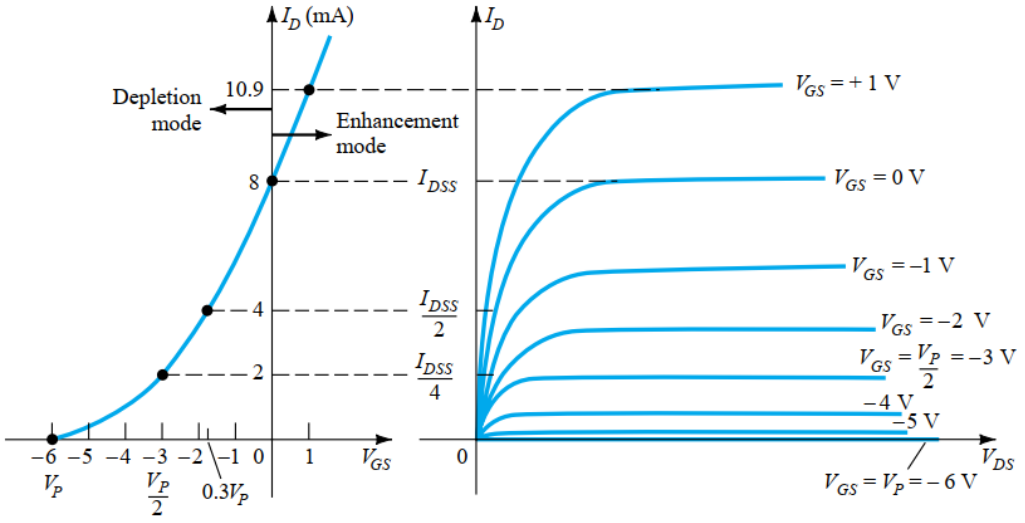
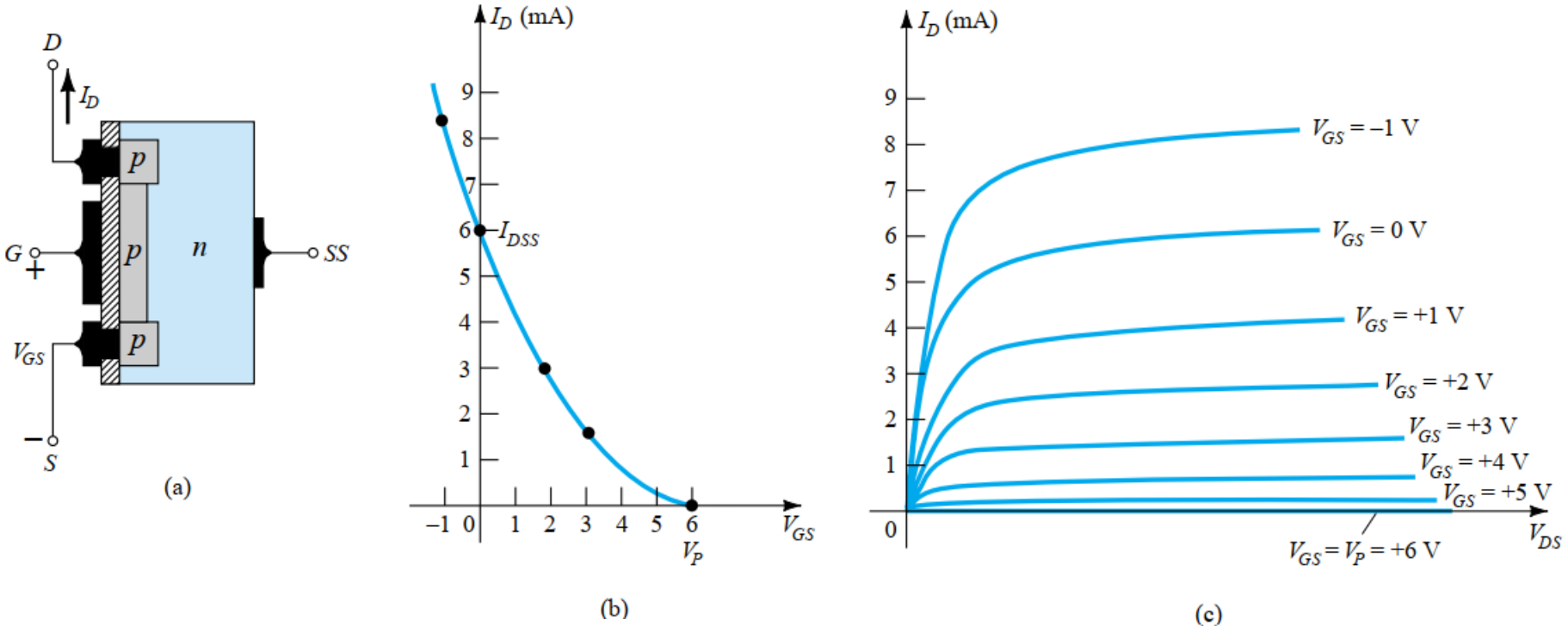


Fig: Drain and transfer characteristics for an *n*-channel depletion-type MOSFET

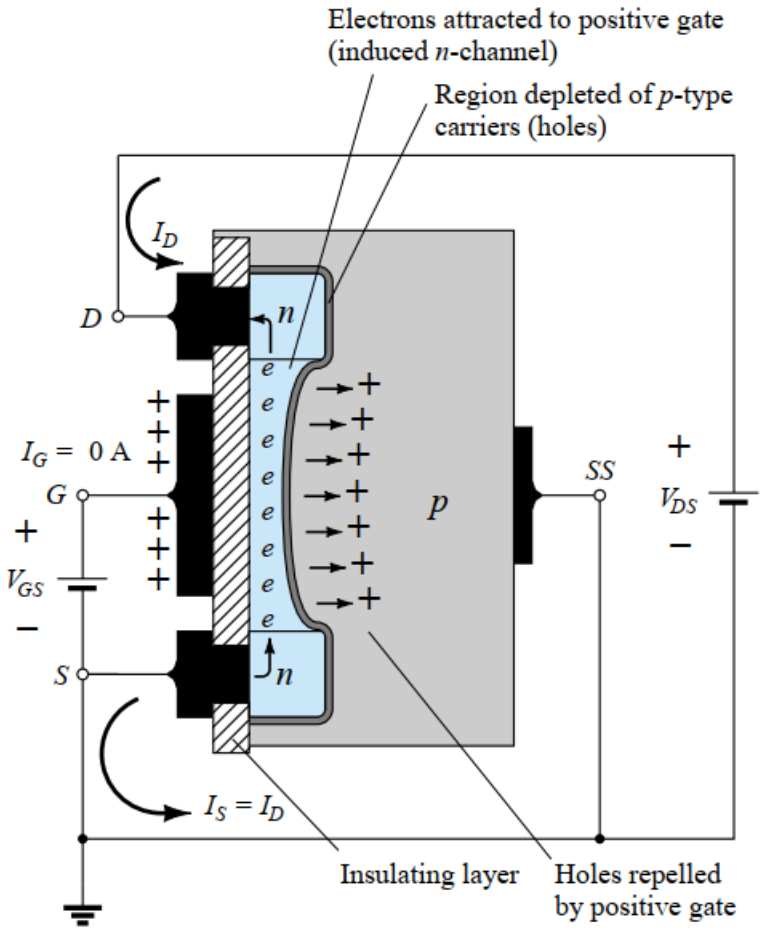
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

P-Channel Depletion MOSFET



p-Channel depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = +6$ V.

N-Channel Enhancement MOSFET



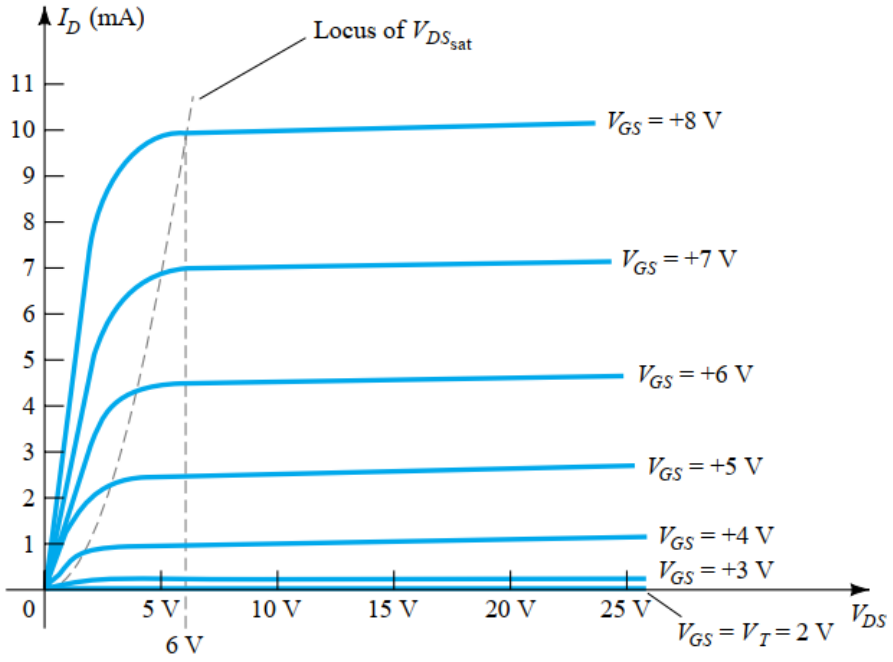
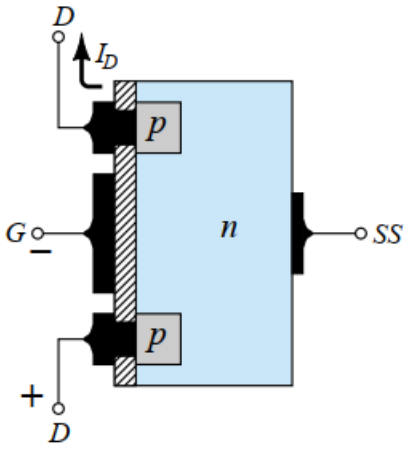


Figure 5.34 Drain characteristics of an *n*-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V^2.

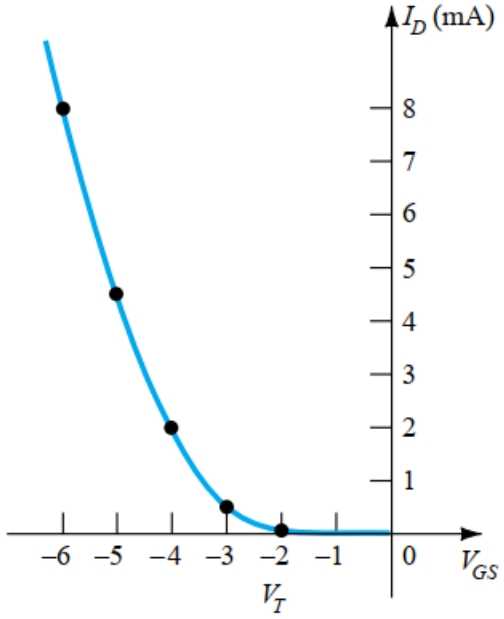
$$V_{DG} = V_{DS} - V_{GS} \qquad V_{DS_{sat}} = V_{GS} - V_T$$

$$I_D = k(V_{GS} - V_T)^2$$

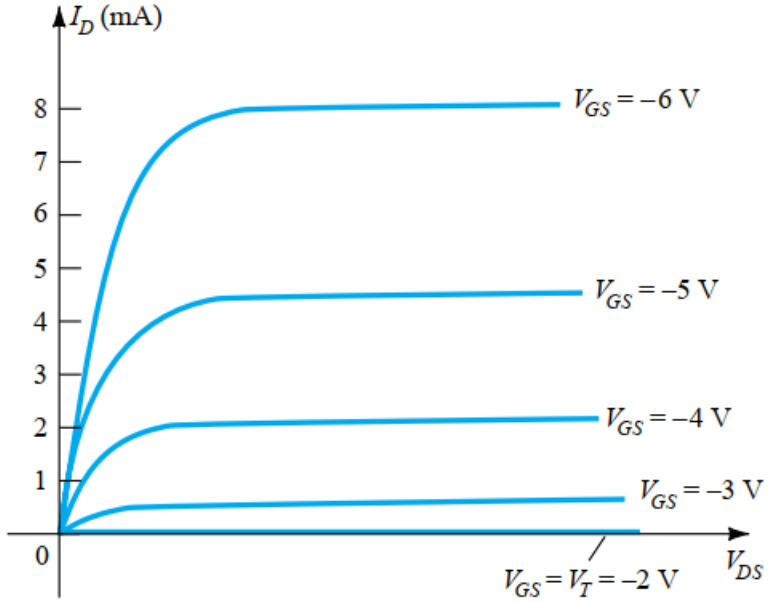
P-Channel Enhancement MOSFET



(a)



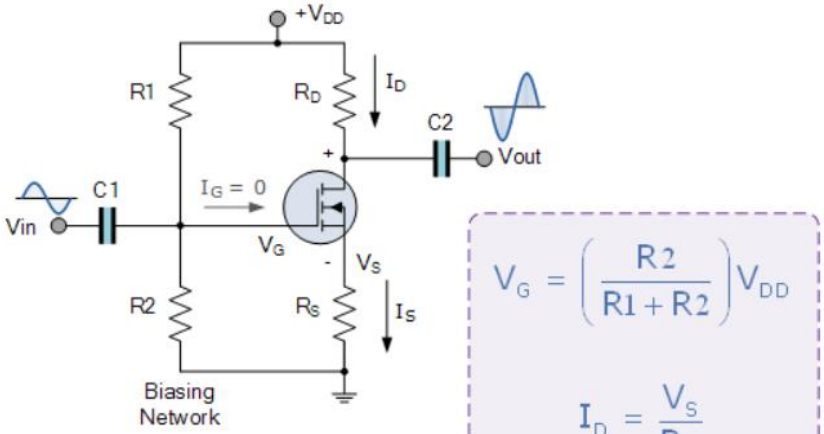
(b)



(c)

p-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V^2.

N-Channel Enhancement MOSFET as Amplifier



$$V_G = \left(\frac{R2}{R1 + R2}\right) V_{DD}$$

$$I_D = \frac{V_S}{R_S}$$

1. Cut-off Region – with $V_{GS} < V_{threshold}$ the gate-source voltage is much lower than the transistors threshold voltage so the MOSFET transistor is switched "fully-OFF" thus, $I_D = 0$, with the transistor acting like an open switch regardless of the value of V_{DS}.

2. Linear (Ohmic) Region – with $V_{GS} > V_{threshold}$ and $V_{DS} < V_{GS}$ the transistor is in its constant resistance region behaving as a voltage-controlled resistance whose resistive value is determined by the gate voltage, V_{GS} level.

3. Saturation Region – with $V_{GS} > V_{threshold}$ and $V_{DS} > V_{GS}$ the transistor is in its constant current region and is therefore "fully-ON". The Drain current I_D = Maximum with the transistor acting as a closed switch.