MODEL NO : TM089CFSP01-00

MODEL VERSION: 00

SPEC VERSION : 1.2

ISSUED DATE: 2019-04-28

■**Preliminary Specification**

□**Final Product Specification**

Customer : UNIZ

Approved by	Notes

TIANMA Confirmed :

Prepared by	Checked by	Approved by
Jack Hua	An guangkun	

This technical specification is subjected to change without notice

Table of Contents

Record of Revision

Rev	Issued Date	Description	Editor
0.1	2018-7-12	Preliminary release.	Beibei_Pan
1.0	2018-8-03	Update interface	Jack Hua
1.1	2018-8-28	Update drawing and PIN assignment	Jack Hua
1.2	2019-04-28	Update Electrical and Optical Characteristics	Jack Hua

1 General Specifications

Feature		Spec
Display Spec.	Size	8.9inch
	Resolution	3840×2400
	Technology Type	a-Si TFT
	Pixel Configuration	Mono-stripe
	Pixel pitch(mm)	0.05×0.05
	Display Mode	Transmissive, Normally Black
	Surface Treatment	Clear
	Viewing Direction	All
	Gray Scale Inversion Direction	NA
Mechanical Characteristics	LCM (W x H x D) (mm) --FOG TFT size	202×133x1.24
	Active Area(mm)	192×120
	With /Without TSP	Without TSP
	Matching Connection Type	BM20B(0.8)-50DP-0.4V(51)
	LED Numbers	NA
	Weight (g)	TBD
Electrical Characteristics	Interface	2 port MIPI
	Color Depth	Mono-LCD
	Driver IC	FT7250*2

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002+HF

Note 3: LCM weight tolerance: ± 5%

2 Input / Output Terminals

Connector type: BM20B(0.8)-50DS-0.4V(51)

Pin No.	Symbol	I/O	Function	Remark
1	VDDI	P	Power Supply for I/O	
2	VDD	P	Power Supply for DC/DC	
3	VDDI	P	Power Supply for I/O	
4	VDD	P	Power Supply for DC/DC	
5	TP_SCL	I/O	I2C Serial Clock	
6	NC	-	No connection	
7	TP_SDA	I/O	I2C Serial data	
8	TP_INT	O	Indicate coordinate data ready	
9	NC	-	No connection	
10	TP_RESET	I	TP reset signal	
11	NC	-	No connection	
12	GND	P	Ground	
13	TE	O	Tearing effect output	
14	NC	-	No connection	
15	RESX	I	Reset Signal	RESX
16	NC	-	No connection	
17	GND	P	Ground	
18	GND	P	Ground	
19	M-DATA-3N	I	Negative MIPI Data3 Input	DATA3N
20	S-DATA-3N	I	Negative MIPI Data3 Input	DATA3N
21	M-DATA-3P	I	Positive MIPI Data3 Input	DATA3P
22	S-DATA-3P	I	Positive MIPI Data3 Input	DATA3P
23	GND	P	Ground	
24	GND	P	Ground	
25	M-DATA-2N	I	Negative MIPI Data2 Input	DATA2N
26	S-DATA-2N	I	Negative MIPI Data2 Input	DATA2N
27	M-DATA-2P	I	Positive MIPI Data2 Input	DATA2P
28	S-DATA-2P	I	Positive MIPI Data2 Input	DATA2P
29	GND	P	Ground	
30	GND	P	Ground	
31	M-CLK_N	I	Negative MIPI Clock Input	CLKN
32	S-CLK_N	I	Negative MIPI Clock Input	CLKN
33	M-CLK_P	I	Positive MIPI Clock Input	CLKP
34	S-CLK_P	I	Positive MIPI Clock Input	CLKP
35	GND	P	Ground	
36	GND	P	Ground	
37	M-DATA-1N	I	Negative MIPI Data1 Input	DATA1N
38	S-DATA-1N	I	Negative MIPI Data1 Input	DATA1N
39	M-DATA-1P	I	Positive MIPI Data2 Input	DATA1P
40	S-DATA-1P	I	Positive MIPI Data2 Input	DATA1P
41	GND	P	Ground	
42	GND	P	Ground	
43	M-DATA-0N	I/O	Negative MIPI Data0 Input	DATA0N
44	S-DATA-0N	I/O	Negative MIPI Data0 Input	DATA0N

45	M-DATA-0P	I/O	Positive MIPI Data0 Input	DATA0P
46	S-DATA-0P	I/O	Positive MIPI Data0 Input	DATA0P
47	GND	P	Ground	
48	GND	P	Ground	
49	NC	-	No connection	
50	NC	-	No connection	

Note1：Please add the FPC connector type and matched one if necessary .

Note2：I——Input, O——Output, P——Power/Ground

3 Absolute Maximum Ratings

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Power Voltage	LCD_VCC	-0.3	4.5	V	
Input voltage	V_{IN}	-0.3	VDDI+0.3	V	
Operating Temperature	Top	-10	70	℃	
Storage Temperature	Tst	-20	80	℃	
Relative Humidity Note1	RH	--	≤95	%	Ta≤40℃
		--	≤85	%	40℃＜Ta≤50℃
		--	≤55	%	50℃＜Ta≤60℃
		--	≤36	%	60℃＜Ta≤70℃
		--	≤24	%	70℃＜Ta≤80℃
Absolute Humidity	AH	--	≤70	g/m³	Ta＞70℃

Table 3 Absolute Maximum Ratings

Note1:
Ta means the ambient temperature.
It is necessary to limit the relative humidity to the specified temperature range.
Condensation on the module is not allowed.

4 Electrical Characteristics

4.1 Driving TFT LCD Panel

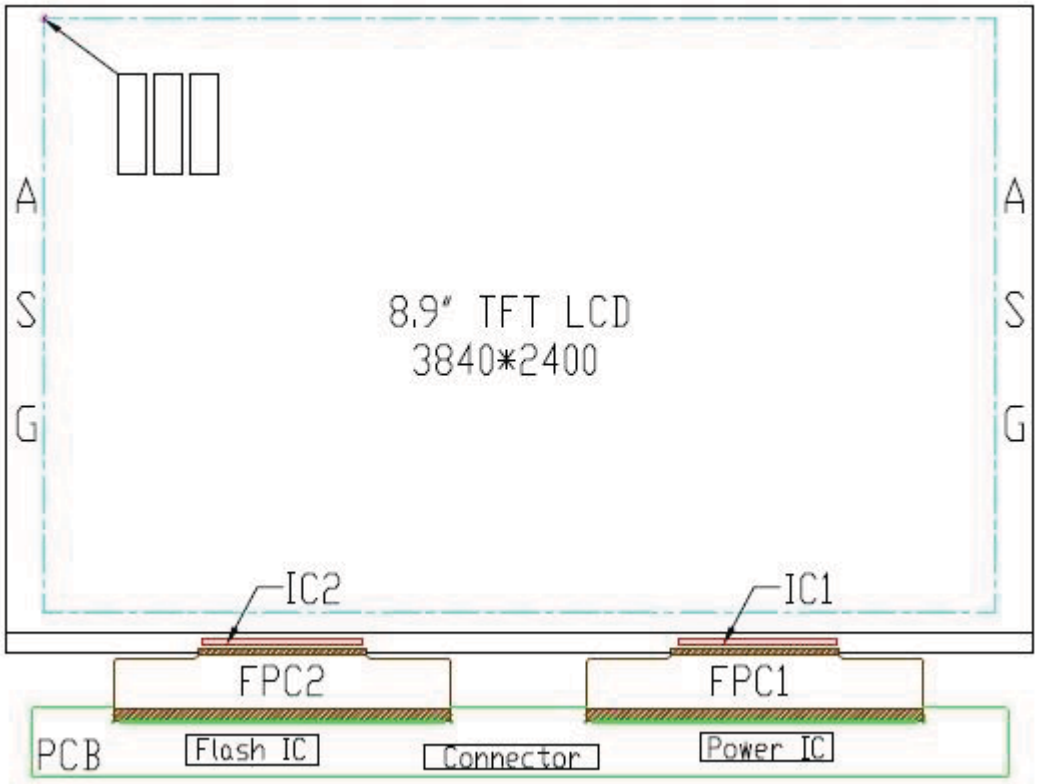
GND=0V, Ta=25℃

Item		Symbol	Min	Typ	Max	Unit	Remark
Power Supply Voltage for Logic and Analog		VDD	VDDI-0.1	3.3	VDDI+0.1	V	
Power Supply for I/O Interface		VDDI	1.7	1.8	1.9	V	
MIPI Supply voltage		VDDAM	1.7	1.8	1.9		Note1
Input Signal Voltage	Low Level	V_{IL}	0	--	0.3xVDDI	V	
	High Level	V_{IH}	0.7xVDDI	--	VDDI	V	
Output Signal Voltage	Low Level	V_{OL}	0	--	0.3xVDDI	V	
	High Level	V_{OH}	0.7xVDDI	--	VDDI	V	
(Panel+LSI) Power Consumption		White Mode (60Hz)		707		mW	
		Standby Mode		131		mW	

Note1: Input voltage include all MIPI data and clock

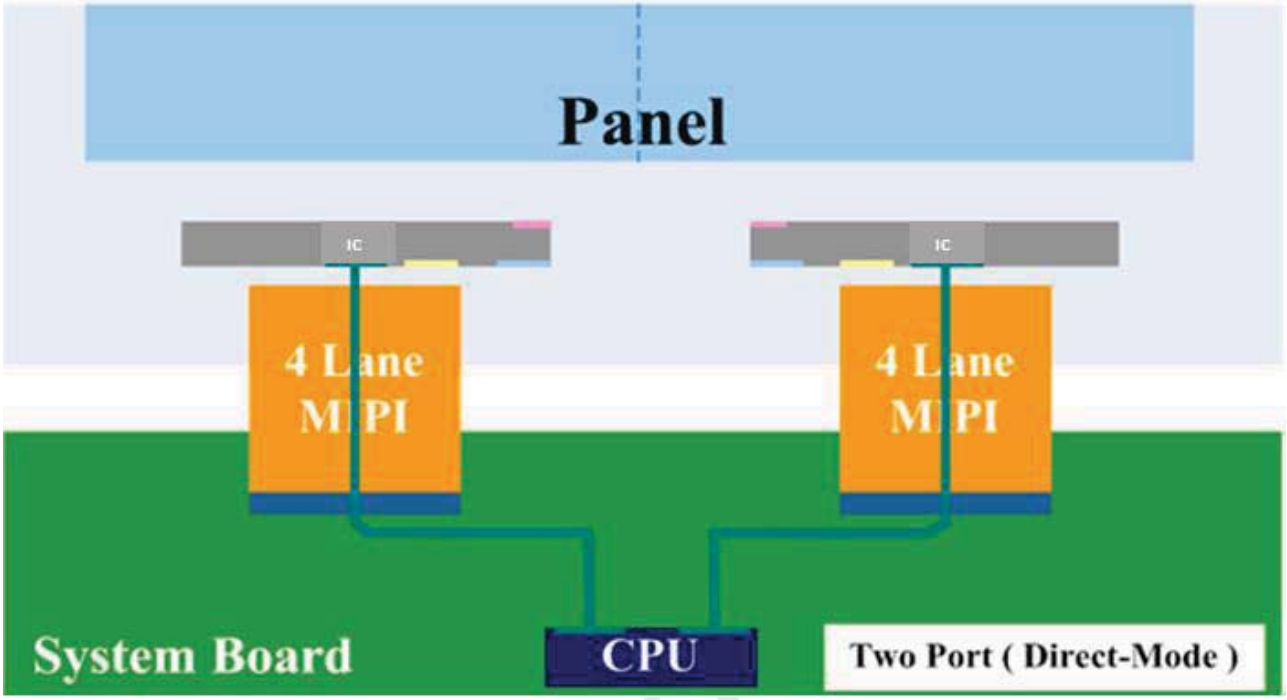
Table 4.1 LCD module electrical characteristics(voltage)

4.2 BLOCK DIAGRAM



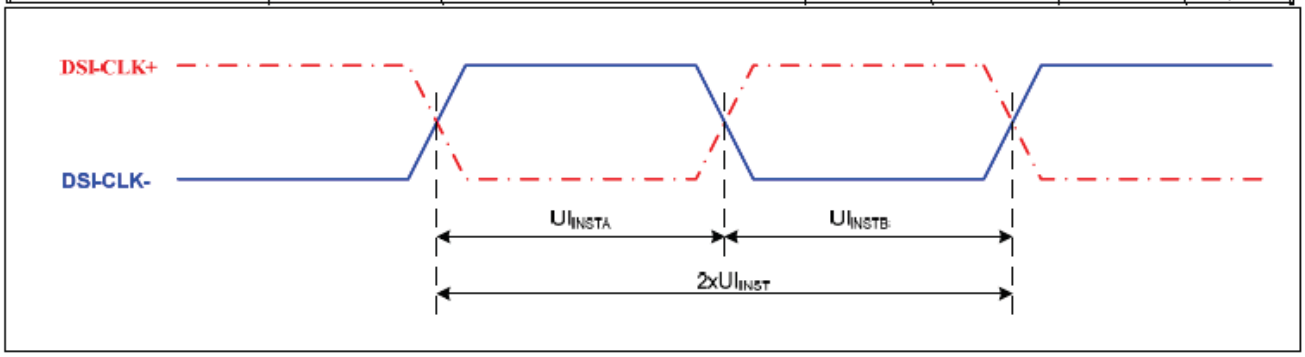
5 Timing Chart

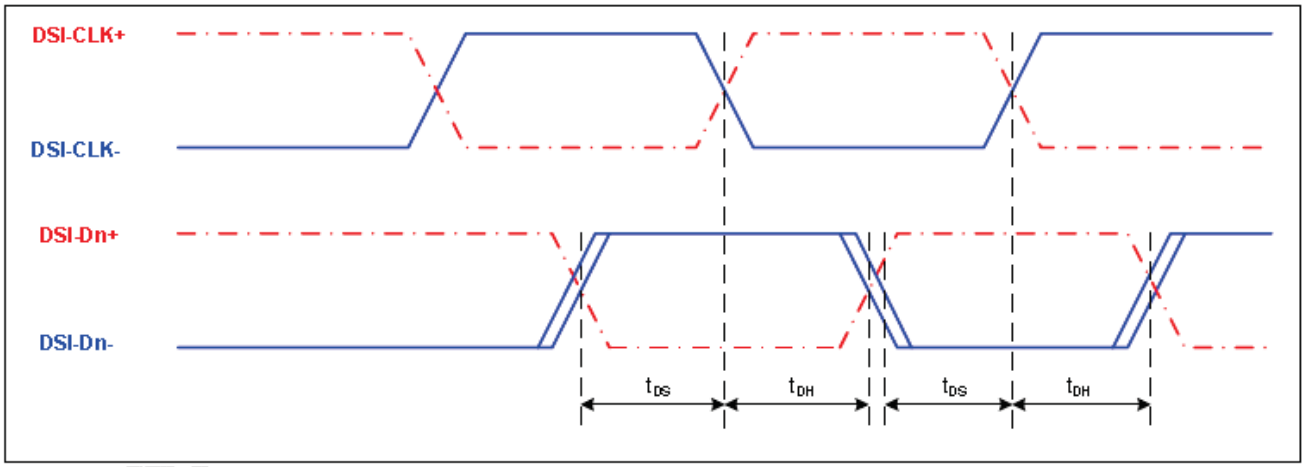
5.1 Interface Architecture



5. 2The Electrical Characteristics of High-Speed Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	2	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	1	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps





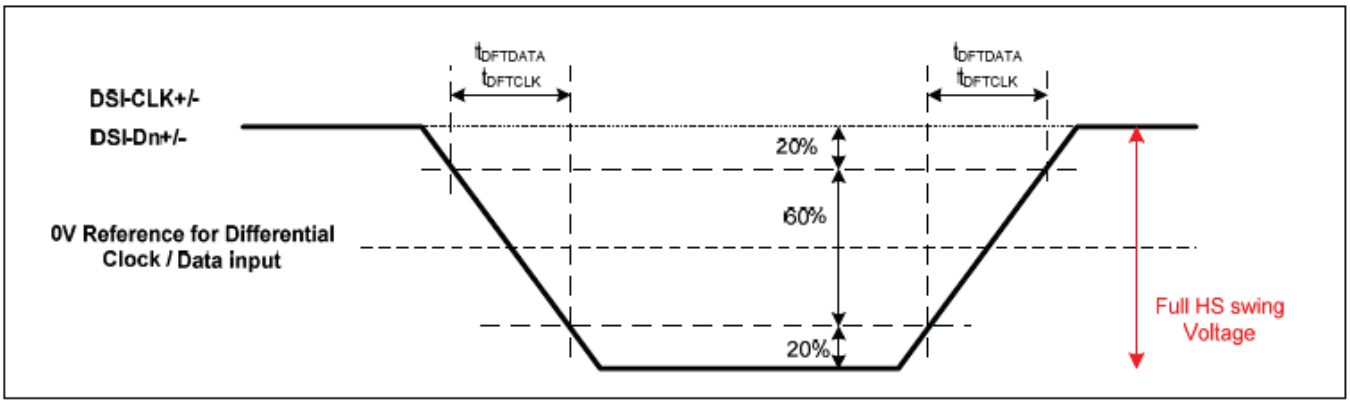


Figure: AC characteristics for MIPI-DSI High speed mode

5.3 The Electrical Characteristics of Low-Power Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	-

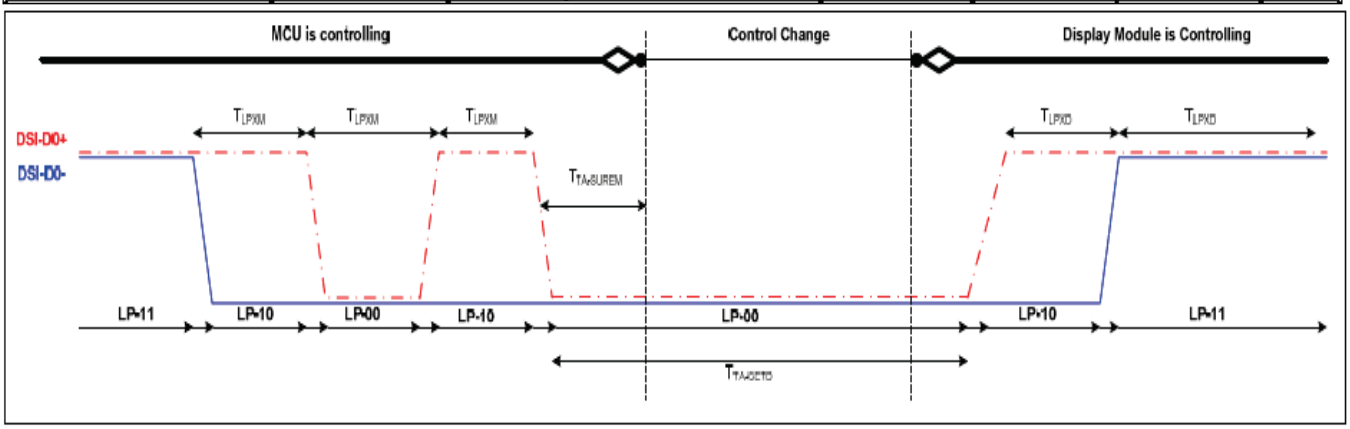


Figure: BTA from the MCU to the Display Module

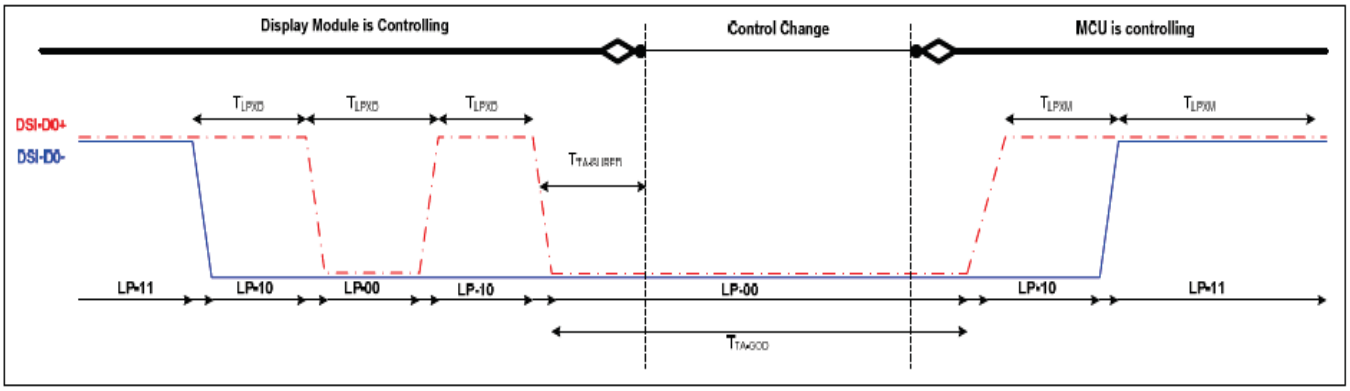


Figure: BTA from the Display Module to the MCU

5.4 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

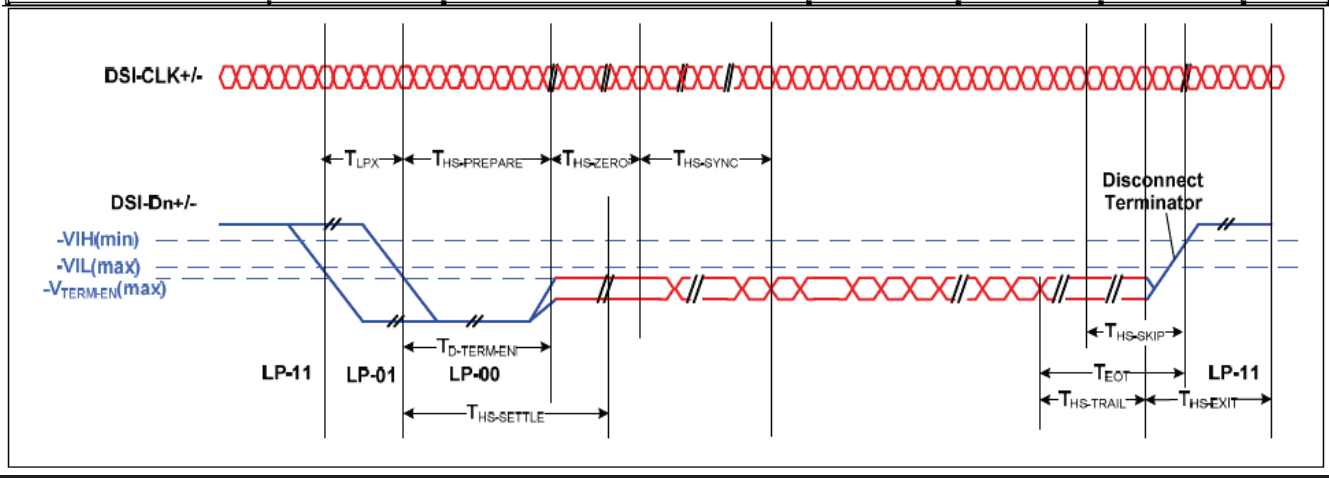


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

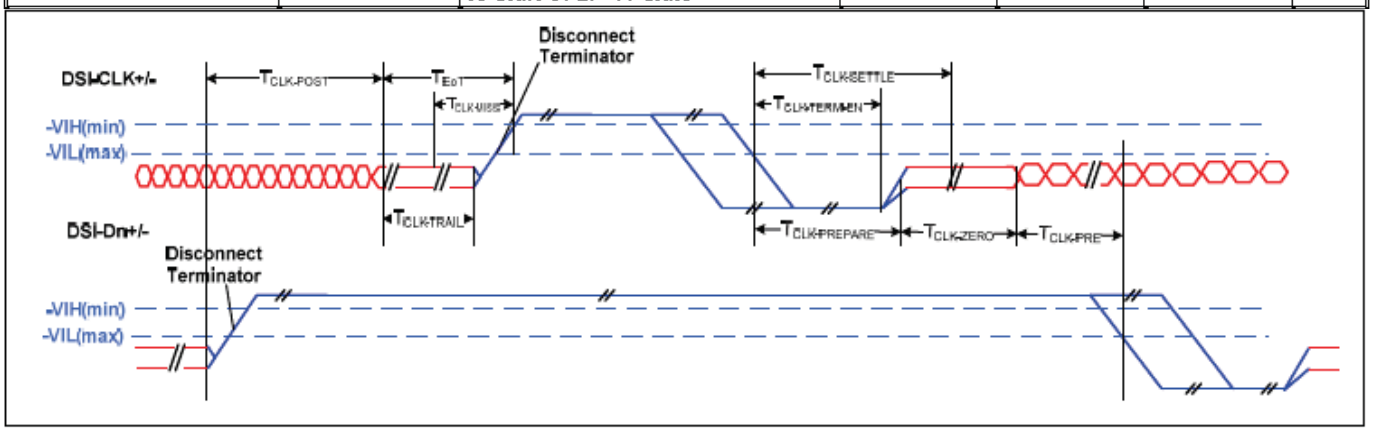


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

5.5 LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4 different combinations, what are listed below, are possible:

1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

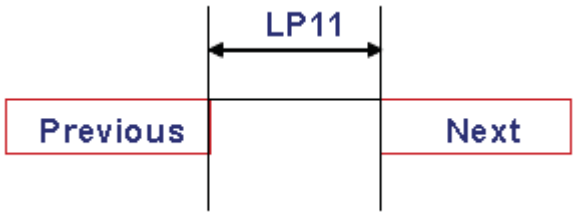
The Low Power Mode is also including 2 different functions:

1. Escape

2. Bus Turnaround (BTA)

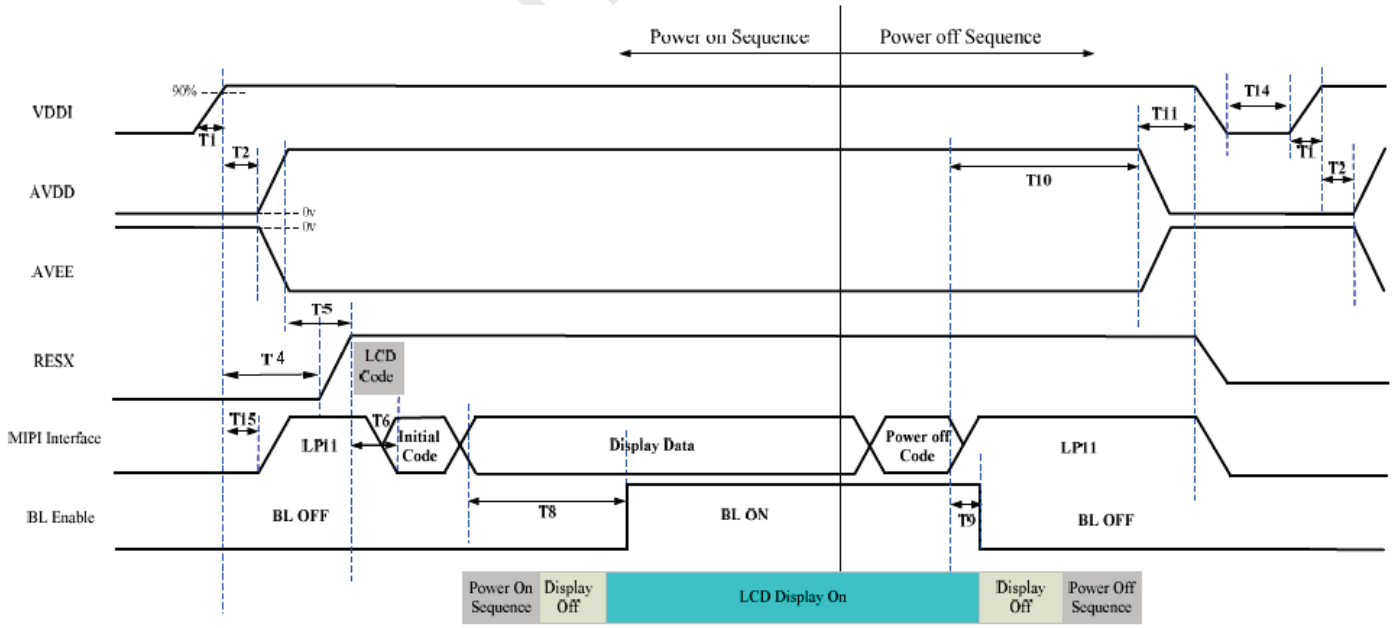
Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100 ns	-	100 ns	-	100 ns	-
HSDT	60ns + 52UI	-	60ns + 52UI	-	60ns + 52UI	-
BTA	100 ns	-	100 ns	-	100 ns	-



5.6 POWER ON/OFF SEQUENCE

1. RESX must be held stablely by host during Power On Sequence, otherwise function is not guaranteed.
2. The display module can also initialize and calibrate DSI-CLK +/- and DSI-D0 +/- lanes within 5ms after LP-11 (Clock and Data Channels),VDDI are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).
3. During Power off, VDDI cab be powered down 5ms after AVDD/AVVEE power down if LCD in Sleep-In Mode.
4. During Abnormal power dropping, VDDI can start power down 5ms after AVDD/AVEE power down.



Parameter	Description	Min	Max	Unit
T1	Rise time from 0.1VDDI to 0.9VDDI	0.47	5	ms
T2	VDD rise after VDDI power on	1		ms
T3	TP reset time after VDDI power on	5		ms
T4	TP reset release time after VDD power on	100		us
T5	TP Reset release to LCD Reset release	5		ms
T8	LED On after Initial Code	150		ms
T9	LED Off after power off code	50		ms
T10	VDD power down after power off code	150		ms
T11	VDDI power down after VDD power down	5		ms
T14	VDDI rise again after previous VDDI powered down	50	120	ms
T15	MIPI signals start (Hi-Z/GND to LP11) after VDDI power on	3		ms

6 Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	75	85	-	Degree	Note2
		θB		75	85	-		
		θL		75	85	-		
		θR		75	85	-		
Contrast Ratio		CR	θ=0°	600	800	-	-	Note1,3
Response Time		T_{ON}	25℃	-	25	35	ms	Note 4
		T_{OFF}						
Chromaticity	White	x	Backlight is on	-	-	-	-	Mono-LCD
		y		-	-	-		
	Red	x		-	-	-	-	
		y		-	-	-		
	Green	x		-	-	-	-	
		y		-	-	-		
	Blue	x		-	-	-	-	
		y		-	-	-		
Uniformity		U	-	90	-	-	%	Note1,5
NTSC		-	-	-	-	-	%	Mono-LCD
Transmittance		T	@405nm	5.0	5.4	-	%	Note1,6

Test Conditions:

1. The ambient temperature is 25℃.
2. The test systems refer to Note 1 (Excluding viewing angle and response time test).
3. Viewing Angle and Response Time test method follow the normal LCD test method.

Note 1: (1) Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen (Excluding Uniformity test). All input terminals LCD panel must be ground when measuring the center area of the panel.

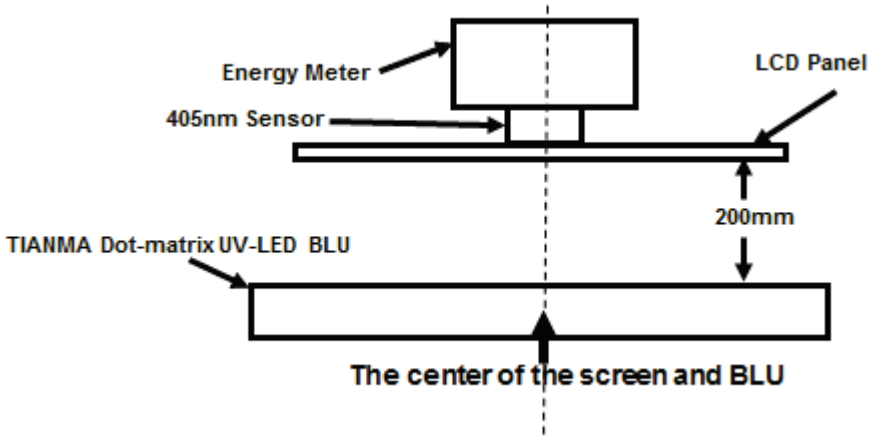


Fig.1

(2)Test instrument and recipe.

As shown in the Fig.1, all optics are measured under a collimating dot-matrix LED backlight, which emitting a wave of 405nm. Energy meter AccuMAX^{TM} –XS-405 is used to measure the following mentioned energy value, the LCD panel is 200mm away from the UV-LED surface. The transmissive energy value of LCD at white state is 2mW/cm^2.(Fig.1)

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD.(Fig.2)

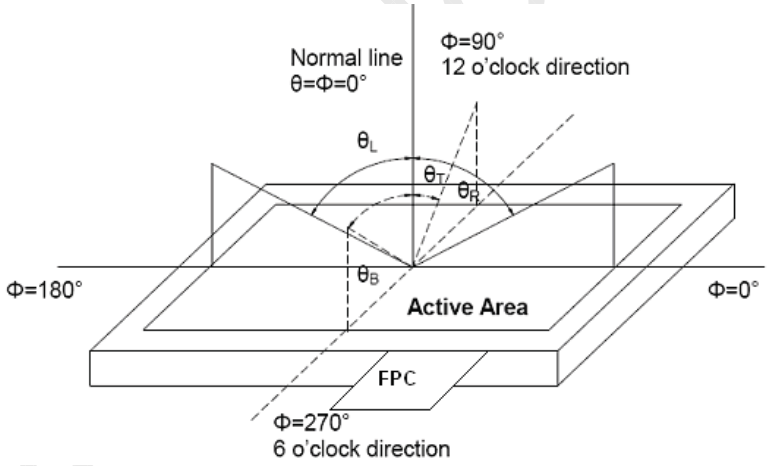


Fig.2

Note 3: Definition of contrast ratio

$$\text{Contrast Ration(CR)} = \frac{\text{Energy value measured when LCD is on the “White” state}}{\text{Energy value measured when LCD is on the “Black” state}}$$

“White state “: The state is that the LCD should be driven by Vwhite.

“Black state”: The state is that the LCD should be driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.(Fig.3)

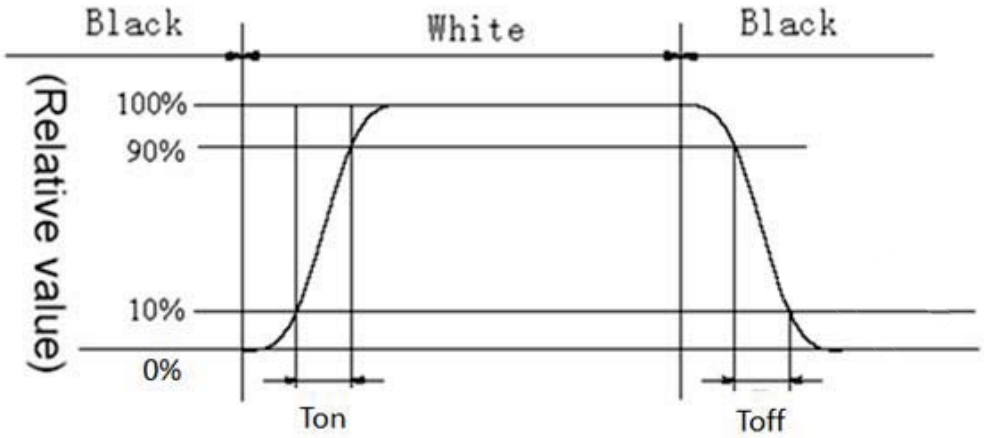


Fig.3

Note 5: Definition of Energy Uniformity

Active area is divided into 9 measuring areas (Fig. 4). Every measuring point is placed at the center of BLU center.

Energy Uniformity (U) = Emin / Emax

L-------Active area length W----- Active area width

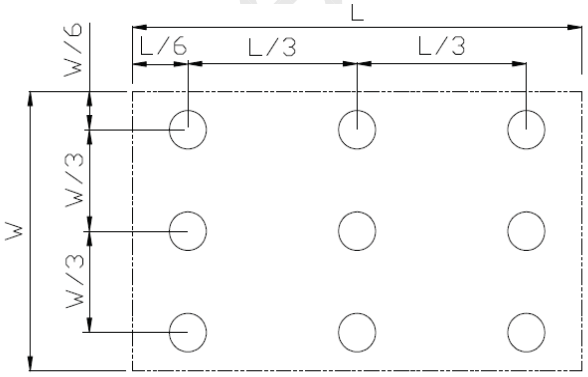


Fig.4

Emax: The measured Maximum Energy value of all the measurement positions.

Emin: The measured Minimum Energy value of all the measurement positions.

Note 6: Definition of transmittance:

$$\text{Transmittance} = \frac{\text{Energy value measured when LCD is on the "White" state}}{\text{Energy value measured from BLU}}$$

7 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts=70℃,240H	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	Ta=-10℃,240H	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta=80℃, 240H	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	Ta=-20℃,240H	IEC60068-2-1:2007 GB2423.1-2008
5	Operation at High Temperature and Humidity	Ta=60℃,90％RH,240H	IEC60068-2-78 :2001 GB/T2423.3—2006
6	Thermal Shock (non-operation)	-20℃-+80℃，30min，Change Time: 5min，total 100cycle	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002
7	Package Vibration Test	Frequency（Hz） 5~20-200Hz, PSD:0.01-0.01-0.001 Total:0.781g2/Hz， time：X/Y/z each direction 30min	IEC60068-2-6:1982 GB/T2423.10—1995
8	Package Drop Test	Total weigh≤10Kg，Height:80cm; Total weigh＞10Kg,，Height:60cm; 1corner,3edges,6surfaces	IEC60068-2-32:1990 GB/T2423.8—1995
9	Life time	4000H ,transmissive 405nm＜1.5mW/cm^2	Optics data delta<10%

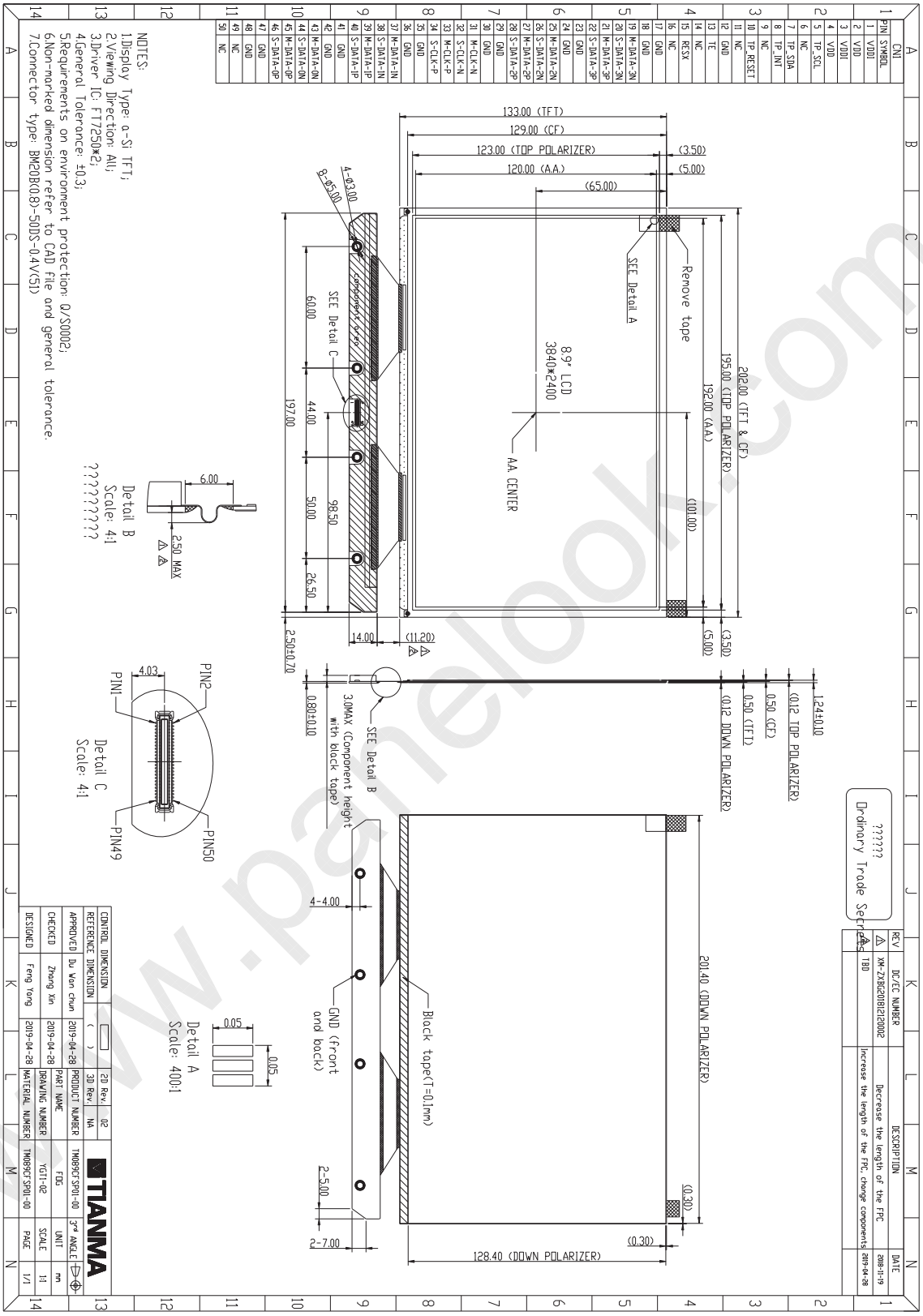
Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

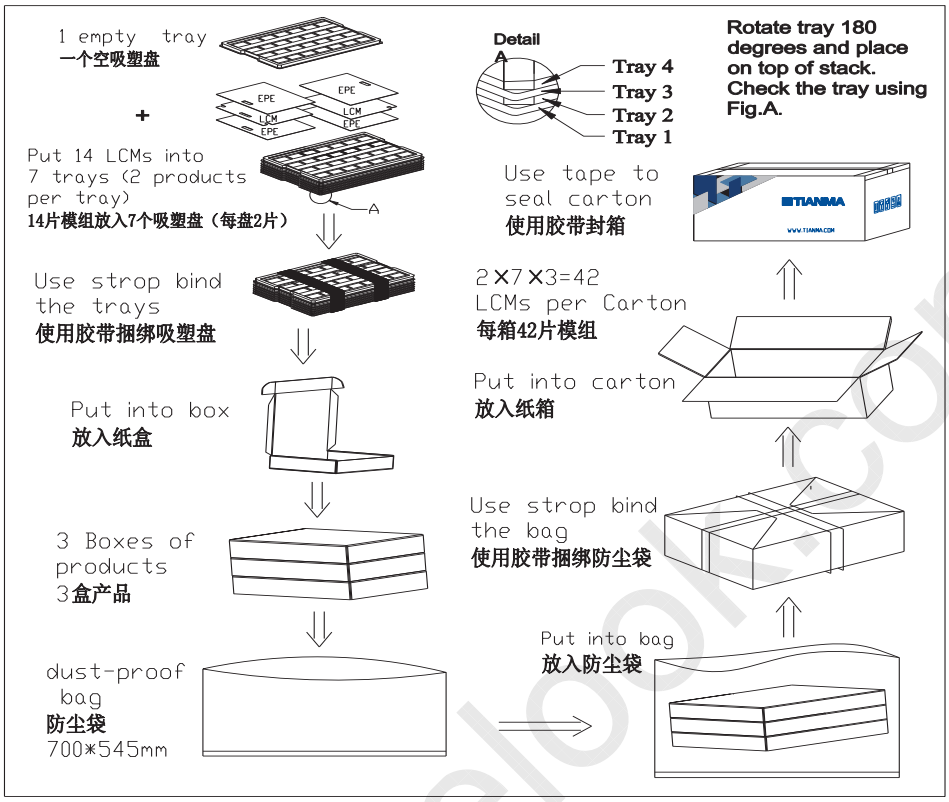
Note3: Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room temperature.

Note4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

8 Mechanical Drawing



9 Packing Drawing



10 Precautions for Use of LCD Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol

— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water

— Ketone

— Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

10.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.