Efficient Real-time Implementation of a Channelizer Filter with a Weighted Overlap-Add Approach

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Abstract *We investigate a real-time implementation of a channelizer filter for joint digital down-conversion, matched-filtering and samplerate conversion of multicarrier signals in coherent access networks. A complexity reduced design is proposed and synthesized with low performance penalty in a system experiment.*

Introduction

An attractive option for long-reach passive optical networks (PON) is the use of ultra-dense wavelength-division multiplexing[1] (UDWDM) passive optical networks (PON) enabled by coherent detection and digital signal processing (DSP). In the downstream, the optical line terminal (OLT) distributes electronically subcarrier-multiplexed signals to the optical network units (ONU). Each ONU is equipped with a coherent receiver frontend and tunes its local oscillator (LO) frequency to the assigned subcarrier channel. The LO source at the ONU is both used for reception and transmission to ensure frequency stable transmission also in the upstream direction which is depicted in Fig. 1(a). This allows for the simultaneous coherent reception of multiple upstream channels by a broadband receiver at the OLT which is shown in Fig. 1 (b). A polarization diversity heterodyne receiver translates the optical field comprising the spectral content of multiple subchannels into the electrical domain. The analog waveform is then sampled by analog-to-digital converters (ADC) and fed to the channelizer which is one of the key DSP components of the coherent OLT receiver as it operates on the full ADC sample rate and applies joint digital down-conversion, matched-filtering and samplerate conversion to the received multicarrier (MC) signal.

In this contribution we present an efficient real-time implementation of a channelizer filter based on a weighted overlap-add (WOLA) approach[2]. A fully parallel design is synthesized and optimized with respect to the number of required hardware (HW) resources in order to fit on a target Xilinx Virtex5 field-programmable gate array (FPGA). The design shows low performance penalty in the reception of 9×2.488 Gb/s polarization-division multiplexed (PDM) differential quadrature phase-shift keying (DQPSK) compared to offline processing.

Weighted overlap-add channelizer

A straight-forward implementation of a channelizer holds major drawbacks as the complex phasor for down conversion and the anti-aliasing filter operate at full sampling rate and need to be implemented redundantly for each subchannel exhausting valuable HW resources.

The WOLA filter resolves these issues by using techniques from discrete Fourier transform (DFT) filterbank processing[2]. HW resources are shared among subchannels and frequency conversion can be implemented using efficient DFT algorithms. The prerequisite for this approach is that all channels possess the same bandwidth and provide a regular frequency spacing. Both requirements are met by system

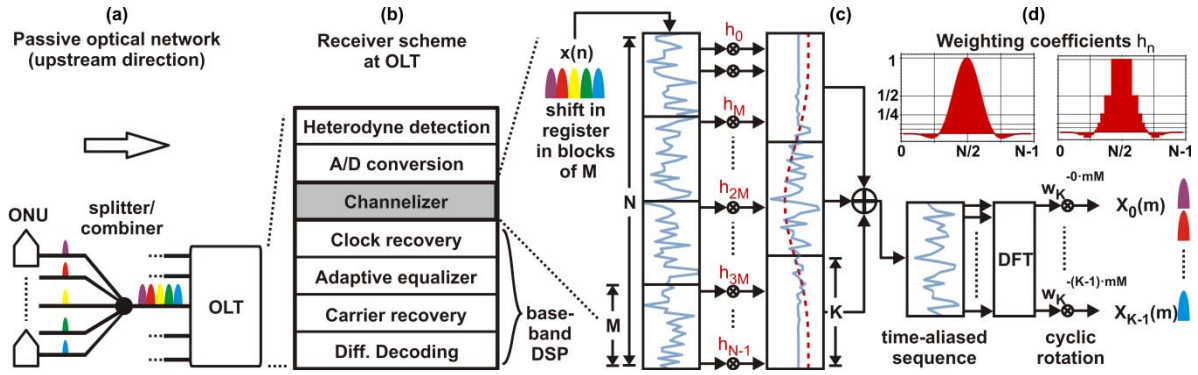

Fig. 1: (a) PON upstream link from optical network units (ONU) to optical line terminal (OLT) with simultaneous coherent reception of multiple ONU upstream channels. (b) OLT receiver scheme using heterodyne detection, multicarrier channel separation in the digital domain, and signal processing for each carrier. (c) Channelizer employing block shift register, weighting, overlap-add stage, discrete-Fourier transform (DFT) and cyclic rotation. (d) Continuous and quantized weighting coefficients.

design, in particular the latter by synchronizing the ONU channels to the OLT's frequency grid.

The working principle of the WOLA filter is shown in Fig. 1 (c), where K refers to the number of output channels, M is the decimation factor and *N* is the length of the shift register. The input sequence is shifted into the register in blocks of M samples. The samples are weighted with coefficients h_n and overlap-added in K-segments. The weighting coefficients resemble the matched impulse response to the transmitter pulse. The sequence is then processed by a DFT of length K and a cyclic rotation corrects for the sliding time reference of the input stream.

Design constraints

The WOLA filter is designed to process subchannels with a symbol rate of 622 MBd each possessing a spectral width of 933 MHz due to root raised cosine (RRC) pulse shaping with roll-off 0.5. The ADCs operate at 29.857 GS/s which makes the received spectrum sliceable to K = 32 frequency slots of 933-MHz width. To obtain a target sampling rate of 2×622 MS/s at each output channel of the WOLA filter, each subchannel experiences an effective decimation by M = 24. Due to the blockwise processing of the WOLA filter, the required throughput is thereby reduced from 29.857 GS/s down to 1.244 GS/s. With an eight-fold parallelization of the design the FPGA is clocked with 155.5 MHz. The number of weighting coefficients N is by design a common multiple of K and M. In simulations, it was found that N = 192 provides sufficient stop-band attenuation and good matched filter characteristics. The weighting function has a RRC shape and is additionally windowed with a Hann window to remove discontinuities at the edges to mitigate unwanted filter side lobes. For an 8-fold parallelization, this would result in 8×192 multipliers which will exceed the HW resources of the target FPGA. Therefore, the weighting coefficients are discretized to the next power of two (see Fig. 1 (d)) to enable HW efficient realization by simple bit shift operations. The DFT is implemented as a complex 4×8 Cooley-Tukey DFT with only 72 HW multipliers. It is only 4-fold parallelized since each complex DFT can process 2 real-valued sample streams. The cyclic rotation at the output of the DFT is effectively a trivial multiplication for given M and K, thus comes at no HW cost.

So, the full design comprises only 4×72 multipliers which are realized with logic slices. The fully parallel design is synthesized for a Xilinx Virtex-5.

Experimental validation

The experimental setup of the UDWDM upstream link in a back-to-back configuration is shown in Fig. 2. The electrical signal generation is done with a 2-channel digital-to-analog converter (DAC), using a sampling rate of 29.856 GS/s to generate the electrical signal with nine SC. Each SC is modulated with a unique random binary sequence. The optical carrier is generated by an external cavity laser (ECL). Optical modulation is realized with a single-polarization I/Q modulator driven by the electrical MC signal and an optical polarization-multiplexing stage. An erbium-doped fiber amplifier followed by a variable optical attenuator is used to vary the received power.

The optical receiver frontend is an integrated polarization-diversity heterodyne receiver[3] shown in the inset of Fig. 2. In order to emulate the frequency tracking between ONUs and OLT, we simultaneously use the transmitter ECL as LO. After optical-electrical conversion, two Micram ADC30 ADCs with 6 bit nominal resolution and real-time interfaces to the following FPGA boards are used. The ADCs operate at a sampling rate of 29.857 GS/s driven by an independent clock source and a slightly higher clock frequency as the DAC. On each FPGA, 2 million samples are saved into block RAMs on a trigger event and are transferred to a personal computer (PC) for offline processing as shown in Fig. 1(b). The

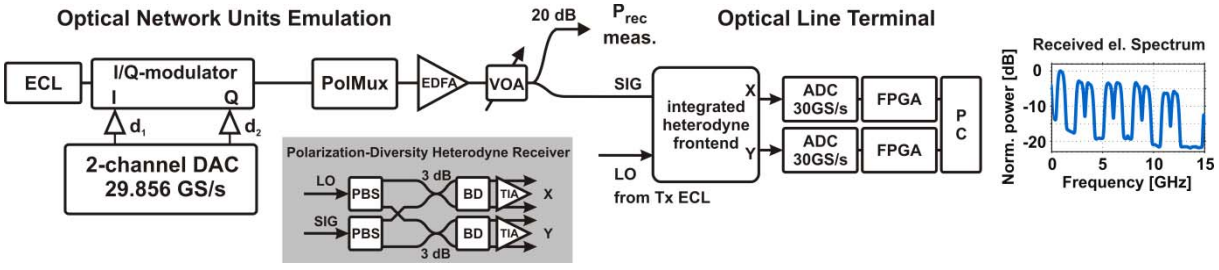

Fig. 2: Experimental setup. ECL: external cavity laser, PolMux: optical polarization-multiplexing stage, DAC: digital-to-analog converter, EDFA: erbium-doped fiber amplifier, VOA: variable optical attenuator, PBS: polarization beam splitter, BD, balanced photo detector TIA: transimpedance amplifier, ADC: analog-to-digital converter, FPGA: field-programmable gate array, PC: personal computer. The inset shows the received single-sided electrical spectrum of the nine-channel MC signal at the input of the WOLA filter.

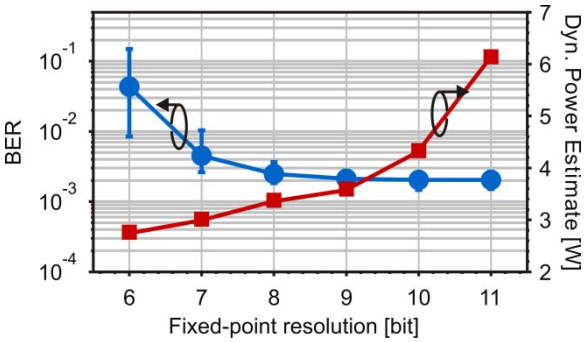

Fig. 3: Measured BER (blue) and dynamic power consumption (red) for P_{rec} = -28.8 dBm versus fixed-point resolution of FPGA behavioral model. The BER is averaged over all UDWDM channels. Error bars indicate BER of best/worst received UDWDM channel.

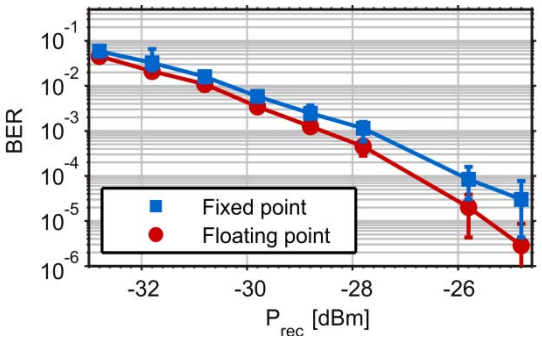

Fig. 4: Measured BER (averaged over all UDWDM channels) versus received power P_{rec} for 9×2.488 Gb/s PDM-DQPSK with floating point offline processing and fixed-point FPGA implementation (8 bit resolution). Error bars indicate BER of best/worst received UDWDM channel.

WOLA filter is simulated using a FPGA behavioral model. For comparison, an equivalent floating point model is used. All subsequent floating point DSP blocks operate in their respective subchannel baseband. Compensation of a clock mismatch is performed by a feedforward timing recovery[4]. The signal is then decimated and processed by a 2×2 T-spaced adaptive time-domain equalizer with 3 taps and a constant-modulus update criterion. The carrier phase is recovered by a sliding window Viterbi-Viterbi algorithm after which decision, demapping, differential decoding and error counting are performed

Results and discussion

The WOLA filter input resolution was kept fixed at 6 bit. The internal logic operations for weighting, overlap-add and DFT were scaled not exceeding a maximum fixed-point bit resolution as stated in Fig. 3. Here, the measured bit error ratio (BER) is shown averaged over all UDWDM channels for a received power of P_{rec}=-28.8 dBm and various resolutions. In the same figure, also the estimated dynamic power consumption (clocks, logic, signals and inputs/outputs) on this particular HW platform is shown for the same bit resolutions. The power analysis can only serve as a trend curve as it varies with the synthesis strategy and is specific to the FPGA platform under consideration. We observe a saturation of the BER at a fixed-point resolution of 8 bit with a dynamic power consumption of 3.4 W at the same resolution.

In Fig. 4 the BER performance of the 8 bit design is shown as a function of the received power and compared to floating point offline processing. Note, that the floating point implementation was not constrained to discretized weighting coefficients in contrast to the FPGA implementation. Error bars indicate best and worst measured BER over 9×500.000 evaluated bits and show stable operation over a wide range of received power. At a BER of 10^{-3} we observe an implementation penalty of only 1 dB compared to floating point. The penalty is attributed to the value-discrete weighting coefficients and accumulated quantization noise causing imperfect channel separation. The occupied resources on the FPGA are reported in Tab. 1. An implementation using 8x192 multipliers in the weighting stage after the shift register would have easily exceeded the HW resources of the targeted Virtex-5 FPGA.

Tab. 1: Occupied FPGA resources (xc5vfx200tff1738-2) for 8 bit resolution and without use of embedded multipliers

	Used	Available
Slice Registers	47155 (38%)	122880
Slice Look-up Tables	42860 (34%)	122880

Conclusion

We report on the resource efficient implementation of a channelizer filter enabled by DFT filterbank with low performance penalty in a system experiment. To save multiplier resources, the weighting coefficients were realized with bit-shift operations on the cost of a moderate 1-dB penalty due to imperfect channel separation.

Acknowledgements

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