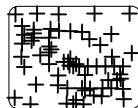
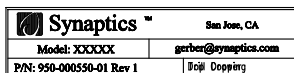
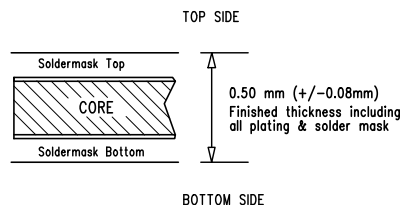


16. Supplier shall submit the first article report per procedure 578-000662-01 and must ensure all the dimensions conform to drawing ME920-XXXXXX in the Bom.
17. PCB outline dimensions to be taken from supplied gerber data.
18. Pack panels or boards in a vacuum-sealed bag with a clean blank sheet of paper between each individual panel to protect surface from scratches.

#### LAYER STRUCTURE (SCALE: NONE)




SIZE	QTY	SYM	PLATED	TOL
0.1	65	+	YES	+/-0.0

#### NOTES: (Unless otherwise specified)

1. ALL requests for design or material changes must be forwarded to Synaptics. No design and material changes shall be implemented without approval from Synaptics PCB DESIGN GROUP. (gerber@synaptics.com).
2. Fabricate board using artwork. All typical dimensions are tolerance non-cumulative.
3. Acceptability shall be based on IPC-A-600 RevG. Performance must meet IPC-6012. Class 2.
4. MATERIAL: Construct PCB using FR-4 (shall meet UL 94V-0) with a minimum Tg of 170 degrees C. Use 1/2 oz.(0.0007" [18um] thick) base copper for all metal layers.
- 4a. All material used and processes applied shall be compliant with EU RoHS directives. Detail requirement refers to the Commission Decision of 18 Aug 2005 amending Directive 2002/95/EC notified under document 2005/618/EC."
5. FABRICATION TOLERANCES:  
Trace width must maintain a +/-20% in tolerance  
All holes and registration must be within 0.076mm [0.003"] of true position.
- 5a. Fabrication process must be UL approved and boards must be identified with Mfr.'s approved logo, type designation, week and year of manufacture. Date code shall be in format WWYY, where WW=2 digit work week and YY=2 digit year. Screen onto bottom silk-screen in box depicted in Gerber and referenced in this drawing. Manufacturer shall NOT add any additional text, such as:"Made in...". All silk-screen shall appear on SOLDER MASK, NOT over exposed Metal.
6. PLATING: Holes to be continuous electrolytic Cu with 0.01778mm/0.0381mm [0.0007"/0.0015"] thick wall. Hole sizes measured after plating.
7. FINAL PLATING: Ni/Au, all exposed circuits 0.00005mm [0.00000197"] minimum thick Au over 0.003mm [0.000118"] minimum thick Ni. The maximum gold thickness is 0.000508mm.
8. Apply GREEN LPI soldermask to PCB per artwork, conforming to IPC-SM-840C, Class T.
9. Screen print the legend using non-conductive WHITE epoxy ink. There shall be no ink on pad, test point or exposed metal as defined by solder mask layer per artwork.
10. Add Letter/number(A1,A2,A3...B1,B2,B3...) to each board on bottom silkscreen layer inside of large product label box (Only required on panel array form. please reference 520-000XXX specification on 920-000XXX BOM) Silkscreen shall not be over exposed metal.
11. Flatness: Measure bow and twist per IPC TM-650.
12. Electronic test shall be performed for opens and shorts.
13. Please send panelized gerber including paste layer to gerber@synaptics.com for approval before process.
14. Fiducials shall be blacked out on board to identify bad boards.
15. Boards panelization is required if board is smaller than 76.2mm [3"] x 76.2mm [3"]. Please reference panelization documentation 520-000XXX specified on PCB BOM 920-000XXX.

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COMPANY:  Synaptics/ADC		San Jose, CA	
TITLE: FAB DWG,TOURMALET DISPLAY ADAPTOR			
DRAWN: Bjorn H	DATED: 06SEP2017	CODE:	SIZE:
CHECKED:	DATED:	DRAWING NO:	REV:
QUALITY CONTROL:	DATED:	FD950-000550-01	1
RELEASED:	DATED:	SCALE: NONE	SHEET: 1 OF 1

 <b>Synaptics</b> <sup>TM</sup>		San Jose, CA
Model: XXXXX		gerber@synaptics.com
P/N: 950-000550-01 Rev 1		Top Silk Screen


950-000550-01 Rev 1  
2017

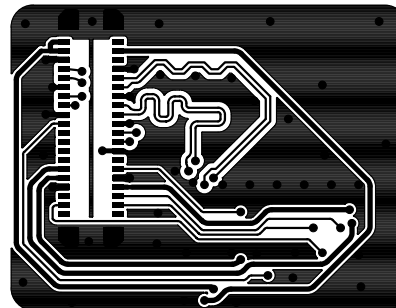
J4



**Synaptics**

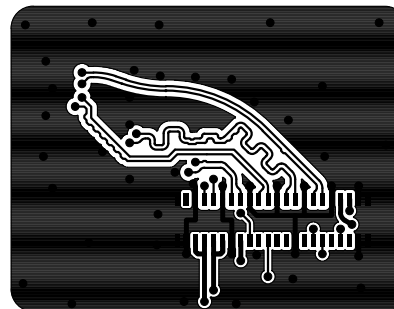
 <b>Synaptics</b> ™		San Jose, CA
Model: XXXXX		gerber@synaptics.com
P/N: 950-000550-01 Rev 1		Top SolderMask




 <b>Synaptics</b> <sup>TM</sup>		San Jose, CA
Model: XXXXX		gerber@synaptics.com
P/N: 950-000550-01 Rev 1		Top Copper




 <b>Synaptics</b> <sup>TM</sup>		San Jose, CA
Model: XXXXX		gerber@synaptics.com
P/N: 950-000550-01 Rev 1		Bottom Copper




 <b>Synaptics</b> ™		San Jose, CA
Model: XXXXX	gerber@synaptics.com	
P/N: 950-000550-01 Rev 1	Bottom SolderMask	

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 <b>Synaptics</b> <sup>TM</sup>		San Jose, CA
Model: XXXXX	gerber@synaptics.com	
P/N: 950-000550-01 Rev 1	Bottom Silk Screen	

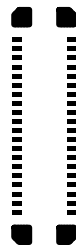
12  
[                      ]  
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 <b>Synaptics</b> <sup>TM</sup>		San Jose, CA
Model: XXXXX		gerber@synaptics.com
P/N: 950-000550-01 Rev 1		PCB Outline





 <b>Synaptics</b> ™		San Jose, CA
Model: XXXXX		gerber@synaptics.com
P/N: 950-000550-01 Rev 1		Top Paste Mask





San Jose, CA

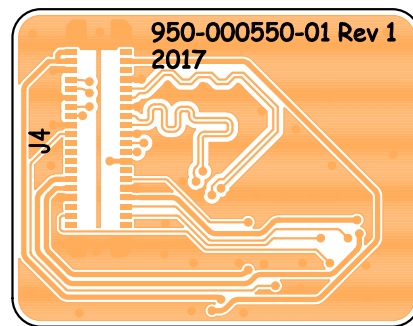
Model: XXXXX


gerber@synaptics.com

P/N: 950-000550-01 Rev 1

Bottom Paste Mask

[illegible]



Synchronous <sup>TM</sup> 		San Jose, CA	
Model: XXXXX		gerber@synchronous.com	
P/N: 950-000550-01 Rev 1		Bottom Silk Screen	

