納 入 仕 様 書

パイオニア株式会社　御中

仕様書番号　A－２０５―１３８４９６―１３４２３９－０８１２２６０２０３

パイオニア品番：ＡＤＳ７８２８Ｅ
弊 社 製 品 名：ＡＤＳ７８２８ＥＩＰＷＲＱ１

部　品　種　名：ＩＣ
日　　付：平成２１年1月８日

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この書類を受領いたしました。

受領印欄	2009年 1月28日 パイオニア株式会社 川越工場技術部	年　月　日

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仕様書発行履歴

仕様書番号:A-205-138496-134239-0812260203

お客様名　　:　　パイオニア株式会社　殿

貴社品名　　:　　ADS7828E
弊社品名　　:　　ADS7828EIPWRQ1

版	発行日	内容
A	2009年1月22日	初版発行

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2007年2月9日

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弊社仕様書の優先言語に関して

拝啓　貴社益々ご清栄のこととお慶び申し上げます。
平素は格別のお引き立てをいただき、厚くお礼申し上げます。
さて、弊社から提出させて頂いております納入仕様書の優先言語につきまして、ご連絡させて頂きます。

仕様書で英文と和文の両方がある場合、基本的には英文仕様書を基に和文仕様書を作成しております関係上、英文を優先させて頂きます。

敬具

DSD #
納入仕様書番号 : **0812260203**

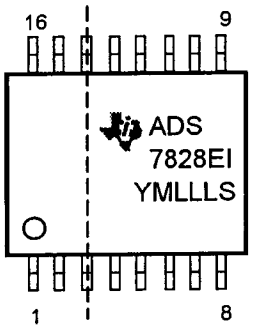
Data Sheet #
データシート番号 : **SBAS456**

Please refer to the Data sheets on below Definition.
データシートについては、下記対象項目をご参照ください。

Effective Device 該当製品名	:	**ADS7828EIPWRQ1**	
Effective Package 該当パッケージ	:	**PW**	Package (Please refer to MECHANICAL DATA.) パッケージ(外形寸法図をご参照ください。)
Effective Grade 該当グレード	:	-	

Symbolization Specification
捺印仕様

(TOP VIEW)



ADS7828EI	:	DEVICE CODE
Y	:	YEAR CODE (1, 2, 3, 4, 5, 6, 7, 8, 9, 0)
M	:	MONTH CODE (1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C)
LLLL	:	LOT TRACE CODE
S	:	ASSEMBLY SITE CODE

12-BIT 8-CHANNEL SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH I²C™ INTERFACE

FEATURES

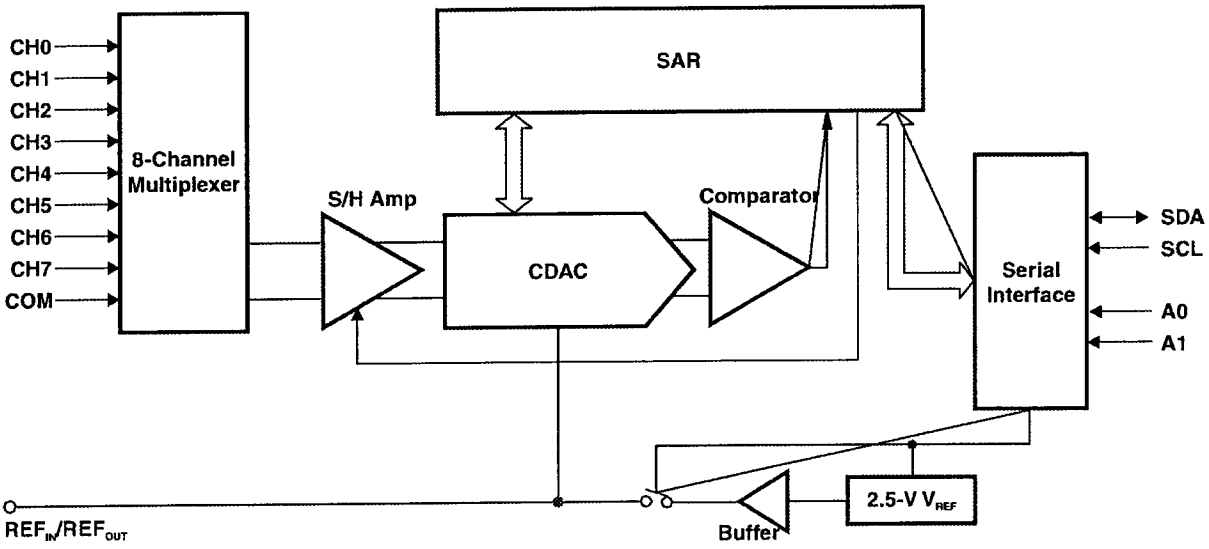
- Qualified for Automotive Applications
- 8-Channel Multiplexer
- 50-kHz Sampling Rate
- No Missing Codes
- 2.7-V to 5-V Operation
- Internal 2.5-V Reference
- I²C™ Interface Supports Standard, Fast, and High-Speed Modes
- TSSOP-16 Package

APPLICATIONS

- Voltage-Supply Monitoring
- Isolated Data Acquisition
- Transducer Interfaces
- Battery-Operated Systems
- Remote Data Acquisition

DESCRIPTION

The ADS7828 is a single-supply low-power 12-bit data acquisition device that features a serial I²C interface and an 8-channel multiplexer. The analog-to-digital (A/D) converter features a sample-and-hold amplifier and internal asynchronous clock. The combination of an I²C serial 2-wire interface and micropower consumption makes the ADS7828 ideal for applications requiring the A/D converter to be close to the input source in remote locations and for applications requiring isolation. The ADS7828 is available in a TSSOP-16 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

I2C is a trademark of NXP Semiconductors.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

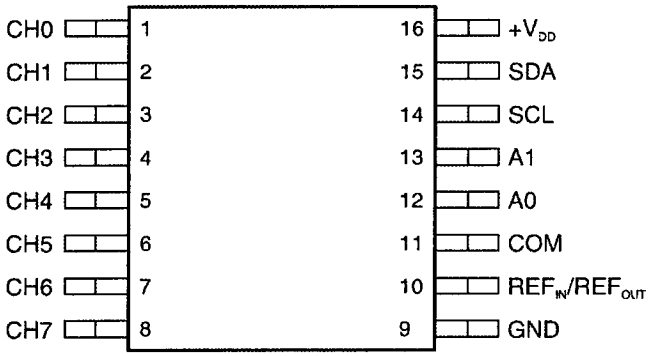
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	±2	TSSOP – PW	Reel of 2500	ADS7828EIPWRQ1	7828EI
	±1			ADS7828EBIPWRQ1	B 7828EI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PW PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
CH0	1	Analog input channel 0
CH1	2	Analog input channel 1
CH2	3	Analog input channel 2
CH3	4	Analog input channel 3
CH4	5	Analog input channel 4
CH5	6	Analog input channel 5
CH6	7	Analog input channel 6
CH7	8	Analog input channel 7
GND	9	Analog ground
REF_{IN}/REF_{OUT}	10	Internal 2.5-V reference / external reference input
COM	11	Common to analog input channel
A0	12	Slave address bit 0
A1	13	Slave address bit 1
SCL	14	Serial clock
SDA	15	Serial data
$+V_{DD}$	16	Power supply, 3.3 V (nominal)

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage		–0.3 V to 6 V
V_{IN}	Digital input voltage		–0.3 V to ($+V_{DD}$ + 0.3 V)
θ_{JA}	Thermal impedance, junction to free air(3)(4)		108.4°C/W
T_A	Operating free-air temperature		–40°C to 85°C
T_J	Operating virtual-junction temperature		150°C
T_{stg}	Storage temperature		–65°C to 150°C
T_{lead}	Lead temperature during soldering	Vapor phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND terminal.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

		TEST CONDITIONS	RATING
ESD	Electrostatic discharge rating	Human-Body Model (HBM)	2000 V
		Machine Model (MM)	200 V
		Charged-Device Model (CDM)	1000 V

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$+V_{DD}$	Supply voltage	2.7-V nominal	2.7		3.6	V
		5-V nominal	4.75	5	5.25	
V_{IN}	Analog input voltage	Positive input	–0.2		$+V_{DD}$ + 0.2	V
		Negative input	–0.2		0.2	
		Full-scale differential (Positive input – Negative input)	0		V_{REF}	V
$V_{IN(REF)}$	Voltage reference input voltage		0.05		$+V_{DD}$	V
V_{IH}	High-level digital input voltage		0.7 × $+V_{DD}$		$+V_{DD}$ + 0.5	V
V_{IL}	Low-level digital input voltage		–0.3		0.3 × $+V_{DD}$	V
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

+V_{DD} = 2.7 V, V_{REF} = 2.5 V, SCL clock frequency = 3.4 MHz (high-speed mode), over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS7828E			ADS7828EB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Analog Input									
I_{leak}	Leakage current			±1			±1		µA
C_i	Input capacitance			25			25		pF
Overall Performance									
	No missing codes		12			12			bits
	Integral linearity error			±1	±2		±0.5	±1	LSB(1)
	Differential linearity error			±1			±0.5	–1/+2	LSB
	Offset error			±1	±3		±0.75	±2	LSB
	Offset error match			±0.2	±1		±0.2	±1	LSB
	Gain error			±1	±4		±0.75	±3	LSB
	Gain error match			±0.2	±1		±0.2	±1	LSB
V_n	Noise	RMS		33			33		µV
PSRR	Power-supply ripple rejection			82			82		dB
Sampling Dynamics									
	Throughput frequency	High-speed mode: SCL = 3.4 MHz			50			50	kHz
		Fast mode: SCL = 400 kHz			8			8	
		Standard mode: SCL = 100 kHz			2			2	
	Conversion time			6			6		µs
AC Accuracy									
THD	Total harmonic distortion(2)	V_{IN} = 2.5 V_{PP} at 10 kHz		–82			–82		dB
	Signal-to- ratio	V_{IN} = 2.5 V_{PP} at 10 kHz		72			72		dB
	Signal-to-(noise+distortion) ratio	V_{IN} = 2.5 V_{PP} at 10 kHz		71			71		dB
	Spurious-free dynamic range	V_{IN} = 2.5 V_{PP} at 10 kHz		86			86		dB
	Channel-to-channel isolation			120			120		dB
Voltage Reference Output									
V_O	Output voltage		2.475	2.5	2.525	2.475	2.5	2.525	V
	Internal reference drift			15			15		ppm/°C
z_o	Output impedance	Internal reference on		110			110		Ω
		Internal reference off		1			1		GΩ
I_Q	Quiescent current			850			850		µA
Voltage Reference Input									
r_i	Input resistance			1			1		GΩ
	Current drain			20			20		µA
Digital Input/Output									
V_{OL}	Low-level output voltage	Minimum 3-mA sink current			0.4			0.4	V
I_{IH}	High-level input current	V_{IH} = +V_{DD} + 0.5 V			10			10	µA
I_{IL}	Low-level input current	V_{IL} = –0.3 V	–10			–10			µA

(1) LSB means least significant bit; with V_{REF} equal to 2.5 V, one LSB is 610 µV.
(2) THD is measured to the ninth harmonic.

ELECTRICAL CHARACTERISTICS (continued)

$+V_{DD}$ = 2.7 V, V_{REF} = 2.5 V, SCL clock frequency = 3.4 MHz (high-speed mode), over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS7828E			ADS7828EB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply									
I_Q	Quiescent current	High-speed mode: SCL = 3.4 MHz		225	320		225	320	µA
		Fast mode: SCL = 400 kHz		100			100		
		Standard mode: SCL = 100 kHz		60			60		
P_D	Power dissipation	High-speed mode: SCL = 3.4 MHz		675	1000		675	1000	µW
		Fast mode: SCL = 400 kHz		300			300		
		Standard mode: SCL = 100 kHz		180			180		
	Power-down current with wrong address selected	High-speed mode: SCL = 3.4 MHz		70			70		µA
		Fast mode: SCL = 400 kHz		25			25		
		Standard mode: SCL = 100 kHz		6			6		
I_{PD}	Full power-down current	SCL pulled high, SDA pulled high		400	3000		400	3000	nA

ELECTRICAL CHARACTERISTICS

+V_{DD} = 5 V, V_{REF} = External 5 V, SCL clock frequency = 3.4 MHz (high-speed mode), over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS7828E			ADS7828EB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Analog Input									
I_{leak}	Leakage current			±1			±1		µA
C_i	Input capacitance			25			25		pF
Overall Performance									
	No missing codes		12			12			bits
	Integral linearity error			±1	±2		±0.5	±1	LSB(1)
	Differential linearity error			±1			±0.5	–1/+2	LSB
	Offset error			±1	±3		±0.75	±2	LSB
	Offset error match				±1.5			±1	LSB
	Gain error			±1	±3		±0.75	±2	LSB
	Gain error match				±1			±1	LSB
V_n	Noise	RMS		33			33		µV
PSRR	Power-supply ripple rejection			82			82		dB
Sampling Dynamics									
	Throughput frequency	High-speed mode: SCL = 3.4 MHz			50			50	kHz
		Fast mode: SCL = 400 kHz			8			8	
		Standard mode: SCL = 100 kHz			2			2	
	Conversion time			6			6		µs
AC Accuracy									
THD	Total harmonic distortion(2)	V_{IN} = 2.5 V_{PP} at 10 kHz		–82			–82		dB
	Signal-to- ratio	V_{IN} = 2.5 V_{PP} at 10 kHz		72			72		dB
	Signal-to-(noise+distortion) ratio	V_{IN} = 2.5 V_{PP} at 10 kHz		71			71		dB
	Spurious-free dynamic range	V_{IN} = 2.5 V_{PP} at 10 kHz		86			86		dB
	Channel-to-channel isolation			120			120		dB
Voltage Reference Output									
V_O	Output voltage		2.475	2.5	2.525	2.475	2.5	2.525	V
	Internal reference drift			15			15		ppm/°C
z_o	Output impedance	Internal reference on		110			110		Ω
		Internal reference off		1			1		GΩ
I_Q	Quiescent current			1300			1300		µA
Voltage Reference Input									
r_i	Input resistance			1			1		GΩ
	Current drain			20			20		µA
Digital Input/Output									
V_{OL}	Low-level output voltage	Minimum 3-mA sink current			0.4			0.4	V
I_{IH}	High-level input current	V_{IH} = +V_{DD} + 0.5 V			10			10	µA
I_{IL}	Low-level input current	V_{IL} = –0.3 V	–10			–10			µA

(1) LSB means least significant bit; with V_{REF} equal to 5 V, one LSB is 1.22 mV.
(2) THD is measured to the ninth harmonic.

ELECTRICAL CHARACTERISTICS (continued)

$+V_{DD}$ = 5 V, V_{REF} = External 5 V, SCL clock frequency = 3.4 MHz (high-speed mode), over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS7828E			ADS7828EB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply									
I_Q	Quiescent current	High-speed mode: SCL = 3.4 MHz		750	1000		750	1000	µA
		Fast mode: SCL = 400 kHz		300			300		
		Standard mode: SCL = 100 kHz		150			150		
P_D	Power dissipation	High-speed mode: SCL = 3.4 MHz		3.75	5		3.75	5	µW
		Fast mode: SCL = 400 kHz		1.5			1.5		
		Standard mode: SCL = 100 kHz		0.75			0.75		
	Power-down current with wrong address selected	High-speed mode: SCL = 3.4 MHz		400			400		µA
		Fast mode: SCL = 400 kHz		150			150		
		Standard mode: SCL = 100 kHz		35			35		
I_{PD}	Full power-down current	SCL pulled high, SDA pulled high		400	3000		400	3000	nA

SWITCHING CHARACTERISTICS[1][2]

+V_{DD} = 2.7 V, over operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	
		High-speed mode	C_b = 100 pF max		3.4	MHz
			C_b = 400 pF max		1.7	
t_{BUF}	Bus free time between Stop and Start conditions	Standard mode		4.7		µs
		Fast mode		1.3		
$t_{HD;\ STA}$	Hold time (repeated) Start condition	Standard mode		4		µs
		Fast mode		600		ns
		High-speed mode		160		
t_{low}	Low period of the SCL clock	Standard mode		4.7		µs
		Fast mode		1.3		
		High-speed mode[3]	C_b = 100 pF max	160		ns
			C_b = 400 pF max	320		
t_{high}	High period of the SCL clock	Standard mode		4		µs
		Fast mode		600		ns
		High-speed mode[3]	C_b = 100 pF max	60		
			C_b = 400 pF max	120		
$t_{SU;\ STA}$	Setup time for a repeated Start condition	Standard mode		4.7		µs
		Fast mode		600		ns
		High-speed mode		160		
$t_{SU;\ DAT}$	Data setup time	Standard mode		250		ns
		Fast mode		100		
		High-speed mode		10		
$t_{HD;\ DAT}$	Data hold time	Standard mode		0	3.45	µs
		Fast mode		0	0.9	
		High-speed mode[3][4]	C_b = 100 pF max	0	82	ns
			C_b = 400 pF max	0	162	
t_{rCL}	Rise time of SCL signal	Standard mode			1000	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode[3]	C_b = 100 pF max	10	40	
			C_b = 400 pF max	20	80	
t_{rCL1}	Rise time of SCL signal after a repeated Start condition and after an acknowledge bit	Standard mode			1000	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode[3]	C_b = 100 pF max	10	80	
			C_b = 400 pF max	20	160	
t_{fCL}	Fall time of SCL signal	Standard mode			300	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode[3]	C_b = 100 pF max	10	40	
			C_b = 400 pF max	20	80	

(1) All values referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.
(2) Not production tested, except for the parameter $t_{HD;\ DAT}$, data hold time, high-speed mode, C_b = 100 pF max.
(3) For bus line loads (C_B) between 100 pF and 400 pF, the timing parameters must be linearly interpolated.
(4) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

SWITCHING CHARACTERISTICS (continued)

+V_{DD} = 2.7 V, over operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{rDA}	Rise time of SDA signal	Standard mode			1000	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode(3)	C_b = 100 pF max	10	80	
			C_b = 400 pF max	20	160	
t_{fDA}	Fall time of SDA signal	Standard mode			300	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode(3)	C_b = 100 pF max	10	80	
			C_b = 400 pF max	20	160	
$t_{SU;\ STO}$	Setup time for Stop condition	Standard mode		4		µs
		Fast mode		600		ns
		High-speed mode		160		
C_b	Capacitive load for SDA or SCL				400	pF
t_{SP}	Pulse width of spike suppressed	Fast mode			50	ns
		High-speed mode			10	
V_{nH}	Noise margin at the high level for each connected device (including hysteresis)			0.2 × V_{DD}		V
V_{nL}	Noise margin at the low level for each connected device (including hysteresis)			0.1 × V_{DD}		V

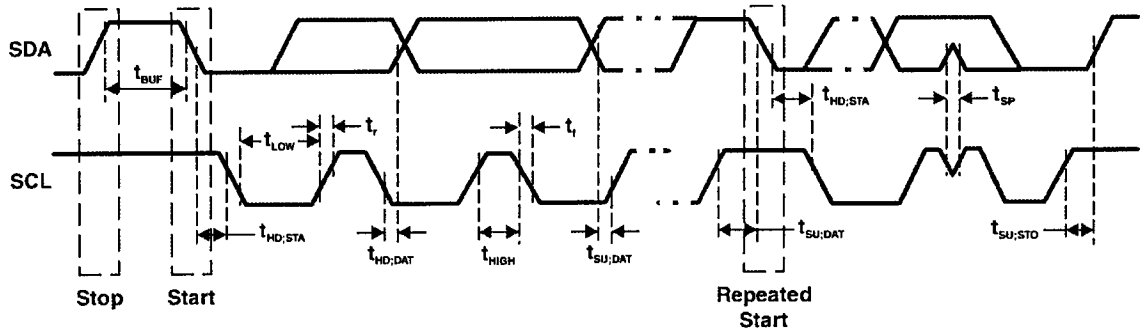
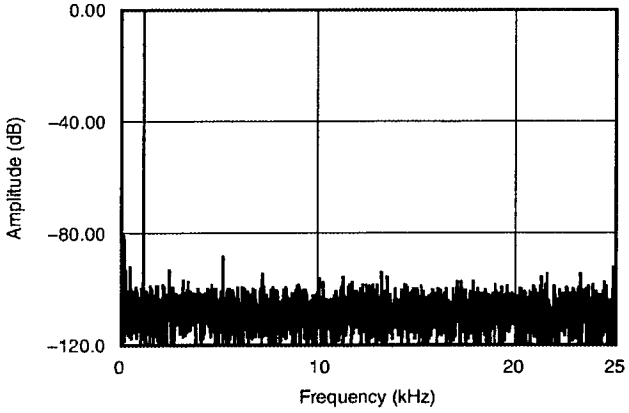


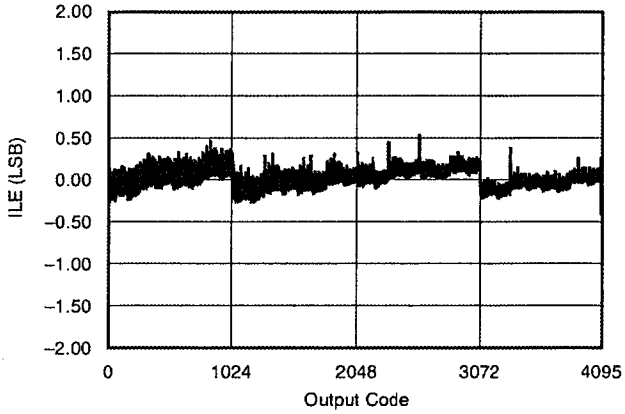
Figure 1. I²C Timing

TYPICAL CHARACTERISTICS

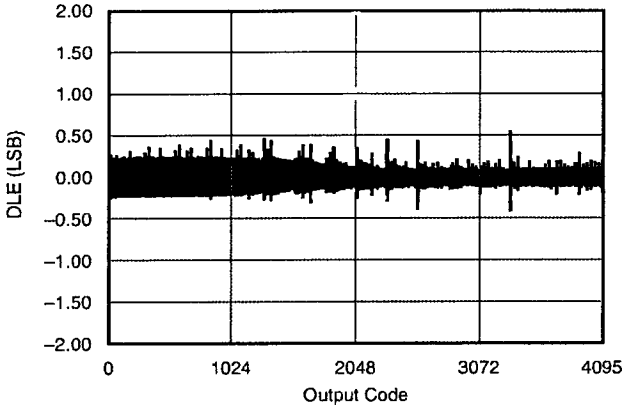
FREQUENCY SPECTRUM
(4096 Point FFT: f_{IN} = 1 kHz, 0 dB)



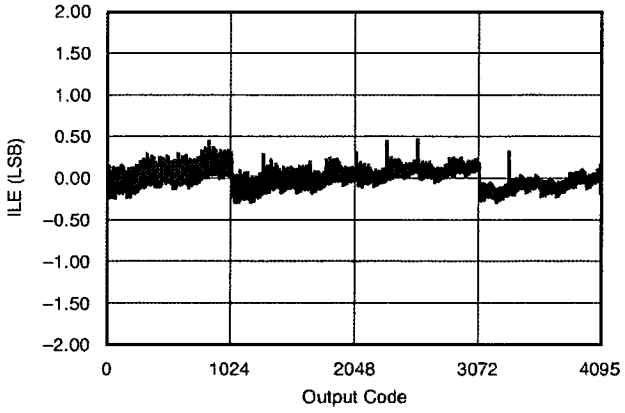
INTEGRAL LINEARITY ERROR vs CODE
(2.5V Internal Reference)



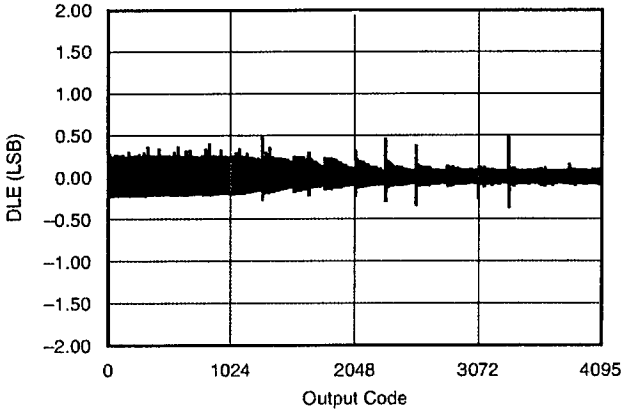
DIFFERENTIAL LINEARITY ERROR vs CODE
(2.5-V Internal Reference)



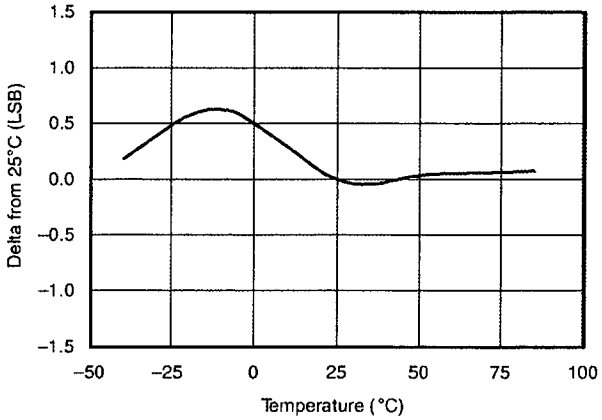
INTEGRAL LINEARITY ERROR vs CODE
(2.5-V External Reference)



DIFFERENTIAL LINEARITY ERROR vs CODE
(2.5-V External Reference)

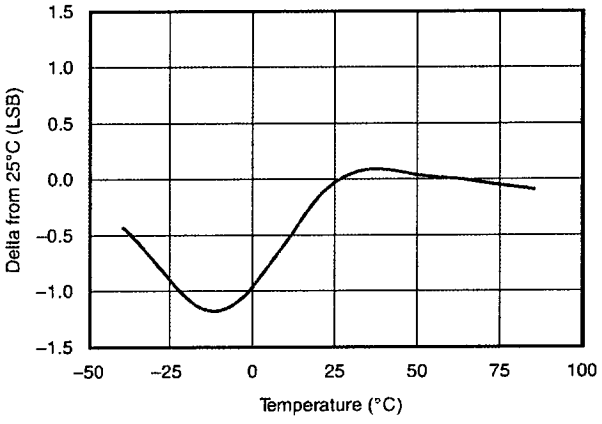


CHANGE IN OFFSET vs TEMPERATURE

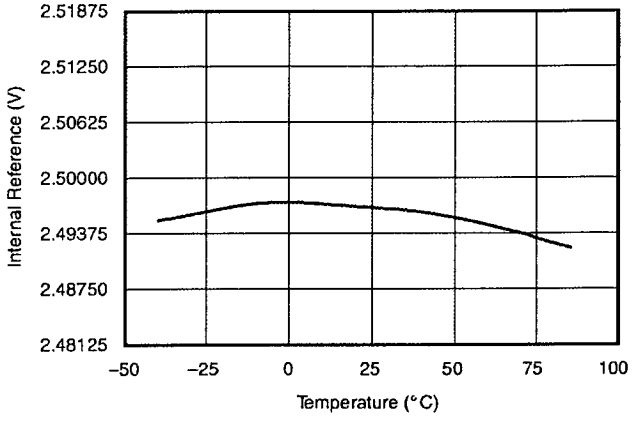


TYPICAL CHARACTERISTICS (continued)

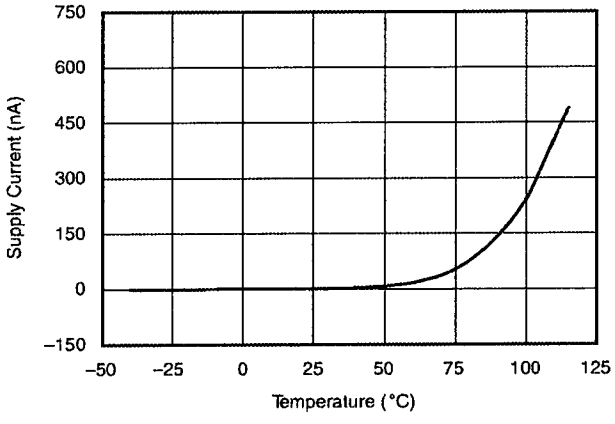
CHANGE IN GAIN vs TEMPERATURE



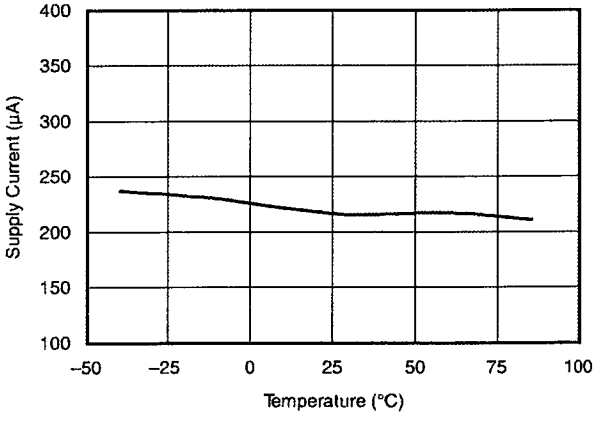
INTERNAL REFERENCE vs TEMPERATURE



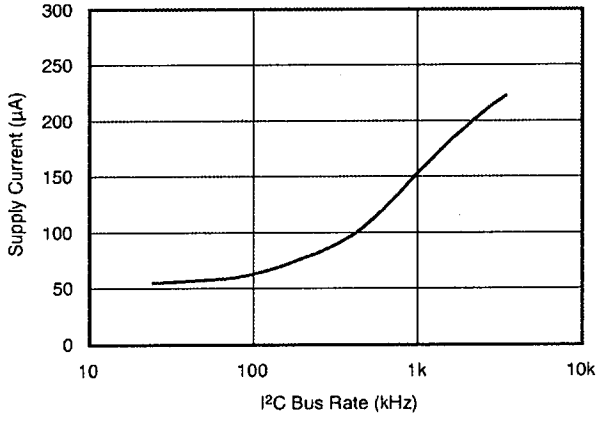
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



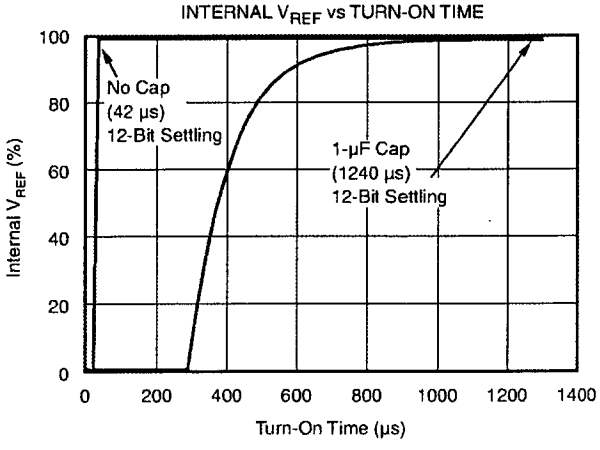
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs I²C BUS RATE



INTERNAL V_{REF} vs TURN-ON TIME



DEVICE INFORMATION

The ADS7828 is a classic Successive Approximation Register (SAR) A/D converter. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6μ CMOS process.

The ADS7828 core is controlled by an internally generated free-running clock. When the ADS7828 is not performing conversions or being addressed, it keeps the A/D converter core powered off, and the internal clock does not operate.

The simplified diagram of input and output for the ADS7828 is shown in Figure 2.

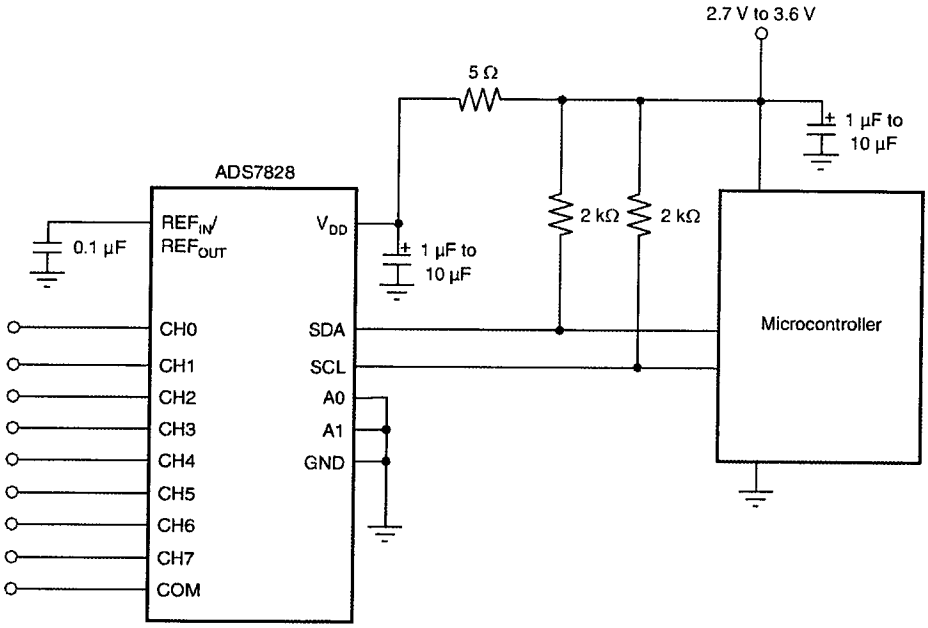


Figure 2. Simplified I/O Diagram

Analog Input

When the converter enters the hold mode, the voltage on the selected CHx pin is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25 pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

Reference

The ADS7828 can operate with an internal 2.5-V reference or an external reference. If a 5-V supply is used, an external 5-V reference is required in order to provide full dynamic range for a 0 V to $+V_{DD}$ analog input. This external reference can be as low as 50 mV. When using a 2.7-V supply, the internal 2.5-V reference will provide full dynamic range for a 0 V to $+V_{DD}$ analog input.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 2.5-V reference, the internal noise of the converter typically contributes only 0.32 LSB peak-to-peak of potential error to the output code. When the external reference is 50 mV, the potential error contribution from the internal noise is 50 times larger—16 LSBs. The errors due to the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

Digital Interface

The ADS7828 supports the I^2C serial bus and data transmission protocol, in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the Start and Stop conditions. The ADS7828 operates as a slave on the I^2C bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figure 3):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

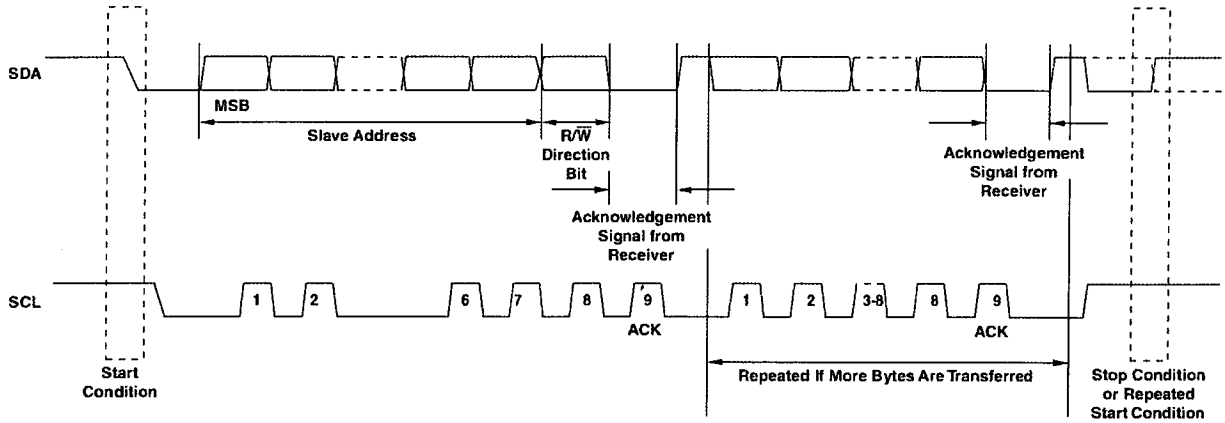


Figure 3. Basic Operation

Accordingly, the following bus conditions have been defined:

- Bus Not Busy

  Both data and clock lines remain high.
- Start Data Transfer

  A change in the state of the data line, from high to low, while the clock is high, defines a Start condition.
- Stop Data Transfer

  A change in the state of the data line, from low to high, while the clock line is high, defines the Stop condition.
- Data Valid

  The state of the data line represents valid data, when, after a Start condition, the data line is stable for the duration of the high period of the clock signal. There is one clock pulse per bit of data.

  Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.

  Within the I^2C bus specifications a standard mode (100-kHz clock rate), a fast mode (400-kHz clock rate), and a highspeed mode (3.4-MHz clock rate) are defined. The ADS7828 works in all three modes.
- Acknowledge

  Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

  A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition.

Figure 3 shows how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

- Data transfer from a master transmitter to a slave receiver.
  The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- Data transfer from a slave transmitter to a master receiver.
  The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned.

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or a repeated Start condition. Since a repeated Start condition is also the beginning of the next serial transfer, the bus will not be released.

The ADS7828 may operate in the following two modes:

- Slave Receiver Mode
  Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. Start and Stop conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- Slave Transmitter Mode
  The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the ADS7828 while the serial clock is input on SCL. Start and Stop conditions are recognized as the beginning and end of a serial transfer.

Address Byte

The address byte is the first byte received following the Start condition from the master device (see Figure 4). The first five bits (MSBs) of the slave address are factory pre-set to 10010. The next two bits of the address byte are the device select bits, A1 and A0. Input pins (A1-A0) on the ADS7828 determine these two bits of the device address for a particular ADS7828. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.

MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/$\overline{W}$

Figure 4. Address Byte

The A1/A0 address inputs can be connected to V_{DD} or digital ground. The device address is set by the state of these pins upon power-up.

The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a 1, a read operation is selected; when set to a 0, a write operation is selected. Following the Start condition, the ADS7828 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bits, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The operating mode is determined by a command byte (see Figure 5).

MSB	6	5	4	3	2	1	LSB
SD	C2	C1	C0	PD1	PD0	X	X

Figure 5. Command Byte

SD: Single-ended or differential inputs
0 = Differential inputs
1 = Single-ended inputs

C2 to C0: Channel selections (see Table 1)

PD1, PD0: Power-down selection (see Table 2)

X: Unused

Table 1. Channel Selection Control Addressed by Command Byte

COMMAND BYTE INPUTS				CHANNEL SELECTIONS								
SD	C2	C1	C0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	0	+IN	–IN	—	—	—	—	—	—	—
0	0	0	1	—	—	+IN	–IN	—	—	—	—	—
0	0	1	0	—	—	—	—	+IN	–IN	—	—	—
0	0	1	1	—	—	—	—	—	—	+IN	–IN	—
0	1	0	0	–IN	+IN	—	—	—	—	—	—	—
0	1	0	1	—	—	–IN	+IN	—	—	—	—	—
0	1	1	0	—	—	—	—	–IN	+IN	—	—	—
0	1	1	1	—	—	—	—	—	—	–IN	+IN	—
1	0	0	0	+IN	—	—	—	—	—	—	—	–IN
1	0	0	1	—	—	+IN	—	—	—	—	—	–IN
1	0	1	0	—	—	—	—	+IN	—	—	—	–IN
1	0	1	1	—	—	—	—	—	—	+IN	—	–IN
1	1	0	0	—	+IN	—	—	—	—	—	—	–IN
1	1	0	1	—	—	—	+IN	—	—	—	—	–IN
1	1	1	0	—	—	—	—	—	+IN	—	—	–IN
1	1	1	1	—	—	—	—	—	—	—	+IN	–IN

Table 2. Power-Down Selection

PD1	PD0	DESCRIPTION
0	0	Power down between A/D converter conversions
0	1	Internal reference off and A/D converter on
1	0	Internal reference on and A/D converter off
1	1	Internal reference on and A/D converter on

Initiating Conversion

Provided the master has write-addressed it, the ADS7828 turns on the A/D converter section and begins conversions when it receives bit 4 of the command byte shown in Figure 5. If the command byte is correct, the ADS7828 returns an ACK condition.

Reading Data

Data can be read from the ADS7828 by read addressing the part (LSB of address byte set to 1) and receiving the transmitted bytes. Converted data can be read from the ADS7828 only after a conversion has been initiated as described in the preceding section.

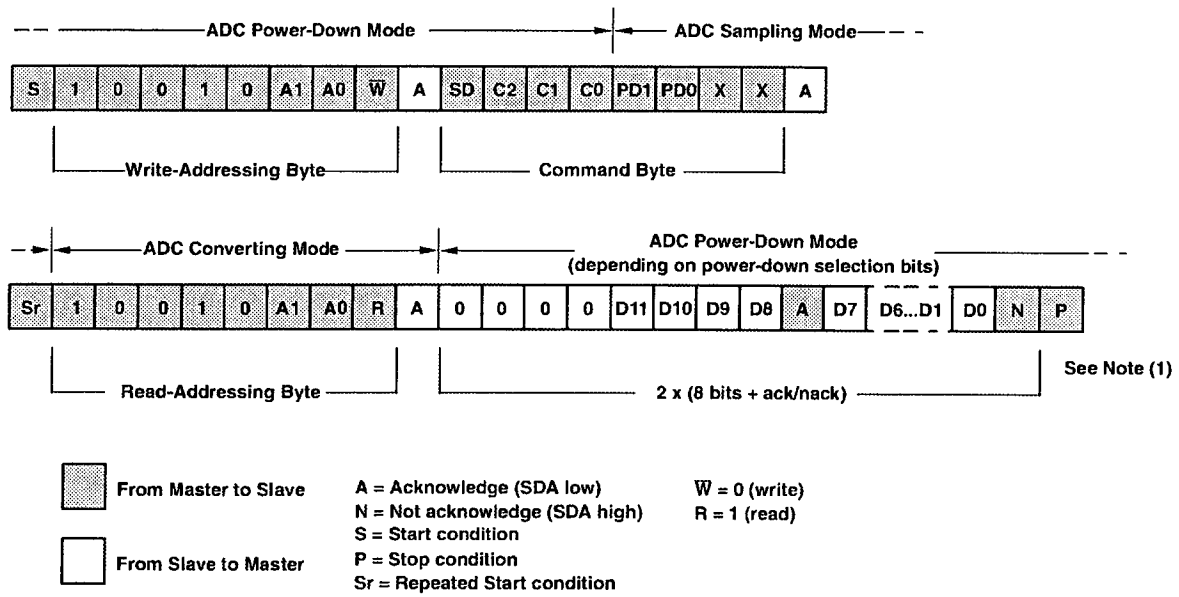
Each 12-bit data word is returned in two bytes (see Figure 6), where D11 is the MSB of the data word, and D0 is the LSB. Byte 0 is sent first, followed by byte 1.

	MSB	6	5	4	3	2	1	LSB
Byte 0	0	0	0	0	D11	D10	D9	D8
Byte 1	D7	D6	D5	D4	D3	D2	D1	D0

Figure 6. Reading Data

Reading in Fast or Standard (F/S) Mode

Figure 7 shows the interaction between the master and the slave ADS7828 in fast or standard (F/S) mode. At the end of reading conversion data, the ADS7828 can be issued a repeated Start condition by the master to secure bus operation for subsequent conversions of the A/D converter. This would be the most efficient way to perform continuous conversions.



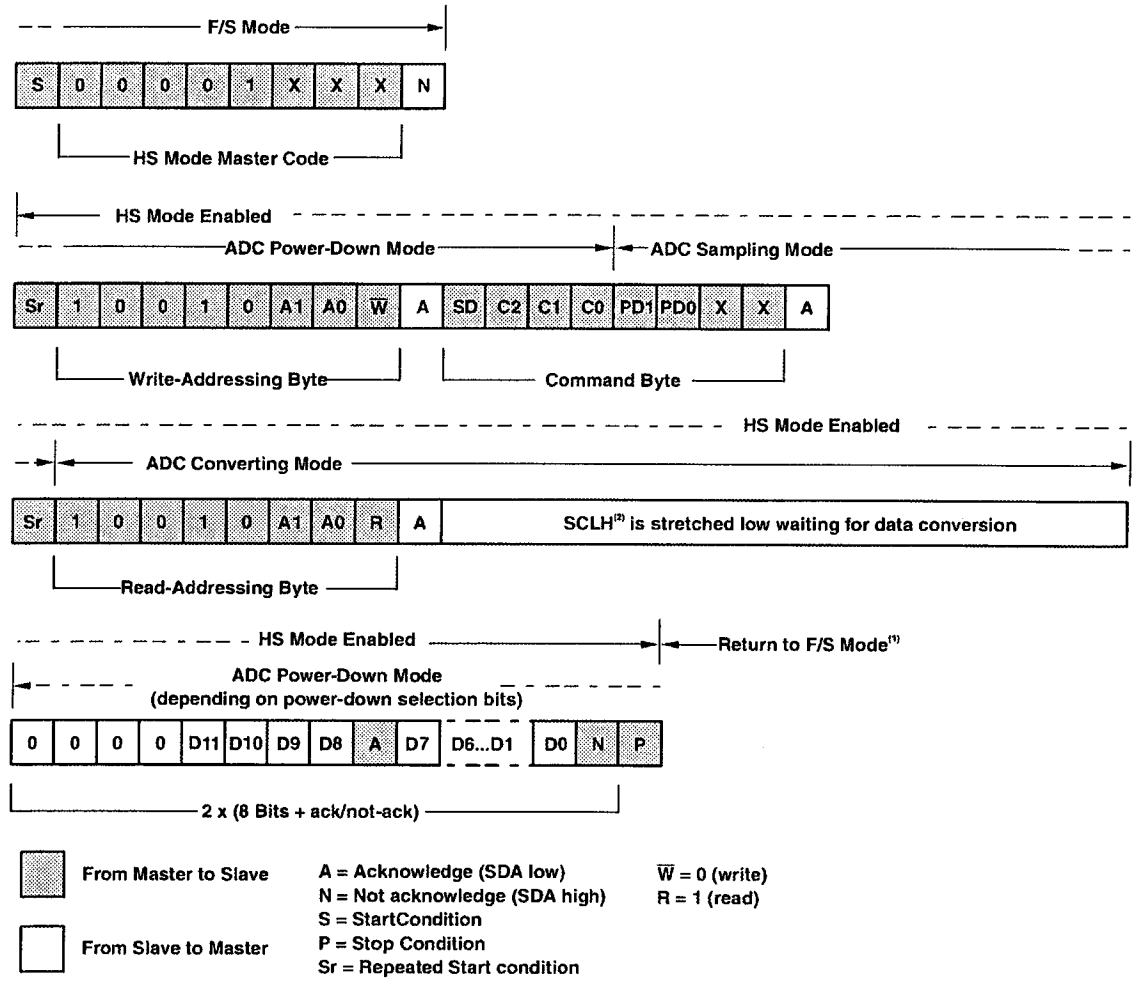
NOTE: (1) To secure bus operation and loop back to the stage of write-addressing for next conversion, use Repeated Start.

Figure 7. Typical Read Sequence in F/S Mode

Reading in High-Speed (HS) Mode

High Speed (HS) mode is fast enough that codes can be read out one at a time. In HS mode, there is not enough time for a single conversion to complete between the reception of a repeated Start condition and the read-addressing byte, so the ADS7828 stretches the clock after the read-addressing byte has been fully received, holding it low until the conversion is complete.

See Figure 8 for a typical read sequence for HS mode. Included in the read sequence is the shift from F/S to HS modes. It may be desirable to remain in HS mode after reading a conversion; to do this, issue a repeated Start instead of a Stop at the end of the read sequence, since a Stop causes the part to return to F/S mode.



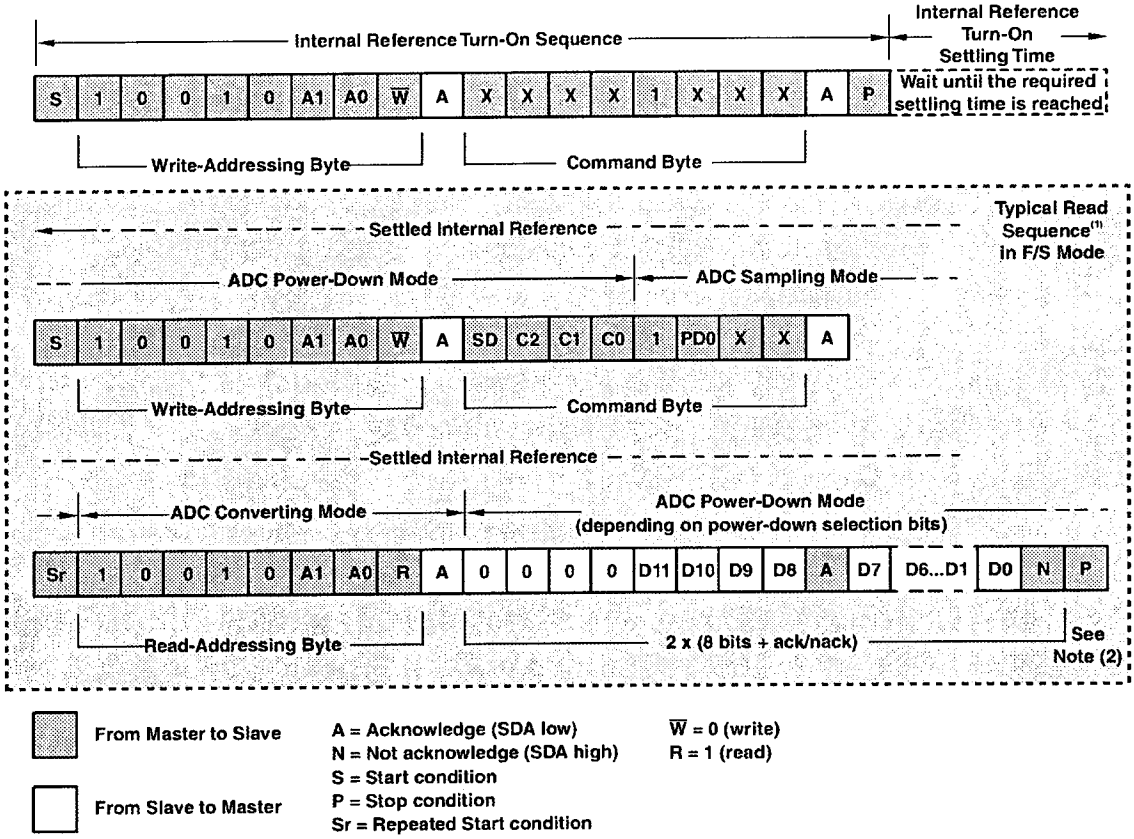
NOTES: (1) To remain in HS mode, use Repeated Start instead of Stop.
(2) SCLH is SCL in HS mode.

Figure 8. Typical Read Sequence in HS Mode

Reading With Reference On/Off

The internal reference defaults to off when the ADS7828 power is on. To turn the internal reference on or off, see Table 2. If the reference (internal or external) is constantly turned on and off, a proper amount of settling time must be added before a normal conversion cycle can be started. The exact amount of settling time needed varies depending on the configuration.

See Figure 9 for an example of the proper internal reference turn-on sequence before issuing the typical read sequences required for the F/S mode when an internal reference is used.



NOTES: (1) Typical read sequences can be reused after the internal reference is settled.
(2) To secure bus operation and loop back to the stage of write-addressing for next conversion, use Repeated Start.

Figure 9. Internal Reference Turn-On Sequence and Typical Read Sequence (F/S Mode Shown)

When using an internal reference, there are three things that must be done:

1. To use the internal reference, the PD1 bit of Command Byte must always be set to logic 1 for each sample conversion that is issued by the sequence, as shown in Figure 7.
2. To achieve 12-bit accuracy conversion when using the internal reference, the internal reference settling time must be considered, as shown in the Internal VREF vs Turn-On Time Typical Characteristic plot. If the PD1 bit has been set to logic 0 while using the ADS7828, then the settling time must be reconsidered after PD1 is set to logic 1. In other words, whenever the internal reference is turned on after it has been turned off, the settling time must be long enough to get 12-bit accuracy conversion.
3. When the internal reference is off, it is not turned on until both the first Command Byte with PD1 = 1 is sent and then a Stop condition or repeated Start condition is issued. (The actual turn-on time occurs once the Stop or repeated Start condition is issued.) Any Command Byte with PD1 = 1 issued after the internal reference is turned on serves only to keep the internal reference on. Otherwise, the internal reference would be turned off by any Command Byte with PD1 = 0.

The example in Figure 9 can be generalized for an HS mode conversion cycle by changing the timing of the conversion cycle. If using an external reference, PD1 must be set to 0, and the external reference must be settled. The typical sequence in Figure 7 or Figure 8 can then be used.

PCB Layout

For optimum performance, care should be taken with the physical layout of the ADS7828 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an "n-bit" SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices.

With this in mind, power to the ADS7828 should be clean and well-bypassed. A 0.1-μF ceramic bypass capacitor should be placed as close to the device as possible. A 1-μF to 10-μF capacitor may also be needed if the impedance of the connection between $+V_{DD}$ and the power supply is high.

The ADS7828 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50 Hz or 60 Hz) can be difficult to remove.

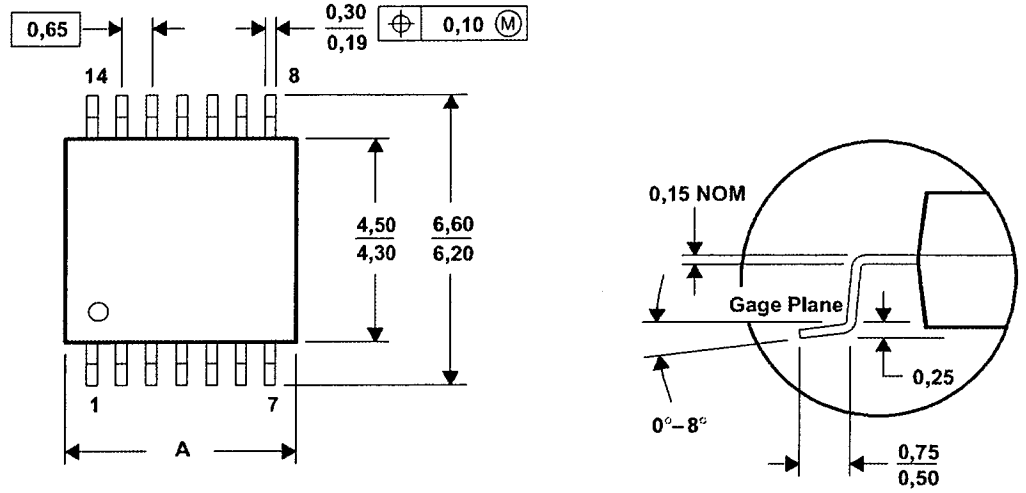
The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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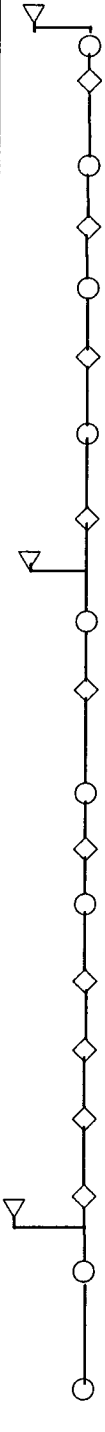
TEXAS INSTRUMENTS

Q C CHART

● WAFAR FABRICATION

FLOW	PROCESS STEP	PROCESS CONTROL	INSPECTION ITEM	INSPECTION	RESPONCE	SPEC
	OXIDATION		OXIDATION CONDITOIN	TEMP/TIME	MFG	TI SPEC
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	PHOTOLITO -GRAPHY		FORM CONDITION	REGISTER APPLICATION	MFG	TI SPEC
				EXPOSURE AMOUNT		
				ETCHING TIME		
		PATTARNING		VISUAL		
	DIFFUSION		DIFFUSION CONDITION	TIME	MFG	TI SPEC
				GAS FLUX		
		DIFFUSION CONDITION		THICKNESS/VISUAL		
				Rho-s		
	EPITAXIAL		EPITAXIAL CONDITION	TEMP/TIME	MFG	TI SPEC
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		EPITAXIAL QUALITY		VISUAL		
				THICKNESS		
				RESISTANCE RATIO		
	METALIZA- TION		METALIZATION CONDITION	TEMO/TIME	MFG	TI SPEC
				VACUUM RATIO		
		METALIZATION QUALITY		VISUAL		
				THICKNESS		
	METAL ETCHING		FORM CONDITION	REGISTER APPLICATION	MFG	TI SPEC
				EXPOSURE AMOUNT		
				ETCHING TIME		
		PATTARNING		VISUAL		
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		QUALITY		REFRACTIVE		
				THICKNESS		
	TEST PROBE	ELEC		Tr PARAMETER	MFG	TI SPEC
				RESISTANCE		
	ELEC TEST		PROGRAM	YEILD	MFG	TI SPEC
			TESTER			
	SHIP CHECK	VISUAL		VISUAL DEFECTS	QRA	TI SPEC
			LOT HISTORY	TRAVELLER		
	PACK	DEVICE/QTY		VISUAL	MFG	TI SPEC
			SPECIAL SPEC			
		DEVICE/QTY	SHIPPING PLAN			
			SHIPPING CUSTOMER			

※OXIDATION, PHOTOLITHOGRAPHY AND DIFFUSION ARE REPEATED SEVRAL TIMES BY DEVICE.

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Sales & Applications Quality

TEXAS INSTRUMENTS

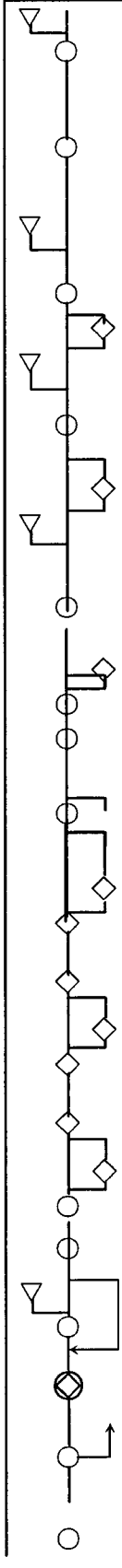
Ｑ Ｃ 工 程 図

● ウェハー工程

フロー	工程名	管理項目	点検項目	検査項目	実施部門	標準類	備考
▽	酸化		生成条件	時間・温度	製造	社内標準による	※酸化、フォトリソグラフィー、拡散工程は製品により数回くり返し行なわれる。 ※コンピューターに必要事項をインプットすることによりステップトラベラーが発行される。
				ガス流量			
		酸化膜の品質		酸化膜厚･外観			
	フォトリソグラフィー		形成条件	レジスト塗布	製造	社内標準による	
				露光量			
				エッチング時間			
		パターン形状		外観			
	拡散		生成条件	時間	製造	社内標準による	
				ガス流量			
		拡散の状態		酸化膜厚･外観			
				シート抵抗			
	エピタキシャル		生成条件	時間・温度	製造	社内標準による	
				ガス流量			
		エピ層の品質		外観			
				エピ層の厚み			
				比抵抗			
▽	メタライゼーション		生成条件	時間・温度	製造	社内標準による	
				真空度			
		金属膜の品質		外観			
				金属膜厚			
	配線形成		形成条件	レジスト塗布	製造	社内標準による	
				露光量			
				エッチング時間			
		パターン形成		外観			
	保護膜生成		生成条件	時間・温度	製造	社内標準による	
				ガス流量			
		保護膜の品質		屈折率			
				保護膜の厚み			
	素子特性検査	電気的特性		トランジスタ特性	製造	社内標準による	
				抵抗値			
	電気的特性検査		使用プログラム	歩留り	製造	社内標準による	
			テスター精度				
	出荷検査	外観特性		外観全般	品質保証	社内標準による	
			ロット履歴	トラベラー			
▽	梱包	デバイス/数量		梱包外観	製造	社内標準による	
			特殊仕様				
	各工程における異常発生時は、工程異常処理標準による。						
○	保管・出荷	デバイス/数量	出荷計画				
			出荷先				

TEXAS INSTRUMENTS

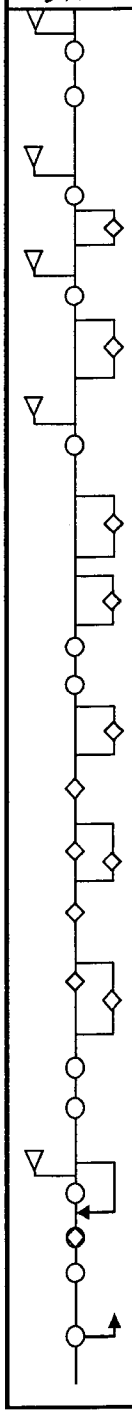
ADS7828EIPWRQ1 QC Chart



PROCESS STEP	PROCESS CONTROL	INSPECTION ITEM	INSPECTION	RESPONCE	SPEC
SETUP	PLAN DAILY CONTROL	DEVICE TYPE STATUS	TRAVELLER	MFG	TI SPEC
DIE PREP	CONDITION	SPEED/PITCH DI WATER RESISTIVITY	SET CONDITION	MFG	
	DICING		VISUAL DEFECTS		
DIE MOUNT	CONDITION	MATERIAL SURVEILLANCE	TEMP	MFG	
			SET CONDITION		
	MOUNT	CURE CONDITION	TEMP/TIME		
WIRE BOND	CONDITION		SET CONDITION	MFG	
		HEATER CONDITION	TEMP		
	BOND		VISUAL DEFECTS		
		WIRE PULL	BOND PULL		
MOLD	CONDITION	MATERIAL SURVEILLANCE		MFG	
		TEMP	VISUAL CONDITION		
		SPEED			
		CURE CONDITION	TEMP/TIME		
	MOLD		VISUAL DEFECTS		
X-Ray	CONDITION		VISUAL DEFECTS	MFG	TI SPEC
REFLOW	CONDITION	PROFILE	TEMP	MFG	TI SPEC
TRIM/FORM SIGULATE	SYMBOL CONDITION			MFG	
	TRIM/FORM CONDITION				
	TRIM/FORM		VISUAL DEFECTS		
85'C ELEC TEST	ELEC	PROGRAM TESTER,ALLUNITS	YIELD	MFG	TI SPEC
LOT ACCEPTANCE	ELEC	PROGRAM	DC/AC PARAMETER	QRA	TI SPEC
			MONITOR		
25'C ELEC TEST	ELEC	PROGRAM TESTER,ALLUNITS	YIELD	MFG	TI SPEC
LOT ACCEPTANCE	ELEC	PROGRAM	DC/AC PARAMETER	QRA	TI SPEC
			MONITOR		
DRY BAKE	CONDITION		TEMP	MFG	
STOCK IN	QTY	LOT HISTORY	TRAVELLER	MFG	
			SPECIAL SPEC		
TAPING	CONDITION	MATERIAL	DEVICE/QTY	MFG	
	TAPING		VISUAL DEFECTS		
SHIP CHECK	SHIPPING CUSTOMER		SPECIAL SPEC	QRA	
DRY PACK	DEVICE/QTY	SHIP PLAN		MFG	TI SPEC
	SHIPPING CUSTOMER	PACK LIST Shipping Information			
SHIP					

TEXAS INSTRUMENTS

ADS7828EIPWRQ1 QC工程図

フロー	工程名	管理項目	点検項目	検査項目	実施部門	関連標準
	ｾｯﾄｱｯﾌﾟ	生産・	ﾃﾞﾊﾞｲｽﾀｲﾌﾟ	ﾄﾗﾍﾞﾗｰ内容	製造	社内標準による
		日程管理	進捗度			
	ﾀﾞｲﾌﾞﾚｯﾌﾟ	ﾀﾞｲｼﾝｸﾞ条件	速度・ﾋﾟｯﾁ	設定条件	製造	社内標準による
			水の電導度			
		ﾀﾞｲｼﾝｸﾞ		外観(ﾁｯﾌﾟｸﾗｯｸ)		
	ﾀﾞｲﾏｳﾝﾄ	ﾏｳﾝﾄ条件	樹脂保管条件	温度	製造	社内標準による
				設定条件		
		ﾏｳﾝﾄ状態	ｷｭｱｰ条件	温度・時間		
	ﾜｲﾔｰﾎﾞﾝﾄﾞ	ﾎﾞﾝﾄﾞ条件		設定条件	製造	社内標準による
			ﾋｰﾀｰ条件	温度		
		ﾎﾞﾝﾄﾞ状態		外観(位置・形状)		
			配線強度	引っ張り強度		
	ﾌﾟﾗｽﾁｯｸ樹脂成形	ﾓｰﾙﾄﾞ条件	材料保管条件		製造	社内標準による
			金型温度	外観		
			ﾗﾑｽﾋﾟｰﾄﾞ	流れ中断・位置		
			ｷｭｱｰ条件	温度・時間		
		ﾓｰﾙﾄﾞ状態		外観全般		
	X線検査	X線条件		外観(断線)	製造	社内標準による
	リフロー	リフロー条件	リフロー条件	設定条件	製造	社内標準による
	捺印切断・形状成形	捺印条件			製造	社内標準による
		切断成形条件				
		切断成形状態		外観・特性		
	85℃電気的特性選別	電気特性	使用ﾌﾟﾛｸﾞﾗﾑ	歩留り	製造	社内標準による
			ﾃｽﾀｰ精度			
	出荷保証検査	電気特性	使用ﾌﾟﾛｸﾞﾗﾑ	DC/AC特性	品質保証	社内標準による
				初期故障モニター		
	25℃電気的特性選別	電気特性	使用プログラム	歩留まり	製造	社内標準による
			テスター精度			
	出荷保障検査	電気特性	使用プログラム	DC/AC特性	品質保証	社内基準による
				初期故障モニター		
			ロット履歴	ﾄﾗﾍﾞﾗｰ内容		
	ドライベイク	ベイク条件	温度		製造	社内基準による
	入庫	ﾃﾞﾊﾞｲｽ数量	ロット履歴	トラベラー	製造	社内標準による
				特殊仕様		
	テーピング	テーピング条件	使用材	デバイス・数量	製造	社内標準による
		テーピング状態		テーピング外観		
	出荷検査	出荷先		特殊仕様	品質保証	社内標準による
	梱包出荷	ﾃﾞﾊﾞｲｽ・数量	納品計画		製造	社内標準による
		出荷先	納品伝票			
	輸送・納品					
		各工程における異常発生時は、工程異常処理標準による。				

TEXAS INSTRUMENTS

リフロー条件について

対象製品：ADS7828EIPWRQ1

貴社より提示戴きました温度プロファイルにてリフロー２回まで推奨可能です。
参考として、弊社推奨実装条件を添付いたしますので参照下さい。

貴社リフロー条件：　250℃ 10sec, 230℃ 60sec

TEXAS INSTRUMENTS

Country of origin

Device name : ADS7828EIPWRQ1

Process	FAB Name	Country	Location
W/F FAB	TSMC(FAB2)	Taiwan	121, Park Ave. III, Hsinchu Science Based Industrial Park, Hsin-chu, Taiwan 300, R.O.C.
ASSY	TI Malaysia	Malaysia	No 1, Lorong Enggang 33, Ampang/Ulu Klang. Kuala Lumpur , 54200, Malaysia
TEST	TI Malaysia	Malaysia	No 1, Lorong Enggang 33, Ampang/Ulu Klang. Kuala Lumpur , 54200, Malaysia

原　産　国

製品名：ADS7828EIPWRQ1

工程	工場名	国名	所在地
前工程	TSMC(FAB2)	台湾	121, Park Ave. III, Hsinchu Science Based Industrial Park, Hsin-chu, Taiwan 300, R.O.C.
後工程	TI Malaysia	マレーシア	No 1, Lorong Enggang 33, Ampang/Ulu Klang. Kuala Lumpur , 54200, Malaysia
検査工程	TI Malaysia	マレーシア	No 1, Lorong Enggang 33, Ampang/Ulu Klang. Kuala Lumpur , 54200, Malaysia

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Automotive New Product Qualification Plan/Summary
(As per AEC-Q100 and JEDEC Guidelines)

Supplier Name:	Texas Instruments Inc.	**Supplier Wafer Fabrication Site:**	TSMC-WF2
Supplier Code:	ADS7828EIPWRQ1	**Supplier Die Rev:**	
Supplier Part Number:	ADS7828EIPWRQ1	**Supplier Assembly/Test Site:**	MLA
Customer Name:	Catalog	**Supplier Package/Pin:**	16/PW
Customer Part Number:	ADS7828EIPWRQ1	**Pb Free Lead Frame (Y/N):**	Y
Device Description:	Quad Opamp	**"Green" Mold Compound (Y/N):**	Y
MSL Rating:	Level-2	**Operating Temp Range:**	-40C to 85C
Peak Solder Reflow Temp:	260C	**Automotive Grade Level (1):**	3
Prepared by Signature:	Uma Annamalai	**Date:**	09/11/2008

Test	#	Reference	Test Conditions	Min Lots (2)	SS / lot (2)	Min Total (2)	Results Lot/pass/fail	Comments: (N/A =Not Applicable)	Exceptions to AEC -Q100
TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (3)									
PC	A1	JESD22 A113 J-STD-020	Preconditioning; SMD only; Moisture Preconditioning for THB/HAST, AC/UHST, TC, HTSL, & HTOL	Performed on ALL SMD devices, Prior to THB, AC, TC & PTC			All/0	QBS to A/T site and PW qual data	
HAST	A2	JESD22 A110	Highly Accelerated Stress Test: 130°C/85% 96 hours	3	77	231	3/231/0	QBS to A/T site and PW qual data	
AC	A3	JESD22 A102	Autoclave: 121C / 96 hours	3	77	231	3/231/0	QBS to A/T site and PW qual data	
TC	A4	JESD22 A104	Temperature Cycle: -65°C/+150°C/ 1000 cycles	3	77	231	3/231/0	QBS to A/T site and PW qual data	
PTC	A5	JESD22-A105	Power Temperature Cycle: -40°C to +125°C for 1000 cycles	1	45	45		N/A. Only applies to devices over 1 W	
HTSL	A6	JESD22 A103	High Temperature Storage Life: 170°C/420 hours (3)	1	45	45	3/231/0	QBS to A/T site and PW qual data	
TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS (3)									
HTOL	B1	JESD22 A108	High Temp Operating Life: 125°C/1000 hours **150°C/500 hours**	3	77	231	15/1772/0	refer to release doc	Pre- and Post Stress Electrical tests performed at room temp
ELFR	B2	AEC-Q100-008	Early Life Failure Rate: 125°C/48 hours **150°C/24hours**	3	800	2400	37/4550/0	refer to release doc	Pre- and Post Stress Electrical tests performed at room temp
TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS (3)									
WBS	C1	AEC-Q100-001	Wire Bond Shear Test: (Ppk > 1.67 and Cpk > 1.33)	30 bonds	5 parts Min.	30 bonds	1/30/0	QBS to Q100 data	
WBP	C2	Mil-Std-883 Method 2011	Wire Bond Pull: Each bonder used (Ppk > 1.67 and Cpk > 1.33)	30 bonds	5 parts Min.	30 bonds	1/30/0	QBS to Q100 data	
SD	C3	JESD22 B102	Solderability: (>95% coverage) 8 hr steam age	1	22	22	1/22/0	Pb SD PB free SD	
PD	C4	JESD22 B100, JESD22 B108	Physical Dimensions: (Ppk > 1.67 and Cpk > 1.33)	3	10	30	3/30/0	QBS to Q100 data	
SBS	C5	AEC-Q100-010	Solder Ball Shear: (Ppk > 1.67 and Cpk > 1.33)	50 balls	3	50		N/A to non-solder ball surface	

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								mount devices	
LI	C6	JESD22 B105 Not Required for SMT parts	Lead Integrity: (No lead cracking or breaking)	50 leads	1	50		N/A to non-solder ball surface mount devices	

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

Test	#	Reference	Test Conditions	Min Lots (2)	S.S. Per Lot (2)	Min Total (2)	Results Lot/pass/fail	Comments: (N/A =Not Applicable)	Exceptions to AEC -Q100
EM	D1	JESD61	Electromigration: (Only if de-rating required beyond design rules)	-	-	-		Data available	
TDDB	D2	JESD35	Time Dependant Dielectric Breakdown:	-	-	-		N/A	
HCI	D3	JESD60 & 28	Hot Injection Carrier	-	-	-		N/A	
TEST GROUP E- ELECTRICAL VERIFICATION									
TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test.	All	All	All		100% of qualification devices	
HBM	E2	AEC Q100-002	Electrostatic Discharge, Human Body Model	1	3	3	500V - 3/0 1000V – 3/0 1500V – 3/0 2000V-3/0		
MM	E2	AEC Q100-003	Machine Model:	1	3	3	50V – 3/0 100V – 3/0 150V – 3/0 200V-3/0		
CDM	E3	AEC Q100-011	Electrostatic Discharge, Charged Device Model; (750V corner leads, 500V for all other leads)	1	3	3	250V – 3/0 500V – 3/0 750V – 3/0 1000V-3/0		Performed per JEDEC
LU	E4	AEC-Q100-004	Latch-Up:	1	6	6	1/6/0		
ED	E5	AEC-Q100-009	Electrical Distributions: (Test across recommended operating temperature range) (Cpk > 1.67 , Ppk > 1.67)	1	30	30	-40C - 30/0 25C - 30/0 85C - 30/0		
ADDITIONAL INFORMATION									
MTBF FIT			Mean Time Between Failures Failures-in-Time. The number of failures per 10E9 device-hours. Estimated usage temperature = 55°C Statistical confidence level = 60% Activation Energy = 0.7 eV Summarized by technology	-	-	-	MTBF = $2.98 * 10^7$ FIT = 33.6		
DPPM			Defective Parts per Million Based on APG customer returns resulting in Corrective Action (N/A for New Products)	-	-	-	NA		

(1) Grade 0 (or A): -40°C to +150°C ambient operating temperature range
Grade 1 (or Q): -40°C to +125°C ambient operating temperature range
Grade 2 (or T): -40°C to +105°C ambient operating temperature range
Grade 3 (or I): -40°C to +85°C ambient operating temperature range
Grade 4 (or C): -0°C to +150°C ambient operating temperature range

(2) These are recommended minimum lot/sample sizes. Lot/sample size may be reduced depending on available data.

(3) Generic data may be used.

Quality and Reliability Data Disclaimer

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customer should provide adequate design and operating safeguards. Quality and reliability data

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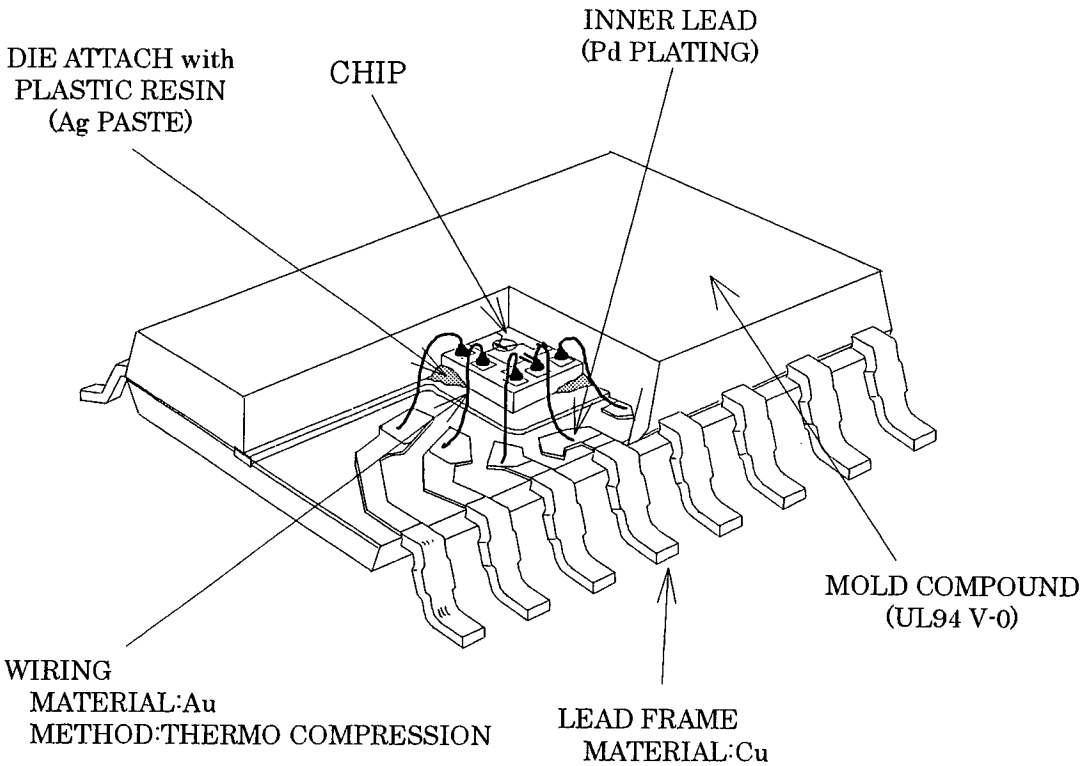
provided by Texas Instruments is intended to be an estimate of product performance based upon history only. It does not imply that any performance levels reflected in such data can be met if the product is operated outside the conditions expressly stated in the latest published data sheet or agreed-to customer specification for a device.

Reliability data shows characteristic failure mechanisms of the specific environmental stress as documented in the industry standards for each stress condition.

◆ STRUCTURE of PACKAGE

(TSSOP)

《 Example 》

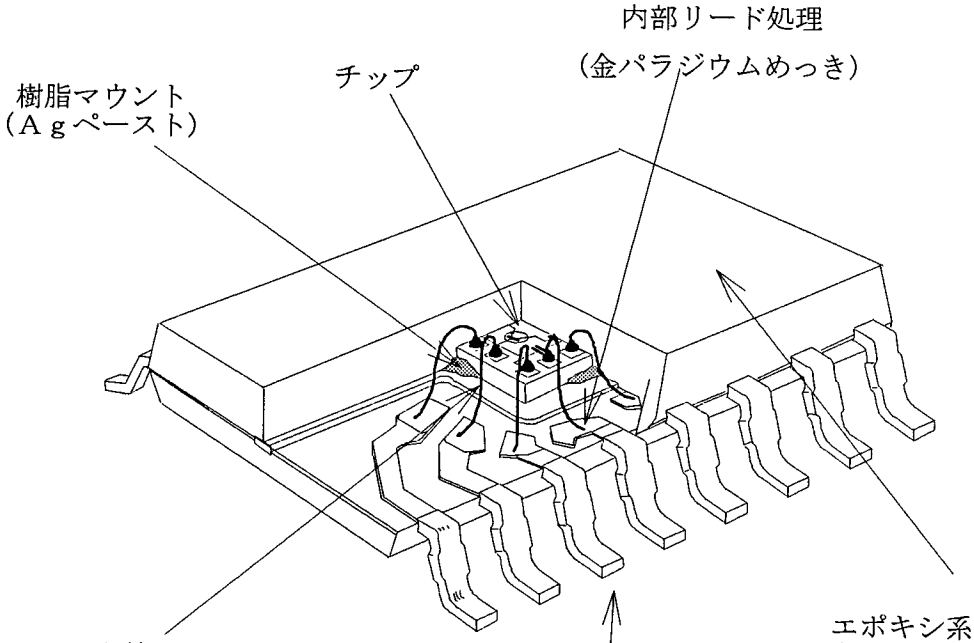


Weight : Ni:89% Pd:4% Au:7%

◆ パッケージの構造図

（ＴＳＳＯＰ）

《 代表例 》



重量比：Ni:89% Pd:4% Au:7%

PROPOSED STORAGE CONDITION / PROFILE

1. PROPOSED STORAGE CONDITION(Level-2)

① STORAGE AMBIENT (For both before/after opening the bag)
TEMPERRATURE : 5～ 30℃
HUMIDITY : 40～ 60%RH

② STORAGE LIMIT

- After opening the bag the device must be mounted on board within 1year.

*If exceed above limit, baking must be done before IC mounting as following condition.

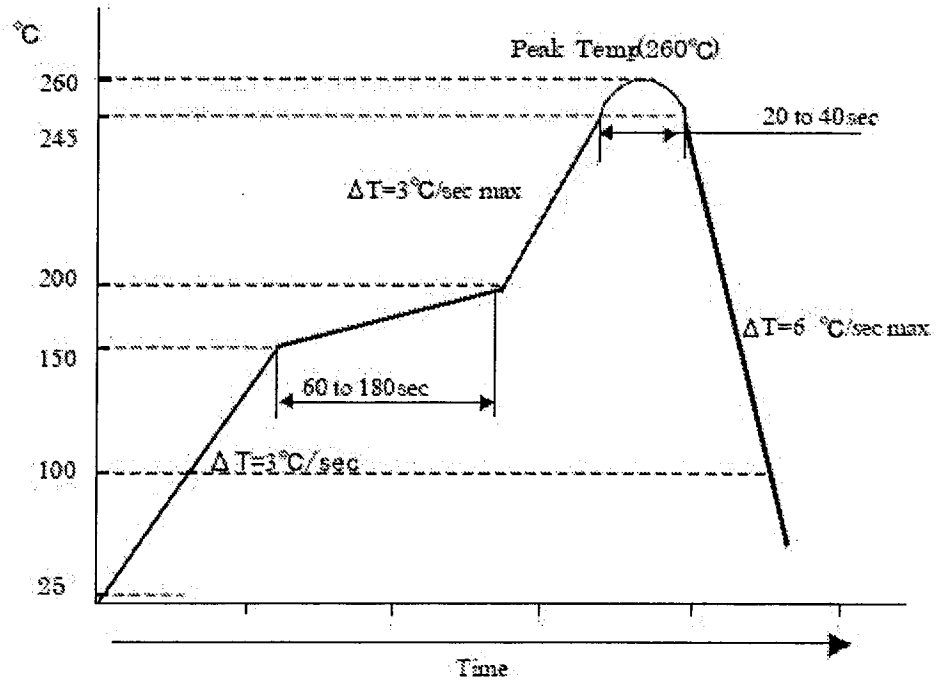
TEMPERATURE : 125deg.℃/Time : 24hours

* PRE MOUNT BAKING IS NOT REQUIRED

③ Heatproof temperature profile

Condition

REFLOW – PEAK TEMPERATURE :245℃ 20 to 40sec or LESS(MAX PEAK TEMP:260℃)



※ Based on TI's recommended profile above, 250℃/10sec & 230℃/60sec can be applicable.

*2TIMES REFLOW ACCEPTABLE

推 奨 保 管 条 件 ・ 耐熱リフロー条件

１．推奨保管条件(Level-2)

① 保管環境（梱包開封前後共）
温度 ： ５～ ３０℃
湿度 ：４０～ ６０％ＲＨ

② 保管期間

● 防湿梱包開封後
１年間以内に実装

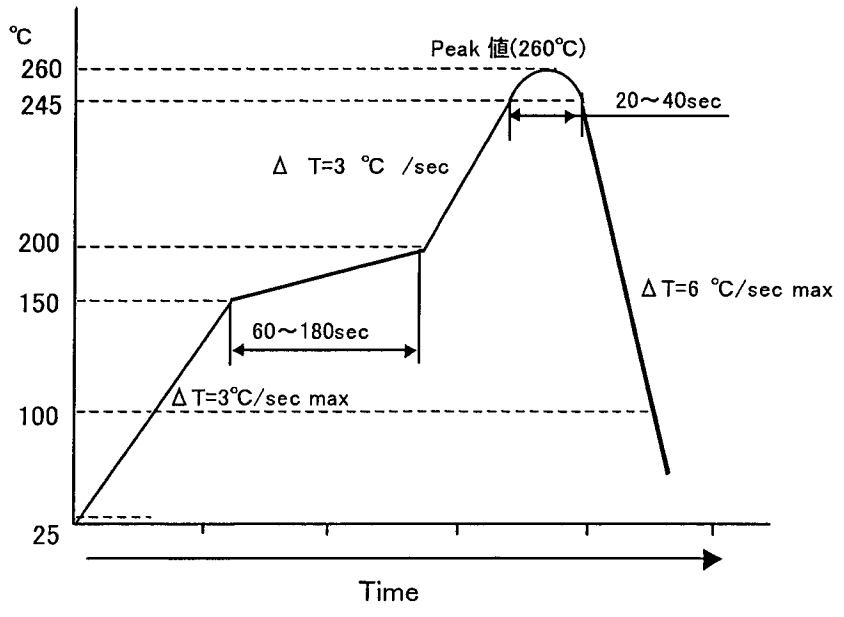
＊ 上記保管期間を越えた場合は、125℃ 24時間程度の乾燥処理を実施下さい。

●実装前のベーキングは必要ありません。

２．耐熱リフロー温度プロファイル

耐熱リフロー条件

リフローはんだ ﾋﾟｰｸ温度 245℃20～40 秒(最大ﾋﾟｰｸ温度 260℃ 5 秒)



＊ ２回リフロー

※ 250℃10sec， 230℃60sec リフロー2回対応可能

日本テキサス・インスツルメンツ（株）
営業・技術本部 品質保証部

《 Clarning condition 》

The flux used when soldering recommends rosin flux. Halogen flux is residual the halogen in packaging outer, affects the reliability of the product negatively, and avoid using, please. Because the lead corrosion etc. occur if flux remains, rosin flux should be washed, and be removed enough. Please note that the mark might disappear when the solvent used for washing is put on the package for a long time. Moreover, please do not rub the stamping side as much as possible of medicine's not drying. Lotus solvent and Daifron solvent are excellent in dissolubility and dissolution and the toxicity of another parts. Moreover, the midair product might receive fatal destruction to the wire bonding part etc. by the ultrasonic cleansing when the vibration happens and avoid the ultrasonic cleansing, please.

The following condition can be recommended at a plastic package.

＊frequencies 28KHz～29KHz (The device must not resonate)

＊Output supersonic wave 15W/liter

＊Neither device nor the printed wiring board must touch the vibration source directly.

＊30 seconds or less

TEXAS INSTRUMENTS

ENGINEERING REPORT ON THE MOLD COMPOUND PACKAGE CLEANING

EVALUATION RESULTS

Cleaning Solvents: "PINE ALPHA (ST100S)" of Arakawa Chemical Industries, LTD.
"CLEAN-THROUGH (750H)" of KAO Corporation.

Cleaning Procedures:
1) Place a soldered PCB in a Teflon container and fully submerge to be cleaned in 60ml/60℃ cleaning solvent for 2 hours.
2) Remove the item and soaked in 60℃ warm pure water.
3) Place the item in the ultrasonic cleaner and activate for 5 minutes.
4) Rinse twice with water and allow part to dry.

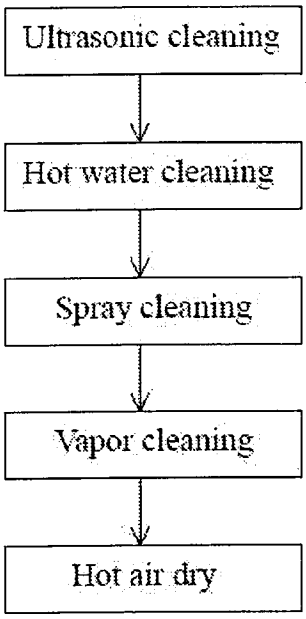
Note: Use an undiluted cleaning solvent.

Evaluation Items:
1) Inspection
Observe the degree of change on the surface by microscope (100X).
2) The package weight change

Evaluation Results:

Cleaning Solvent	Package material	Surface change	Weight change (%)
(Current Mode)	A B C	None	-
PINE ALPHA (ST100S)	A B C	None	0.01> 0.01> 0.01>
CLEAN-THROUGH (750H)	A B C	None	0.01> 0.01> 0.01>

GENERAL CLEANING FLOW



Note: In operation of the Ultrasonic cleaning, DO NOT cause any excess of the applicable frequency, power and time to avoid any destruction by the device agitation.

This is a general cleaning flow to be used but it is appropriate to apply recommendations from the cleaner makers as the cleaning conditions basically determines a type of cleaning solvents.

《洗浄条件》

半田付け時に使用するフラックスは、ロジン系フラックスを推奨します。
ハロゲン系フラックスはハロゲンがパッケージ外周に残留しやすく、製品の信頼性に悪影響を与えますので使用は避けて下さい。ロジン系フラックスでもフラックスが残っていますとリード腐食などが発生しますので十分に洗浄し、除去する必要があります。
なお、洗浄に使用する溶剤を長時間パッケージに付着させておきますとマークが消えることがありますのでご注意下さい。また、容剤が乾燥しないうちはできるだけ捺印面は擦らないようにして下さい。
ロータスソルベント・ダイフロンソルベント等が、溶解性・他部品の溶解・毒性からみても良好であります。
また、超音波洗浄につきましては、ＣＡＮタイプ、ハーメチックタイプ、サイドブレーズドタイプの場合パッケージ内部が中空になっておりますので、共振が起こりますとワイヤーボンディング部分などに致命的な破壊を受けることがありますので、超音波洗浄は避けて下さい。
プラスチックパッケージの場合は次の条件が推奨できます。

○周波数 ２８ＫＨｚ～２９ＫＨｚ （デバイスが共振しないこと）
○超音波出力 １５Ｗ／リットル
○振動源にデバイス、プリント基板が直接タッチしないこと
○時間 ３０秒以下

洗浄剤による封止材への影響調査 及び 洗浄フローについて

・洗 浄 剤　：パインアルファ(ST100S)　荒川化学
　　クリーンスルー(750H)　花王

・洗浄方法　：成形品をテフロン容器に入れ、洗浄剤を６０ｍｌ注ぎ、６０℃の湯浴中で２Ｈ浸透させる。
　　その後形成品を取り出し６０℃の純水に入れ、超音波洗浄器の中で５分間、２回すすぎ洗浄を行う。（洗浄剤は原液をそのまま使用する）

・測定項目　：
（１）外観
　　洗浄前と後のパッケージの外観を顕微鏡（100倍）で観察し、その変化を調べる。
（２）重量変化
　　洗浄前と後のパッケージの重量変化を測定。

・評価結果

洗　浄　剤	封　止　材　料	外観異常	重量変化 (%)
(初期値)	A B C	無	—
ﾊﾟｲﾝα　ST100S	A B C	無	０．０１＞ ０．０１＞ ０．０１＞
ｸﾘｰﾝｽﾙｰ750H	A B C	無	０．０１＞ ０．０１＞ ０．０１＞

基本的には、洗浄剤の種類によって洗浄条件は決まりますので、その洗浄剤メーカーの推奨条件に準じるのが妥当と思われます。
尚、一般的な洗浄方法としては、超音波洗浄、浸漬洗浄、スプレー洗浄、蒸気洗浄等が有ります。
通常はそれらを組み合わせて使われますので、以下にその一般的フローを提示致します。

一般的な洗浄フロー

超音波洗浄 → 温液洗浄 → スプレー洗浄 → 蒸気洗浄 → 乾燥

＊）超音波洗浄に関しましては、デバイスの破壊を防止する上で印加周波数、電力、時間及びデバイスが共振しないよう御注意下さい。

『This product is compliant with Pioneer group standard.GGP-001』

『本品はパイオニアグループ規定ＧＧＰ－００１に準拠しております』

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検定部品情報

課長	照査	担当
黒沢	中山	小峯

メーカー名	日本テキサス・インスツルメンツ

部品名	IC	パイオニア部品番号	ADS7828E
処理方法	(新規) 差し替え　追加	メーカー部品番号	ADS7828EIPWRQ1

納入仕様書の流れ

部品技術部 電気部品課 (1/28) → 技管経由 → 市販設計部　設計１０課　鈴木　洋輔　様 (2/2) 内容を確認の上、照査願います

- 変更あり → 部品技術部 → 技術管理課 配布
- 変更なし → 技術管理課 配布

２部もしくは３部

＊部品技術部ファイル済みの場合は２部

コメント

信頼性試験

検定試験	要　・　(不要)	
不要の場合理由にチェック	■同一構造類似部品にて検定済 ■同一生産工場部品にて検定済 □他部品にて代用 （部番：　　）	□記載事項の追加による差し替え □記載事項の変更による差し替え □その他 （　　）
試験の実施	パイオニア社内　・　部品製作メーカー　・　その他（　　）	
試験結果 合格 / 不合格	理由及び改善経過等を記入	

環境負荷物質の確認

①　環境負荷物質報告書	■　ＧＧＰ－００１に準じている
②　ＥＤＸによる分析	■　分析の結果、ＧＧＰ－００１に準じている □　他の類似部品で確認済み（部品番号:　　）

部品耐熱性ランク及び端子メッキの確認

部品耐熱性ランク	(A) B C D E F Z	端子メッキ無鉛	(対応) 未対応 ・ 非該当
端子メッキ組成	Ni－Pd－Au(89:4:7)		

（技術管理課にて、仕様書とあわせて管理願います）