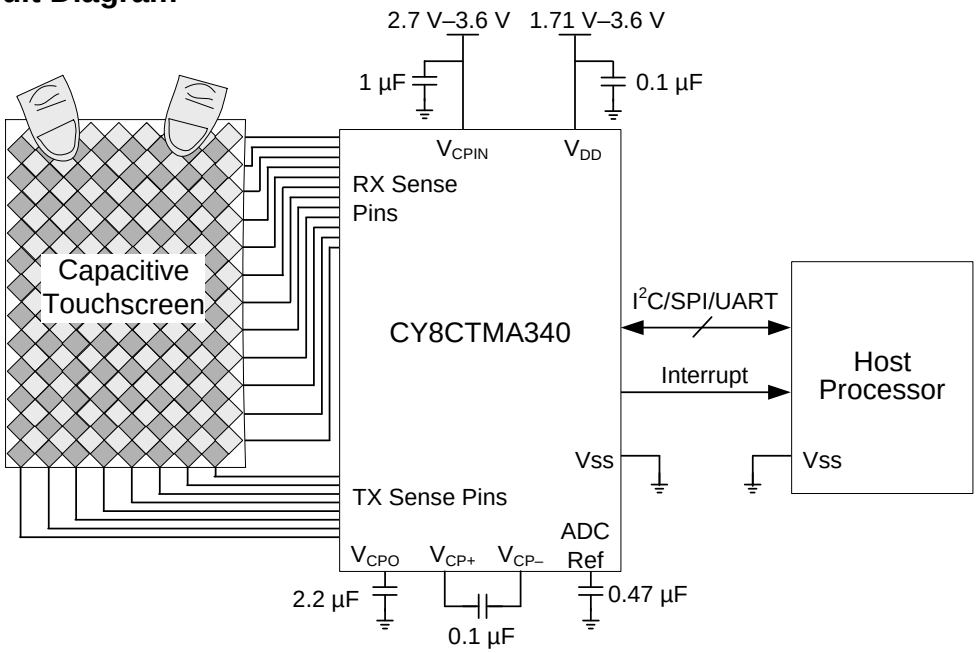
CY8CTMA340

TrueTouch™ Multi-Touch All-Points Touchscreen Controller

Features

- TrueTouch™ capacitive touchscreen controller
  - Single chip, up to four touches with independent finger position tracking
  - Up to 32 sense pins. Senses up to 256 intersections
  - Screen sizes up to 4.5 inches diagonal
  - Typical noise free resolution 0.1 mm
  - Core accuracy less than 0.7 mm
  - Typical scan time 2.9 ms (345 Hz)
  - Dual-rail power
    - 1.71-V to 3.6-V digital supply voltage
    - 2.7-V to 3.6-V analog supply voltage
  - Integrated voltage regulators
    - No need for dedicated voltage regulators
  - Robust sensing
    - Water on screen does not cause false touches
    - Immune to many types of liquid crystal display (LCD) noise
    - Robust operation in noisy radio frequency (RF) environments
  - Flexible pinout – each sense pin is configurable as receiver or transmitter
  - Buttons and slider sensing supported
  - Configurable to work with plastic film and glass touch sensors
  - Works with a variety of touchscreen sensors and stackups
  - Face detection – can discriminate a face (or a large surface in contact with the touchscreen) from fingers
  - Self calibrating touch sensing in response to environmental changes
  - In-system programming for easy field firmware upgrades
- Multiple communication protocols
  - I^2C slave
    - Selectable 100-kHz, 400-kHz, or 1-MHz operation
    - Hardware address detection for wakeup from sleep mode
  - SPI up to 2 MHz
  - UART up to 1 MHz (for debug only)
  - Supports secondary communication interface for easy debugging
- Package options
  - 36-pin 5 × 5 × 0.6 mm QFN
  - 48-pin 6 × 6 × 0.6 mm QFN
  - 49-ball 3.2 × 3.2 × 0.55 mm CSP

Operating Circuit Diagram



Contents

TrueTouch CY8CTMA340 Overview

The TrueTouch CY8CTMA340 is a capacitive touchscreen controller with the sensing technology to resolve touch locations of multiple fingers on the touchscreen. It converts an array of intersecting sensors into digital values. This array of digital information is processed by touch detection and position resolution algorithms in the touchscreen controller to determine the location of each finger on the touchscreen.

The CY8CTMA340 is available in 36-pin QFN, 48-pin QFN, and 49-ball CSP packages. The 36-pin QFN provides up to 24 sense pins, while the 48-pin QFN and 49-ball CSP provide up to 32 sense pins. A sense pin is a pin that can connect to a capacitive sensing channel within the chip. Each sense pin is programmable as a TX or RX within the particular channel to which the sense pin belongs. A pin configured as a TX transmits charge by driving a voltage waveform on one side of a capacitor, while a pin configured for RX receives charge on the other side of the capacitor. There are eight channels available for sensing eight intersections in parallel. A channel can transmit on one pin while receiving on another pin at the same time.

For the 36-pin QFN, each channel can be multiplexed to three sense pins ($3 \times 8 = 24$ sense pins). For the 48-pin QFN and 49-ball CSP, each channel can be multiplexed to four sense pins ($4 \times 8 = 32$ sense pins). PSoC Designer™, a development suite, provides a pin configuration tool to help set the pins properly.

The RX section of a channel receives a charge through a capacitor placed between TX and RX sensors. The charge is accumulated (or summed) on an internal integration capacitor. This is called analog integration. The charge is accumulated on the integration capacitor for a programmable period of time and then sampled by an analog-to-digital converter (ADC). The output of the ADC is accumulated (or summed) as a digital integration. The end of digital integration completes a conversion. The RX sections from all eight channels share a single ADC. A hardware sequencer is included to automatically control the operation of each channel's internal sequencing, as well as the sequencing of the channels to the ADC.

After a conversion is complete, the CPU processes the digital data using on-chip algorithms provided in the TrueTouch TMA340 controller. If the algorithms detect a finger, on-chip position resolution algorithms interpolate finger position between sensors. The touchscreen resolution is firmware programmable and is set to match the number of LCD pixels. For example, if the display is a QVGA with 320 × 240 pixels, the touchscreen controller is also set to 320 × 240 pixels.

Introduction to Capacitive Touchscreens

A capacitive touchscreen detects changes in measured capacitance to determine the location of one or more fingers on the surface of the touchscreen. The capacitive touchscreen consists of a capacitive touchscreen sensor, a touchscreen controller, and a flexible printed circuit (FPC) that connects them together. The touchscreen sensor is positioned between the LCD and a protective cover lens that the user touches. The touchscreen sensor is normally connected to the Cypress TrueTouch touchscreen controller through an FPC that is bonded to the sensor using a conductive adhesive. The FPC is connected to the main application host processor through a connector on the host printed circuit board (PCB). The Cypress TrueTouch controller can either be affixed to this FPC, or directly on the host PCB. Users can interact with the user interface displayed on the LCD through finger movements and gestures on the surface of the protective cover lens.

A capacitive touchscreen sensor usually uses a multilayer plastic film/glass construction or a single-layer glass construction. The capacitive sensor is typically created with a transparent conductive material called indium tin oxide (ITO). ITO sensors are formed on the plastic film or glass substrates in a grid of rows and columns. A thin isolation layer separates the row sensors from the column sensors. The ITO sensors are typically several hundred angstroms thick and must be handled with care to prevent damage. Experienced sensor suppliers can control the deposition to achieve thin, transparent sensors, while optimizing sensing performance. Metal traces run along the border of the sensor grid to connect the conductive ITO sensors to the FPC and touchscreen controller. Because the metal traces are not transparent, the cover lens requires an opaque border outlining the active area of the touchscreen.

Power Supply

Signal-to-noise ratio (SNR) is a significant contributing factor to touchscreen performance. Increasing the transmitter voltage increases the signal. The CY8CTMA340 contains an integrated charge pump that steps up the voltage at V_{CPIN} to 4.8 V (see Figure 1 on page 4). The 4.8-V charge pump output, V_{CPO}, supplies the sensing circuits. V_{CORE} is an internal supply to the digital core of the chip, including the CPU. V_{CORE} is connected to the output of a 1.8-V internal low dropout regulator (LDO) that is powered by V_{DD}. When V_{DD} is less than or equal to 1.8 V, this LDO is automatically bypassed. You can program the device to derive GPIO input logic levels from V_{DD} or V_{CORE}. Deriving GPIO logic levels from V_{CORE} allows I^2C communication with a host that is 1.8 V while V_{DD} is connected to a supply higher than 1.8 V.

Figure 1. Power Supply Connection

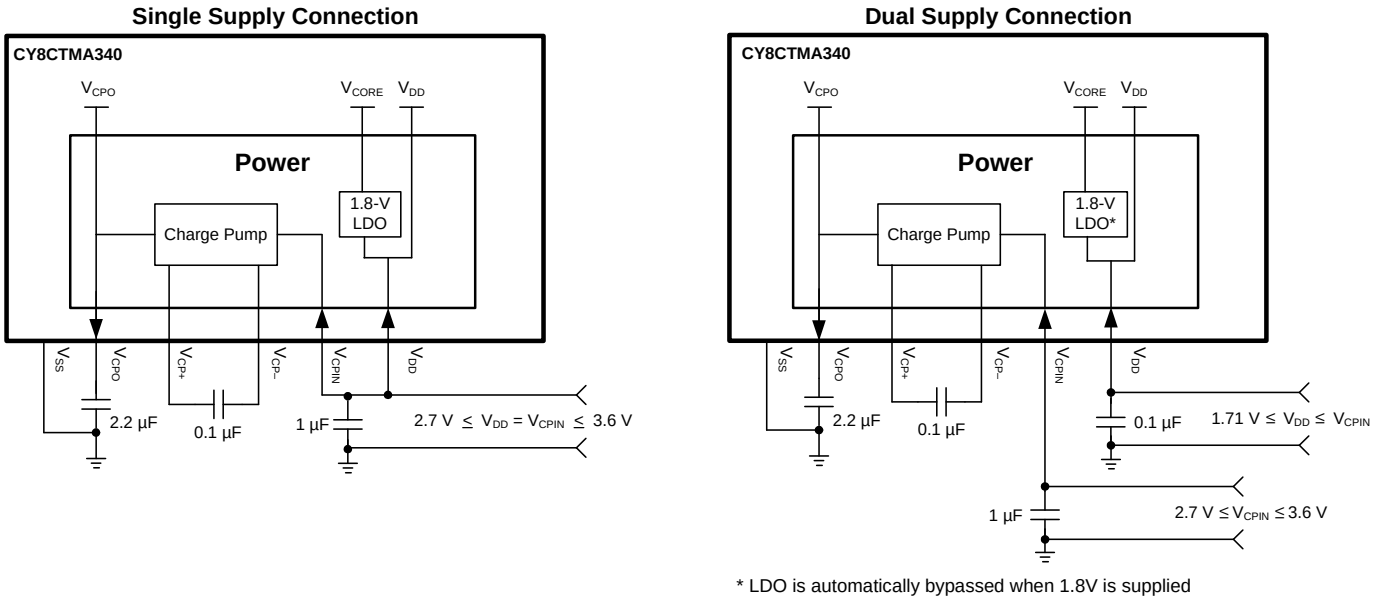


Table 1. Typical Average Currents and Power

Conditions	$T_{REFRESH}$ [ms]	I_{DDAVG} [mA]	$I_{CPINAVG}$ [mA]	Average Total Power P_{AVG} [mW]
V_{DD} = 1.8, V_{CPIN} = 2.7	8	3.8	3.6	17
V_{DD} = 1.8, V_{CPIN} = 2.7	16	1.9	1.8	8.3
V_{DD} = 1.8, V_{CPIN} = 2.7	100	0.30	0.29	1.3

Note Lowest average power is achieved by sleeping after scanning and processing is complete. The scan time, T_{SCAN} is the time it takes to convert all intersection capacitances on the touchscreen to digital values. The process time, $T_{PROCESS}$, is the time it takes the CPU to process the digital values and resolve the finger position. The sleep time, T_{SLEEP}, is the time, after the scanning and processing, that the device is asleep. The refresh rate is the periodic time when fresh data is available to read from the device. $T_{REFRESH} = T_{SCAN} + T_{PROCESS} + T_{SLEEP}$. For the fastest refresh time, $T_{SLEEP} = 0$. In Table 1, three refresh rates were selected for a 8 × 12 panel with a typical scan time of 2.9 ms and a process time of 1 ms for one finger touch. The 8- and 16-ms refresh rates are typical rates for the host to track a finger position in real time. The 100-ms refresh rate saves power by waiting for a finger touch to occur before changing to the faster 8- and 16-ms refresh rates. Average current and power numbers were calculated in the table by using I_{DD} and I_{CPIN} typical values from Table 7 on page 9 ($F_{IMO} = F_{CPU}$ = 24 MHz) and the following equations.

$$I_{DDAVG} = \frac{I_{DD} \times (T_{SCAN} + T_{PROCESS})}{T_{REFRESH}} \quad \textbf{Equation 1}$$

$$I_{CPINAVG} = \frac{I_{CPIN} \times T_{SCAN}}{T_{REFRESH}} \quad \textbf{Equation 2}$$

$$P_{AVG} = V_{DD} \times I_{DDAVG} + V_{CPIN} \times I_{CPINAVG} \quad \textbf{Equation 3}$$

Pin Information

The CY8CTMA340 is available in several packages. This section provides the pin names, descriptions, and mapping to the physical package.

Table 2. 36-Pin QFN (CY8CTMA340)

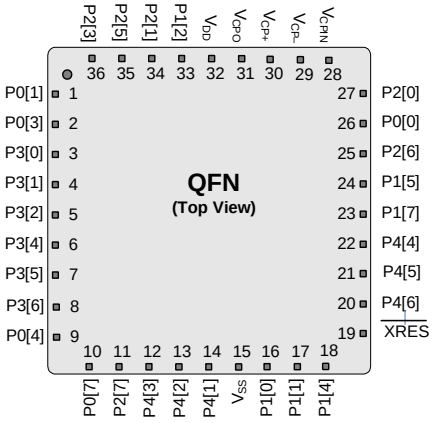
Pin No.	Type		Name	Description	CY8CTMA340
	Digital	Analog			
1	I/O	I/O	P0[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
2	I/O	I/O	P0[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
3	I/O	I/O	P3[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
4	I/O	I/O	P3[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
5	I/O	I/O	P3[2]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
6	I/O	I/O	P3[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
7	I/O	I/O	P3[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
8	I/O	I/O	P3[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
9	I/O	I/O	P0[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
10	I/O	I/O	P0[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
11	I/O	I/O	P2[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
12	I/O	I/O	P4[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
13	I/O	I/O	P4[2]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
14	I/O	I/O	P4[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
15	Power		V_{SS}	Connect to circuit ground	
16	I/O	I/O	P1[0]	GPIO / ISSP DATA / I^2C SDA	
17	I/O	I/O	P1[1]	GPIO / ISSP CLK / I^2C SCL	
18	I/O	I/O	P1[4]	ADC reference output. Bypass with 0.47 µF capacitor	
19	Input		$\overline{XRES}$	Active LOW external reset with internal pull-up	
20	I/O	I/O	P4[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
21	I/O	I/O	P4[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
22	I/O	I/O	P4[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
23	I/O	I/O	P1[7]	GPIO / I^2C SCL	
24	I/O	I/O	P1[5]	GPIO / I^2C SDA	
25	I/O	I/O	P2[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
26	I/O	I/O	P0[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
27	I/O	I/O	P2[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
28	Power		V_{CPIN}	Charge pump input. See Figure 1 on page 4 and Table 7 on page 9	
29	Power		V_{CP-}	Charge pump flying capacitor negative signal. See Figure 1 on page 4	
30	Power		V_{CP+}	Charge pump flying capacitor positive signal. See Figure 1 on page 4	
31	Power		V_{CPO}	Charge pump output. See Figure 1 on page 4 and Table 7 on page 9	
32	Power		V_{DD}	Digital supply voltage. See Figure 1 on page 4 and Table 7 on page 9	
33	I/O	I/O	P1[2]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
34	I/O	I/O	P2[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
35	I/O	I/O	P2[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
36	I/O	I/O	P2[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
EP	–	–	–	Exposed pad. Connect to circuit ground. See Figure 5 on page 15	

Table 3. 48-Pin QFN (CY8CTMA340)

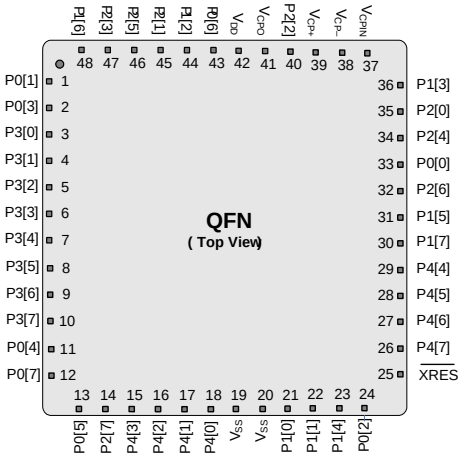
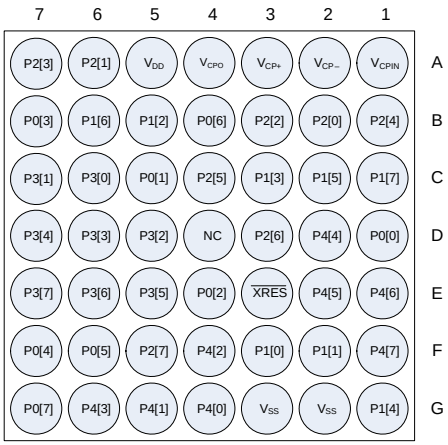
Pin No.	Type		Name	Description	CY8CTMA340
	Digital	Analog			
1	I/O	I/O	P0[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
2	I/O	I/O	P0[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
3	I/O	I/O	P3[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
4	I/O	I/O	P3[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
5	I/O	I/O	P3[2]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
6	I/O	I/O	P3[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
7	I/O	I/O	P3[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
8	I/O	I/O	P3[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
9	I/O	I/O	P3[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
10	I/O	I/O	P3[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
11	I/O	I/O	P0[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
12	I/O	I/O	P0[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
13	I/O	I/O	P0[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
14	I/O	I/O	P2[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
15	I/O	I/O	P4[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
16	I/O	I/O	P4[2]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
17	I/O	I/O	P4[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
18	I/O	I/O	P4[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
19	Power		V_{SS}	Connect to circuit ground	
20	Power		V_{SS}	Connect to circuit ground	
21	I/O	I/O	P1[0]	GPIO / ISSP DATA / I^2C SDA	
22	I/O	I/O	P1[1]	GPIO / ISSP CLK / I^2C SCL	
23	I/O	I/O	P1[4]	ADC reference output. Bypass with 0.47 µF capacitor	
24	I/O	I/O	P0[2]	GPIO	
25	Input		$\overline{XRES}$	Active LOW external reset with internal pull-up	
26	I/O	I/O	P4[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
27	I/O	I/O	P4[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
28	I/O	I/O	P4[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
29	I/O	I/O	P4[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
30	I/O	I/O	P1[7]	GPIO / I^2C SCL	
31	I/O	I/O	P1[5]	GPIO / I^2C SDA	
32	I/O	I/O	P2[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
33	I/O	I/O	P0[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
34	I/O	I/O	P2[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
35	I/O	I/O	P2[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
36	I/O	I/O	P1[3]	GPIO	
37	Power		V_{CPIN}	Charge pump input. See Figure 1 on page 4 and Table 7 on page 9	
38	Power		V_{CP-}	Charge pump flying capacitor negative signal. See Figure 1 on page 4	
39	Power		V_{CP+}	Charge pump flying capacitor positive signal. See Figure 1 on page 4	
40	I/O	I/O	P2[2]	GPIO	
41	Power		V_{CPO}	Charge pump output. See Figure 1 on page 4 and Table 7 on page 9	
42	Power		V_{DD}	Digital supply voltage. See Figure 1 on page 4 and Table 7 on page 9	
43	I/O	I/O	P0[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
44	I/O	I/O	P1[2]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
45	I/O	I/O	P2[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
46	I/O	I/O	P2[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
47	I/O	I/O	P2[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
48	I/O	I/O	P1[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
EP	–	–	–	Exposed pad. Connect to circuit ground. See Figure 6 on page 16	

Table 4. 49-Ball CSP (CY8CTMA340)

Pin No.	Type		Name	Description	CY8CTMA340
	Digital	Analog			
1A	Power		V_{CPIN}	Charge pump input. See Figure 1 on page 4 and Table 7 on page 9	
1B	I/O	I/O	P2[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
1C	I/O	I/O	P1[7]	GPIO / I^2C SCL	
1D	I/O	I/O	P0[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
1E	I/O	I/O	P4[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
1F	I/O	I/O	P4[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
1G	I/O	I/O	P1[4]	ADC reference output. Bypass with 0.47 µF capacitor	
2A	Power		V_{CP-}	Charge pump flying capacitor negative signal. See Figure 1 on page 4	
2B	I/O	I/O	P2[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
2C	I/O	I/O	P1[5]	GPIO / I^2C SDA	
2D	I/O	I/O	P4[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
2E	I/O	I/O	P4[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 5	
2F	I/O	I/O	P1[1]	GPIO / ISSP CLK / I^2C SCL	
2G	Power		V_{SS}	Connect to circuit ground	
3A	Power		V_{CP+}	Charge pump flying capacitor positive signal. See Figure 1 on page 4	
3B	I/O	I/O	P2[2]	GPIO	
3C	I/O	I/O	P1[3]	GPIO	
3D	I/O	I/O	P2[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 6	
3E	Input		$\overline{XRES}$	Active LOW external reset with internal pull-up	
3F	I/O	I/O	P1[0]	GPIO / ISSP DATA / I^2C SDA	
3G	Power		V_{SS}	Connect to circuit ground	
4A	Power		V_{CPO}	Charge pump output. See Figure 1 on page 4 and Table 7 on page 9	
4B	I/O	I/O	P0[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
4C	I/O	I/O	P2[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
4D		I/O	NC	No Connect	
4E	I/O	I/O	P0[2]	GPIO	
4F	I/O	I/O	P4[2]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
4G	I/O	I/O	P4[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
5A	Power		V_{DD}	Digital supply voltage. See Figure 1 on page 4 and Table 7 on page 9	
5B	I/O	I/O	P1[2]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
5C	I/O	I/O	P0[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
5D	I/O	I/O	P3[2]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
5E	I/O	I/O	P3[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
5F	I/O	I/O	P2[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
5G	I/O	I/O	P4[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
6A	I/O	I/O	P2[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 7	
6B	I/O	I/O	P1[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
6C	I/O	I/O	P3[0]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
6D	I/O	I/O	P3[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
6E	I/O	I/O	P3[6]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
6F	I/O	I/O	P0[5]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
6G	I/O	I/O	P4[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 4	
7A	I/O	I/O	P2[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
7B	I/O	I/O	P0[3]	GPIO / sense pin multiplexable to TX or RX sections of channel 0	
7C	I/O	I/O	P3[1]	GPIO / sense pin multiplexable to TX or RX sections of channel 1	
7D	I/O	I/O	P3[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
7E	I/O	I/O	P3[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 2	
7F	I/O	I/O	P0[4]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	
7G	I/O	I/O	P0[7]	GPIO / sense pin multiplexable to TX or RX sections of channel 3	



Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CTMA340 TrueTouch devices.

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature		–55	+25	+125[1]	°C
V_{SUP}	Power pin voltage	V_{DD}, V_{CPIN}, V_{CP+}, $V_{CP–}$, V_{CPO}	–0.5	–	+6.0	V
V_{IO}	I/O pin voltage	P0[2], P1[0], P1[1], P1[5], P1[7], P1[3], and P2[2]	V_{SS} – 0.5	–	V_{DD} + 0.5	V
		All sense pins	V_{SS} – 0.5	–	V_{CPO}	
I_{IO}	Current into I/O pin		–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	–	–	V
		Charged device model	500	–	–	

Operating Temperature

Table 6. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature		–40	–	+85	°C
T_J	Operational die temperature	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 17.	–40	–	+90	°C

Note
1. Storing programmed devices at or above 85 °C may reduce flash retention time below $Flash_{DR}$ (min) in Table 10 on page 11.

DC Chip Level Specifications

Table 7 lists guaranteed maximum and minimum specifications for –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at T_A = 25 °C. $V_{DD} \leq V_{CPIN}$.

By default, the device is set up with 24-MHz IMO and CPU clock frequency. This is optimal for fastest code execution and sensing circuit speed. Lower clock frequency reduces power at the expense of slower code execution and sensing circuit speed.

The IMO has 6-, 12-, or 24-MHz clock frequency options. Set the frequency by programming the CPU_SCR1 register. The CPU can run directly from the IMO or a fraction of the IMO by setting the OSC_CR0 register.

Table 7. DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Digital supply voltage input	Charge pump enabled	1.71	–	3.60	V
V_{CPIN}	Charge pump input range	Charge pump enabled	2.70	–	3.60	V
V_{CPO}	Charge pump output range	Charge pump enabled	–	4.8	–	V
I_{DD}	V_{DD} supply current	$F_{IMO} = F_{CPU}$ = 24 MHz	–	7.7	9.63	mA
		$F_{IMO} = F_{CPU}$ = 12 MHz	–	4.8	6.00	
		$F_{IMO} = F_{CPU}$ = 6 MHz	–	2.9	3.63	
I_{CPIN}	V_{CPIN} supply current	V_{CPIN} = 2.7 V $F_{IMO} = F_{CPU}$ = 24 MHz Charge pump clock = 12 MHz	–	10	13.0	mA
		V_{CPIN} = 3.3 V $F_{IMO} = F_{CPU}$ = 24 MHz Charge pump clock = 12 MHz	–	9.4	11.8	
		V_{CPIN} = 3.6 V $F_{IMO} = F_{CPU}$ = 24 MHz Charge pump clock = 12 MHz	–	9.3	11.6	
I_{SB0}	Standby current with POR, LVD, sleep timer and ILO active	$V_{CPIN} = V_{DD}$ = 2.7 V Charge pump disabled	–	1	4	µA
		$V_{CPIN} = V_{DD}$ = 3.3 V Charge pump disabled	–	1	4	
I_{SB1}[2]	Deep sleep current (sleep timer and ILO disabled)	$V_{CPIN} = V_{DD}$ = 2.7 V Charge pump disabled All sense pins driven strong low	–	0.2	4	µA
		$V_{CPIN} = V_{DD}$ = 3.3 V Charge pump disabled All sense pins driven strong low	–	0.2	4	

Note
2. Must disable all interrupt sources before entering deep sleep. Use only $\overline{\text{XRES}}$ to wake the device from deep sleep.

DC General Purpose I/O Specifications

Table 8 lists guaranteed maximum and minimum specifications for 1.71 V ≤ V_{DD} ≤ 3.6 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at V_{DD} = 3.3 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and T_A = 25 °C.

Table 8. DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Internal pull-up resistance	Pin configured for internal pull-up	4.0	5.6	8.0	kΩ
V_{OH}	High output voltage	I_{OH} = 10 µA	V_{DD} – 0.2	–	–	V
		I_{OH} = 0.5 mA	V_{DD} – 0.6	–	–	
V_{OL}	Low output voltage	I_{OL} = –4 mA, 1.71 V ≤ V_{DD} ≤ 3.0 V	–	–	0.40	V
		I_{OL} = –20 mA, 3.0 V ≤ V_{DD} ≤ 3.6 V	–	–	1.0	
V_{IL}[3]	Input low voltage	Input buffer referenced to V_{DD}	–	–	0.3 × V_{DD}	V
		Input buffer referenced to V_{CORE}	–	–	0.45	
		Sleep modes referenced to V_{CORE}	–	–	0.24	
V_{IH}[3]	Input high voltage	Input buffer referenced to V_{DD}	0.7 × V_{DD}	–	–	V
		Input buffer referenced to V_{CORE}	1.26	–	–	
		Sleep modes referenced to V_{CORE}	1.18	–	–	
V_H	Input hysteresis voltage		–	50	–	mV
I_{IL}	Input leakage (absolute value)	Gang tested with all I/Os to 1 µA	–	1	25	nA
C_{IN}	Input pin capacitance	Package and pin dependent T_A = 25 °C	–	5	7.5	pF
C_{OUT}	Output pin capacitance	Package and pin dependent T_A = 25 °C	–	5	7.5	pF

DC POR and LVD Specifications

Table 9 lists guaranteed maximum and minimum specifications for 1.71 V ≤ V_{DD} ≤ 3.6 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at V_{DD} = 3.3 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and T_A = 25 °C.

The device resets when V_{DD} falls below the programmed POR threshold.

Table 9. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POR}	1.66 V selected in PSoC Designer	Valid only after the registers are initialized at startup	–	1.66	1.71	V
	2.36 V selected in PSoC Designer		–	2.36	2.42	
	2.60 V selected in PSoC Designer		–	2.60	2.67	
	2.82 V selected in PSoC Designer		–	2.82	2.89	
V_{LVD}	2.45 V selected in PSoC Designer	Valid only after the registers are initialized at startup	2.39	2.45	2.51	V
	2.71 V selected in PSoC Designer		2.64	2.71	2.78	
	2.92 V selected in PSoC Designer		2.85	2.92	2.99	
	3.02 V selected in PSoC Designer		2.95	3.02	3.10	
	3.13V selected in PSoC Designer		3.05	3.13	3.21	
	1.90 V selected in PSoC Designer		1.85	1.90	1.95	
	1.80 V selected in PSoC Designer		1.75	1.80	1.85	

Note
3. Input logic levels are referable to V_{DD} or V_{CORE}.

DC Programming Specifications

Table 10 lists guaranteed maximum and minimum specifications for 1.71 V ≤ V_{DD} ≤ 3.6 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at V_{DD} = 3.3 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and T_A = 25 °C.

See Cypress Application Notes AN2026D and AN59388 for details on Cypress's programming protocol.

Table 10. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DDIWRITE}$	Supply voltage for flash write operations		1.71	–	–	V
I_{DDP}	Supply current during programming or verify		–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See DC General Purpose I/O Specifications on page 10 V_{DD} = 1.8 V	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See DC General Purpose I/O Specifications on page 10 V_{DD} = 1.8 V	V_{IH}	–	–	V
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.50	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	0.80	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC General Purpose I/O Specifications on page 10	V_{OH}	–	V_{DD}	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	10,000	–	–	Cycles
$Flash_{DR}$	Flash data retention		20[4]	–	–	Years

Capacitive Touchscreen Specifications

Table 11 lists guaranteed maximum and minimum specifications for 1.71 V ≤ V_{DD} ≤ 3.6 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at V_{DD} = 3.3 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and T_A = 25 °C.

Table 11. Capacitive Touchscreen Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
C_N	Input referred capacitive noise		–	4.2	–	fF-RMS
C_T	Change in measured capacitance per change in ambient temperature		–	1.1	13	fF/°C
C_V	Change in measured capacitance per change in V_{CPIN}		–	39	–	fF/V
V_{TXOL}	TX output low voltage	No load	–	V_{SS}	–	V
V_{TXOH}	TX output high voltage	No load	–	V_{CPO}	–	V
I_{TXDR}	TX drive current output (sink or source)	Low	55	90	130	µA
		Medium-low	110	180	260	
		Medium-high	165	270	390	
		High	220	360	520	

Note
4. Storing programmed devices at or above 85 °C may reduce flash retention time below $Flash_{DR}$ (min).

AC Chip Level Specifications

Table 12 lists guaranteed maximum and minimum specifications for 1.71 V ≤ V_{DD} ≤ 3.6 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at V_{DD} = 3.3 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and T_A = 25 °C.

Table 12. AC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{32K1}	Internal low-speed oscillator frequency		19.2	32	50.0	kHz
F_{IMO}	Internal main oscillator frequency	Configured at 24 MHz	23.5	24	24.5	MHz
		Configured at 12 MHz	11.7	12	12.3	
		Configured at 6 MHz	5.88	6.0	6.12	
T_{XRST}	External reset pulse width at power up	After supply voltage is valid	1	–	–	ms
T_{XRST2}	External reset pulse width after power up	After startup	10	–	–	µs

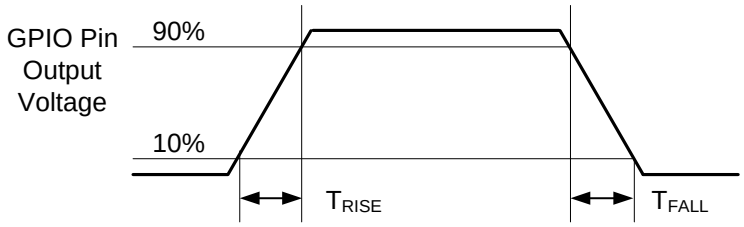
AC GPIO Output Specifications

Table 13 lists guaranteed maximum and minimum specifications for 1.71 V ≤ V_{DD} ≤ 3.6 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at V_{DD} = 3.3 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and T_A = 25 °C.

Table 13. AC GPIO Output Specifications

Symbol	Description	Conditions		Min	Typ	Max	Units
F_{GOUT}	GPIO output operating frequency	C_{LOAD} = 25 pF		0	–	5.0	MHz
F_{GIN}	GPIO input operating frequency			0	–	24	MHz
T_{RISE}	Rise time	C_{LOAD} = 25 pF	V_{DD} > 2.5 V	10	–	60	ns
			V_{DD} < 2.5 V	10	–	80	
T_{FALL}	Fall time	C_{LOAD} = 25 pF	V_{DD} > 2.5 V	5	–	45	ns
			V_{DD} < 2.5 V	5	–	75	

Figure 2. GPIO Timing Diagram



AC Programming Specifications

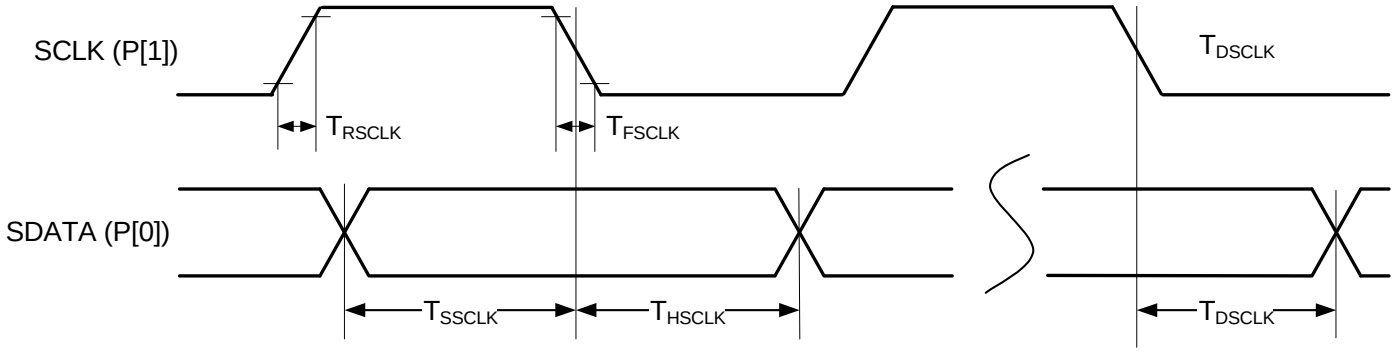
Table 14 lists guaranteed maximum and minimum specifications for 1.71 V ≤ V_{DD} ≤ 3.6 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at V_{DD} = 3.3 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and T_A = 25 °C.

See Cypress Application Notes AN2026D and AN59388 for details on Cypress's programming protocol.

Table 14. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise time of SCLK		1	–	20	ns
T_{FSCLK}	Fall time of SCLK		1	–	20	ns
T_{SSCLK}	Data setup time to falling edge of SCLK		40	–	–	ns
T_{HSCLK}	Data hold time from falling edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK	3.0 V ≤ V_{DD} ≤ 3.6 V	0	–	8	MHz
		1.71 V ≤ V_{DD} ≤ 3.0 V	0	–	5	
T_{ERASEB}	Flash erase time (block)		–	–	18	ms
T_{WRITE}	Flash block write time		–	–	25	ms
T_{DSCLK}	Data out delay from falling edge of SCLK	3.0 V ≤ V_{DD} ≤ 3.6 V (C_{LOAD} ≤ 30 pF)	–	–	75	ns
		1.71 V ≤ V_{DD} ≤ 3.0 V (C_{LOAD} ≤ 30 pF)	–	–	130	

Figure 3. AC Programming Timing Diagram



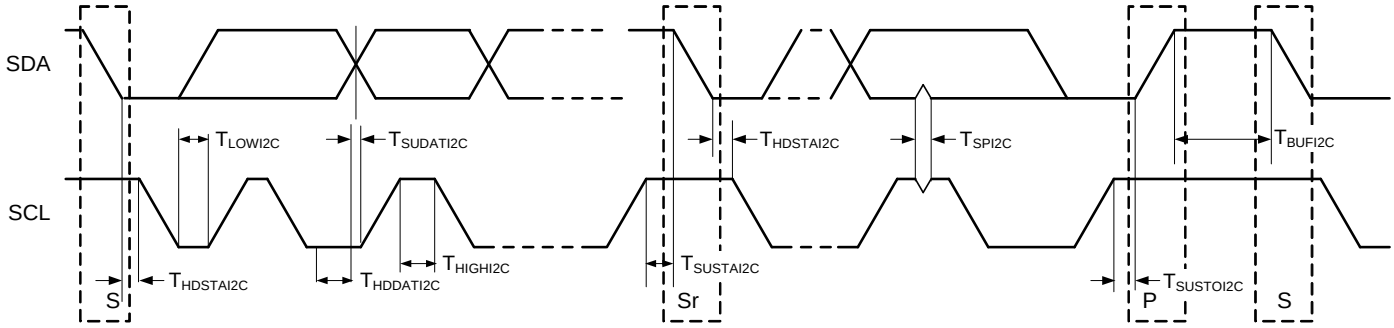
I²C Specifications

Table 15 lists guaranteed maximum and minimum specifications for 1.71 V ≤ V_{DD} ≤ 3.6 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at V_{DD} = 3.3 V, 2.7 V ≤ V_{CPIN} ≤ 3.6 V, and T_A = 25 °C.

Table 15. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Conditions	Standard-Mode		Fast-Mode		Fast-Mode Plus		Units
			Min	Max	Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency		0	100	0	400	0	1000	kHz
$T_{HDSTAI2C}$	Hold time (repeated) Start condition. After this period, the first clock pulse is generated.		4.0	–	0.60	–	0.26	–	µs
T_{LOWI2C}	LOW period of SCL clock		4.7	–	1.3	–	0.50	–	µs
$T_{HIGHI2C}$	HIGH period of SCL clock		4.0	–	0.60	–	0.26	–	µs
$T_{SUSTAI2C}$	Setup time for repeated Start condition		4.7	–	0.60	–	0.26	–	µs
$T_{HDDATI2C}$	Data hold time		0	–	0	–	0	–	µs
$T_{SUDATI2C}$	Data setup time		250	–	100	–	50	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition		4.0	–	0.60	–	0.26	–	µs
T_{BUFI2C}	Bus free time between a Stop and Start condition		4.7	–	1.3	–	0.50	–	µs
T_{SPI2C}[5]	Pulse width of spikes that are suppressed by input filter	I²C Specification 3.0 maximum is 50 ns	–	–	0	50	0	40[6]	ns
C_{BUS}	Capacitance load for SDA or SCL		–	200[7]	–	200[7]	–	150[7]	pF

Figure 4. Timing Diagram for Fast/Standard Mode of the I²C Bus



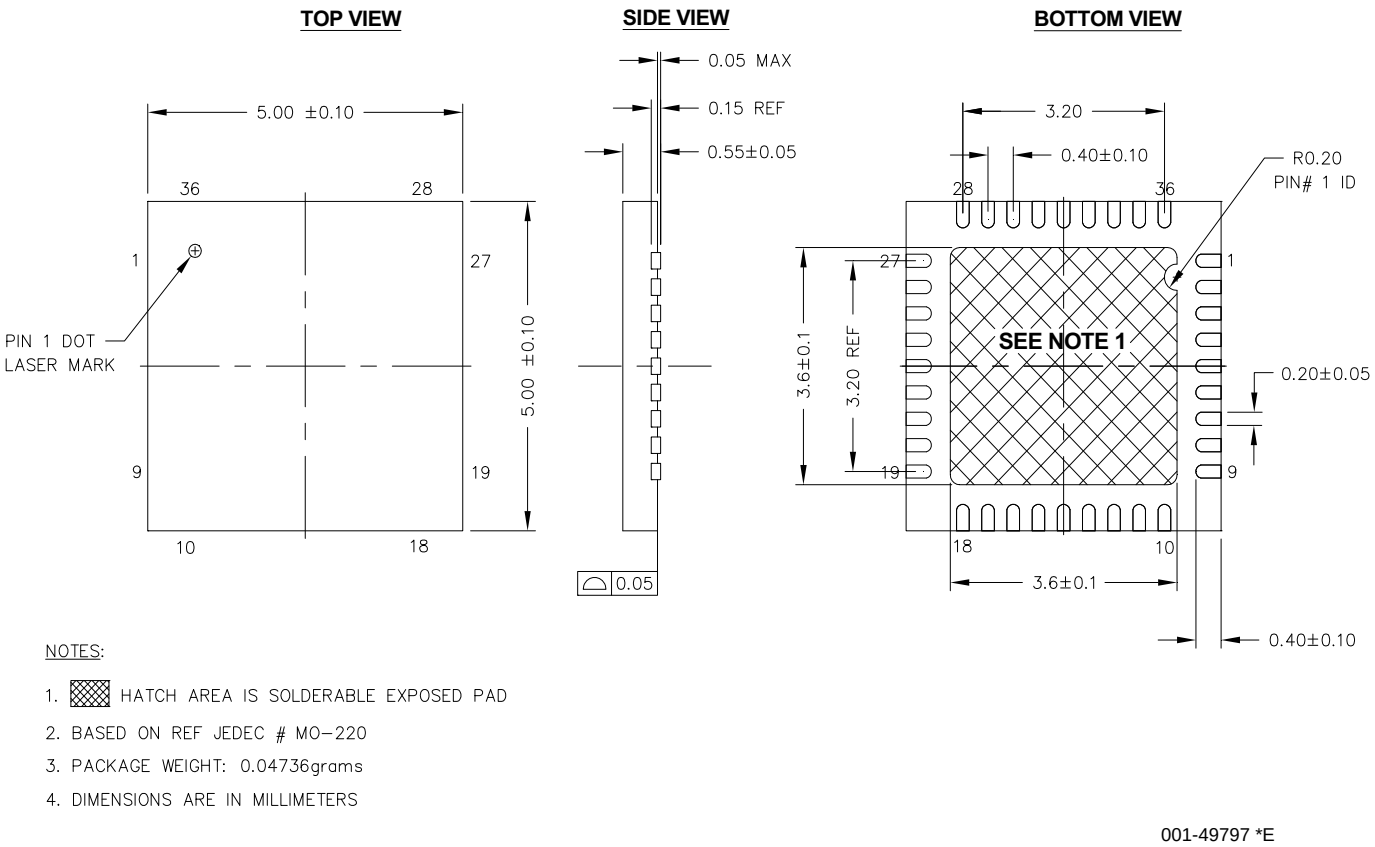
LEGEND
S I²C Start Condition
Sr I²C Repeat Start Condition
P I²C Stop Condition

Notes
5. In I²C sleep mode, the device can wake up from sleep when the address matches its own slave address. When this happens, there is no glitch/spike filtering on SCL and SDA lines on the 7-bit address + R/W bit. After the device wakes up, there is glitch/spike filtering on SCL and SDA lines.
6. This does not fully meet the I²C requirement of 50 ns.
7. This does not fully meet the I²C max capacitive load targets of ≥ 400 pF.

Packaging Information

This section illustrates the packaging specifications for the CY8CTMA340 devices.

Figure 5. 36-Pin (5 × 5 × 0.6 mm) QFN

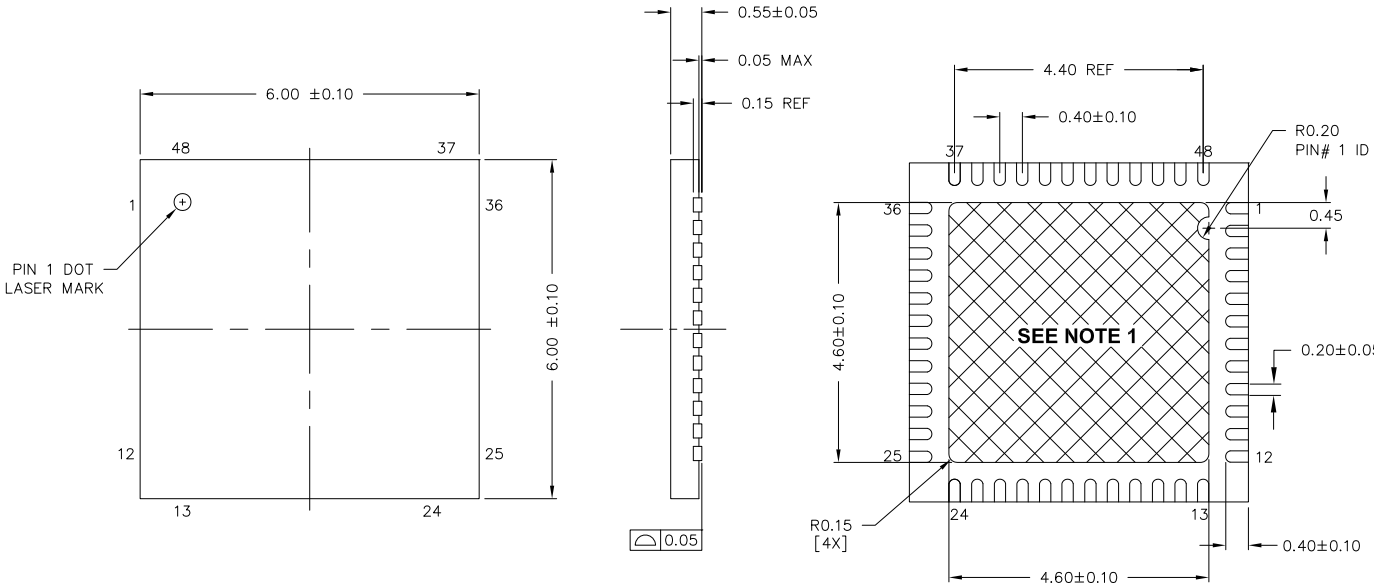


001-49797 *E

Important Note

■ For information on the preferred dimensions for mounting QFN packages, see the application note at Application Notes for Surface Mount Assembly of Amkor's *Micro*LeadFrame® (MLF®) Packages

Figure 6. 48-Pin (6 × 6 × 0.6 mm) QFN



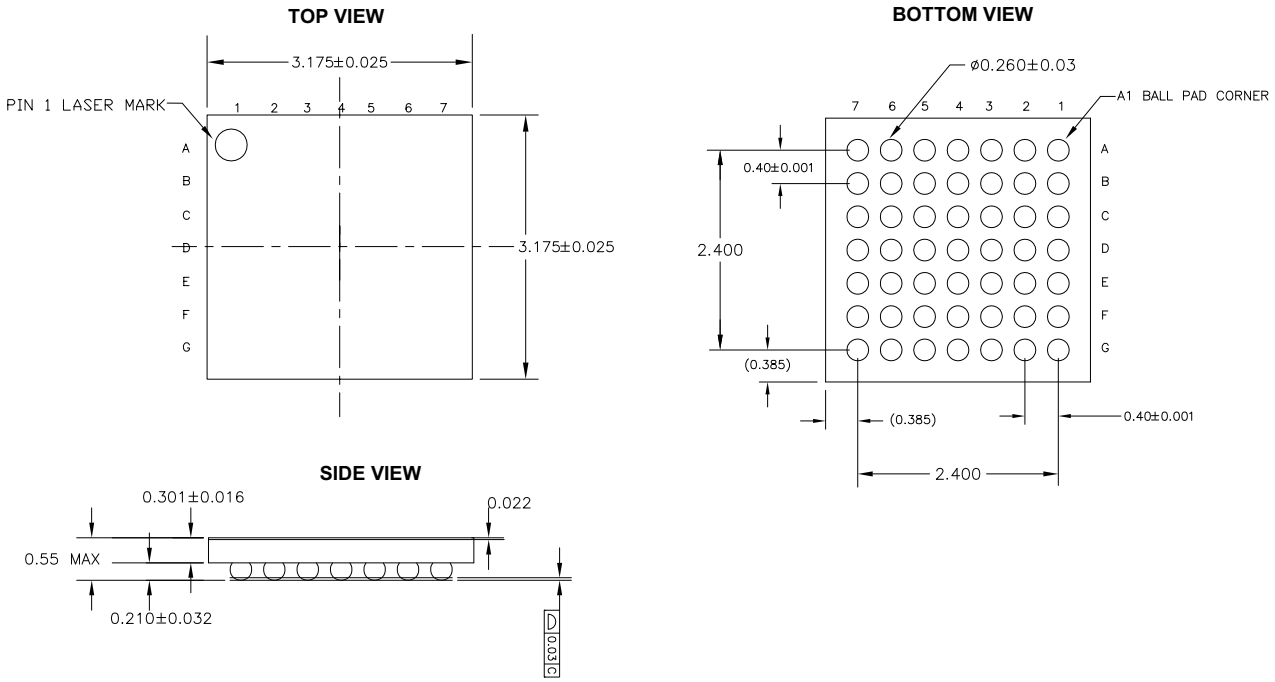
TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. PACKAGE WEIGHT: 1.482 grams
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *A

Figure 7. 49-Ball CSP (3.2 × 3.2 × 0.55 mm)



NOTES:
ALL DIMENSION ARE IN MILLIMETER
PACKAGE WEIGHT: 0.010grams
JEDEC PUBLICATION 95

001-50507 *C

Important Note

For information on the preferred dimensions for mounting CSP packages, see the application note at Application Note for Surface Mount Assembly of Amkor's Eutectic and Lead-Free CSP[nl]™ Wafer Level Chip Scale Packages

Thermal Impedances

Table 16. Thermal Impedances per Package[8]

Package	Typical θ_{JA}
36-Pin QFN	19 °C/W
48-Pin QFN	19 °C/W
49-Ball CSP	30 °C/W

Solder Reflow

Table 17 lists the maximum solder reflow peak temperatures to achieve good solderability. Thermal ramp rate during preheat should be 3 °C/s or lower

Table 17. Solder Reflow

Package	Maximum Peak Temperature	Time at Maximum Temperature
36-Pin QFN	260 °C, –5/+0 °C	10–20s
48-Pin QFN	260 °C, –5/+0 °C	10–20s
49-Ball CSP	260 °C, –5/+0 °C	10–20s

Note
8. $T_J = T_A + \text{Power} \times \theta_{JA}$.

Development Tools

This section presents the development tools available for the CY8CTMA340 devices.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Used by thousands of PSoC developers, this robust software has made designing with PSoC easy for half a decade. TrueTouch products require a dedicated PSoC Designer installer. Contact your local sales representative or send your request to tsbusdev@cypress.com.

PSoC Programmer

PSoC Programmer is flexible enough to be used on the bench in development, yet suitable for factory programming. It works as a standalone programming application, or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with PSoC MiniProg. PSoC programmer is available free of charge at
http://www.cypress.com/psocprogrammer.

Development Kits

Contact your local Cypress sales representative to order a CY3290-TMA300 development kit.

Device Programmers

All device programmers are available for purchase from The Cypress Store.

For programming during development, use:

- MiniProg1 Programming Unit (does not support debug monitor). It is available for purchase through the Cypress online store as part of kit:CY3210-MiniProg1.
- MiniProg3 Programming Unit (supports debug monitor). It is available for purchase through the Cypress online store as part of kit:CY8CKIT-002.

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Ordering Information

The following table lists the TrueTouch Standard Product Multi-Touch All-Points Touchscreen Controllers. For information on other TrueTouch families, please visit http://www.cypress.com/truetouch.

Table 18. Device Ordering Information

	TrueTouch									TrueTouch+				Sensor										
Part Number	Max Screen Size (in.) (4:3 Aspect Ratio)	Maximum Nodes	Maximum Fingers	Ghost Free Tracking	Grip Suppression	Wet Finger Tracking	Water Rejection	On-chip Gesture Decoding	Face Suppression (Large Object)	Capacitive Buttons/Slider	Proximity Detection	Hover Tracking	Stylus	Glass	Film	Minimum Interface Voltage	Digital Supply Voltage Operating Range	Analog Supply Voltage Operating Range Voltage	Bootloader	I^2C	SPI	Package	Unique ID
CY8CTMA340-LQI-11(T)	3.2	132	4	✔	–	–	✔	✔	✔	✔	✔	✔	✔	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	36 QFN	058DH
CY8CTMA340-48LQI-11(T)	4.5	256	4	✔	–	–	✔	✔	✔	✔	✔	✔	✔	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	48 QFN	058EH
CY8CTMA340-FNI-11T	4.5	256	4	✔	–	–	✔	✔	✔	✔	✔	✔	✔	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	49 CSP	058FH
CY8CTMA340-LQI-09(T)	3.2	132	4	✔	–	–	✔	✔	✔	✔	–	–	–	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	36 QFN	0590H
CY8CTMA340-48LQI-09(T)	4.5	256	4	✔	–	–	✔	✔	✔	✔	–	–	–	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	48 QFN	0591H
CY8CTMA340-FNI-09T	4.5	256	4	✔	–	–	✔	✔	✔	✔	–	–	–	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	49 CSP	0592H
CY8CTMA340-LQI-03(T)	3.2	132	2	✔	–	–	✔	✔	✔	✔	✔	✔	✔	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	36 QFN	0596H
CY8CTMA340-48LQI-03(T)	4.5	256	2	✔	–	–	✔	✔	✔	✔	✔	✔	✔	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	48 QFN	0597H
CY8CTMA340-FNI-03T	4.5	256	2	✔	–	–	✔	✔	✔	✔	✔	✔	✔	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	49 CSP	0598H
CY8CTMA340-LQI-01(T)	3.2	132	2	✔	–	–	✔	✔	✔	✔	–	–	–	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	36 QFN	0599H
CY8CTMA340-48LQI-01(T)	4.5	256	2	✔	–	–	✔	✔	✔	✔	–	–	–	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	48 QFN	059AH
CY8CTMA340-FNI-01T	4.5	256	2	✔	–	–	✔	✔	✔	✔	–	–	–	✔	✔	1.8	1.71-3.3	2.7-3.3	✔	✔	✔	49 CSP	059BH

Ordering Code Definitions

CY8 C TMA 340 - xxx xx(T)

Feature Set: (T=Tape and Reel)
01 = 2 fingers
03 = 2 fingers, stylus, proximity and hover
09 = 4 fingers
11 = 4 fingers, stylus, proximity and hover

Pins/Package Type:
LQI = 36-Pin 0.6 mm Height QFN
48LQI = 48-Pin 0.6 mm Height QFN
FNI = 49-Ball 0.55 mm Height CSP, Tape and Reel Only

Sub-family Identifier

Family Code: TMA = Multi-Touch All-Points Controller

Technology Code: C = CMOS

Marketing Code: CY8 = Cypress PSoC

Document Conventions

Port Nomenclature

Px[y] describes a particular bit “y” available within an I/O port “x.” For example, P4[2] reads “port 4, bit 2."

Bit Field Nomenclature

z[x:y] describes a particular range of bits “x to y” within a register named “z.” For example, TSNV[15:11] refers to bits 15 through 11 within a register named TSNV.

Acronyms

Acronym	Description
ADC	analog-to-digital converter
CPU	central processing unit
CSP	chip scale package
EP	exposed pad
ESD	electrostatic discharge
FPC	flexible printed circuit
GPIO	general purpose input/output
ILO	internal low speed oscillator
IMO	internal main oscillator
ISSP	in-system serial programming
ITO	indium tin oxide
I^2C	inter-integrated circuit
I/O	input/output
LCD	liquid crystal display
LDO	low dropout regulator
LVD	low voltage detect
PCB	printed circuit board
POR	power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
QFN	quad flat no-lead
QVGA	quarter video graphics array
RF	radio frequency
SCL	serial I^2C clock
SCLK	serial ISSP clock
SDA	serial I^2C data
SDATA	serial ISSP data
SNR	signal-to-noise ratio
SPI	serial peripheral interface
SRAM	static random access memory
TRM	technical reference manual
UART	universal asynchronous receiver/transmitter

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohms
MHz	megahertz
MΩ	megaohms
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µVrms	microvolts root-mean-square
fF-rms	femtofarads root-mean-square
µW	microwatts
mA	milliamperes
mm	millimeters
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pA	picoamperes
pF	picofarads
pp	peak-to-peak
ppm	parts per million
ps	picoseconds
sps	samples per second
σ	sigma: one standard deviation
V	volts

See the Glossary on page 21 for definitions of terms used in this document.

Reference Documents

Reference documents are available through your local Cypress sales representative. You can also direct your requests to tsbusdev@cypress.com.

001-55166 – *TrueTouch™ Standard Products Platform Technical Reference Manual (TRM)*. Contains detailed information on communication protocol, modes and registers, power states, and instructions on getting started with supporting tools.

001-49389 – *TrueTouch™ Performance Parameters*. Contains Cypress touchscreen parameter definitions, justification for parameters, and parameter test methodologies.

001-50467 – *TrueTouch™ Touchscreen Module Design Best Practices.* A system-level design guide for building a capacitive touchscreen module, covering topics such as touchscreen traces, shielding, mechanical design, FPC/PCB design, and LCD considerations.

001-56148 – *TrueTouch™ Touchscreen Module Integration Best Practices.* Describes the best practices to be followed when integrating a touchscreen module into a completed end-product in its final form factor, from completion of touchscreen module bench testing to production readiness.

001-59452 – *In-System Serial Programming (ISSP) Protocol for CY8CTMA3xx AN2026D*. Contains information and directions for externally programming a CY8CTMA3xx device.

001-59388 – *Host Sourced Serial Programming for CY8CTMA3xx AN59388.* Contains information and directions for programming a CY8CTMA3xx device from the system host processor.

Glossary

All-Points	Cypress brand name for TrueTouch devices capable of unlimited number of independent finger tracking.
analog integration	The process of accumulating charge on an internal integration capacitor. Each TX waveform cycle (period) contributes to the charge accumulation. The accumulation of charge causes the integration capacitor voltage to rise. After analog integration, the integration capacitor voltage is sampled by the ADC.
channel	The analog circuitry responsible for measuring capacitance. It contains RX and TX sections and a multiplexer to connect the sense pins to the RX and TX sections. Eight parallel channels are available for capacitance sensing.
conversion	The process of measuring the capacitance of a sensor connected to a pin (self capacitance) or capacitance between a pair of sensors connected to different pins (mutual capacitance). The result is a number that can be processed by the CPU. A conversion result is made available to the CPU after digital integration is complete.
core accuracy	The maximum position error in the core (center) region of the touchscreen, excluding a border around the perimeter of the touchscreen. See Cypress's *TrueTouch™ Touchscreen Controller Performance Parameters* (001-49389) for more information.
digital integration	The process of accumulating ADC samples in a register.
mutual capacitance	The capacitance between two sense pins. This includes the capacitance formed between the intersection of TX and RX sensors.
noise free resolution	The minimum jitter-free resolvable distance expressed in millimeters. See Cypress's *TrueTouch™ Touchscreen Controller Performance Parameters* (001-49389) for more information.
RX	Receive. A sensor is defined as RX if it connects to a sense pin configured as RX. A sense pin is configured as RX if it is multiplexed to a RX section of a channel. The RX section of a channel is responsible for integrating the charge received through a sense pin configured as RX.
scan	The conversion of all sensor capacitances to digital values.
self capacitance	The capacitance between one or more sense pins to circuit ground.
sense pin	A pin that can be multiplexed to the RX or TX sections of a channel.
signal-to-noise ratio (SNR)	The ratio between a capacitive finger signal and system noise. See Cypress's *Touchscreen Controller Performance Parameters* (001-049389) for more information.
stackup	Layers of materials of different thicknesses in defined order that make up a touchscreen panel.
startup	The period of register initialization after a supply voltage is applied to V_{DD}.
$T_{PROCESS}$	The time it takes to process the new digital information after a scan and then signal an interrupt to the host.
$T_{REFRESH}$	The time between two consecutive frames of touchscreen data available in a data buffer while a finger is present on the touchscreen. The refresh rate is a sum of T_{SCAN}, $T_{PROCESS}$, and T_{SLEEP}. The fastest refresh rate is achieved when the sleep time is removed. See Cypress's *TrueTouch™ Touchscreen Controller Performance Parameters* (001-49389) for more information.

T_{SCAN}	The time it takes to convert all intersection capacitances on the touchscreen to digital values, including all analog and digital integration time.
T_{SLEEP}	The time the device is asleep during $T_{REFRESH}$ in order to reduce average power.
TX	Transmit. A sensor is defined as TX if it connects to a sense pin configured as TX. A sense pin is configured as TX if it is multiplexed to a TX section of a channel. The TX section of a channel is responsible for transmitting charge from a sense pin configured as TX. The TX waveform is periodic and toggles between two voltages.
V_{CORE}	Internal digital supply that powers the CPU, SROM, IMO, ILO, and flash.

Document History Page

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3053510	JPX	10/08/2010	New datasheet.

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