ADC Start Conversion Timing (max)

T_{ACW}

| | 746ns | 813.8ns | 203.4ns |

AD8-AD15

Start

EOC

10μs

ADC Read Timing (max)

T_{ACW} T_{ACH}

746ns   813.8ns   203.4ns

AD8-AD15

OE

DB0-DB7   Valid Data

250ns   250ns
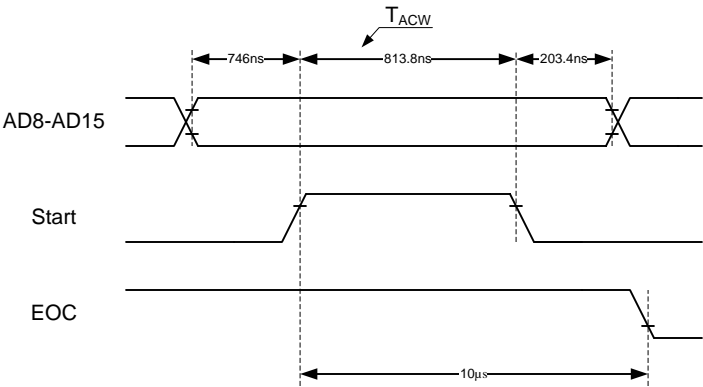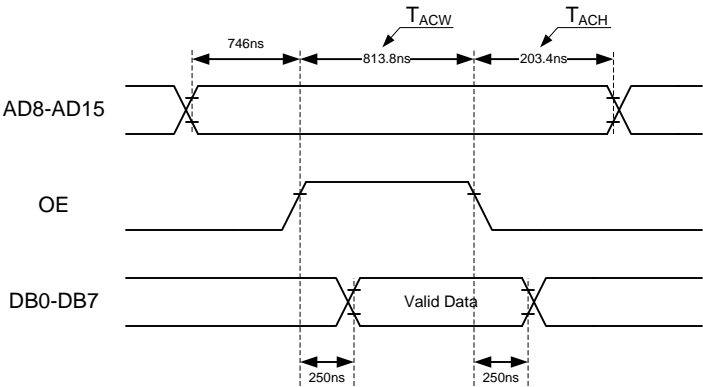
MCU External Memory Interface (EMI) Timing Parameters			
SYSCLK ⟶ 14.7456MHz		Period ⟶ 6.78168E-08	
EMI Parameter	Pulse Width Extension Factor	Total Pulse Width (sec.)	Description
T_{ALEH}	4	2.71267E-07	Address/Control latch enable high time
T_{ALEL}	4	2.71267E-07	Address/Control latch enable low time
T_{ACS}	3	2.03451E-07	Address/Control setup time
T_{ACW}	12	8.13802E-07	Address/Control pulse width for /WR & /RD
T_{ACH}	3	2.03451E-07	Address/Control hold time

ADC Timing					
	SIZE	FSCM NO	DWG NO		REV
DRAWN TBL			Figure 3: ADC Timing		1.0
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