HD66710

(Dot Matrix Liquid Crystal Display Controller/Driver)

HITACHI

Description

The HD66710 dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, numbers, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimum system can be interfaced with this controller/driver.

A single HD66710 is capable of displaying a single16-character line, two 16-character lines, or up to four 8-character lines.

The HD66710 software is upwardly compatible with the LCD-II (HD44780) which allows the user to easily replace an LCD-II with an HD66710. In addition, the HD66710 is equipped with functions such as segment displays for icon marks, a 4-line display mode, and a horizontal smooth scroll, and thus supports various display forms. This achieves various display forms. The HD66710 character generator ROM is extended to generate 240 5×8 dot characters.

The low voltage version (2.7V) of the HD66710, combined with a low power mode, is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5×8 dot matrix possible
- Low power operation support:
  - 2.7V to 5.5V (low voltage)
- Booster for liquid crystal voltage
  - Two/three times (13V max.)
- Wide range of liquid crystal display driver voltage
  - 3.0V to 13V
- Extension driver interface
- High-speed MPU bus interface (2 MHz at 5-V operation)
- 4-bit or 8-bit MPU interface capability
- 80×8-bit display RAM (80 characters max.)

- 9,600-bit character generator ROM
  - 240 characters (5 × 8 dot)
- 64 × 8-bit character generator RAM
  - 8 characters (5 × 8 dot)
- 8 × 8-bit segment RAM
  - 40-segment icon mark
- 33-common × 40-segment liquid crystal display driver
- Programmable duty cycle (See List 1)
- Wide range of instruction functions:
  - Functions compatible with LCD-II: Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
  - Additional functions: Icon mark control, 4-line display, horizontal smooth scroll, 6-dot character width control, white-black inverting blinking cursor
- Software upwardly compatible with HD44780
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with an external resistor
- Low power consumption
- QFP1420-100 pin, TQFP1414-100 pin bare-chip

List 1 Programmable Duty Cycles

Number of Lines	Duty Ratio	Displayed Character	Maximum Number of Displayed Characters Single-Chip Operation
1	1/17	5 × 8-dot	One 16-character line + 40 segments
2	1/33	5 × 8-dot	Two 16-character lines + 40 segments
4	1/33	5 × 8-dot	Four 8-character lines + 40 segments

Ordering Information

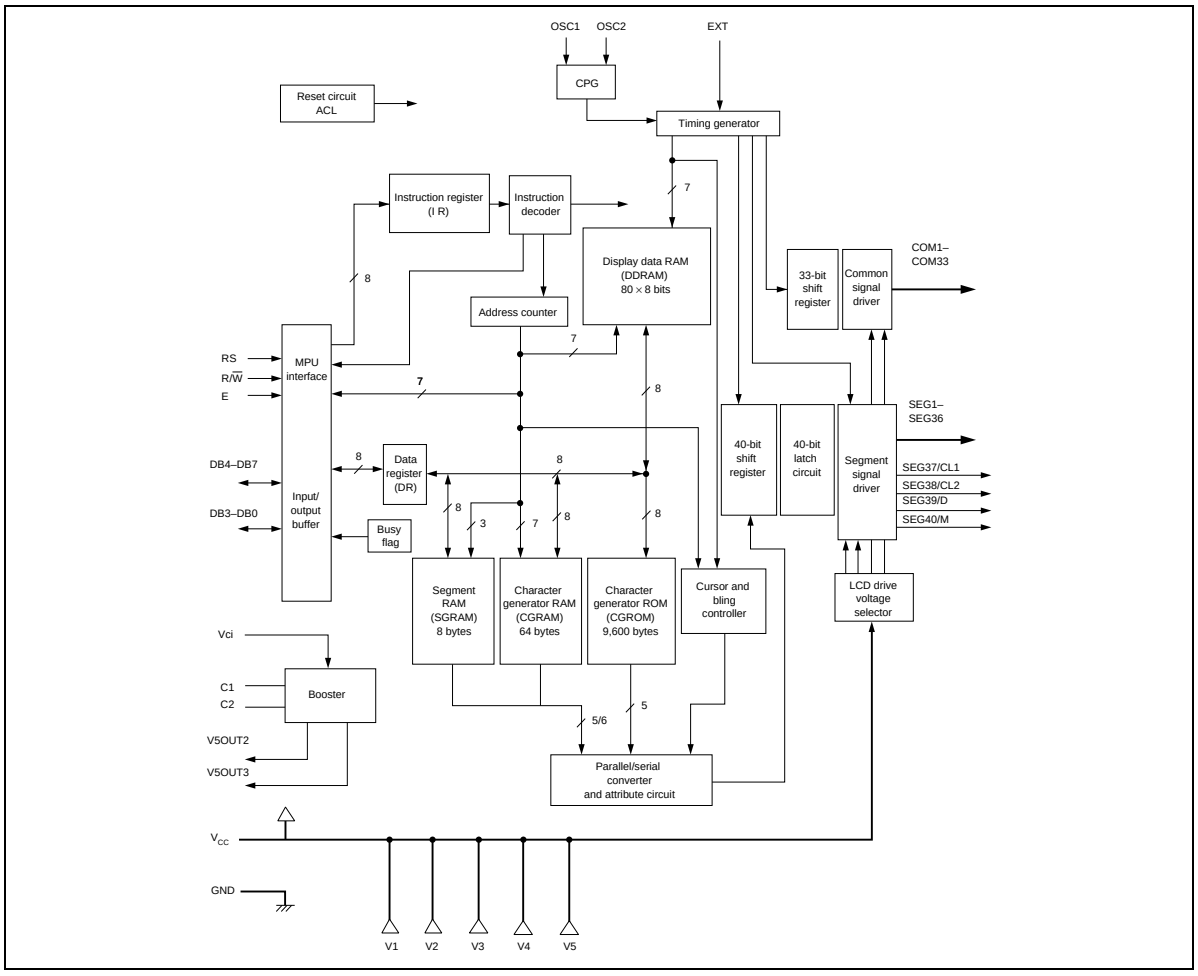
Type No.	Package	CGROM
HD66710A00FS	QFP1420-100 (FP-100A)	Japanese standard
HD66710A00TF	TQFP1414-100 (TFP-100B)	
HCD66710A00	Chip	

LCD-II Family Comparison

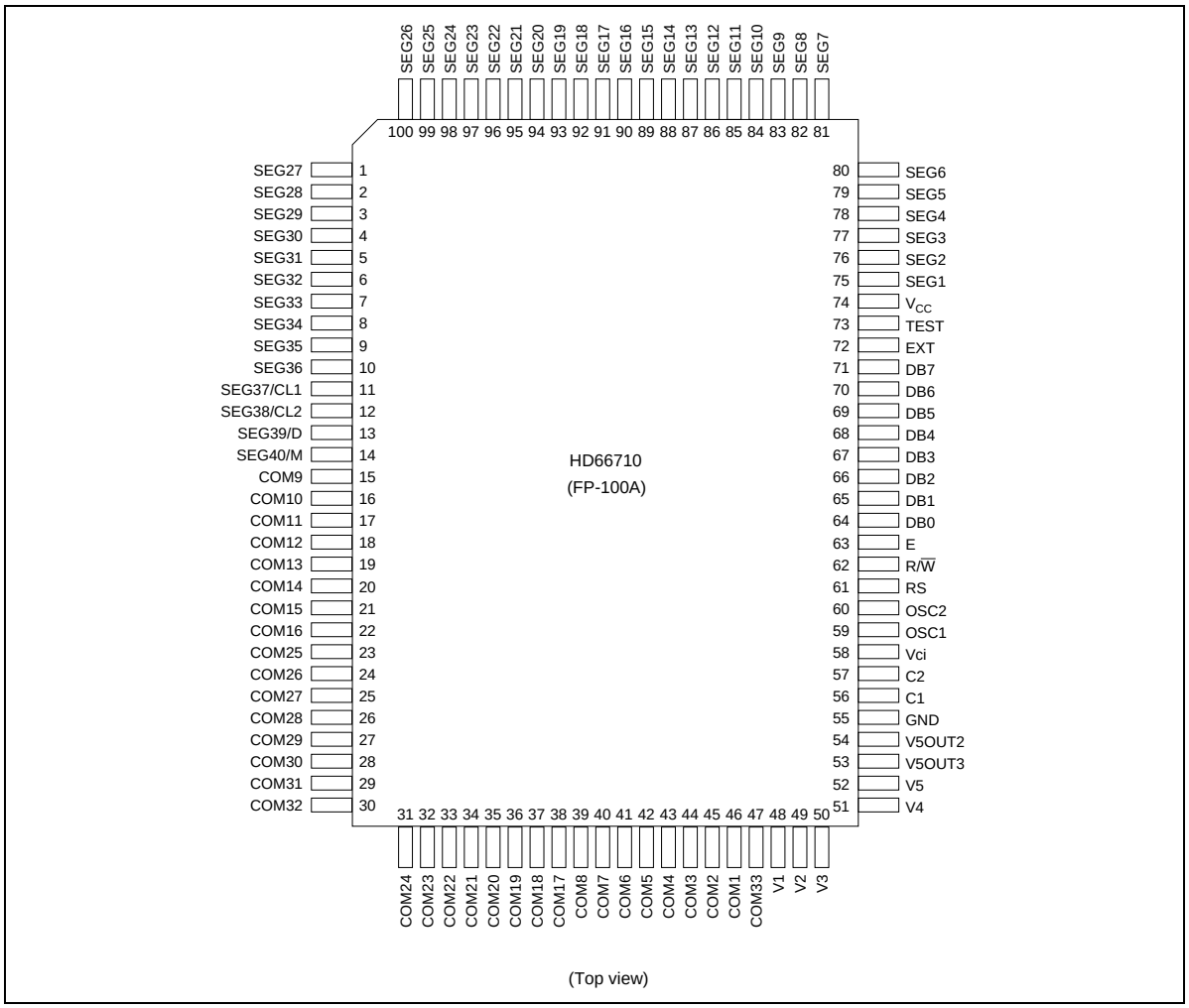
Item	LCD-II (HD44780U)	HD66702R	HD66710	HD66712U
Power supply voltage	2.7V to 5.5V	5V ±10% (standard) 2.7V to 5.5V (low voltage)	2.7V to 5.5V	2.7V to 5.5V
Liquid crystal drive voltage	3.0V to 11V	3.0V to 8.3V	3.0V to 13.0V	2.7V to 11.0V
Maximum display digits per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines	24 characters × 2 lines/ 12 characters × 4 lines
Segment display	None	None	40 segments	60 segments
Display duty cycle	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/17 and 1/33	1/17 and 1/33
CGROM	9,920 bits (208 5 × 8 dot characters and 32 5 × 10 dot characters)	7,200 bits (160 5 × 7 dot characters and 32 5 × 10 dot characters)	9,600 bits (240 5 × 8 dot characters)	9,600 bits (240 5 × 8 dot characters)
CGRAM	64 bytes	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes	80 bytes
SEGRAM	None	None	8 bytes	16 bytes
Segment signals	40	100	40	60
Common signals	16	16	33	34
Liquid crystal drive waveform	A	B	B	B
Bleeder resistor for LCD power supply	External (adjustable)	External (adjustable)	External (adjustable)	External (adjustable)
Clock source	Extenal resistor or external clock	External resistor or external clock	External resistor or external clock	External resistor or external clock
R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycle; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ±30% (70 to 130 Hz for 1/8 and 1/16 duty cycle; 51 to 95 Hz for 1/11 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)
R_f resistance	91 kΩ: 5-V operation; 75 kΩ: 3-V operation	68 kΩ: 5-V operation; 56 kΩ: (3-V operation)	91 kΩ: 5-V operation; 75 kΩ: 3-V operation)	130 kΩ: 5-V operation; 110 kΩ: 3-V operation
Liquid crystal voltage booster circuit	None	None	2-3 times step-up circuit	2-3 times step-up circuit

Item	LCD-II (HD44780U)	HD66702R	HD66710	HD66712U
Extension driver control signal	Independent control signal	Independent control signal	Used in common with a driver output pin	Independent control signal
Reset function	Power on automatic reset	Power on automatic reset	Power on automatic reset	Power on automatic reset or reset input
Instructions	LCD-II (HD44780)	Fully compatible with the LCD-II	Upper compatible with the LCD-II	Upper compatible with the LCD-II
Number of displayed lines	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4
Low power mode	None	None	Available	Available
Horizontal scroll	Character unit	Character unit	Dot unit	Dot unit
Bus interface	4 bits/8 bits	4 bits/8 bits	4 bits/8 bits	Serial; 4 bits/8 bits
CPU bus timing	2 MHz: 5-V operation; 1 MHz: 3-V operation	1 MHz	2 MHz: 5-V operation; 1 MHz: 3-V operation	2 MHz: 5-V operation; 1 MHz: 3-V operation
Package	QFP-1420-80 80-pin bare chip	LQFP-2020-144 144-pin bare chip	QFP-1420-100 100-pin bare chip TQFP1414-100	TCP-128 128-pin bare chip

HD66710 Block Diagram

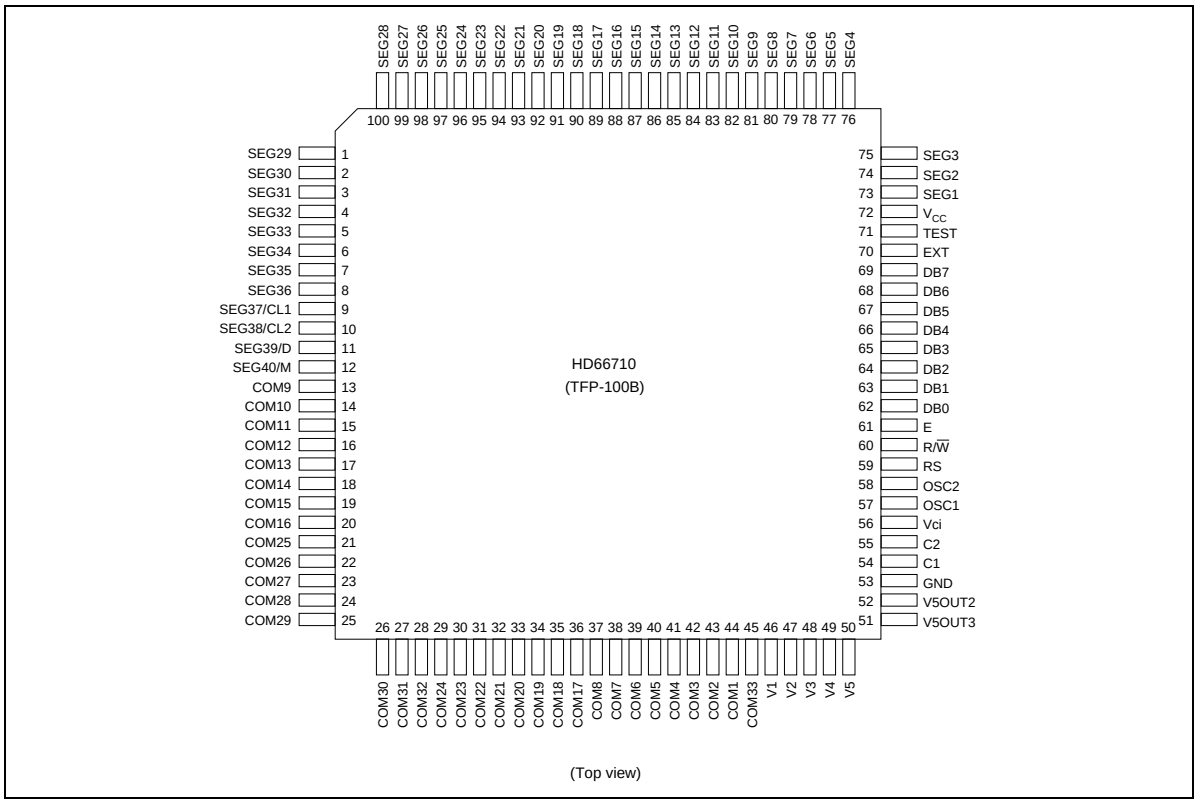


HD66710 Pin Arrangement



(Top view)

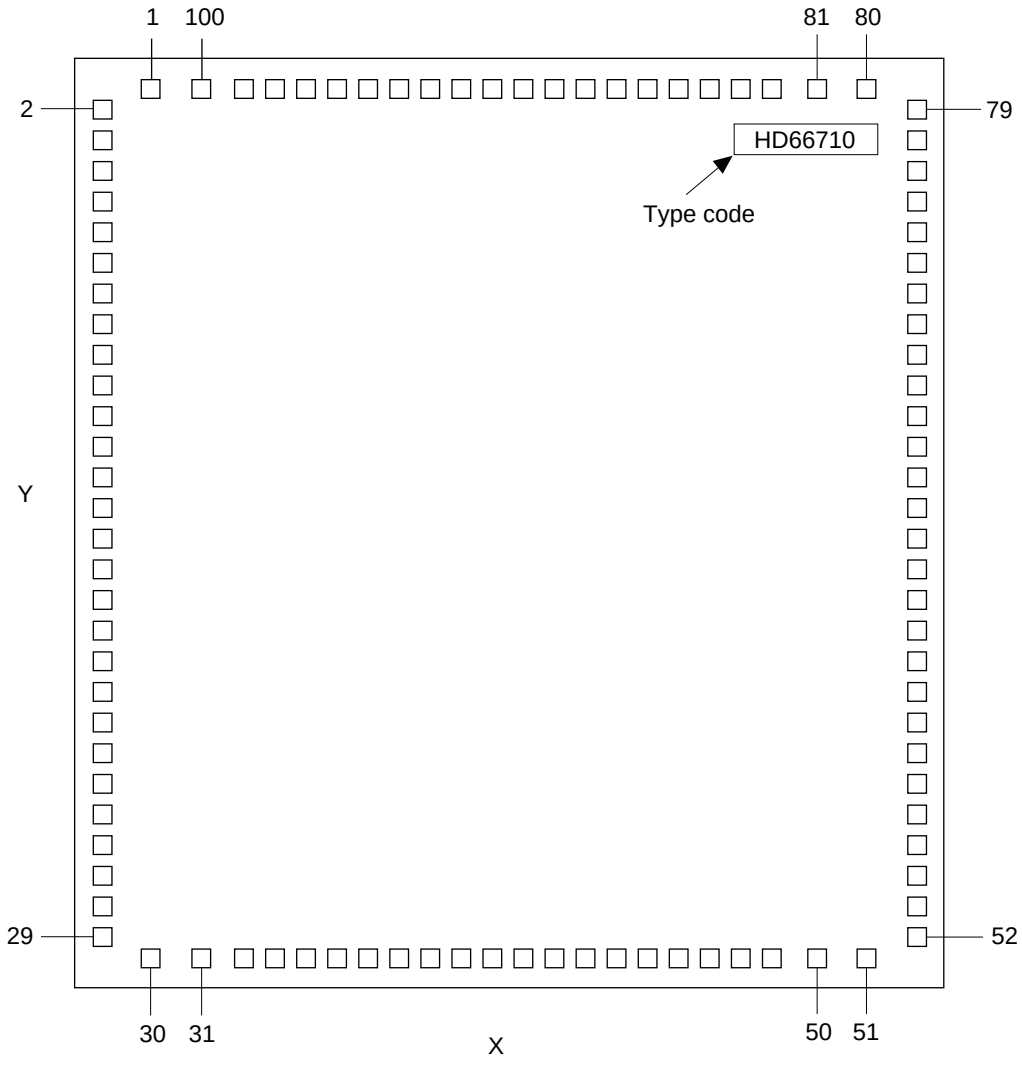
HD66710 Pin Arrangement (TQFP1414-100 Pin)



(Top view)

HD66710 Pad Arrangement

Chip size (X × Y): 5.36 mm × 6.06 mm
Coordinate : Pad center
Origin : Chip center
Pad size (X × Y) : 100 µm × 100 µm



HD66710 Pad Location Coordinates

Pin No.	Pad Name	X	Y
1	SEG27	–2495	2910
2	SEG28	–2695	2730
3	SEG29	–2695	2499
4	SEG30	–2695	2300
5	SEG31	–2695	2100
6	SEG32	–2695	1901
7	SEG33	–2695	1698
8	SEG34	–2695	1498
9	SEG35	–2695	1295
10	SEG36	–2695	1099
11	SEG37	–2695	900
12	SEG38	–2695	700
13	SEG39	–2695	501
14	SEG40	–2695	301
15	COM9	–2695	98
16	COM10	–2695	–113
17	COM11	–2695	–302
18	COM12	–2695	–501
19	COM13	–2695	–701
20	COM14	–2695	–900
21	COM15	–2695	–1100
22	COM16	–2695	–1303
23	COM25	–2695	–1502
24	COM26	–2695	–1702
25	COM27	–2695	–1901
26	COM28	–2695	–2101
27	COM29	–2695	–2300
28	COM30	–2695	–2500
29	COM31	–2695	–2731
30	COM32	–2495	–2910
31	COM24	–2051	–2910
32	COM23	–1701	–2910
33	COM22	–1498	–2910
34	COM21	–1302	–2910
35	COM20	–1102	–2910
36	COM19	–899	–2910
37	COM18	–700	–2910
38	COM17	–500	–2910
39	COM8	–301	–2910
40	COM7	–101	–2910
41	COM6	99	–2910
42	COM5	302	–2910
43	COM4	502	–2910
44	COM3	698	–2910
45	COM2	887	–2910
46	COM1	1077	–2910
47	COM33	1266	–2910
48	V1	1488	–2910
49	V2	1710	–2910
50	V3	2063	–2910
51	V4	2458	–2910
52	V5	2660	–2731
53	V5OUT3	2660	–2500
54	V5OUT2	2660	–2300
55	GND	2640	–2090
56	C1	2650	–1887
57	C2	2675	–1702
58	Vci	2675	–1502
59	OSC1	2675	–1303
60	OSC2	2675	–1103
61	RS	2675	–900
62	R/$\overline{W}$	2675	–701
63	E	2675	–501
64	DB0	2675	–302
65	DB1	2675	–99
66	DB2	2675	98
67	DB3	2675	301
68	DB4	2675	501
69	DB5	2675	700
70	DB6	2675	900
71	DB7	2675	1099
72	EXT	2675	1299
73	TEST	2675	1502
74	V_{CC}	2695	1698
75	SEG1	2695	1901
76	SEG2	2695	2104
77	SEG3	2695	2300
78	SEG4	2695	2503
79	SEG5	2695	2730
80	SEG6	2495	2910
81	SEG7	2049	2910
82	SEG8	1699	2910
83	SEG9	1499	2910
84	SEG10	1300	2910
85	SEG11	1100	2910
86	SEG12	901	2910
87	SEG13	701	2910
88	SEG14	502	2910
89	SEG15	299	2910
90	SEG16	99	2910
91	SEG17	–101	2910
92	SEG18	–301	2910
93	SEG19	–500	2910
94	SEG20	–700	2910
95	SEG21	–899	2910
96	SEG22	–1099	2910
97	SEG23	–1302	2910
98	SEG24	–1501	2910
99	SEG25	–1701	2910
100	SEG26	–2051	2910

Pin Functions

Table 1 Pin Functional Description

Signal	I/O	Device Interfaced with	Function
RS	I	MPU	Selects registers 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/$\overline{W}$	I	MPU	Selects read or write 0: Write 1: Read
E	I	MPU	Starts data read/write
DB4 to DB7	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66710. DB7 can be used as a busy flag.
DB0 to DB3	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66710. These pins are not used during 4-bit operation.
COM1 to COM33	O	LCD	Common signals; those are not used become non-selected waveforms. At 1/17 duty rate, COM1 to COM16 are used for character display, COM17 for icon display, and COM18 to COM33 become non-selected waveforms. At 1/33 duty rate, COM1 to COM32 are used for character display, and COM33 for icon display.
SEG1 to SEG35	O	LCD	Segment signals
SEG36	O	LCD	Segment signal. When EXT = high, the same data as that of the first dot of the extension driver is output.
SEG37/CL1	O	LCD/ Extension driver	Segment signal when EXT = low. When EXT = high, outputs the extension driver latch pulse.
SEG38/CL2	O	LCD/ Extension driver	Segment signal when EXT = low. When EXT = high, outputs the extension driver shift clock.
SEG39/D	O	LCD/ Extension driver	Segment signal at EXT = low. At EXT = high, the extension driver data. Data on and after the 36th dot is output.
SEG40/M	O	LCD/ Extension driver	Segment signal when EXT = low. When EXT = high, outputs the extension driver AC signal.
EXT	I	—	Extension driver enable signal. When EXT = high, SEG37 to SEG40 become extension driver interface signals. At this time, make sure that V5 level is lower than GND level (0 V). V5 (low) ≤ GND (high).
V1 to V5	—	Power supply	Power supply for LCD drive V_{cc} – V5 = 13V (max)

Table 1 Pin Functional Description (cont)

Signal	I/O	Device Interfaced with	Function
V_{cc}, GND	—	Power supply	V_{cc}: +2.7V to 5.5V, GND: 0V
OSC1, OSC2	—	Oscillation resistor clock	When CR oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1.
Vci	I	—	Input voltage to the booster, from which the liquid crystal display drive voltage is generated. Vci is reference voltage and power supply for the booster. Vci = 1.0V to 5.0V ≤ V_{cc}
V5OUT2	O	V5 pin/ Booster capacitance	Voltage input to the Vci pin is boosted twice and output When the voltage is boosted three times, the same capacity as that of C1–C2 should be connected.
V5OUT3	O	V5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	—	Booster capacitance	External capacitance should be connected when using the booster.
TEST	I	—	Test pin. Should be wired to ground.

Function Description

Registers

The HD66710 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for the display data RAM (DDRAM), the character generator RAM (CGRAM), and the segment RAM (SEGRAM). The MPU can only write to IR, and cannot be read from.

The DR temporarily stores data to be written into DDRAM, CGRAM, or SEGRAM. Data written into the DR from the MPU is automatically written into DDRAM, CGRAM, or SEGRAM by an internal operation. The DR is also used for data storage when reading data from DDRAM, CGRAM, or SEGRAM. When address infor-mation is written into the IR, data is read and then stored into the DR from DDRAM, CGRAM, or SEGRAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DDRAM, CGRAM, or SEGRAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (Table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66710 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/$\overline{W}$ = 1 (Table 2), the busy flag is output from DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DDRAM, CGRAM, or SEGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DDRAM, CGRAM, and SEGRAM is also determined concurrently by the instruction.

After writing into (reading from) DDRAM, CGRAM, or SEGRAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB0 to DB6 when RS = 0 and R/$\overline{W}$ = 1 (Table 2).

Table 2 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DDRAM, CGRAM, or SEGRAM)
1	1	DR read as an internal operation (DDRAM, CGRAM, or SEGRAM to DR)

Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (ADD) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (Figure 2)
  - — When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD66710, 16 characters are displayed. See Figure 3.

    When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

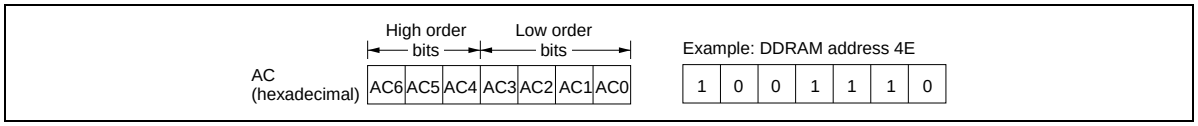


Figure 1 DDRAM Address

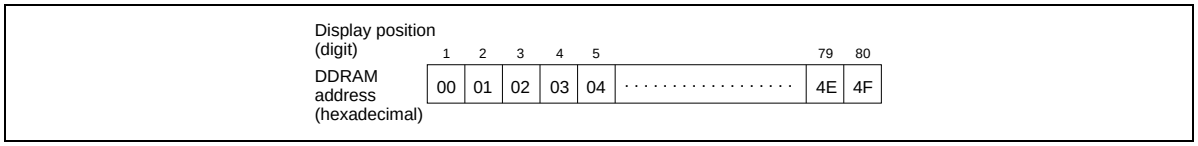


Figure 2 1-Line Display

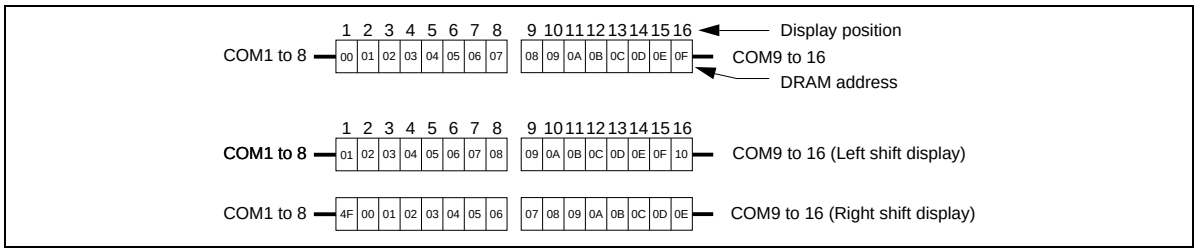


Figure 3 1-line by 16-Character Display Example

- 2-line display (N = 1, and NW = 0)
  - — Case 1: The first line is displayed from COM1 to COM16, and the second line is displayed from COM17 to COM32. Care is required because the end address of the first line and the start address of the second line are not consecutive. For example, the case is shown in Figure 5 where 16 × 2-line display is performed using the HD66710. When a display shift operation is performed, the DDRAM address shifts. See Figure 4.

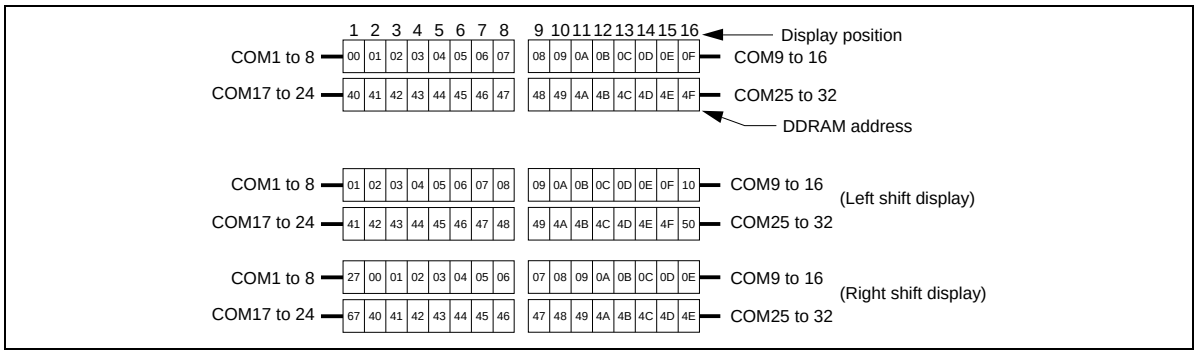


Figure 4 2-line by 16-Character Display Example

  - — Case 2: Figure 5 shows the case where the EXT pin is fixed to high, the HD66710 and the 40-output extension driver are used to extend the number of display characters.

    In this case, the start address from COM9 to COM16 of the HD66710 is 0AH, and that from COM25 to COM32 of the HD66710 is 4AH. To display 24 characters, the addresses starting at SEG11 should be used.

    When a display shift operation is performed, the DDRAM address shifts. See Figure 5.

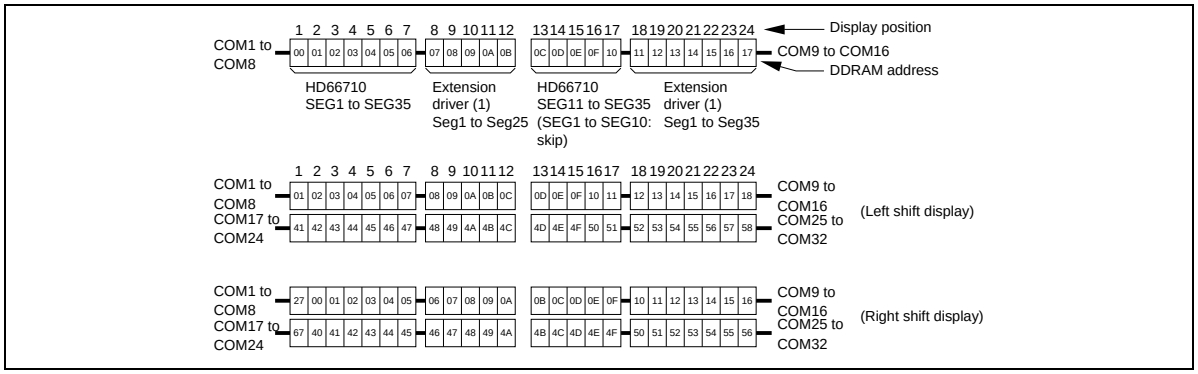


Figure 5 2-Line by 24 Character Display Example

- 4-line display (NW = 1)
  - Case 1: The first line is displayed from COM1 to COM8, the second line is displayed from COM9 to COM16, the third line is displayed from COM17 to COM24, and the fourth line is displayed from COM25 to COM32. Care is required because the DDRAM addresses of each line are not consecutive. For example, the case is shown in Figure 6 where 8 × 4-line display is performed using the HD66710.

    When a display shift operation is performed, the DDRAM address shifts. See Figure 6.

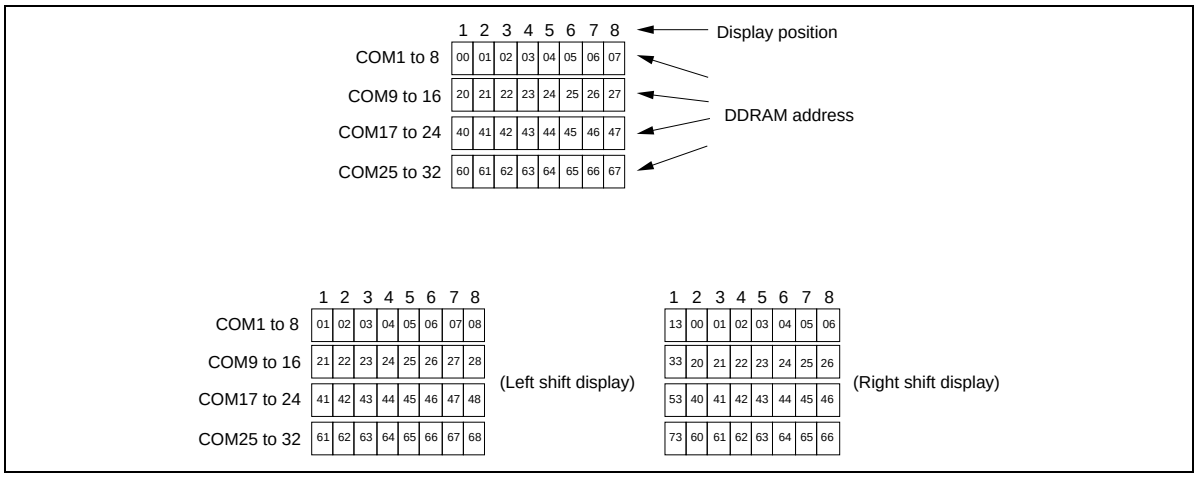


Figure 6 4-Line Display

— Case 2: The case is shown in figure where the EXT pin is fixed high, and the HD66710 and the 40-output extension driver are used to extend the number of display characters.

When a display shift operation is performed, the DDRAM address shifts. See Figure 7.

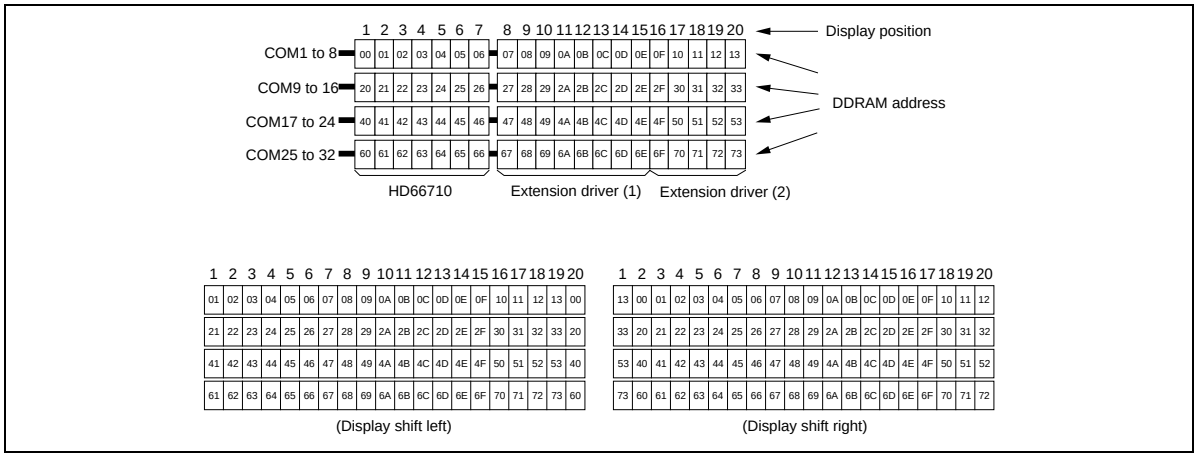


Figure 7 4-Line by 20-Character Display Example

Character Generator ROM (CGROM)

The character generator ROM generates 5 × 8 dot character patterns from 8-bit character codes (Table 3). It can generate 240 5 × 8 dot character patterns. User-defined character patterns are also available using a mask-programmed ROM.

Character Generator RAM (CGRAM)

The character generator RAM allows the user to redefine the character patterns. In the case of 5 × 8 characters, up to eight may be redefined.

Write the character codes at the addresses shown as the left column of Table 3 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns.

Segment RAM (SEGRAM)

The segment RAM (SEGRAM) is used to enable control of segments such as an icon and a mark by the user program.

For a 1-line display, SEGRAM is read from the COM17 output, and as for 2- or 4-line displays, it is from the COM33 output, to performs 40-segment display.

As shown in Table 6, bits in SEGRAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DDRAM and CGRAM.

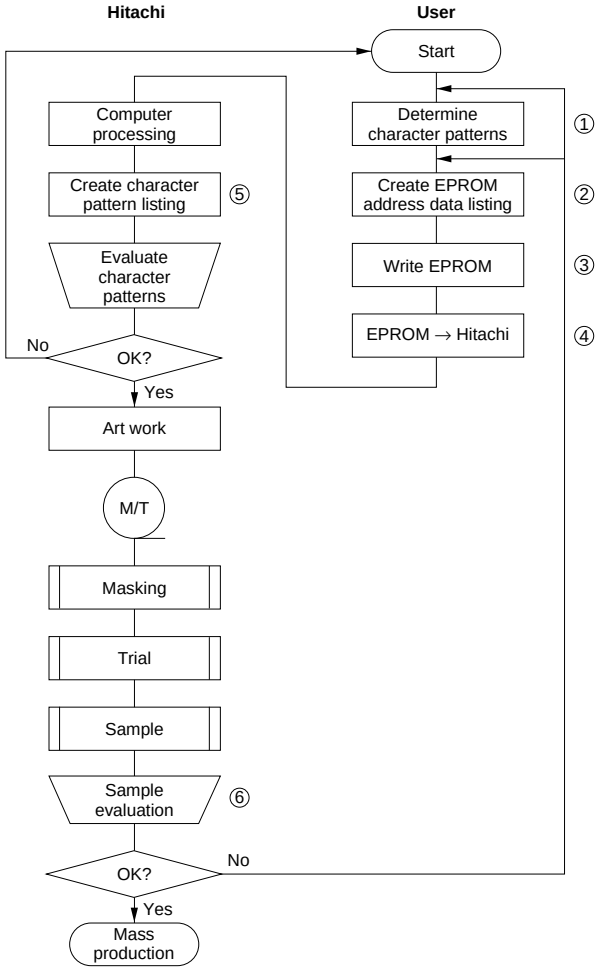
SEGRAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

Modifying Character Patterns

- Character pattern development procedure

  The following operations correspond to the numbers listed in Figure 8:

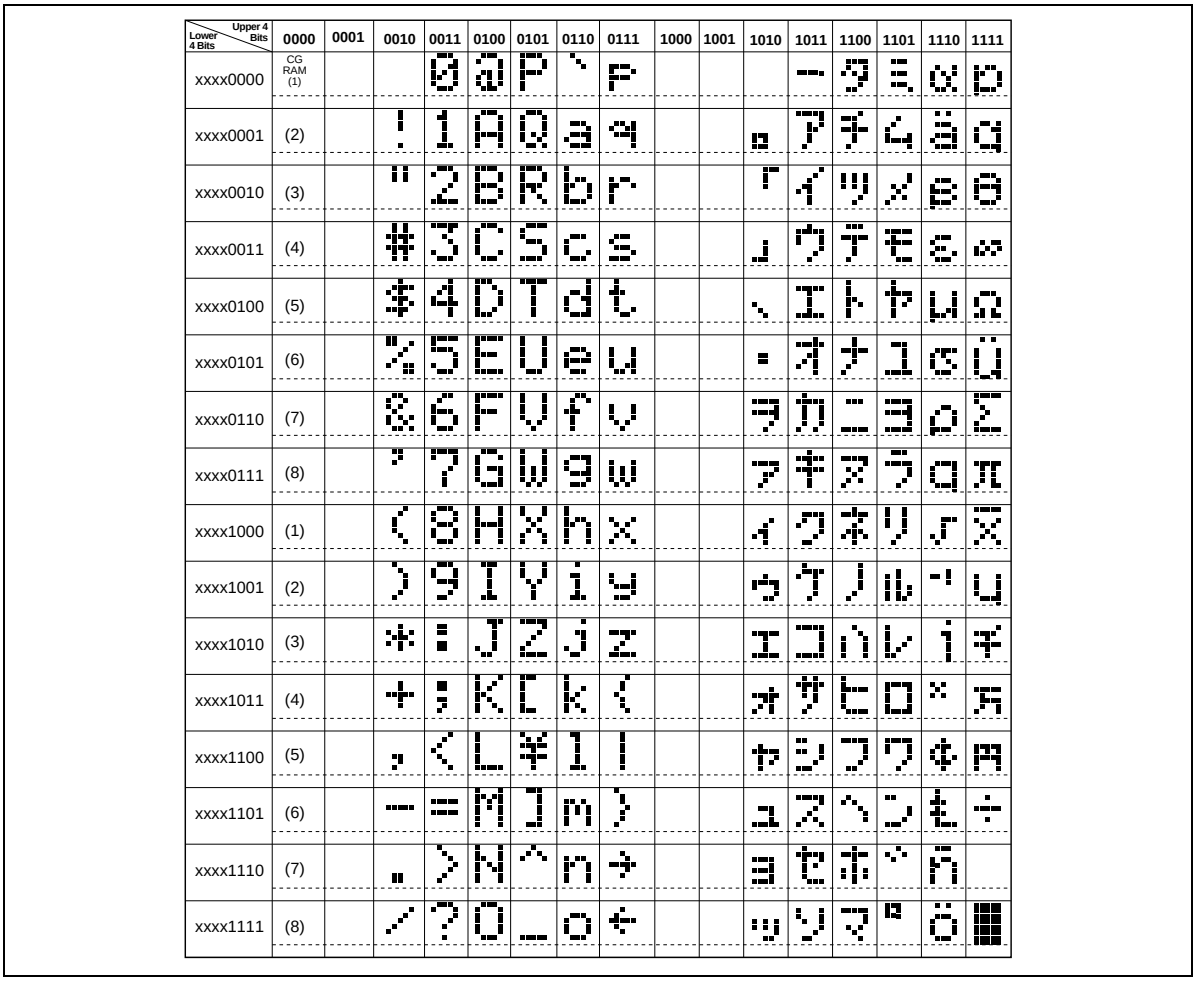
  1. Determine the correspondence between character codes and character patterns.
  2. Create a listing indicating the correspondence between EPROM addresses and data.
  3. Program the character patterns into an EPROM.
  4. Send the EPROM to Hitachi.
  5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
  6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI will proceed at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 8 Character Pattern Development Procedure

Table 3 Correspondence between Character Codes and Character Patterns (Hitachi Standard HD66710)



Upper 4 Bits / Lower 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)			0	@	P	`	p				—	夕	ミ	α	p
xxxx0001	(2)		!	1	A	Q	a	q			。	ア	チ	ム	ä	q
xxxx0010	(3)		"	2	B	R	b	r			「	イ	ツ	メ	ß	θ
xxxx0011	(4)		#	3	C	S	c	s			」	ウ	テ	モ	ε	∞
xxxx0100	(5)		$	4	D	T	d	t			、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)		%	5	E	U	e	u			・	オ	ナ	ユ	σ	ü
xxxx0110	(7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)		'	7	G	W	g	w			ァ	キ	ヌ	ラ	q	π
xxxx1000	(1)		(	8	H	X	h	x			ィ	ク	ネ	リ	√	𝑥
xxxx1001	(2)		)	9	I	Y	i	y			ゥ	ケ	ノ	ル	-1	y
xxxx1010	(3)		*	:	J	Z	j	z			ェ	コ	ハ	レ	j	千
xxxx1011	(4)		+	;	K	[	k	{			ォ	サ	ヒ	ロ	x	万
xxxx1100	(5)		,	<	L	¥	l	|			ャ	シ	フ	ワ	¢	円
xxxx1101	(6)		-	=	M	]	m	}			ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)		.	>	N	^	n	→			ョ	セ	ホ	゛	ñ	
xxxx1111	(8)		/	?	O	_	o	←			ッ	ソ	マ	゜	ö	■

Note: The user can specify any pattern in the character-generator RAM.

- Programming character patterns

  This section explains the correspondence between addresses and data used to program character patterns in EPROM. The HD66710 character generator ROM can generate 240 5×8 dot character patterns.

  — Character patterns

  EPROM address data and character pattern data correspond with each other to form a 5×8 dot character pattern (Table 4).

Table 4 Example of Correspondence between EPROM Address Data and Character Pattern (5×8 Dots)

EPROM Address												Data				
												MSB				LSB
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	O0
0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
								0	0	0	1	1	0	0	0	1
								0	0	1	0	1	0	0	0	1
								0	0	1	1	0	1	0	1	0
								0	1	0	0	0	0	1	0	0
								0	1	0	1	0	0	1	0	0
								0	1	1	0	0	0	1	0	0
								0	1	1	1	0	0	0	0	0
Character code								"0"	Line position							

Notes: 1. EPROM addresses A11 to A4 correspond to a character code.
2. EPROM addresses A2 to A0 specify a line position of the character pattern. EPROM address A3 should be set to 0.
3. EPROM data O4 to O0 correspond to character pattern data.
4. Area which are lit (indicated by shading) are stored as 1, and unlit are as 0.
5. The eighth line is also stored in the CGROM, and should also be programmed. If the eighth line is used for a cursor, this data should all be set to zero.
6. EPROM data bits O7 to O5 are invalid. 0 should be written in all bits.

— Handling unused character patterns

1. EPROM data outside the character pattern area: This is ignored by the character generator ROM for display operation so any data is acceptable.
2. EPROM data in CGRAM area: Always fill with zeros. (EPROM addresses 00H to FFH.)
3. Treatment of unused user patterns in the HD66710 EPROM: According to the user application, these are handled in either of two ways:

a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.

b. When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

Table 5 Example of Correspondence between Character Code and Character Pattern (5 × 8 Dots) in CGRAM

a) When Character Pattern in 5 × 8 Dots

Character code (DDRAM data)								CGRAM address						CGRAM data (MSB … LSB)								
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0		O7	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	*	0	0	0	0	0	0	0	0	0		*	*	*	1	0	0	0	1
											0	0	1					1	0	0	0	1
											0	1	0					1	0	0	0	1
											0	1	1					0	1	0	1	0
											1	0	0					0	0	1	0	0
											1	0	1					0	0	1	0	0
											1	1	0					0	0	1	0	0
											1	1	1					0	0	0	0	0
0	0	0	0	*	1	1	1	1	1	1	0	0	0		*	*	*	1	0	0	0	1
											0	0	1					1	0	0	0	1
											0	1	0					1	0	0	0	1
											0	1	1					0	1	0	1	0
											1	0	0					0	0	1	0	0
											1	0	1					0	0	1	0	0
											1	1	0					0	0	1	0	0
											1	1	1					0	0	0	0	0

Character pattern (1)

Character pattern (8)

Table 5 Example of Correspondence between Character Code and Character Pattern (5 × 8 Dots) in CGRAM (cont)

b) When Character Pattern in 6 × 8 Dots

Character code (DDRAM data)								CGRAM address						CGRAM data (MSB … LSB)								
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0		O7	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	*	0	0	0	0	0	0	0	0	0		*	*	0	1	0	0	0	1
											0	0	1				0	1	0	0	0	1
											0	1	0				0	1	0	0	0	1
											0	1	1				0	0	1	0	1	0
											1	0	0				0	0	0	1	0	0
											1	0	1				0	0	0	1	0	0
											1	1	0				0	0	0	1	0	0
											1	1	1				0	0	0	0	0	0
0	0	0	0	*	1	1	1	1	1	1	0	0	0		*	*	0	1	0	0	0	1
											0	0	1				0	1	0	0	0	1
											0	1	0				0	1	0	0	0	1
											0	1	1				0	0	1	0	1	0
											1	0	0				0	0	0	1	0	0
											1	0	1				0	0	0	1	0	0
											1	1	0				0	0	0	1	0	0
											1	1	1				0	0	0	0	0	0

Character pattern (1)

Character pattern (8)

Notes: 1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).

2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
3. The character data is stored with the rightmost character element in bit 0, as shown in Table 5. Characters with 5 dots in width (FW = 0) are stored in bits 0 to 4, and characters with 6 dots in width (FW = 1) are stored in bits 0 to 5.
4. When the upper four bits (bits 7 to 4) of the character code are 0, CGRAM is selected.

   Bit 3 of the character code is invalid (*). Therefore, for example, the character codes 00 (hexadecimal) and 08 (hexadecimal) correspond to the same CGRAM address.
5. A set bit in the CGRAM data corresponds to display selection, and 0 to non-selection.
6. When the BE bit of the function set register is 1, pattern blinking control of the lower six bits is controlled using the upper two bits (bits 7 and 6) in CGRAM.

   When bit 7 is 1, of the lower six bits, only those which are set are blinked on the display.

   When bit 6 is 1, a bit 4 pattern can be blinked as for a 5-dot font width, and a bit 5 pattern can be blinked as for a 6-dot font width.

* Indicates no effect.

Table 6 Relationships between SEGRAM Addresses and Display Patterns

SEGRAM address			SEGRAM data															
			a) 5-dot font width								b) 6-dot font width							
A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	B1	B0	*	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	1	B1	B0	*	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	1	0	B1	B0	*	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	1	1	B1	B0	*	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
1	0	0	B1	B0	*	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
1	0	1	B1	B0	*	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
1	1	0	B1	B0	*	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
1	1	1	B1	B0	*	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
			Blinking control			Pattern on/off					Blinking control		Pattern on/off					

Notes: 1. Data set to SEGRAM is output when COM17 is selected, as for a 1-line display, and output when COM33 is selected, as for a 2-line or a 4-line display.

2. S1 to S48 are pin numbers of the segment output driver.
   S1 is positioned to the left of the monitor.
   S37 to S48 are extension driver outputs for a 6-dot character width.
3. After S40 output at 5-dot font and S48 output at 6-dot font, S1 output is repeated again.
4. As for a 5-dot font width, lower five bits (D4 to D0) are display on.off information of each segment. For a 6-dot character width, the lower six bits (D5 to D0) are the display information for each segment.
5. When the BE bit of the function set register is 1, pattern blinking of the lower six bits is controlled using the upper two bits (bits 7 and 6) in SEGRAM.
   When bit 7 is 1, only a bit set to “1” of the lower six bits is blinked on the display.
   When bit 6 is 1, only a bit 4 pattern can be blinked as for a 5-dot font width, and only a bit 5 pattern can be blinked as for 6-dot font width.
6. Bit 5 (D5) is invalid for a 5-dot font width.
7. Set bits in the CGRAM data correspond to display selection, and zeros to non-selection.

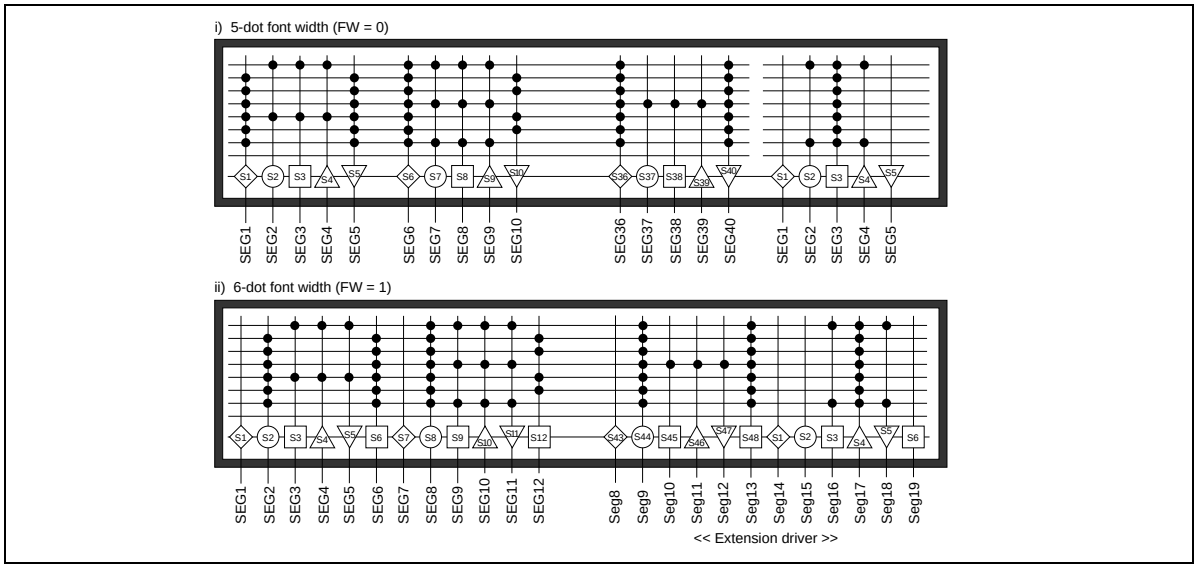


Figure 9 Relationships between SEGRAM Data and Display

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM, CGRAM, and SEGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 33 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs.

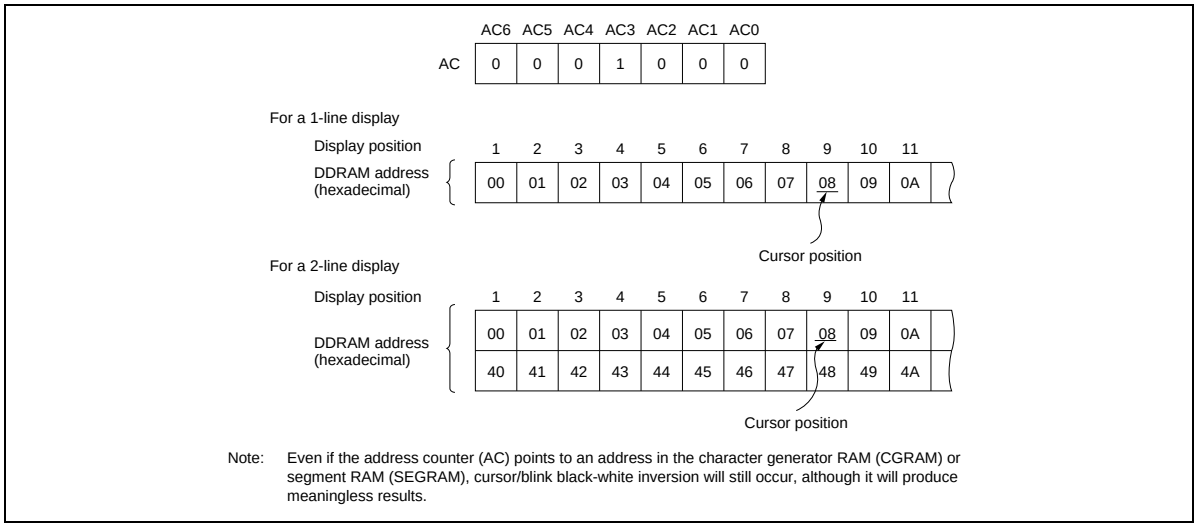
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DDRAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66710 drives from the head display.

Cursor/Blink Control Circuit

The cursor/blink (or white-black inversion) control is used to produce a cursor or a flashing area on the display at a position corresponding to the location in stored in the address counter (AC).

For example (Figure 10), when the address counter is 08H, a cursor is displayed at a position corresponding to DDRAM address 08H.



Note: Even if the address counter (AC) points to an address in the character generator RAM (CGRAM) or segment RAM (SEGRAM), cursor/blink black-white inversion will still occur, although it will produce meaningless results.

Figure 10 Cursor/Blink Display Example

Interfacing to the MPU

The HD66710 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. Bus lines DB0 to DB3 are disabled. The data transfer between the HD66710 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transfered before the four low order bits (for 8-bit operation, DB0 to DB3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.
- For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

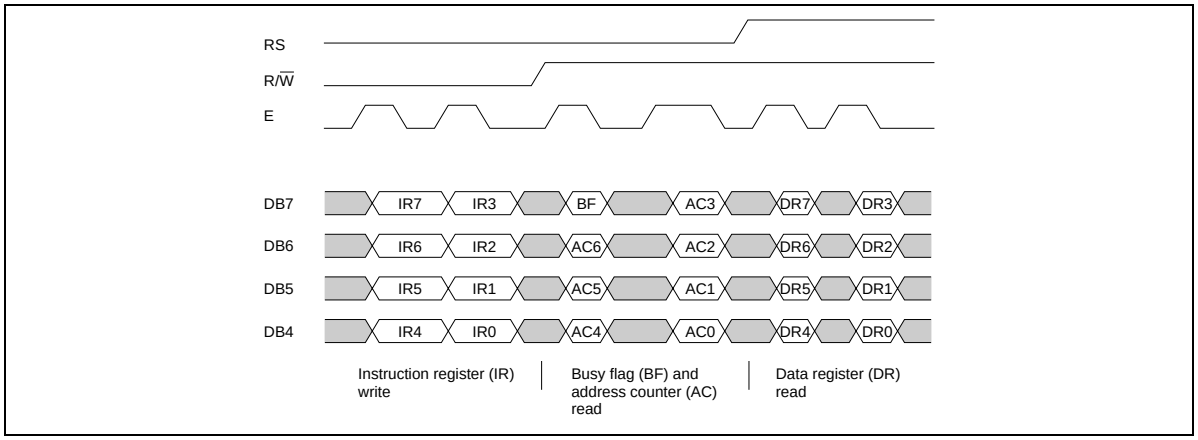


Figure 11 4-Bit Transfer Example

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66710 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 15 ms after V_{CC} rises to 4.5V or 40 ms after the V_{CC} rises to 2.7V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   RE = 0; Extension register write disable
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
   BE = 0; CGRAM/SEGRAM blinking off
   LP = 0; Not in low power mode
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift
5. Extension function set:
   FW = 0; 5-dot character width
   B/W = 0; Normal cursor (eighth line)
   NW = 0; 1- or 2-line display (depending on N)
6. SEGRAM address set:
   HDS = 000; No scroll

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66710. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66710 can be controlled by the MPU. Before starting internal operation of the HD66710, control information is temporarily stored in these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66710 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write (R/$\overline{W}$), and the data bus (DB0 to DB7), make up the HD66710 instructions (Table 7). There are four categories of instructions that:

- Designate HD66710 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66710 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (Table 7) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66710 is not in the busy state (BF = 1) before sending an instruction from the MPU to the HD66710. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Table 7 for the list of each instruction execution time.

Table 7 Instructions

Instruction	Code RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (Max) (when f_{cp} or f_{osc} is 270 kHz)
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	1.52 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control (RE = 0)	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Extension function set (RE = 1)	0	0	0	0	0	0	1	FW	B/W	NW	Sets a font width, a black-white inverting cursor (B/W), a 6-dot font width (FW), and a 4-line display (NW).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DDRAM contents.	37 µs
Function set (RE = 0)	0	0	0	0	1	DL	N	RE	—	—	Sets interface data length (DL), number of display lines (N), and extension register write enable (RE).	37 µs
(RE = 1)	0	0	0	0	1	DL	N	RE	BE	LP	Sets CGRAM/SEGRAM blinking enable (BE), and low power mode (LP). LP is available when the EXT pin is low.	37 µs
Set CGRAM address (RE = 0)	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM address. CGRAM data is sent and received after this setting.	37 µs
Set DDRAM address (RE = 0)	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM address. DDRAM data is sent and received after this setting.	37 µs
Set SEGRAM address (RE = 1)	0	0	1	HDS	HDS	HDS	*—	ASG	ASG	ASG	Sets SEGRAM address. DDRAM data is sent and received after this setting. Also sets a horizontal dot scroll quantity (HDS).	37 µs

Table 7 Instructions (cont)

Instruction	Code RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs
Write data to RAM (RE = 0/1)	1	0	Write data								Writes data into DDRAM, CGRAM, or SEGRAM. To write data to DDRAM CGRAM, clear RE to 0; or to write data to SEGRAM, set RE to 1.	37 µs t_{ADD} = 5.5 µs*
Read data from RAM (RE = 0/1)	1	1	Read data								Reads data from DDRAM, CGRAM, or SEGRAM. To read data from DDRAM or CGRAM, clear RE to 0; to read data from SEGRAM, set RE to 1.	37 µs t_{ADD} = 5.5 µs*
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift D = 1: Display on C = 1: Cursor on B = 1: Blink on FW = 1: 6-dot font width B/W = 1: Black-white inverting cursor on NW = 1: Four lines NW = 0: One or two lines S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line RE = 1: Extension register access enable BE = 1: CGRAM/SEGRAM blinking enable LP = 1: Low power mode BF = 1: Internally operating BF = 0: Instructions acceptable											DDRAM: Display data RAM CGRAM: Character generator RAM SEGRAM: Segment RAM ACG: CGRAM address ADD: DDRAM address (corresponds to cursor address) ASEG: Segment RAM address HDS: Horizontal dot scroll quantity AC: Address counter used for both DD, CG, and SEGRAM addresses.	

Notes: 1. — indicates no effect.

* After execution of the CGRAM/DDRAM/SEGRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off.

In Figure 12, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

2. Extension time changes as frequency changes. For example, when f is 300 kHz, the execution time is: 37 µs × 270/300 = 33 µs.
3. Execution time in a low power mode (LP = 1 & EXT = low) becomes four times as long as for a 1-line mode, and twice as long as for a 2- or 4-line mode.

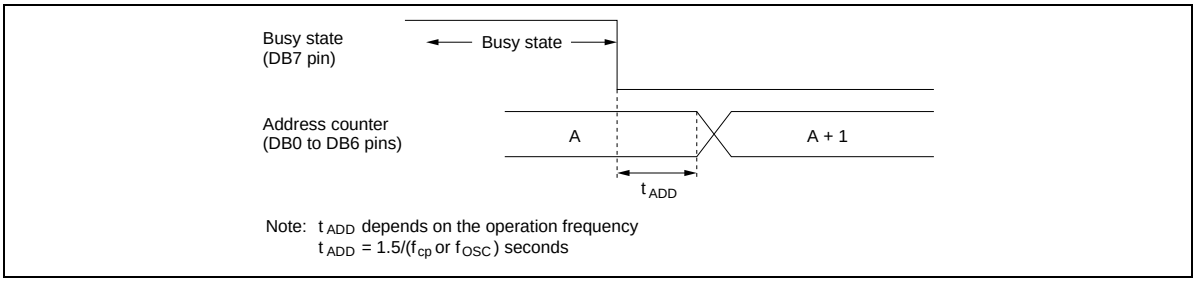


Figure 12 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code (20)H (character pattern for character code (20)H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change. It resets the extended register enable bit (RE) to 0 in function set.

Return Home

Return home sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DDRAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed). It resets the extended register enable bit (RE) to 0 in function set. In addition, flicker may occur in a moment at the time of this instruction issue.

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CGRAM and SEGRAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1 during DDRAM write. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DDRAM. Also, writing into or reading out from CGRAM and SEGRAM does not shift the display. In a low power mode (LP = 1), do not set S = 1 because the whole display does not normally shift.

Display On/Off Control

When extension register enable bit (RE) is 0, bits D, C, and B are accessed.

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DDRAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5×8 dot character font.

B: The character indicated by the cursor blinks when B is 1 (Figure 13). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 370-ms intervals when f_{cp} or f_{OSC} is 270 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 300 kHz, $370 \times 270/300 = 333$ ms.)

Extended Function Set

When the extended register enable bit (RE) is 1, FW, B/W, and NW bit shown below are accessed. Once these registers are accessed, the set values are held even if the RE bit is set to zero.

FW: When FW is 1, each displayed character is controlled with a 6-dot width. The user font in CGRAM is displayed with a 6-bit character width from bits 5 to 0. As for fonts stored in CGROM, no display area is assigned to the leftmost bit, and the font is displayed with a 5-bit character width. If the FW bit is changed, data in DDRAM and CGRAM SEGRAM is destroyed. Therefore, set FW before data is written to RAM. When font width is set to 6 dots, the frame frequency decreases to 5/6 compared to 5-dot time. See “Oscillator Circuit” for details.

B/W: When B/W is 1, the character at the cursor position is cyclically displayed with black-white invertion. At this time, bits C and B in display on/off control register are “Don’t care”. When f_{CP} or f_{OSC} is 270 kHz, display is changed by switching every 370 ms.

NW: When NW is 1, 4-line display is performed. At this time, bit N in the function set register is “Don’t care”.

Note: After changing the N or NW or LP bit, please issue the return home or clear display instructions to cancel to shift display.

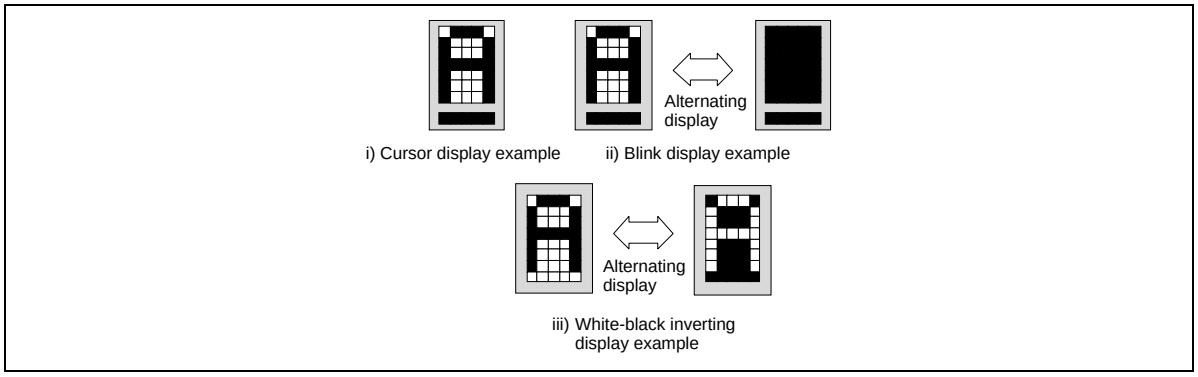


Figure 13 Cursor Blink Width Control

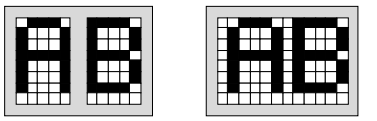


Figure 14 Character Width Control

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (Table 8). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. In a 4-line display, the cursor moves to the second line when it passes the 20th character of the line. Note that, all line displays will shift at the same time. When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

These instruction reset the extended register enable bit (RE) to 0 in function set.

The address counter (AC) contents will not change if the only action performed is a display shift.

In low power mode (LP = 1), whole-display shift cannot be normally performed.

Function Set

Only when the extended register enable bit (RE) is 1, the BE bit shown below can be accessed. Bits DL and N can be accessed regardless of RE.

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB7 to DB0) when DL is 1, and in 4-bit lengths (DB7 to DB4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

Table 8 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

N: When bit NW in the extended function set is 0, a 1- or a 2-line display is set. When N is 0, 1-line display is selected; when N is 1, 2-line display is selected. When NW is 1, a 4-line display is set. At this time, N is “Don’t care”.

RE: When the RE bit is 1, bit BE and LP in the extended function set registe, the SEGRAM address set register, and the extended function set register can be accessed. When bit RE is 0, the registers described above cannot be accessed, and the data in these registers is held.

To maintain compatibility with the HD44780, the RE bit should be fixed to 0.

Clear display, return home and cursor or display shift instruction a reset the RE bit to 0.

BE: When the RE bit is 1, this bit can be rewritten. When this bit is 1, the user font in CGRAM and the segment in SEGRAM can be blinked according to the upper two bits of CGRAM and SEGRAM.

LP: When the RE bit is 1, this bit can be rewritten. When LP is set to 1 and the EXT pin is low (without an extended driver), the HD66710 operates in low power mode. In 1-line display mode, the HD66710 operates on a 4-division clock, and in a 2-line or a 4-line display mode, the HD66710 operates on a 2-division clock. According to these operations, instruction execution takes four times or twice as long. Notice that in a low power mode, display shift cannot be performed.

Note: Perform the DL, N, NW, FW functions at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, if bit N, NW, or FW is changed after other instructions are executed, RAM contents may be lost.

After changing the N or NW or LP bit, please issue the return home or clear display instruction cancel to shift display.

Set CGRAM Address

A CGRAM address can be set while the RE bit is cleared to 0. Set CGRAM address sets the CGRAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CGRAM.

Table 9 Display Line Set

N	NW	No. of Display Lines	Character Font	Duty Factor	Maximum Number of Characters/1 Line with Extended Drivers
0	0	1	5 × 8 dots	1/17	50 characters
1	0	2	5 × 8 dots	1/33	30 characters
*	1	4	5 × 8 dots	1/33	20 characters

Note: * Indicates don’t care.

Set DDRAM Address

Set DDRAM address sets the DDRAM address binary AAAAAAA into the address counter while the RE bit is cleared to 0.

Data is then written to or read from the MPU for DDRAM.

However, when N and NW is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 and NW is 0 (2-line display), AAAAAAA is (00)H to (27)H for the first line, and (40)H to (67)H for the second line. When NW is 1 (4-line display), AAAAAAA is (00)H to (13)H for the first line, (20)H to (33)H for the second line, (40)H to (53)H for the third line, and (60)H to (73)H for the fourth line.

Set SEGRAM Address

Only when the extended register enable bit (RE) is 1, HS2 to HS0 and the SEGRAM address can be set.

The SEGRAM address in the binary form AAA is set to the address counter. SEGRAM can then be written to or read from by the MPU.

Note: When performing a horizontal scroll is described above by connecting an extended driver, the maximum number of characters per line decreases by one. In other words, 49 characters, 29 characters, and 19 characters are displayed in 1-line, 2-line, and 4-line modes, respectively. Notice that in low power mode (LP = 1), the display shift and scroll cannot be performed.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by all CG, DD, and SEGRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for CGRAM, DDRAM, and SEGRAM address set instructions.

Table 10 HS2 to HS0 Settings

HS2	HS1	HS0	Description
0	0	0	No shift.
0	0	1	Shift the display position to the left by one dot.
0	1	0	Shift the display position to the left by two dots.
0	1	1	Shift the display position to the left by three dots.
1	0	0	Shift the display position to the left by four dots.
1	0	1	Shift the display position to the left by five dots.
1	1	0 or 1	No shift.

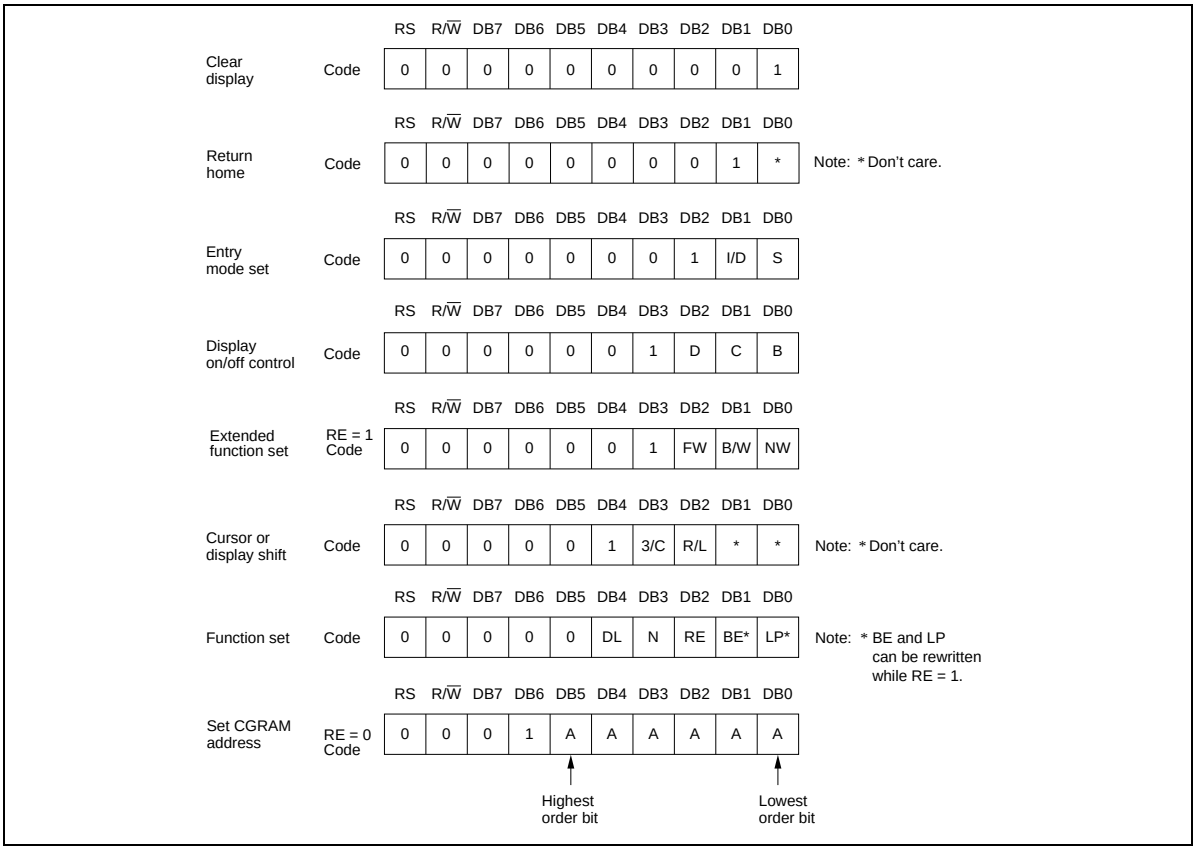


Figure 15 Character Width Control

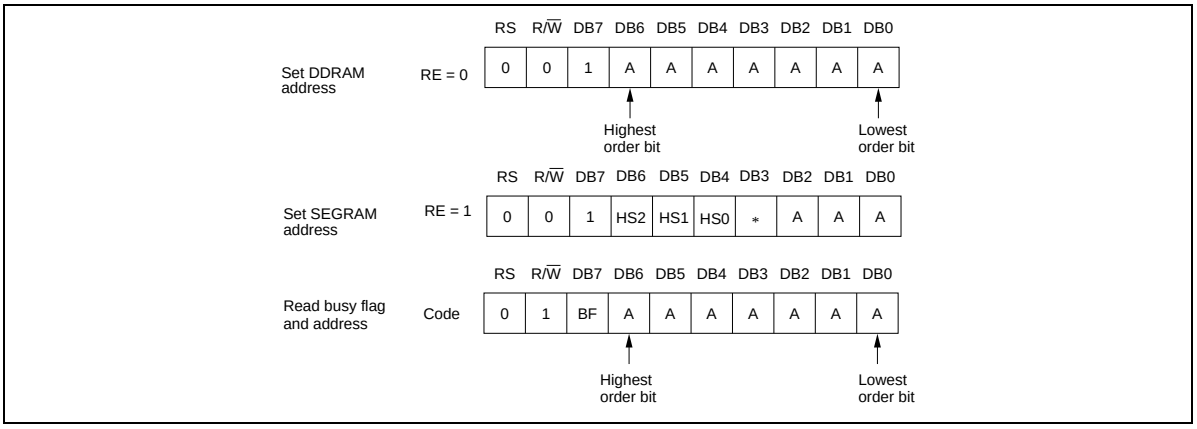


Figure 15 Character Width Control (cont)

Write Data to CG, DD, or SEGRAM

This instruction writes 8-bit binary data DDDDDDDD to CG, DD or SEGRAM. If the RE bit is cleared, CG or DDRAM is selected, as determined by the previous specification of the address set instruction; if the RE bit is set, SEGRAM is selected. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift direction.

Read Data from CG, DD, or SEGRAM

This instruction reads 8-bit binary data DDDDDDDD from CG, DD, or SEGRAM. If the RE bit is cleared, CG or DDRAM is selected, as determined by the previous specification of the address set instruction; if the RE bit is set, SEGRAM is selected. If no address is specified, the first data read will be invalid. When executing serial read instructions, the next address is normally read from the next address. An address set instruction need not be executed just before this read instruction when shifting the cursor by a cursor shift instruction (when reading from DDRAM). A cursor shift instruction is the same as a set DDRAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, a display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented after write instructions to CG, DD or SEGRAM. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to read data correctly, execute either an address set instruction or a cursor shift instruction (only with DDRAM), or alternatively, execute a preliminary read instruction to ensure the address is correctly set up before accessing the data.

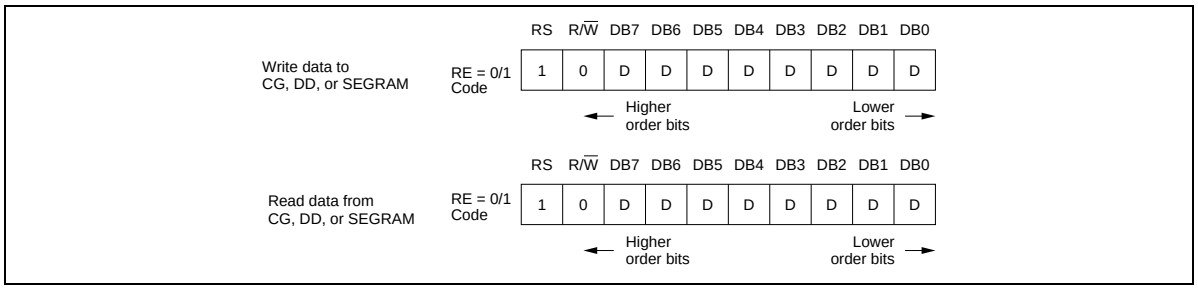


Figure 15 Character Width Control (cont)

Interfacing the HD66710

1) Interface to 8-Bit MPUs

HD66710 can interface to 8-bit MPU directly with E clock, or to 8-bit MCU through I/O port. When number of I/O port in MCU, or interfacing bus width, 4-bit interface function is useful.

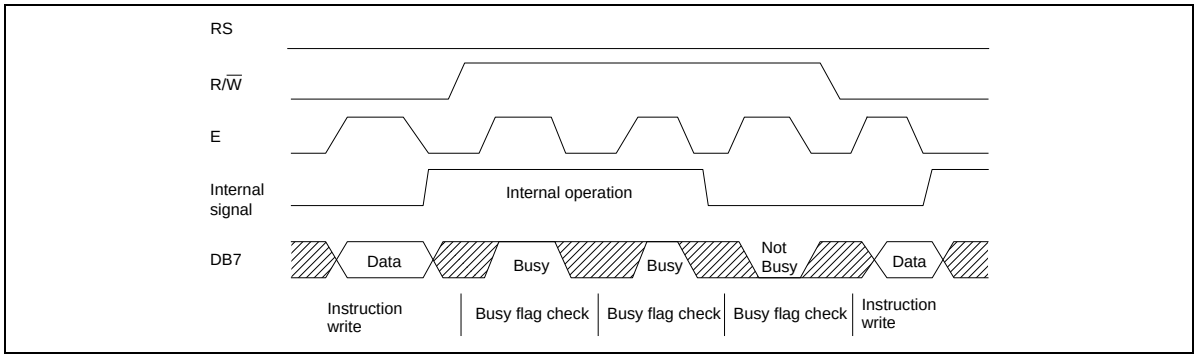


Figure 16 Example of 8-Bit Data Transfer Timing Sequence

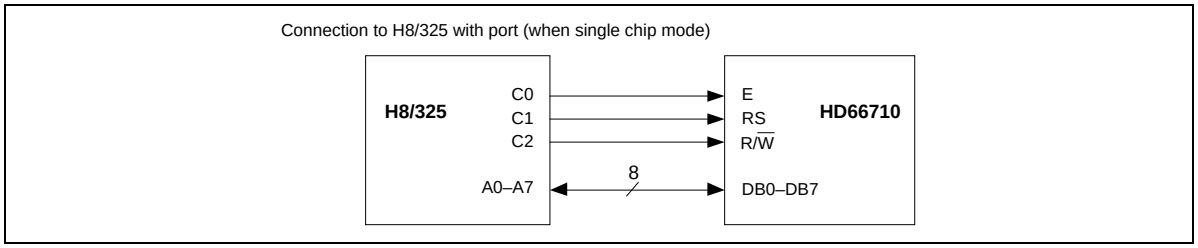


Figure 17 8-Bit MPU Interface

2) Interface to 4-Bit MPUs

HD66710 can interface to 4-bit MCU through I/O port. 4-bit data for high and low order must be transferred twice continuously. The DL bit in function set selects the interface data length.

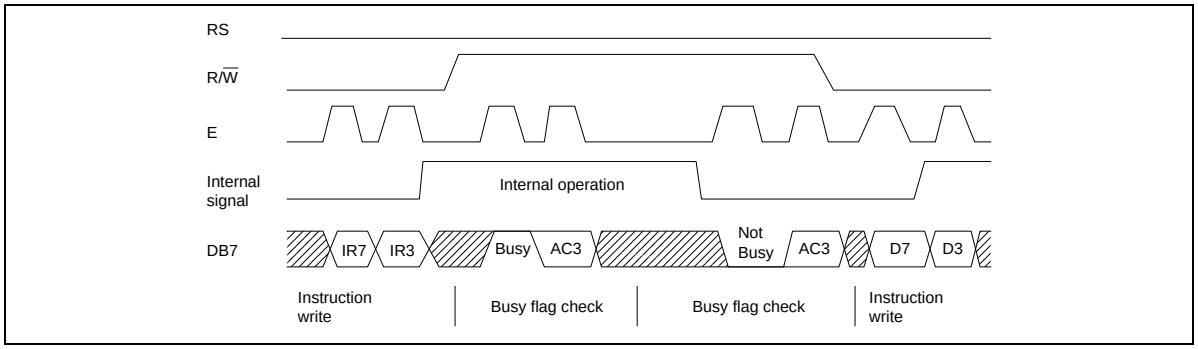


Figure 18 Example of 4-Bit Data Transfer Timing Sequence

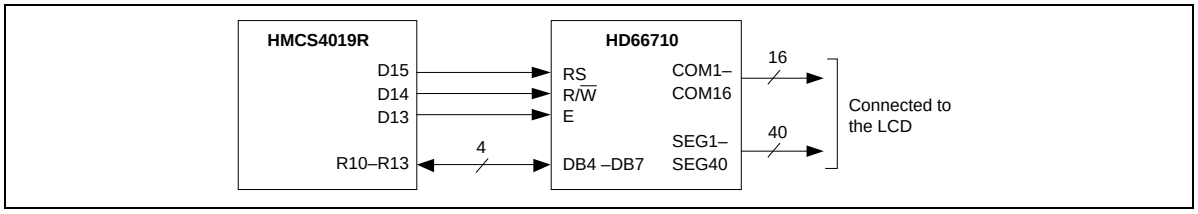


Figure 19 Interface to HMCS4019R

Oscillator Circuit

- Relationship between Oscillation frequency and Liquid Crystal Display Frame Frequency
  The liquid crystal display frame frequencies of Figure 21 apply only when the oscillation frequency is 270 kHz (one clock period: 3.7 µs).

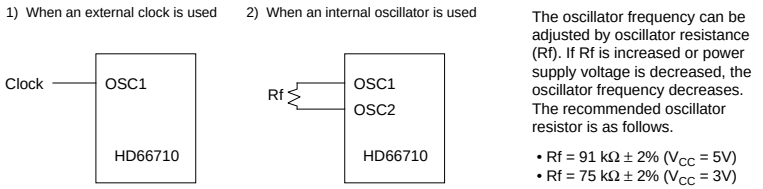
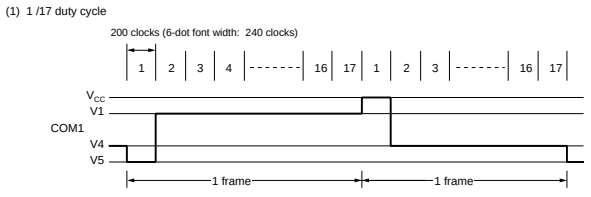
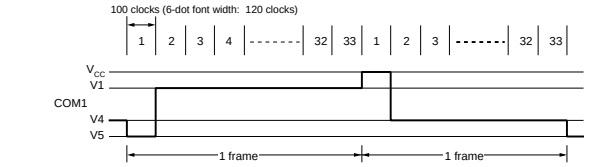


Figure 20 Oscillator Circuit



	Normal Display Mode (LP = 0)		Low Power Mode (LP = 1)	
Item	**5-Dot Font Width**	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
Line selection period	200 clocks	240 clocks	50 clocks	60 clocks
Frame frequency	79.4 Hz	66.2 Hz	79.4 Hz	66.2 Hz

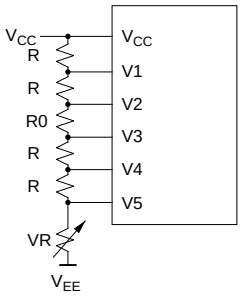


	Normal Display Mode (LP = 0)		Low Power Mode (LP = 1)	
Item	**5-Dot Font Width**	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
Line selection period	100 clocks	120 clocks	50 clocks	60 clocks
Frame frequency	81.8 Hz	68.2 Hz	81.8 Hz	68.2 Hz

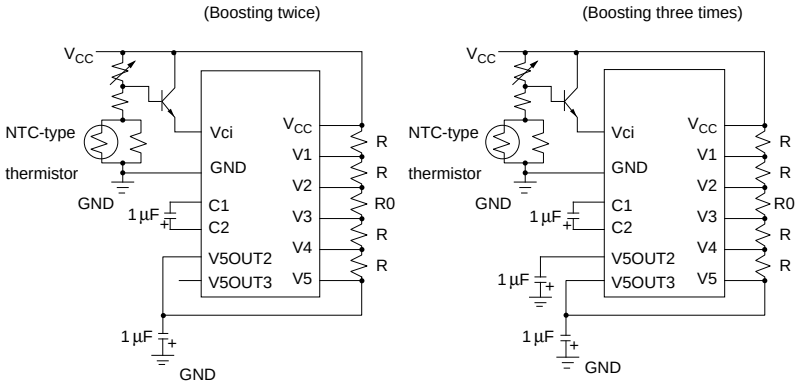
Figure 21 Frame Frequency

Power Supply for Liquid Crystal Display Drive

1) When an external power supply is used



2) When an internal booster is used



Notes: 1. Boosting output voltage should not exceed the power supply voltage (2) (13V max.) in the absolute maximum ratings. Especially, voltage of over 4.3V should not be input to the reference voltage (Vci) when boosting three times.

2. Vci input terminal is used for reference voltage and power supply for the internal booster. Input current into the Vci pin needs three times or more of load current through the bleeder resistor for LCD. So, when it adjusts LCD driving voltage (Vlcd), input voltage should be controlled with transistor to supply LCD load current.

3. Please notice connection (+/–) when it uses capacitors with poler.

Table 11 Duty Factor and Power Supply for Liquid Crystal Display Drive

Item		Data	
Number of Lines		1	2/4
Duty factor		1/17	1/33
Bias		1/5	1/6.7
Divided resistance	R	R	R
	R0	R	2.7R

Note: R changes depending on the size of liquid crystal penel. Normally, R must be 4.7 kΩ to 20 kΩ.

Extension Driver LSI Interface

By bringing the EXT pin high, segment driver pins (SEG37 to SEG40) functions as the extended driver interface outputs. From these pins, a latch pulse (CL1), a shift clock (CL2), data (D), and an AC signal (M) are output. The same data is output from the SEG36 pin of the HD66710 and the start segment pin (Seg1) of the extension driver. Due to the character baundary, the Seg1 output is used for the 5-dot font width. For the 6-dot font width, the SEG36 output is used, and the Seg1 output of the extension driver must not be used. When the extension driver LSI interface is used, ground level (GND) must be higher than the V5 level.

Table 12 Required Number of 40-Output Extension Driver

Controller	HD66710*		HD44780	HD66702
Display Line	**5-Dot Width**	**6-Dot Width**	**5-Dot Width**	**5-Dot Width**
16 × 2 lines	Not required	1	1	Not required
20 × 2 lines	1	1	2	Not required
24 × 2 lines	1	2	2	1
40 × 2 lines	Disabled	Disabled	4	3
12 × 4 lines	1	1	Disabled	Disabled
16 × 4 lines	2	2	Disabled	Disabled
20 × 4 lines	2	3	Disabled	Disabled

Note: * The number of display lines can be extended to 30 × 2 lines or 20 × 4 lines.

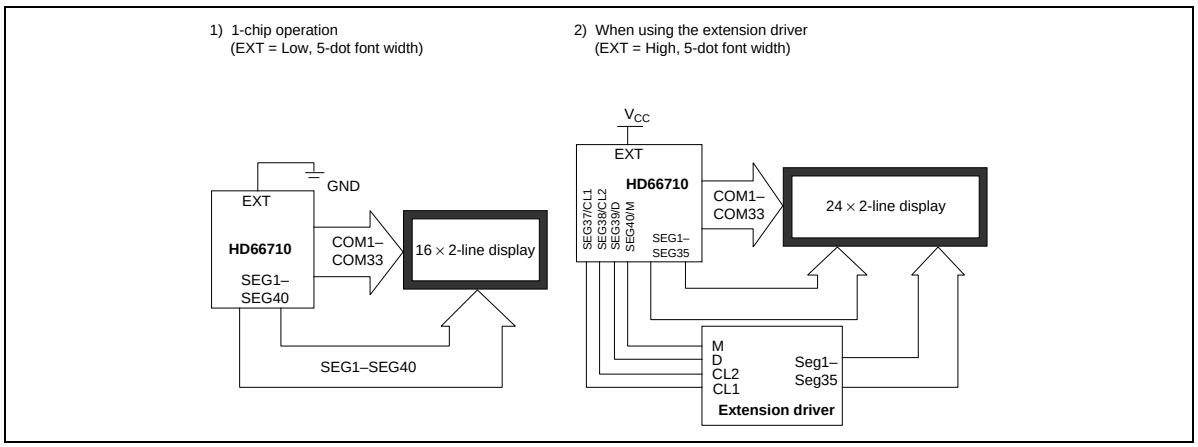


Figure 22 HD66710 and the Extension Driver Connection

When using one HD66710, the start address of COM9–COM16/COM25–COM33 is calculated by adding 8 to the start address of COM9–COM16 COM25–COM32. When extending the address, the start address is calculated by adding A(10) to COM9–COM16/COM25 to COM32. The relationship betweenmodes and display start addresses is shown below.

Table 13 Display Start Address in Each Mode

	Number of Lines				
	1-Line Mode		2-Line Mode		4-Line Mode
Output	**EXT Low**	**EXT High**	**EXT Low**	**EXT High**	**EXT Low/High**
COM1–COM8	D00±1	D00±1	D00±1	D00±1	D00±1
COM9–COM16	D08±1	D0A±1	D08±1	D0A±1	D20±1
COM17–COM24	—	—	D40±1	D40±1	D40±1
COM25–COM32	—	—	D48±1	D4A±1	D60±1
COM17	S00	S00	—	—	—
COM33	—	—	S00	S00	S00

Notes: 1. When an EXT pin is low, the extension driver is not used; otherwise, the extension driver is used.
2. D— is the start address of display data RAM (DDRAM) for each display line.
3. S— is the start address of segment RAM (SEGRAM).
4. ±1 following D— indicates increment or decrement at display shift.

Interface to Liquid Crystal Display

- Example of 5-dot font width connection

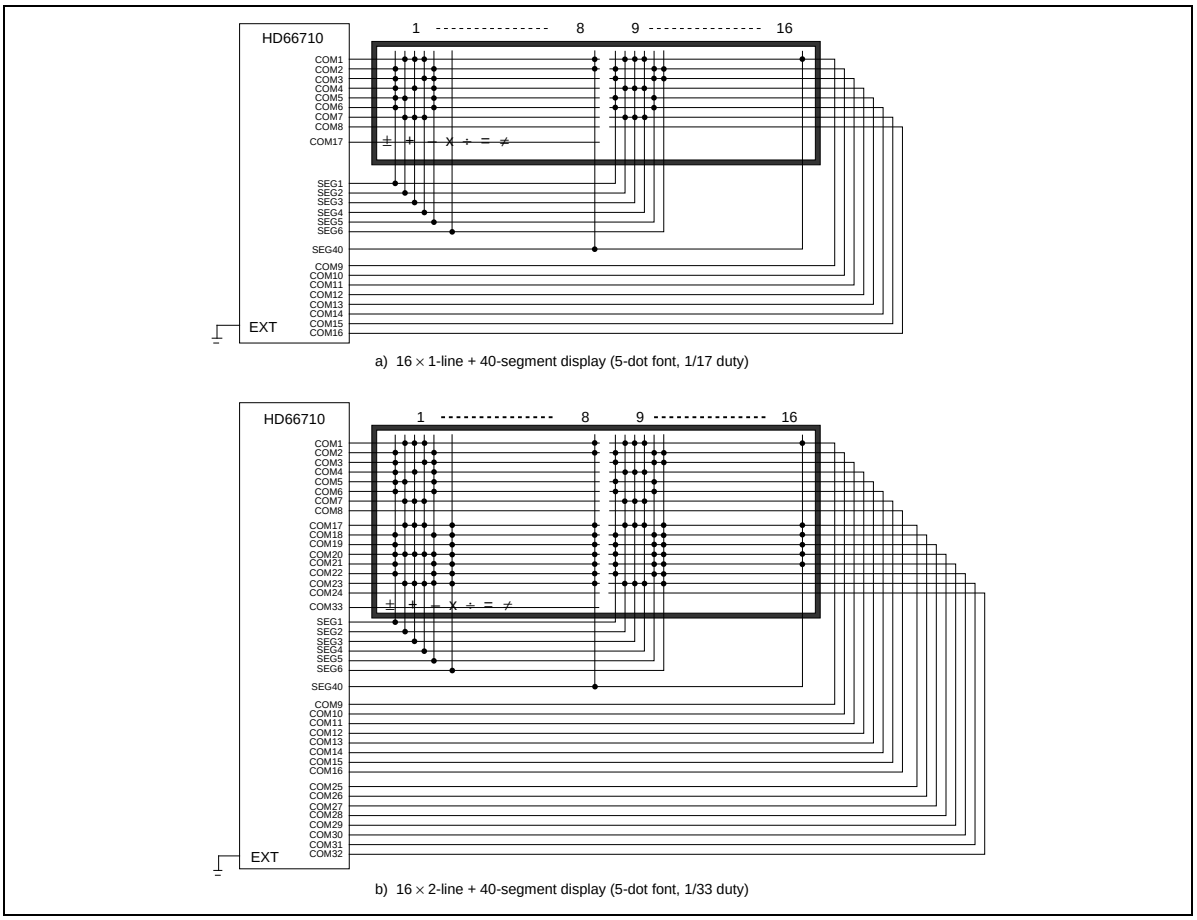


Figure 23 Liquid Crystal Display and HD66710 Connections (Single-Chip Operation)

- Example of 6-dot font width connection

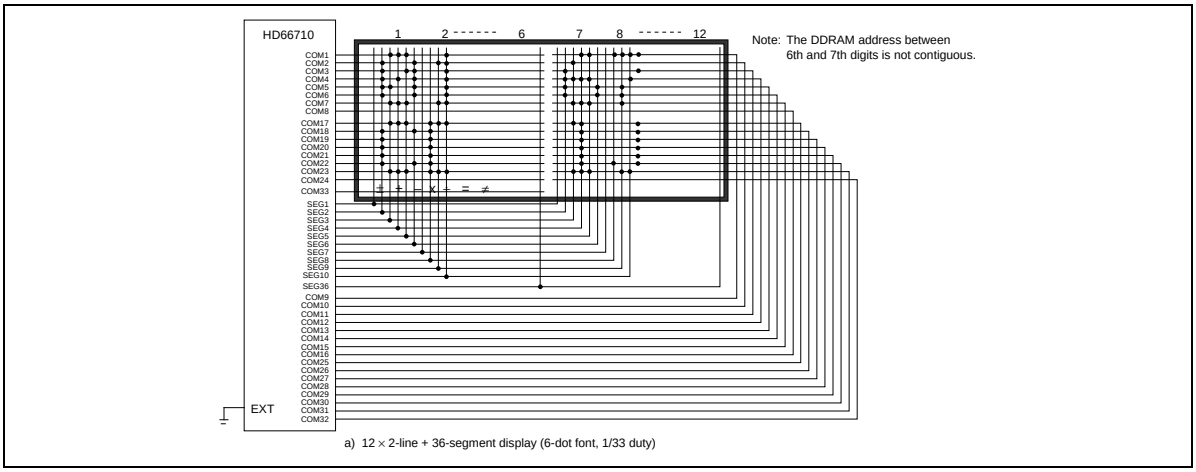


Figure 24 Liquid Crystal Display and HD66710 Connections (6-Dot Font Width)

Instruction and Display Correspondence

- 8-bit operation, 16-digit × 1-line display with internal reset

  Refer to Table 14 for an example of an 16-digit × 1-line display in 8-bit operation. The HD66710 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, a character unit scroll can be performed by a display shift instruction. A dot unit smooth scroll can also be performed by a horizontal scroll instruction. Since data of display RAM (DDRAM) is not changed by a display shift instruction, the display can be returned to the first set display when the return home operation is performed.
- 4-bit operation, 16-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (Table 15). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB0 to DB3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see Table 15). Thus, DB4 to DB7 of the function set instruction is written twice.
- 8-bit operation, 16-digit × 2-line display with internal reset

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 16 characters in the first line, the DDRAM address must be again set after the 16th character is completed (See Table 16).

  The display shift is performed for the first and second lines. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.
- 8-bit operation, 8-digit × 4-line display with internal reset

  The RE bit must be set by the function set instruction and then the NW bit must be set by an extension function set instruction. In this case, 4-line display is always performed regardless of the N bit setting (Table 17).

  In a 4-line display, the cursor automatically moves from the first to the second line after the 20th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set again after the 8th character is completed. Display shifts are performed on all lines simultaneously.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD66710 must be initialized by instructions. See the section, Initializing by Instruction.

Table 14 8-Bit Operation, 16-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 1-line display. Bit 2 must always be cleared.
	0	0	0	0	1	1	0	0	*	*		
3	Display on/off control											Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0	_	
4	Entry mode set											Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0	_	
5	Write data to CGRAM/DDRAM											Writes H. DDRAM has already been selected by initialization when the power was turned on.
	1	0	0	1	0	0	1	0	0	0	H_	
6	Write data to CGRAM/DDRAM											Writes I.
	1	0	0	1	0	0	1	0	0	1	HI_	
7						. . . . .					. . . . .	
8	Write data to CGRAM/DDRAM											Writes I.
	1	0	0	1	0	0	1	0	0	1	HITACHI_	
9	Entry mode set											Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1	HITACHI_	
10	Write data to CGRAM/DDRAM											Writes a space.
	1	0	0	0	1	0	0	0	0	0	ITACHI _	

Table 14 8-Bit Operation, 16-Digit × 1-Line Display Example with Internal Reset (cont)

Step	Instruction											
No.	RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
11	Write data to CGRAM/DDRAM										TACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
12						. . . . .					. . . . .	
13	Write data to CGRAM/DDRAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CGRAM/DDRAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CGRAM/DDRAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20						. . . . .					. . . . .	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 15 4-Bit Operation, 16-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 4-bit operation. Clear bit 2. In this case, operation is handled as 8 bits by initialization. *
	0	0	0	0	1	0	—	—	—	—		
	—	—	—	—	—	—	—	—	—	—		
3	Function set											Sets 4-bit operation and selects1-line display. Clear BE, LP bits. 4-bit operation starts from this step.
	0	0	0	0	1	0	—	—	—	—		
	0	0	0	1	0	0	—	—	—	—		
4	Function set											Sets 4-bit operation and selects1-line display. Clear RE bit.
	0	0	0	0	1	0	—	—	—	—		
	0	0	0	0	*	*	—	—	—	—		
5	Return home											Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	—	—	—	—		
	0	0	0	0	1	0	—	—	—	—		
6	Display on/off control											Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	—	—	—	—	_	
	0	0	1	1	1	0	—	—	—	—		
7	Entry mode set											Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
	0	0	0	0	0	0	—	—	—	—	_	
	0	0	0	1	1	0	—	—	—	—		
8	Write data to CGRAM/DDRAM											Writes H. DDRAM has already been selected by initialization.
	1	0	0	1	0	0	—	—	—	—	H_	
	1	0	1	0	0	0	—	—	—	—		

Note: 1. The control is the same as for 8-bit operation beyond step #8.
2. When DB3 to DB0 pins are open in 4-bit mode, the RE, BE, LP bits are set to “1” at step #2. So, these bits are clear to “0” at step #3.

Table 16 8-Bit Operation, 16-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	0	1	1	1	0	*	*	Sets to 8-bit operation and selects 1-line display. Clear bit 2.
3	Display on/off control	0	0	0	0	0	0	1	1	1	0	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry mode set	0	0	0	0	0	0	0	1	1	0	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
5	Write data to CGRAM/DDRAM	1	0	0	1	0	0	1	0	0	0	Writes H. DDRAM has already been selected by initialization when the power was turned on.
6	. . . . .					. . . . .					. . . . .	
7	Write data to CGRAM/DDRAM	1	0	0	1	0	0	1	0	0	1	Writes I.
8	Set DDRAM address	0	0	1	1	0	0	0	0	0	0	Sets RAM address so that the cursor is positioned at the head of the second line.

Table 16 8-Bit Operation, 16-Digit × 2-Line Display Example with Internal Reset (cont)

Step	Instruction											
No.	RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
9	Write data to CGRAM/DDRAM										HITACHI M_	Writes a space.
	1	0	0	1	0	0	1	1	0	1		
10						.					.	
						.					.	
						.					.	
						.					.	
						.					.	
11	Write data to CGRAM/DDRAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
12	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
13	Write data to CGRAM/DDRAM										ITACHI ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
14						.					.	
						.					.	
						.					.	
						.					.	
						.					.	
15	Return home										HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 17 8-Bit Operation, 8-Digit × 4-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8 bit operation and the extended register enable bit.
	0	0	0	0	1	1	0	1	*	*		
3	4-line mode set											Sets 4-line display.
	0	0	0	0	0	0	1	0	0	1		
4	Function set Clear extended register enable bit											Clears the extended register enable bit. Setting the N bit is “don’t care”.
	0	0	0	0	1	1	0	0	*	*		
5	Display on/off control											Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0	_	
6	Entry mode set											Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0	_	
7	Write data to CGRAM/DDRAM											Writes H. DDRAM has already been selected by initialization when the power was turned on.
	1	0	0	1	0	0	1	0	0	0	H_	
8	—											

Table 17 8-Bit Operation, 8-Digit × 4-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
9	Write data to CGRAM/DDRAM 1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
10	Set DDRAM address 0	0	1	0	1	0	0	0	0	0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the second line.
11	Write data to CGRAM/DDRAM 1	0	0	0	1	1	0	0	0	0	HITACHI 0_	Writes 0.

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

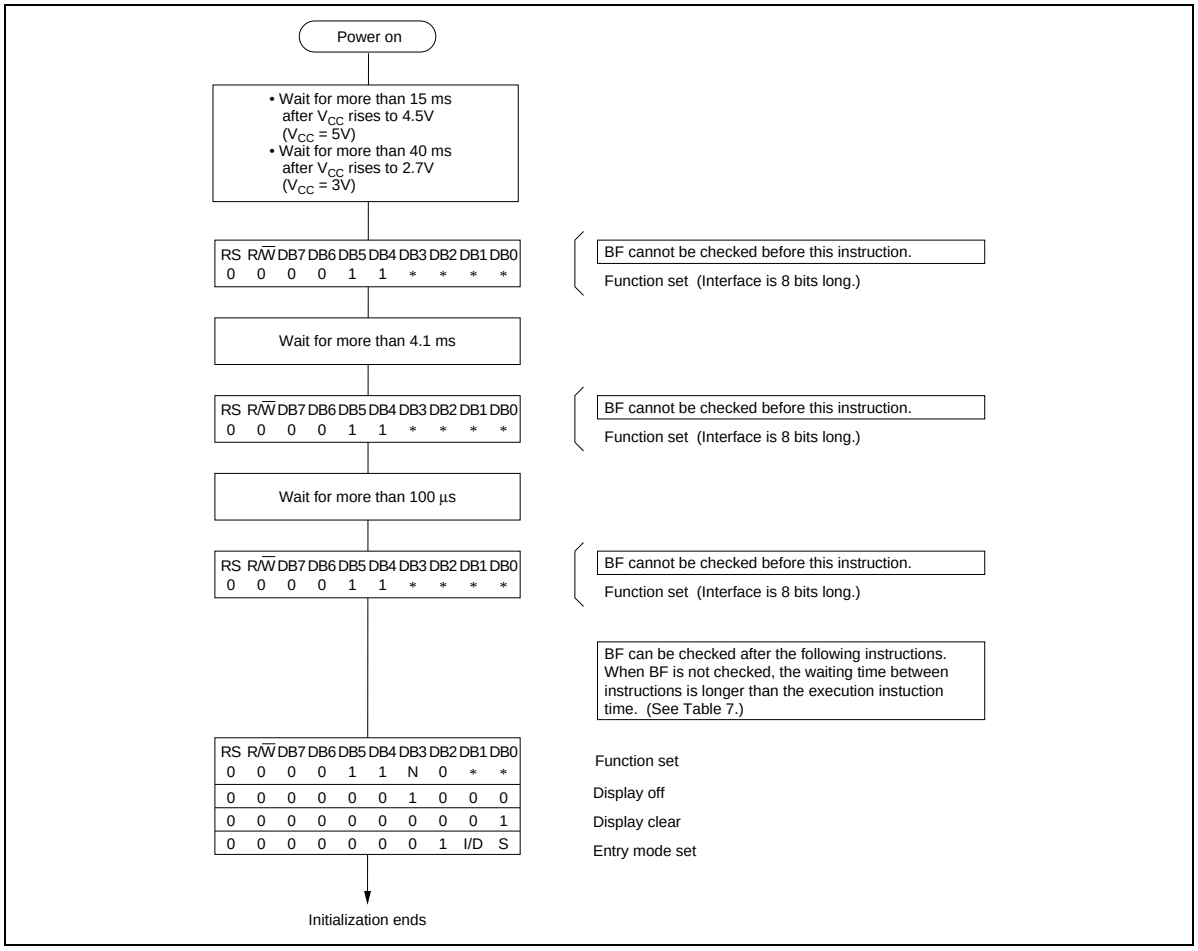


Figure 25 8-Bit Interface

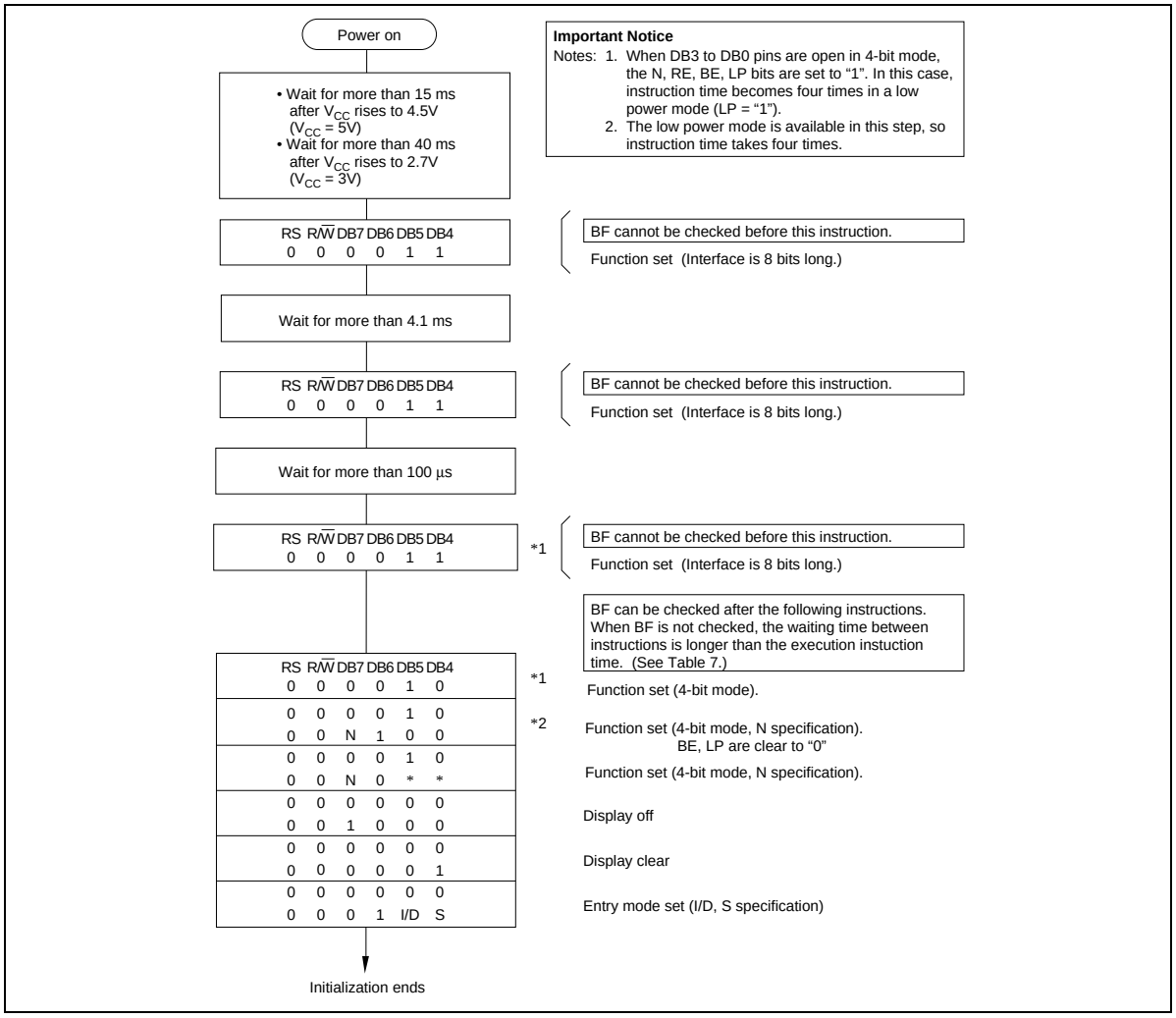


Figure 26 4-Bit Interface

Horizontal Dot Scroll

Dot unit shifts are performed by setting the horizontal dot scroll bit (HDS) when the extension register is enabled (RE = 1). By combining this with character unit display shift instructions, smooth horizontal scrolling can be performed on a 6-dot font width display as shown below.

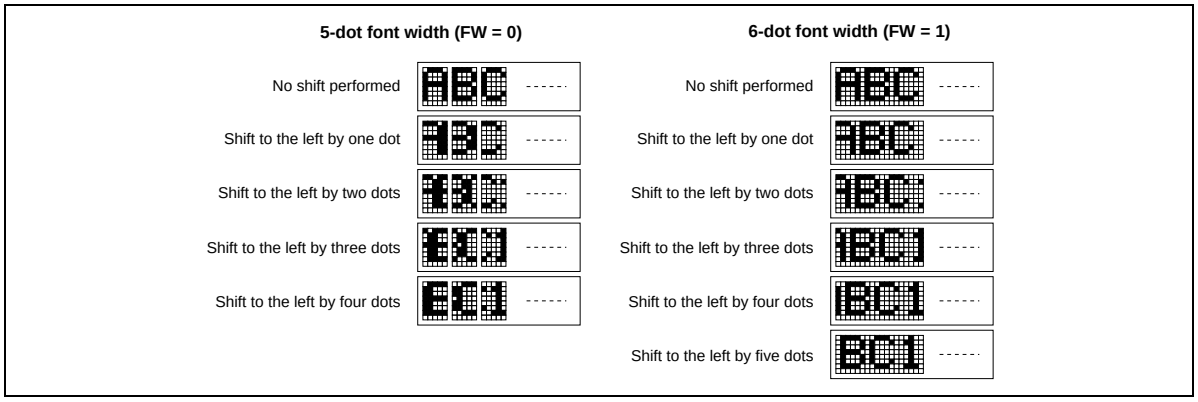


Figure 27 Shift in 5- and 6-Dot Font Width

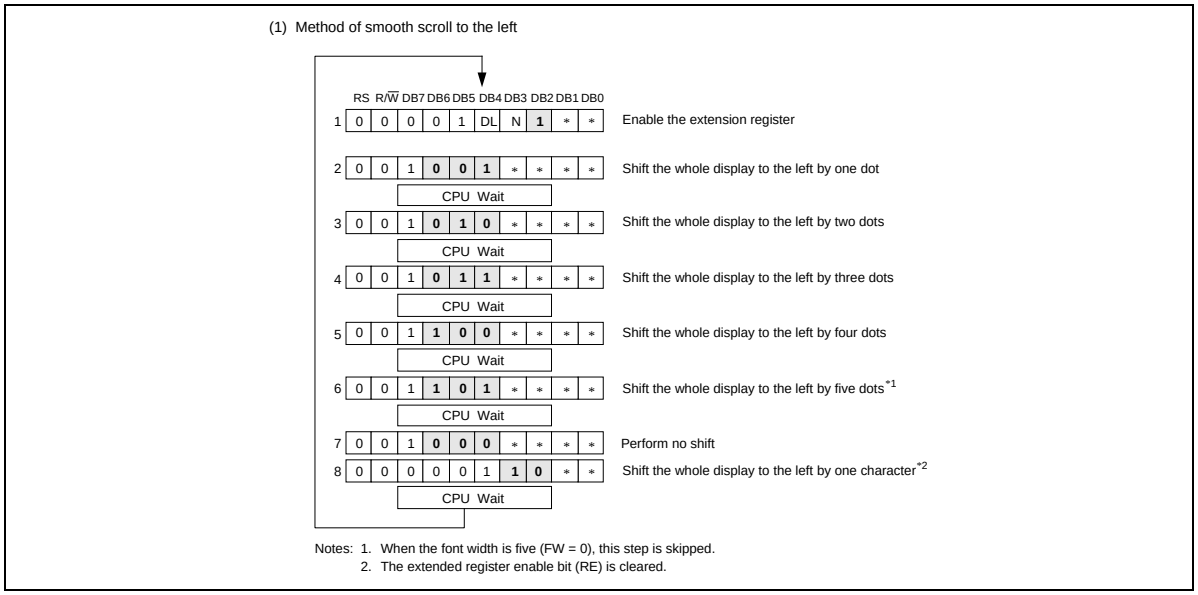


Figure 28 Smooth Scroll to the Left

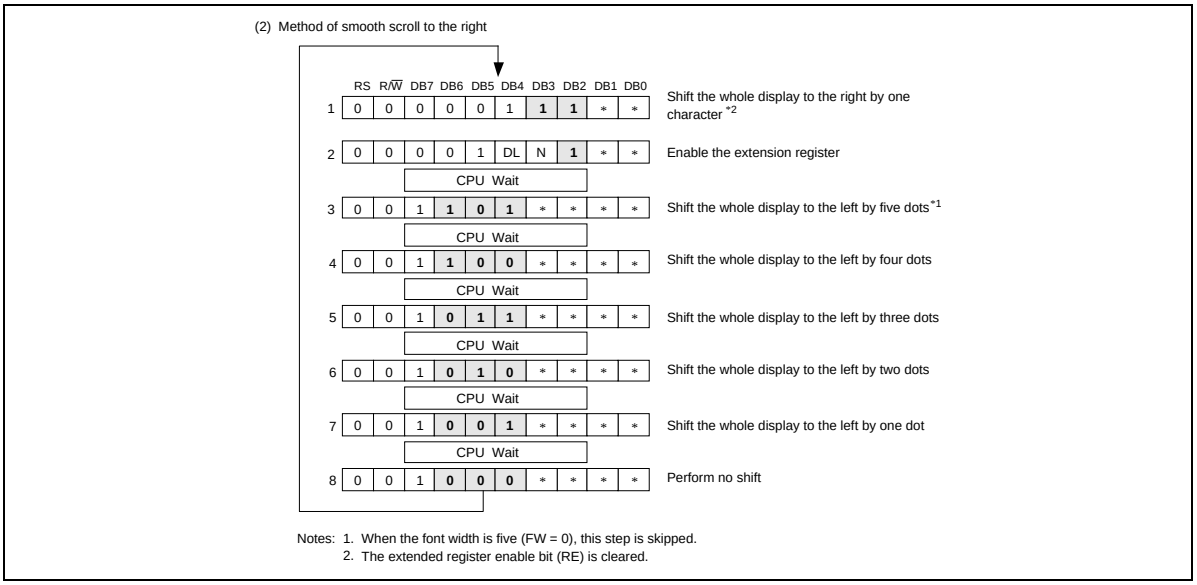


Figure 28 Smooth Scroll to the Left (cont)

Low Power Mode

When LP bit is 1 and the EXT pin is low (without an extended driver), the HD66710 operates in low power mode. In 1-line display mode, the HD66710 operates on a 4-division clock, and in 2-line or 4-line display mode, it operates on 2-division clock. So, instruction execution takes four times or twice as long. Notice that in this mode, display shift and scroll cannot be performed. Clear display shift with the return home instruction, and the horizontal scroll quantity.

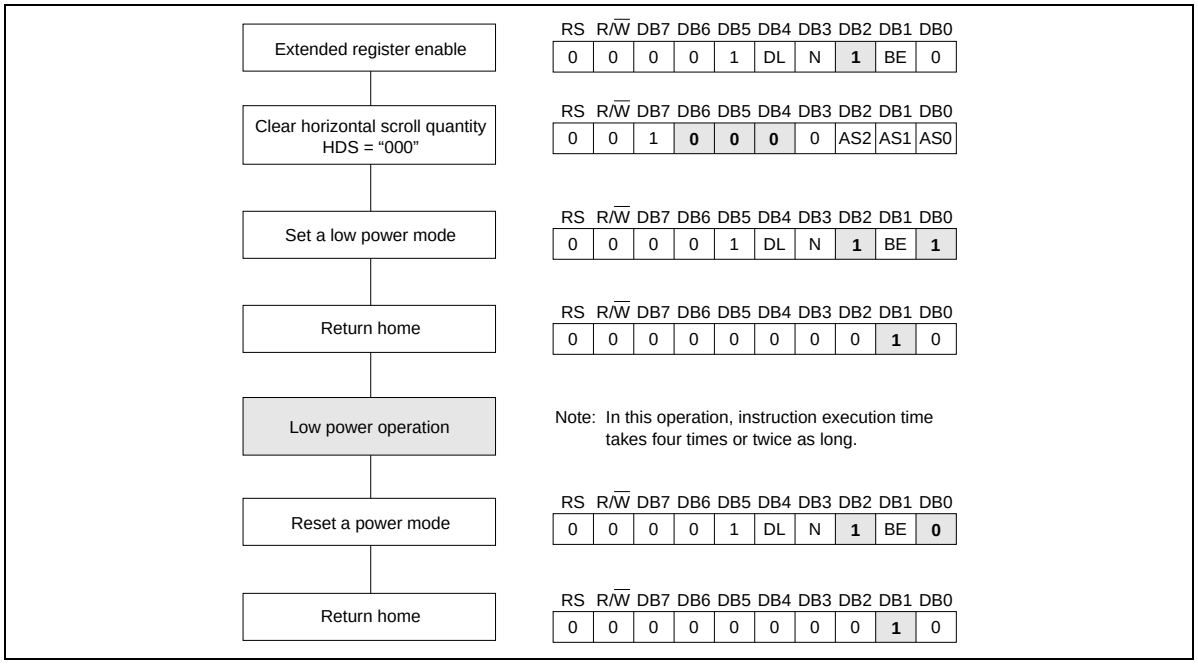


Figure 29 Low Power Mode Operation

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes*
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V5	–0.3 to +15.0	V	1, 2
Input voltage	Vt	–0.3 to V_{CC} +0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	4

Notes: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

* Refer to the Electrical Characteristics Notes section following these tables.

DC Characteristics (V_{CC} = 2.7V to 5.5V, T_a = –20°C to +75°C*[3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC1)	VIH1	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage (1) (except OSC1)	VIL1	–0.3	—	$0.2V_{CC}$	V		6
		–0.3	—	0.6			
Input high voltage (2) (OSC1)	VIH2	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC1)	VIL2	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (D0–D7)	VOH1	$0.75V_{CC}$	—	—	V	$–I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D0–D7)	VOL1	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D0–D7)	VOH2	$0.8V_{CC}$	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D0–D7)	VOL2	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	2	20	kΩ	±Id = 0.05 mA (COM) VLCD = 4V	13
Driver on resistance (SEG)	R_{SEG}	—	2	30	kΩ	±Id = 0.05 mA (SEG) VLCD = 4V	13
I/O leakage current	I_{LI}	–1	—	1	µA	VIN = 0 to V_{CC}	9
Pull-up MOS current (D0–D7, RS, R/$\overline{W}$)	–Ip	5	50	120	µA	V_{CC} = 3V VIN = 0V	
Power supply current	I_{CC}	—	150	300	µA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
	I_{LP1}	—	80	—	µA	LP mode, 1/17 duty V_{CC} = 3V, f_{OSC} = 270 kHz	
	I_{LP2}	—	100	—	µA	LP mode, 1/33 duty V_{CC} = 3V, f_{OSC} = 270 kHz	
LCD voltage	VLCD1	3.0	—	13.0	V	V_{CC}–V5, 1/5 bias	16
	VLCD2	3.0	—	13.0	V	V_{CC}–V5, 1/6.7 bias	

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	VUP2	7.5	8.7	—	V	Vci = 4.5V, I0 = 0.25 mA, C = 1 µF, f_{OSC} = 270 kHz, T_a = 25°C	18, 19
Output voltage(V5OUT3 pin)	VUP3	7.0	7.7	—	V	Vci = 2.7V, I0 = 0.25 mA, C = 1 µF, f_{OSC} = 270 kHz, T_a = 25°C	18, 19
Input voltage	VCi	1.0	—	5.0	V		18, 19, 20

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.7V to 5.5V, T_a = –20°C to +75°C*[3])

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	350	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 91 kΩ, V_{CC} = 5V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics (1) (V_{CC} = 2.7V to 4.5V, T_a = –20°C to +75°C*[3])

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 30
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 31
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Bus Timing Characteristics (2) (V_{CC} = 4.5V to 5.5V, T_a = –20°C to +75°C*[3])

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 30
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 31
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Segment Extension Signal Timing (V_{CC} = 2.7V to 5.5V, T_a = –20°C to +75°C*[3])

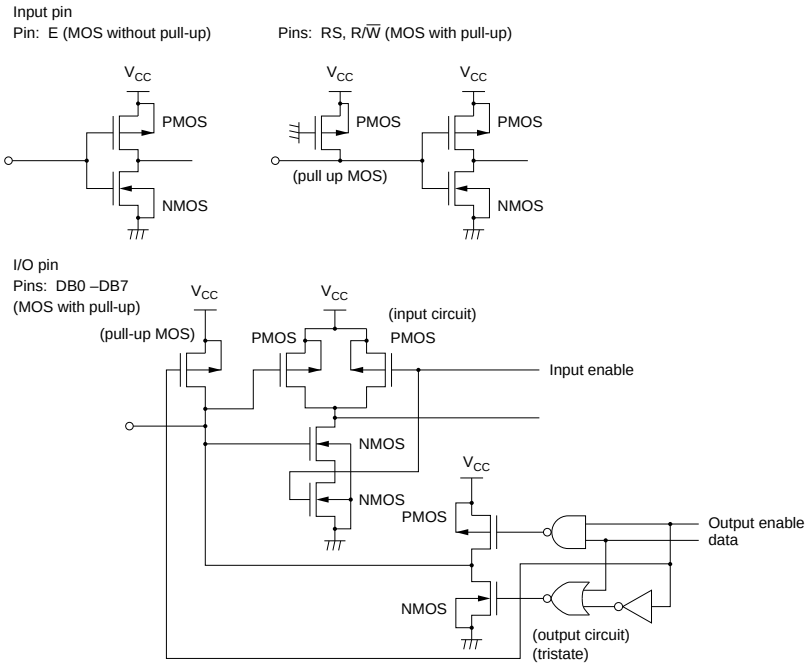
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	500	—	—	ns	Figure 32
	Low level	t_{CWL}	500	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	600		

Power Supply Conditions Using Internal Reset Circuit

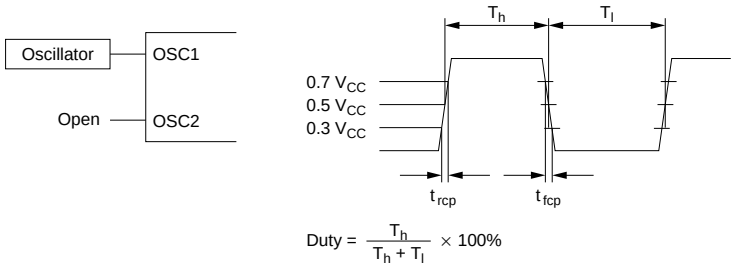
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 33
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

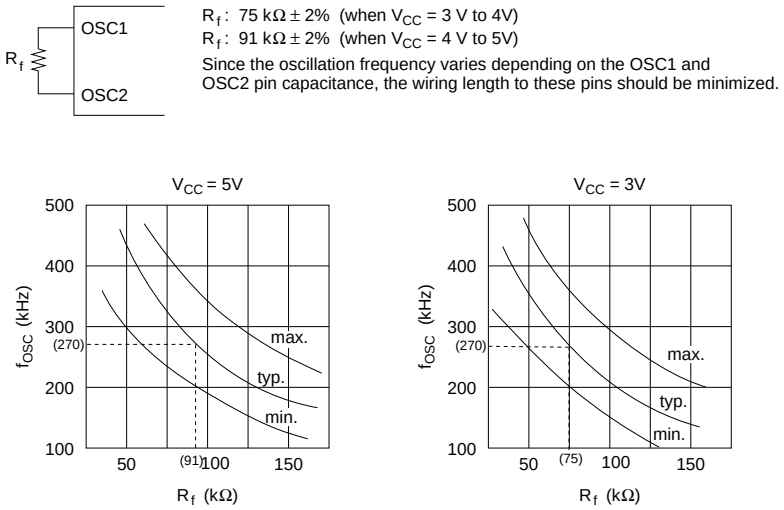
1. All voltage values are referred to GND = 0V. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.
2. $V_{CC} \geq V5$ must be maintained. In addition, if the SEG37/CL1, SEG38/CL2, SEG39/D, and SEG40/M are used as extension driver interface signals (EXT = high), GND ≥ V5 must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.



6. Applies to input pins and I/O pins, excluding the OSC1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull-up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.



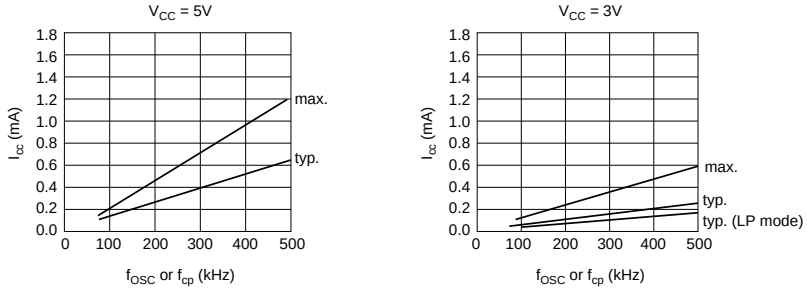
12. Applies only to the internal oscillator operation using oscillation resistor Rf.



13. RCOM is the resistance between the power supply pins (V_{CC}, V1, V4, V5) and each common signal pin (COM1 to COM33).

    RSEG is the resistance between the power supply pins (V_{CC}, V2, V3, V5) and each segment signal pin (SEG1 to SEG40).

14. The following graphs show the relationship between operation frequency and current consumption.

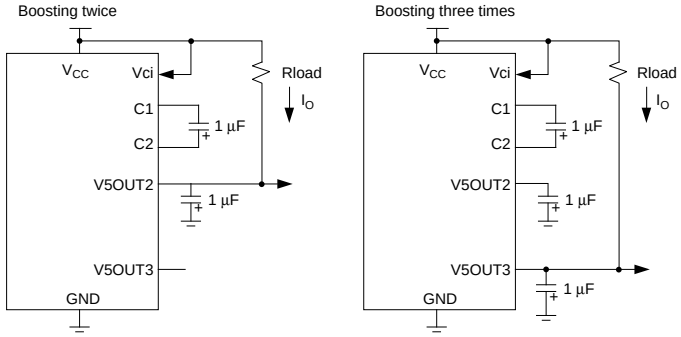


15. Applies to the OSC1 pin.

16. Each COM and SEG output voltage is within ±0.15V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.

17. The TEST pin must be fixed to the ground, and the EXT or V_{CC} pin must also be connected to the ground.

18. Booster characteristics test circuits are shown below.



19. Reference data

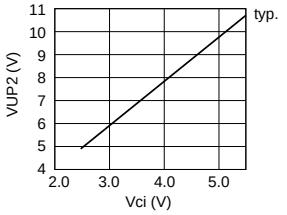
The following graphs show the liquid crystal voltage booster characteristics.

VUP2 = V_{CC}–V5OUT2

VUP3 = V_{CC}–V5OUT3

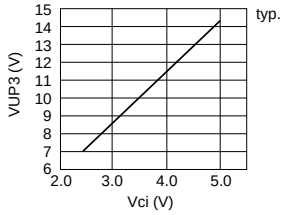
(1) VUP2, VUP3 vs Vci

Boosting twice



Test condition: Vci = V_{CC}, f_{cp} = 270 kHz
T_a = 25°C, Rload = 25 kΩ

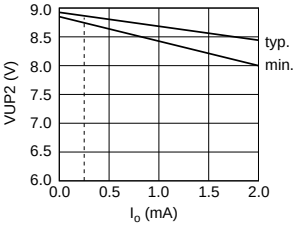
Boosting three times



Test condition: Vci = V_{CC}, f_{cp} = 270 kHz
Ta = 25°C, Rload = 25 kΩ

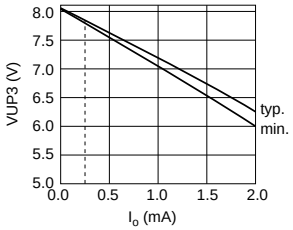
(2) VUP2, VUP3 vs I_o

Boosting twice



Test condition: Vci = V_{CC} = 4.5V
R_f = 91 kΩ, T_a = 25°C

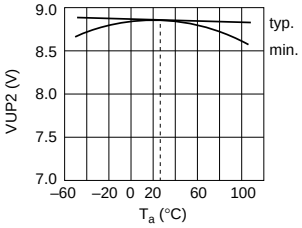
Boosting three times



Test condition: Vci = V_{CC} = 2.7V
R_f = 75 kΩ, T_a = 25°C

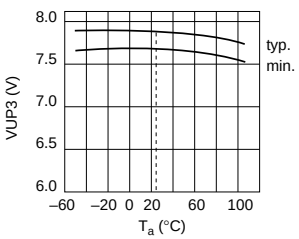
(3) VUP2, VUP3 vs T_a

Boosting twice



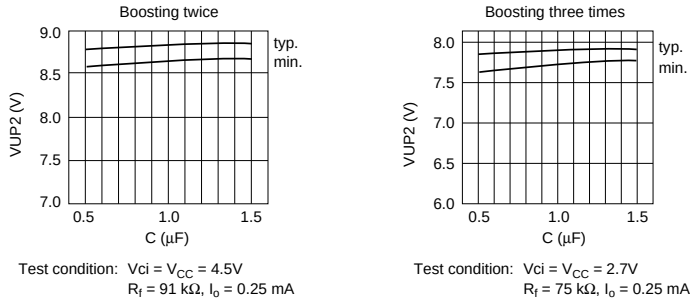
Test condition: Vci = V_{CC} = 4.5V
R_f = 91 kΩ, I_o = 0.25 mA

Boosting three times



Test condition: Vci = V_{CC} = 2.7V
R_f = 75 kΩ, I_o = 0.25 mA

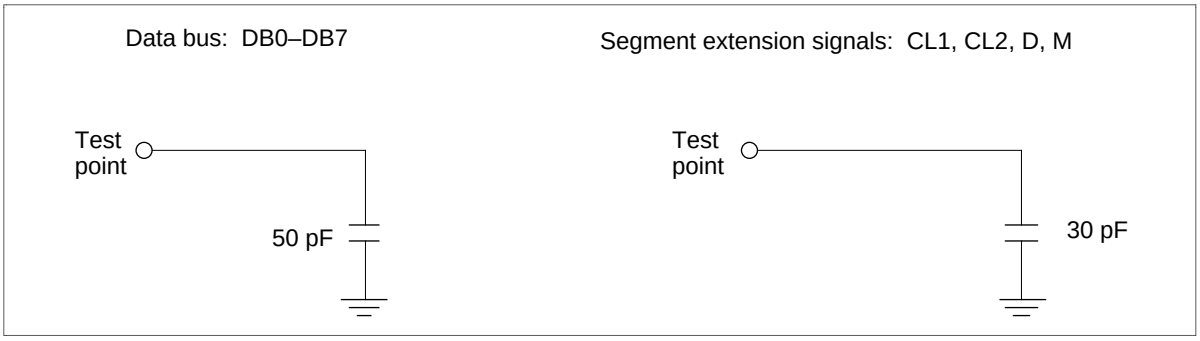
(4) VUP2, VUP3 vs Capacitance



20. Vci ≤ V_{CC} must be maintained.

Load Circuits

AC Characteristics Test Load Circuits



Timing Characteristics

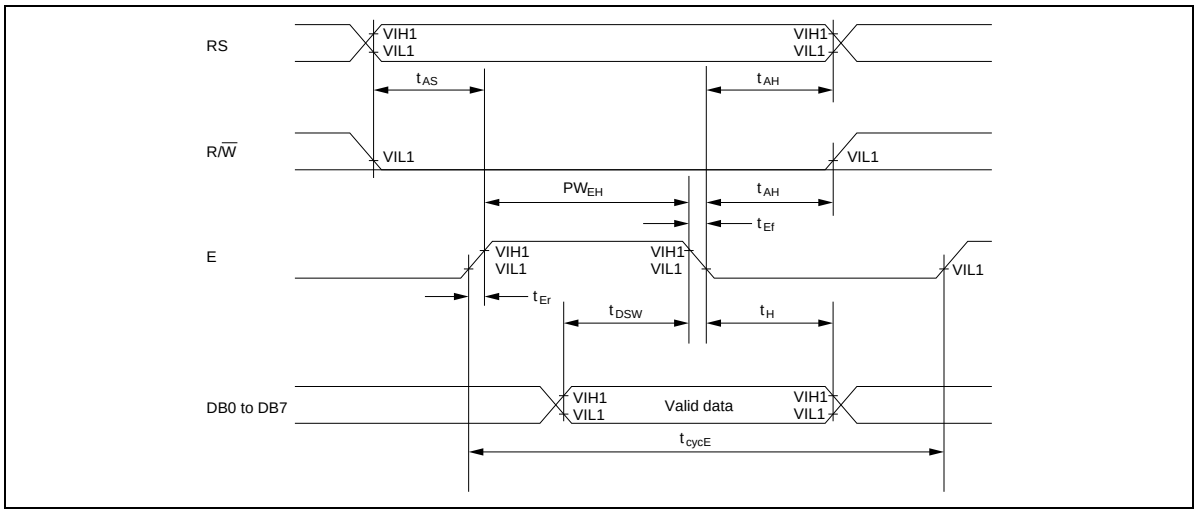


Figure 30 Write Operation

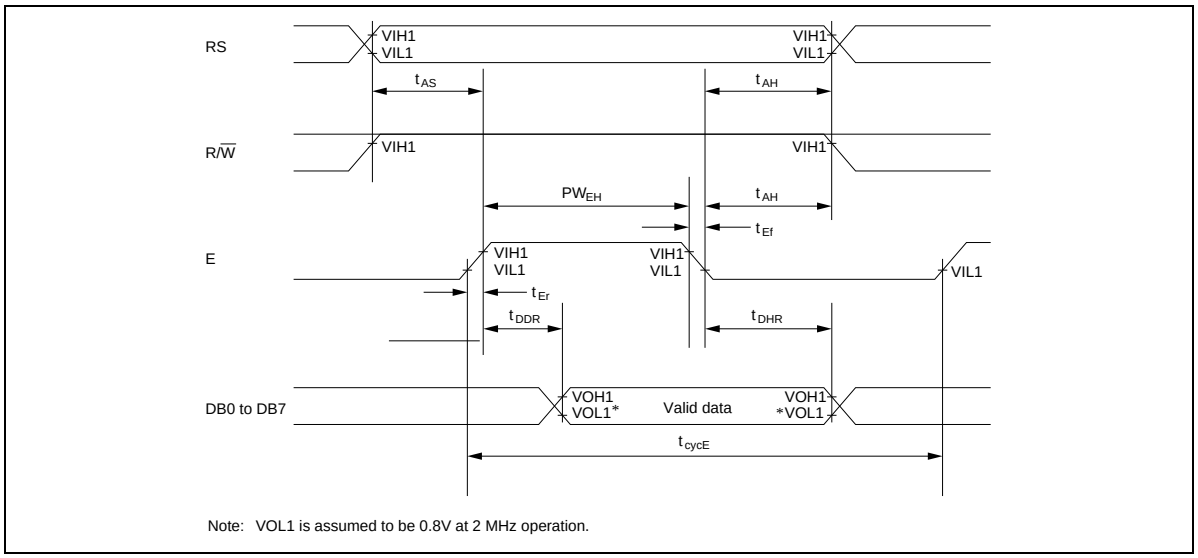


Figure 31 Read Operation

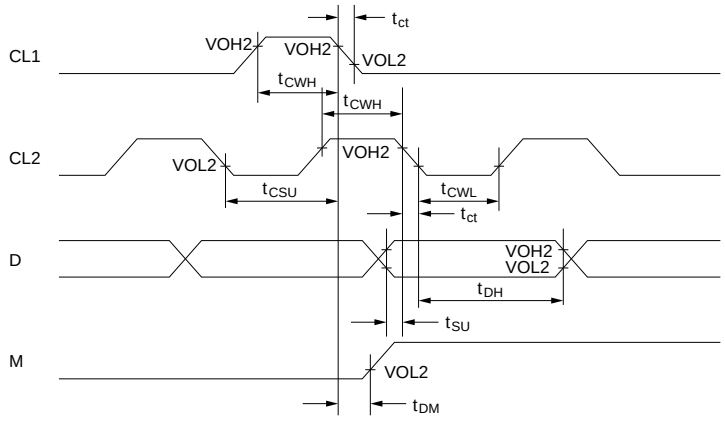
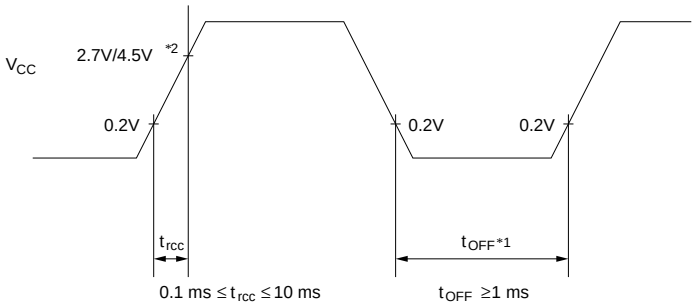


Figure 32 Interface Timing with External Driver



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5V for standard voltage operation, and at 2.7V for low voltage operation.
3. If the above electrical conditions are not satisfied, the internal reset circuit will not operate normally. In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 33 Power Supply Sequemce