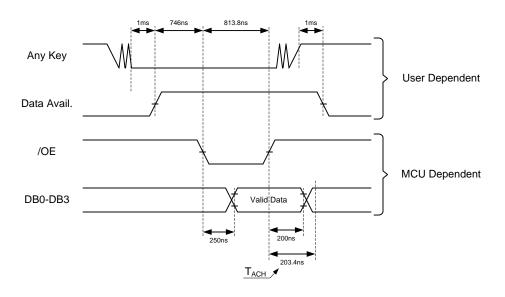
Key Read Timing (max)



| MCU External Memory Interface (EMI) Timing Parameters | | | | | | | |
|---|------------------------------------|-----------------------------|---|--|--|--|--|
| SYS@LK → | 14.7456MHz | Period | 6.78168E-08 | | | | |
| | | | | | | | |
| EMI Parameter | Pulse Width Extension Factor | Total Pulse Width (sec.) | Description | | | | |
| T _{ALEH} | 4 | 2.71267E-07 | Address/Control latch enable high time | | | | |
| TALEL | 4 | 2.71267E-07 | Address/Control latch enable low time | | | | |
| TACS | 3 | 2.03451E-07 | Address/Control setup time | | | | |
| _ | 12 | 8 13902F-07 | Address/Control pulse width for /WR & /RD | | | | |
| T _{ACW} | 12 | 0.1300ZL-07 | Address/ Control palse Wath Tol / WK C/ND | | | | |

| Key | Encoder Timing | SIZE I | FSCM NO | I DWG NO | T REV 1 |
|--------|----------------|--------|---------|------------------------------|---------|
| DRAWN | TBL | | | Figure 4: Key Encoder Timing | 1.0 |
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