SIEMENS

Schule für Daten- und Informationssysteme

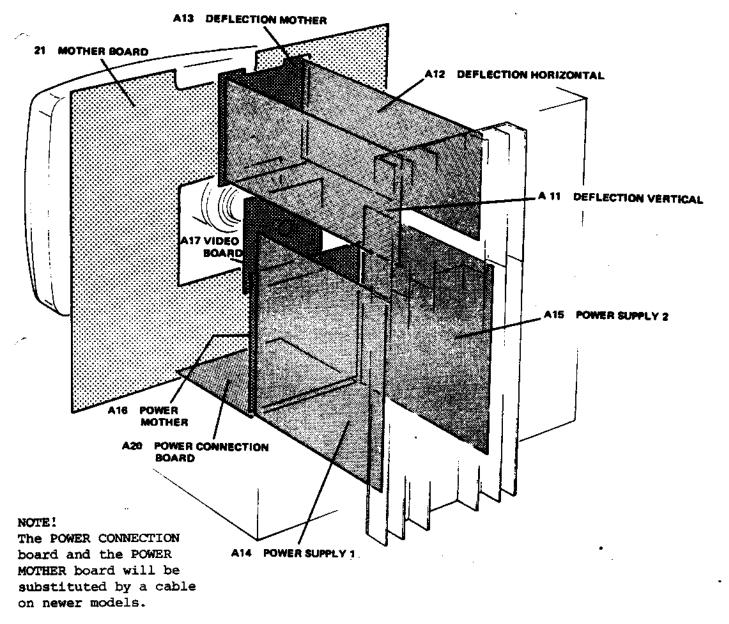
Technische Ausbildung

REGISTER III

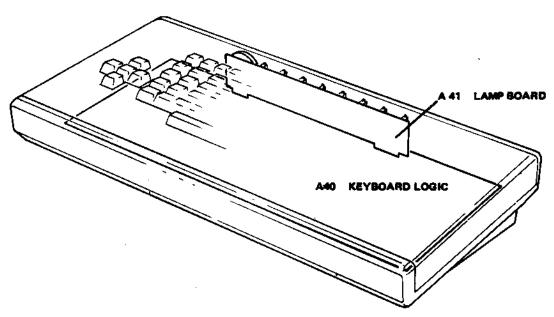
0 Verdrahtung

1 Verschiedenes

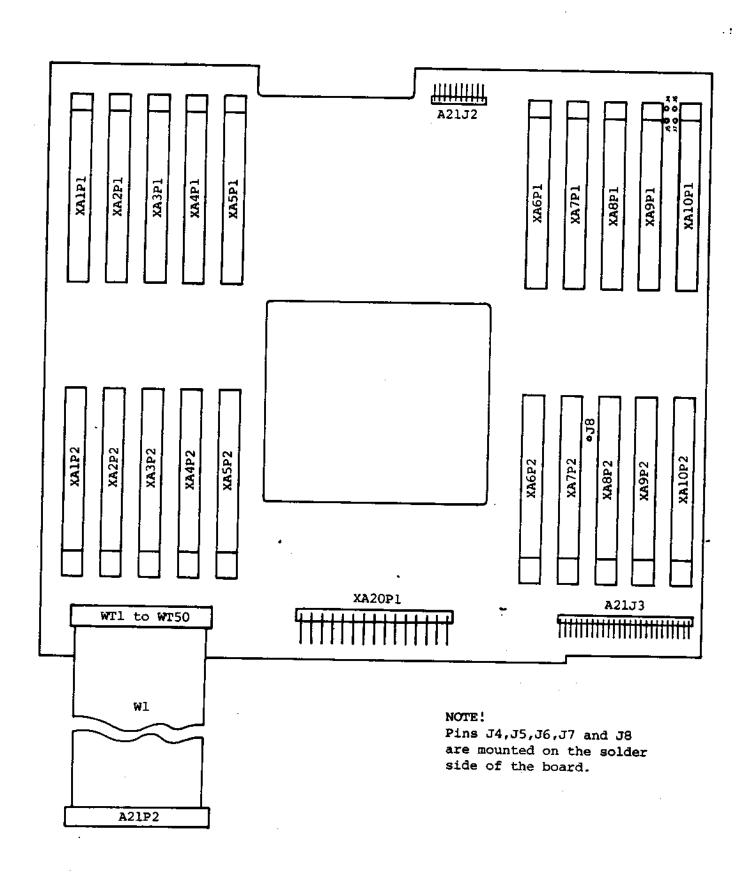
Position number	Assembly number	Board part number	Board name	Comments
Al		960321	DISKETTE CONTROLLER	
A2	:	960320	CASSETTE CONTROLLER	
A3		9 6 0316	CLUSTER INTERFACE	
A 4		960319	SYNCHRONOUS INTERFACE	
• A5		960314	PROM CR/PTR INTERFACE	Programmable Read Only . Memory with Card Reader and Paper Tape Reader
		•		Interface.
A 6				A second Cluster Inter-
110				face board, a PROM board
		·		or a RAM board can be
				used in this position.
A7		960315	RAM BCARD	Random Access Memory.
A8		960313	CPU BOARD	Central Processing Unit.
A9		960310	DISPLAY LOGIC 2	
A10		960309	DISPLAY LOGIC 1	[
All	ן	960307	DEFLECTION V .	
A12	1 1	960308	DEFLECTION H	
A13		960377	DEFLECTION MOTHER	1
A14	1	960305	POWER SUPPLY 2	
A15	} 2	960304	POWER SUPPLY 1	
A16		960345	POWER MOTHER	
AÏ7		960306	VIDEO BOARD	
A20		960346	POWER CONNECTION	
A21		960312	MOTHER BOARD	·
A22		960318	CONNECTOR BOARD	
A23		900249	POWER TERMINATION	Mounted on Power Supply 2.
A31		960330	CASSETTE DRIVE UNIT	
A32		960329	DISKETTE DRIVE UNIT	1
A40		960303	KEYBOARD LOGIC	Separate unit
A41			LAMP BOARD	
A30 `		960384	ASYNCHRONOUS/ISOCHRONOUS	Separate unit, not inside
			CONVERTER	the cabinet.



LOCATION OF THE BOARDS IN THE TDV 2114



LOCATION OF THE BOARDS IN THE KEYBOARD UNIT



THE MOTHERBOARD SEEN FROM THE COMPONENT SIDE

PIN NO.	SIGNAL NAME	A1 E E E E E E E E E E E E E E E E E E E	A2 E CARTR. CONTR. Z	A3 CLUSTER 5 INTF.	A4 E SYNCHR. O CR/PTR Z	A5 PROM S	A6 EL OZ	A7 LCG
							 	
1	GND	GND	GND	GND	GND	GND	GND	GND
2	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
3	OUT E 7	-	_	_	_	_	-	_
4	OUT E 6			 			- '	 -
5	OUT E 5	-	_	-	-	-	–	-
6	OUT E 4	_ 		_	_		4.00	1
7 8	AB 8	AB8	AB8		_	AB8	AB8	AB8
9	AB 10 DB 0	AB10 DB0	AB10 DB0	DB0	DB0	DB0	AB10 DB0	AB10 DB0
10	GRANT 4	_	DBU	DBU	DBU		DBU	טפען
11	DB 2	DB2	DB2	DB2	DB2	DB2	DB2	DB2
12	GRANT 1		DD2	_	DD2	-	DD2	DD2
13	AB 14	AB14	AB14		_	AB14	AB14	AB14
14	AB 12	AB12	AB12	· _ ·	_	AB12	AB12	AB12
15	DB 7	DB7	DB7	DB7	DB7	DB7	DB7	DB7
16	AB 4	AB4	AB4	AB4	AB4	AB4	AB4	AB4
17	DR 1	_	_	_	_	_	_	
18	AB 0	AB0	AB0	AB0	AB0	ABO	AB0	AB0
19	AB 5	AB5	AB5	AB5	AB5	AB5	AB5	AB5
20	AB 1	AB1	AB1	AB1	AB1	AB1	AB1	AB1
21	DR 2	DR2		-	_	-	_	
22	+ 12 V		+ 12 V	+ 12 V	+ 12 V.	+ 12 V	+ 12 V	
23	- 5 V	·	_	_	-	- 5 V	- 5 V	I –
24	IREQ 3			_	_		_	l
25	IREQ 1				· · · · · · · · · · · · · · · · · · ·			
26	IREQ 6	IREQ6	_	_	_	_ !		! -
27	IACK 6	IACK6		_		_	_	_
28	IACK 4	_		IACK4	_		_	_
29	IACK 2	_	_	_	IACK2 8	_		
30	IACK 0		_	_	_	·	_	-
31	DB 4	DB4	DB4	DB4	DB4	DB4	DB4	DB4
32	IACK 7	_	IACK7	·	_		_	-
P1 B								
1	GND	GND	GND	GND	GND	GND	GND	GND
2	+ 5 V	+ 5 V	+ 5 V	+ 5 V	4 5 V	+ 5 V	+ 5 V	+ 5 V
3	IN E4		. J ¥	. J ¥				+ 5 V
4	IN E5							
5	IN E6							
6	IN E0 IN E7							
7	AB 9	AB9	AB9		_	AB9	AB9	AB9
8	AB 11	AB11	AB11		_	AB11	AB11	AB11
9	DB 1	DB1	DB1	DB1	DB1	DB1		DB1
10	GRANT 3	-	GRANT3	_	-		-	-
11	GRANT 2	GRANT2	-		_	_	_	_
12	AB 15	AB15	AB15			AB15		AB15
13	AB 13	AB13	AB13	_		AB13		AB13
14	DB 6	DB6	DB6	DB6	DB6	DB6		DB6
	DD 0							
	AB 6	AB6	AB6		AB6	AB6 1	1100 1	ADD
15 16				AB6 AB2	AB6 AB2	AB6 AB2		AB6 AB2
15 16 17	AB 6	AB6 AB2	AB6	AB6				
15 16 17 18	AB 6 AB 2 DR 4 AB 7	AB6 AB2	AB6 AB2	AB6 AB2	AB2	AB2	AB2	AB2
15 16 17 18 19	AB 6 AB 2 DR 4 AB 7 AB 3	AB6 AB2	AB6 AB2	AB6 AB2 —	AB2	AB2	AB2 - AB7	AB2 -
15 16 17 18 19 20	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT	AB6 AB2 — AB7	AB6 AB2 AB7 AB3	AB6 AB2 — AB7	AB2 — AB7	AB2 - AB7	AB2 - AB7	AB2 - AB7
15 16 17 18 19 20	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT	AB6 AB2 — AB7 AB3	AB6 AB2 — AB7 AB3	AB6 AB2 — AB7 AB3	AB2 AB7 AB3	AB2 	AB2 - AB7 AB3 -	AB2 - AB7 AB3
15 16 17 18 19 20 21	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V	AB6 AB2 — AB7 AB3	AB6 AB2 AB7 AB3	AB6 AB2 — AB7 AB3	AB2 AB7 AB3	AB2 AB7 AB3 - + 12 V	AB2 - AB7 AB3 - + 12 V	AB2 - AB7 AB3
15 16 17 18 19 20 21 22 23	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V - 5 V	AB6 AB2 — AB7 AB3 —	AB6 AB2 AB7 AB3 DR3	AB6 AB2 — AB7 AB3 — —	AB2 AB7 AB3 	AB2 	AB2 - AB7 AB3 -	AB2 AB7 AB3
15 16 17 18 19 20 21 22 23	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V - 5 V IREQ 4	AB6 AB2 — AB7 AB3 — — —	AB6 AB2 — AB7 AB3 — DR3 —	AB6 AB2 — AB7 AB3 — — — — IREQ4	AB2 AB7 AB3 	AB2 AB7 AB3 - + 12 V - 5 V	AB2 - AB7 AB3 - + 12 V - 5 V	AB2
15 16 17 18 19 20 21 22 23 24	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V - 5 V IREQ 4 IREQ 2	AB6 AB2 — AB7 AB3 — — —	AB6 AB2 — AB7 AB3 — DR3 —	AB6 AB2 — AB7 AB3 — — — — IREQ4	AB2 AB7 AB3 	AB2 AB7 AB3 - + 12 V	AB2 - AB7 AB3 - + 12 V	AB2
15 16 17 18 19 20 21 22 23 24 25	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V - 5 V IREQ 4 IREQ 2 IREQ 7	AB6 AB2 — AB7 AB3 — — —	AB6 AB2 — AB7 AB3 — DR3 — — — — IREQ7	AB6 AB2 — AB7 AB3 — — — — IREQ4	AB2 AB7 AB3 	AB2 AB7 AB3 - + 12 V - 5 V	AB2 - AB7 AB3 - + 12 V - 5 V	AB2
15 16 17 18 19 20 21 22 23 24 25 26 27	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V - 5 V IREQ 4 IREQ 2 IREQ 7 IREQ 5	AB6 AB2 — AB7 AB3 — — —	AB6 AB2 — AB7 AB3 — DR3 — — — IREQ7	AB6 AB2 AB7 AB3 IREQ4 IREQ5	AB2 AB7 AB3 	AB2 AB7 AB3 - + 12 V - 5 V	AB2 - AB7 AB3 - + 12 V - 5 V	AB2
15 16 17 18 19 20 21 22 23 24 25 26 27 28	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V - 5 V IREQ 4 IREQ 2 IREQ 7 IREQ 5 IACK 5	AB6 AB2 — AB7 AB3 — — — — — — — —	AB6 AB2 — AB7 AB3 — DR3 — — — IREQ7	AB6 AB2 — AB7 AB3 — — — — IREQ4	AB2	AB2 AB7 AB3 - + 12 V - 5 V	AB2 - AB7 AB3 - + 12 V - 5 V	AB2
15 16 17 18 19 20 21 22 23 24 25 26 27 28	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V - 5 V IREQ 4 IREQ 2 IREQ 7 IREQ 5 IACK 5	AB6 AB2 — AB7 AB3 — — — — — —	AB6 AB2 — AB7 AB3 — DR3 — — — IREQ7	AB6 AB2 AB7 AB3 IREQ4 IREQ5	AB2 AB7 AB3 IREQ2 8	AB2 AB7 AB3 - + 12 V - 5 V - - -	AB2 - AB7 AB3 - + 12 V - 5 V	AB2
15 16 17 18 19 20 21 22 23 24 25 26 27 28	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V - 5 V IREQ 4 IREQ 2 IREQ 7 IREQ 5 IACK 5 IACK 3 IACK 1	AB6 AB2 — AB7 AB3 — — — — — — — — —	AB6 AB2 AB7 AB3 - DR3 - IREQ7	AB6 AB2 AB7 AB3 IREQ4 IREQ5 IACK5	AB2	AB2 AB7 AB3 - + 12 V - 5 V	AB2 	AB2 AB7 AB3
15 16 17 18 19 20 21 22 23 24 25 26 27 28	AB 6 AB 2 DR 4 AB 7 AB 3 WAIT DR 3 + 12 V - 5 V IREQ 4 IREQ 2 IREQ 7 IREQ 5 IACK 5	AB6 AB2 — AB7 AB3 — — — — — — — —	AB6 AB2 AB7 AB3 - DR3 - IREQ7 - DB3	AB6 AB2 AB7 AB3 IREQ4 IREQ5 IACK5 DB3	AB2 AB7 AB3 IRLQ2 B DB3	AB2 AB7 AB3 - + 12 V - 5 V DB3	AB2 	AB2

•			These cor	nec ard	tors DO NOT hab	ve	
NOTE	A8 CPU	NOTE	A9 DISPLAY LOGIC II	NOTE	A10 DISPLAY LOGIC I	NOTE	PIN NO.
	GND + 5 V OUT E7		GND + 5 V -		GND + 5 V IFCOM (OE7)		1 2 3
	OUT E5		<u> </u>		CTRAW (OE6) CRAW (OE5) CPU RLD (OE4	`	4 5 6
	OUT E4 AB8 AB10		ODB0 ODB5	1	ODB0 ODB5	1 1	7 8
	DB0 GRANT4 DB2		DB0 VIDEO DB2	4	DBO TSB DB2	2	9 10 11
	GRANT1 AB14		LHC ODB1	1	LHC ODB1	1 1	12 13
	AB12 DB7		CCADV DB7 CURAD	1	CCADV DB7 CURAD	1	14 15 16
	AB4 DR1 AB0		CURL CURD	1	CURL CURDV	1	17 18
	AB5 AB1 DR2		RINPEN HOME DEC72	1	RINPEN HOME DEC72	1 1	19 20 21
	+ 12 V 5 V IREQ3		+ 12 V 80 CHAR -	•	+ 12 V CH80 IREQ3		22 23 24
	IREQ1 IREQ6 IACK6		IREQ1 DEC25 LVC	1	DEC25 LVC	1	25 26 27
	IACK4 IACK2 IACK0	8	EOL CCEN SAB7	1 1 1	EOL CCEN SAB7	1 1	28 29 30
	DB4 IACK7		DB4 ODB7	1	DB4 ODB7	1	31 32
	GND + 5 V INE4		GND + 5 V -		GND + 5 V IE4		1 2 3
· ·	INE5 INE6 INE7				CRAR (I E5) IE6 IFST (IE7)		4 5 6
	AB9 AB11		DEC24 ODB6	1 1	DEC24 ODB6 DB1	1	7 8 9
	DB1 GRANT3 GRANT2		DB1 BLANKN VSYNC	3	EPS NP	2 2	10 11
	AB15 AB13 DB6		ODB3 ODB4 DB6	1	ODB3 ODB4 DB6	1	12 13 14
	AB6 AB2		ODB2 Lointa	1 3	ODB2 KSTR	1 4	15 16
	DR4 AB7 AB3 WAIT		LF RESCC RAMWRP EOP	1 1 1	LF RESCC RAMWRP EOP	1 1 1	17 18 19 20
	DR3 + 12 V		HSYNC + 12 V CCUP	1	HSYNC + 12 V CCUP	1	21 22 23
	IREO4 IRFQ2	8	CURUP ROLLF	1	CURUP ROLLF	1	24 25 26
	IREQ7 IREQ5 IACK5		VIDOF CURBL MBSY	1 1 1	VIDOF CURBL MBSY	1 1 1	27 28
	IACK3 IACK1		IACK1		IACK3		29 30 31
	DB3 DB5		DB3 DB5		DB3 DB5		32

Positions marked – means that the bus signal is present on the connector but not in use on the listed board.

The list gives the determined positions for the boards. Locations A5 to A7 may be used for memory boards (max. 48k) in other configurations.

NOTE 1: Signals connecting Display Logic I and II.

NOTE 2: Goes to connector board via W1P1 - connector board cable (location 7

NOTE 3: Signals go to the TV circuits via A21 J2.

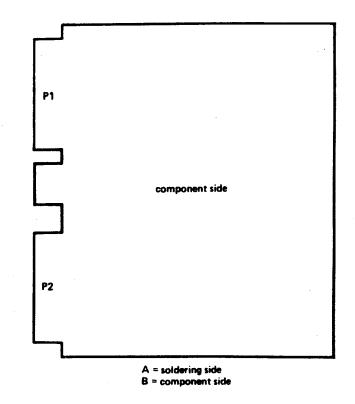
NOTE 4: Video signal to video board via J4-J5.

NOTE 5: Keyboard signals to and from keyboard via A21 J3.

NOTE 6: Bell signal going to loudspeaker via J6-J7.

NOTE 7: CPU clear signal from push button in front via J8.

NOTE 8: On Motherboards L-92655-0, L-92655-1 and L-92655-2 connections must be strapped between CPU and Sync Interface when Sync Inetrface is used.



NOTE: The table does not indicate the polarity of the signal!

SIGNAL NAMES ON THE P1 CONNECTORS ON THE TDV 2114 MOTHERBOARD

	PIN NO.	SIGNAL NAME	A1 DISKETTE CONTR.	A2 E CARTR. O CONTR. Z	A3 CLUSTER O INTF.	A4 SYNCHR. E CR/PTR Z	A5 PROM D	A6 EL ON SINGE	A7 LCG ON	A8 CPU
ŀ			·				·			CLOC
	1 2	– 12 V	-	-	– 12 V	- 12 V		-		12 V
	3	DMARW INTE	_	-	_			DMARW	-	DMAR INTE
ŀ	5	INTA	_			.+	-		-	INTA
1	6	MEMR		· -	-			W. 1887		MEMR OUT
	7	OUT	_	-	INP	OUT		-	_	INP
ŀ	9	INP 3000			INF					3000
1	10	SINGLE							-	SINGI
	11	PH2 TTL	-		_	-	-	-	PH2 TTL	PH2 T STEP
_	12	STEP	- Drove	RESET	RESET	RESET	RESET	RESET	RESET	RESE
	13 14	RESET MCLR	RESET -	KESE I	-	— .	-	-		MCLR
1	15	MIN	MIN	MIN	<u> </u>		MIN	MIN	MIN	MIN
L	16	MW	MW	MW				MW	MW	MW
	17	IOIN	IOIN	IOIN	IOIN	IOIN	IOIN	WTRQ		WTRQ
Ī	18 19	WTRQ IOW	- IOW	IOM -	IOW	IOW		WIKQ -	IOW	IOW
	20	DMAPLS	DMAPLS	DMAPLS		-				DMAP
` 		307.2 kHz	-	-	307.2 kHz	307.2 kHz		_	_	307.2 KEY I
	22	KEY LO			_	- .		_		KEY I
	23	KEY HI		-	_ FL+12 V	_	_	- -	_	FL+12
ŀ	24 25	FL + 12 V FL - 12 V			FL-12 V	_		-	_	FL-13
-		PRINT HI	_		_			-	-	PRINT
Ţ	27	PRINT LO	-		_		-	-	-	PRINT
L	28							 	 	
1	29 30	STROBE	· _ ·		_			STROBE	_	STRO
		PH1 TTL			_	-	-	PH1 TTL	PH1 TTL	PH1 T
	32		<u> </u>				<u> </u>			
	P2 B									
ſ	1									
•	2		.	CND*						TEST
	3 4	}	GND GND	GND* GND*		•				
H	5		GND	GND*						
	6		+ 5 V	+ 5 V*						
	7		+ 5 V	+ 5 V*						
ᅪ	9				·			-		
1	10]		CP1 8]	CPCL
1	11						8	1	1	
	12						& 8 - 8		 	
	13 14						0 8		1	
	15				1		1 8		1	
L	16						2 8			
	17				[3 8 4 8		1	
	18 19	l					5 8			
	20						ST 1 8			
Г	21		, , ,				ST 2 8			
	22					CT108 2 CT105 2	& or 6 8		1	
	23					101105 2	,	1		
	24					CT104 2	5 8			
Г	25					CT107 2	2 8			
	26	1			ł	CT106 2 CT109 2	3 8 1 or 9 8			
	27 28					CT114 2	0 or 8 8			
	29					CT115 2	- or 7 8			INF6
	30					CT125 2	CP2 8		1	INF7
1	31	İ	110 4C 5 5	}		1				
Ĺ	32		WMODE		<u>L</u>	<u>L</u>	<u> </u>	1	<u>1</u>	

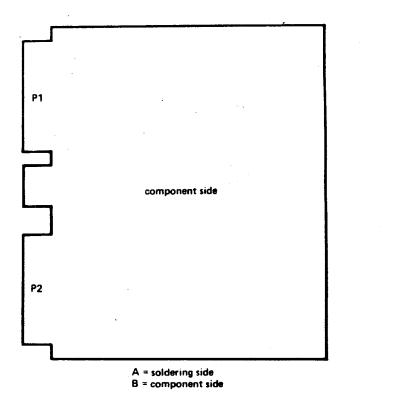
^{*}These five signals are not in use on the Cartridge Controller, but a second Diskette Controller can be used in this location.

CI.OCK	NOIE	A8 CPU	NOTE	A9 DISPLAY LOGIC II	NOTE	A10 DISPLAY LOGIC I	NOTE	PIN NO.
NTE						- 12 V		1 2 3
MEMR		INTE		HSYNC		KB6		4
INP		MEMR		RAB3	l	RAB3		5 6 7
PH2 TTL TREN 1 TREN 1 TREN 1 TRESTEP CHCLK1 1 CHCLK1 1 CHCLK1 1 TRESTEP SAB8 1 SAB8 1 MCLR MC	-	INP 3000		SAB11	1	SAB11	1	9
RESET SABS 1 SABS 1 MCLR	PH2 TTL		TREN	l	TREN	l	10 11 12	
MIN MW		RESET	·	SAB8	_	SAB8		13 14
WTRQ IOW DMAPLS CLEARK 5		MIN			1	CHCLK OCTC		15 16
DMAPLS		WTRQ		SETB8	1	SETB8		17 18 19
KEY LO 8 KEY HI 8 FL+12 V 8 FL+12 V 8 FL+12 V 8 FL+12 V FL CLDOC	$\frac{1}{1}$	DMAPLS				CLEARK	5	20 21
FI.—12 V 8 PRINT HI 8 PRINT LO 8 PRINT LO 8 PRINT LO 8 PRINT LO 8 EOL ENQL 5 CARL 5 ERRORL 5 ERRORL 5 OCTA 2 RB1 1 RB1 1 RAB4 1 TEST RAB5 1 RAB5 1 CARRY 1 RACRY 1 DOTCLK3 1 RAB2 1 RAB2 1 RAB2 1 RAB5 5 KB3 5 KB7 5 KB3 5 KB7 5 KB4 5 CT106 2 CT103 2 TRANSK 5 BREAK 5 CT106 2 CLDOCI 2 LLB 1 LLB 1 CT105 2 CT107 2 ACKL 5	1	KEY LO KEY HI	8			CT108	.2 2	22 23 24
PRINT LO 8 EOL	٦	FL-12 V	8			12 V FL		25
STROBE				EOL		WAITL	5	26 27 28
RB1 1 RB1 1 RAB4 1 RAB4 1 TEST RAB5 1 RAB5 1 CARRY 1 RACRY 1 DOTCLK3 1 RAB2 1 RAB2 1 KB5 5 KB3 5 KB3 5 KB7 5 KB4 5 KB4 5 NNLIL 5 NLINEK 5 SAB9 1 SAB9 1 ERASE 1 ERASB 1 OCT B 2 VBLANK 1 VBLANK 1 CLDICO 2 CT103 2 TRANSK 5 BREAK 5 CT106 2 CLDOCI 2 LLB 1 LLB 1 CT105 2 CT107 2 ACKL	1	STROBE				CARL ERRORL	-5	29 30
RAB4 1 RAB4 1 RAB5 1 RAB5 1 CARRY 1 RACRY 1 DOTCLK3 1 RAB2 1 RAB2 1 KB5 5 KB3 5 KB3 5 KB7 5 KB4 5 RACRY KB1 5 ONLIL 5 SAB9 1 SAB9 1 ERASE 1 ERASB 1 OCT B 2 VBLANK 1 VBLANK 1 CLDICO 2 CT103 2 TRANSK 5 DEC72 BREAK 5 CT106 2 CLDOCI 2 LLB 1 LLB 1 CT105 2 CT107 2 ACKL 5		PH1 TTL						$\frac{31}{32}$
RAB4 1 RAB4 1 RAB5 1 RAB5 1 CARRY 1 RACRY 1 DOTCLK3 1 RAB2 1 RAB2 1 KB5 5 KB3 5 KB3 5 KB7 5 KB4 5 RACRY KB1 5 ONLIL 5 SAB9 1 SAB9 1 ERASE 1 ERASB 1 OCT B 2 VBLANK 1 VBLANK 1 CLDICO 2 CT103 2 TRANSK 5 DEC72 BREAK 5 CT106 2 CLDOCI 2 LLB 1 LLB 1 CT105 2 CT107 2 ACKL 5								
CARRY 1 RACRY 1		•		RAB4		RAB4	1	1 2
RAB2 1 RAB2 1 KB5 5 KB3 5 KB3 5 KB3 5 KB7 5 KB4 5 KB4 5 KB4 5 KB4 5 KB1 5 ONLIL 5 LINEK 5 SAB9 1 ERASE 1 ERASE 1 ERASE 1 OCT B 2 VBLANK 1 VBLANK 1 CLDICO 2 CT103 2 TRANSK 5 DEC72 BREAK 5 CT106 2 CLDOCI 2 LLB 1 LLB 1 LLB 1 CT105 2 CT107 2 ACKL 5	\downarrow	TEST	_	CARRY	1			2 3 4 5
CPCL 7 RACRY KB4 5 KB4 5 KB1 5 ONLIL 5 LINEK 5 SAB9 1 SAB9 1 ERASE 1 ERASB 1 OCT B 2 VBLANK 1 VBLANK 1 CLDICO 2 CT103 2 TRANSK 5 DEC72 BREAK 5 CT106 2 CLDOCI 2 LLB 1 LLB 1 CT105 2 CT107 2 ACKL 5							5	6 7
RACRY KB1 5 ONLIL 5 LINEK 5 SAB9 1 SAB9 1 ERASE 1 ERASB 1 OCT B 2 VBLANK 1 VBLANK 1 CLDICO 2 CT103 2 TRANSK 5 DEC72 BREAK 5 CT106 2 CLDOCI 2 LLB 1 LLB 1 CT105 2 CT107 2 ACKL 5	+	·			_			8
LINEK 5 SAB9 1 ERASE 1 ERASB 1 OCT B 2		CPCL	7	RACRY		KB1	5	10
ERASE 1 ERASB 1 OCT B 2	+		_	·	-			12 13
VBLANK 1				-		ERASB	1	14 15 16
CT103 2 TRANSK 5 DEC72 BREAK 5 CT106 2 CLDOC1 2	†			VBLANK	1	VBLANK	1	17 18
CT106 2 CLDOCI 2 LLB 1 LLB 1 CT105 2 CT107 2 ACKL 5						CT103	2 5	19 20
LLB 1 LLB 1 CT105 2 CT107 2 ACKL 5	T			DEC72		CT106	2	21 22
CT105 2 CT107 2 ACKL 5				LLB	1			23 24
ACKL 5	T					CT105	2	25 26
						ACKL CT104	5 2	27 28
INF6 - IRST (IF6) URSTIN (IF7)	- 1			<u>-</u>			1	29 30 31
								$\frac{31}{32}$

Positions marked – means that the bus signal is present on the connector but not in use on the listed board.

The list gives the determined positions for the boards. Locations A5 to A7 may be used for memory boards (max. 48k) in other configurations.

- NOTE 1: Signals connecting Display Logic I and II.
- NOTE 2: Goes to connector board via W1P1 connector board cable (location 7).
- NOTE 3: Signals go to the TV circuits via A21 J2.
- NOTE 4: Video signal to video board via J4-J5.
- NOTE 5: Keyboard signals to and from keyboard via A21 J3.
- NOTE 6: Bell signal going to loudspeaker via J6-J7.
- NOTE 7: CPU clear signal from push button in front via J8.
- NOTE 8: On Motherboards L-92655-0, L-92655-1 and L-92655-2 connections must be strapped between CPU and C Sync Interface when Sync Interface is used.



NOTE: The table does not indicate the polarity of the signal!

SIGNAL NAMES ON THE P2 CONNECTORS ON THE TDV 2114 MOTHERBOARD

WIPL CONNECTOR BOARD CABLE

Pin no.	Comes from	Goes to	Signal name
1	XA20P1-3	A22J1-1A	+12V
2	XA20P1-5	" 1B	-12V
3	XA20P1-7	" 2A	GROUND
4	XA20P1-7	" 2B	GROUND
5	XA20P1-2	" 3A	+5V
6		" 3B	A OCTAL SWITCH
7	XA5P2-19B	" 4A	5 CR1
8	XA5P2-18B	40	4 CR1
9		ļ JA	B OCTAL SWITCH
10	XA5P2-17B	36	3 CR1
11	XA5P2-16B	OA.	2 CR1
12	XA5P2-15B	OB	1 CR1
13		/A	C OCTAL SWITCH
14	W75D0 14D	/ b	EPS SWITCH
15	XA5P2-14B	OA.	O CR1
16	XA5P1-13B	0.5	- CR1
17		" 9A " 9B	TSB SWITCH NP SWITCH
18	VXED 100	95	& CR1
19	XA5P2-12B	" 10A " 10B	CP1 CR1
20 21	XA5P2-10B	" 11A	INT ECHO SWITCH
21 22	XA4P2-28B	" 11B	CT 114
23	XA4P2-20B	" 12A	CT 109
23	XA10P2-8A	" 12B	CL DATA IN
25	XA4P2-26B	" 13A	CT 106
26	XA4P2-25B	" 13B	CT 107
27	XA4P2-23B XA4P2-24B	" 14A	CT 104
28	XA10P2-18B	" 14B	CL DATA IN RET
29	XA4P2-23B	" 15A	CT 105
30	XA4P2-22B	" 15B	CT 108
31	XA10P2-19B	" 16A	TRD CT 103A
32		" 16B	CT 106A
33	XA4P2-21B	" 17A	CT 103
34	XA5P2-20B	" 17B	STI CR1
35	XA10P2-23B	" 18A	CL DATA OUT
36	XA10P2-23A	" 18B	CON CT 108 A
37	XA4P2-30B	" 19A	CT 125
38	XA4P2-29B	" 19B	CT 115
39	XA10P2-25B	" 20A	ROTS CT 105A
40	XA10P2-26B	" 20B	CT 107A
41	XA8P2-22A	" 21A,	KEY LO
42	XA8P2-23A	" 21B	KEY HI
43	XA10P2-26A	" 22A	CT 109A
44	XA10P2-28A	" 22B	CT 104A
45	XA20P1-	" 23A	+12V FLOAT
46	XA20P1-	" 23B	-12V FLOAT
47	XA10P2-22A	" 24A	CT 125A
48		" 24B	PROT GND CT 101
49	xa8P2-26a	" 25A	PRINT HI
50	XA8P2-27A	" 25B	PRINT LO

W2P1 CLUSTER CABLE

Pin no.	Colour	Goes to	Signal name
(I)		A22J2- 1A	GND V24
2 3		" 1B	GND V24
3		" 2A	TRD1, V24
4	*	" 2B	TRD0, V24
5		" 3A	RD1, V24
6		" 3B	RDO, V24
7		" 4A	+CL1, TRD
8		" 4B	+CLO, TRD
9		" 5A	-CL1, TRD
10		" 5B	-CLO, TRD
11		" 6A	+CL1, RD
12		" 6B	+CLO, RD
13		" 7A	-CL1, RD
14		" 7B	-CLO, RD
15		" 8A	TRD3, V24
16	•	" 8B	TRD2, V24
17	· <u>+</u>	" 9A	RD3, V24
18		" 9B	RD2, V24
19		" 10A	+CL3, TRD
20		" 10B	+CL2, TRD
21	:	" 11A	-CL3, TRD
22	Flat cable,grey	" 11B	-CL2, trd
23	g.	" 12A	+CL3, RD
24	Ð	" 12B	+CL2, RD
25	व	" 13A	-CL3, RD
26	ပိ	" 13B	-CL2, RD
27	<u> </u>	" 14A	1
28	119	" 14B	Unused
29	124	" 15A	onabea
30		" 15B	
31		" 16A	+CL5, TRD
32		" 16в	+CL4, TRD
33		" 17A	-CL5, TRD
34	,	" 17B	-CL4, TRD
35		" 18A	+CL5, RD
36		" 18B	+CL4, RD
37		" 19A	-CL5, RD
38		" 19B	-CL4, RD
39		" 20A	7
40		" 20B	.
41		" 21A	>Unused
42		" 21B	Shubeu
43		" 22A	
44		" 22B	+CL6, TRD
45		" 23A	Unused
45		" 23B	-CL6, TRD
47		" 24A	Unused
47		24A	+CL6, RD
1		" 24B " 25A	1
49		25A	Unused
50		" 25B	-CL6, RD

W3P1 KEYBOARD CABLE

Pin no.	Colour	Goes to	Signal name
1	Black	P2-22	GROUND
2	Dark green	P2-24	+12V
3	Red/yellow	P2-4	BREAK
4	White	P2-17	TRB3
5	Orange	P2-19	TRB6
6	Pink ·	P2-16	TRB7
7	Yellow	P2-20	TRB2
8	Violet	P2-18	TRB5
9	Brown	P2-14	TRB1
10	Grey	P2-15	TRB4
11	Blue/grey	P2-1	INTENSITY
12	Red/white	P2-13	L2, ON LINE LED
13	Red/grey	P2-9	L3, CARRIER LED
14	Red	P2-25	+5 ♥
15	Screen	P2-21	CHASSIS GROUND
16	Light green	P2-3	STROBE
17	Red/brown	P2-5	TRANSK
· 18	Red/green	P2-6	CLEARK
19	Red/blue	P2-12	LINEK
20	Blue	P2-23	-12V
21	Blue/yellow	P2-11	L7, NAK LED
22	Blue/white	P2-7	L8, WAIT LED
23	Blue/green	P2-2	L6, ACK LED
24	Blue/brown	P2-8	L5, ENQ LED
25	Red/black	P2-10	L4, ERROR LED

W4P1 DEFLECTION CABLE

Pin no.	Colour	Goes to	Signal name
1	Violet	A13J1-3	+12V
2	Brown	" 4	-12V
3	Orange	" 7	+24V
4	-	-	-
5	Black	" 8	GROUND
6	Blue	" 1	H SYNC
7	Grey	" 5	H/L INT
8	Green	" 9	V SYNC
9	Grey	" 2 ′	BLANK
10	White	" 6	INT

W5P1 VIDEO CABLE

Pin no.	Colour	Goes to	Signal name
1	White	DEFLECTION UNIT, pin 5	HORIZONTAL DEFLECTION
2	Grey	DEFLECTION UNIT, pin 2	HORIZONTAL DEFLECTION
3	Yellow	A17J4-4	FOCUS
4	Black	DEFLECTION UNIT, pin 1	VERTICAL DEFLECTION
5	Brown	DEFLECTION UNIT, pin 6	VERTICAL DEFLECTION

W5P2 VIDEO CABLE

Pin no.	Colour	Goes to	Signal name
9 8 7 6 5	White Grey Brown Violet Blue Red	A17J3-1 A17J3-4 A17J3-7 A17J3-3 A17J4-1 A17J4-5	INT H/L INT -12V +12V GRID NO.2 VOLTAGE +120V
3 2 1	Green Green Grey	A17J4-3 A17J4-2 A17J3-2	HEATER VOLTAGE HEATER VOLTAGE BLANK

W6Pl DISKETTE CABLE

Pin no.	Colour	Goes to	Signal name
1			
	:	A32J1-49	GND
2 3		·	
4		" 47	GND
5		" 46	RDATA
6		" 4 5	GND
7		" 44	WRTPT
8		" 43	GND
9		" 42 " 41	TRACK 00
10		" 40	GND WRITE GATE
11 12		" 39	GND
13		" 38	WDATA
14		" 37 [.]	GND
15		" 36	STEP
16		" 35	GND
17		" 34	SDIR
18		" 33	GND
19		" 32	SEL4
20		" 31	GND
21	$oldsymbol{\dot{X}}_{i}$	" 30	SEL3
22	Jre	" 29 " 29	GND
23	0.	20	SEL2
24 25	b 16	" 27 " 26	GND SEL1
25 26	cable,grey.	" 25	GND
27	Ä	" 24	GIVD.
28	Flat	" 23	GND
29	H ₄	" 22	READY
30		" 21	GND
31		" 20	INDEX
32		" 19	GND
33			
34		" 17	GND
35		" 15	
36		" 15	GND
37		" 13	GND
38 39		. 13	GND
40		" 11	GND
40		**	<u> </u>
42		" 9	GND
43			
44		" 7	GND
45			
46		" 5	GND
47			
48		" 3	GND
49		" 1	GND
50		T	מאט

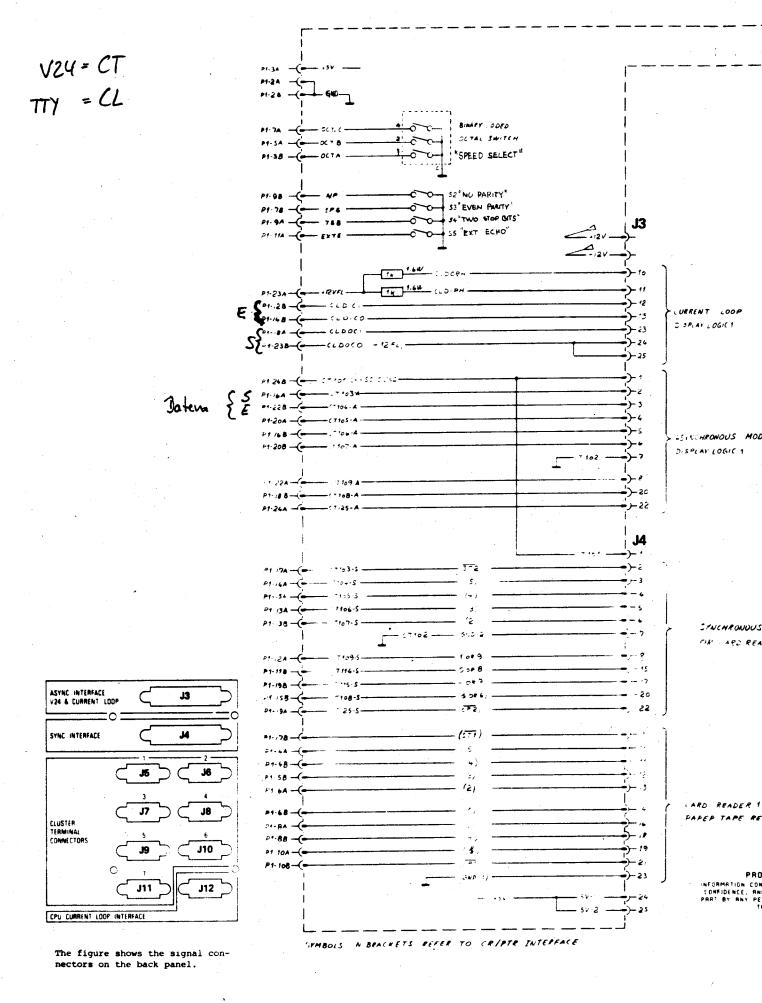
W8P1 DISKETTE POWER CABLE

Pin no.	Colour	Goes to	Signal
1	Red	A32J2-5	+5V
2	Blue	" 4	-5 v
5	Yellow	" 1	+24V
6	Green	" 2	GND (+24V)
7	Brown	6 and 3	GND (±5V)

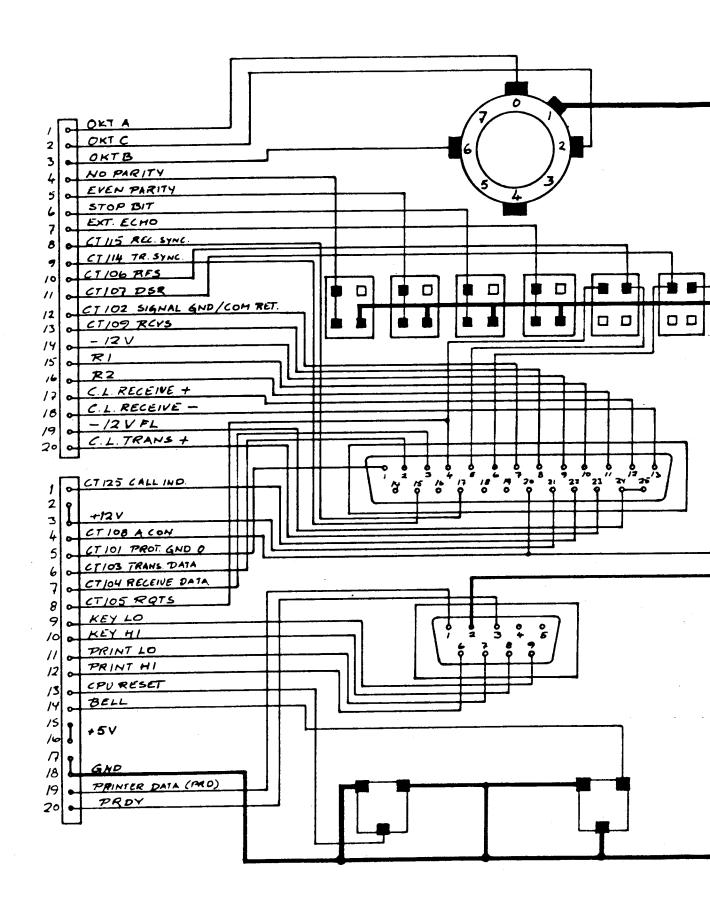
W7P1 CASSETTE CABLE

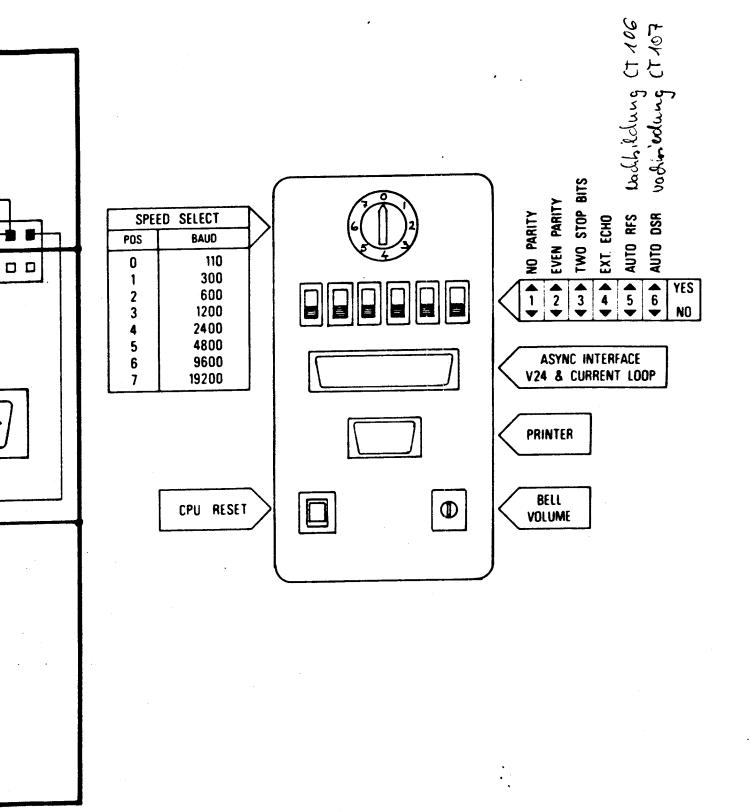
Pin no.	Colour	Goes to	Signal name
1		A3J1-1A	GND
2	,	" 1B	SLBC
3		" 2A	GND
4		" 2B	SLAC
5		" 3A	GND
6		" 3B	TRBC
7		" 4A	GND
8		" 4B	TRAC
9		" 5A	GND
10		" 5B	WENC
11		" 6A	GND
12		" 6B	WRDAT
13		/≏	GND
14		, , ,	WPS
15		l OA	GND DDS
16		" 8B " 9A	GND
17 18		" 9B	RD RD
18 19		" 10A	GND
20		" 10B	RCLK
21	.•	" 11A	GND
22	cable,grey.	" 11B	REVC
23	gr	" 12A	GND
24	Θ,	" 12B	FSTC
25	[ط ^د	" 13A	GND
26		" 13B	RUNC
27	at	" 14A	GND
28	Flat	" 14B	REWC
29	-	" 15A	GND
30		" 15B	UNLC
31		" 16A	GND
32		" 16B	RDYS
33		" 17A	GND
34		" 17B	,
35		" 18A	GND
36		" 18B	TPAS
37		" 19A	GND
38		" 19B " 203	TPBS
39		20A	GND
40		" 20B " 21A	CMID
41		" 21A " 21B	GND RUNS
42 43	İ	" 21B	GND
43		" 22B	CEXS
44		" 23A	GND
45 46		" 23B	GND
47	į	" 24A	GND
48		" 24B	
49		" 25A	GND
50		" 25B	

S + E out Bilds chivm computer bezogen

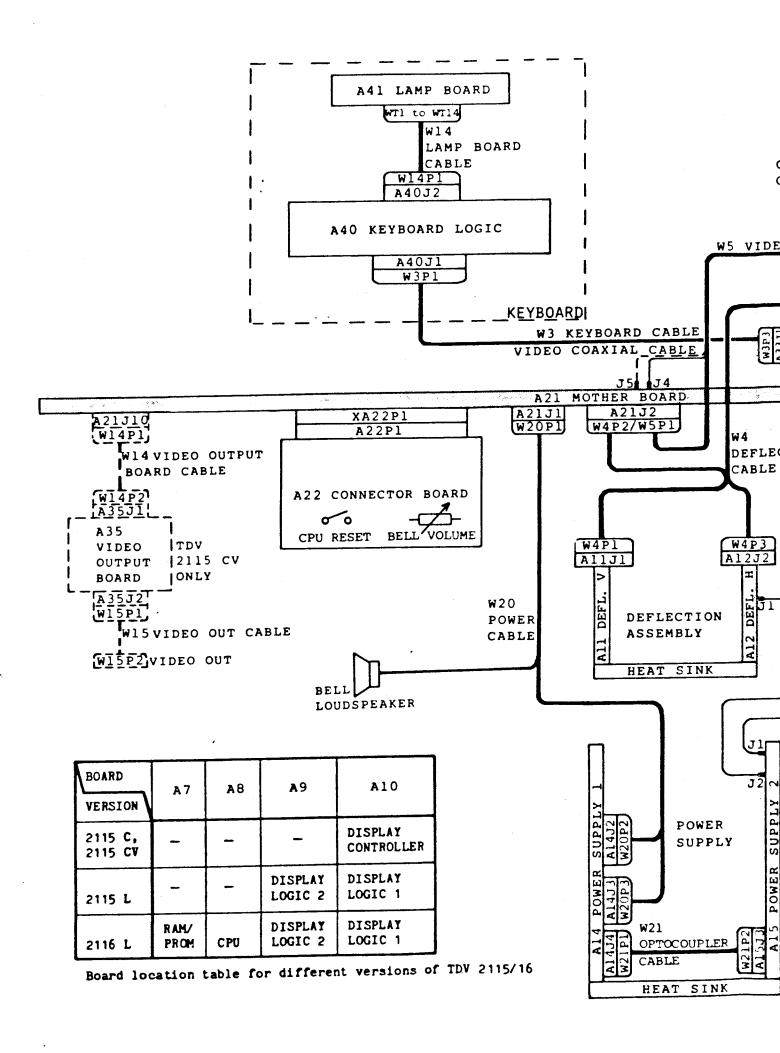


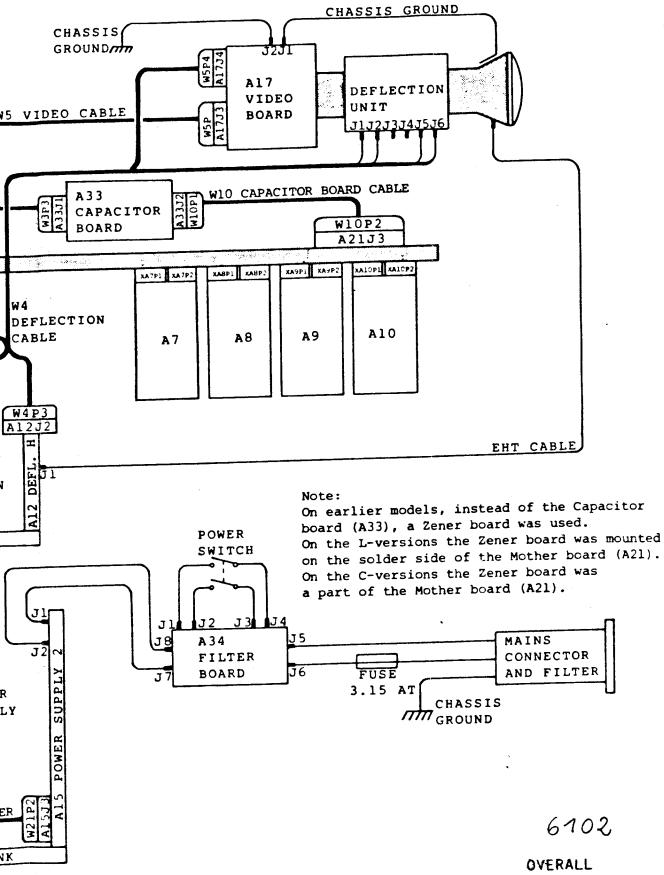
Für 6.610



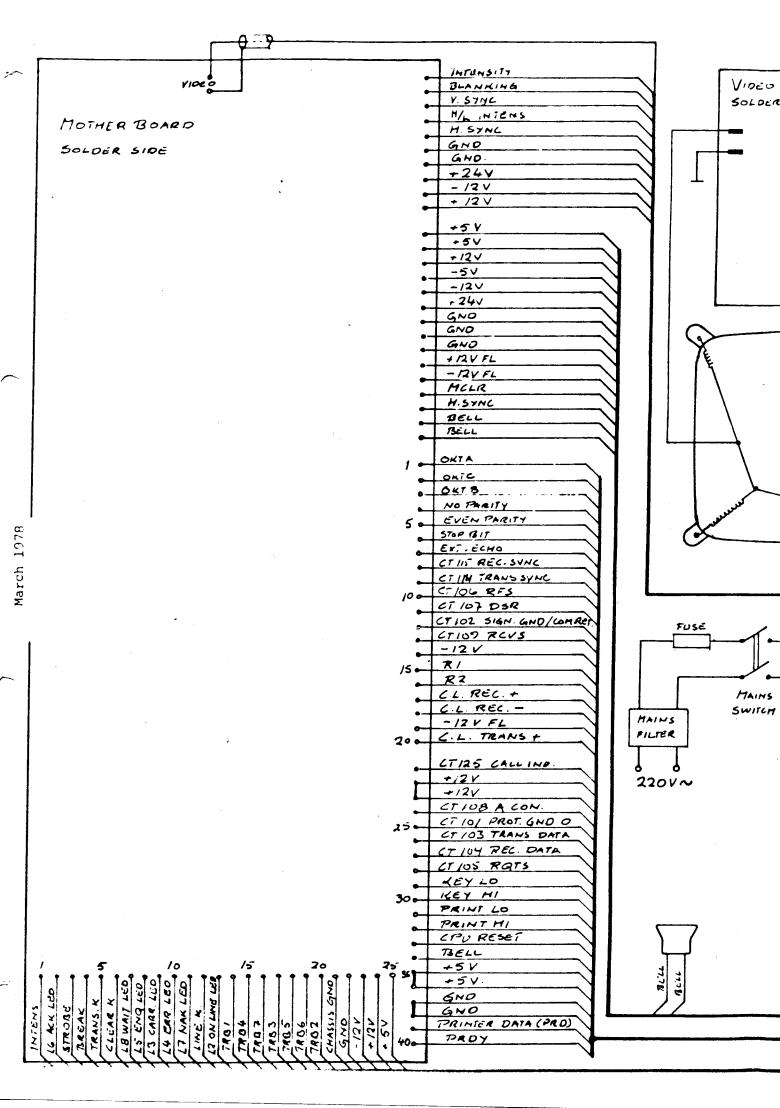


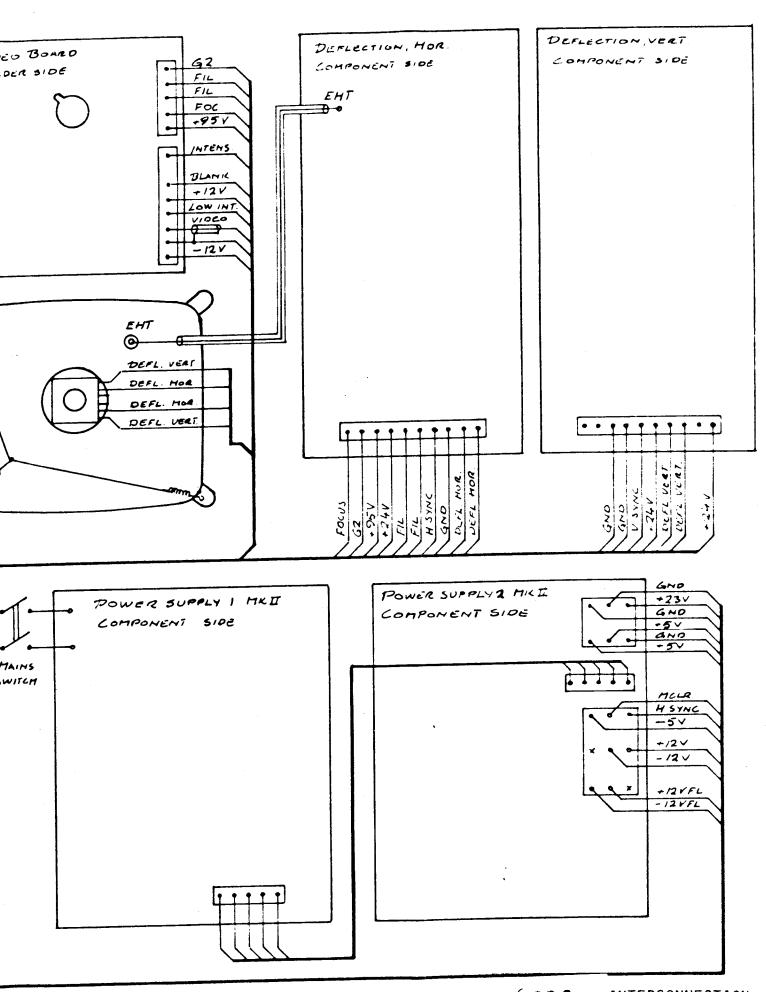
6102 CONNECTOR BOARD WIRING DIAGRAM AND BACK COVER SWITCHES





OVERALL
INTERCONNECTION
DIAGRAM December 1978





TO CONNECTOR BOARD

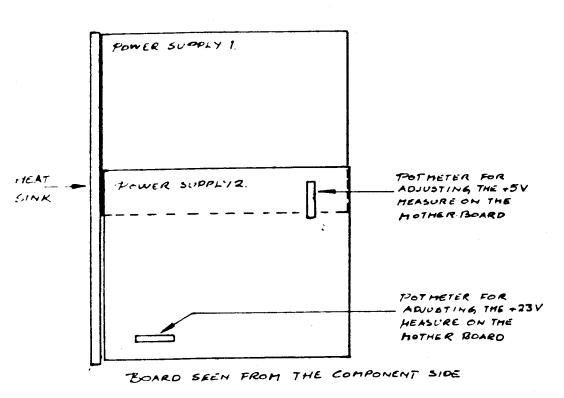
6702 DIAGRAM

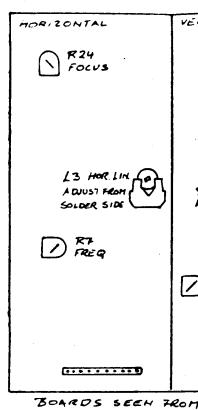
6102 INTERCONNECTION

TO KEYBOARD

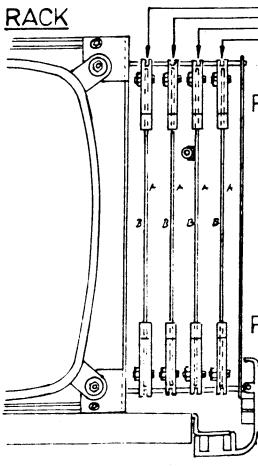
POWER SUPPLY

DEFLECTION





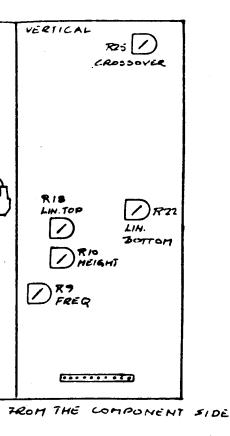
MOTHER BOARD INTENDITY RLANKING V. SYNK LOW INT. H. SYNC 1-54 +12V - 5 V - 12 V - 23V 0 0 GND 0 0 + 12V FL 0 - 12 V FL HCLR 0 HSYNC 0 LOUDSP BELL) 0 LOUDSP. (BELL)

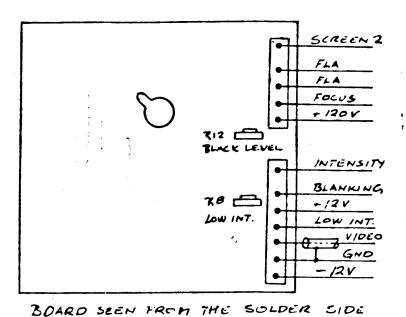


BOARD SCEN FROM THE COMPONENT SIDE

BOARD RACK SEEN FROM THE

VIDEO





MOTHER BOARD PIN CONFIGURATIONS

AND BOARD LOCATIONS

