# Properties of the Differential Amplifier

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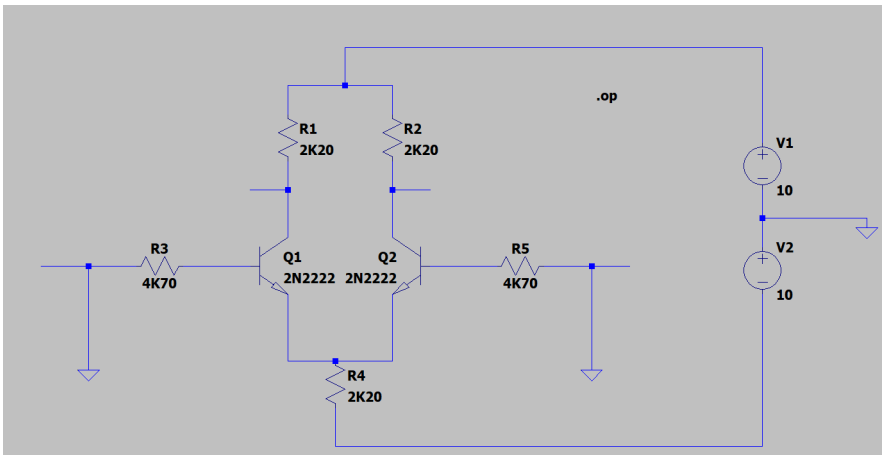
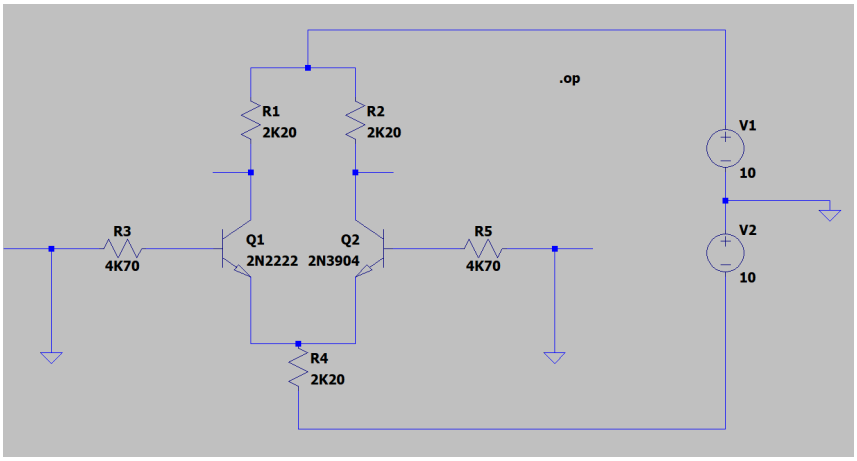
# 1 Introduction - Prelab

## 1.1 Simulation of a Differential Amplifier

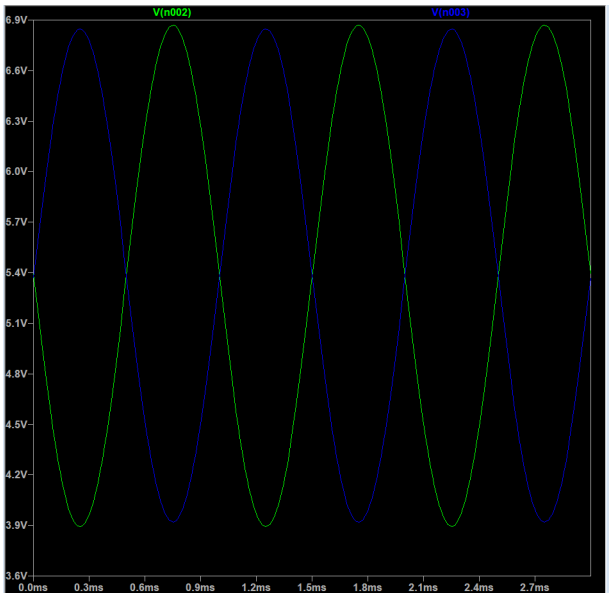
1. 

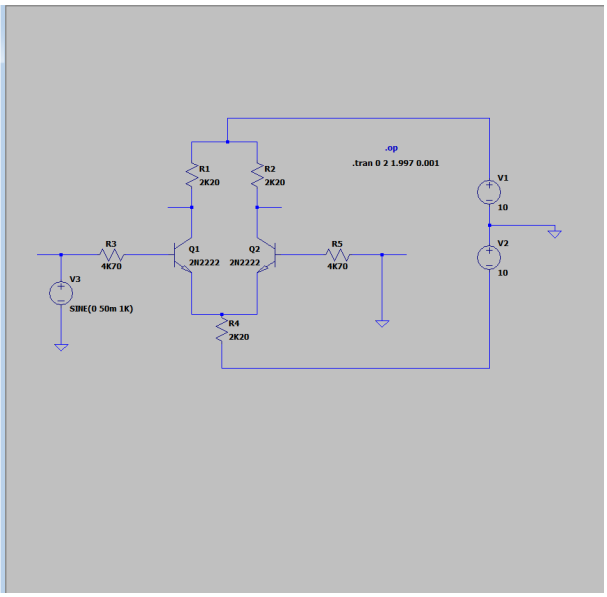

**Measured voltages and currents:**
$V_{BE}$ = -47.09 - (-720.71) = 767.8mV, $V_C$ = 5.382V, $I_C$ = 2.099mA, $I_E$ = 2.109mA, $I_{RE}$ = 4.219mA.




By changing one transistor the $V_{BE}$, $V_C$, $I_C$, $I_E$ values are not symmetric anymore (ex.: $V_C$(Q1) = 5.911V, $V_C$(Q2) = 4.837V), therefore the circuit cannot work properly.

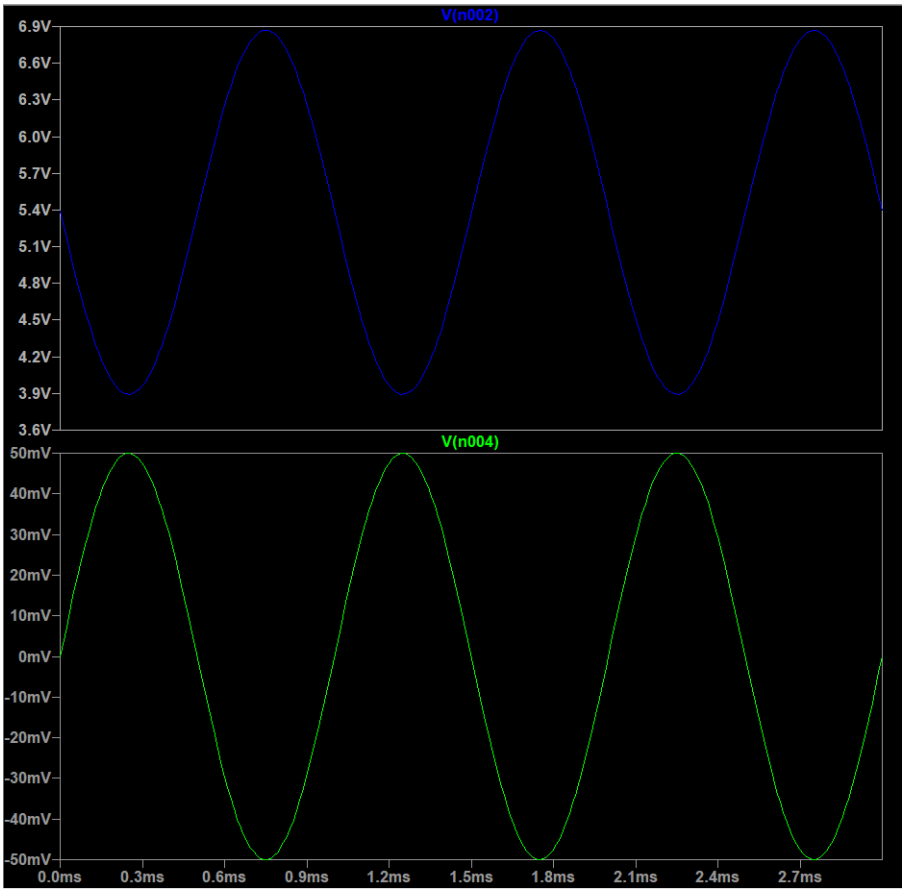
2. **Single ended input analysis**



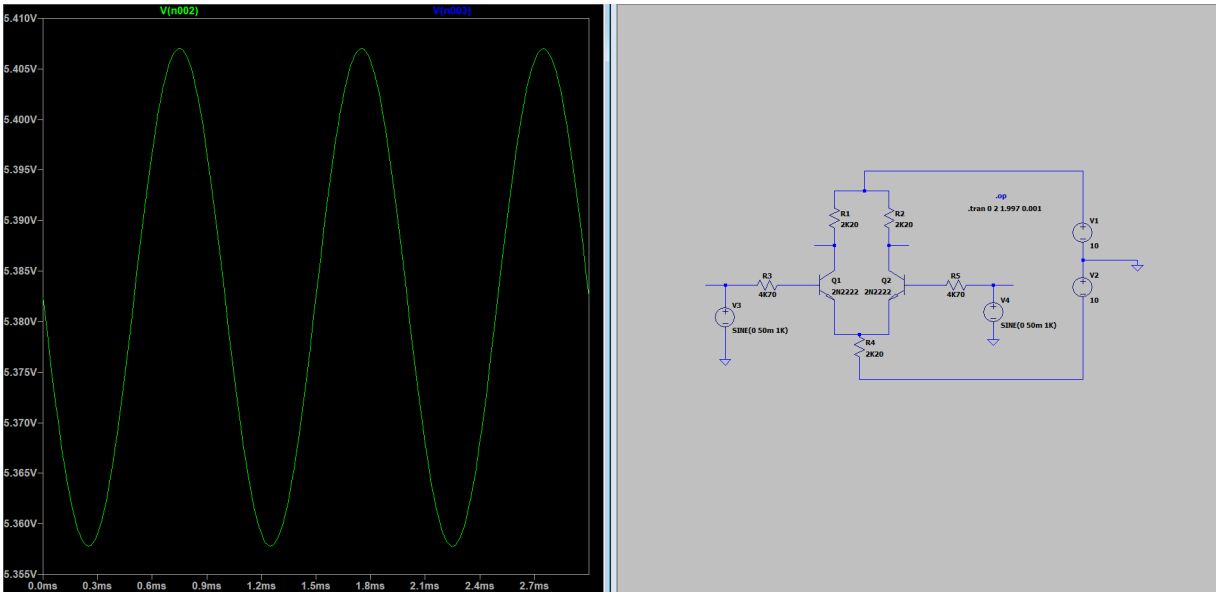

Green line: $V_C$(Q1), blue line: $V_C$(Q2). (peak to peak: 2.923V)

To calculate $A_{Vdiff}$ I need $V_{od}$ and $V_{id}$.

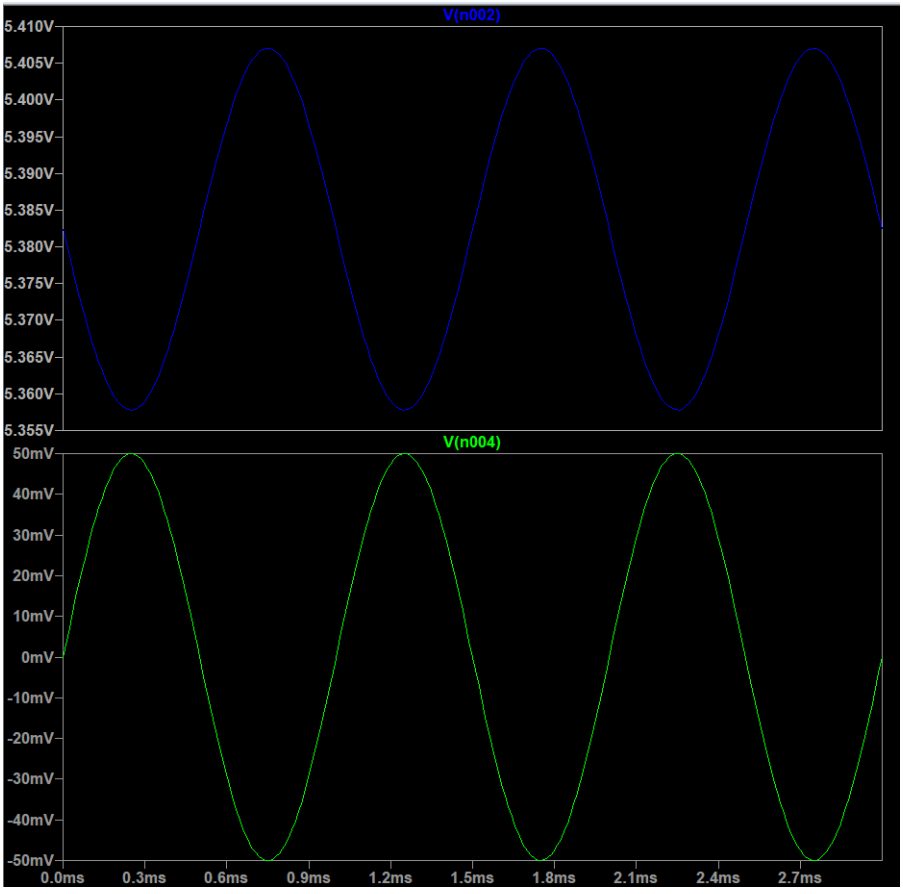



Top pane: $V_{o1}$, bottom pane: $V_{i1}$
$V_{id} = V_{i1} - V_{i2} = 100\text{mV}$ peak to peak
$V_{od} = V_{o1} = 3\text{V}$ peak to peak
$A_{Vdiff} = 20log(\frac{V_{od}}{V_{id}}) = 29.5$ dB.

3. **Common mode input analysis**




$V_C$(Q1) and $V_C$(Q2) are overlapping. (peak to peak: 49.17mV).
To calculate $A_{Vcm}$ I need $V_{oc}$ and $V_{ic}$.



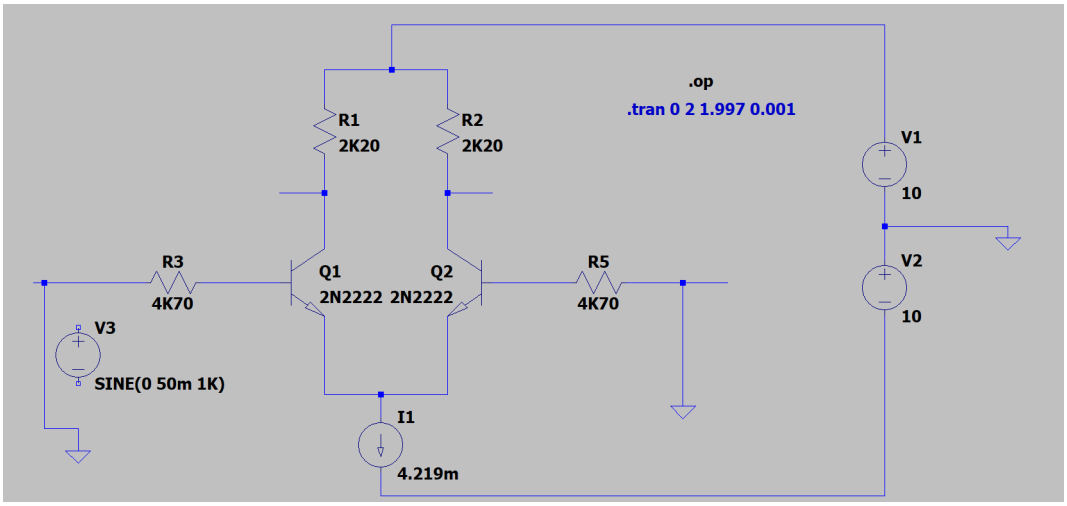

Top pane: $V_{o1}$, bottom pane: $V_{i1}$

$V_{ic} = (V_{i1} + V_{i2})/2 = 100$mV peak to peak
$V_{oc} = V_{o1} = 49.18$mV peak to peak
$A_{Vcm} = 20log(\frac{V_{oc}}{V_{ic}})$= -6.16 dB.

4. **Common mode rejection**

$CMRR = 20log(\frac{A_{Vdiff}}{A_{Vcm}})$= 35.7dB.
current source: 4.219 from top to bottom

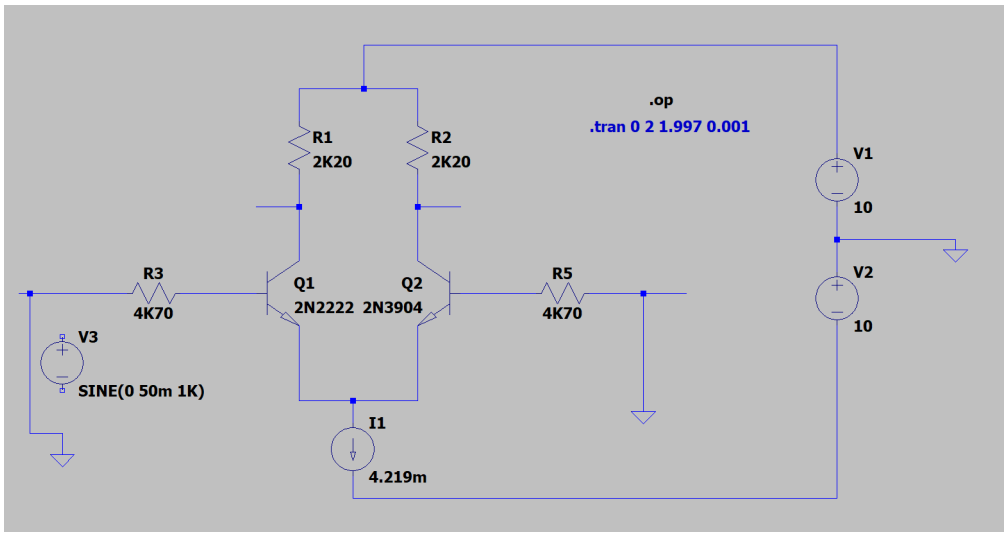
5. **Replacing R4 by equivalent current source**




6. **Analyses using the current source**

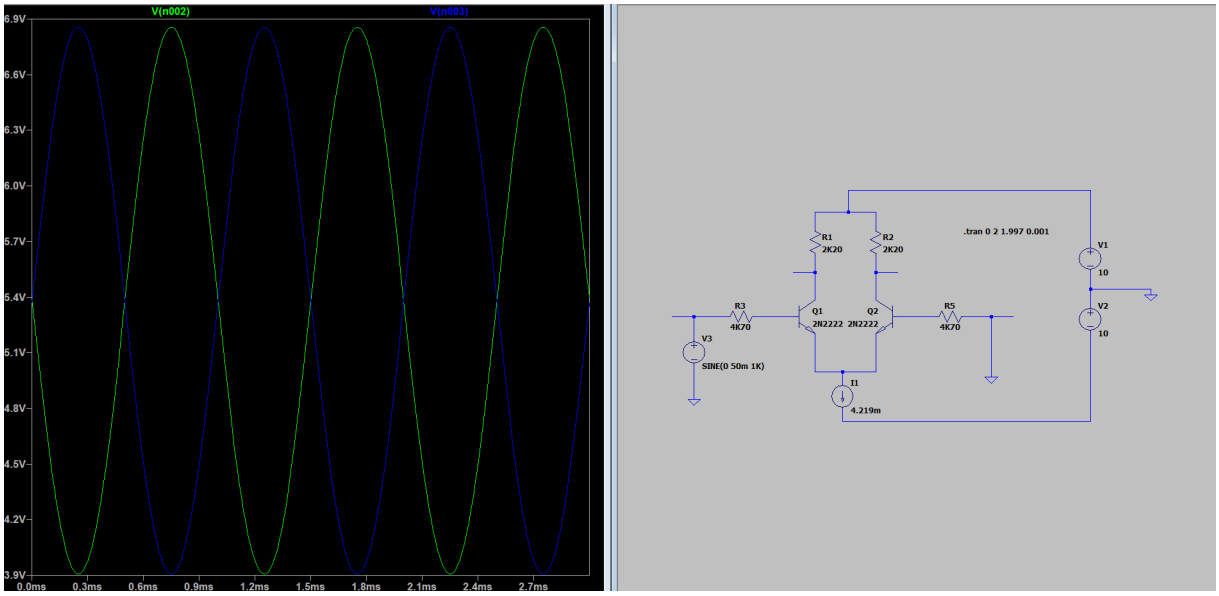
   (a) **DC operation point analysis**

   $V_{BE}$ = -47.11 - (-720.74) = 767.85mV, $V_C$ = 5.381V, $I_C$ = 2.099mA, $I_E$ = 2.109mA, $I_{RE}$ = 4.219mA. (current source)



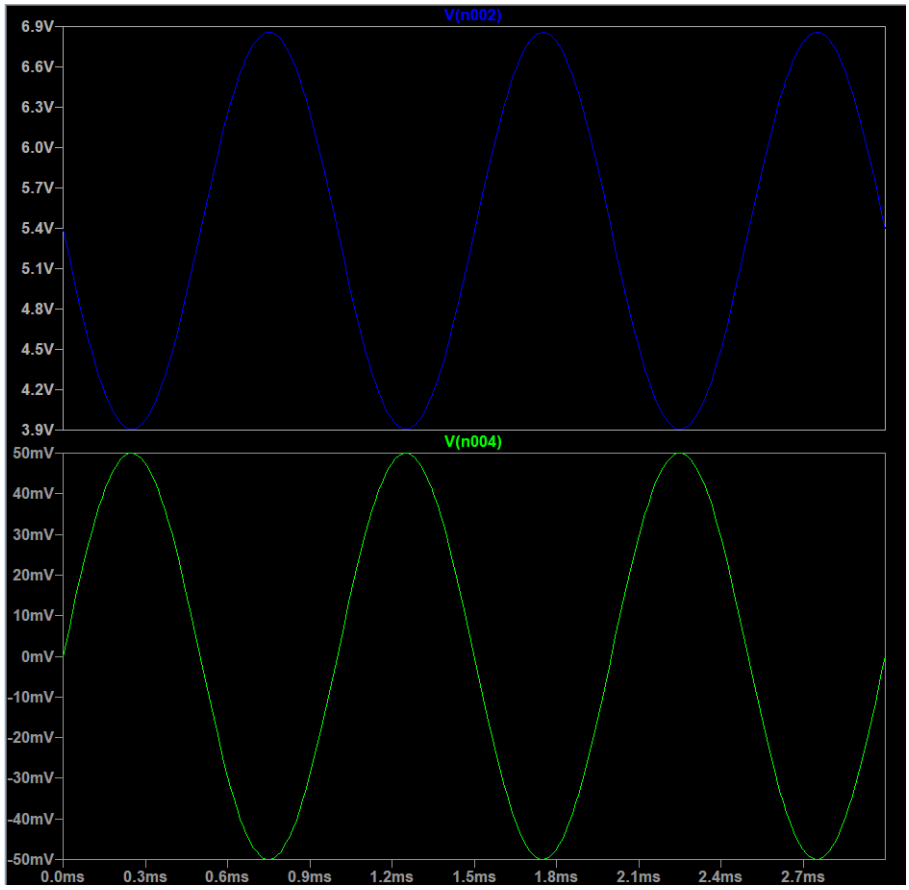

   By changing one transistor the $V_{BE}$, $V_C$, $I_C$, $I_E$ values are not symmetric anymore (ex.: $V_C$(Q1) = 5.913V, $V_C$(Q2) = 4.841V), therefore the circuit cannot work properly.

(b) **Single ended input analysis**



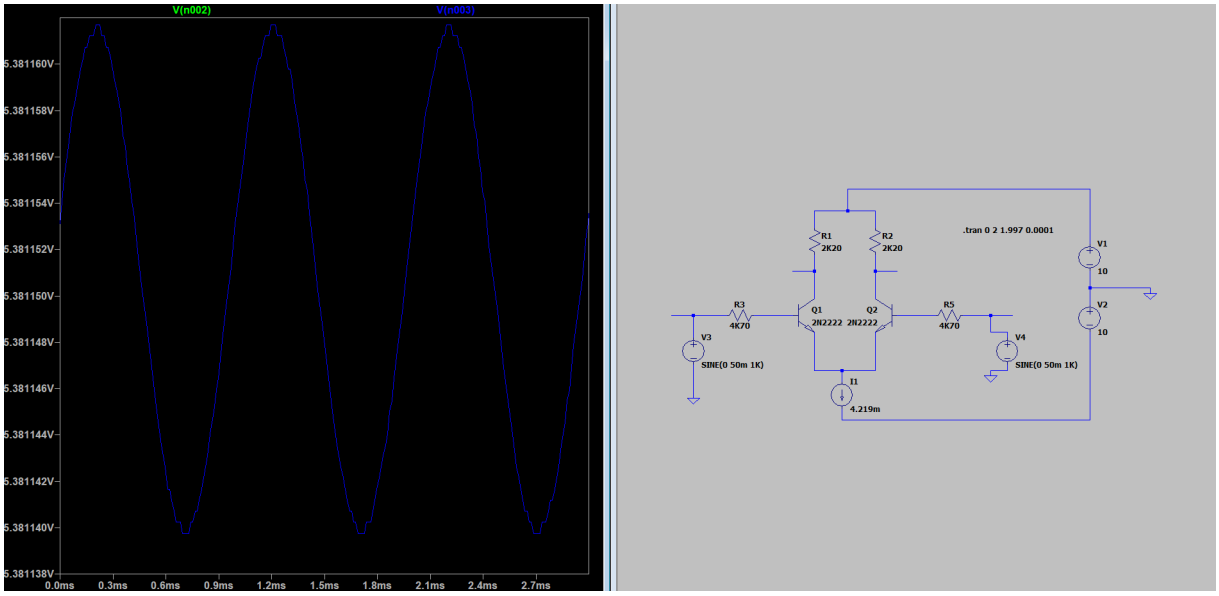

Green line: $V_C$(Q1), blue line: $V_C$(Q2). (peak to peak: 2.95V)

To calculate $A_{Vdiff}$ I need $V_{od}$ and $V_{id}$.



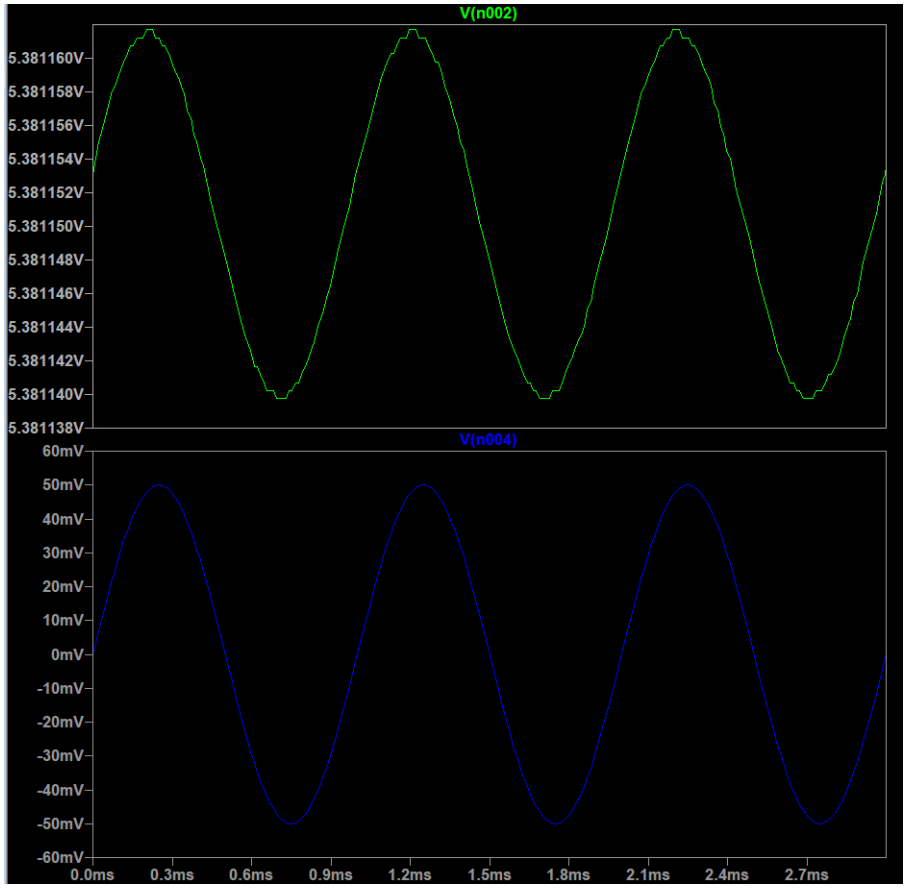

Top pane: $V_{o1}$, bottom pane: $V_{i1}$
$V_{id} = V_{i1} - V_{i2} = 100$mV peak to peak
$V_{od} = V_{o1} = 2.95$V peak to peak
$A_{Vdiff} = 20log(\frac{V_{od}}{V_{id}})= 29.4$ dB.

(c) **Common mode input analysis**




$V_C$(Q1) and $V_C$(Q2) are overlapping. (peak to peak: 21.93$\mu$V).

To calculate $A_{Vcm}$ I need $V_{oc}$ and $V_{ic}$.




Top pane: $V_{o1}$, bottom pane: $V_{i1}$

$V_{ic} = (V_{i1} + V_{i2})/2 = 100$mV peak to peak
$V_{oc} = V_{o1} = 21.93\mu$V peak to peak
$A_{Vcm} = 20log(\frac{V_{oc}}{V_{ic}})$= -73.28 dB.

(d) **Common mode rejection**

$CMRR = 20log(\frac{A_{Vdiff}}{A_Vcm})$= 102.6dB.

# 2 Experimental Set-up and Results

## 2.1 Differential amplifier using a fixed emitter resistor

1. Experimental DC bias values: $V_B(T_1, T_2)$= 5.680V, $V_B(T_1, T_2)$= 45.6mV, $V_{BE}(T_1, T_2)$= 634.1mV, $I_{RE}$ = 1.93mA. Some reasons for the differences between the simulated values and the measured ones could be the following:

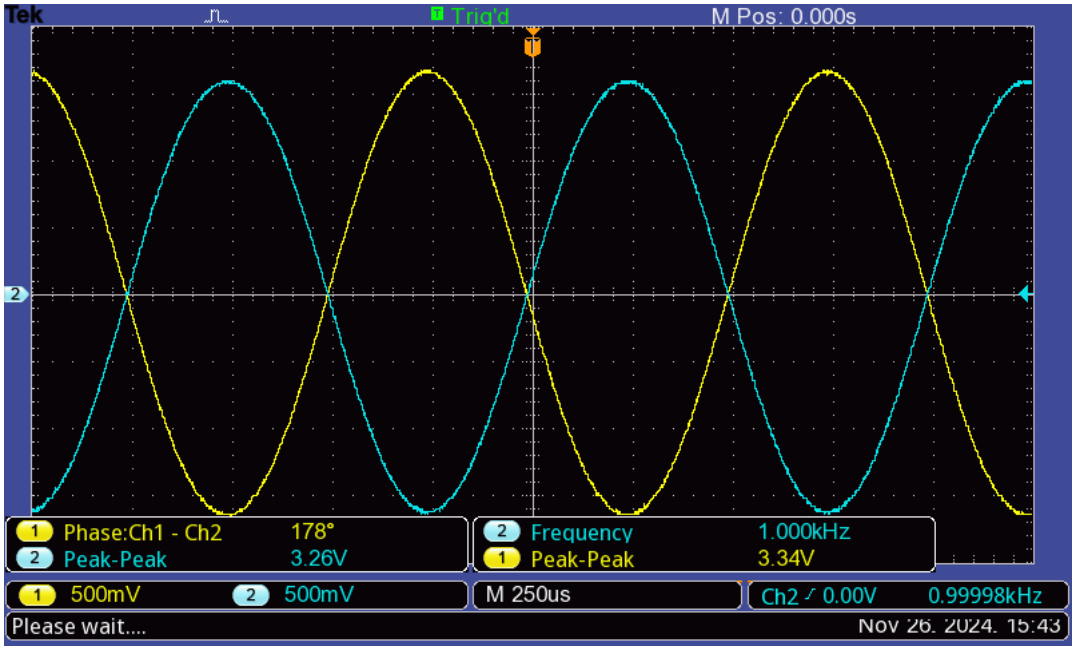
   (a) Transistor calibration: the bjts in the simulation are identical while, on the experiment, the two bjts used are sold in multiple numbers and not calibrated to be pairs as identical as possible.

   (b) Temperature difference: the most temperature sensitive voltages (ex: $V_{BE}$) could be different since the ambient temperature in the lab is not monitored while the assumed temperature in the simulation is always 25°C.

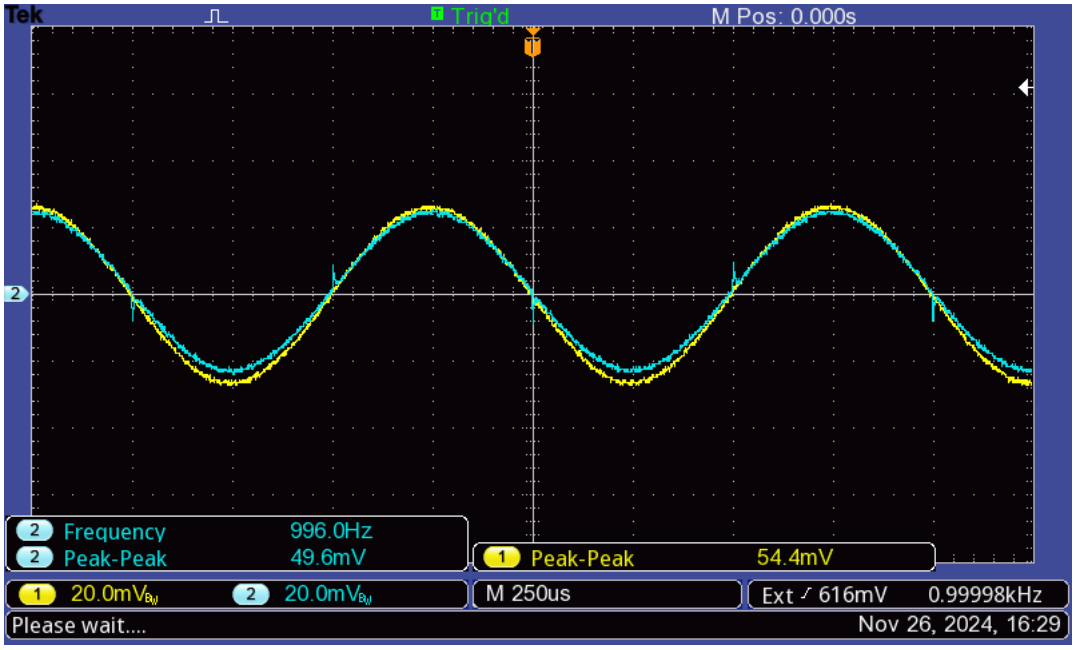
   (c) Parasitic Effects: using a breadboard, there could be parasitic capacities and resistances due to the prototypical wiring and the fact that used resistors are not precise and could have induced some imbalances in the supposed symmetric circuit.

2. **CMRR calculation**

Output voltage in single ended mode:




Output voltage in common mode:




Since the input is 100mV peak to peak

$V_{vdm} = 20log\frac{3300}{100} = 30.4\text{dB}$

$V_{vcm} = 20log\frac{51.5}{100} = \text{-}5.76\text{dB}$

$\text{CMRR} = 20log\frac{V_{vdm}}{V_{vcm}} = \frac{\frac{3300}{100}}{\frac{51.5}{100}} = 36.1\text{dB}$

## 2.2 Differential amplifier using a current source

1. Experimental DC bias values: $V_B(T_1, T_2)$= 5.612V, $V_B(T_1, T_2)$= 0.040V, $V_{BE}(T_1, T_2)$= 0.63V, $I_C(T_1, T_2)$= 2.08mA, $I_{RE}$ = 3.92mA.
   Some reasons for the differences between the simulated values and the measured ones could be the following:

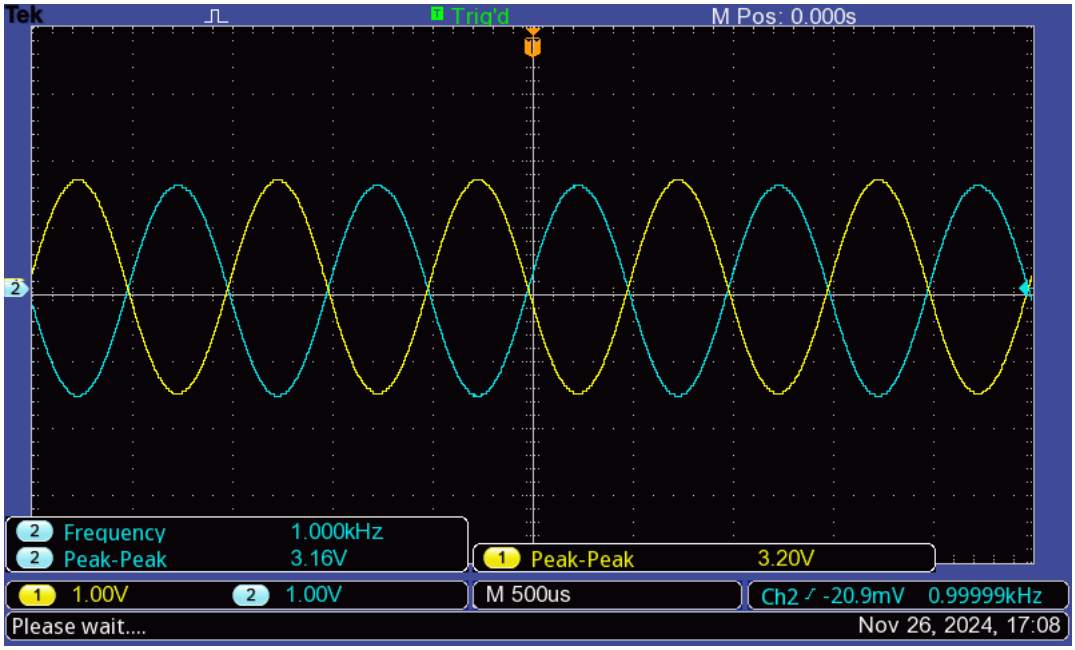
   (a) Transistor calibration: the bjts in the simulation are identical while, on the experiment, the two bjts used are sold in multiple numbers and not calibrated to be pairs as identical as possible.

   (b) Temperature difference: the most temperature sensitive voltages (ex: $V_{BE}$) could be different since the ambient temperature in the lab is not monitored while the assumed temperature in the simulation is always 25°C.

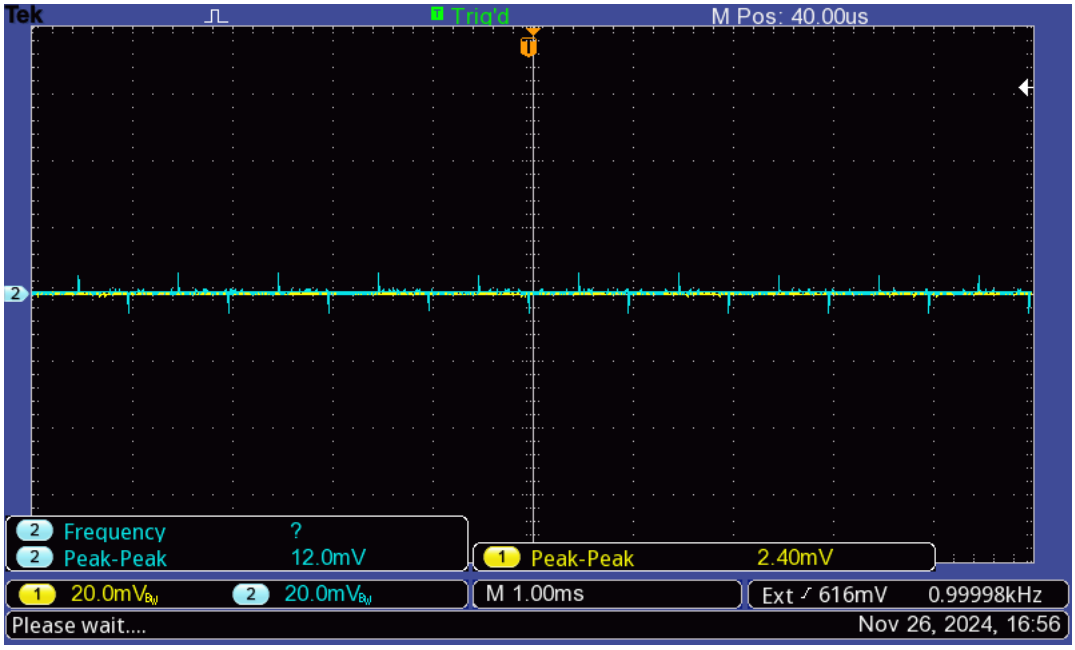
   (c) Parasitic Effects: using a breadboard, there could be parasitic capacities and resistances due to the prototypical wiring and the fact that used resistors are not precise (ex: R1 in the current source circuit was supposed to be 530Ω but we used a 530Ω one) and could have induced some imbalances in the supposed symmetric circuit.

2. **CMRR calculation**

Output voltage in single ended mode:




Output voltage in common mode:




The output voltage in common mode is too small to be precisely measured by the oscilloscope, for the calculation I'll use the simulated value instead (21.93$\mu$V peak to peak).

Since the input is 100mV peak to peak

$V_{vdm} = 20log\frac{3180}{100} = 30.05\text{dB}$

$V_{vcm} = 20log\frac{0.0219}{100} = -73.2\text{dB}$

$\text{CMRR} = 20log\frac{V_{vdm}}{V_{vcm}} = \frac{\frac{3180}{100}}{\frac{0.0219}{100}} = 83.2\text{dB}$

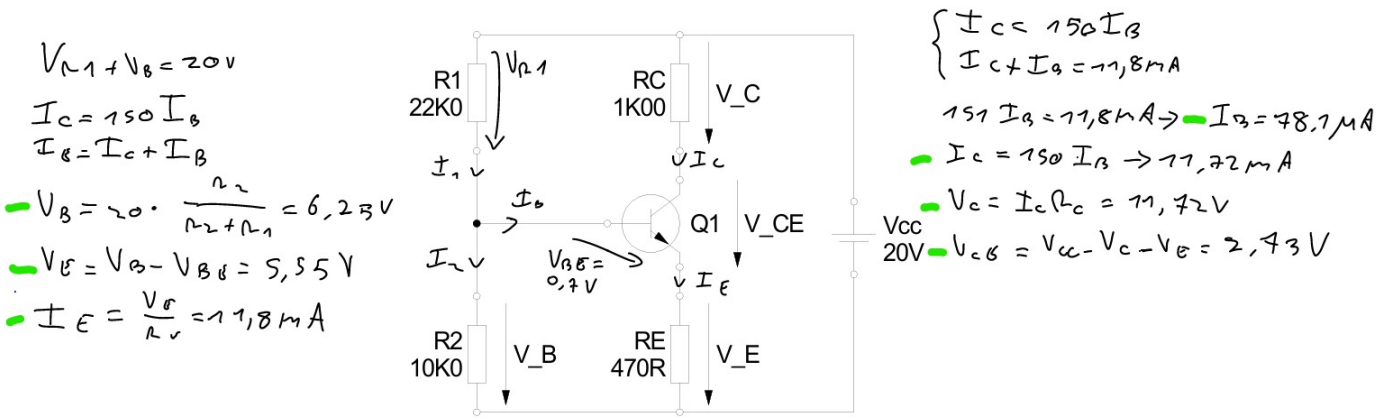
3. **Performance comparison**

While using a fixed emitter resistor the differential voltage gain is almost the same as when using a current source (30.4dB vs 30.5dB), the common mode rejection ratio is around 224 times bigger when using a fixed current source (36.1dB vs 83.2dB).

# 3 Lab 3 Prelab

## 3.1 Biasing of Bipolar Junction Transistor

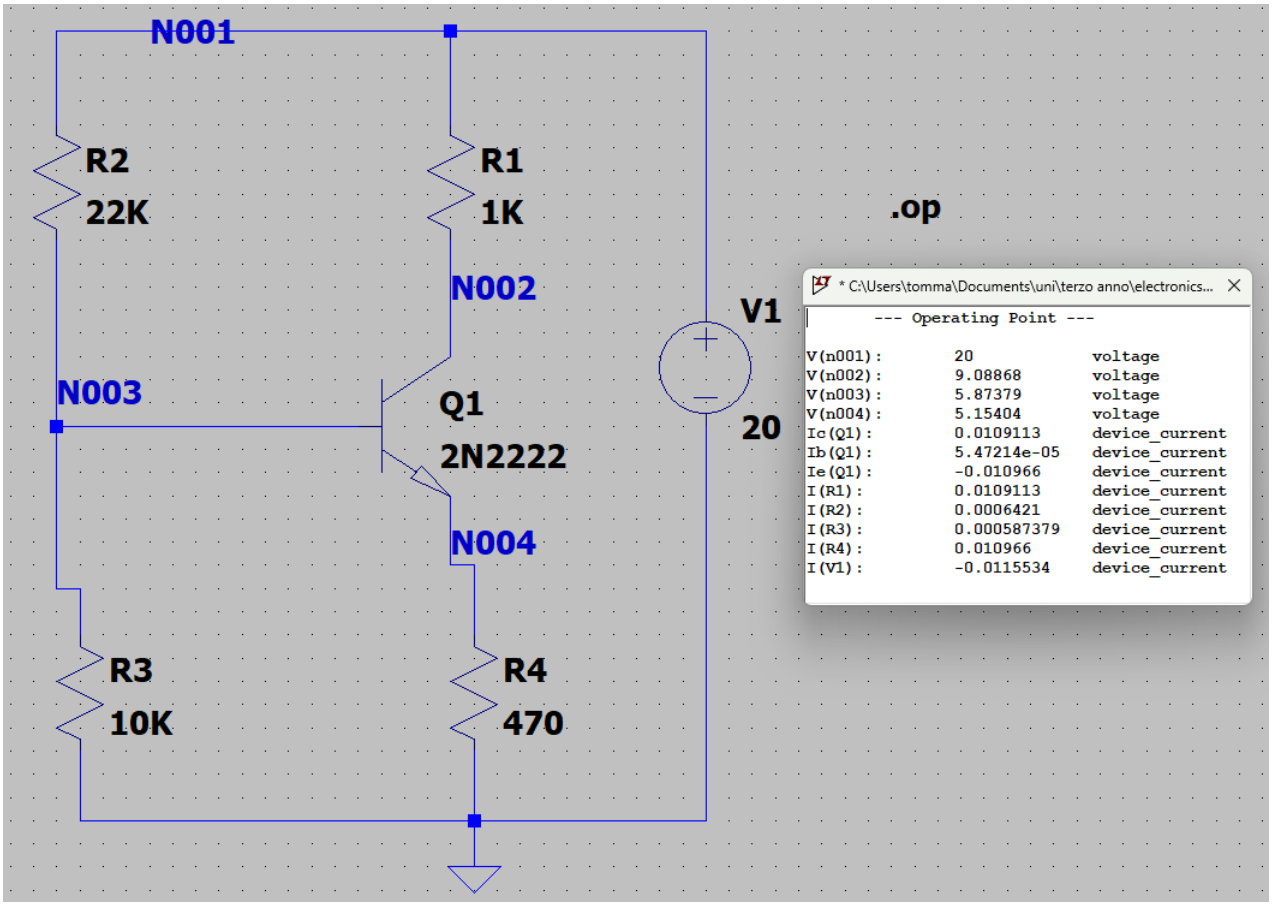
1. **Calculations**




$\beta = 150$ and $V_{BE} = 0.7\,\text{V}$

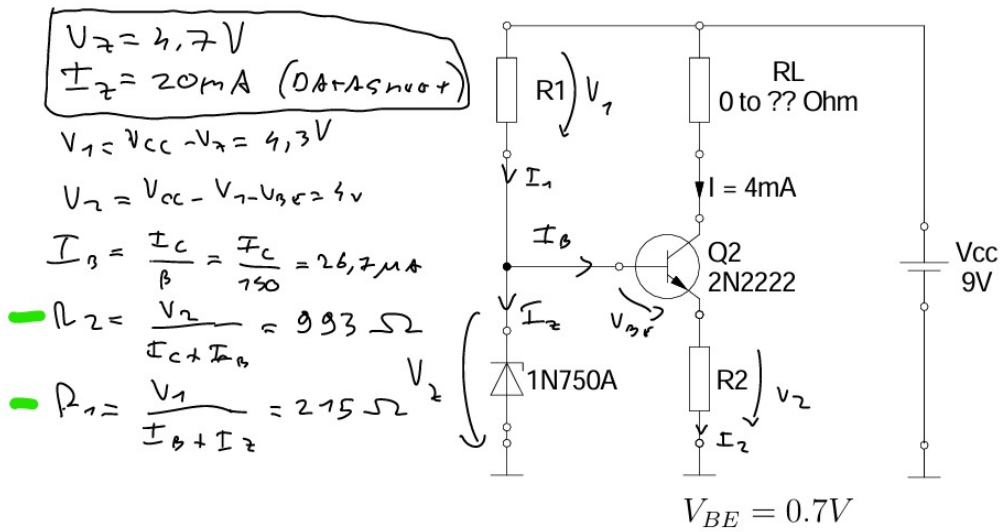
1. (a) Calculate $V_B$, $V_E$, $V_{CE}$, and $V_C$.
   (b) Calculate $I_B$, $I_E$, and $I_C$.

**LTSpice simulation**

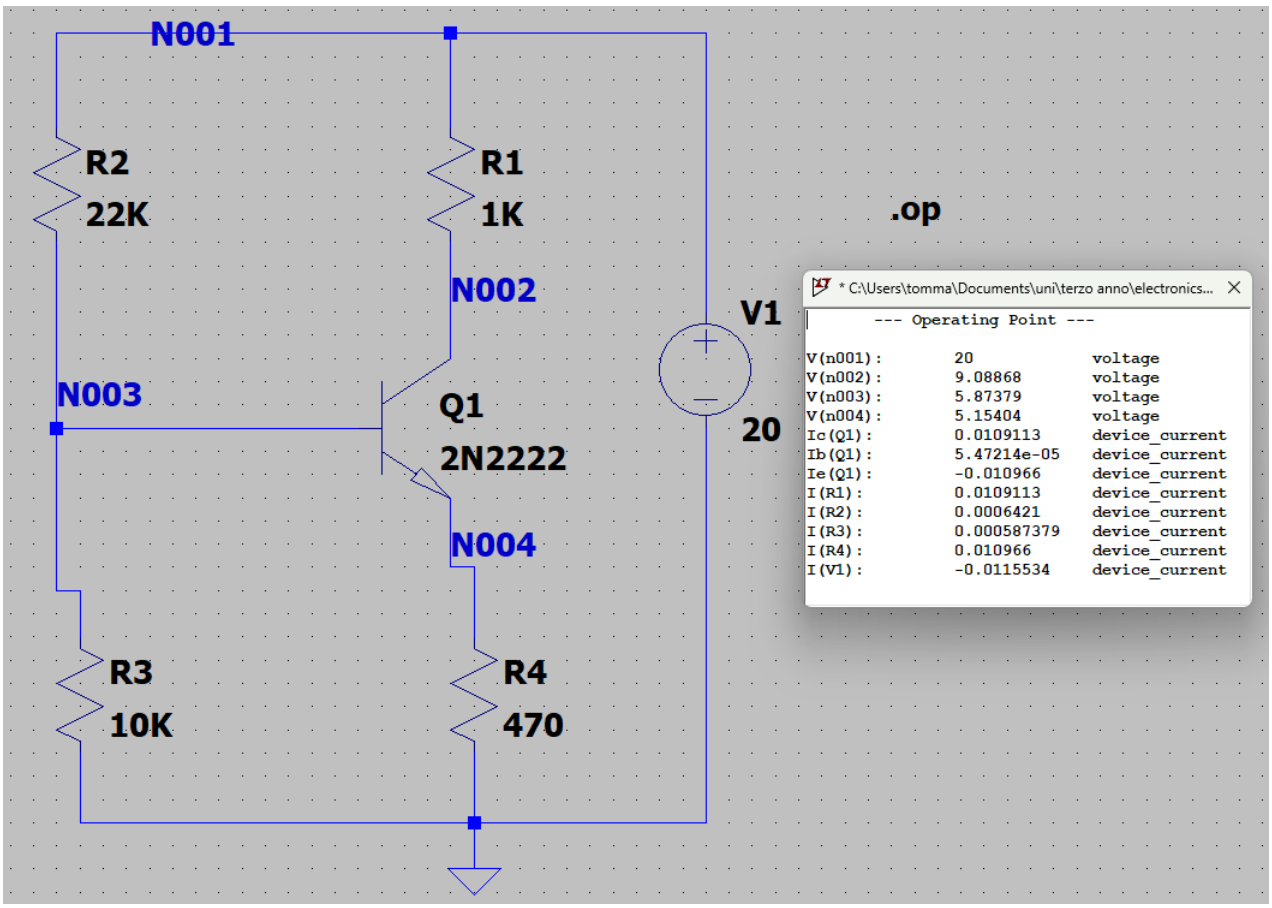


## 3.2 Constant Current Source

1. **Calculations and simulation on LTSpice**

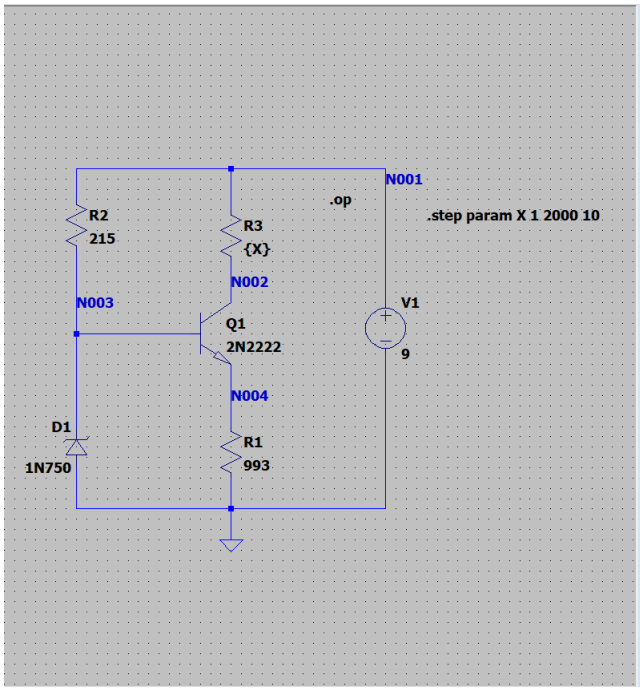


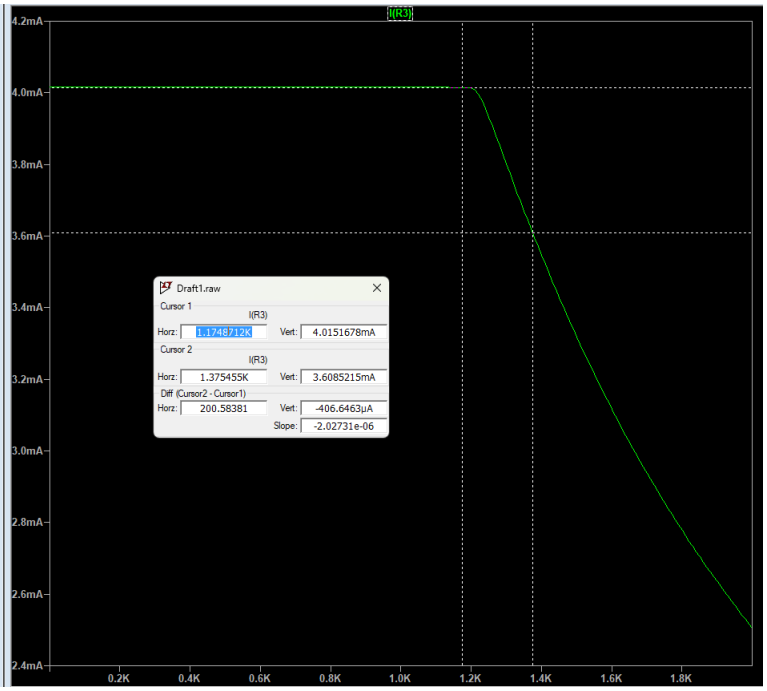

2. R1 = 215Ω, R2 = 993Ω




3. To have a constant current $V_{CE}$ has to be higher than 0.3V (from 2N2222 datasheet) to stay in active mode. So the condition for RL is $V_{RL} < V_{CC} - 0.3V - V_2 = V_{RL} < 4.7V$ so $R_L$ must be lower than $\frac{4.7}{0.004} = 1175\ \Omega$.

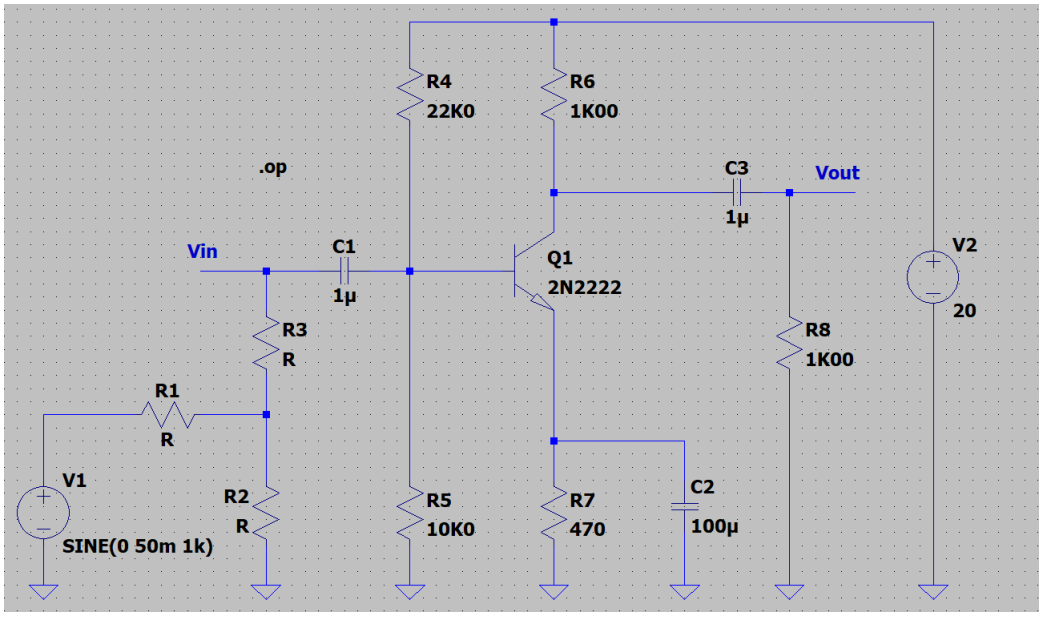
4. **Max $R_L$ in LTSpice**




At 1275Ω the current is 4mA, at 1375Ω the current is 10% less (3.6mA).

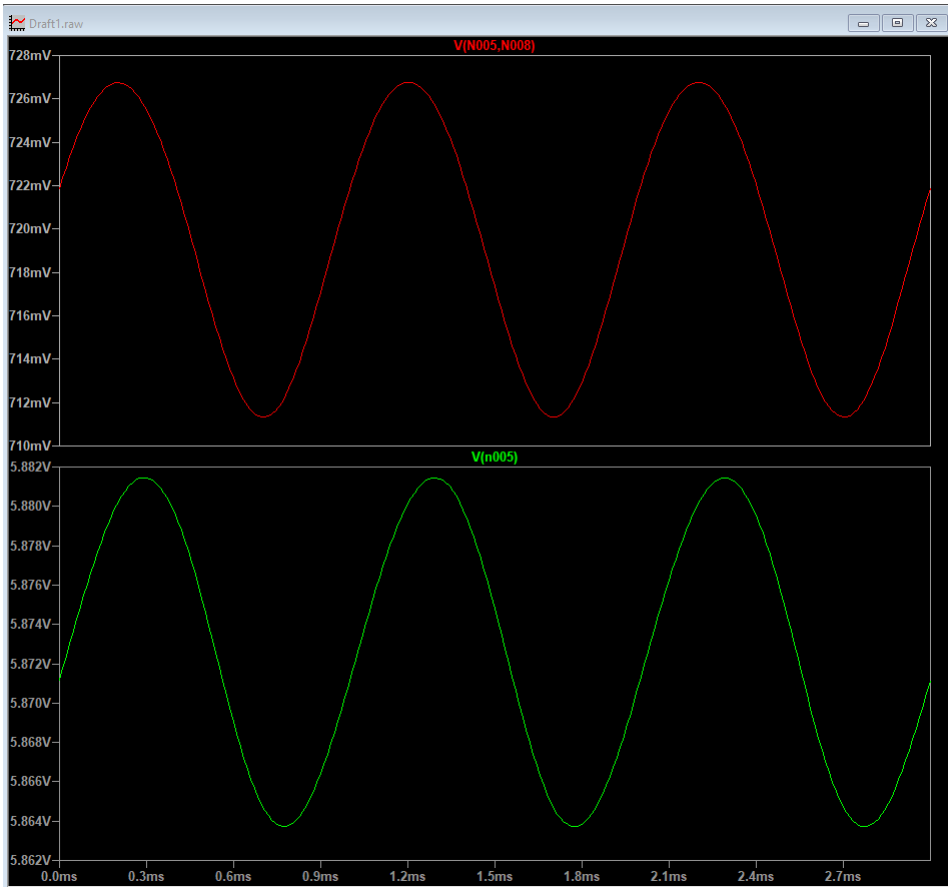
## 3.3 Amplifier circuit

1. 

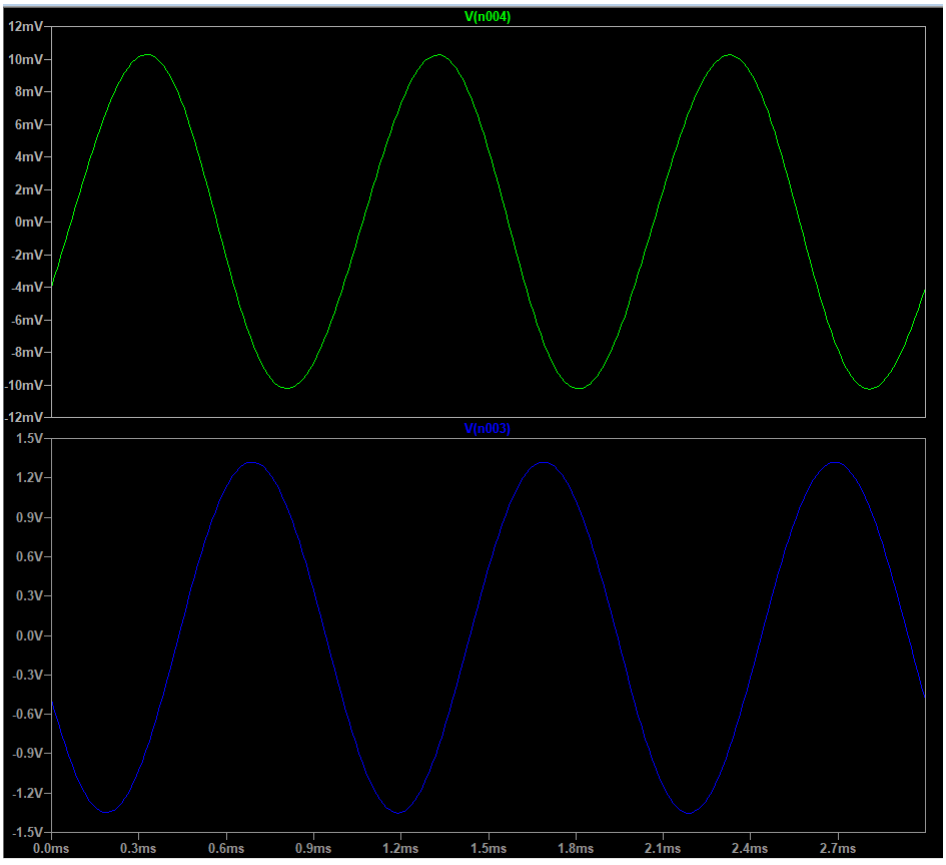

2. **DC operation point values**

$I_C = 0.011$ A, $I_B = 54.7$ uA
$V_B = 5.87$V, $V_E = 5.15$ V, $V_C = 9.09$V, $V_BE = 0.12$, $V_CE = 3.94$V

3. **Transient analysis at 50mV**



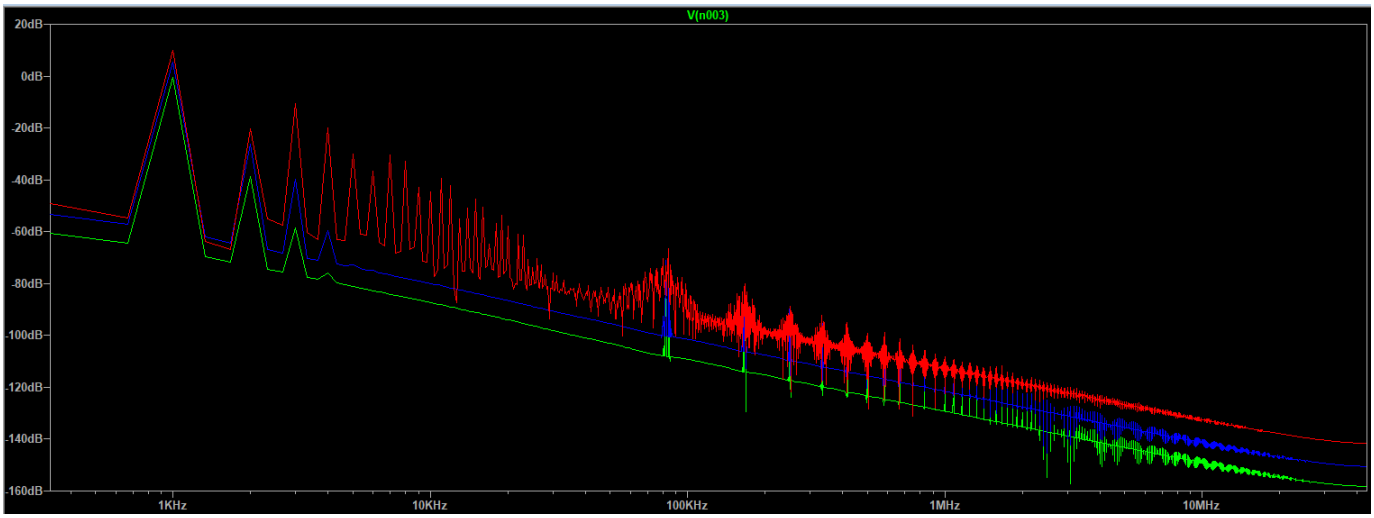

Green line: $V_B$: 17.7mV peak to peak, red line: $V_{BE}$: 15.4mV peak to peak.




Green line: $V_i$: 20.5mV peak to peak, blue line: $V_o$: 2.67V.

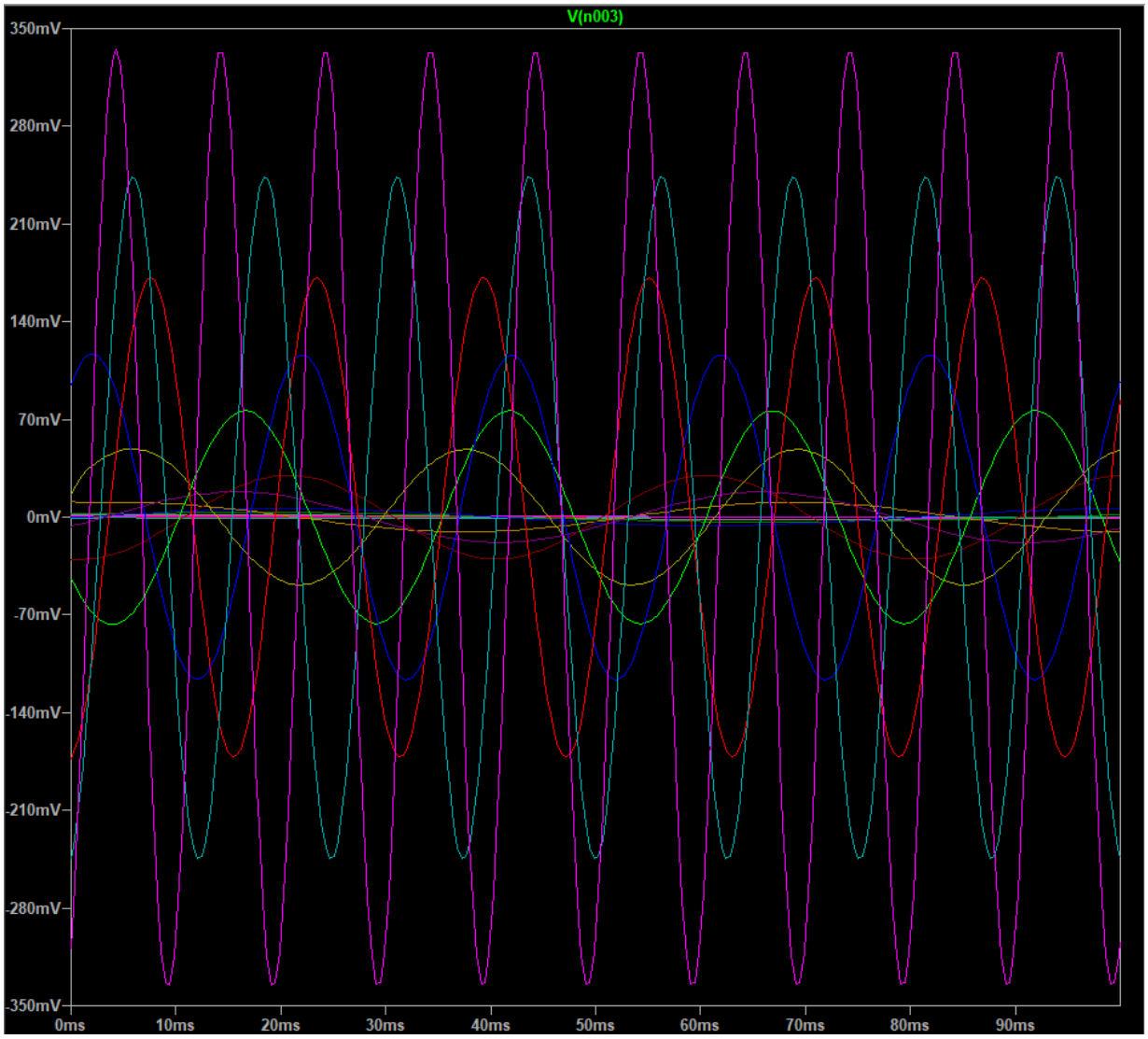
Gain: $\frac{V_o}{V_i} = 130$.

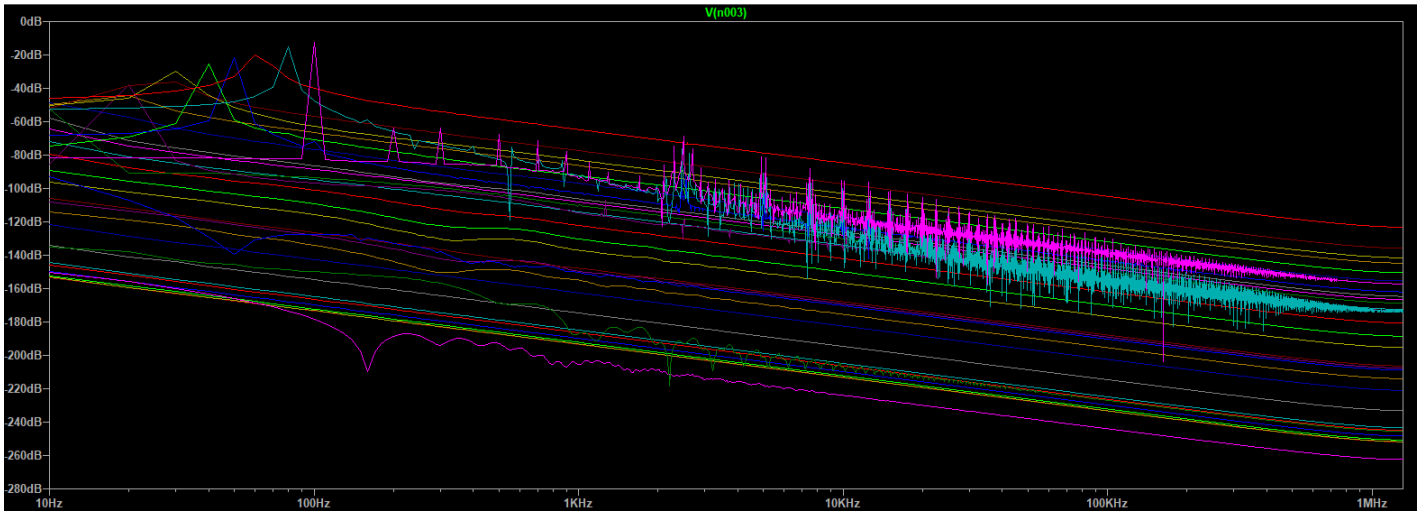
4. **Harmonic distortion analysis**




According to the FFT the harmonic distortion is similar between 50mV and 100mV as input amplitude and is much worse when using 200mV.

5. **AC analysis**




6. **Bandwidth measurement**

Lower -3dB frequency: 326.2 Hz
Upper -3dB frequency: 479.5 kHz
Bandwidth: 479.3 kHz