

# Diode

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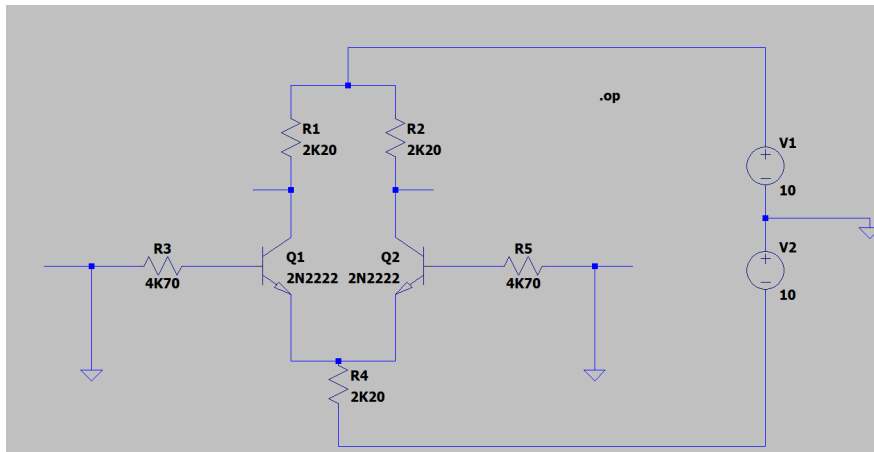
Instructor Uwe Pagel

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# 1 Introduction - Prelab

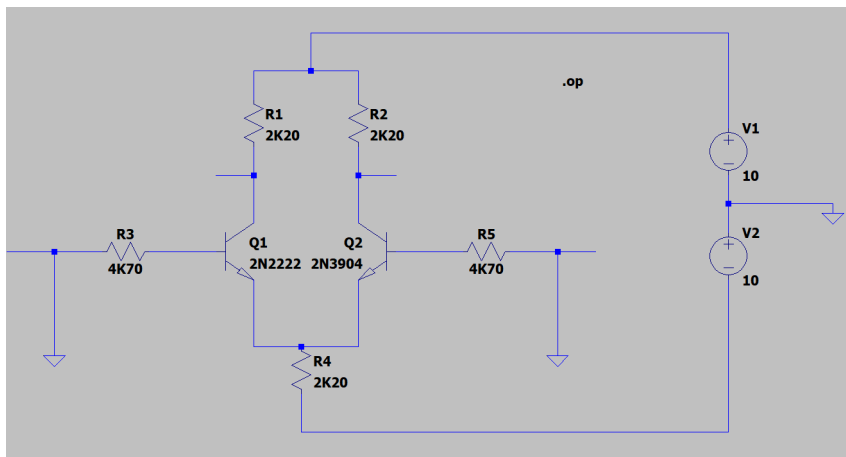
## 1.1 Simulation of a Differential Amplifier

1.



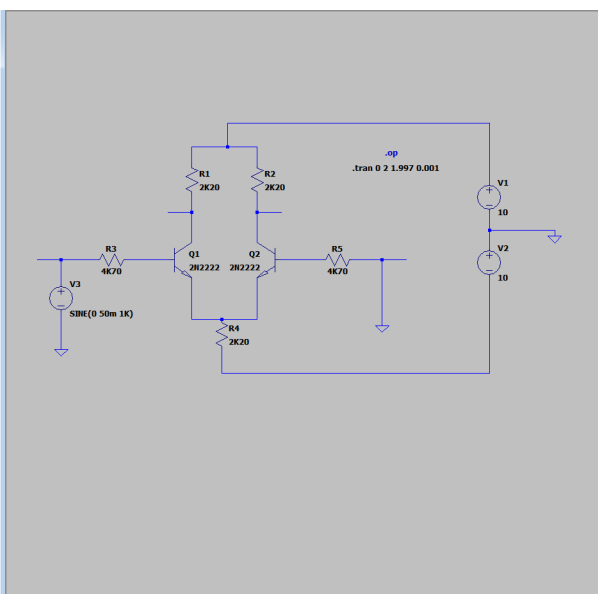
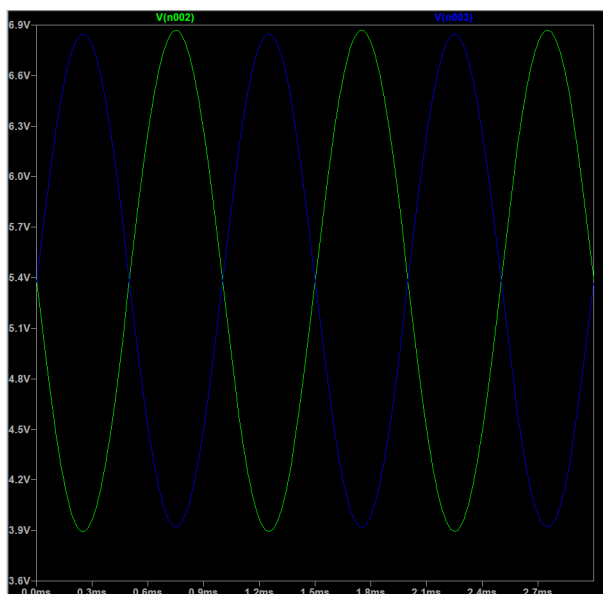
**Measured voltages and currents:**

$V_{BE} = -47.09 - (-720.71) = 767.8\text{mV}$ ,  $V_C = 5.382\text{V}$ ,  $I_C = 2.099\text{mA}$ ,  $I_E = 2.109\text{mA}$ ,  $I_{RE} = 4.219\text{mA}$ .



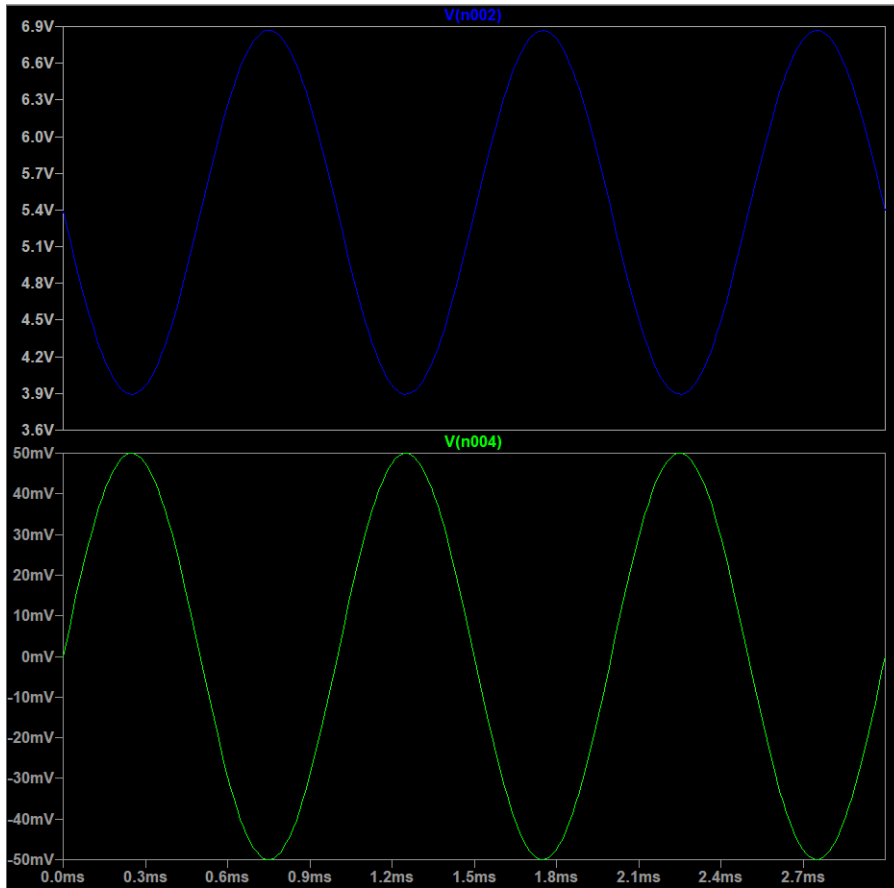
By changing one transistor the  $V_{BE}$ ,  $V_C$ ,  $I_C$ ,  $I_E$  values are not symmetric anymore (ex.:  $V_C(Q1) = 5.911\text{V}$ ,  $V_C(Q2) = 4.837\text{V}$ ), therefore the circuit cannot work properly.

## 2. Single ended input analysis



Green line:  $V_C(Q1)$ , blue line:  $V_C(Q2)$ . (peak to peak: 2.923V)

To calculate  $A_{V_{diff}}$  I need  $V_{od}$  and  $V_{id}$ .



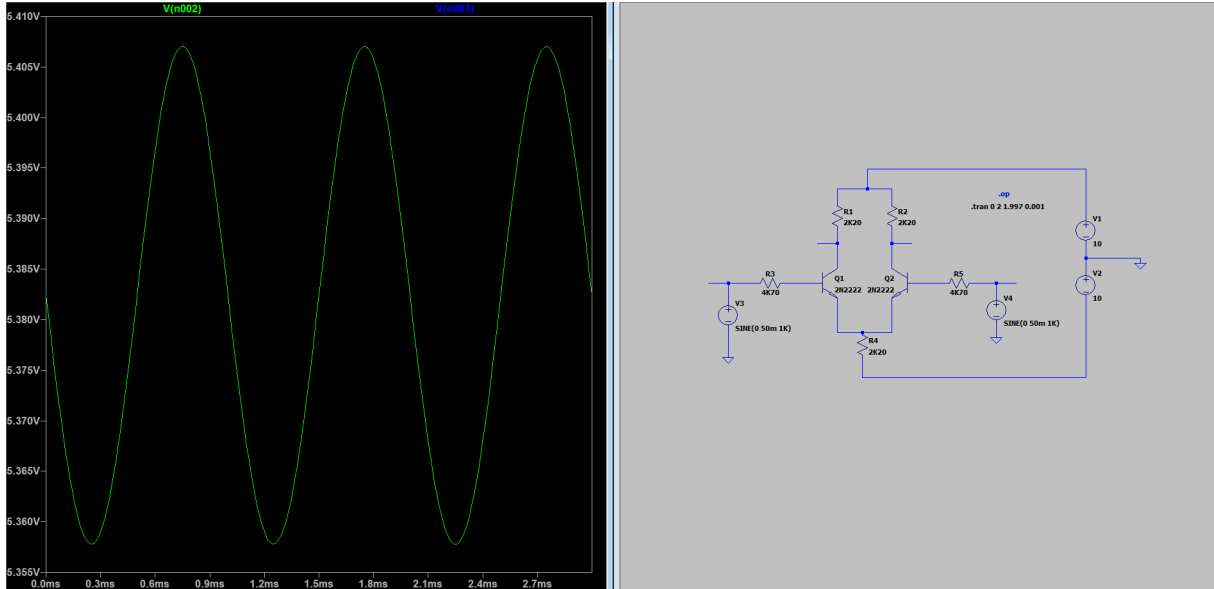
Top pane:  $V_{o1}$ , bottom pane:  $V_{i1}$

$V_{id} = V_{i1} - V_{i2} = 100\text{mV}$  peak to peak

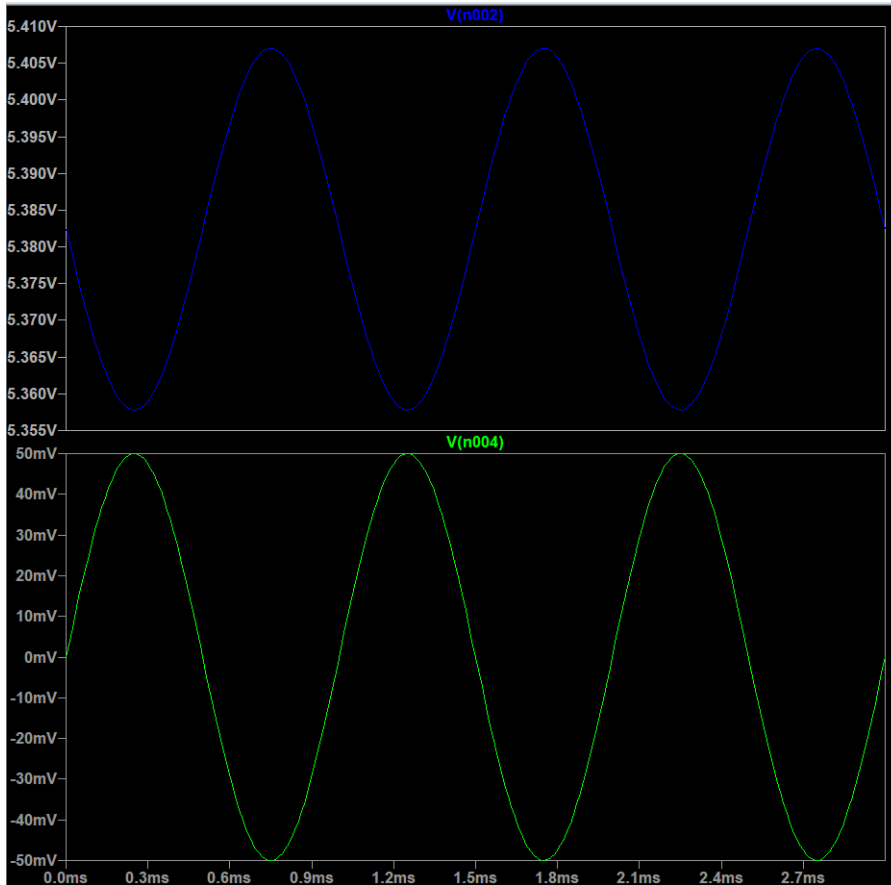
$V_{od} = V_{o1} = 3\text{V}$  peak to peak

$A_{V_{diff}} = 20\log(\frac{V_{od}}{V_{id}}) = 29.5 \text{ dB}$ .

### 3. Common mode input analysis



$V_C(Q1)$  and  $V_C(Q2)$  are overlapping. (peak to peak: 49.17mV).  
To calculate  $A_{V_{cm}}$  I need  $V_{oc}$  and  $V_{ic}$ .



Top pane:  $V_{o1}$ , bottom pane:  $V_{i1}$

$$V_{ic} = (V_{i1} + V_{i2})/2 = 100\text{mV peak to peak}$$

$$V_{oc} = V_{o1} = 49.18\text{mV peak to peak}$$

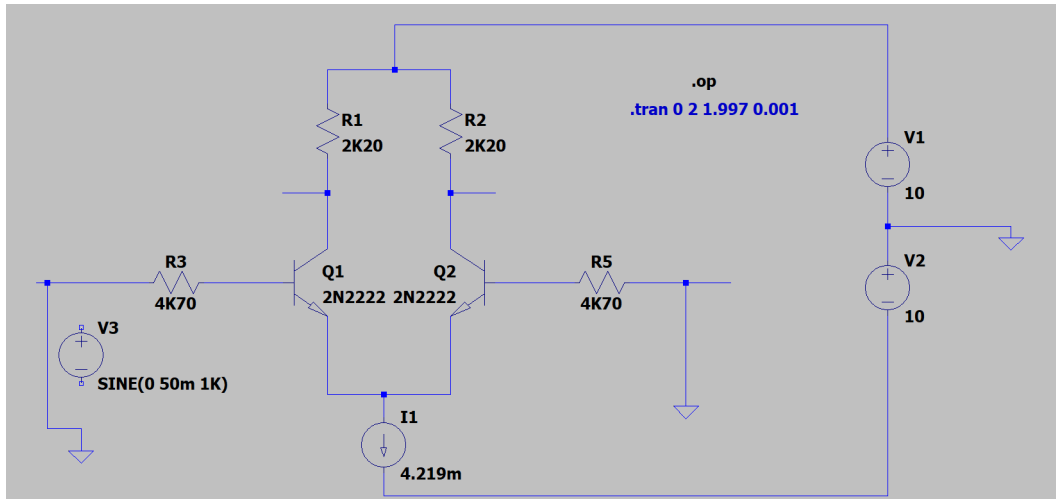
$$A_{V_{cm}} = 20\log\left(\frac{V_{oc}}{V_{ic}}\right) = -6.16 \text{ dB.}$$

### 4. Common mode rejection

$$CMRR = 20\log\left(\frac{A_{V_{diff}}}{A_{V_{cm}}}\right) = 35.7\text{dB.}$$

current source: 4.219 from top to bottom

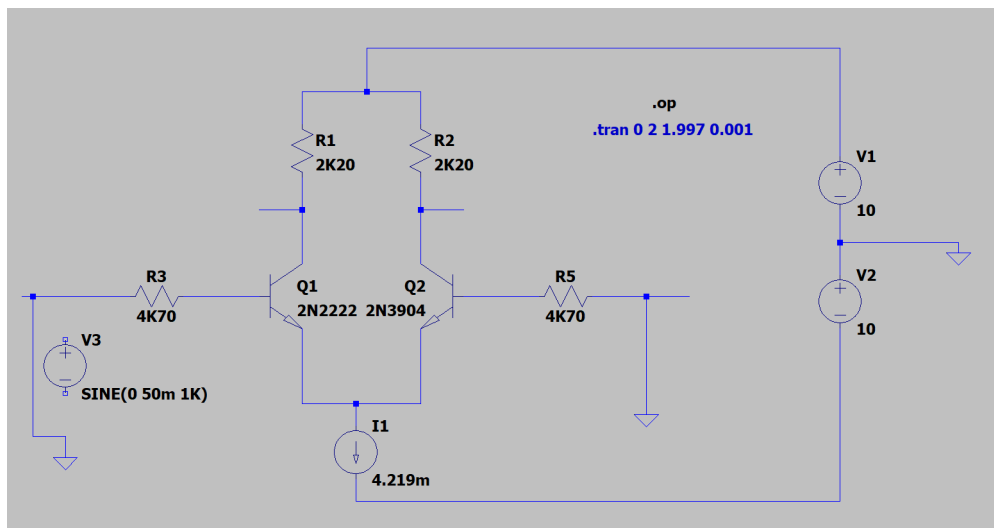
## 5. Replacing R4 by equivalent current source



## 6. Analyses using the current source

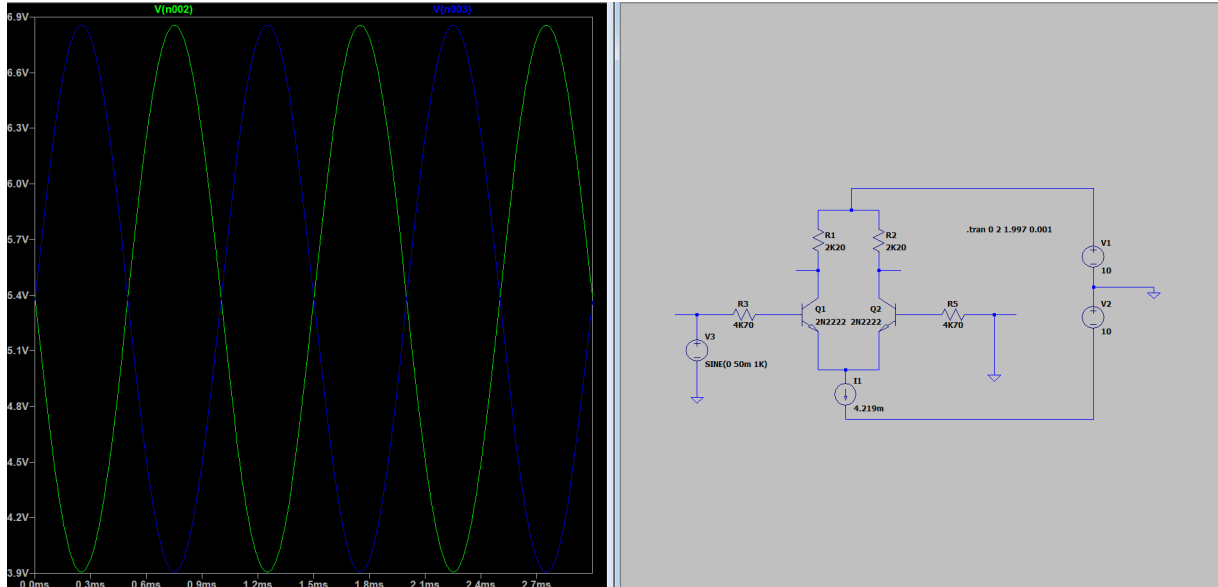
### (a) DC operation point analysis

$V_{BE} = -47.11 - (-720.74) = 767.85\text{mV}$ ,  $V_C = 5.381\text{V}$ ,  $I_C = 2.099\text{mA}$ ,  $I_E = 2.109\text{mA}$ ,  $I_{RE} = 4.219\text{mA}$ . (current source)



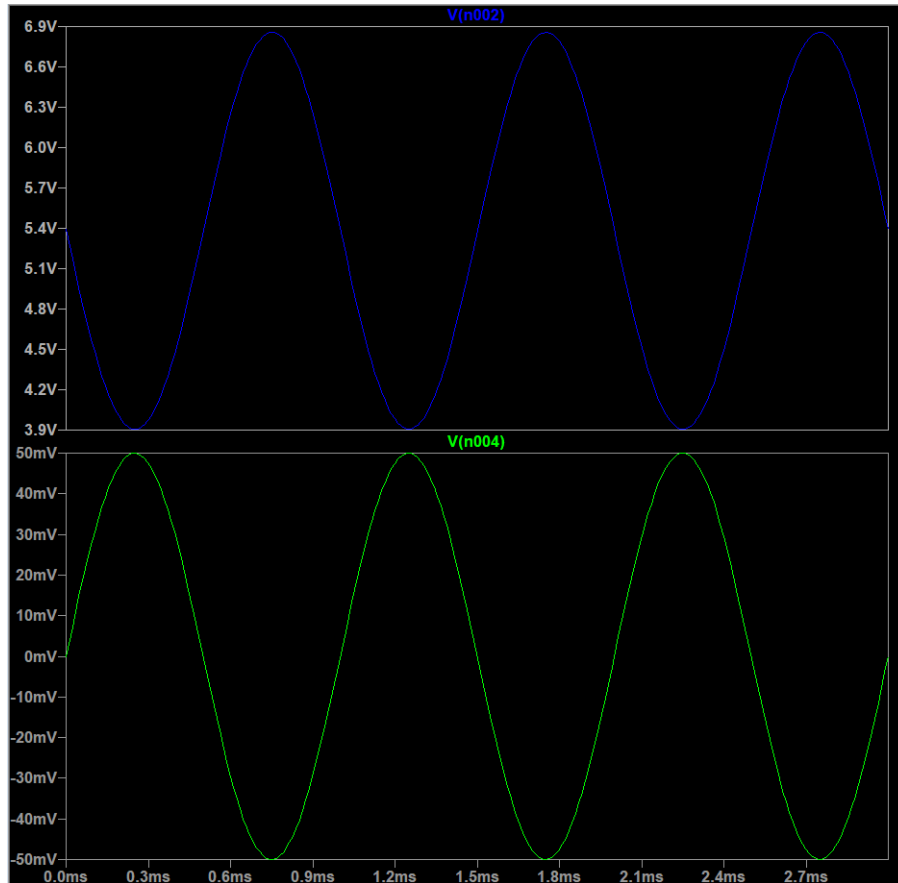
By changing one transistor the  $V_{BE}$ ,  $V_C$ ,  $I_C$ ,  $I_E$  values are not symmetric anymore (ex.:  $V_C(Q1) = 5.913\text{V}$ ,  $V_C(Q2) = 4.841\text{V}$ ), therefore the circuit cannot work properly.

(b) Single ended input analysis



Green line:  $V_C(Q1)$ , blue line:  $V_C(Q2)$ . (peak to peak: 2.95V)

To calculate  $A_{V_{diff}}$  I need  $V_{od}$  and  $V_{id}$ .



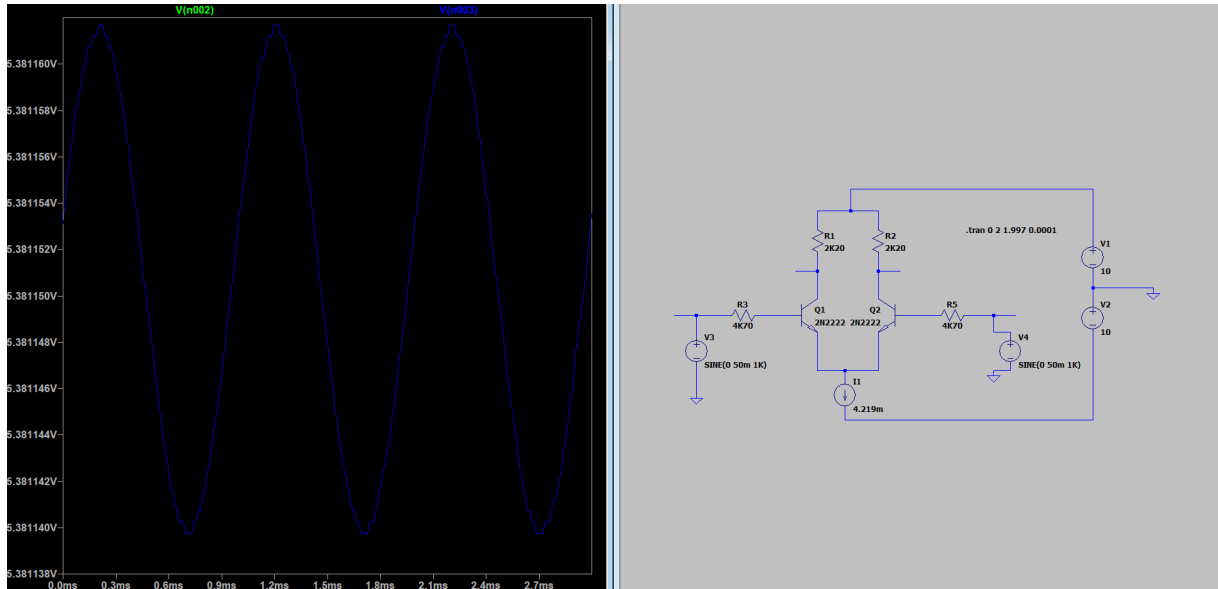
Top pane:  $V_{o1}$ , bottom pane:  $V_{i1}$

$V_{id} = V_{i1} - V_{i2} = 100\text{mV}$  peak to peak

$V_{od} = V_{o1} = 2.95\text{V}$  peak to peak

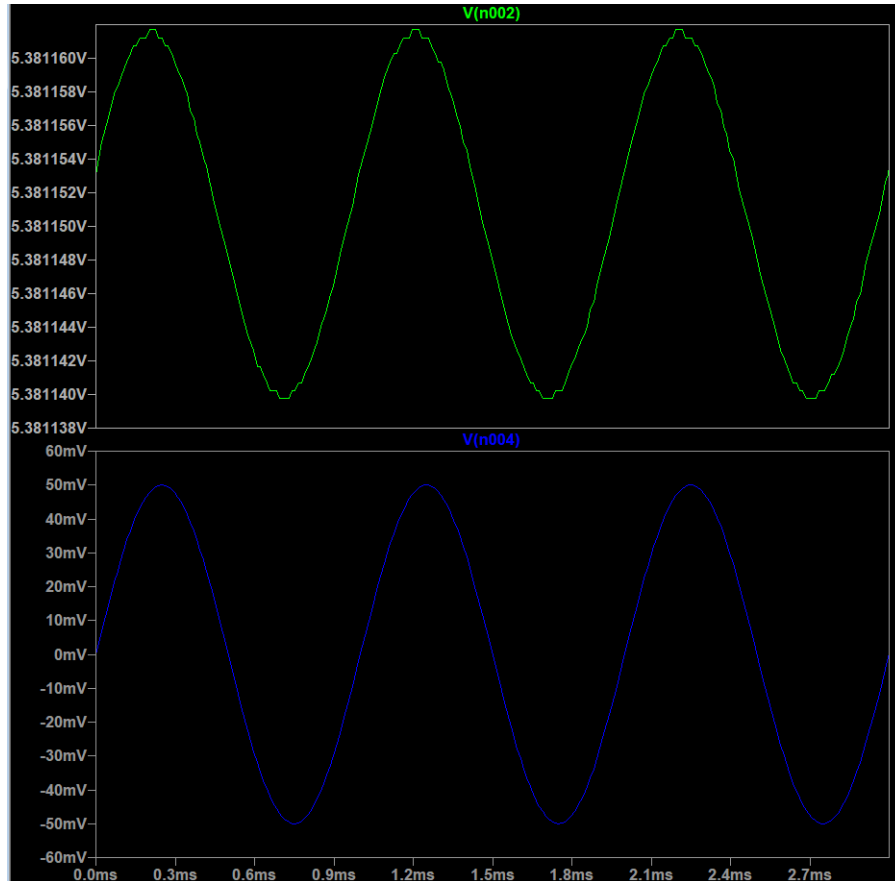
$A_{V_{diff}} = 20\log\left(\frac{V_{od}}{V_{id}}\right) = 29.4 \text{ dB}$ .

(c) Common mode input analysis



$V_C(Q1)$  and  $V_C(Q2)$  are overlapping. (peak to peak:  $21.93\mu V$ ).

To calculate  $A_{V_{cm}}$  I need  $V_{oc}$  and  $V_{ic}$ .



Top pane:  $V_{o1}$ , bottom pane:  $V_{i1}$

$$V_{ic} = (V_{i1} + V_{i2})/2 = 100mV \text{ peak to peak}$$

$$V_{oc} = V_{o1} = 21.93\mu V \text{ peak to peak}$$

$$A_{V_{cm}} = 20\log\left(\frac{V_{oc}}{V_{ic}}\right) = -73.28 \text{ dB.}$$

(d) Common mode rejection

$$CMRR = 20\log\left(\frac{A_{V_{diff}}}{A_{V_{cm}}}\right) = 102.6dB.$$