Metal Oxide Field Effect Transistor

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1 Introduction - Prelab

1.1 Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

1. Enhancement MOSFET: - The transistor is normally off when no gate voltage is applied. - A positive (for NMOS) or negative (for PMOS) gate voltage is required to induce a conductive channel and turn it on. - Commonly used in modern electronics due to its low power consumption in the off state.
   Depletion MOSFET: - The transistor is normally on without any gate voltage applied. - A gate voltage opposite to the type of the MOSFET (negative for NMOS, positive for PMOS) is applied to turn it off. - Less common compared to enhancement-mode MOSFETs.

2. NMOS Transistor:

   - Built using n-type material as the channel. - Requires a positive voltage at the gate relative to the source to turn it on. - Typically faster and has better electron mobility than PMOS. - Used for high-speed and high-performance applications.
   PMOS Transistor:

   - Built using p-type material as the channel. - Requires a negative voltage at the gate relative to the source to turn it on. - Slower than NMOS due to lower hole mobility. - Often used for low-power applications.

1.2 MOSFET as Amplifier

1. $V_{GS} = V_G - V_S$, $V_S = I_D \cdot R_S$

   $V_G = V_{DD} \cdot \frac{R_2}{R_1+R_2} = 5\text{V}$

   Using the saturation current equation: $I_D = k \cdot ((V_G - I_D \cdot R_S) - V_{th})^2$

   $I_D = 0.888\text{mA}$

   $V_{DS} = V_{DD} - I_D(R_D + R_S) = \text{-}0.67\text{V}$

   $V_{GS} = V_G - V_S = \text{-}0.33\text{V}$

2. To verify that the MOSFET is in the saturation region V_DS must be greater than $V_{GS} - V_{th}$

   $V_{DS} = \text{-}0.67\text{V}$, $V_{GS} = \text{-}0.33\text{V}$, $V_{th} = 1\text{V}$, so the condition is verified.

1.3 MOSFET as Switch

1. When U_{in} is 0V the mosfet is off, no current flows so $V_{RD} = 0\text{V}$ and $V_{DS} = V_{DD} = 10\text{V}$.

2. From the graph, when V_{GS} is 2.4V, $I_D \approx 55\text{mA}$

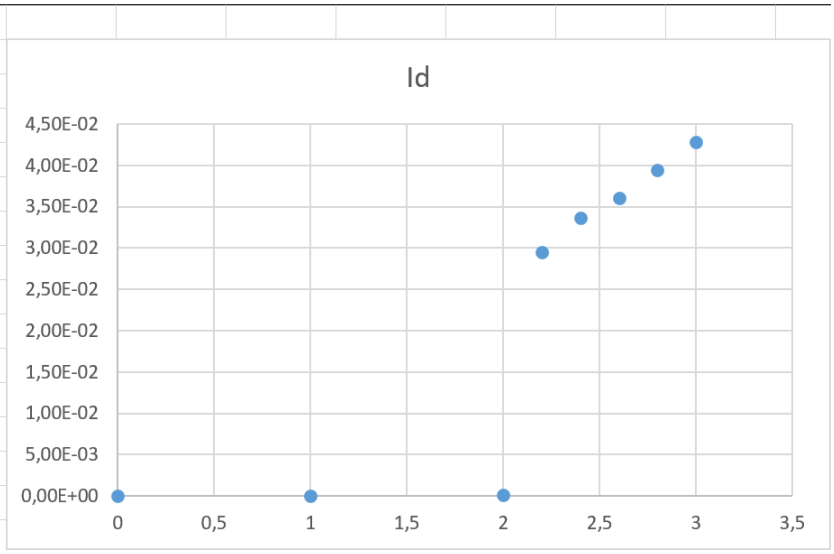
   $V_{DS} = V_{DD} - I_D \cdot R_D = 3.125\text{V}$

2 Experimental Set-up and Results

2.1 I/V Characteristic of a MOSFET

1. Measured MOSFET transfer Characteristics

Vgs	Id
0	3,00E-07
1	3,20E-07
2	1,79E-04
2,2	2,95E-02
2,4	3,36E-02
2,6	3,61E-02
2,8	3,94E-02
3	4,28E-02



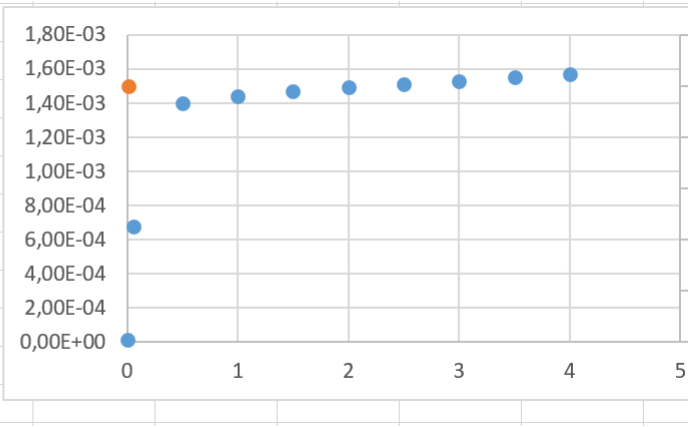
2. The measured V_{th} was 2.185V.
The orange dot in the graphs represent the point (on the x-axis) where $V_{DS}(V_{GS} - V_{th})$ is $= 0$.

$V_{GS} = 2$V (under the threshold)

Vgs	Vd	Id
2	0	8,95E-06
	2	8,11E-05
	4	6,47E-05

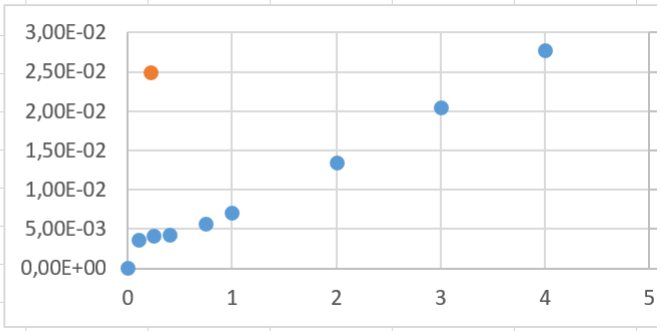
$V_{GS} = 2.2$V

Vgs	Vd	Id
2,2	0	9,30E-06
	0,06	6,74E-04
Vth	0,5	1,40E-03
2,185	1	1,44E-03
	1,5	1,47E-03
Vds	2	1,49E-03
0,015	2,5	1,51E-03
	3	1,53E-03
	3,5	1,55E-03
	4	1,57E-03



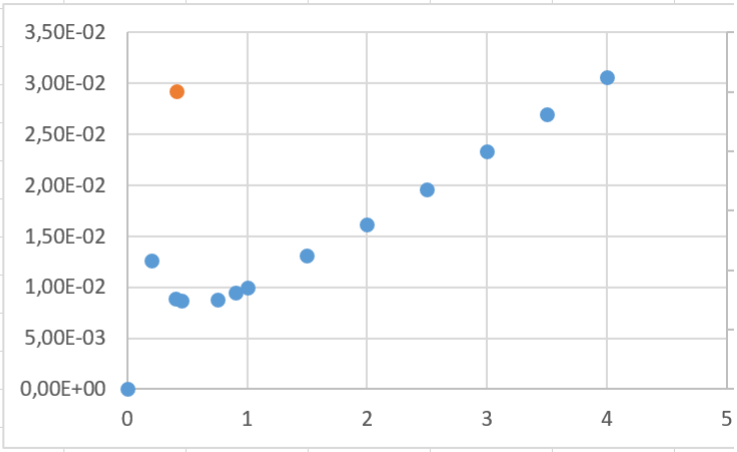
$V_{GS} = 2.4$V

Vgs	Vd	Id
2,4	0	9,80E-06
	0,1	3,59E-03
Vth	0,25	4,10E-03
2,185	0,4	4,22E-03
	0,75	5,70E-03
Vds	1	7,05E-03
0,215	2	1,35E-02
	3	2,05E-02
	4	2,78E-02



$V_{GS} = 2.6$V

Vgs	Vd	Id
2,6	0	1,56E-05
	0,2	1,26E-02
Vth	0,4	8,90E-03
2,185	0,45	8,65E-03
	0,75	8,81E-03
Vds	0,9	9,43E-03
0,415	1	9,93E-03
	1,5	1,31E-02
	2	1,62E-02
	2,5	1,96E-02
	3	2,34E-02
	3,5	2,70E-02
	4	3,06E-02

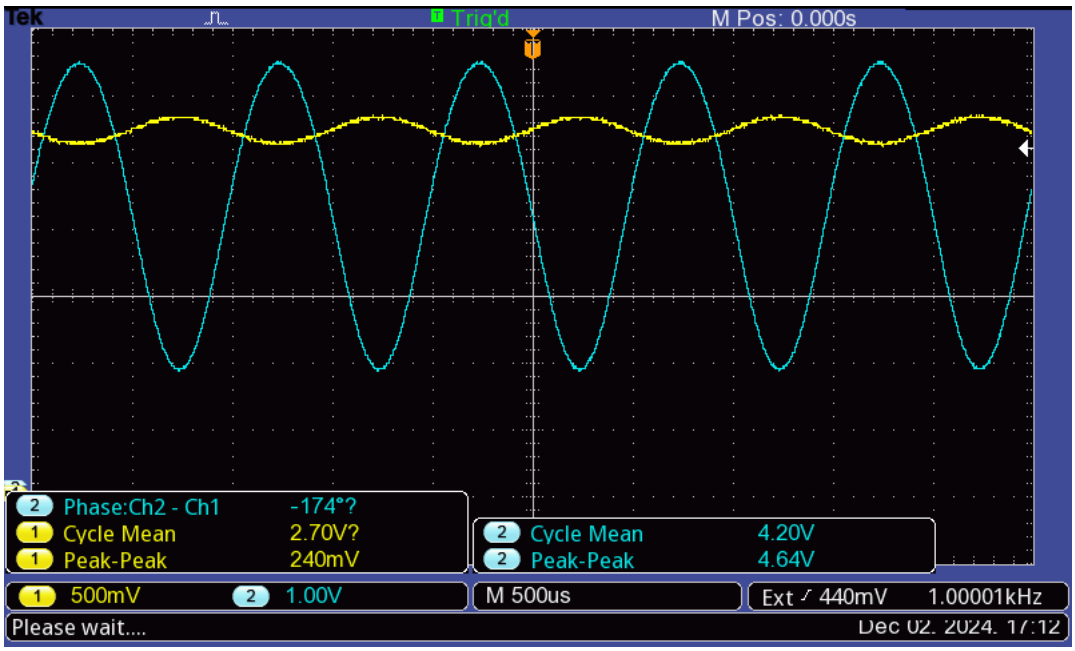


2.2 MOSFET as Amplifier

1. During amplification the MOSFET operates in saturation mode.
   This mode is ideal for amplification since the current I_D is primarly controlled by V_{GS} and the relationship between input and output is stable. The linear mode is not optimal for amplification since the MOSFET acts more as a resistor then as a controlled current source.

2. Using the max $V_{out} = V_{DD} = 10$V and the min V_{out} =0V, the max clipping-free $V_{in} = \frac{5V}{G}$ where G is the gain of the amplifier.

3. Using the following formula to calculate the gain $G = -2kR_D(V_{GS} - V_{th})$ and the provided and used values for R_D and k, $G = 17.1$
   So the largest possigle input voltage amplitude usable without having clipping is 0.29V

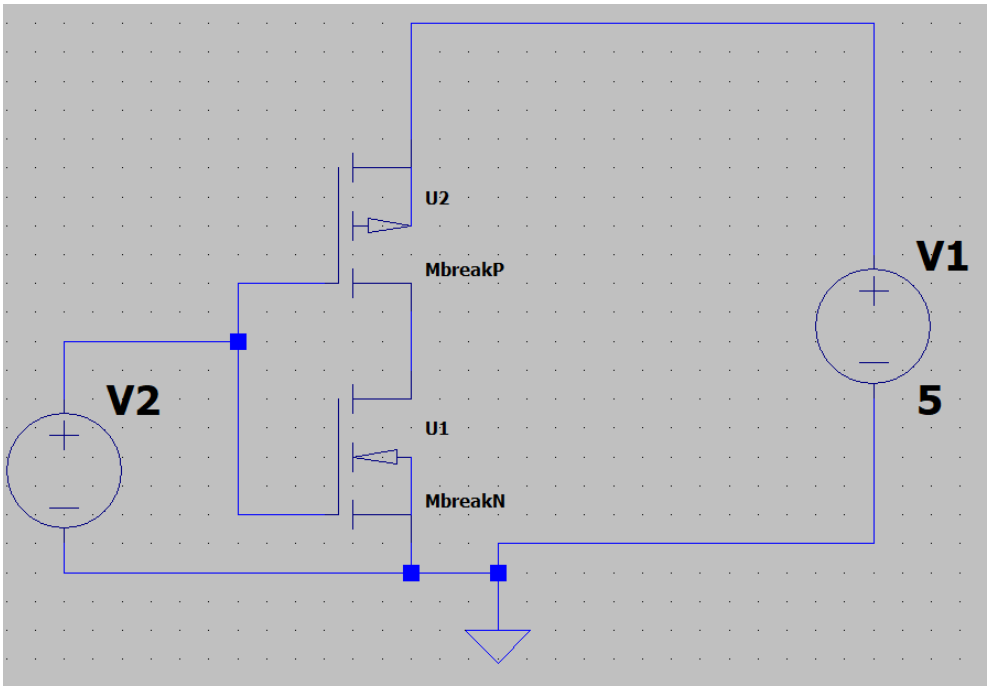
4. 

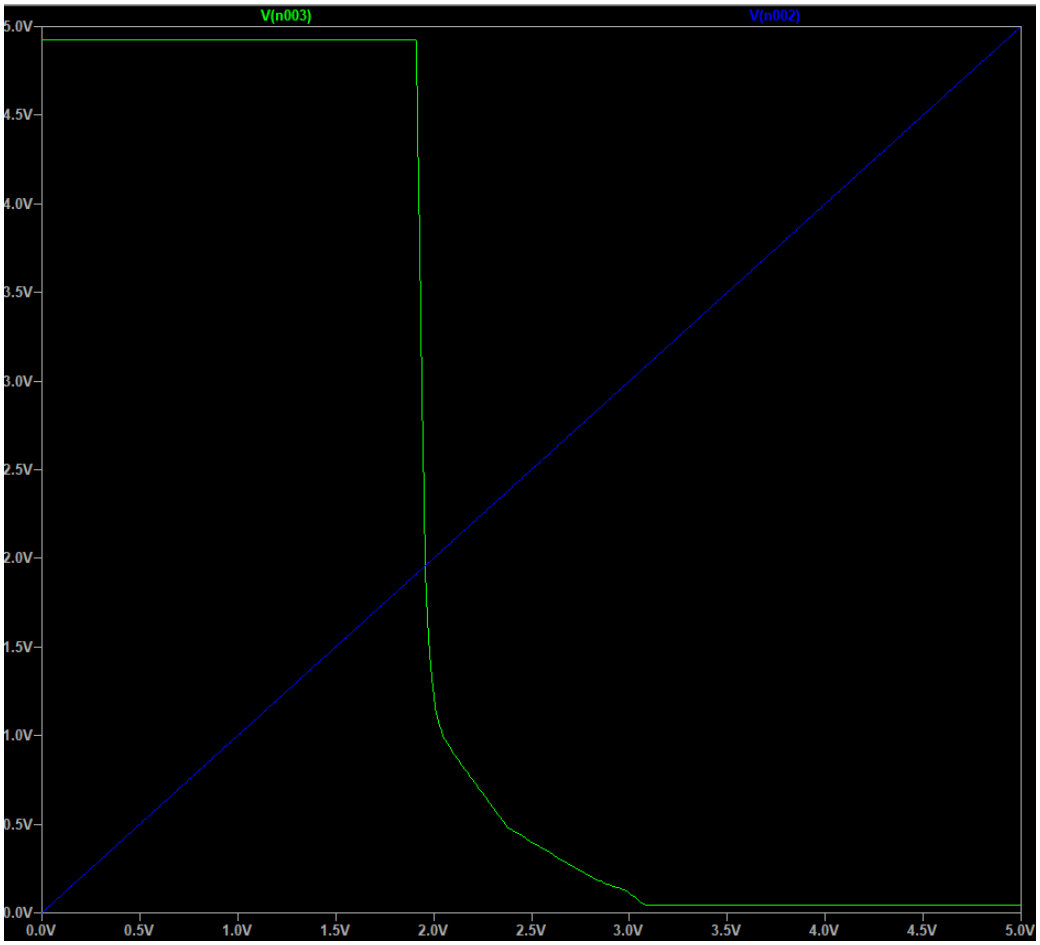
   Input peak to peak voltage: 0.24V, output peak to peak voltage: 4.64V, Gain: 19.3, this value is a bit different from the theoretical one, this can be due to the different R_D used, to the physical transistor used and the different real k value.

5. The output voltage is 180° phase shifted compared to the input voltage. This phase shift is due relationship between I_D and the output voltage V_{out}. As I_D rises (along V_{in}), the voltage drop across R_D increases, pulling V_{out} closer to the ground. Because of this inverted relationship, there is a 180° phase shift between the input and output voltage.

3 Lab 6 prelab

3.1 Voltage Transfer Characteristic of a CMOS inverter

1. 

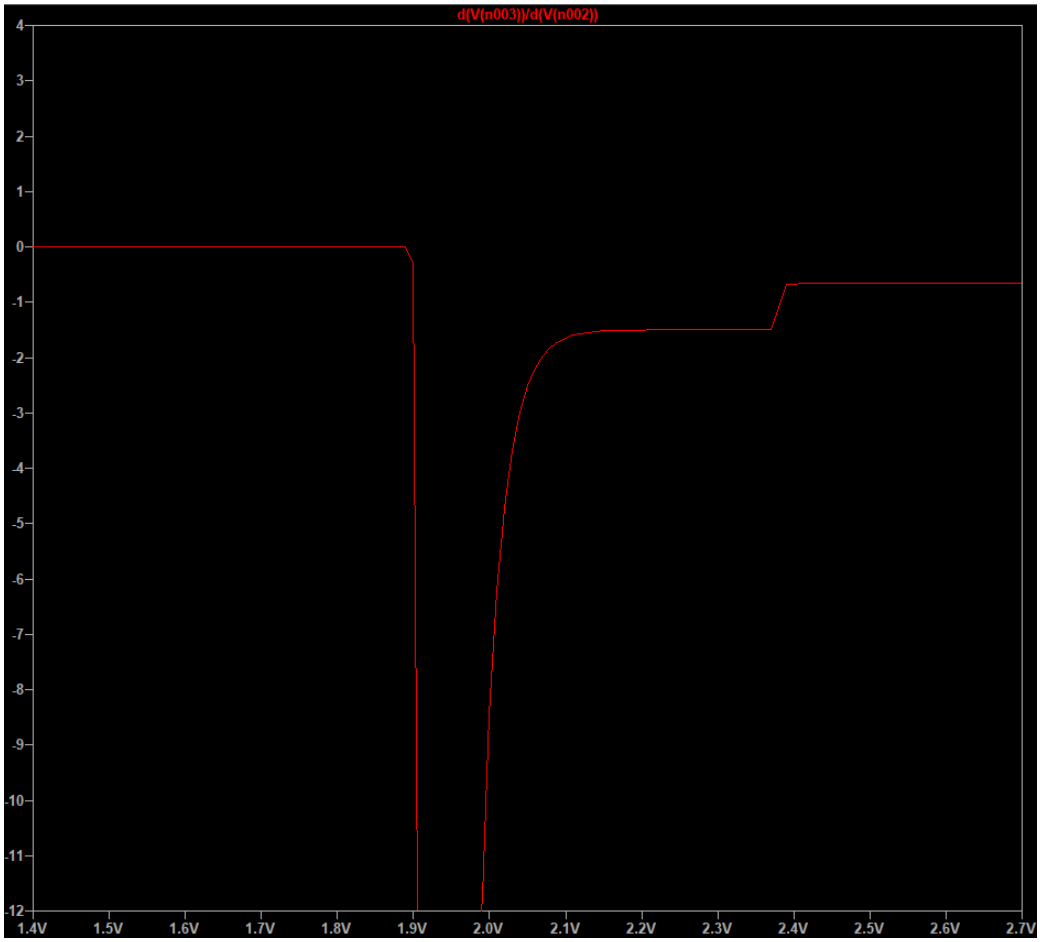


Blue line: DC sweep of V_{in}, Green line: V_{out}

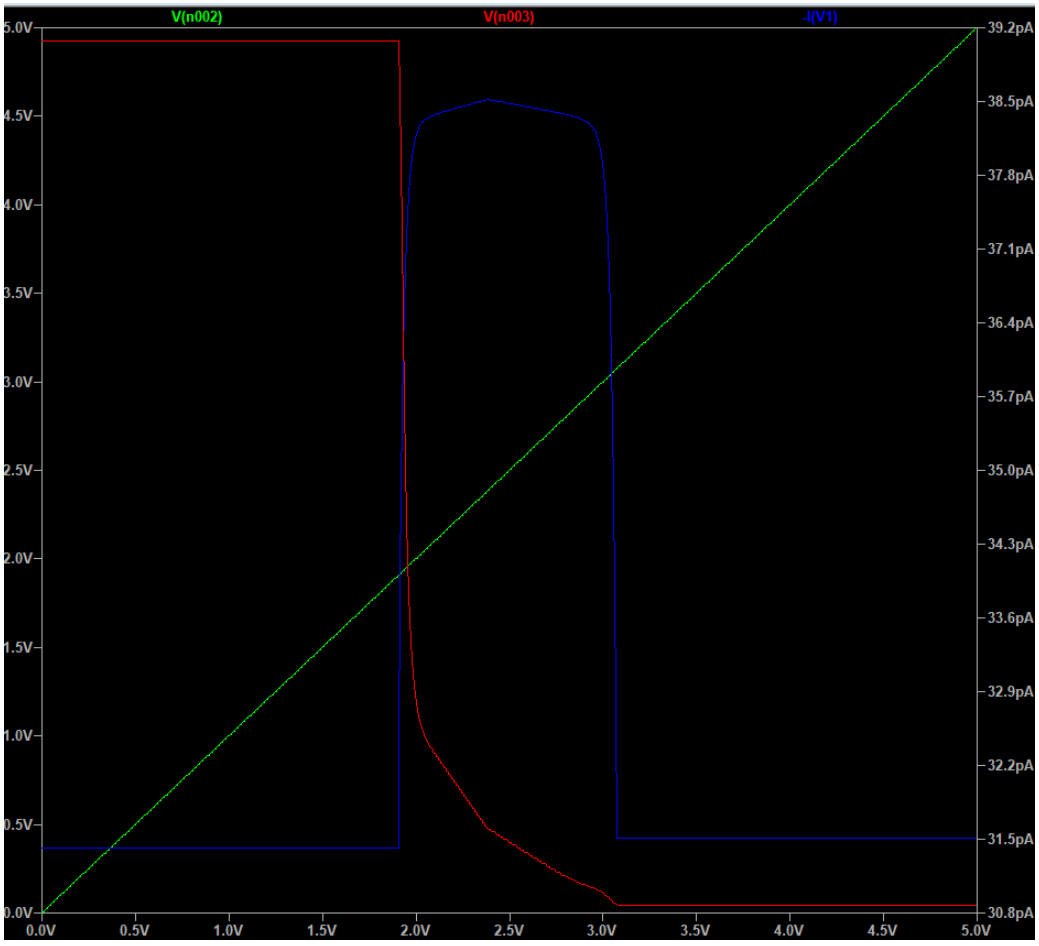
By measuring the graph:

- $V_{OH} = 4.93\text{V}$
- $V_{OL} = 40\text{mV}$
- $V_{th} = 1.96\text{V}$

To measure V_{IH} and V_{IL} i plot $d(V_{out})/d(V_{in})$



- $V_{IH} = 2.38\text{V}$
- $V_{IL} = 1.91\text{V}$
- $NM_L =$ -3.02V
- $NM_H = 2.34\text{V}$

2. 

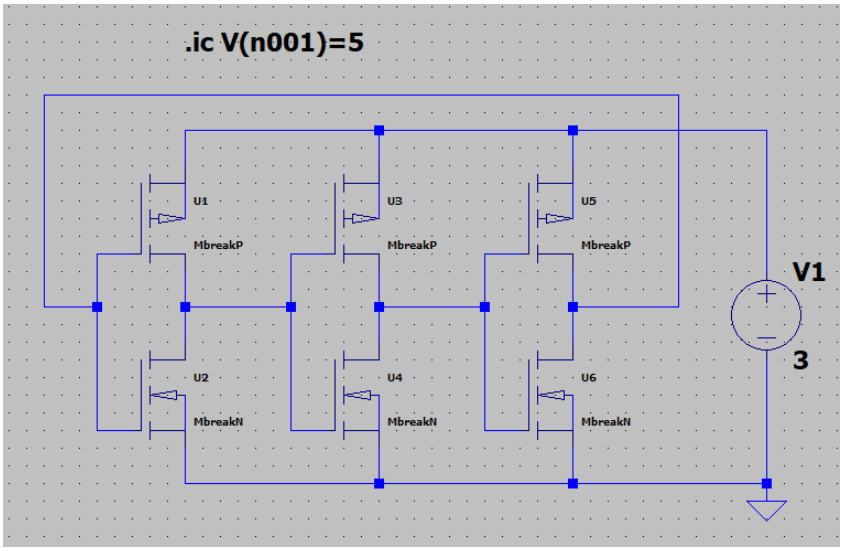
   The blue line is the current through the inverter, the maximum is 38.5pA.

3. The current reaches the maximum when the input level is 2.37V, this is due because both the NMOS and PMOS transistors are partially conducting, this happens around the transition region of the VTC curve.

3.2 CMOS Inverter with Capacitive Load

1. Propagation delay for the different capacitors' values:
   - 25pF: 96ns
   - 50pF: 78ns
   - 75pF: 67ns
   - 100pF: 60ns
2. Power dissipation for the different capacitors' values:
   - 25pF: 0.3125 μW
   - 50pF: 0.625 μW
   - 75pF: 0.9375 μW
   - 100pF: 1.25 μW

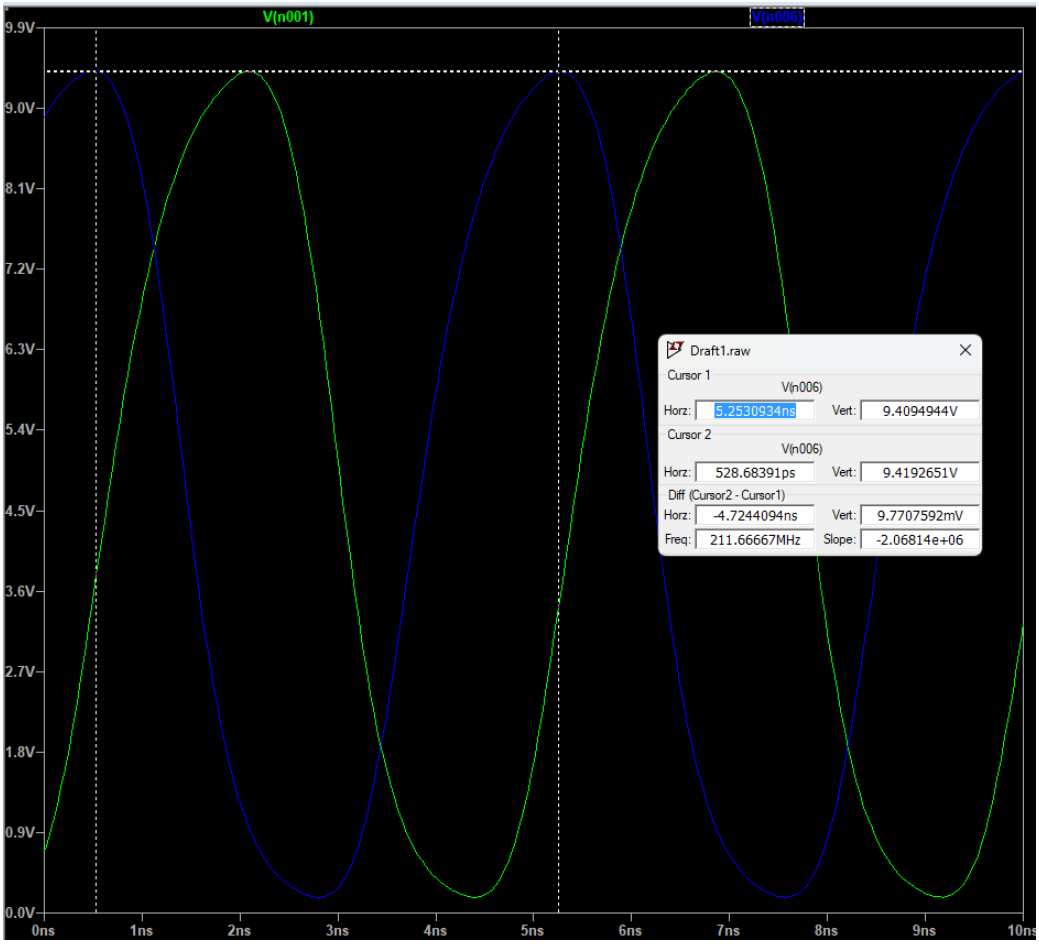
3.3 Propagation Delay of an Inverter Stage

1. 

   The propagation delays and the oscillation frequencies of the ring oscillator at the different supply voltages are the following:

   - 3V: 46.8ns, 7.5MHz
   - 5V: 7.9ns, 42.8MHz
   - 7V: 3.4ns, 98.1MHz
   - 10V: 1.6ns, 211.7MHz

   Example of measuring the oscillation frequency in the 10V case.



2. Behaviour of the ring oscillator with a 50pF capacitor added to each inverter stage. supply voltages.

   Propagation delay: 230ns, oscillation frequency: 1.44MHz, power dissipation: $P_d = C_l \cdot V_{DD}^2 \cdot f = 1.8\text{mW}$

3. The presence of the capacitive load decreases the oscillation frequency and increases the propagation delay of the ring oscillator.

4. According to the power dissipation formula, an increase on the capacitive load increases the power dissipation, and a linear increase on the supply voltage causes a quadratic increase in the power dissipation.