Expansion header

File: expansion_header.kicad_sch

CPU

File: cpu.kicad_sch

Memory

File: memory.kicad_sch

Ethernet

File: ethernet.kicad_sch

UART

File: uart.kicad_sch

Timer & RTC

File: timer_rtc.kicad_sch

Reset

File: reset.kicad_sch

CPLD

File: cpld.kicad_sch

Onboard IO

File: onboard_io.kicad_sch

X busses

File: xbusses.kicad_sch

ROM

File: rom.kicad_sch

NON-COMMERCIAL USE

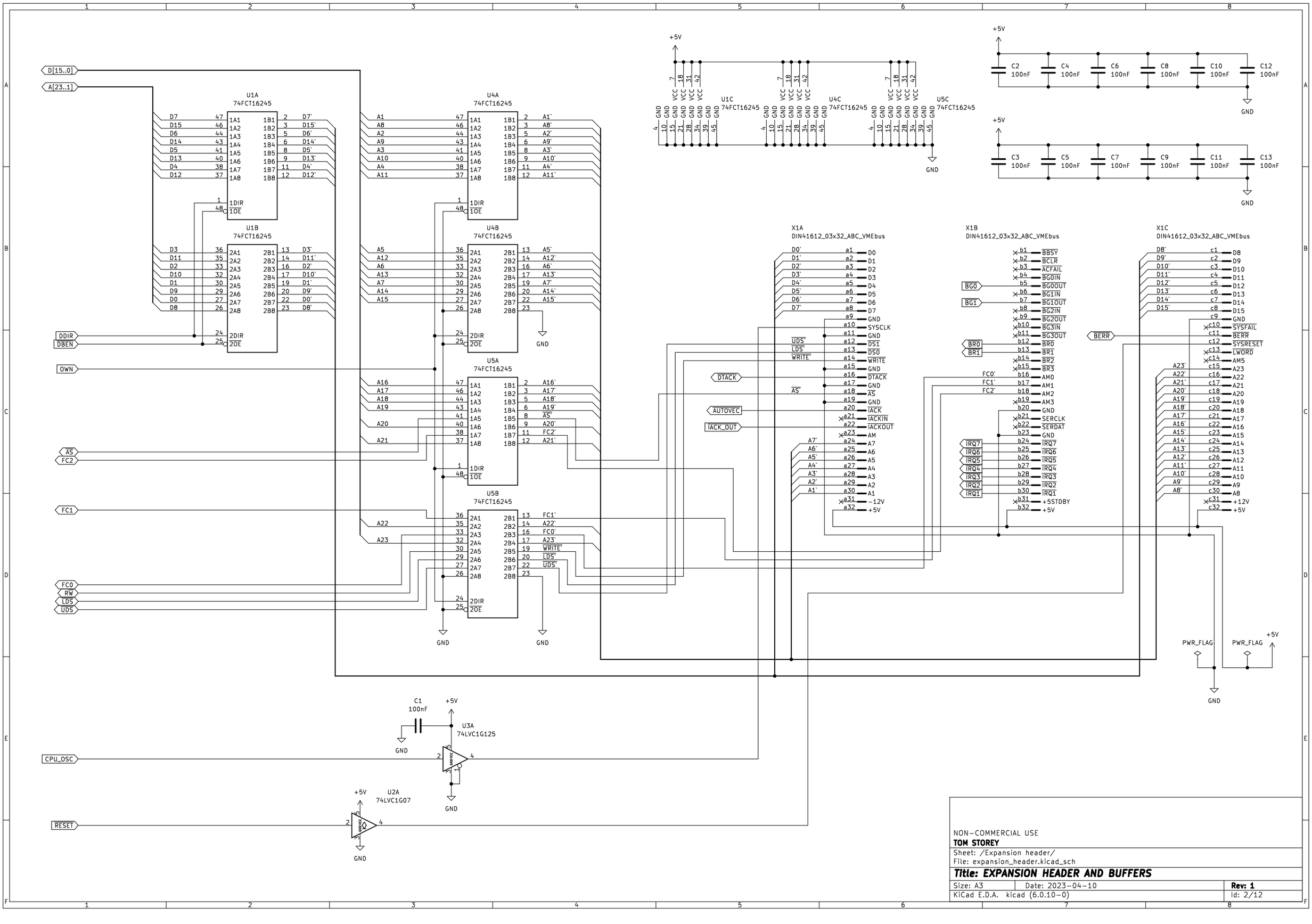
TOM STOREY

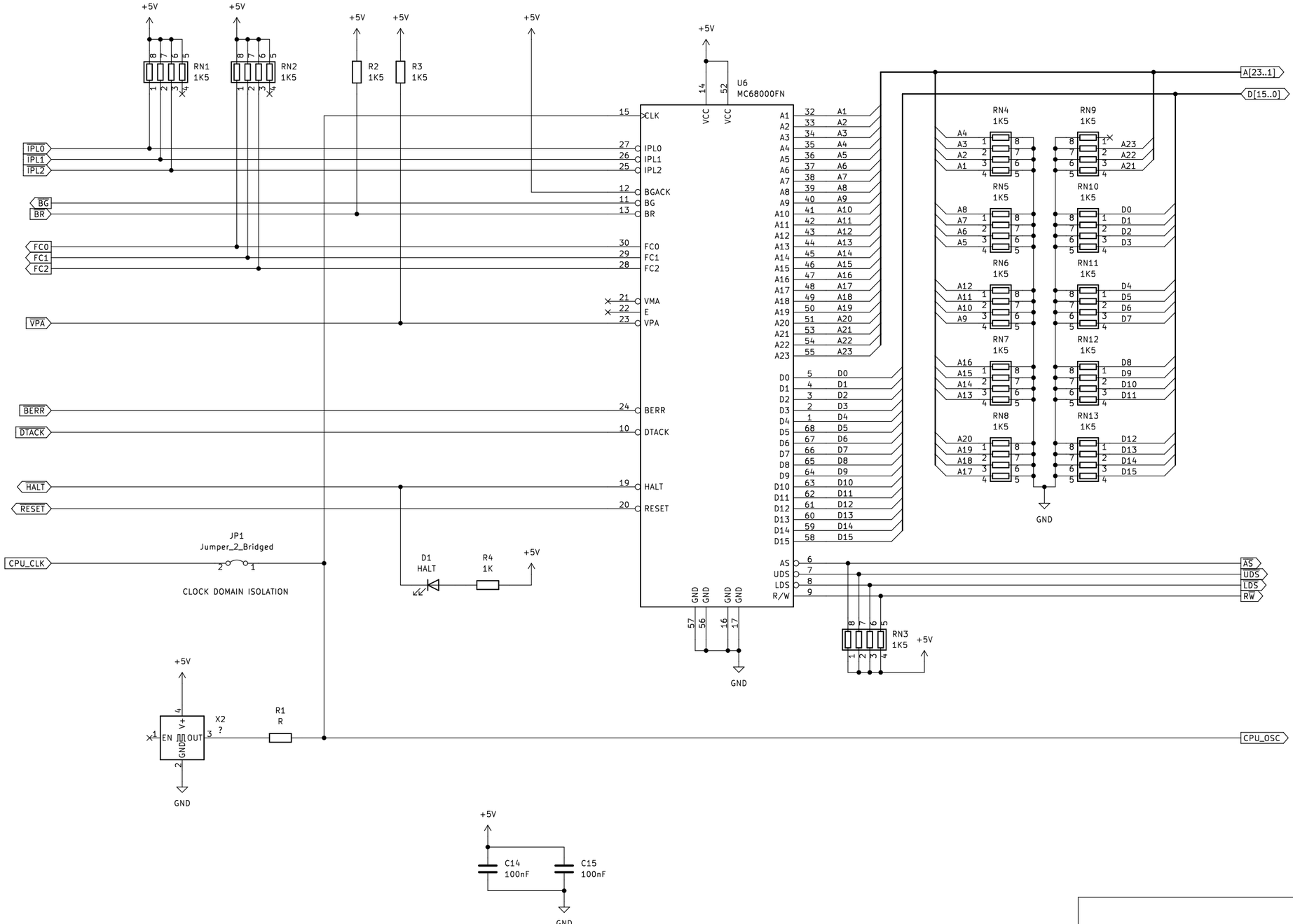
Sheet: /

File: COMET68k.kicad_sch

Title: COMET68k

Size: A3	Date: 2023-04-10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10-0)		Id: 1/12


D[15..0]
A[23..1]
U1A
74FCT16245
U1B
74FCT16245
U4A
74FCT16245
U4B
74FCT16245
U5A
74FCT16245
U5B
74FCT16245
U1C
74FCT16245
U4C
74FCT16245
U5C
74FCT16245
+5V
GND
C2 100nF
C4 100nF
C6 100nF
C8 100nF
C10 100nF
C12 100nF
C3 100nF
C5 100nF
C7 100nF
C9 100nF
C11 100nF
C13 100nF
DDIR
DBEN
OWN
AS
FC2
FC1
FC0
RW
LDS
UDS
A22
A23
X1A
DIN41612_03x32_ABC_VMEbus
X1B
DIN41612_03x32_ABC_VMEbus
X1C
DIN41612_03x32_ABC_VMEbus
DTACK
AUTOVEC
IACK_OUT
BG0
BG1
BR0
BR1
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
IRQ2
IRQ1
BERR
PWR_FLAG
C1 100nF
U3A
74LVC1G125
CPU_OSC
U2A
74LVC1G07
RESET
NON-COMMERCIAL USE
TOM STOREY
Sheet: /Expansion header/
File: expansion_header.kicad_sch
Title: EXPANSION HEADER AND BUFFERS
Size: A3
Date: 2023-04-10
Rev: 1
KiCad E.D.A. kicad (6.0.10-0)
Id: 2/12



NON-COMMERCIAL USE

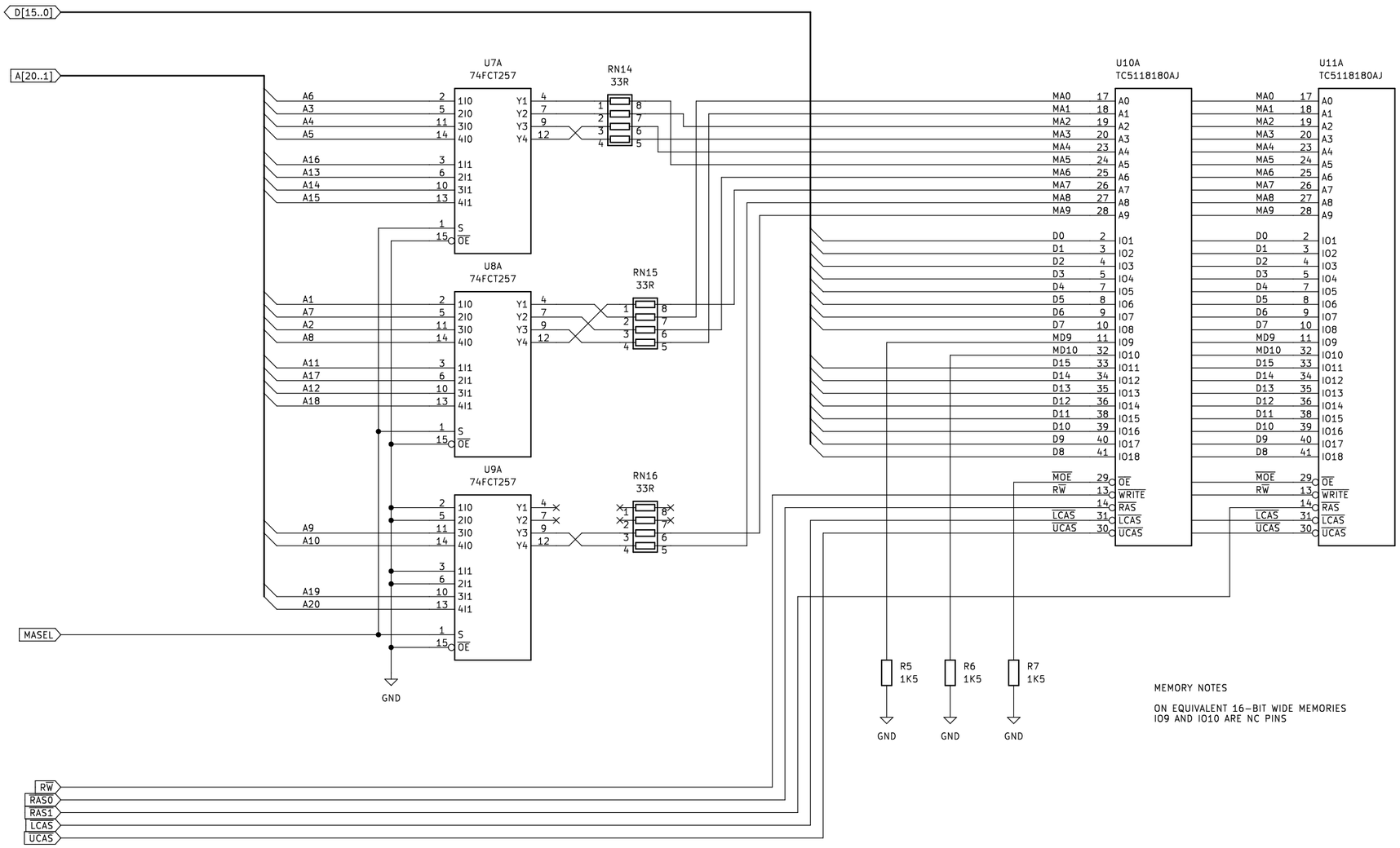
TOM STOREY

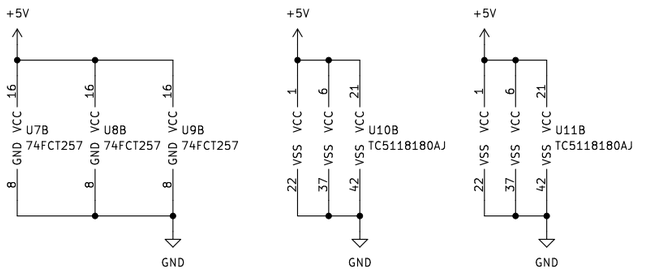
Sheet: /CPU/

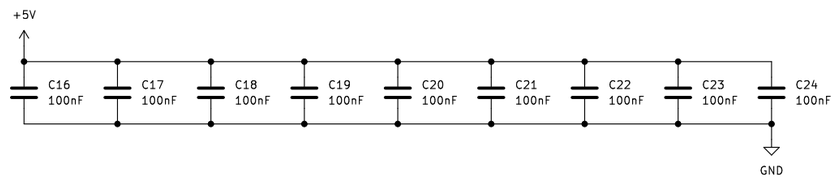
File: cpu.kicad_sch

Title: CPU

Size: A3	Date: 2023-04-10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10-0)		Id: 3/12







NON-COMMERCIAL USE

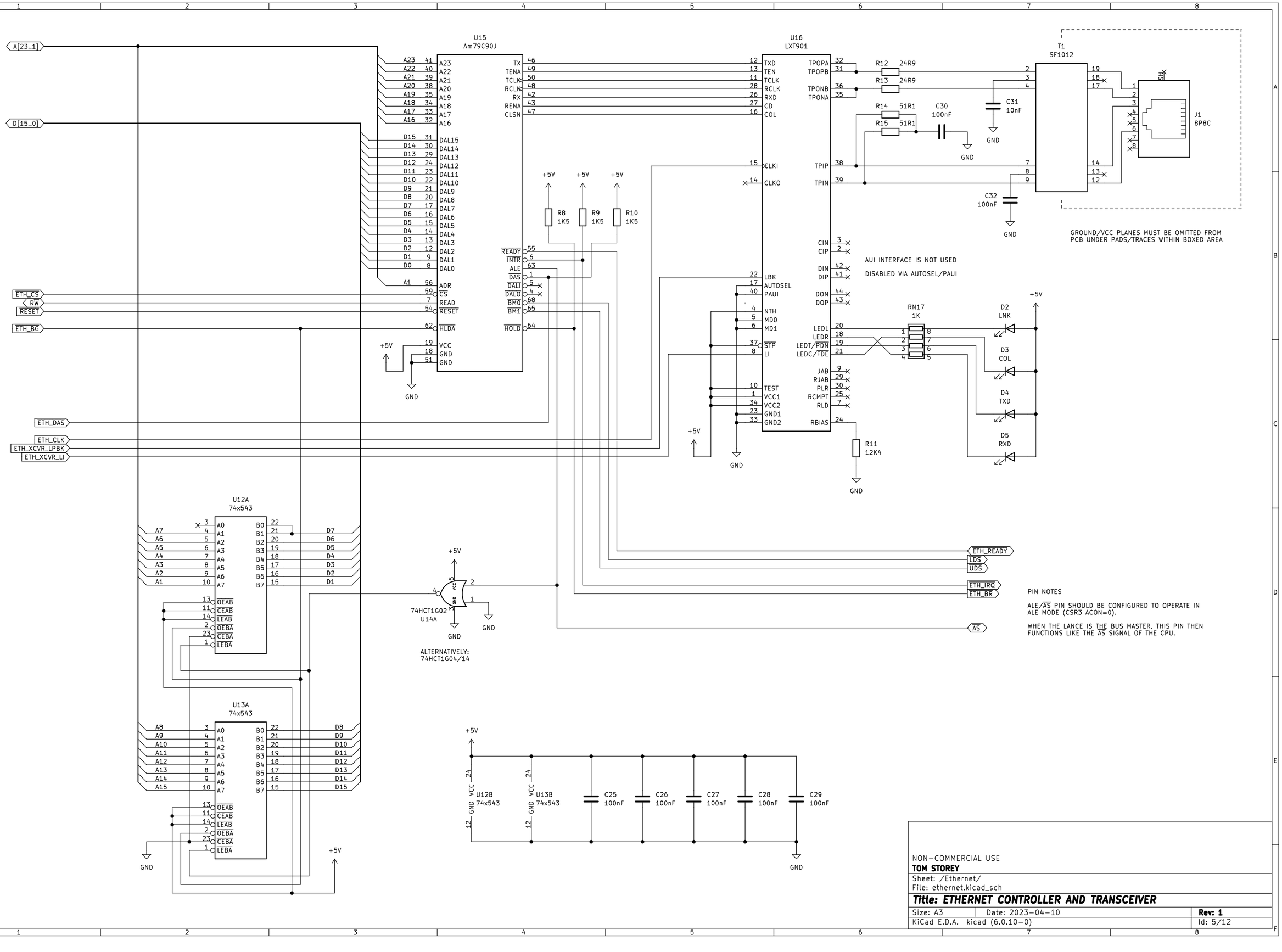
TOM STOREY

Sheet: /Memory/

File: memory.kicad_sch

Title: MEMORY

Size: A3	Date: 2023-04-10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10-0)		Id: 4/12



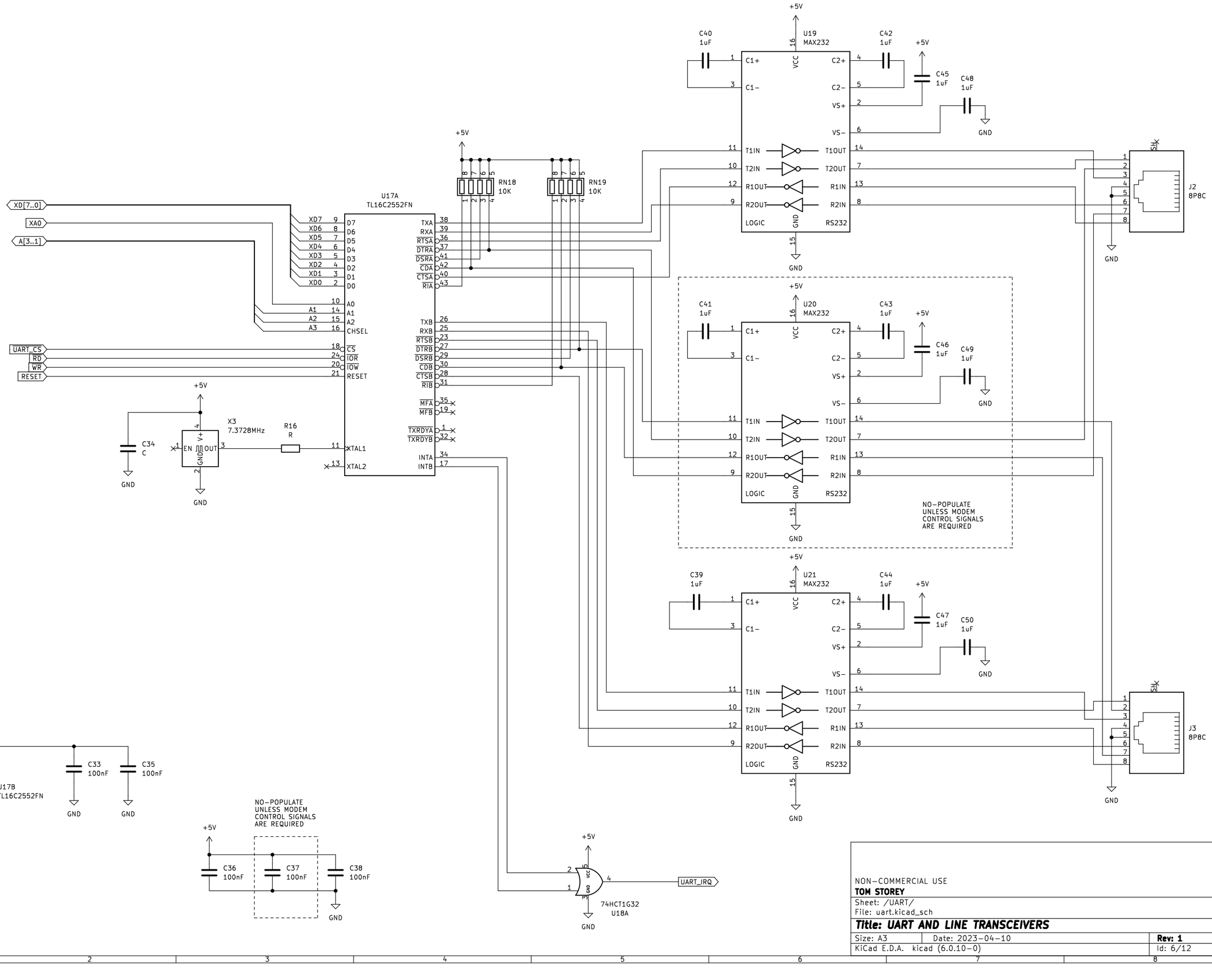
NON-COMMERCIAL USE

TOM STOREY

Sheet: /Ethernet/
File: ethernet.kicad_sch

Title: ETHERNET CONTROLLER AND TRANSCEIVER

Size: A3	Date: 2023-04-10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10-0)		Id: 5/12



NON−COMMERCIAL USE

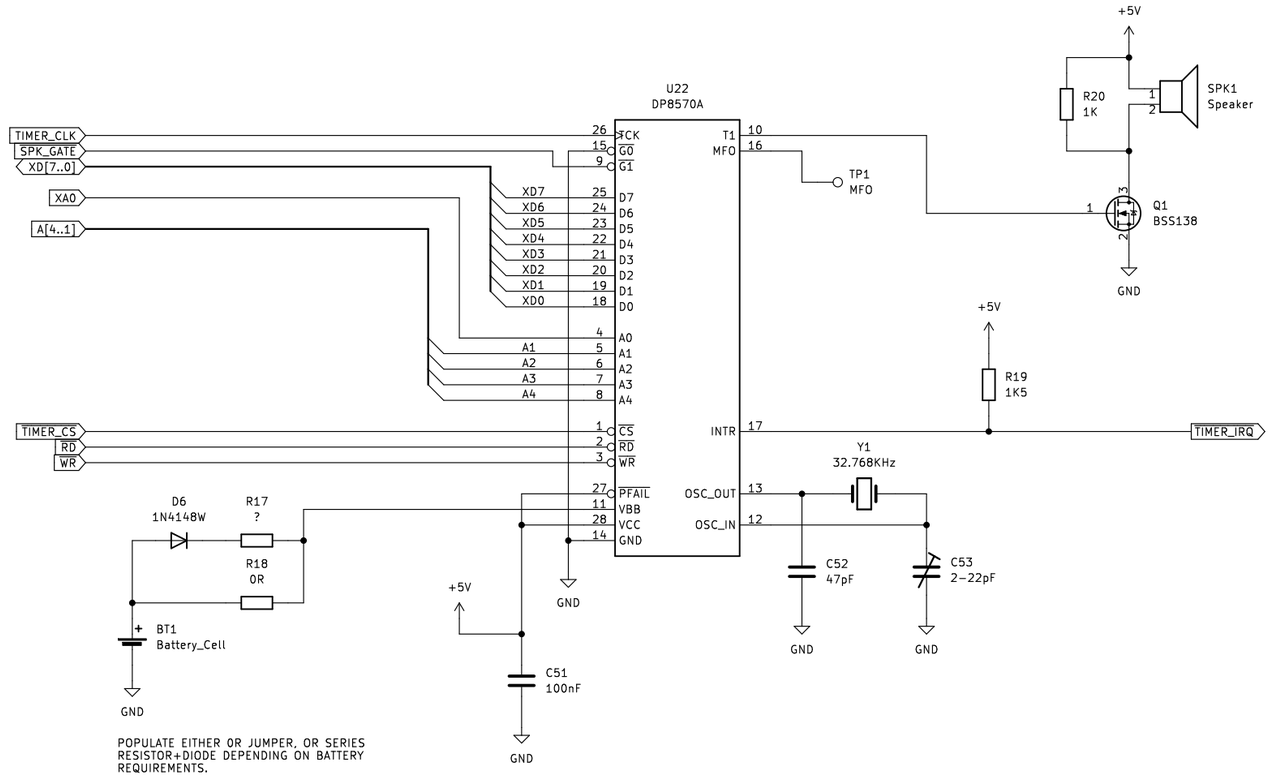
TOM STOREY

Sheet: /UART/

File: uart.kicad_sch

Title: UART AND LINE TRANSCEIVERS

Size: A3	Date: 2023−04−10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10−0)		Id: 6/12

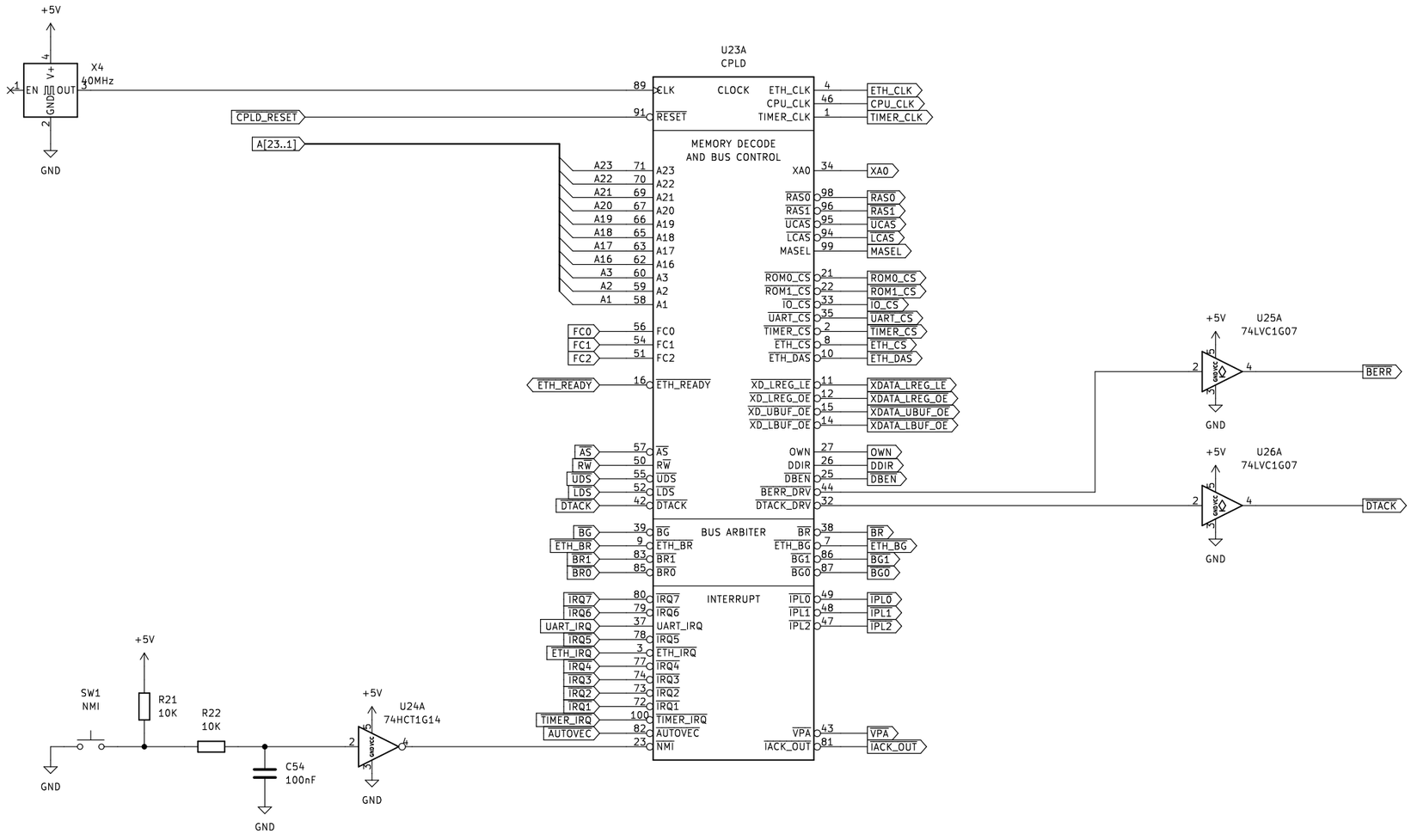


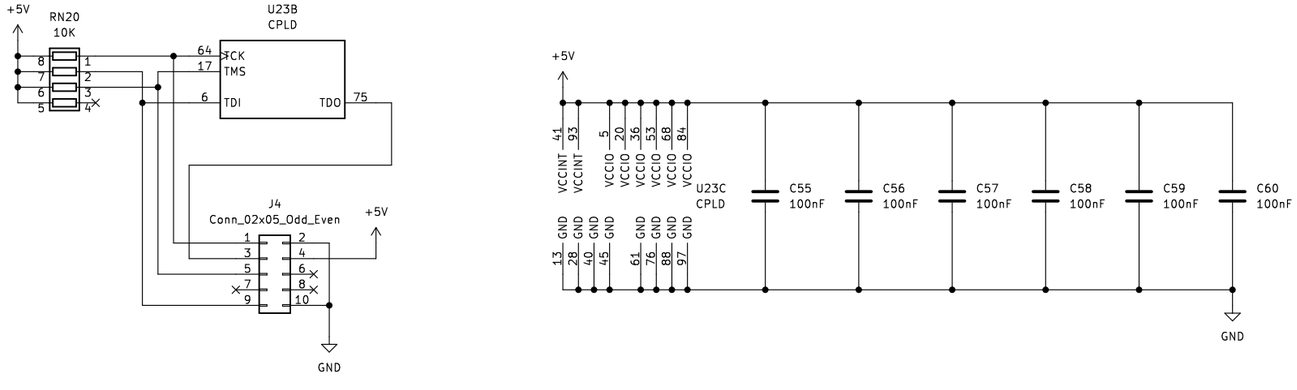
TOM STOREY

Sheet: /Timer & RTC/
File: timer_rtc.kicad_sch

Title: RTC/TIMERS AND SPEAKER

Size: A3	Date: 2023-04-10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10-0)		Id: 7/12





NON-COMMERCIAL USE

TOM STOREY

Sheet: /CPLD/		
File: cpld.kicad_sch		
Title: CPLD		
Size: A3	Date: 2023-04-10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10-0)		Id: 8/12

IO DECODE SUMMARY

OFFSET	WRITE	READ	FUNCTION
0	X		WRITE CONTROL REGISTER 1
0		X	READ CONTROL REGISTER 1
1	X		WRITE CONTROL REGISTER 2
1		X	READ CONTROL REGISTER 2
2		X	WATCHDOG TIMER RESET
3		X	SOFTWARE RESET (IF ENABLED VIA CR 2)

CONTROL REGISTER 1

RW–x	RW–x	RW–x	RW–x	RW–x	RW–x	RW–x	RW–x
		ETH_LI	ETH_LPBK	LED_D	LED_C	LED_B	LED_A
BIT 7							BIT 0

BIT 5 ETH_LI: ETHERNET LINK INTEGRITY TEST
1 = LINK INTEGRITY TEST ENABLED
0 = LINK INTEGRITY TEST DISABLED

BIT 4 ETH_LPBK: ETHERNET LOOPBACK
1 = LOOPBACK ENABLED
0 = LOOPBACK DISABLED

BIT 3 LED_D: LED D CONTROL
1 = LED OFF
0 = LED ON

BIT 2 LED_C: LED C CONTROL
1 = LED OFF
0 = LED ON

BIT 1 LED_B: LED B CONTROL
1 = LED OFF
0 = LED ON

BIT 0 LED_A: LED A CONTROL
1 = LED OFF
0 = LED ON

CONTROL REGISTER 2

R–1	R–0	RW–0	RW–0	R–x	R–x	R–x	R–x
POR	WDTO	SOFT_RST_EN	WDT_EN	CONFIG3	CONFIG2	CONFIG1	CONFIG0
BIT 7							BIT 0

BIT 7 POR: POWER ON RESET FLAG (1)(3)
1 = POWER ON RESET OCCURRED
0 = NORMAL RESET

BIT 6 WDTO: WATCHDOG TIMEOUT FLAG (2)(3)
1 = WATCHDOG TIMEOUT CAUSED RESTART
0 = NORMAL RESET

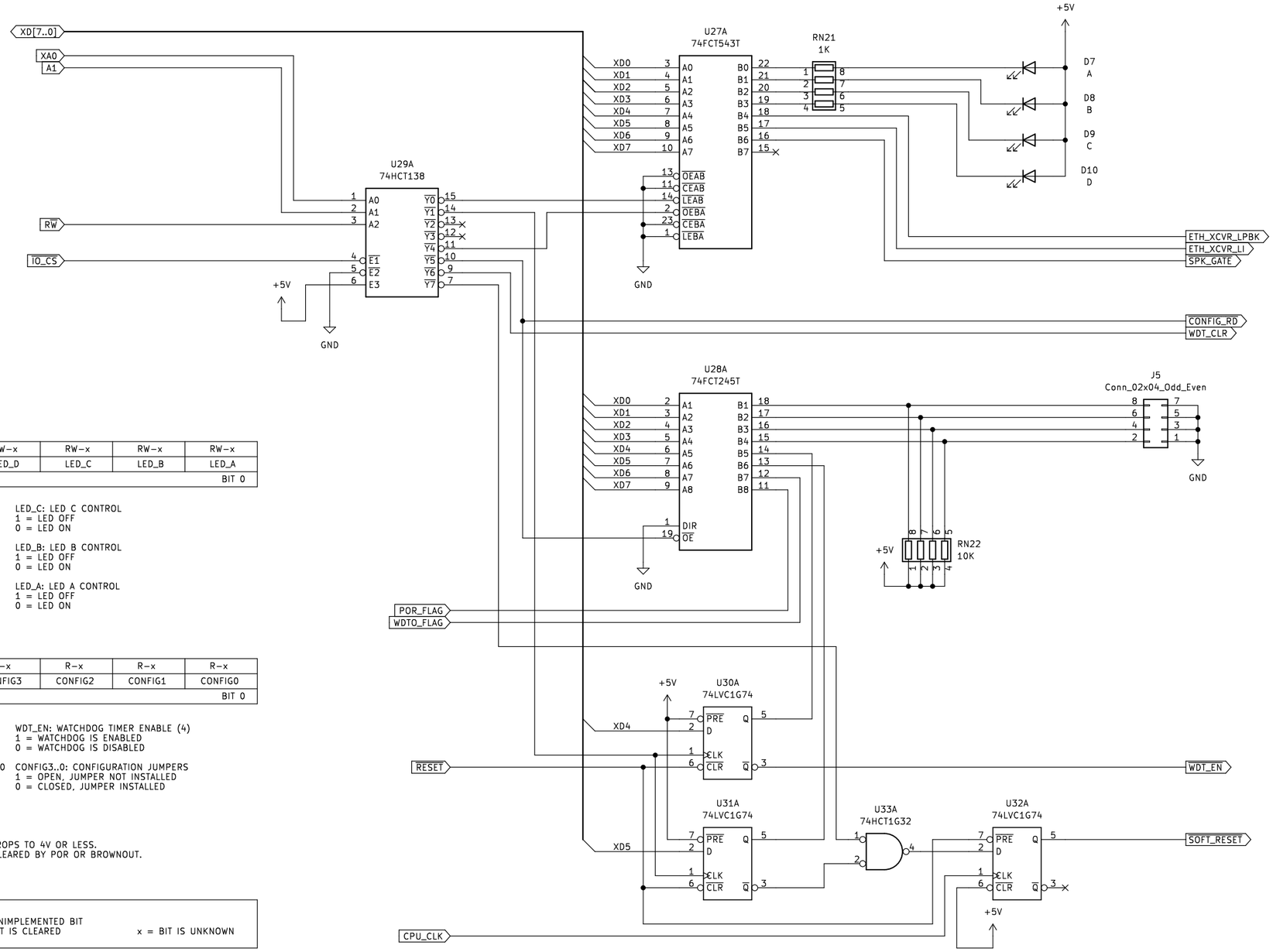
BIT 5 SOFT_RST_EN: SOFTWARE RESET ENABLE (4)
1 = SOFTWARE RESET MAY BE PERFORMED
0 = SOFTWARE RESET IS INHIBITED

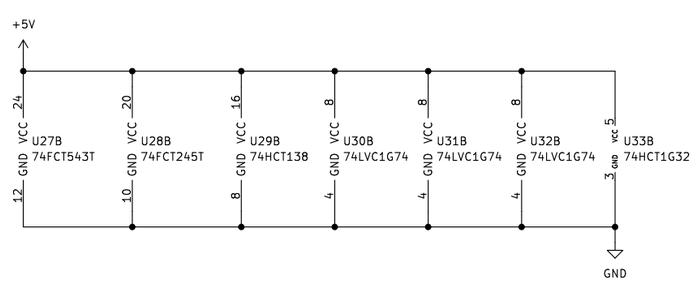
BIT 4 WDT_EN: WATCHDOG TIMER ENABLE (4)
1 = WATCHDOG IS ENABLED
0 = WATCHDOG IS DISABLED

BIT 3–0 CONFIG3..0: CONFIGURATION JUMPERS
1 = OPEN, JUMPER NOT INSTALLED
0 = CLOSED, JUMPER INSTALLED

NOTE 1: BIT IS SET DURING POWER UP, OR BROWNOUT IF VOLTAGE DROPS TO 4V OR LESS.
NOTE 2: BIT IS SET IN THE EVENT OF A WATCHDOG TIMEOUT. BIT IS CLEARED BY POR OR BROWNOUT.
NOTE 3: BIT IS CLEARED AFTER CONTROL REGISTER 2 IS READ.
NOTE 4: BIT IS CLEARED FOLLOWING ANY RESET CAUSE.

LEGEND:
R = READABLE BIT W = WRITABLE BIT U = UNIMPLEMENTED BIT
–n = VALUE AT POR 1 = BIT IS SET 0 = BIT IS CLEARED x = BIT IS UNKNOWN

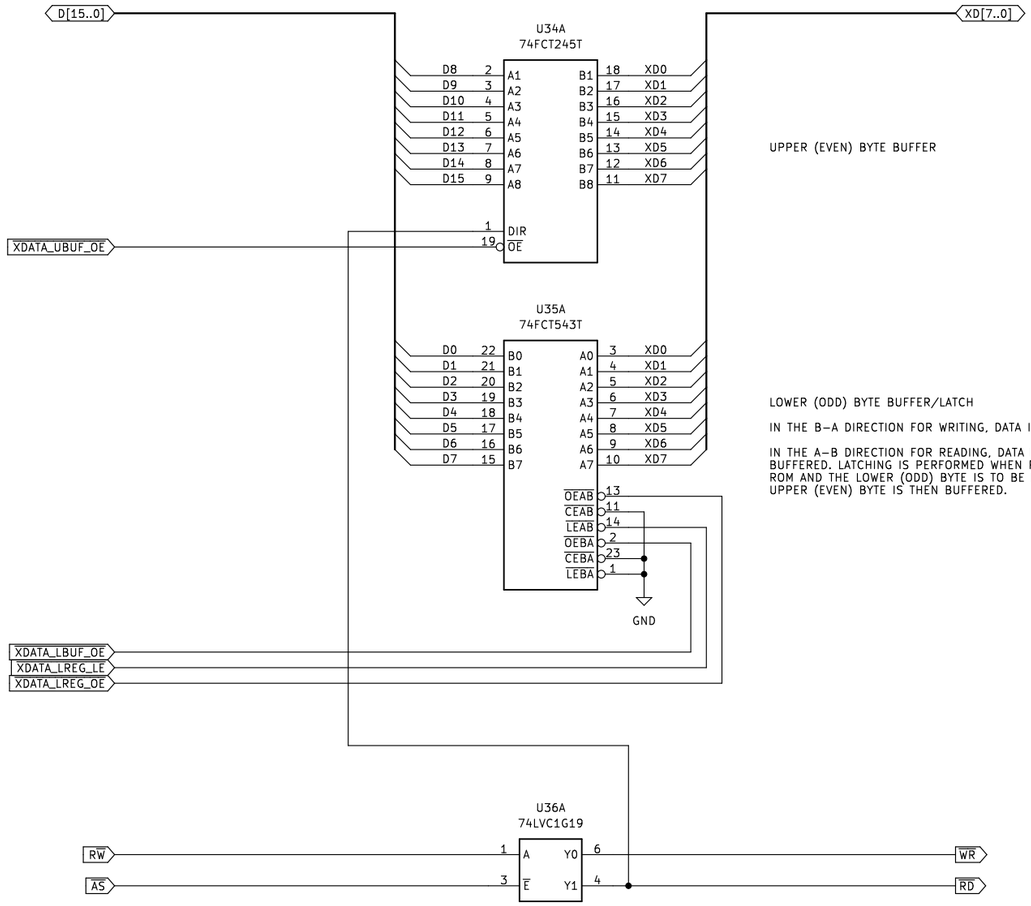




NON–COMMERCIAL USE
TOM STOREY
Sheet: /Onboard IO/
File: onboard_io.kicad_sch

Title: ON–BOARD I/O PORTS

Size: A3	Date: 2023–04–10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10–0)		Id: 9/12

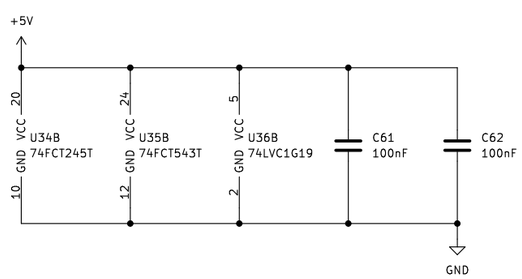


UPPER (EVEN) BYTE BUFFER

LOWER (ODD) BYTE BUFFER/LATCH

IN THE B–A DIRECTION FOR WRITING, DATA IS BUFFERED ONLY.

IN THE A–B DIRECTION FOR READING, DATA MAY BE LATCHED OR BUFFERED. LATCHING IS PERFORMED WHEN READING A WORD FROM ROM AND THE LOWER (ODD) BYTE IS TO BE LATCHED BEFORE THE UPPER (EVEN) BYTE IS THEN BUFFERED.

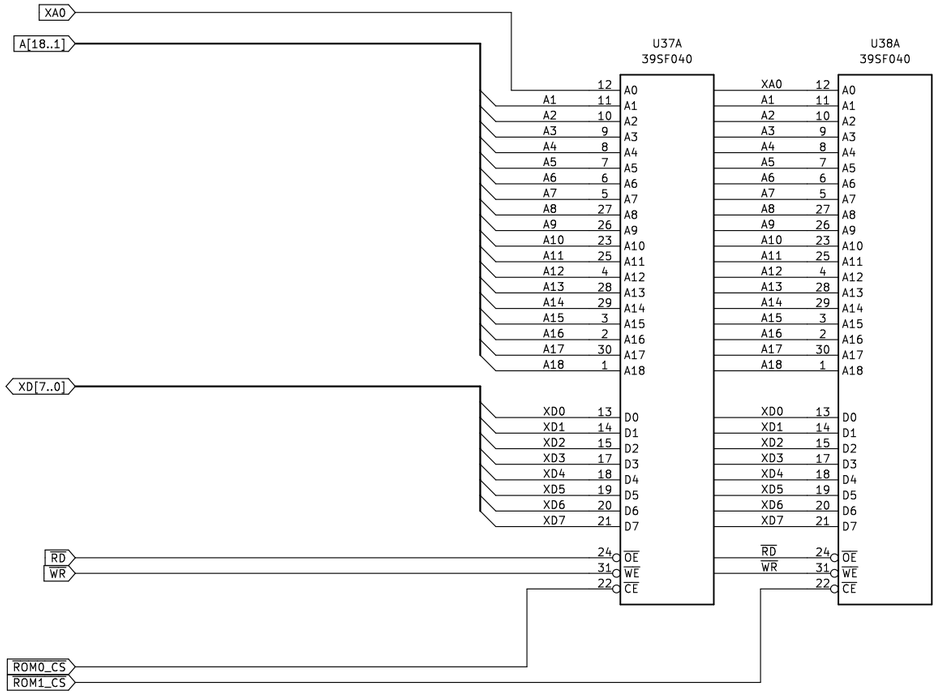


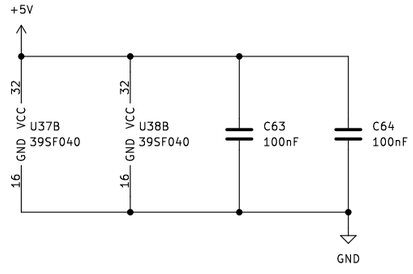
TOM STOREY

Sheet: /X busses/
File: xbusses.kicad_sch

Title: X–BUS

Size: A3	Date: 2023–04–10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10–0)		Id: 10/12





NON-COMMERCIAL USE

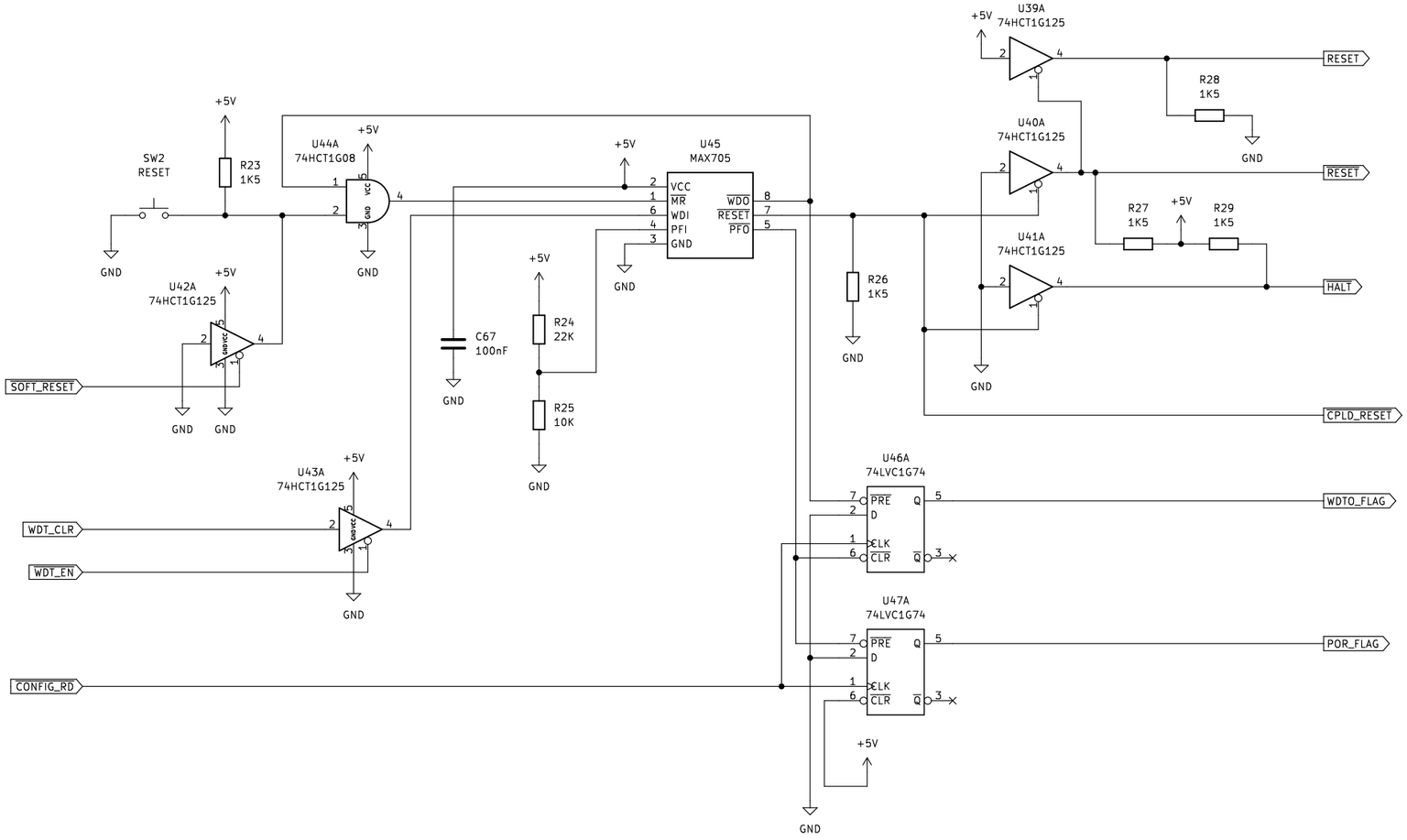
TOM STOREY

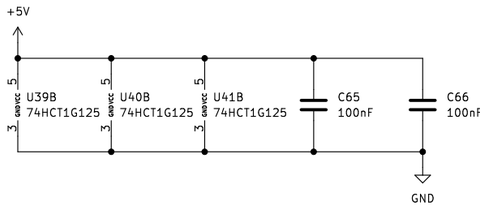
Sheet: /ROM/
File: rom.kicad_sch

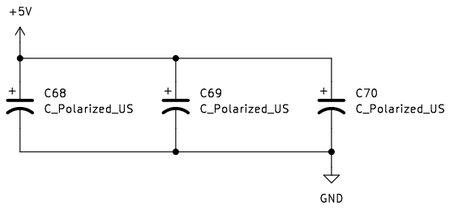
Title: ROM SOCKETS

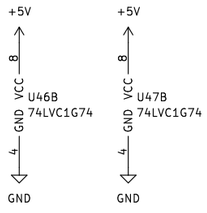
Size: A3	Date: 2023-04-10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10-0)		Id: 11/12

THE "RESET" SIGNAL IS THE COMPLEMENT OF $\overline{\text{RESET}}$ SPECIFICALLY
SO THAT IF THE CPU ASSERTS $\overline{\text{RESET}}$, THEN THIS WILL CAUSE ALL
PERIPHERALS USING A POSITIVE RESET SIGNAL TO BE RESET AS WELL.









TOM STOREY

Sheet: /Reset/
File: reset.kicad_sch

Title: RESET, VOLTAGE SUPERVISOR, WATCHDOG

Size: A3	Date: 2023-04-10	**Rev: 1**
KiCad E.D.A. kicad (6.0.10-0)		Id: 12/12