Expansion header

File: expansion_header.kicad_sch

CPU

File: cpu.kicad_sch

Memory

File: memory.kicad_sch

Ethernet

File: ethernet.kicad_sch

UART

File: uart.kicad_sch

Timer & RTC

File: timer_rtc.kicad_sch

Reset

File: reset.kicad_sch

CPLD

File: cpld.kicad_sch

Onboard IO

File: onboard_io.kicad_sch

X busses

File: xbusses.kicad_sch

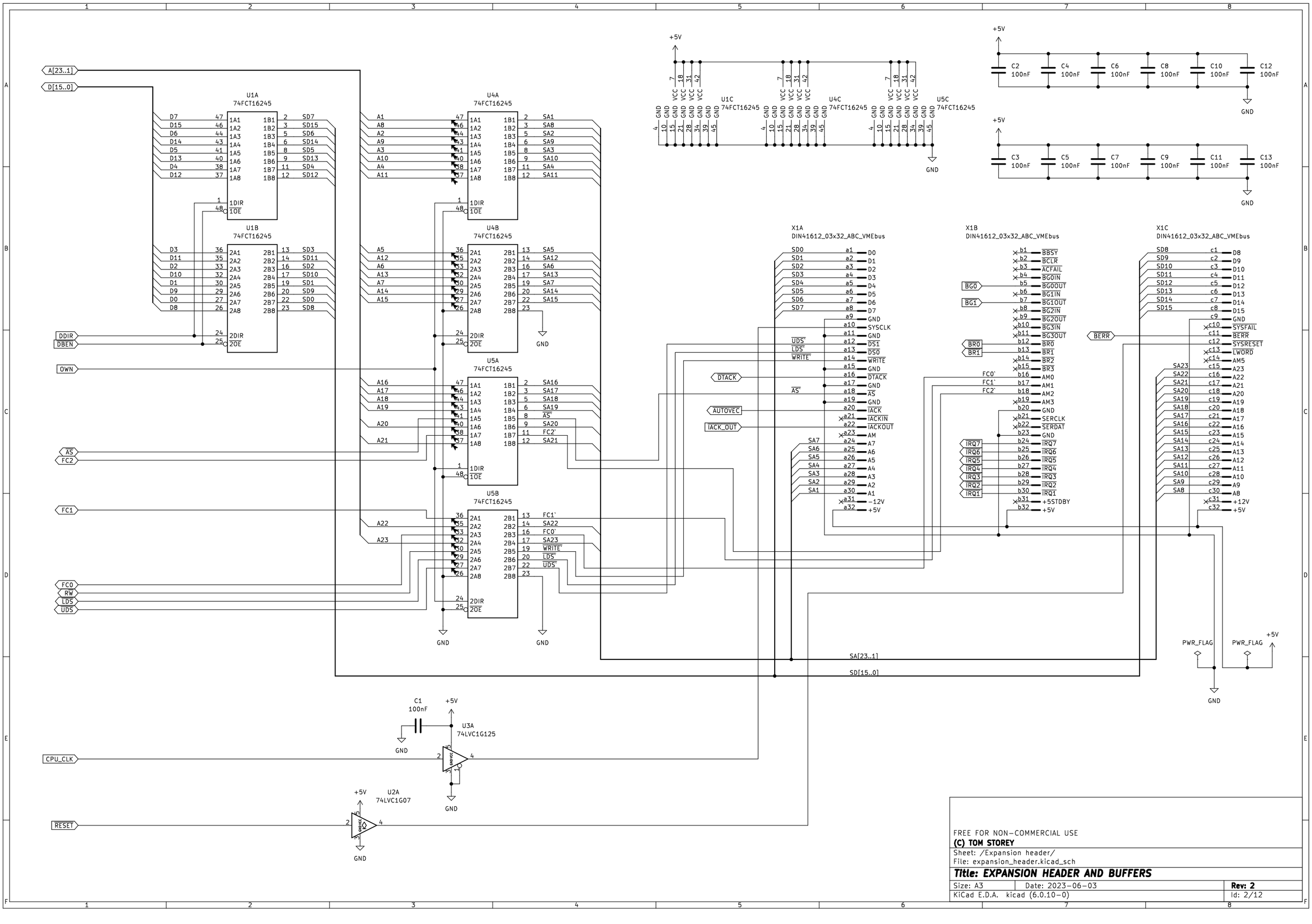
ROM

File: rom.kicad_sch

Sheet: /
File: COMET68k.kicad_sch

Title: COMET68k

Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 1/12



FREE FOR NON-COMMERCIAL USE

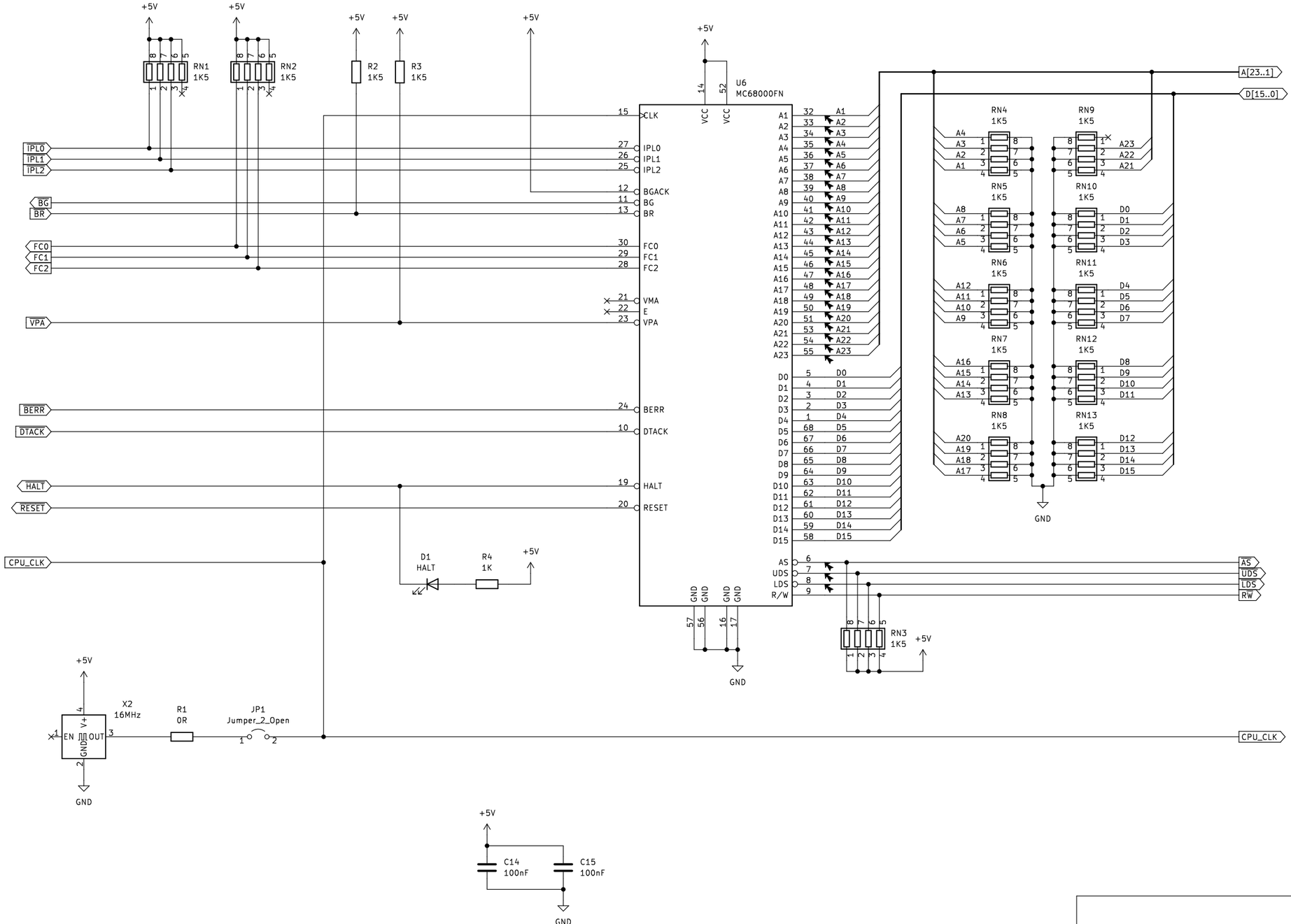
(C) TOM STOREY

Sheet: /Expansion header/

File: expansion_header.kicad_sch

Title: EXPANSION HEADER AND BUFFERS

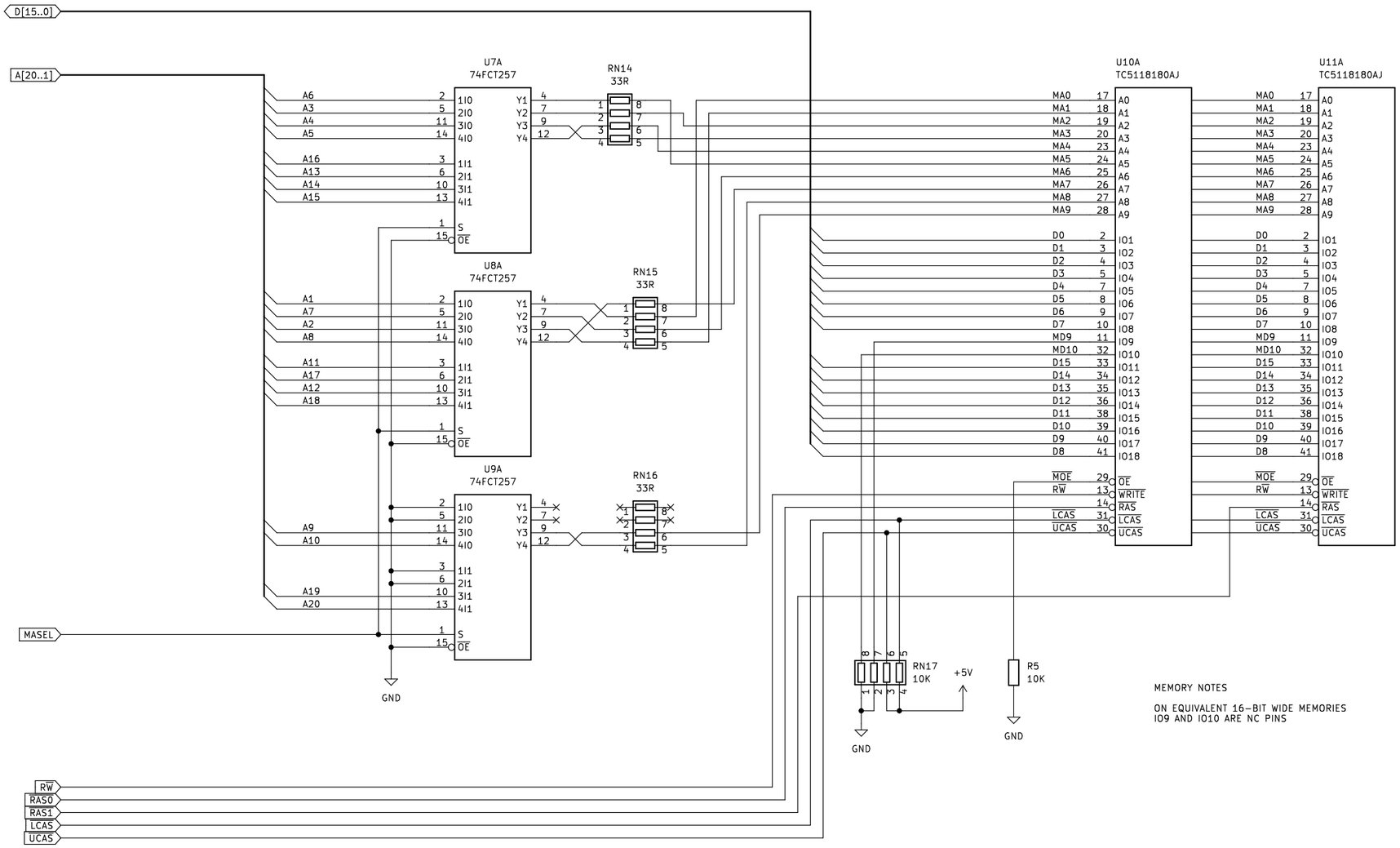
Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 2/12

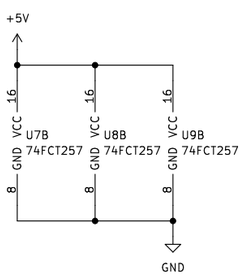


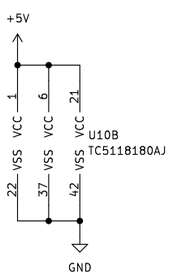
Sheet: /CPU/
File: cpu.kicad_sch

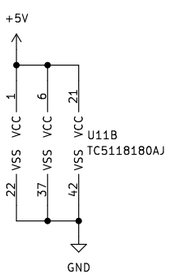
Title: CPU

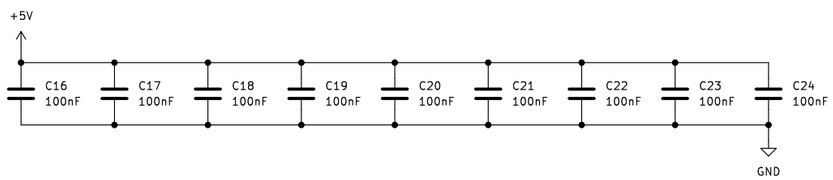
Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 3/12







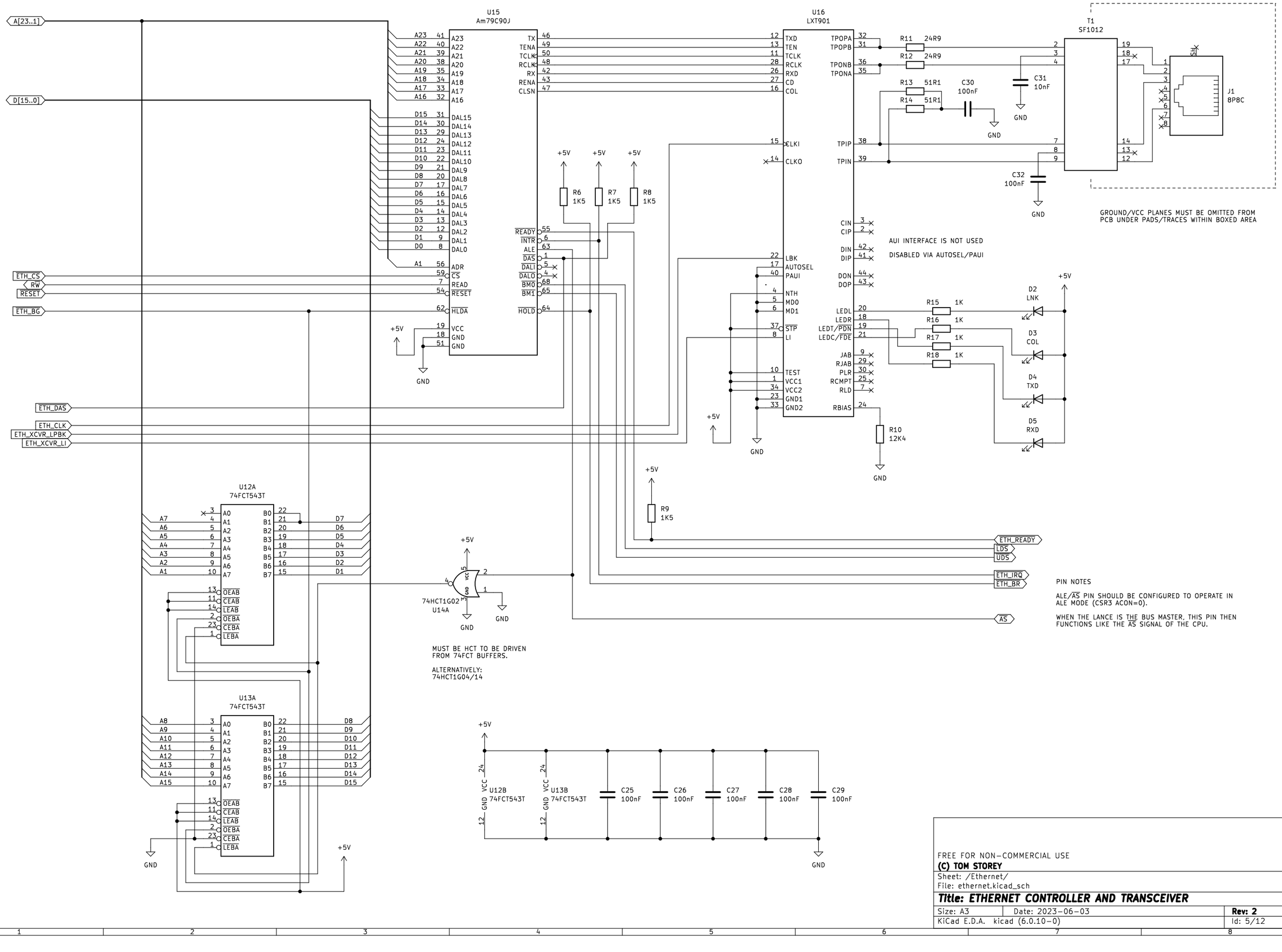




Sheet: /Memory/
File: memory.kicad_sch

Title: *MEMORY*

Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 4/12



Sheet: /Ethernet/		
File: ethernet.kicad_sch		
Title: ETHERNET CONTROLLER AND TRANSCEIVER		
Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 5/12

U17A
TL16C2552FN

U19
MAX232

U20
MAX232

U21
MAX232

U17B
TL16C2552FN

U18A
74LVC1G32

RN18
10K

RN19
10K

X3
7.3728MHz

R19
0R

C34
100nF

C33
100nF

C35
100nF

C36
100nF

C37
100nF

C38
100nF

C39
1uF

C40
1uF

C41
1uF

C42
1uF

C43
1uF

C44
1uF

C45
1uF

C46
1uF

C47
1uF

C48
1uF

C49
1uF

C50
1uF

J2
8P8C

J3
8P8C

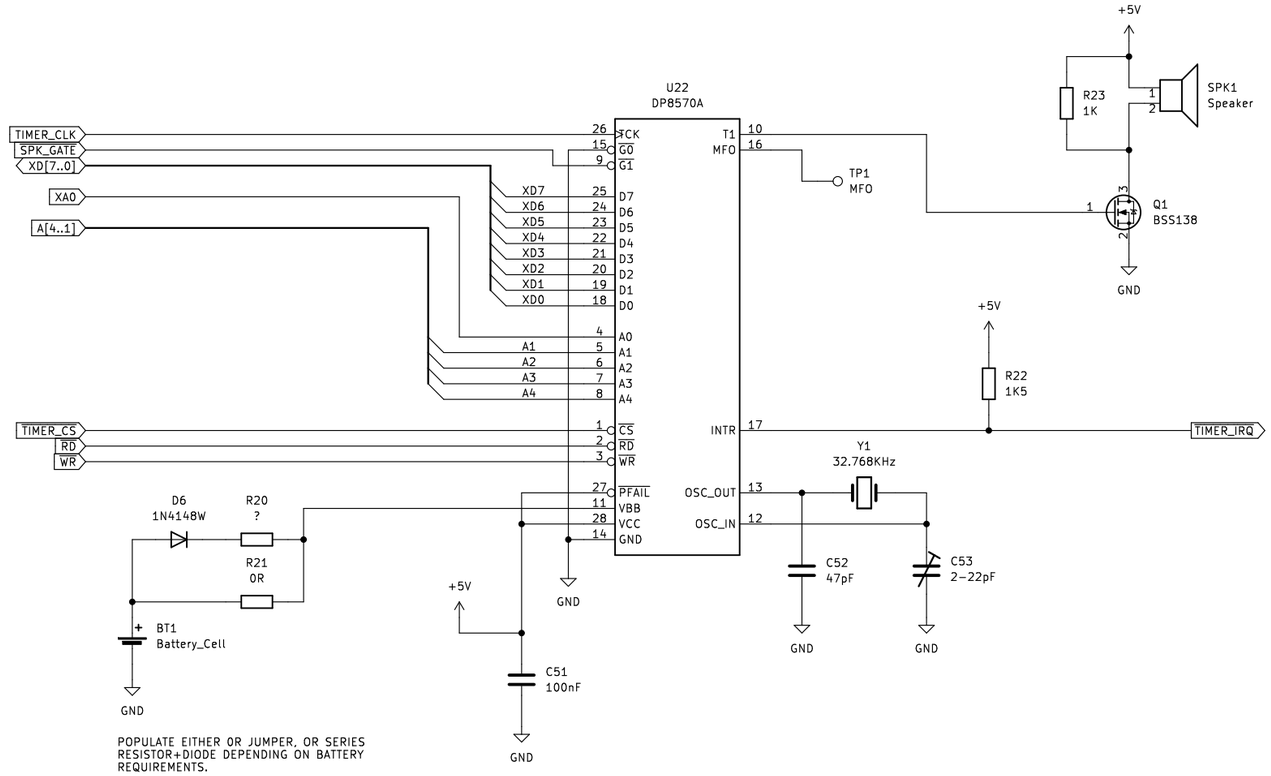
NO-POPULATE
UNLESS MODEM
CONTROL SIGNALS
ARE REQUIRED

NO-POPULATE
UNLESS MODEM
CONTROL SIGNALS
ARE REQUIRED

Sheet: /UART/
File: uart.kicad_sch

Title: UART AND LINE TRANSCEIVERS

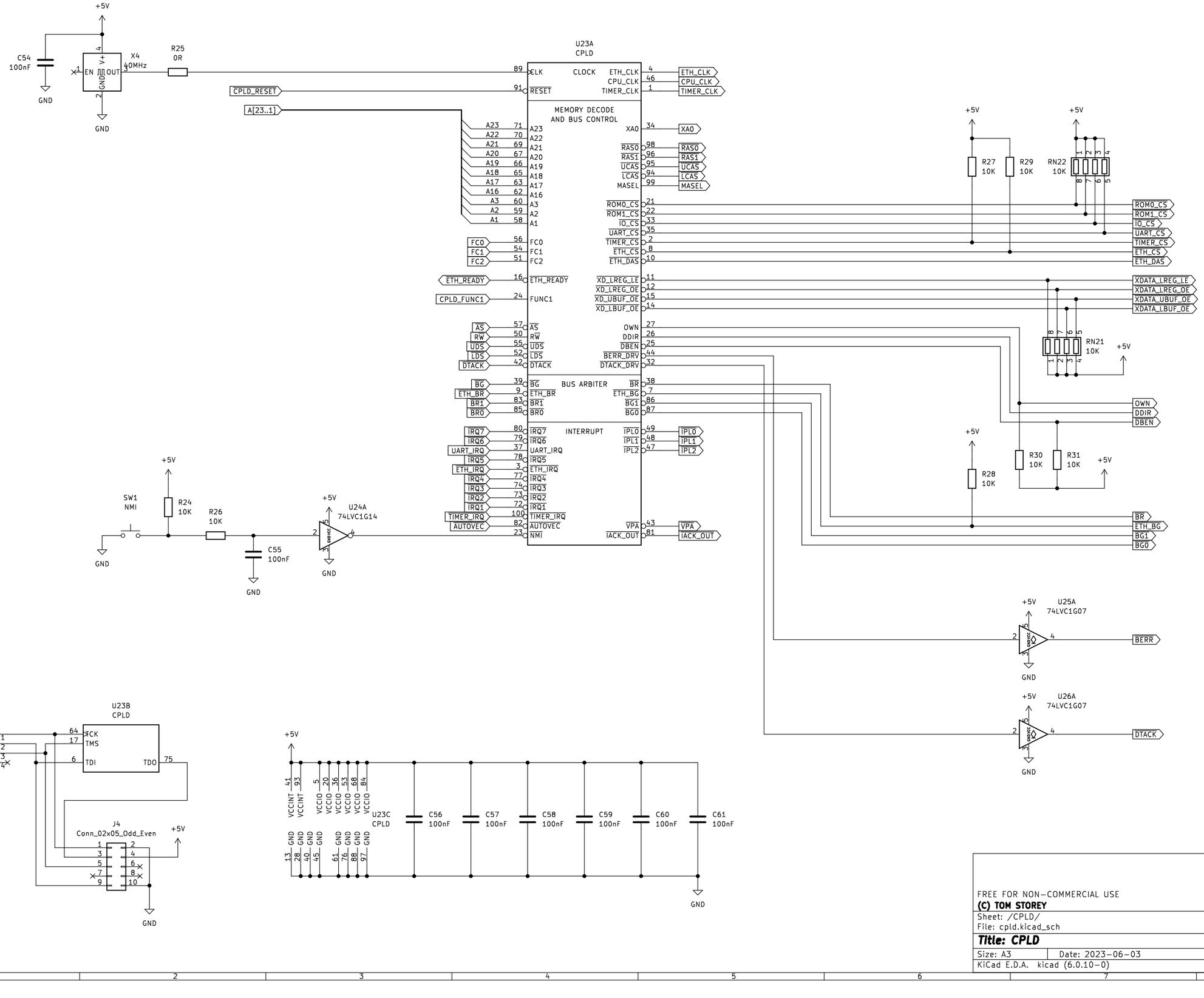
Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 6/12



Sheet: /Timer & RTC/
File: timer_rtc.kicad_sch

Title: RTC/TIMERS AND SPEAKER

Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 7/12



Sheet: /CPLD/
File: cpld.kicad_sch

Title: CPLD

Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 8/12

IO DECODE SUMMARY

OFFSET	WRITE	READ	FUNCTION
0	X	X	READ/WRITE CONTROL REGISTER 1
1	X	X	READ/WRITE CONTROL/STATUS REGISTER 2
2		X	WATCHDOG TIMER RESET
3		X	SOFTWARE RESET (IF ENABLED VIA CSR 2)

CONTROL REGISTER 1

RW-x	RW-x	RW-x	RW-x	RW-x	RW-x	RW-x	RW-x
CPLD_FUNC1	SPK_GATE	ETH_LI	ETH_LPBK	LED_D	LED_C	LED_B	LED_A
BIT 7							BIT 0

BIT 7 CPLD_FUNC1: CPLD FUNCTION 1
0 = LOGIC LOW TO CPLD PIN
1 = LOGIC HIGH TO CPLD PIN

BIT 6 SPK_GATE: SPEAKER GATE
1 = SPEAKER TIMER IS GATED
0 = SPEAKER TIMER IS RUNNING

BIT 5 ETH_LI: ETHERNET LINK INTEGRITY TEST
1 = LINK INTEGRITY TEST ENABLED
0 = LINK INTEGRITY TEST DISABLED

BIT 4 ETH_LPBK: ETHERNET LOOPBACK
1 = LOOPBACK ENABLED
0 = LOOPBACK DISABLED

BIT 3 LED_D: LED D CONTROL
1 = LED OFF
0 = LED ON

BIT 2 LED_C: LED C CONTROL
1 = LED OFF
0 = LED ON

BIT 1 LED_B: LED B CONTROL
1 = LED OFF
0 = LED ON

BIT 0 LED_A: LED A CONTROL
1 = LED OFF
0 = LED ON

CONTROL/STATUS REGISTER 2

R-1	R-0	RW-0	RW-0	R-x	R-x	R-x	R-x
POR	WDTO	SOFT_RST_EN	WDT_EN	CONFIG3	CONFIG2	CONFIG1	CONFIG0
BIT 7							BIT 0

BIT 7 POR: POWER ON RESET FLAG (1)(3)
1 = POWER ON RESET OCCURRED
0 = NORMAL RESET

BIT 6 WDTO: WATCHDOG TIMEOUT FLAG (2)(3)
1 = WATCHDOG TIMEOUT CAUSED RESTART
0 = NORMAL RESET

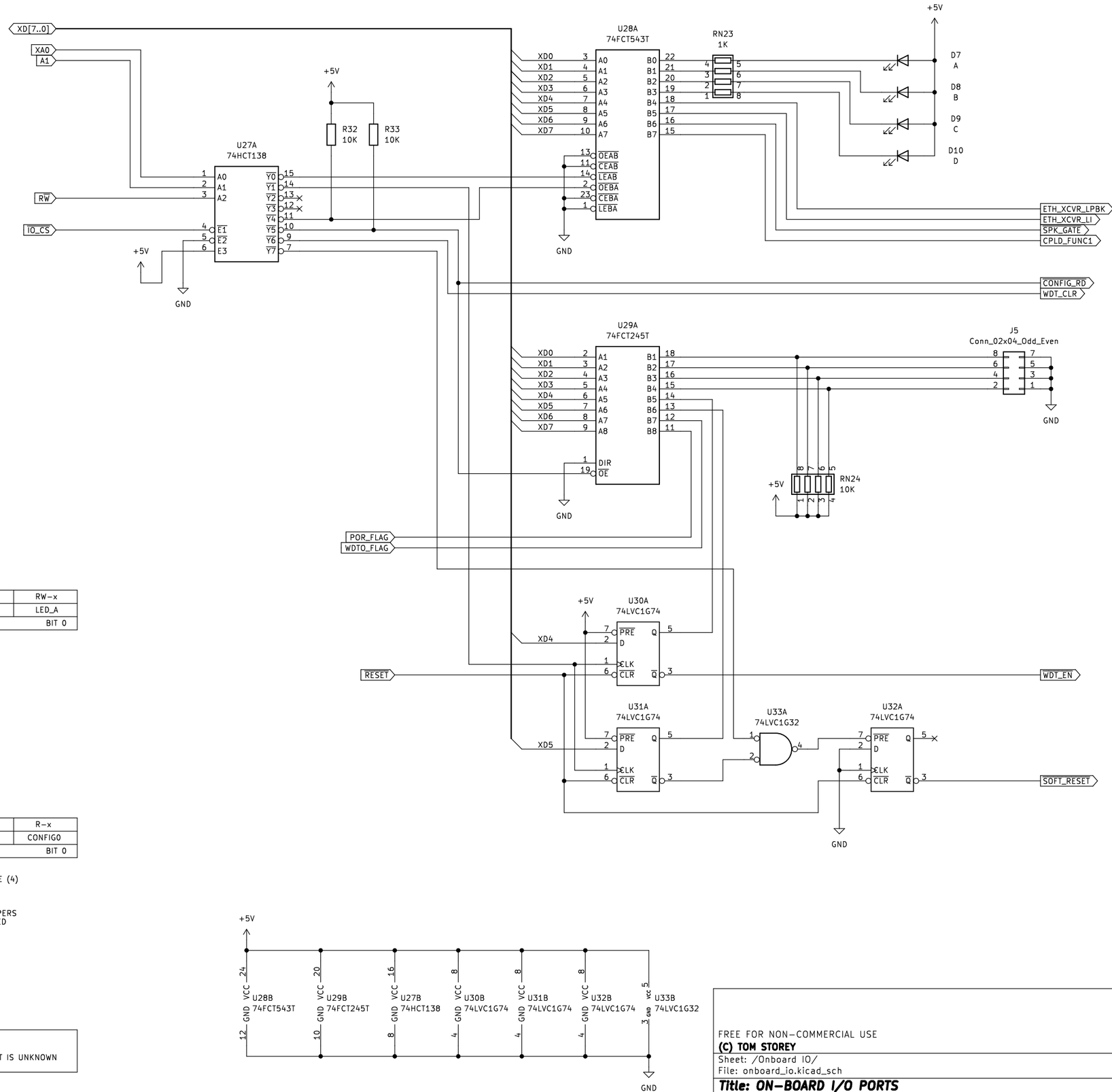
BIT 5 SOFT_RST_EN: SOFTWARE RESET ENABLE (4)
1 = SOFTWARE RESET MAY BE INITIATED
0 = SOFTWARE RESET IS INHIBITED

BIT 4 WDT_EN: WATCHDOG TIMER ENABLE (4)
1 = WATCHDOG IS ENABLED
0 = WATCHDOG IS DISABLED

BIT 3-0 CONFIG3..0: CONFIGURATION JUMPERS
1 = OPEN, JUMPER NOT INSTALLED
0 = CLOSED, JUMPER INSTALLED

NOTE 1: BIT IS SET DURING POWER UP, OR BROWNOUT IF VOLTAGE DROPS TO 4V OR LESS.
NOTE 2: BIT IS SET IN THE EVENT OF A WATCHDOG TIMEOUT. BIT IS CLEARED BY POR OR BROWNOUT.
NOTE 3: BIT IS CLEARED AFTER CONTROL/STATUS REGISTER 2 IS READ.
NOTE 4: BIT IS CLEARED FOLLOWING ANY RESET CAUSE.

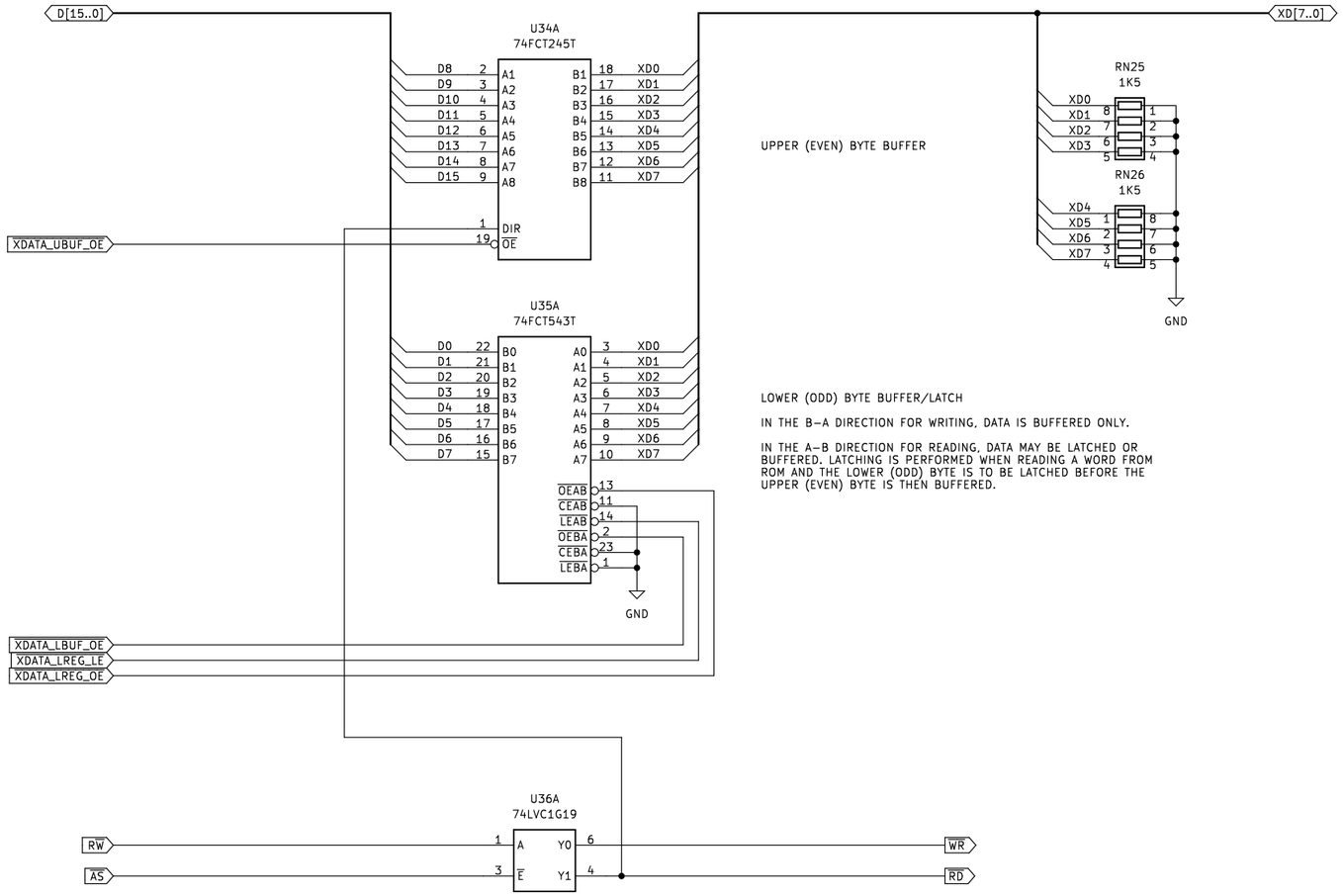
LEGEND:
R = READABLE BIT
-n = VALUE AT POR
W = WRITABLE BIT
1 = BIT IS SET
U = UNIMPLEMENTED BIT
0 = BIT IS CLEARED
x = BIT IS UNKNOWN



Sheet: /Onboard IO/
File: onboard_io.kicad_sch

Title: ON-BOARD I/O PORTS

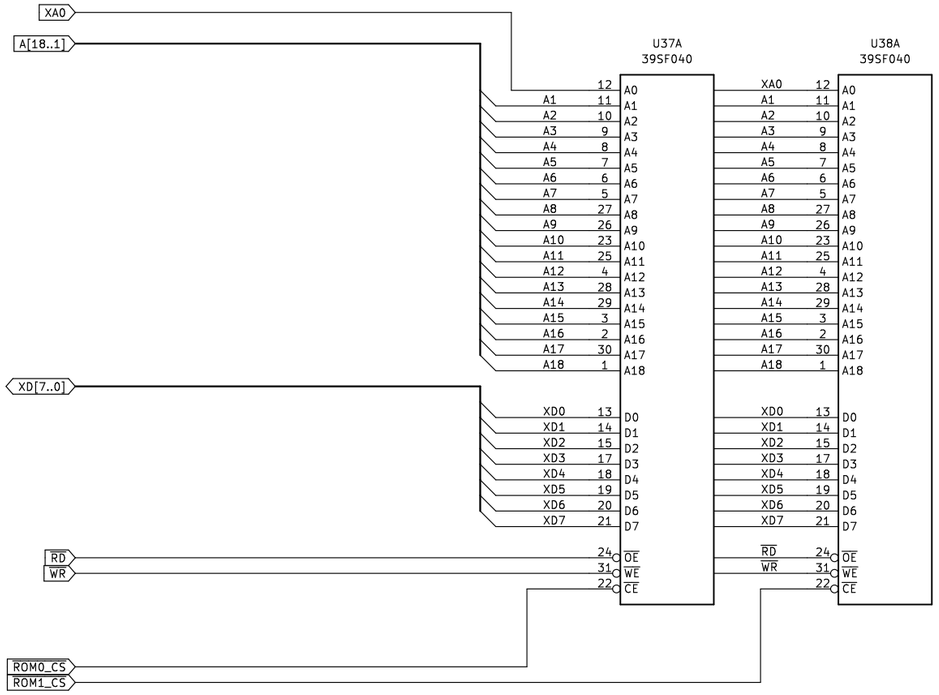
Size: A3	Date: 2023-06-03	Rev: 2
KiCad E.D.A. kicad (6.0.10-0)		Id: 9/12

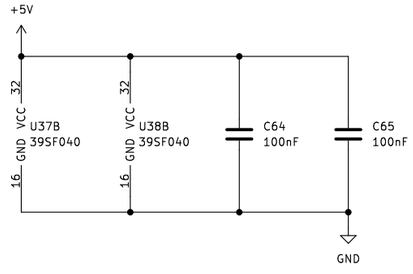


Sheet: /X busses/
File: xbusses.kicad_sch

Title: X–BUS

Size: A3	Date: 2023–06–03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10–0)		Id: 10/12



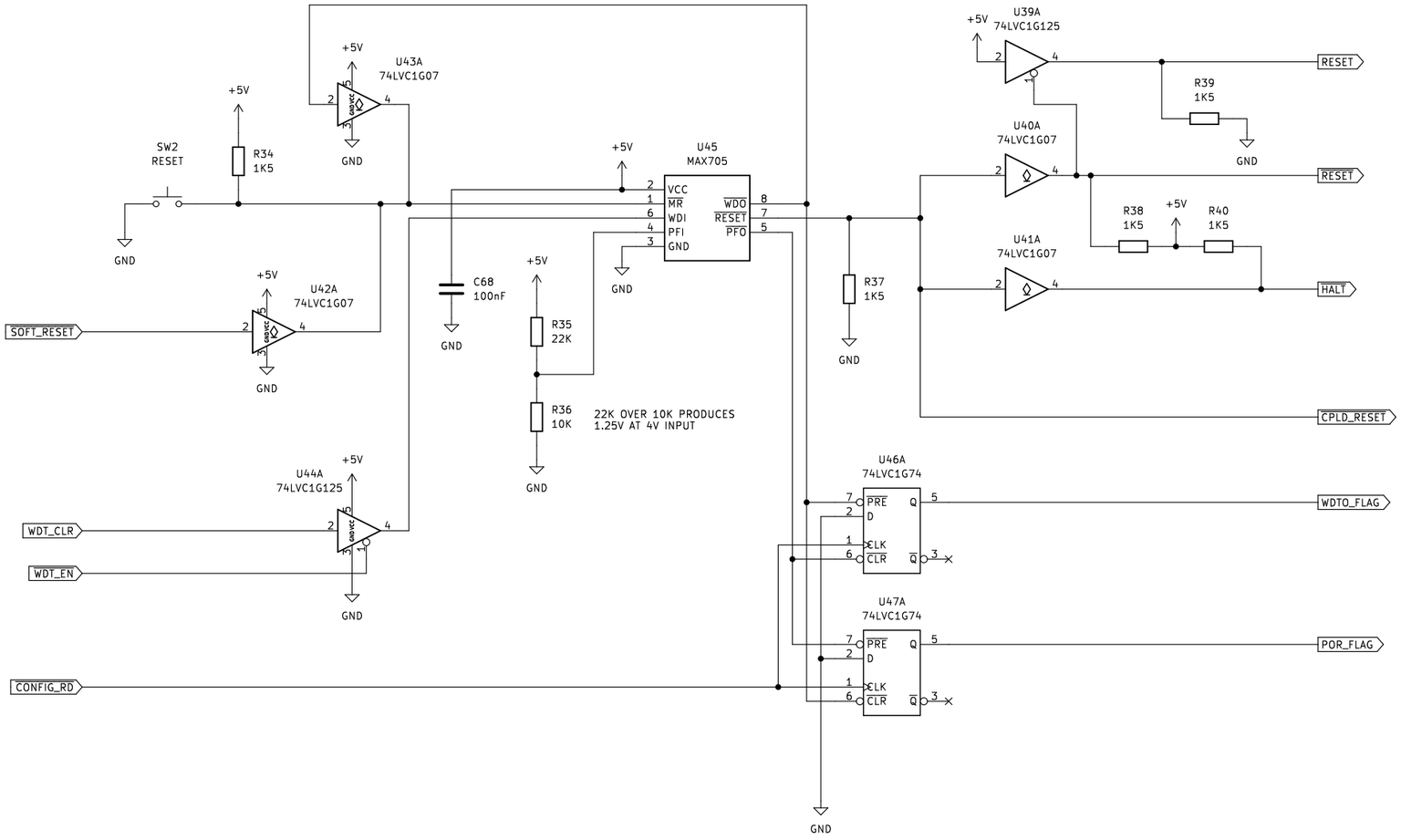


Sheet: /ROM/
File: rom.kicad_sch

Title: ROM SOCKETS

Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 11/12

THE "RESET" SIGNAL IS THE COMPLEMENT OF $\overline{\text{RESET}}$ SPECIFICALLY SO THAT IF THE CPU ASSERTS $\overline{\text{RESET}}$, THEN THIS WILL CAUSE ALL PERIPHERALS USING A POSITIVE RESET SIGNAL TO BE RESET AS WELL.



RESET CAUSE TRUTH TABLE

POR	WDTO	CAUSE
0	0	SOFTWARE
0	1	WATCHDOG TIMEOUT
1	0	POWER ON RESET OR BROWNOUT
1	1	INVALID COMBINATION

Sheet: /Reset/
File: reset.kicad_sch

Title: RESET, VOLTAGE SUPERVISOR, WATCHDOG

Size: A3	Date: 2023-06-03	**Rev: 2**
KiCad E.D.A. kicad (6.0.10-0)		Id: 12/12