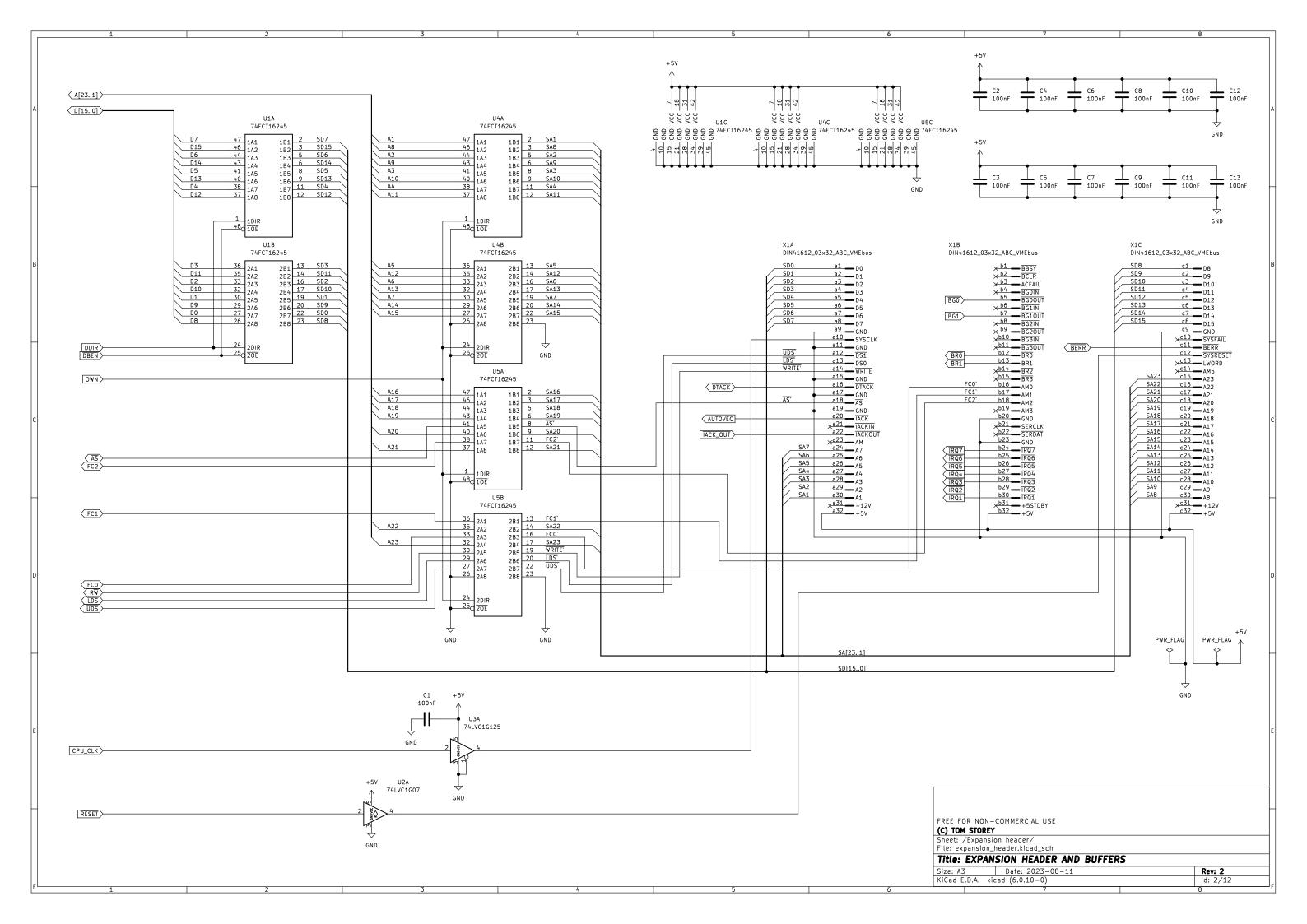
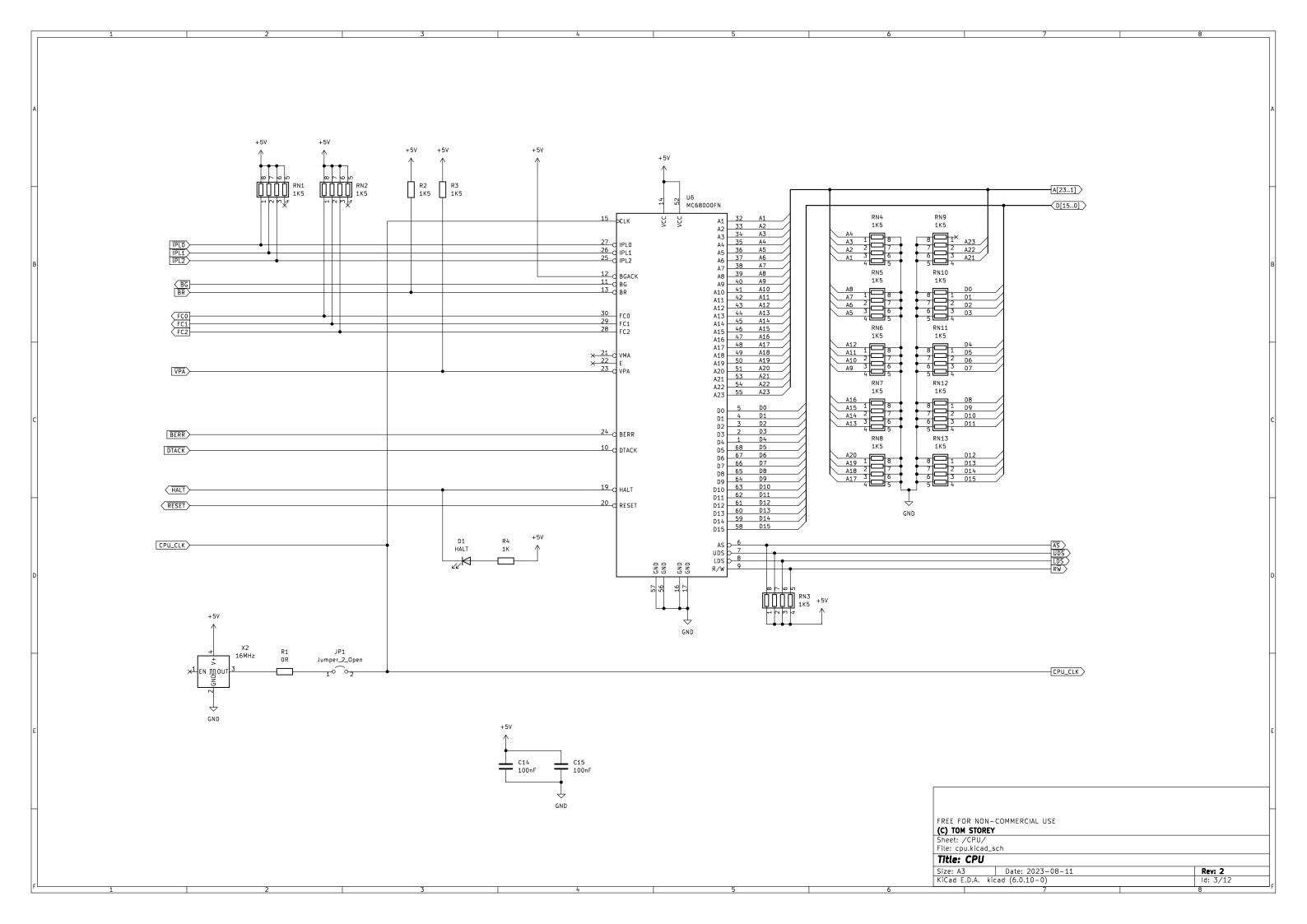
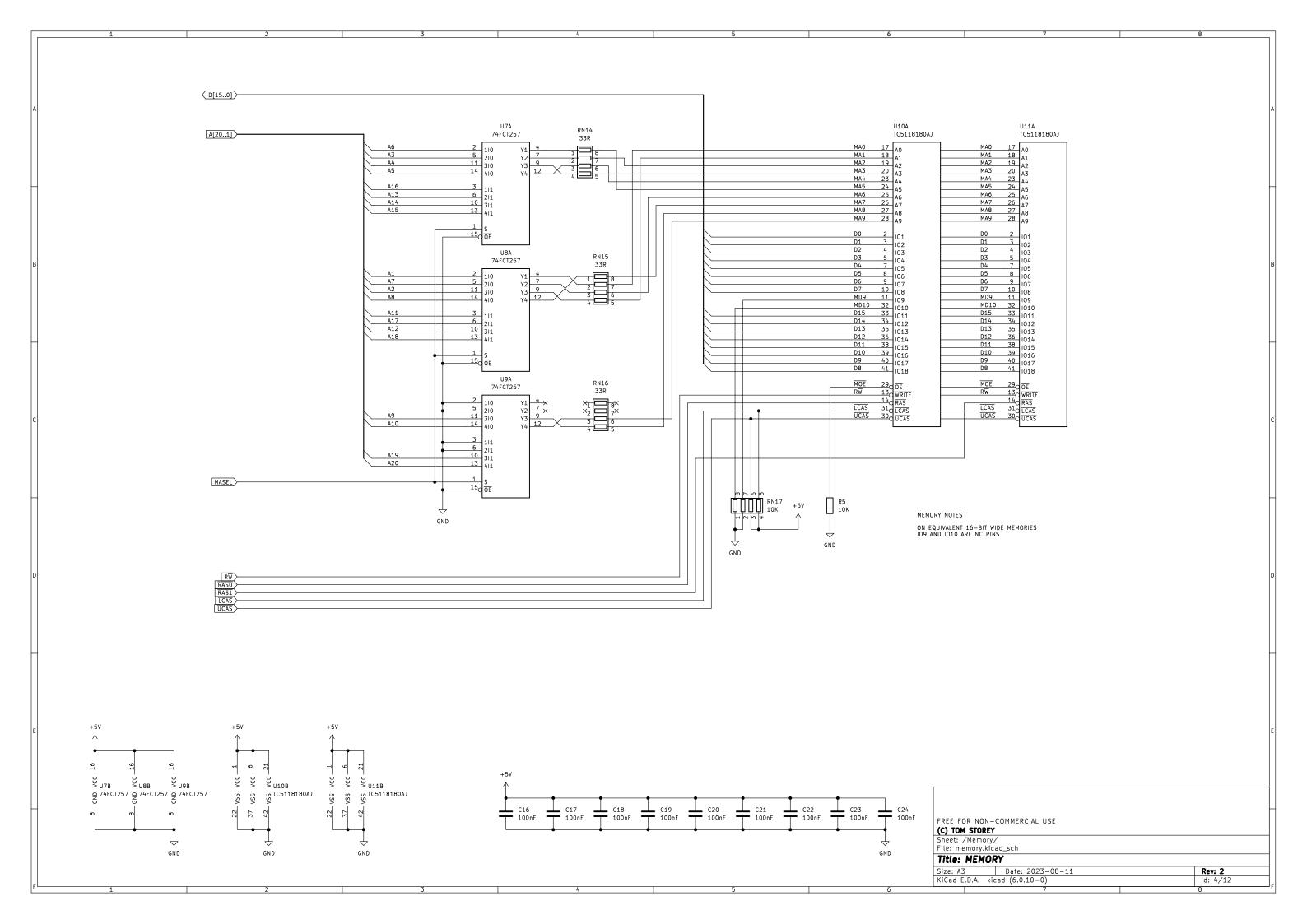
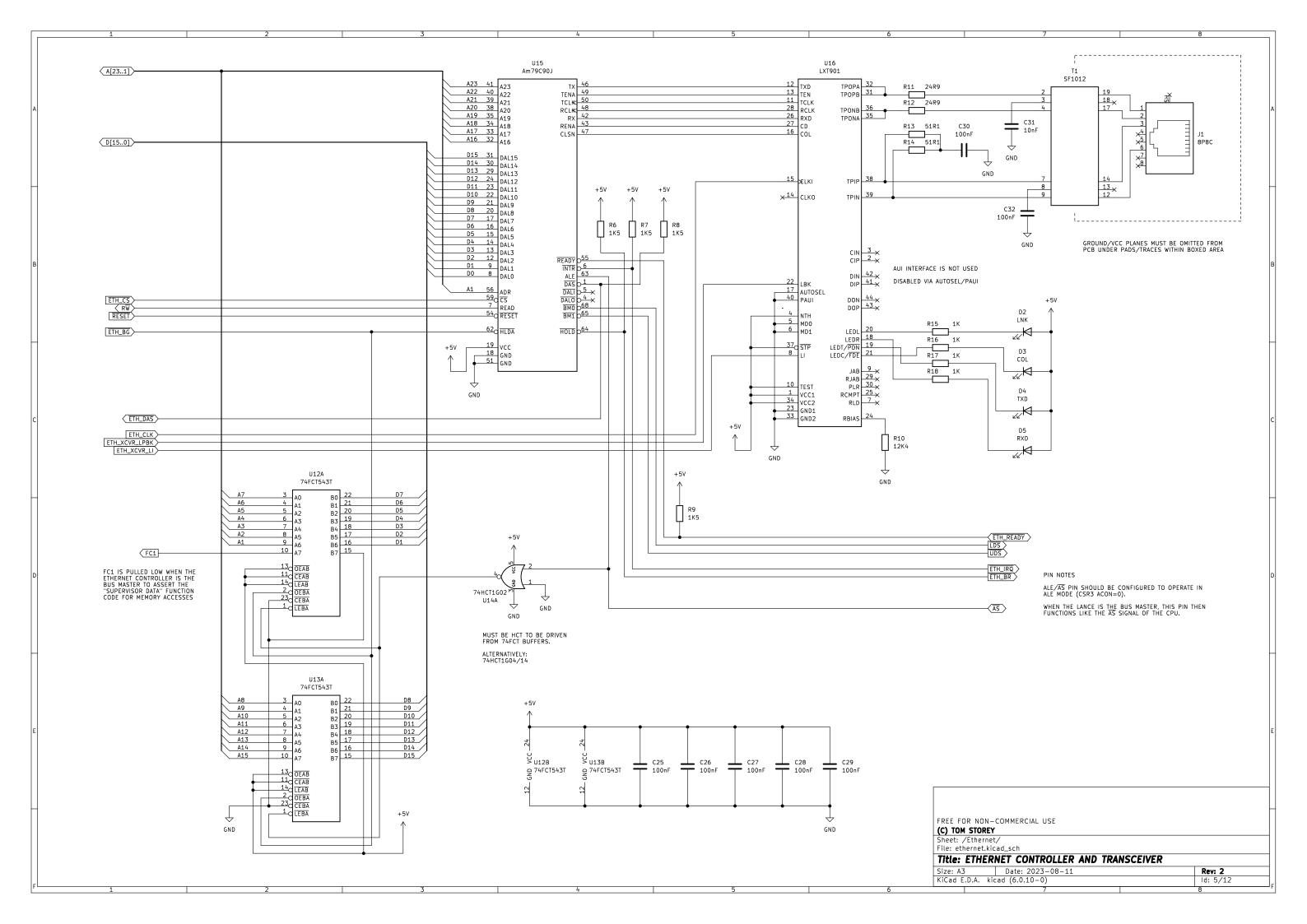
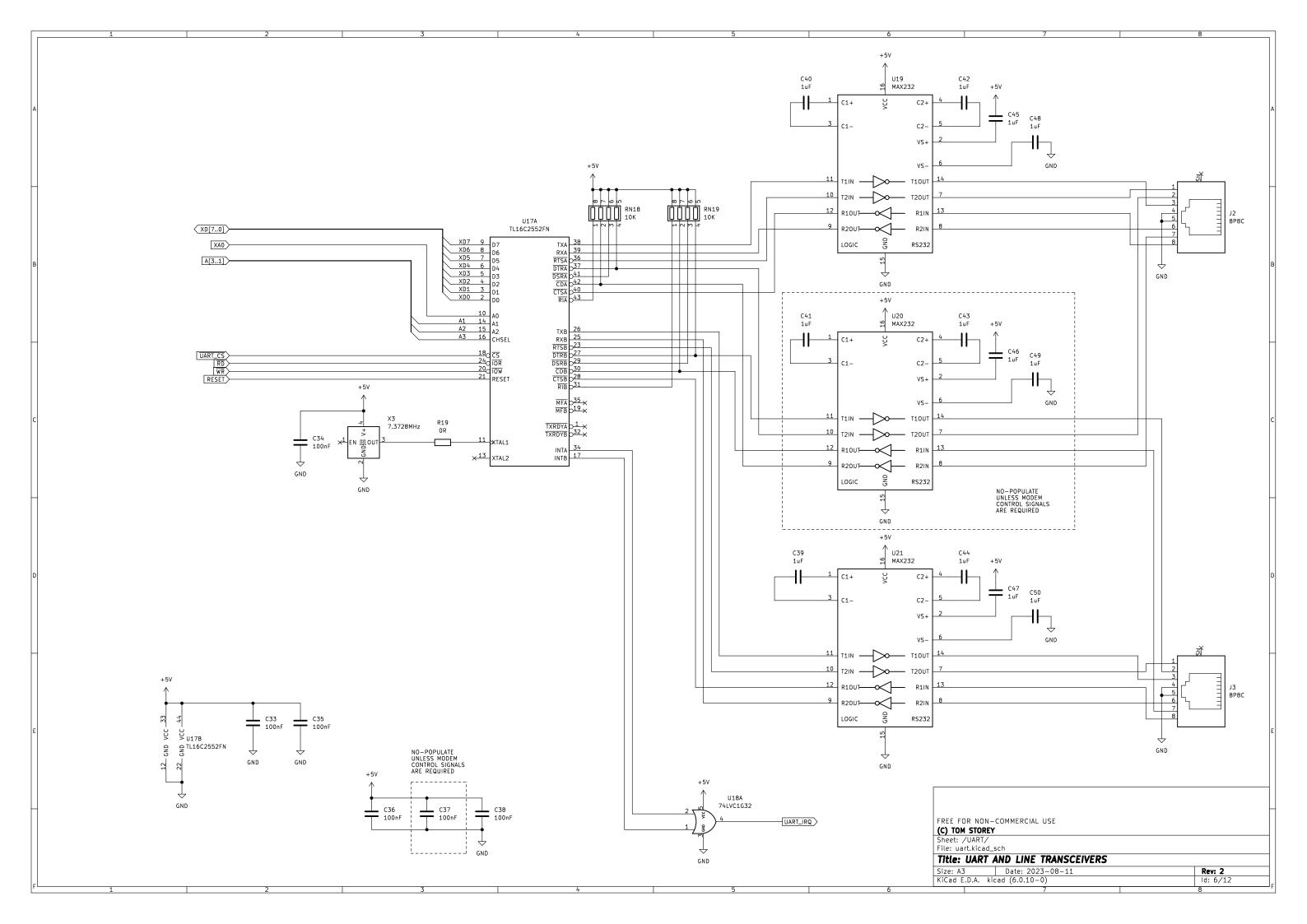
Expansion header Memory Ethernet UART Timer & RTC File: expansion_header.kicad_sch File: cpu.kicad_sch File: memory.kicad_sch File: ethernet.kicad_sch File: uart.kicad_sch File: timer_rtc.kicad_sch CPLD Onboard 10 X busses File: reset.kicad_sch File: cpld.kicad_sch File: onboard_io.kicad_sch File: xbusses.kicad_sch File: rom.kicad_sch FREE FOR NON-COMMERCIAL USE
(C) TOM STOREY
Sheet: /
File: COMET68k.kicad_sch

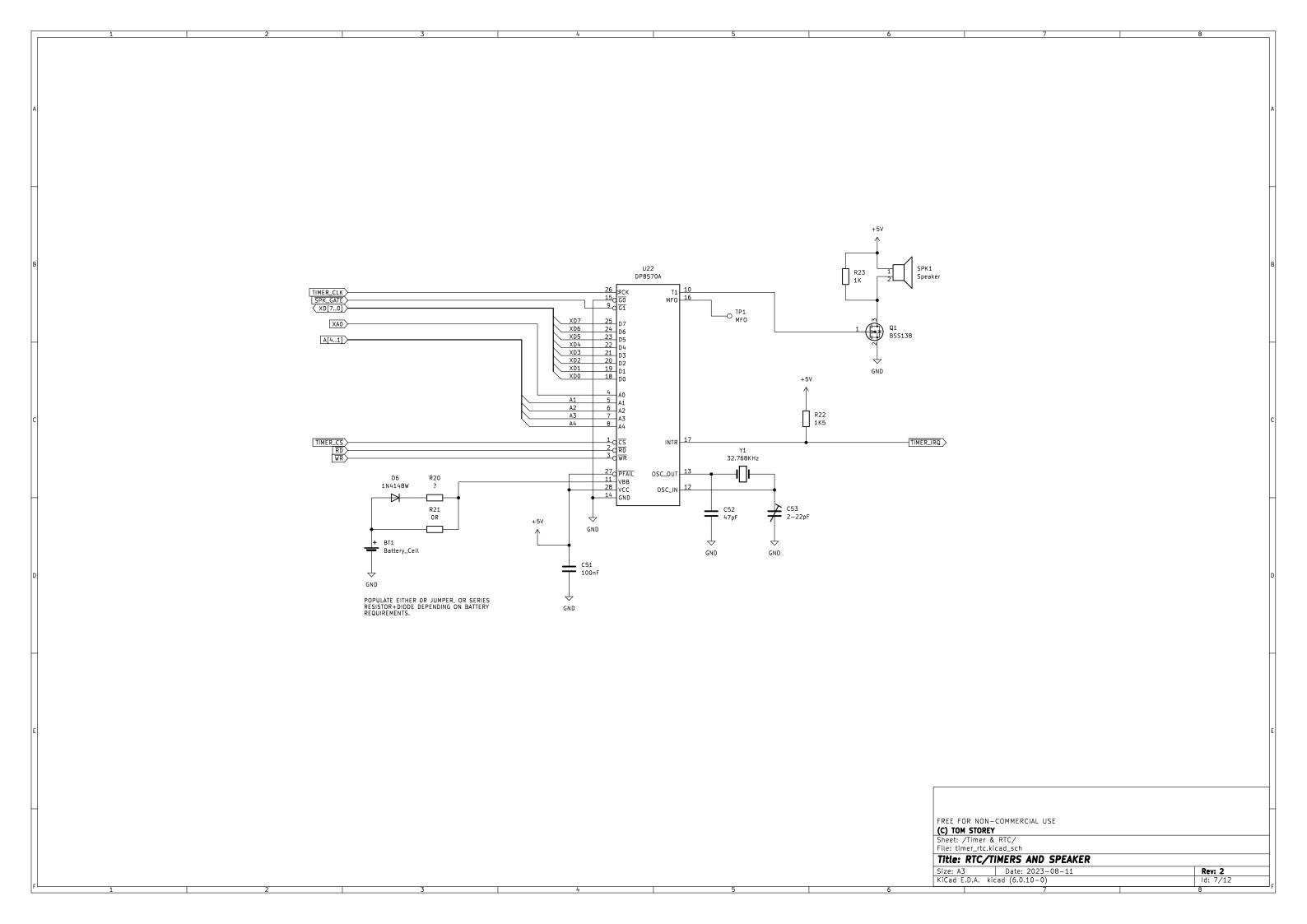


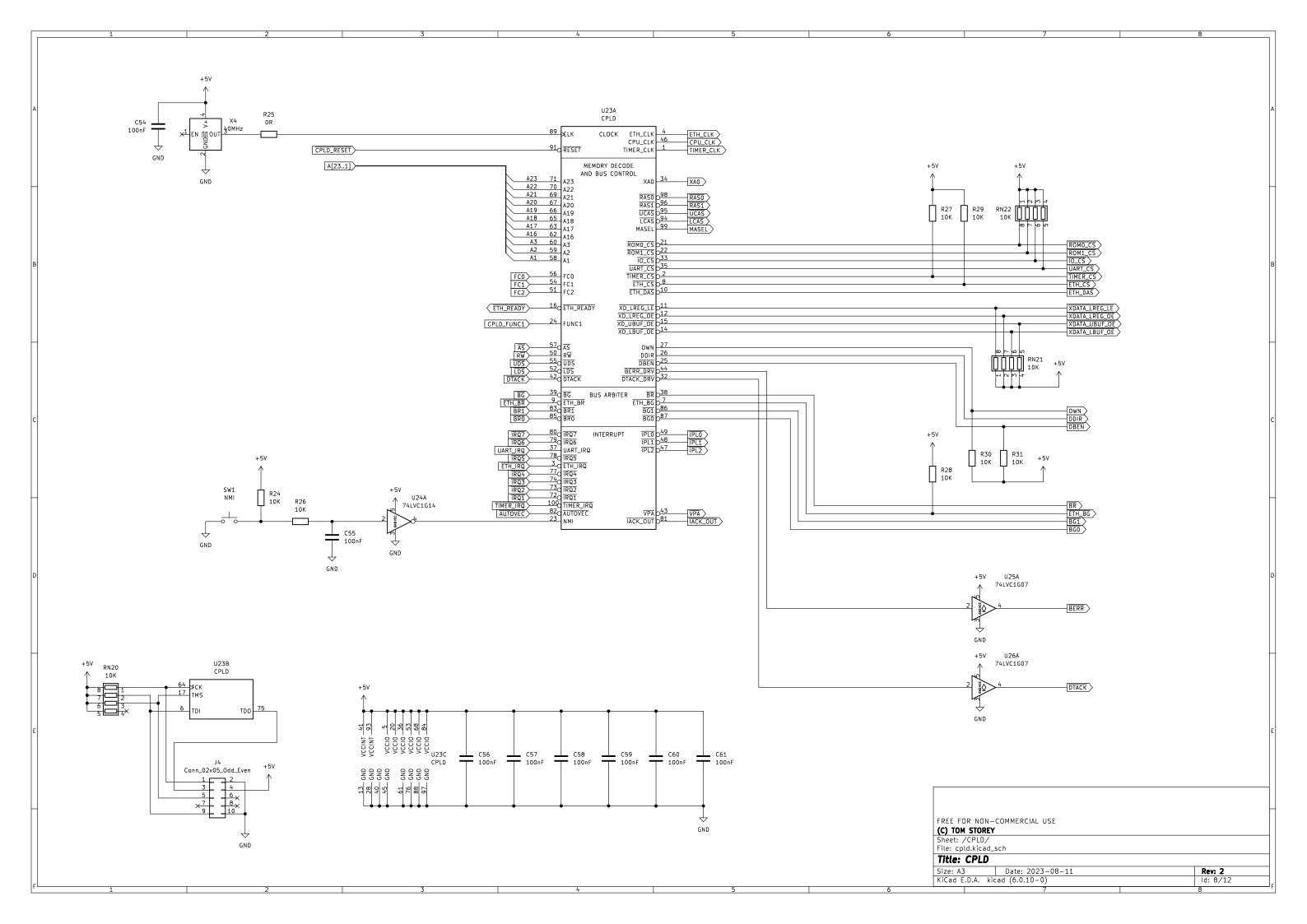












+5٧ U28A 74FCT543T XD[7..0] RN23 XA0 XD1 +5٧ XD3 XD4 -LL XD5 —<u>//</u> 9 10 A6 A7 XD6 B6 16 B7 15 R32 R33 10K U27A D10 130 OEAB 74HCT138 11C CEAB 14C LEAB 2C OEBA 23C CEBA 1 LEBA 71 014 72 013 × 73 012 × 74 011 75 010 76 0 9 $R\overline{W}$ ETH_XCVR_LPBK SPK_GATE ĪO_CS IO DECODE SUMMARY CPLD_FUNC1) OFFSET WRITE READ FUNCTION GND READ/WRITE CONTROL REGISTER 1 READ/WRITE CONTROL/STATUS REGISTER 2 WATCHDOG TIMER RESET SOFTWARE RESET (IF ENABLED VIA CSR 2) CONFIG_RD WDT_CLR GND U29A 74FCT245T Conn_02x04_0dd_Even XD1 B3 16 XD3 B4 15 XD4 XD5 XD6 B7 12 B8 11 GND 9 A8 XD7 19 DIR GND POR_FLAG CONTROL REGISTER 1 RW-x RW-x RW-xRW-xRW-xRW-xRW-xRW-x+5٧ U30A CPLD_FUNC1 SPK_GATE ETH_LI ETH_LPBK LED_D LED_C LED_B LED_A 74LVC1G74 BIT 0 LED_D: LED D CONTROL 1 = LED OFF 0 = LED ON CPLD_FUNC1: CPLD FUNCTION 1 0 = LOGIC LOW TO CPLD PIN 1 = LOGIC HIGH TO CPLD PIN BIT 7 RESET der R WDT_EN SPK_GATE: SPEAKER GATE 1 = SPEAKER TIMER IS GATED 0 = SPEAKER TIMER IS RUNNING LED_C: LED C CONTROL 1 = LED OFF 0 = LED ON U31A U32A ETH_LI: ETHERNET LINK INTEGRITY TEST 1 = LINK INTEGRITY TEST ENABLED 0 = LINK INTEGRITY TEST DISABLED LED_B: LED B CONTROL 1 = LED OFF 0 = LED ON U33A 74LVC1G74 74LVC1G74 74LVC1G32 PRE PRE BIT 4 ETH_LPBK: ETHERNET LOOPBACK 1 = LOOPBACK ENABLED 0 = LOOPBACK DISABLED BIT 0 LED_A: LED A CONTROL 1 = LED OFF 1 = LED O... 0 = LED ON 6 CLR 6 CLR SOFT_RESET CONTROL/STATUS REGISTER 2 R-1 R-0 RW-0 RW-0 R-x R-x POR WDTO SOFT_RST_EN WDT_EN CONFIG3 CONFIG2 CONFIG1 CONFIG0 GND BIT 7 POR: POWER ON RESET FLAG (1)(3)(5) 1 = POWER ON RESET OCCURRED 0 = NORMAL RESET WDT_EN: WATCHDOG TIMER ENABLE (4) 1 = WATCHDOG IS ENABLED 0 = WATCHDOG IS DISABLED WDTO: WATCHDOG TIMEOUT FLAG (2)(3)(5) 1 = WATCHDOG TIMEOUT CAUSED RESTART 0 = NORMAL RESET BIT 3-0 CONFIG3..0: CONFIGURATION JUMPERS 1 = OPEN, JUMPER NOT INSTALLED 0 = CLOSED, JUMPER INSTALLED +5٧ BIT 5 SOFT_RST_EN: SOFTWARE RESET ENABLE (4) 1 = SOFTWARE RESET MAY BE INITIATED 0 = SOFTWARE RESET IS INHIBITED NOTE 1: BIT IS SET DURING POWER UP, OR BROWNOUT IF VOLTAGE DROPS TO 4V OR LESS.
NOTE 2: BIT IS SET IN THE EVENT OF A WATCHDOG TIMEOUT. BIT IS CLEARED BY POR OR BROWNOUT.
NOTE 3: BIT IS CLEARED AFTER CONTROL/STATUS REGISTER 2 IS READ.
NOTE 4: BIT IS CLEARED FOLLOWING ANY RESET CAUSE.
NOTE 5: REFER TO RESET SHEET FOR NOTES ABOUT RESET CAUSE FLAG LIMITATIONS. S U28B Ş U32B ≥ U30B ¥ U31B ≥ u33B ≥ U29B ≥ U27B 974LVC1G74 974LVC1G74 974LVC1G74 874LVC1G32 ⊋ 74FCT543T 74FCT245T ⊋ 74HCT138 FREE FOR NON-COMMERCIAL USE LEGEND: R = READABLE BIT -n = VALUE AT POR (C) TOM STOREY W = WRITABLE BIT 1 = BIT IS SET U = UNIMPLEMENTED BIT O = BIT IS CLEARED Sheet: /Onboard IO/ File: onboard_io.kicad_sch x = BIT IS UNKNOWN Title: ON-BOARD I/O PORTS GND Size: A3 Date: 2023-08-11 KiCad E.D.A. kicad (6.0.10-0)

