

POSITIONS

Assistant Professor – ECE Department, University of Utah 2019—present
Research Assistant Professor – ECE Department, University of Illinois at Urbana-Champaign 2018—2019

EDUCATION





PhD – ECE Department, University of Illinois at Urbana-Champaign, IL, USA 2013—2017
BS/MS – CS Department, National Cheng Kung University, Tainan, Taiwan 2006—2011

RESEARCH INTERESTS

I create novel software systems to streamline the building of high-performance scientific computing applications.

SOFTWARE

I prioritize both technical and system innovations. My software releases have accumulated more than **1.5M downloads** and **6K stars** in GitHub repositories, being used by many academic research prototypes and industrial production projects.

Software	GitHub
 Taskflow: A General-purpose Parallel and Heterogeneous Task Computing System	https://github.com/taskflow/taskflow <ul style="list-style-type: none"> • 2020 IEEE HPEC Graph Challenge Champion Award • 2019 ACM Multimedia Best Open-source Software Award • 2018 C++ Conference Best Poster Award in Parallelism
 SNIG: A Novel Inference Engine for Large Sparse Neural Network using Task Graph Parallelism	https://github.com/dian-lun-lin/SNIG <ul style="list-style-type: none"> • 2020 IEEE HPEC Graph Challenge Champion Award
 OpenTimer: A High-performance Timing Analysis Tool for VLSI Systems	https://github.com/OpenTimer/OpenTimer <ul style="list-style-type: none"> • 2019 ACM SIGDA Outstanding PhD Dissertation Award • 2018 WOS@ICCAD Best EDA Software Tool • 2014–2016 ACM TAU Contest Top-3 Winners • 2014–2016 Golden Timers of ACM TAU Contests
 DtCraft: A General-purpose Distributed Programming System using Data-parallel Streams	https://github.com/twhuang-uiuc/DtCraft <ul style="list-style-type: none"> • 2018 ACM Multimedia Best Open-source Software Award

SELECTED AWARDS

- Humboldt Research Fellowship Award, Alexander von Humboldt Foundation, 2022-2025
- Faculty Early Career Development Program (CAREER) Award, NSF, 2022
- Best Paper Award for “GPU-Accelerated Path-based Timing Analysis”, ACM TAU Workshop, 2021
- Champion of the IEEE/MIT/Amazon HPEC Large Sparse Neural Network Challenge, 2020
- 2nd Place (Taskflow), Open-source Software Competition, ACM Multimedia Conference, 2019
- ACM SIGDA Outstanding PhD Dissertation Award (thesis title: “Distributed Timing Analysis”), 2019
- Best Tool Award (OpenTimer), Workshop on Open-source EDA Technology, 2018
- Best Open-source Software Award (DtCraft), ACM Multimedia Conference, 2018
- Best Poster Award for Open-source Parallel Programming Library (Taskflow), CPP Conference, 2018
- 2nd and 1st Place, ACM/SIGDA CADathlon International Programming Contest, 2014 and 2017
- 1st, 2nd, and 1st Place, ACM TAU Timing Analysis Contest, 2014 through 2016
- Yi-Min Wang and Pi-Yu Chung Endowed Research Award, ECE Dept. UIUC, 2016
- Rambus Computer Engineering Fellowship, ECE Dept. UIUC, 2015—2016
- Study Abroad Scholarship for Outstanding EECS Students, Ministry of Education, Taiwan, 2013—2014
- 2nd Place, ACM Student Research Competition Grand Final, ACM Annual Award Banquet, 2011

- Best Master’s Thesis Award, Taiwan Institute of Electrical and Electronic Engineering, 2011
- Best Master’s Thesis Award, IEEE Taiwan Tainan Section, 2011
- Best Master’s Thesis Award, Taiwan Institute of Information and Computing Machinery, 2011
- 1st Place, Master’s Thesis Contest, Chinese Institute of Electrical Engineering, Taiwan, 2011
- Outstanding Graduate Recruiting Fellowship, National Cheng Kung University, 2010
- Outstanding Student Scholarship, Garmin Corporation, Taiwan, 2010
- 1st Place, ACM/SIGDA Student Research Competition, Design Automation Conference, 2010
- 3rd Place, National Collegiate Cell-Based IC Design Contest, Ministry of Education, Taiwan, 2010
- Distinguished Engineering Student Fellowship, Chinese Institute of Engineers, Taiwan, 2009
- 1st Place, National Collegiate Nano Device CAD Contest, Nano Device Laboratories, Taiwan, 2009
- 3rd Place, National Collegiate Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, National Collegiate IC/CAD Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, Presidential Award in CS Department, National Cheng Kung University, Taiwan, 2009

RESEARCH GRANT

1. PI, “Taskflow with Constrained Parallelism,” \$16K, 8/2022—8/2023, NSF Research Experience for Undergraduates (REU) Supplement (under CCF-2126672)
2. PI, “CAREER: Accelerating Static Timing Analysis with Intelligent Heterogeneous Parallelism,” \$500K, 2022—2027, NSF Faculty Early Career Development Program (CAREER), CCF-2144523
3. PI, “GPU Acceleration for Static Timing Analysis,” RTX 6000 24GB Donation (x2) through Nvidia Applied Research Acceleration Program, 11/2021 (valued at \$10K)
4. PI, “A General-purpose Parallel and Heterogeneous Task Graph Computing System for VLSI CAD,” \$403K, 10/2021—10/2024, NSF Computer and Information Science and Engineering (CISE), CCF-2126672
5. PI, “Standard GPU Algorithms with Task Graph Parallelism,” \$5K, 05/2021—02/2022, NumFOCUS
6. PI, “Taskflow-San: Sanitizing Erroneous Control Flows in Taskflow,” \$5K, 05/2021—02/2022, NumFOCUS
7. PI, “OpenTimer and DtCraft,” \$427K, 06/2018—07/2019, DARPA Intelligent Design of Electronic Assets (IDEA) Program, FA 8650-18-2-7843

CONFERENCE

1. Cheng-Hsiang Chiu and Tsung-Wei Huang, “Composing Pipeline Parallelism using Control Taskflow Graph,” *ACM International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, Minneapolis, Minnesota, 2022
2. Cheng-Hsiang Chiu and Tsung-Wei Huang, “Efficient Timing Propagation with Simultaneous Structural and Pipeline Parallelisms,” *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2022
3. Tsung-Wei Huang and Yibo Lin, “Concurrent CPU-GPU Task Programming using Modern C++,” *International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS)*, France, 2022
4. Kexing Zhou, Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, “Efficient Critical Paths Search Algorithm using Mergeable Heap,” *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Taiwan, 2022
5. Guannan Guo, Tsung-Wei Huang, and Martin Wong, “GPU-accelerated Path-based Timing Analysis,” *ACM/IEEE Design Automation Conference (DAC)*, CA, 2021
6. Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, “A Provably Good and Practically Efficient Common Path Pessimism Removal Algorithm for Large Designs,” *ACM/IEEE Design Automation Conference (DAC)*, CA, 2021
7. McKay Mower, Luke Majors, and Tsung-Wei Huang, “Taskflow-San: Sanitizing Erroneous Control Flow in Taskflow Programs,” *IEEE Workshop on Extreme Scale Programming Models and Middleware (ESPM2)*, St. Louis, Missouri, 2021
8. Tsung-Wei Huang, “TFProf: Profiling Large Taskflow Programs with Modern D3 and C++,” *IEEE International Workshop on Programming and Performance Visualization Tools (ProTools)*, St. Louis, Missouri, 2021
9. Dian-Lun Lin and Tsung-Wei Huang, “Efficient GPU Computation using Task Graph Parallelism,” *European Conference on Parallel and Distributed Computing (Euro-Par)*, Portugal, 2021
10. Yasin Zamani and Tsung-Wei Huang, “A High-Performance Heterogeneous Critical Path Analysis Framework,” *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2021
11. Cheng-Hsiang Chiu, Dian-Lun Lin and Tsung-Wei Huang, “An Experimental Study of SYCL Task Graph Parallelism for Large-Scale Machine Learning Workloads,” *International Workshop of Asynchronous Many-Task Systems for Exascale (AMTE)*, 2021
12. Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, “HeteroCPPR: Accelerating Common Path Pessimism Removal with

- Heterogeneous CPU-GPU Parallelism,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, Germany, 2021
13. Guannan Guo, Tsung-Wei Huang, Yibo Lin, and Martin Wong, “GPU-accelerated Critical Path Generation with Path Constraints,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, Germany, 2021
 14. Tsung-Wei Huang, Yu-Guan Chen, Chun-Yao Wang, and Takashi Sato, “Overview of 2021 CAD Contest at ICCAD,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, Germany, 2021
 15. Kuan-Ming Lai, Tsung-Wei Huang, Pei-Yu Lee, and Tsung-Yi Ho, “ATM: A High Accuracy Extracted Timing Model for Hierarchical Timing Analysis,” *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Tokyo, Japan, 2021
 16. Chun-Xun Lin, Tsung-Wei Huang, and Martin D. F. Wong, “An Efficient Work-Stealing Scheduler for Task Dependency Graph,” *IEEE International Conference on Parallel and Distributed Systems (ICPADS)*, Hong Kong, 2020
 17. D.-L. Lin and Tsung-Wei Huang, “A Novel Inference Algorithm for Large Sparse Neural Network using Task Graph Parallelism,” *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2020 (**Sparse Neural Network Graph Challenge Champion Award**)
 18. Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, “GPU-Accelerated Static Timing Analysis,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020
 19. Tsung-Wei Huang, “A General-purpose Parallel and Heterogeneous Task Programming System for VLSI CAD,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020
 20. Ing-Chao Lin, Ulf Schlichtmann, Tsung-Wei Huang, and Pao-Hun Lin, “Overview of 2020 CAD Contest at ICCAD,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020
 21. G. Guo, Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, “An Efficient Critical Path Generation Algorithm Considering Extensive Path Constraints,” *IEEE/ACM Design Automation Conference (DAC)*, San Francisco, CA, 2020
 22. Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo, and Martin D. F. Wong, “A Modern C++ Parallel Task Programming Library,” *ACM Multimedia Conference (MM)*, Nice, France, 2019 (**Second Prize of Open-Source Software Competition**)
 23. Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo, and Martin D. F. Wong, “An Efficient and Composable Parallel Programming Library,” *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2019
 24. Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, “Cpp-Taskflow: Fast Task-based Parallel Programming using Modern C++,” *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, Rio De Janeiro, Brazil, 2019
 25. Kuan-Ming Lai, Tsung-Wei Huang, and Tsung-Yi Ho, “A General Cache Framework for Efficient Generation of Timing Critical Paths,” *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019
 26. Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, “Essential Building Blocks for Creating an Open-source EDA Project,” *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019
 27. Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, “Distributed Timing Analysis at Scale,” *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019
 28. Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, “A General-purpose Distributed Programming Systems using Data-parallel Streams,” *ACM Multimedia Conference (MM)*, Seoul, Korea, 2018 (**Best Open-Source Software Award**)
 29. Chun-Xun Lin, Tsung-Wei Huang, G. Guo, and Martin D. F. Wong, “MtDetector: A High-performance Marine Traffic Detector at Stream Scale,” *ACM Distributed Event-based System Conference (DEBS)*, Hamilton, New Zealand, 2018
 30. Chun-Xun Lin, Tsung-Wei Huang, T. Yu, and Martin D. F. Wong, “A Distributed Power Grid Analysis Framework from Sequential Stream Graph,” *ACM Great Lakes Symposium (GLSVLSI)*, Chicago, IL, 2018
 31. Chun-Xun Lin, Tsung-Wei Huang, and Martin D. F. Wong, “Routing at Compile Time,” *IEEE International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, 2018
 32. Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, “DtCraft: A Distributed Execution Engine for Compute-intensive Applications,” *ACM/IEEE International Conference on Computer-aided Design (ICCAD)*, Irvine, CA, 2017
 33. Tin-Yin Lai, Tsung-Wei Huang, and Martin D. F. Wong, “An Effective and Accurate Macro-modeling Algorithm for Large Hierarchical Designs,” *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, 2017 (**First Place of TAU Timing Analysis Contest**)
 34. Tsung-Wei Huang, Martin D. F. Wong, D. Sinha, K. Kalafala, and N. Venkateswaran, “A Distributed Timing Analysis Framework for Large Designs,” *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, 2016
 35. Tsung-Wei Huang and Martin D. F. Wong, “OpenTimer: A High-performance Timing Analysis Tool,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, TX, 2015 (**Second Place of TAU Timing Analysis Contest**)
 36. Tsung-Wei Huang and Martin D. F. Wong, “On Fast Timing Closure: Speeding Up Incremental Path-Based Timing

- Analysis with MapReduce,” *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, CA, 2015
37. Tsung-Wei Huang and Martin D. F. Wong, “Accelerated Path-Based Timing Analysis with MapReduce,” *ACM International Symposium on Physical Design (ISPD)*, Monterey, CA, 2015
 38. Tsung-Wei Huang, P.-C. Wu, and Martin D. F. Wong, “Fast Path-Based Timing Analysis for CPPR,” *IEEE/ACM ACM/IEEE International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2014 (**First Place of TAU Timing Analysis Contest**)
 39. Tsung-Wei Huang, P.-C. Wu, and Martin D. F. Wong, “UI-Timer: An Ultra-Fast Clock Network Pessimism Removal Algorithm,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2014
 40. Tsung-Wei Huang, P.-C. Wu, and Martin D. F. Wong, “UI-Route: An Ultra-Fast Incremental Maze Routing Algorithm,” *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, San Francisco, CA, 2014
 41. S.-H. Yeh, J.-W. Chang, Tsung-Wei Huang, and Tsung-Yi Ho, “Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWO chips,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2012
 42. Tsung-Wei Huang, J.-W. Chang, and Tsung-Yi Ho, “Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips,” *ACM International Symposium on Physical Design (ISPD)*, Napa, CA, 2012
 43. J.-W. Chang, Tsung-Wei Huang, and Tsung-Yi Ho, “An ILP-based Obstacle-Avoiding Routing Algorithm for Pin-Constrained EWO chips,” *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Sydney, Australia, 2012
 44. Tsung-Wei Huang, Tsung-Yi Ho, and K. Chakrabarty, “Reliability-Oriented Broadcast Electrode-Addressing for Pin-Constrained Digital Microfluidic Biochips,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2011
 45. Tsung-Wei Huang, Yan-You Lin, J.-W. Chang, and Tsung-Yi Ho, “Recent Research and Emerging Challenges in the Designs and Optimizations for Digital Microfluidic Biochips,” invited paper, *IEEE System on Chip Conference (SOCC)*, 2011.
 46. Tsung-Wei Huang, Yan-You Lin, J.-W. Chang, and Tsung-Yi Ho, “Chip-Level Design and Optimization for Digital Microfluidic Biochips,” invited paper, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011.
 47. P.-H. Yuh, C. C.-Y. Lin, Tsung-Wei Huang, Tsung-Yi Ho, C.-L. Yang, and Y.-W. Chang, “A SAT-Based Routing Algorithm for Cross-Referencing Biochips,” *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, San Diego, CA, June 2011.
 48. Tsung-Wei Huang, H.-Y. Su, and Tsung-Yi Ho, “Progressive Network-Flow Based Broadcast Addressing for Pin-Constrained Digital Microfluidic Biochips,” *ACM/IEEE Design Automation Conference (DAC)*, pp. 741—746, San Diego, CA, June 2011.
 49. Tsung-Wei Huang, S.-Y. Yeh, and Tsung-Yi Ho, “A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast Electrode-Addressing EWO chips,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, pp. 425-431, San Jose, CA, 2010.
 50. Tsung-Wei Huang and Tsung-Yi Ho, “A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips,” *ACM International Symposium on Physical Design (ISPD)*, pp. 201—208, San Francisco, CA, 2010.
 51. Tsung-Wei Huang, C.-H. Lin, and Tsung-Yi Ho, “A Contamination-Aware Droplet Routing Algorithm for Digital Microfluidic Biochips,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, pp. 151—156, San Jose, CA, 2009.
 52. Tsung-Wei Huang and Tsung-Yi Ho, “A Fast Routability- and Performance-Driven Droplet Routing Algorithm for Digital Microfluidic Biochips,” *IEEE International Conference on Computer Design (ICCD)*, pp. 445—450, Lake Tahoe, CA, 2009

JOURNAL

1. Dian-Lun Lin and Tsung-Wei Huang, “Accelerating Large Sparse Neural Network Inference using GPU Task Graph Parallelism,” *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, accepted, 2022
2. Tsung-Wei Huang, Dian-Lun Lin, Chun-Xun Lin, and Yibo Lin, “Taskflow: A Lightweight Parallel and Heterogeneous Task Graph Computing System,” *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 33, no. 6, pp. 1303—1320, June 2022
3. Zizheng Guo, Mingwei Yang, Tsung-Wei Huang, and Yibo Lin, “A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, accepted, 2021

4. Jia-Ruei Yu, Chun-Hsien Chen, Tsung-Wei Huang, Jang-Jih Lu, Chia-Ru Chung, Ting-Wei Lin, Min-Hsien Wu, Yi-Ju Tseng, Hsin-Yao Wang, “Energy Efficiency of Inference Algorithms for Medical Datasets: A Green AI study,” *Journal of Medical Internet Research (JMIR)*, accepted, 2021
5. Tsung-Wei Huang, Dian-Lun Lin, Yibo Lin, and Chun-Xun Lin, “Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, accepted, 2021
6. Tsung-Wei Huang, Chun-Xun Lin, and Martin. D. F. Wong, “OpenTimer v2: A Parallel Incremental Timing Analysis Engine,” *IEEE Design and Test (DAT)*, vol. 38, no. 2, pp. 62—68, April 2021
7. Tsung-Wei Huang, Yibo Lin, Chun-Xun Lin, G. Guo, and Martin. D. F. Wong, “Cpp-Taskflow: A General-purpose Parallel Task Programming System at Scale,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 8, pp. 1687—1700, Aug. 2021
8. Tsung-Wei Huang, G. Guo, Chun-Xun Lin, and Martin. D. F. Wong, “OpenTimer v2: A New Parallel Incremental Timing Analysis Engine,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 4, pp. 776—789, April, 2021
9. Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, “DtCraft: A High-performance Distributed Execution Engine at Scale,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 6, pp. 1070—1083, June 2018
10. Tsung-Wei Huang and Martin D. F. Wong, “UI-Timer 1.0: An Ultra-Fast Path-Based Timing Analysis Algorithm for CPPR,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 11, pp. 1862—1875, Nov. 2016
11. S.-H. Yeh, J.-W. Chang, Tsung-Wei Huang, S.-T. Yu, and Tsung-Yi Ho, “Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWO Chip,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no.9, pp. 1302—1315, Sep. 2014.
12. J.-W. Chen, C.-L. Hsu, L.-C. Tsai, Tsung-Wei Huang, and Tsung-Yi Ho, “An ILP-Based Routing Algorithm for Pin-Constrained EWO Chip with Obstacle Avoidance,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no.11, pp. 1655—1667, Nov. 2013.
13. Y.-H. Chen, C.-L. Hus, Tsung-Wei Huang, and Tsung-Yi Ho, “A Reliability-Oriented Placement Algorithm for Reconfigurable Digital Microfluidic Biochips using 3D Deferred Decision-Making Technique,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 8, pp. 1151—1162, Aug. 2013.
14. J.-W. Chang, S.-H. Yeh, Tsung-Wei Huang, and Tsung-Yi Ho, “Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no 2, pp. 216—227, Feb. 2013.
15. Tsung-Wei Huang, S.-Y. Yeh, and Tsung-Yi Ho, “A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast-Addressing EWO Chip,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 12, pp. 1786—1799, Dec. 2011.
16. Tsung-Wei Huang and Tsung-Yi Ho, “A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 2, pp. 215—228, Feb. 2011.
17. Tsung-Wei Huang, C.-H. Lin, and Tsung-Yi Ho, “A Contamination-Aware Droplet Routing Algorithm for the Synthesis of Digital Microfluidic Biochips,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 29, no. 11, pp. 1682—1695, Nov. 2010.

PATENTS

1. T.-W. Huang, K. Kalafala, D. Sinha, and N. Venkateswaran, “Incremental Common Path Pessimism Analysis,” *USA Patent*, 14/946043, 2015 (assignee: IBM)
2. Tsung-Wei Huang, K. Kalafala, D. Sinha, and N. Venkateswaran, “Distributed Timing Analysis of a Partitioned Integrated Circuit Design”, *USA Patent*, 9916405B2, 03/13/2018 (assignee: IBM)

TALKS

1. “Intelligent Heterogeneous Computing,” ECE Distinguished Lecture, Stevens Institute of Technology, 2022
2. “Intelligent Heterogeneous Computing,” ECE Department, University of Minnesota, 2022
3. “Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System,” IXPUG, 2021
4. “cudaFlow: A Modern C++ Programming Model for GPU Task Graph Parallelism,” CppCon, 2021
5. “Taskflow: A General-purpose Parallel and Heterogeneous Task Computing System,” CUHK, Aug 2021
6. “HeteroTime: Accelerating Static Timing Analysis with GPUs,” Nvidia Research, June 2021

7. “Taskflow: A Lightweight Heterogeneous Task Programming System with Control Flow,” CPPNow, 2021
8. “GPU-Accelerated Static Timing Analysis and Beyond,” GTC, April 2021
9. “Machine Learning-enabled System for EDA,” VLSI-DAT, April 2021
10. “GPU-Accelerated Static Timing Analysis,” UCSC EDA Seminar, Feb 2021
11. “A General-purpose Parallel and Heterogeneous Task Programming System,” CIE/USA-GNYC, Oct 2020
12. “Taskflow: Parallel and Heterogeneous Task Programming in C++,” C++ Programmer Meetup, Oct 2020
13. “Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System,” CppIndia, Oct 2020
14. “Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System,” MUC++, Oct 2020
15. “Programming Systems for Parallelizing VLSI CAD and Beyond,” VLSI-DAT, April 2020
16. “A General-purpose Parallel and Heterogeneous Task Programming System at Scale,” ORNL, March 2020
17. “Growing Your Open-Source Projects,” WOSSET at IEEE/ACM ICCAD, November 2019
18. “Essential Building Blocks for Creating an Open-source EDA Project,” IEEE/ACM DAC, June 2019
19. “Task-based Parallel Programming using Modern C++,” CSL Social Hour, Sep 2018
20. “Distributed Timing Analysis in 100 Lines Code,” VSD webinar, May 2018
21. “DtCraft: A High-performance Distributed Execution Engine at Scale,” CSLSC, UIUC, IL, 2018
22. “OpenTimer: An open-source high-performance timing analysis tool,” ORCONF, Bologna, Italy, 2016
23. “Distributed Timing Analysis: Framework and Systems,” Cadence, Austin, June 2016
24. “OpenTimer: A High-performance Timing Analysis Tool,” Special Session, IEEE/ACM ICCAD, 2015
25. “Fast Path-based Timing Analysis,” Special Session, IEEE/ACM ICCAD, 2014

INDUSTRY EXPERIENCE

Software Engineer – High-performance Computing Group, Citadel, Chicago, IL	2017/06—2017/08
Software Engineer – Timing Group, IBM, Fishkill, NY	2015/05—2015/08
Software Engineer – Timing Group, Mentor Graphics, Fremont, CA	2014/05—2014/08

TEACHING EXPERIENCE

Instructor – Data Structure and Algorithms, CS 2420, Utah (UAC-FA21)
Instructor – Object-oriented Programming, CS 1410, Utah (FA20, UAC-FA21)
Instructor – Advanced Programming, ECE 5960, Utah (SP20)
Instructor – Logic Synthesis, ECE 462, UIUC (SP19)
Instructor – Competitive Programming, CSIE 3001, NCKU (FA10, SP11)
Teaching Assistant – Computer System and Programming, ECE 220, UIUC (FA15, FA16, SP17)
Teaching Assistant – VLSI CAD: Logic to Layout, Coursera (SP16)

EXTERNAL SERVICE

Organizer

- Chair/Co-chair, IEEE/ACM ICCAD CAD Contest, 2020, 2021, 2022
- Publicity Chair, International Workshop on Logic Synthesis (IWLS), 2020
- Chair/Co-chair, ACM SIGDA CADathlon International Programming Contest, 2018—2021
- Chair, VSD Open Online EDA Conference, 2018
- Co-chair, ACM TAU Timing Analysis Contest, 2018

Editorial Service

- Guest editor, Special Issue of VLSI Integration, 2022

Program Committee

- ACM/IEEE Design Automation Conference (DAC), 2022
- ACM TAU Workshop, 2020-2021
- IEEE/ACM International Conference on Computer-aided Design (ICCAD), 2019—2021
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2020—2021
- IEEE International Conference on Computer Design (ICCD), 2020—2021
- The C++ Conference (CppCon), 2019, 2021

Journal Reviewer

- IEEE Transactions on Parallel and Distributed Computing Systems (TPDS)
- IEEE Transactions on Computer-aided Design for Integrated Circuits and Systems (TCAD)

- IEEE Transactions on Very Large-scale Integration (TVLSI)
- IEEE Transactions on Circuits and Systems (TCAS)
- IEEE Transactions on Big Data (TBD)
- ACM Transaction son Design Automation of Electronic Systems (TODAES)
- VLSI Integration Journal

Conference Reviewer

- ACM International Symposium on Physical Design (ISPD)
- IEEE/ACM International Conference on Computer-aided Design (ICCAD)
- IEEE/ACM Design Automation Conference (DAC)
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)

INTERNAL SERVICE AT THE UNIVERSITY OF UTAH

Department of Electrical and Computer Engineering

- Graduate Student and Admission Committee, 2021—present
- University of Utah Asia Campus Committee, 2021—present
- University of Utah Asia Campus Students Summer Visit Program Chair, 2021—present
- University of Utah Asia Campus faculty recruiting committee, 2021—present
- Artificial Intelligence and Data-science Faculty recruiting committee, 2020