

Tsung-Wei Huang's CV

Website: <https://tsung-wei-huang.github.com>

GitHub: <https://github.com/tsung-wei-huang>

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POSITIONS

Assistant Professor – ECE Department, University of Utah

2019-present

Research Assistant Professor – ECE Department, University of Illinois at Urbana-Champaign

2018-2019

EDUCATION

PhD – ECE Department, University of Illinois at Urbana-Champaign, IL, USA

2013-2017

BS/MS – CS Department, National Cheng Kung University, Tainan, Taiwan




2006-2011

RESEARCH INTERESTS

Parallel and heterogeneous computing, computer-aided design, machine learning systems

SOFTWARE

My software releases have received >1M downloads and 5K stars in GitHub's records.

Software	GitHub
 Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System	https://github.com/taskflow/taskflow - Champion of 2020 IEEE HPEC Neural Network Challenge - 2 nd Place of Open Source Software Award in ACM MM19 - Best Poster Award in 2018 C++ Conference (CppCon)
 OpenTimer: A High-performance Timing Analysis Tool for VLSI Systems	https://github.com/OpenTimer/OpenTimer - Best EDA Software Tool in 2018 WOSET@ICCAD - ACM TAU Top-3 Winners in 2014-2016 - Golden Timers of ACM TAU Contests in 2014-2016
 DtCraft: A General-purpose Distributed Programming System using Data-parallel Streams	https://github.com/twhuang-uiuc/DtCraft - Best Open-source Software Award in ACM MM18

SELECTED AWARDS

- Champion of the IEEE/MIT/Amazon HPEC Large Sparse Neural Network Challenge, 2020
- 2nd Place (Taskflow), Open-source Software Competition, ACM Multimedia Conference, 2019
- ACM SIGDA Outstanding PhD Dissertation Award (thesis title: "Distributed Timing Analysis"), 2019
- Best Tool Award (OpenTimer), Workshop on Open-source EDA Technology, 2018
- Best Open-source Software Award (DtCraft), ACM Multimedia Conference, 2018
- Best Poster Award for Open-source Parallel Programming Library (Taskflow), CPP Conference, 2018
- 2nd and 1st Place, ACM/SIGDA CADathlon International Programming Contest, 2014 and 2017
- 1st, 2nd, and 1st Place, ACM TAU Timing Analysis Contest, 2014 through 2016
- Yi-Min Wang and Pi-Yu Chung Endowed Research Award, ECE Dept. UIUC, 2016
- Rambus Computer Engineering Fellowship, ECE Dept. UIUC, 2015-2016
- Study Abroad Scholarship for Outstanding EECS Students, Ministry of Education, Taiwan, 2013-2014
- 2nd Place, ACM Student Research Competition Grand Final, ACM Annual Award Banquet, 2011
- Best Master's Thesis Award, Taiwan Institute of Electrical and Electronic Engineering, 2011
- Best Master's Thesis Award, IEEE Taiwan Tainan Section, 2011

- Best Master's Thesis Award, Taiwan Institute of Information and Computing Machinery, 2011
- 1st Place, Master's Thesis Contest, Chinese Institute of Electrical Engineering, Taiwan, 2011
- Outstanding Graduate Recruiting Fellowship, National Cheng Kung University, 2010
- Outstanding Student Scholarship, Garmin Corporation, Taiwan, 2010
- 1st Place, ACM/SIGDA Student Research Competition, Design Automation Conference, 2010
- 3rd Place, National Collegiate Cell-Based IC Design Contest, Ministry of Education, Taiwan, 2010
- Distinguished Engineering Student Fellowship, Chinese Institute of Engineers, Taiwan, 2009
- 1st Place, National Collegiate Nano Device CAD Contest, Nano Device Laboratories, Taiwan, 2009
- 3rd Place, National Collegiate Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, National Collegiate IC/CAD Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, Presidential Award in CS Department, National Cheng Kung University, Taiwan, 2009

RESEARCH GRANT

1. PI, DARPA "OpenTimer and DtCraft," \$427K, 06/2018 – 07/2019 (with University of Illinois)

CONFERENCE

1. Chun-Xun Lin, Tsung-Wei Huang, and Martin D. F. Wong, "An Efficient Work-Stealing Scheduler for Task Dependency Graph," *IEEE International Conference on Parallel and Distributed Systems (ICPADS)*, Hong Kong, 2020
2. Kuan-Ming Lai, Tsung-Wei Huang, Pei-Yu Lee, and Tsung-Yi Ho, "ATM: A High Accuracy Extracted Timing Model for Hierarchical Timing Analysis," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Tokyo, Japan, 2021
3. D.-L. Lin and Tsung-Wei Huang, "A Novel Inference Algorithm for Large Sparse Neural Network using Task Graph Parallelism," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2020
4. Z. Guo, Tsung-Wei Huang, and Yibo Lin, "GPU-Accelerated Static Timing Analysis," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020
5. G. Guo, Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "An Efficient Critical Path Generation Algorithm Considering Extensive Path Constraints," *IEEE/ACM Design Automation Conference (DAC)*, San Francisco, CA, 2020
6. Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo, and Martin D. F. Wong, "A Modern C++ Parallel Task Programming Library," *ACM Multimedia Conference (MM)*, Nice, France, 2019
7. Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo, and Martin D. F. Wong, "An Efficient and Composable Parallel Programming Library," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2019
8. Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, "Cpp-Taskflow: Fast Task-based Parallel Programming using Modern C++," *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, Rio De Janeiro, Brazil, 2019
9. Kuan-Ming Lai, Tsung-Wei Huang, and Tsung-Yi Ho, "A General Cache Framework for Efficient Generation of Timing Critical Paths," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019
10. Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, "Essential Building Blocks for Creating an Open-source EDA Project," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019
11. Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "Distributed Timing Analysis at Scale," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019
12. Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, "A General-purpose Distributed Programming Systems using Data-parallel Streams," *ACM Multimedia Conference (MM)*, Seoul, Korea, 2018
13. Chun-Xun Lin, Tsung-Wei Huang, G. Guo, and Martin D. F. Wong, "MtDetector: A High-performance Marine Traffic Detector at Stream Scale," *ACM Distributed Event-based System Conference (DEBS)*, Hamilton, New Zealand, 2018
14. Chun-Xun Lin, Tsung-Wei Huang, T. Yu, and Martin D. F. Wong, "A Distributed Power Grid Analysis Framework

- from Sequential Stream Graph,” *ACM Great Lakes Symposium (GLSVLSI)*, Chicago, IL, 2018
15. Chun-Xun Lin, Tsung-Wei Huang, and Martin D. F. Wong, “Routing at Compile Time,” *IEEE International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, 2018
 16. Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, “DtCraft: A Distributed Execution Engine for Compute-intensive Applications,” *ACM/IEEE International Conference on Computer-aided Design (ICCAD)*, Irvine, CA, 2017
 17. Tin-Yin Lai, Tsung-Wei Huang, and Martin D. F. Wong, “An Effective and Accurate Macro-modeling Algorithm for Large Hierarchical Designs,” *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, 2017
 18. Tsung-Wei Huang, Martin D. F. Wong, D. Sinha, K. Kalafala, and N. Venkateswaran, “A Distributed Timing Analysis Framework for Large Designs,” *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, 2016
 19. Tsung-Wei Huang and Martin D. F. Wong, “OpenTimer: A High-performance Timing Analysis Tool,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, TX, 2015
 20. Tsung-Wei Huang and Martin D. F. Wong, “On Fast Timing Closure: Speeding Up Incremental Path-Based Timing Analysis with MapReduce,” *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, CA, 2015
 21. Tsung-Wei Huang and Martin D. F. Wong, “Accelerated Path-Based Timing Analysis with MapReduce,” *ACM International Symposium on Physical Design (ISPD)*, Monterey, CA, 2015
 22. Tsung-Wei Huang, P-C. Wu, and Martin D. F. Wong, “Fast Path-Based Timing Analysis for CPPR,” *IEEE/ACM ACM/IEEE International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2014
 23. Tsung-Wei Huang, P-C. Wu, and Martin D. F. Wong, “UI-Timer: An Ultra-Fast Clock Network Pessimism Removal Algorithm,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2014
 24. Tsung-Wei Huang, P-C. Wu, and Martin D. F. Wong, “UI-Route: An Ultra-Fast Incremental Maze Routing Algorithm,” *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, San Francisco, CA, 2014
 25. S.-H. Yeh, J.-W. Chang, Tsung-Wei Huang, and Tsung-Yi Ho, “Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2012
 26. Tsung-Wei Huang, J.-W. Chang, and Tsung-Yi Ho, “Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips,” *ACM International Symposium on Physical Design (ISPD)*, Napa, CA, 2012
 27. J.-W. Chang, Tsung-Wei Huang, and Tsung-Yi Ho, “An ILP-based Obstacle-Avoiding Routing Algorithm for Pin-Constrained EWOD Chips,” *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Sydney, Australia, 2012
 28. Tsung-Wei Huang, Tsung-Yi Ho, and K. Chakrabarty, “Reliability-Oriented Broadcast Electrode-Addressing for Pin-Constrained Digital Microfluidic Biochips,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2011
 29. Tsung-Wei Huang, Yan-You Lin, J.-W. Chang, and Tsung-Yi Ho, “Recent Research and Emerging Challenges in the Designs and Optimizations for Digital Microfluidic Biochips,” invited paper, *IEEE System on Chip Conference (SOCC)*, 2011.
 30. Tsung-Wei Huang, Yan-You Lin, J.-W. Chang, and Tsung-Yi Ho, “Chip-Level Design and Optimization for Digital Microfluidic Biochips,” invited paper, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011.
 31. P.-H. Yuh, C. C.-Y. Lin, Tsung-Wei Huang, Tsung-Yi Ho, C.-L. Yang, and Y.-W. Chang, “A SAT-Based Routing Algorithm for Cross-Referencing Biochips,” *EEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, San Diego, CA, June 2011.
 32. Tsung-Wei Huang, H.-Y. Su, and Tsung-Yi Ho, “Progressive Network-Flow Based Broadcast Addressing for Pin-Constrained Digital Microfluidic Biochips,” *ACM/IEEE Design Automation Conference (DAC)*, pp. 741-746, San Diego, CA, June 2011.
 33. Tsung-Wei Huang, S.-Y. Yeh, and Tsung-Yi Ho, “A Network-Flow Based Pin-Count Aware Routing Algorithm for

Broadcast Electrode-Addressing EWOD Chips,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, pp. 425-431, San Jose, CA, 2010.

34. Tsung-Wei Huang and Tsung-Yi Ho, “A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips,” *ACM International Symposium on Physical Design (ISPD)*, pp. 201-208, San Francisco, CA, 2010.
35. Tsung-Wei Huang, C.-H. Lin, and Tsung-Yi Ho, “A Contamination-Aware Droplet Routing Algorithm for Digital Microfluidic Biochips,” *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, pp. 151-156, San Jose, CA, 2009.
36. Tsung-Wei Huang and Tsung-Yi Ho, “A Fast Routability- and Performance-Driven Droplet Routing Algorithm for Digital Microfluidic Biochips,” *IEEE International Conference on Computer Design (ICCD)*, pp. 445-450, Lake Tahoe, CA, 2009

JOURNAL

1. Tsung-Wei Huang, Yibo Lin, Chun-Xun Lin, G. Guo, and Martin. D. F. Wong, “Cpp-Taskflow: A General-purpose Parallel Task Programming System at Scale,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, to appear, 2020
2. Tsung-Wei Huang, G. Guo, Chun-Xun Lin, and Martin. D. F. Wong, “OpenTimer v2: A New Parallel Incremental Timing Analysis Engine,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, to appear, 2020
3. Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, “DtCraft: A High-performance Distributed Execution Engine at Scale,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 6, pp. 1070-1083, June 2018
4. Tsung-Wei Huang and Martin D. F. Wong, “UI-Timer 1.0: An Ultra-Fast Path-Based Timing Analysis Algorithm for CPPR,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 11, pp. 1862-1875, Nov. 2016
5. S.-H. Yeh, J.-W. Chang, Tsung-Wei Huang, S.-T. Yu, and Tsung-Yi Ho, “Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no.9, pp. 1302-1315, Sep. 2014.
6. J.-W. Chen, C.-L. Hsu, L.-C. Tsai, Tsung-Wei Huang, and Tsung-Yi Ho, “An ILP-Based Routing Algorithm for Pin-Constrained EWOD Chips with Obstacle Avoidance,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no.11, pp. 1655-1667, Nov. 2013.
7. Y.-H. Chen, C.-L. Hus, Tsung-Wei Huang, and Tsung-Yi Ho, “A Reliability-Oriented Placement Algorithm for Reconfigurable Digital Microfluidic Biochips using 3D Deferred Decision-Making Technique,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 8, pp. 1151-1162, Aug. 2013.
8. J.-W. Chang, S.-H. Yeh, Tsung-Wei Huang, and Tsung-Yi Ho, “Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no 2, pp. 216-227, Feb. 2013.
9. Tsung-Wei Huang, S.-Y. Yeh, and Tsung-Yi Ho, “A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast-Addressing EWOD Chips,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 12, pp. 1786-1799, Dec. 2011.
10. Tsung-Wei Huang and Tsung-Yi Ho, “A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 2, pp. 215-228, Feb. 2011.
11. Tsung-Wei Huang, C.-H. Lin, and Tsung-Yi Ho, “A Contamination-Aware Droplet Routing Algorithm for the Synthesis of Digital Microfluidic Biochips,” *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 29, no. 11, pp. 1682-1695, Nov. 2010.

PATENT

1. T.-W. Huang, K. Kalafala, D. Sinha, and N. Venkateswaran, "Incremental Common Path Pessimism Analysis," *USA Patent*, 14/946043, 2015 (assignee: IBM)
2. Tsung-Wei Huang, K. Kalafala, D. Sinha, and N. Venkateswaran, "Distributed Timing Analysis of a Partitioned Integrated Circuit Design", *USA Patent*, 9916405B2, 03/13/2018 (assignee: IBM)

INVITED TALK

1. "A General-purpose Parallel and Heterogeneous Task Programming System," CIE/USA-GNYC, Oct 2020
2. "Taskflow: Parallel and Heterogeneous Task Programming in C++," C++ Programmer Meetup, Oct 2020
3. "Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System," CppIndia, Oct 2020
4. "Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System," MUC++, Oct 2020
5. "Programming Systems for Parallelizing VLSI CAD and Beyond," VLSI-DAT, April 2020
6. "A General-purpose Parallel and Heterogeneous Task Programming System at Scale," ORNL, March 2020
7. "Growing Your Open-Source Projects," WOSET at IEEE/ACM ICCAD, November 2019
8. "Essential Building Blocks for Creating an Open-source EDA Project," IEEE/ACM DAC, June 2019
9. "Task-based Parallel Programming using Modern C++", CSL Social Hour, Sep 2018
10. "Distributed Timing Analysis in 100 Lines Code," VSD webinar, May 2018
11. "DtCraft: A High-performance Distributed Execution Engine at Scale," CSLSC, UIUC, IL, 2018
12. "OpenTimer: An open-source high-performance timing analysis tool," ORCONF, Bologna, Italy, 2016
13. "Distributed Timing Analysis: Framework and Systems," Cadence, Austin, June 2016
14. "OpenTimer: A High-performance Timing Analysis Tool," Special Session, IEEE/ACM ICCAD, 2015
15. "Fast Path-based Timing Analysis," Special Session, IEEE/ACM ICCAD, 2014

INDUSTRY EXPERIENCE

Software Engineer – High-performance computing Group, Citadel, Chicago, IL	2017/06–2017/08
Software Engineer – Timing Group, IBM, Fishkill, NY	2015/05–2015/08
Software Engineer – Timing Group, Mentor Graphics, Fremont, CA	2014/05–2014/08

TEACHING EXPERIENCE

Instructor – Object-oriented Programming, CS 1410, Utah (FA20)
Instructor – Advanced Programming, ECE 5960, Utah (SP20)
Instructor – Logic Synthesis, ECE 462, UIUC (SP19)
Instructor – Competitive Programming, CSIE 3001, NCKU (FA10, SP11)
Teaching Assistant – Computer System and Programming, ECE 220, UIUC (FA15, FA16, SP17)
Teaching Assistant – VLSI CAD: Logic to Layout, Coursera (SP16)

SERVICE

Journal Reviewer

- IEEE Transaction on Computer-aided Design for Integrated Circuits and Systems (TCAD)
- IEEE Transaction on Very Large Scale Integration (TVLSI)
- IEEE Transaction on Big Data (TBD)
- ACM Transaction on Design Automation of Electronic Systems (TODAES)
- VLSI Integration Journal

Conference Reviewer

- ACM International Symposium on Physical Design (ISPD)
- IEEE/ACM International Conference on Computer-aided Design (ICCAD)

- IEEE/ACM Design Automation Conference (DAC)
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)

Organizer

- Co-chair, CAD Contest in IEEE/ACM ICCAD, 2020
- Publicity Chair, International Workshop on Logic Synthesis (IWLS), 2020
- Chair/Co-chair, ACM SIGDA CADathlon International Programming Contest, 2018-2020
- Chair, VSDOpen Online EDA Conference, 2018
- Co-chair, ACM TAU Timing Analysis Contest, 2018

Program Committee

- ACM TAU Workshop, 2020
- IEEE/ACM International Conference on Computer-aided Design (ICCAD), 2019-2020
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2020-2021
- IEEE International Conference on Computer Design (ICCD), 2020
- The C++ Conference (CppCon), 2019