# Tsung-Wei Huang's CV

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## POSITIONS

**Research Assistant Professor** – ECE Dept., University of Illinois at Urbana-Champaign          2018-present

## EDUCATION

**PhD** – ECE Dept., University of Illinois at Urbana-Champaign, IL, USA          2013-2017
**BS/MS** – CS Dept., Taiwan's National Cheng Kung University, Tainan, Taiwan          2006-2011

## RESEARCH INTERESTS

- Computer Systems, Artificial Intelligence Systems, Big-data Computing
- Distributed Systems, Parallel Programming Models
- VLSI Design Automation, Circuit Simulation and Timing Analysis

## SOFTWARE

- OpenTimer: A High-performance Timing Analysis Tool for VLSI Systems
  - https://github.com/OpenTimer/OpenTimer, MIT License
  - Top-3 winners in ACM TAU Timing Analysis Contests (2014-2016), Best Tool Award in WOSET 2018
- DtCraft: A General-purpose Distributed Programming System using Data-parallel Streams
  - https://github.com/twhuang-uiuc/DtCraft, MIT License
  - Best Tool Award in ACM Multimedia 2018
- Cpp-Taskflow: Fast Parallel Programming with Task Dependencies using Modern C++
  - https://github.com/cpp-taskflow/cpp-taskflow, MIT License
  - Best Poster Award in CPP Conference 2018 (voted by +1000 developers)
  - Received +100,000 downloads

## SELECTED AWARDS

- Best Tool Award (OpenTimer), Workshop on Open-source EDA Technology, 2018
- Best Open-source Software Award (DtCraft), ACM Multimedia Conference, 2018
- Best Poster Award for Open-source Parallel Programming Library (Cpp-Taskflow), CPP Conference, 2018
- 2nd and 1st Place, ACM/SIGDA CADathlon International Programming Contest, 2014 and 2017
- 1st, 2nd, and 1st Place, ACM TAU Timing Analysis Contest, 2014 through 2016
- Yi-Min Wang and Pi-Yu Chung Endowed Research Award, ECE Dept. UIUC, 2016
- Rambus Computer Engineering Fellowship, ECE Dept. UIUC, 2015-2016
- Study Abroad Scholarship for Outstanding EECS Students, Ministry of Education, Taiwan, 2013-2014
- 2nd Place, ACM Student Research Competition Grand Final, ACM Annual Award Banquet, 2011
- Best Master's Thesis Award, Taiwan Institute of Electrical and Electronic Engineering, 2011
- Best Master's Thesis Award, IEEE Taiwan Tainan Section, 2011

- Best Master's Thesis Award, Taiwan Institute of Information and Computing Machinery, 2011
- 1st Place, Master's Thesis Contest, Chinese Institute of Electrical Engineering, Taiwan, 2011
- Outstanding Graduate Recruiting Fellowship, National Cheng Kung University, 2010
- Outstanding Student Scholarship, Garmin Corporation, Taiwan, 2010
- 1st Place, ACM/SIGDA Student Research Competition, Design Automation Conference, 2010
- 3rd Place, National Collegiate Cell-Based IC Design Contest, Ministry of Education, Taiwan, 2010
- Distinguished Engineering Student Fellowship, Chinese Institute of Engineers, Taiwan, 2009
- 1st Place, National Collegiate Nano Device CAD Contest, Nano Device Laboratories, Taiwan, 2009
- 3rd Place, National Collegiate Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, National Collegiate IC/CAD Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, Presidential Award in CS Department, National Cheng Kung University, Taiwan, 2009

**RESEARCH GRANT EXPERIENCE**

1. PI, DARPA "OpenTimer and DtCraft," $1.7M, 06/2018-06/2022
2. Submitted a Proposal to SRC as a Lead PI on "Machine Learning in Timing Analysis," $360K, 2018
3. Helped Prof. Martin Wong acquire an NSF grant on "Distributed Timing Analysis and Beyond," $400K, 2017

**CONFERENCE**

1. T.-W. Huang, C.-X. Lin, G. Guo, and Martin D. F. Wong, "Cpp-Taskflow: Fast Task-based Parallel Programming using Modern C++," *IEEE IPDPS*, Rio De Janeiro, Brazil, 2019
2. K.-M Lai, T.-W. Huang, and T.-Y. Ho, "A General Cache Framework for Efficient Generation of Timing Critical Paths," *ACM/IEEE DAC*, Las Vegas, NV, 2019
3. T.-W. Huang and C.-X. Lin, "Essential Building Blocks for Creating an Open-source EDA Project," *ACM/IEEE DAC*, Las Vegas, NV, 2019
4. T.-W. Huang, C.-X. Lin, G. Guo, and Martin D. F. Wong, "A General-purpose Distributed Programming Systems using Data-parallel Streams," *ACM MM*, Seoul, Korea, 2018
5. C.-X. Lin, T.-W. Huang, G. Guo, and Martin D. F. Wong, "MtDetector: A High-performance Marine Traffic Detector at Stream Scale," *ACM DEBS*, Hamilton, New Zealand, 2018
6. C.-X. Lin, T.-W. Huang, T. Yu, and Martin D. F. Wong, "A Distributed Power Grid Analysis Framework from Sequential Stream Graph," *ACM GLSVLSI*, Chicago, IL, 2018
7. C.-X. Lin, T.-W. Huang, and Martin D. F. Wong, "Routing at Compile Time," *IEEE ISQED*, Santa Clara, CA, 2018
8. T.-W. Huang, C.-X. Lin, and Martin D. F. Wong, "DtCraft: A Distributed Execution Engine for Compute-intensive Applications," *ACM/IEEE ICCAD*, Irvine, CA, 2017
9. T.-Y. Lai, T.-W. Huang, and Martin D. F. Wong, "An Effective and Accurate Macro-modeling Algorithm for Large Hierarchical Designs," *ACM/IEEE DAC*, Austin, TX, 2017
10. T.-W. Huang, Martin D. F. Wong, D. Sinha, K. Kalafala, and N. Venkateswaran, "A Distributed Timing Analysis Framework for Large Designs," *ACM/IEEE DAC*, Austin, TX, 2016
11. T.-W. Huang and Martin D. F. Wong, "OpenTimer: A High-performance Timing Analysis Tool," *IEEE/ACM ICCAD*, TX, 2015
12. T.-W. Huang and Martin D. F. Wong, "On Fast Timing Closure: Speeding Up Incremental Path-Based Timing Analysis with MapReduce," *IEEE/ACM SLIP*, CA, 2015
13. T.-W. Huang and Martin D. F. Wong, "Accelerated Path-Based Timing Analysis with MapReduce," *ACM ISPD*,

Monterey, CA, 2015

14. T.-W. Huang, P.-C. Wu, and Martin D. F. Wong, "Fast Path-Based Timing Analysis for CPPR," *IEEE/ACM ICCAD*, San Jose, CA, 2014

15. T.-W. Huang, P.-C. Wu, and Martin D. F. Wong, "UI-Timer: An Ultra-Fast Clock Network Pessimism Removal Algorithm," *IEEE/ACM ICCAD*, San Jose, CA, 2014

16. T.-W. Huang, P.-C. Wu, and Martin D. F. Wong, "UI-Route: An Ultra-Fast Incremental Maze Routing Algorithm," *ACM SLIP*, San Francisco, CA, 2014

17. S.-H. Yeh, J.-W. Chang, T.-W. Huang, and T.-Y. Ho, "Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips," *IEEE/ACM ICCAD*, San Jose, CA, 2012

18. T.-W. Huang, J.-W. Chang, and T.-Y. Ho, "Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips," *ACM ISPD*, Napa, CA, 2012

19. J.-W. Chang, T.-W. Huang, and T.-Y. Ho, "An ILP-based Obstacle-Avoiding Routing Algorithm for Pin-Constrained EWOD Chips," *IEEE/ACM ASPDAC*, Sydney, Australia, 2012

20. T.-W. Huang, T.-Y. Ho, and K. Chakrabarty, "Reliability-Oriented Broadcast Electrode-Addressing for Pin-Constrained Digital Microfluidic Biochips," *IEEE/ACM ICCAD*, San Jose, CA, 2011

21. T.-W. Huang, Y.-Y. Lin, J.-W. Chang, and T.-Y. Ho, "Recent Research and Emerging Challenges in the Designs and Optimizations for Digital Microfluidic Biochips," invited paper, *IEEE SOCC*, 2011.

22. T.-W. Huang, Y.-Y. Lin, J.-W. Chang, and T.-Y. Ho, "Chip-Level Design and Optimization for Digital Microfluidic Biochips," invited paper, *IEEE MWSCAS*, 2011.

23. P.-H. Yuh, C. C.-Y. Lin, T.-W. Huang, T.-Y. Ho, C.-L. Yang, and Y.-W. Chang, "A SAT-Based Routing Algorithm for Cross-Referencing Biochips," *EEE/ACM SLIP,* San Diego, CA, June 2011.

24. T.-W. Huang, H.-Y. Su, and T.-Y. Ho, "Progressive Network-Flow Based Broadcast Addressing for Pin-Constrained Digital Microfluidic Biochips," *ACM IEEE DAC*, pp. 741-746, San Diego, CA, June 2011.

25. T.-W. Huang, S.-Y. Yeh, and T.-Y. Ho, "A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast Electrode-Addressing EWOD Chips," *IEEE/ACM ICCAD*, pp. 425-431, San Jose, CA, 2010.

26. T.-W. Huang and T.-Y. Ho, "A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips," *ACM ISPD*, pp. 201-208, San Francisco, CA, 2010.

27. T.-W. Huang, C.-H. Lin, and T.-Y. Ho, "A Contamination-Aware Droplet Routing Algorithm for Digital Microfluidic Biochips," *IEEE/ACM ICCAD*, pp. 151-156, San Jose, CA, 2009.

28. T.-W. Huang and T.-Y. Ho, "A Fast Routability- and Performance-Driven Droplet Routing Algorithm for Digital Microfluidic Biochips," *IEEE ICCD*, pp. 445-450, Lake Tahoe, CA, 2009

**JOURNAL**

1. T.-W. Huang, C.-X. Lin, and Martin D. F. Wong, "DtCraft: A High-performance Distributed Execution Engine at Scale," *IEEE TCAD*, 2018

2. T.-W. Huang and Martin D. F. Wong, "UI-Timer 1.0: An Ultra-Fast Path-Based Timing Analysis Algorithm for CPPR," *IEEE TCAD*, vol. 35, no. 11, pp. 1862-1875, Nov. 2016

3. S.-H. Yeh, J.-W. Chang, T.-W. Huang, S.-T. Yu, and T.-Y. Ho, "Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips," *IEEE TCAD*, vol. 33, no.9, pp. 1302-1315, Sep. 2014.

4. J.-W. Chen, C.-L. Hsu, L.-C. Tsai, T.-W. Huang, and T.-Y. Ho, "An ILP-Based Routing Algorithm for Pin-Constrained EWOD Chips with Obstacle Avoidance," *IEEE TCAD*, vol. 32, no.11, pp. 1655-1667, Nov. 2013.

5. Y.-H. Chen, C.-L. Hus, T.-W. Huang, and T.-Y. Ho, "A Reliability-Oriented Placement Algorithm for Reconfigurable

Digital Microfluidic Biochips using 3D Deferred Decision-Making Technique," *IEEE TCAD*, vol. 32, no. 8, pp. 1151-1162, Aug. 2013.

6. J.-W. Chang, S.-H. Yeh, <u>T.-W. Huang</u>, and T.-Y. Ho, "Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips," *IEEE TCAD*, vol. 32, no 2, pp. 216-227, Feb. 2013.

7. <u>T.-W. Huang</u>, S.-Y. Yeh, and T.-Y. Ho, "A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast-Addressing EWOD Chips," *IEEE TCAD*, vol. 30, no. 12, pp. 1786-1799, Dec. 2011.

8. <u>T.-W. Huang</u> and T.-Y. Ho, "A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips," *IEEE TCAD*, vol. 30, no. 2, pp. 215-228, Feb. 2011.

9. <u>T.-W. Huang</u>, C.-H. Lin, and T.-Y. Ho, "A Contamination-Aware Droplet Routing Algorithm for the Synthesis of Digital Microfluidic Biochips," *IEEE TCAD*, vol. 29, no. 11, pp. 1682-1695, Nov. 2010.

## PATENT

1. <u>T.-W Huang</u>, K. Kalafala, D. Sinha, and N. Venkateswaran, "Incremental Common Path Pessimism Analysis," *USA Patent*, 14/946043, 2015

2. <u>T.-W. Huang</u>, K. Kalafala, D. Sinha, and N. Venkateswaran, "Distributed Timing Analysis of a Partitioned Integrated Circuit Design", US9916405B2, 03/13/2018

## PRESENTATION

1. "Fast Parallel Programming using Modern C++," CPP Conference, Sep 2018
2. "Task-based Parallel Programming using Modern C++", CSL Social Hour, Sep 2018
3. "Distributed Timing Analysis in 100 Lines Code," VSD webinar, May 2018
4. "DtCraft: A High-performance Distributed Execution Engine at Scale," CSLSC, UIUC, IL, 2018
5. "OpenTimer: An open-source high-performance timing analysis tool," ORCONF, Bologna, Italy, 2016
6. "Distributed Timing Analysis: Framework and Systems," Cadence, Austin, June 2016
7. "OpenTimer: A High-performance Timing Analysis Tool," Special Session, IEEE/ACM ICCAD, 2015
8. "Fast Path-based Timing Analysis," Special Session, IEEE/ACM ICCAD, 2014

## INDUSTRY EXPERIENCE

**Software Engineer** – High-performance computing Group, Citadel, Chicago, IL        2017/06–2017/08
**Software Engineer** – Timing Group, IBM, Fishkill, NY        2015/05–2015/08
**Software Engineer** – Timing Group, Mentor Graphics, Fremont, CA        2014/05–2014/08

## TEACHING EXPERIENCE

**Teaching Assistant** – Competitive Programming, CSIE 3001, NCKU (FA10, SP11)
**Teaching Assistant** – Computer System and Programming, ECE 220, UIUC (FA15, FA16, SP17)
**Teaching Assistant** – VLSI CAD: Logic to Layout, Coursera (SP16)
**Instructor** – Logic Synthesis, ECE 462, UIUC (SP19)

## PROFESSIONALISM

**Journal Reviewer**
- IEEE Transaction on Computer-aided Design for Integrated Circuits and Systems (TCAD)
- IEEE Transaction on Very Large Scale Integration (TVLSI)

- IEEE Transaction on Big Data (TBD)
- ACM Transaction on Design Automation of Electronic Systems (TODAES)

**Conference Reviewer**

- ACM International Symposium on Physical Design (ISPD)
- IEEE/ACM International Conference on Computer-aided Design (ICCAD)
- IEEE/ACM Design Automation Conference (DAC)
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)

**Organizer**

- Chair, VSDOpen Online EDA Conference, 2018
- Co-chair, ACM SIGDA CADathlon International Programming Contest, 2018
- Committee, ACM TAU Timing Analysis Contest, 2018