TSUNG-WEI (TW) HUANG

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APPOINTMENT

Associate Professor, Department of Electrical and Computer Engineering University of Wisconsin at Madison, Madison, Wisconsin, USA	2025 – present
Assistant Professor, Department of Electrical and Computer Engineering University of Wisconsin at Madison, Madison, Wisconsin, USA	2023 – 2025
Assistant Professor, Department of Electrical and Computer Engineering University of Utah, Salt Lake City, Utah, USA	2019 – 2023
Research Assistant Professor, Department of Electrical and Computer Engineering University of Illinois at Urbana-Champaign, IL, USA	2018 – 2019

EDUCATION

PhD, Department of Electrical and Computer Engineering University of Illinois at Urbana-Champaign, IL, USA	2013 – 2017
MS, Department of Computer Science and Information Engineering National Cheng Kung University, Tainan, Taiwan	2010 – 2011
BS, Department of Computer Science and Information Engineering National Cheng Kung University, Tainan, Taiwan	2006 – 2010

RESEARCH INTEREST

Electronic Design Automation, High-performance Computing, Quantum Computing

SOFTWARE PROJECT

Our software projects have been used by thousands of people from both industry and academia:

1. Taskflow: A General-purpose Parallel and Heterogeneous Programming System
https://taskflow.github.io/ (8–11K weekly downloads)
- C++ Conference Best Poster Award, 2025
- PPoPP FastCode Programming Challenge Winner (2nd Place), 2025
- MIT/Amazon/HPEC Graph Challenge Innovation Award (2nd Place), 2023
- MIT/Amazon/HPEC Graph Challenge Champion Award (1st Place), 2020
- ACM Multimedia Best Open-source Software Award, 2019
- C++ Conference Best Poster Award, 2018

2. OpenTimer: A High-performance Timing Analysis Tool for VLSI Systems
https://github.com/OpenTimer/OpenTimer
- IEEE/ACM ICCAD 10-year Retrospective Most Influential Paper Award, 2024
- ACM SIGDA Outstanding PhD Dissertation Award, 2019
- Best EDA Software Tool, WOSET@ICCAD, 2018
- Top-3 Winners of ACM TAU Contests, 2014–2016
- Golden Timers of ACM TAU Contests, 2017–2021
- Golden Timer of IEEE/ACM ICCAD CAD Contest, 2015

3. RTLflow: A GPU Acceleration Flow for RTL Simulation with Batch Stimulus
https://github.com/dian-lun-lin/rtlflow

4. SNIG: A Task-parallel Inference Engine for Large Sparse Neural Network
https://github.com/dian-lun-lin/SNIG
- MIT/Amazon/HPEC Graph Challenge Champion Award, 2020

5. DtCraft: A Data-parallel Distributed Streaming System
https://github.com/twhuang-uiuc/DtCraft
- ACM Multimedia Best Open-source Software Award, 2018

AWARDS

- Vilas Early-career Investigator Award, Trustees of the William F. Vilas Estate. Funding, 2025
- DAC Under-40 Innovator Award, 2025
- CoE Award for Excellence in Graduate Student Mentoring, UW-Madison, 2025
- Second Place, ACM SIGPLAN PPoPP Fast Code Programming Challenge (FCPC), 2025
- Honorable Mention (6th Place out of 90 teams), IEEE/ACM ICCAD CAD Contest, 2024
- ICCAD 10-year Retrospective Most Influential Paper Award, 2024
- 2nd Place, MIT/Amazon/HPEC Large Sparse Neural Network Challenge, 2023
- 2nd Place, MIT/Amazon/HPEC Streaming Graph Challenge, 2023
- ACM SIGDA Outstanding New Faculty Award, 2023
- ACM SIGDA Meritorious Service Award, 2022
- Humboldt Research Fellowship Award, Alexander von Humboldt Foundation, 2022
- Faculty Early Career Development Program (CAREER) Award, NSF, 2022
- Best Paper Award for "GPU-Accelerated Path-based Timing Analysis," ACM TAU Workshop, 2021
- 1st Place, MIT/Amazon/HPEC Large Sparse Neural Network Challenge, 2020
- 2nd Place (Taskflow), Open-source Software Competition, ACM Multimedia Conference, 2019
- ACM SIGDA Outstanding PhD Dissertation Award (thesis title: "Distributed Timing Analysis"), 2019
- Best Tool Award (OpenTimer), Workshop on Open-source EDA Technology, 2018
- Best Open-source Software Award (DtCraft), ACM Multimedia Conference, 2018
- Best Poster Award (Taskflow), CPP Conference, 2018
- 2nd and 1st Place, ACM/SIGDA CADathlon International Programming Contest, 2014 and 2017
- 1st, 2nd, and 1st Place, ACM TAU Timing Analysis Contest, 2014–2016
- Yi-Min Wang and Pi-Yu Chung Endowed Research Award, ECE Dept. UIUC, 2016
- Rambus Computer Engineering Fellowship, ECE Dept. UIUC, 2015—2016
- Study Abroad Scholarship, Ministry of Education, Taiwan, 2013—2014
- 2nd Place, ACM Student Research Competition Grand Final, ACM Annual Award Banquet, 2011
- Best Master's Thesis Award, Taiwan Institute of Electrical and Electronic Engineering, 2011
- Best Master's Thesis Award, IEEE Taiwan Tainan Section, 2011
- Best Master's Thesis Award, Taiwan Institute of Information and Computing Machinery, 2011
- 1st Place, Master's Thesis Contest, Chinese Institute of Electrical Engineering, Taiwan, 2011
- Outstanding Graduate Recruiting Fellowship, National Cheng Kung University, 2010
- Outstanding Student Scholarship, Garmin Corporation, Taiwan, 2010
- 1st Place, ACM/SIGDA Student Research Competition, Design Automation Conference, 2010
- 3rd Place, National Collegiate Cell-Based IC Design Contest, Ministry of Education, Taiwan, 2010
- Distinguished Engineering Student Fellowship, Chinese Institute of Engineers, Taiwan, 2009
- 1st Place, National Collegiate Nano Device CAD Contest, Nano Device Laboratories, Taiwan, 2009
- 3rd Place, National Collegiate Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, National Collegiate IC/CAD Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, Presidential Award in CS Department, National Cheng Kung University, Taiwan, 2009

Research Grants

Fall Research Competition Award
PI, $56K, Office of the Vice Chancellor for Research, UW-Madison   July 2026 – June 2027

Vilas Early-career Investigator Award
PI, $60K, Trustees of the William F. Vilas Estate. Funding   July 2025 – July 2028

Co-Design of Chiral Quantum Photonic Devices and Circuits
Co-PI, $400K, NSF, DMR-2235276   Aug 2023 – July 2025

Toward a Task-parallel Programming Ecosystem for Modern Scientific Computing
PI, $298K, NSF, TI-2229304/-2349144   Sep 2022 – Aug 2024

GPU Acceleration for Satisfiability Solver
PI, $5K (hardware donation), Intel   Oct 2022

Developer Training Programs for Taskflow
PI, $5K, NumFOCUS Small Development Grant   Sep 2022 – May 2023

Transpiling Parallel Task Graph Programming Models for Scientific Software
PI, $488K, NSF, OAC-2209957/-2349143   July 2022 – July 2025

Taskflow with Constrained Parallelism
PI, $16K, NSF, CCF-2126672 (REU supplement)   Aug 2022 – Aug 2023

Accelerating Static Timing Analysis with Intelligent Heterogeneous Parallelism
PI, $500K, NSF, CCF-2144523/-2349582 (CAREER)   Jan 2022 – Jan 2027

GPU Acceleration for Static Timing Analysis
PI, $10K (hardware donation), Nvidia Applied Research Acceleration Program   Nov 2021

A General-purpose Heterogeneous Task Graph Computing System for VLSI CAD
PI, $403K, NSF, CCF-2126672/-2349141   Oct 2021 – Oct 2024

Standard GPU Algorithms with Task Graph Parallelism
PI, $5K, NumFOCUS Small Development Grant   May 2021 – Feb 2022

Taskflow-San: Sanitizing Erroneous Control Flows in Taskflow
PI, $5K, NumFOCUS Small Development Grant   May 2021 – Feb 2022

OpenTimer and DtCraft
PI, $427K, DARPA, FA 8650-18-2-7843   June 2018 – July 2019

Conference Publication

1. **[ASP-DAC'26]** Aditya Das Sarma, Shui Jiang, Wan-Luan Lee, Tsung-Yi Ho, and Tsung-Wei Huang, "TIMBER: A Fast Algorithm for Timing and Power Optimization using Multi-bit Flip-flops," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Hong Kong, 2026

2. **[HPEC'25]** Chedi Morchdi, Cheng-Hsiang Chiu, Wan-Luan Lee, Tsung-Wei Huang, and Yi Zhou, "Enhancing Graph Partitioning with Reinforcement Learning-based Initialization", *IEEE High-performance and Extreme Computing Conference (HPEC)*, virtual, 2025

3. **[HPEC'25]** Jie Tong, Zhengxiong Li, Umit Yusuf Ogras, and Tsung-Wei Huang, "A Scalable Code Generation Flow for Heterogeneous Parallel RTL Simulation using MLIR", *IEEE High-performance and Extreme Computing Conference (HPEC)*, virtual, 2025

4. **[MLCAD'25]** Cheng-Hsiang Chiu, Chedi Morchdi, Chih-Chun Chang, Cunxi Yu, Yi Zhou, and Tsung-Wei Huang, "Optimizing CUDA Graph Scheduling with Reinforcement Learning: A Case Study in SSTA Propagation," *ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD)*, San Cruz, CA, 2025

5. **[Euro-Par'25]** Yi-Hua Chung, Shui Jiang, Wan Luan Lee, Yanqing Zhang, Haoxing Ren, Tsung-Yi Ho, and Tsung-Wei Huang, "SimPart: A Simple Yet Effective Replication-aided Partitioning Algorithm for Logic Simulation on GPU," *International European Conference on Parallel and Distributed Computing (Euro-Par)*, Dresden, Germany, 2025

6. **[Euro-Par'25]** Jie Tong, Wan-Luan Lee, Umit Yusuf Ogras, and Tsung-Wei Huang, "Scalable Code Generation for RTL Simulation of Deep Learning Accelerators with MLIR," *International European Conference on Parallel and Distributed Computing (Euro-Par)*, Dresden, Germany, 2025

7. **[DAC'25]** Wan-Luan Lee, Shui Jiang, Dian-Lun Lin, Che Chang, Boyang Zhang, Yi-Hua Chung, Ulf Schlichtmann, Tsung-Yi Ho, and Tsung-Wei Huang, "iG-kway: Incremental k-way Graph Partitioning on GPU," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2025

8. **[DAC'25]** Chih-Chun Chang and Tsung-Wei Huang, "Statistical Timing Graph Scheduling Algorithm for GPU Computation," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2025

9. **[DAC'25]** Chih-Chun Chang and Tsung-Wei Huang, "Statistical Timing Graph Scheduling Algorithm for GPU Computation," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2025

10. **[ASPLOS'25]** Shui Jiang, Yi-Hua Chung, Chih-Chun Chang, Tsung-Yi Ho, and Tsung-Wei Huang, "BQSim: GPU-accelerated Batch Quantum Circuit Simulation using Decision Diagram," *ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Rotterdam, Netherlands, 2025

11. **[FCPC'25]** Pao-I Chen and Tsung-Wei Huang, "An Efficient Implemenetation of Parallel Breadth-first Search," *ACM SIGPLAN PPoPP Workshop on Fast Code Programming Challenge (FCPC)*, Las Vegas, Nevada, 2025

12. **[ExHET'25]** Serhan Gener, Sahil Hassan, Liangliang Chang, Chaitali Chakrabarti, Tsung-Wei Huang, Umit Ograss, and Ali Akoglu, "A Unified Portable and Programmable Framework for Task-Based Execution and Dynamic Resource Management on Heterogeneous Systems," *ACM International Workshop on Extreme Heterogeneity Solutions (ExHET)*, Las Vegas, Nevada, 2025

13. **[WAMTA'25]** Cheng-Hsiang Chiu, Wan-Luan Lee, Boyang Zhang, Yi-Hua Chung, Che Chang, and Tsung-Wei Huang, "A Task-parallel Pipeline Programming Model with Token Dependency," *Workshop on Asynchronous Many-Task Systems and Applications (WAMTA)*, St. Louis, MO, 2025

14. **[ASP-DAC'25]** Wan-Luan Lee, Dian-Lun Lin, Cheng-Hsiang Chiu, Ulf Schlichtmann, and Tsung-Wei Huang, "HyperG: Multilevel GPU-Accelerated k-way Hypergraph Partitioner," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, 2025

15. **[ASP-DAC'25]** Boyang Zhang, Che Chang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yang Sui, Chih-Chun Chang, Yi-Hua Chung, Wan-Luan Lee, Zizheng Guo, Yibo Lin, and Tsung-Wei Huang, "iTAP: An Incremental Task Graph Partitioner for Task-parallel Static Timing Analysis," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, 2025

16. **[ASP-DAC'25]** Che Chang, Boyang Zhang, Cheng-Hsiang Chiu, Dian-Lun Lin, Yi-Hua Chung, Wan-Luan Lee, Zizheng Guo, Yibo Lin, and Tsung-Wei Huang, "PathGen: An Efficient Parallel Critical Path Generation Algorithm," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, 2025

17. **[ASP-DAC'25]** Cheng-Hsiang Chiu, Chedi Morchdi, Yi Zhou, Boyang Zhang, Che Chang, and Tsung-Wei Huang, "Reinforcement Learning-generated Topological Order for Dynamic Task Graph Scheduling," *IEEE High-performance and Extreme Computing Conference (HPEC)*, MA, 2024

18. **[ICCAD'25]** Zizheng Guo, Zuodong Zhang, Wuxi Li, Tsung-Wei Huang, Xizhe Shi, Yufan Du, Yibo Lin, Runsheng Wang, and Ru Huang, "HeteroExcept: Heterogeneous Engine for General Timing Path Exception Analysis," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, New York, 2024

19. **[ICPP'24]** Chih-Chun Chang, Boyang Zhang, and Tsung-Wei Huang, "GSAP: A GPU-Accelerated Stochastic Graph Partitioner" *ACM International Conference on Parallel Processing (ICPP)*, Gotland, Sweden, 2024

20. **[ICPP'24]** Shui Jiang, Rongliang Fu, Lukas Burgholzer, Robert Wille, Tsung-Yi Ho, and Tsung-Wei Huang, "FlatDD: A High-Performance Quantum Circuit Simulator using Decision Diagram and Flat Array," *ACM International Conference on Parallel Processing (ICPP)*, Gotland, Sweden, 2024

21. **[Euro-Par'24]** Dian-Lun Lin, Joshua San Miguel, Umit Ogras, Tsung-Wei Huang, "TaroRTL: Accelerating RTL Simulation using Coroutine-based Heterogeneous Task Graph Scheduling," *International European Conference on Parallel and Distributed Computing (Euro-Par)*, Madrid, Spain, 2024

22. **[DAC'24]** Wan Luan Lee, Dian-Lun Lin, Tsung-Wei Huang, Shui Jiang, Tsung-Yi Ho, Yibo Lin, and Bei Yu, "G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2024

23. **[DAC'24]** Che Chang, Tsung-Wei Huang, Dian-Lun Lin, Guannan Guo, and Shiju Lin, "Ink: Efficient Incremental k-Critical Path Generation," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2024

24. **[DAC'24]** Boyang Zhang, Dian-Lun Lin, Che Chang, Cheng-Hsiang Chiu, Bojue Wang, Wan Luan Lee, Chih-Chun Chang, Donghao Fang, and Tsung-Wei Huang, "G-PASTA: GPU Accelerated Partitioning Algorithm for Static Timing Analysis," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2024

25. **[DAC'24]** Shiju Lin, Guannan Guo, Tsung-Wei Huang, Weihua Sheng, Evangeline Young, and Martin Wong, "GCS-Timer: GPU-Accelerated Current Source Model Based Static Timing Analysis," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2024

26. **[ISVLSI'24]** Jie Tong, Liangliang Chang, Umit Yusuf Ogras, and Tsung-Wei Huang, "BatchSim: Parallel RTL Simulation using Inter-cycle Batching and Task Graph Parallelism," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Knoxville, Tennessee, 2024

27. **[ISVLSI'24]** Che Chang, Cheng-Hsiang Chiu, Boyang Zhang, and Tsung-Wei Huang, "Incremental Critical Path Generation for Dynamic Graphs," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Knoxville, Tennessee, 2024

28. **[ISVLSI'24]** Cheng-Hsiang Chiu and Tsung-Wei Huang, "An Experimental Study of Dynamic Task Graph Parallelism for Large-Scale Circuit Analysis Workloads," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Knoxville, Tennessee, 2024

29. **[AAMAS'24]** Shao-Hung Chan, Zhe Chen, Dian-Lun Lin, Yue Zhang, Daniel Harabor, Tsung-Wei Huang, Sven Koenig, and Thomy Phan, "Anytime Multi-Agent Path Finding using Operator Parallelism in Large Neighborhood Search," *International Conference on Autonomous Agents and Multi-Agent Systems (AAMAS)*, Auckland, New Zealand, 2024

30. **[ISPD'24]** Tsung-Wei Huang, Boyang Zhang, Dian-Lun Lin, and Cheng-Hsiang Chiu, "Parallel and Heterogeneous Timing Analysis: Partition, Algorithm, and System," *ACM International Symposium on Physical Design (ISPD)*, Taipei, Taiwan, 2024

31. **[HPC-Asia]** Cheng-Hsiang Chiu, Zhicheng Xiong, Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "An Efficient Task-parallel Pipeline Programming Framework," *ACM International Conference on High-performance Computing in Asia-Pacific Region (HPC-Asia)*, Nagoya, Japan, 2024

32. **[DATE'24]** Zizheng Guo, Tsung-Wei Huang, Jin Zhou, Cheng Zhuo, Yibo Lin, Runsheng Wang, and Ru Huang, "Heterogeneous Static Timing Analysis with Advanced Delay Calculator," *IEEE/ACM Design, Automation and Test in Europe Conference (DATE)*, Valencia, Spain, 2024

33. **[ASP-DAC'24]** Chedi Morchdi, Cheng-Hsiang Chiu, Yi Zhou, and Tsung-Wei Huang, "A Resource-efficient Task Scheduling System using Reinforcement Learning," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Korea, 2024

34. **[ICCAD'23]** Cheng-Hsiang Chiu, Dian-Lun Lin, and Tsung-Wei Huang, "Programming Dynamic Task Parallelism for Heterogeneous EDA Algorithms," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2023

35. **[ICCAD'23]** Takashi Sato, Chun-Yao Wang, Yu-Guang Chen, and Tsung-Wei Huang, "Overview of 2023 CAD Contest at ICCAD," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2023

36. **[HPEC'23]** Shui Jiang, Tsung-Wei Huang, and Tsung-Yi Ho, "GLARE: Accelerating Sparse DNN Inference Kernels with Global Memory Access Reduction," *IEEE High Performance Extreme Computing (HPEC)*, Virtual, 2023 (**Graph Challenge Innovation Award**)

37. **[HPEC'23]** Chih-Chun Chang and Tsung-Wei Huang, "GLARE: Accelerating Sparse DNN Inference Kernels with Global Memory Access Reduction," *IEEE High Performance Extreme Computing (HPEC)*, Virtual, 2023 (**Graph Challenge Innovation Award**)

38. **[ICPP'23]** Shui Jiang, Tsung-Wei Huang, Bei Yu, and Tsung-Yi Ho, "SNICIT: Accelerating Sparse Neural Network Inference via Compression at Inference Time on GPU," *ACM International Conference on Parallel Processing (ICPP)*, Salt Lake City, Utah, 2023

39. **[DAC'23]** Dian-Lun Lin, Yanqing Zhang, Haoxing Ren, Shih-Hsin Wang, Brucek Khailany, and Tsung-Wei Huang, "GenFuzz: GPU-accelerated Hardware Fuzzing using Genetic Algorithm with Multiple Inputs," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2023

40. **[IPDPS'23]** Tsung-Wei Huang, "qTask: Task-parallel Quantum Circuit Simulation with Incrementality," *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, St. Petersburg, Florida, 2023

41. **[IPDPSW'23]** Elmir Dzaka, Dian-Lun Lin, and Tsung-Wei Huang, "Parallel And-Inverter Graph Simulation Using a Task-graph Computing System," *IEEE International Parallel and Distributed Processing Symposium Workshop (IPDPSW)*, St. Petersburg, Florida, 2023

42. **[DATE'23]** Guannan Guo, Martin D. F. Wong, and Tsung-Wei Huang, "Fast STA Graph Partitioning Framework for Multi-GPU Acceleration," *IEEE/ACM Design, Automation and Test in Europe Conference (DATE)*, Antwerp, Belgium, 2023

43. **[HPEC'22]**Tsung-Wei Huang and Leslie Hwang, "Task-parallel Programming with Constrained Parallelism," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2022

44. **[HPEC'22]** Tsung-Wei Huang, "Enhancing the Performance Portability of Heterogeneous Circuit Analysis Programs," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2022

45. **[ICPP'22]** Dian-Lun Lin, Haoxing Ren, Yanqing Zhang, Brucek Khailany, and Tsung-Wei Huang, "From RTL to CUDA: A GPU Acceleration Flow for RTL Simulation with Batch Stimulus," *ACM International Conference on Parallel Processing (ICPP)*, Bordeaux, France, 2022

46. **[HPDC'22]** Cheng-Hsiang Chiu and Tsung-Wei Huang, "Composing Pipeline Parallelism using Control Taskflow Graph," *ACM International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, Minneapolis, Minnesota, 2022

47. **[ICCAD'22]** Yu-Guan Chen, Chun-Yao Wang, Tsung-Wei Huang, and Takashi Sato, "Overview of 2022 CAD Contest at ICCAD," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, CA, 2022

48. **[DAC'22]** Cheng-Hsiang Chiu and Tsung-Wei Huang, "Efficient Timing Propagation with Simultaneous Structural and Pipeline Parallelisms," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2022

49. **[HIPS'22]** Tsung-Wei Huang and Yibo Lin, "Concurrent CPU-GPU Task Programming using Modern C++," *International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS)*, France, 2022

50. **[ASP-DAC'22]** Kexing Zhou, Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "Efficient Critical Paths Search Algorithm using Mergeable Heap," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taiwan, 2022

51. **[DAC'21]** Guannan Guo, Tsung-Wei Huang, and Martin Wong, "GPU-accelerated Path-based Timing Analysis," *ACM/IEEE Design Automation Conference (DAC)*, CA, 2021

52. **[DAC'21]** Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "A Provably Good and Practically Efficient Common Path Pessimism Removal Algorithm for Large Designs," *ACM/IEEE Design Automation Conference (DAC)*, CA, 2021

53. **[ESPM2'21]** McKay Mower, Luke Majors, and Tsung-Wei Huang, "Taskflow-San: Sanitizing Erroneous Control Flow in Taskflow Programs," *IEEE Workshop on Extreme Scale Programming Models and Middleware (ESPM2)*, St. Louis, Missouri, 2021

54. **[ProTools'21]** Tsung-Wei Huang, "TFProf: Profiling Large Taskflow Programs with Modern D3 and C++," *IEEE International Workshop on Programming and Performance Visualization Tools (ProTools)*, St. Louis, Missouri, 2021

55. **[Euro-Par'21]** Dian-Lun Lin and Tsung-Wei Huang, "Efficient GPU Computation using Task Graph Parallelism," *European Conference on Parallel and Distributed Computing (Euro-Par)*, Portugal, 2021

56. **[HPEC'21]** Yasin Zamani and Tsung-Wei Huang, "A High-Performance Heterogeneous Critical Path Analysis Framework," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2021

57. **[AMET'21]** Cheng-Hsiang Chiu, Dian-Lun Lin and Tsung-Wei Huang, "An Experimental Study of SYCL Task Graph Parallelism for Large-Scale Machine Learning Workloads," *International Workshop of Asynchronous Many-Task Systems for Exascale (AMTE)*, 2021

58. **[ICCAD'21]** Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "HeteroCPPR: Accelerating Common Path Pessimism Removal with Heterogeneous CPU-GPU Parallelism," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, Germany, 2021

59. **[ICCAD'21]** Guannan Guo, Tsung-Wei Huang, Yibo Lin, and Martin D. F. Wong, "GPU-accelerated Critical Path Generation with Path Constraints," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, Germany, 2021

60. **[ICCAD'21]** Tsung-Wei Huang, Yu-Guan Chen, Chun-Yao Wang, and Takashi Sato, "Overview of 2021 CAD Contest at ICCAD," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, Germany, 2021

61. **[ASP-DAC'21]** Kuan-Ming Lai, Tsung-Wei Huang, Pei-Yu Lee, and Tsung-Yi Ho, "ATM: A High Accuracy Extracted Timing Model for Hierarchical Timing Analysis," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, 2021

62. **[ICPADS'21]** Chun-Xun Lin, Tsung-Wei Huang, and Martin D. F. Wong, "An Efficient Work-Stealing Scheduler for Task Dependency Graph," *IEEE International Conference on Parallel and Distributed Systems (ICPADS)*, Hong Kong, 2020

63. **[HPEC'20]** Dian-Lun Lin and Tsung-Wei Huang, "A Novel Inference Algorithm for Large Sparse Neural Network using Task Graph Parallelism," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2020 (**Graph Challenge Champion Award**)

64. **[ICCAD'20]** Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "GPU-Accelerated Static Timing Analysis," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020

65. **[ICCAD'20]** Tsung-Wei Huang, "A General-purpose Parallel and Heterogeneous Task Programming System for VLSI CAD," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020

66. **[ICCAD'20]** Ing-Chao Lin, Ulf Schlichtmann, Tsung-Wei Huang, and Pao-Hun Lin, "Overview of 2020 CAD Contest at ICCAD," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020

67. **[DAC'20]** Guannan Guo, Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "An Efficient Critical Path Generation Algorithm Considering Extensive Path Constraints," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2020

68. **[MM'19]** Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo, and Martin D. F. Wong, "A Modern C++ Parallel Task Programming Library," *ACM Multimedia Conference (MM)*, Nice, France, 2019 (**Second Prize of Open-Source Software Competition**)

69. **[HPEC'19]** Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo, and Martin D. F. Wong, "An Efficient and Composable Parallel Programming Library," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2019

70. **[IPDPS'19]** Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, "Cpp-Taskflow: Fast Task-based Parallel Programming using Modern C++," *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, Rio De Janeiro, Brazil, 2019

71. **[DAC'19]** Kuan-Ming Lai, Tsung-Wei Huang, and Tsung-Yi Ho, "A General Cache Framework for Efficient Generation of Timing Critical Paths," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019

72. **[DAC'19]** Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, "Essential Building Blocks for Creating an Open-source EDA Project," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019

73. **[DAC'19]** Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "Distributed Timing Analysis at Scale," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019

74. **[MM'18]** Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, "A General-purpose Distributed Programming Systems using Data-parallel Streams," *ACM Multimedia Conference (MM)*, Seoul, Korea, 2018 (**Best Open-Source Software Award**)

75. **[DEBS'18]** Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo, and Martin D. F. Wong, "MtDetector: A High-performance Marine Traffic Detector at Stream Scale," *ACM Distributed Event-based System Conference (DEBS)*, Hamilton, New Zealand, 2018

76. **[GLSVLSI'18]** Chun-Xun Lin, Tsung-Wei Huang, T. Yu, and Martin D. F. Wong, "A Distributed Power Grid Analysis Framework from Sequential Stream Graph," *ACM Great Lakes Symposium (GLSVLSI)*, Chicago, IL, 2018

77. **[ISQED'18]** Chun-Xun Lin, Tsung-Wei Huang, and Martin D. F. Wong, "Routing at Compile Time," *IEEE International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, 2018

78. **[ICCAD'17]** Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "DtCraft: A Distributed Execution Engine for Compute-intensive Applications," *ACM/IEEE International Conference on Computer-aided Design (ICCAD)*, Irvine, CA, 2017

79. **[DAC'17]** Tin-Yin Lai, Tsung-Wei Huang, and Martin D. F. Wong, "An Effective and Accurate Macro-modeling Algorithm for Large Hierarchical Designs," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, 2017 (First Place of TAU Timing Analysis Contest)

80. **[DAC'16]** Tsung-Wei Huang, Martin D. F. Wong, D. Sinha, K. Kalafala, and N. Venkateswaran, "A Distributed Timing Analysis Framework for Large Designs," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, 2016

81. **[ICCAD'15]** Tsung-Wei Huang and Martin D. F. Wong, "OpenTimer: A High-performance Timing Analysis Tool," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, TX, 2015 (**2024 ICCAD 10-year Retrospective Most Influential Paper Award**)

82. **[SLIP'15]** Tsung-Wei Huang and Martin D. F. Wong, "On Fast Timing Closure: Speeding Up Incremental Path-Based Timing Analysis with MapReduce," *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, CA, 2015

83. **[ISPD'15]** Tsung-Wei Huang and Martin D. F. Wong, "Accelerated Path-Based Timing Analysis with MapReduce," *ACM International Symposium on Physical Design (ISPD)*, Monterey, CA, 2015

84. **[ICCAD'14]** Tsung-Wei Huang, P.-C. Wu, and Martin D. F. Wong, "Fast Path-Based Timing Analysis for CPPR," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2014 (First Place of TAU Timing Analysis Contest)

85. **[ICCAD'14]** Tsung-Wei Huang, P.-C. Wu, and Martin D. F. Wong, "UI-Timer: An Ultra-Fast Clock Network Pessimism Removal Algorithm," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2014

86. **[SLIP'14]** Tsung-Wei Huang, P.-C. Wu, and Martin D. F. Wong, "UI-Route: An Ultra-Fast Incremental Maze Routing Algorithm," *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, San Francisco, CA, 2014

87. **[ICCAD'12]** S.-H. Yeh, J.-W. Chang, Tsung-Wei Huang, and Tsung-Yi Ho, "Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2012

88. **[ISPD'12]** Tsung-Wei Huang, J.-W. Chang, and Tsung-Yi Ho, "Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips," *ACM International Symposium on Physical Design (ISPD)*, Napa, CA, 2012

89. **[ASP-DAC'12]** J.-W. Chang, Tsung-Wei Huang, and Tsung-Yi Ho, "An ILP-based Obstacle-Avoiding Routing Algorithm for Pin-Constrained EWOD Chips," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Sydney, Australia, 2012

90. **[ICCAD'11]** Tsung-Wei Huang, Tsung-Yi Ho, and K. Chakrabarty, "Reliability-Oriented Broadcast Electrode-Addressing for Pin-Constrained Digital Microfluidic Biochips," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2011

91. **[SOCC'11]** Tsung-Wei Huang, Yan-You Lin, J.-W. Chang, and Tsung-Yi Ho, "Recent Research and Emerging Challenges in the Designs and Optimizations for Digital Microfluidic Biochips," *IEEE System on Chip Conference (SOCC)*, 2011.

92. **[MWSCAS'11]** Tsung-Wei Huang, Yan-You Lin, J.-W. Chang, and Tsung-Yi Ho, "Chip-Level Design and Optimization for Digital Microfluidic Biochips," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011.

93. **[SLIP'11]** P.-H. Yuh, C. C.-Y. Lin, Tsung-Wei Huang, Tsung-Yi Ho, C.-L. Yang, and Y.-W. Chang, "A SAT-Based Routing Algorithm for Cross-Referencing Biochips," *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, San Diego, CA, June 2011.

94. **[DAC'11]** Tsung-Wei Huang, H.-Y. Su, and Tsung-Yi Ho, "Progressive Network-Flow Based Broadcast Addressing for Pin-Constrained Digital Microfluidic Biochips," *ACM/IEEE Design Automation Conference (DAC)*, pp. 741—746, San Diego, CA, June 2011.

95. **[ICCAD'10]** Tsung-Wei Huang, S.-Y. Yeh, and Tsung-Yi Ho, "A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast Electrode-Addressing EWOD Chips," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, pp. 425-431, San Jose, CA, 2010.

96. **[ISPD'10]** Tsung-Wei Huang and Tsung-Yi Ho, "A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips," *ACM International Symposium on Physical Design (ISPD)*, pp. 201—208, San Francisco, CA, 2010.

97. **[ICCAD'09]** Tsung-Wei Huang, C.-H. Lin, and Tsung-Yi Ho, "A Contamination-Aware Droplet Routing Algorithm for Digital Microfluidic Biochips," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, pp. 151—156, San Jose, CA, 2009.

98. **[ICCD'09]** Tsung-Wei Huang and Tsung-Yi Ho, "A Fast Routability- and Performance-Driven Droplet Routing Algorithm for Digital Microfluidic Biochips," *IEEE International Conference on Computer Design (ICCD)*, pp. 445—450, Lake Tahoe, CA, 2009

JOURNAL PUBLICATION

1. **[FGCS'25]** Serhan Gener, Sahil Hassan, H. Umut Suluhan, Liangliang Chang, Chaitali Chakrabarti, Tsung-Wei Huang, Umit Ogras, and Ali Akoglu, "A portable framework with generalized runtime features for task graph execution and concurrent multi-application deployment on heterogeneous systems," *Future Generation Computer Systems (FGCS)*, 2025

2. **[TODAES'25]** Wan-Luan Lee, Dian-Lun Lin, Shui Jiang, Cheng-Hsiang Chiu, Yibo Lin, Bei Yu, Tsung-Yi Ho, and Tsung-Wei Huang, "G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner using Task Graph Parallelism," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2025

3. **[TCAD'23]** G. Guo, Tsung-Wei Huang, Y. Lin, Z. Guo, S. Yellapragada, and M. D. F. Wong, "A GPU-Accelerated Framework for Path-Based Timing Analysis," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 42, no. 11, pp. 4219-4232, Nov. 2023

4. **[TCAD'23]** Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "Accelerating Static Timing Analysis using CPU-GPU Heterogeneous Parallelism," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 12, pp. 4973-4984, Dec. 2023

5. **[TPDS'22]** Dian-Lun Lin and Tsung-Wei Huang, "Accelerating Large Sparse Neural Network Inference using GPU Task Graph Parallelism," *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 33, no. 11, pp. 3041—3052, Nov 2022

6. **[TPDS'22]** Tsung-Wei Huang, Dian-Lun Lin, Chun-Xun Lin, and Yibo Lin, "Taskflow: A Lightweight Parallel and Heterogeneous Task Graph Computing System," *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 33, no. 6, pp. 1303—1320, June 2022

7. **[TCAD'22]** Zizheng Guo, Mingwei Yang, Tsung-Wei Huang, and Yibo Lin, "A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 10, pp. 3466—3478, Oct. 2022

8. **[JMIR'22]**Jia-Ruei Yu, Chun-Hsien Chen, Tsung-Wei Huang, Jang-Jih Lu, Chia-Ru Chung, Ting-Wei Lin, Min-Hsien Wu, Yi-Ju Tseng, Hsin-Yao Wang, "Energy Efficiency of Inference Algorithms for Medical Datasets: A Green AI study," *Journal of Medical Internet Research (JMIR)*, vol. 24, no. 1, Jan. 2022

9. **[TCAD'22]** Tsung-Wei Huang, Dian-Lun Lin, Yibo Lin, and Chun-Xun Lin, "Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 5, pp. 1448—1452, May 2022

10. **[DAT'21]** Tsung-Wei Huang, Chun-Xun Lin, and Martin. D. F. Wong, "OpenTimer v2: A Parallel Incremental Timing Analysis Engine," *IEEE Design and Test (DAT)*, vol. 38, no. 2, pp. 62—68, April 2021

11. **[TCAD'21]** Tsung-Wei Huang, Yibo Lin, Chun-Xun Lin, Guannan Guo, and Martin. D. F. Wong, "Cpp-Taskflow: A General-purpose Parallel Task Programming System at Scale," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 8, pp. 1687—1700, Aug. 2021

12. **[TCAD'21]** Tsung-Wei Huang, Guannan Guo, Chun-Xun Lin, and Martin. D. F. Wong, "OpenTimer v2: A New Parallel Incremental Timing Analysis Engine," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 4, pp. 776—789, April, 2021

13. **[TCAD'18]** Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "DtCraft: A High-performance Distributed Execution Engine at Scale," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 6, pp. 1070—1083, June 2018

14. **[TCAD'16]** Tsung-Wei Huang and Martin D. F. Wong, "UI-Timer 1.0: An Ultra-Fast Path-Based Timing Analysis Algorithm for CPPR," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 11, pp. 1862—1875, Nov. 2016

15. **[TCAD'14]** S.-H. Yeh, J.-W. Chang, Tsung-Wei Huang, S.-T. Yu, and Tsung-Yi Ho, "Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no.9, pp. 1302—1315, Sep. 2014.

16. **[TCAD'13]** J.-W. Chen, C.-L. Hsu, L.-C. Tsai, Tsung-Wei Huang, and Tsung-Yi Ho, "An ILP-Based Routing Algorithm for Pin-Constrained EWOD Chips with Obstacle Avoidance," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no.11, pp. 1655—1667, Nov. 2013.

17. **[TCAD'13]** Y.-H. Chen, C.-L. Hus, Tsung-Wei Huang, and Tsung-Yi Ho, "A Reliability-Oriented Placement Algorithm for Reconfigurable Digital Microfluidic Biochips using 3D Deferred Decision-Making Technique," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 8, pp. 1151—1162, Aug. 2013.

18. **[TCAD'13]** J.-W. Chang, S.-H. Yeh, Tsung-Wei Huang, and Tsung-Yi Ho, "Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no 2, pp. 216—227, Feb. 2013.

19. **[TCAD'11]** Tsung-Wei Huang, S.-Y. Yeh, and Tsung-Yi Ho, "A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast-Addressing EWOD Chips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 12, pp. 1786—1799, Dec. 2011.

20. **[TCAD'11]** Tsung-Wei Huang and Tsung-Yi Ho, "A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 2, pp. 215—228, Feb. 2011.

21. **[TCAD'10]** Tsung-Wei Huang, C.-H. Lin, and Tsung-Yi Ho, "A Contamination-Aware Droplet Routing Algorithm for the Synthesis of Digital Microfluidic Biochips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 29, no. 11, pp. 1682—1695, Nov. 2010.

PATENT

Incremental Common Path Pessimism Analysis	USA-14/946043
Tsung-Wei Huang, K. Kalafala, D. Sinha, and N. Venkateswaran	
Distributed Timing Analysis of a Partitioned Integrated Circuit Design	USA-9916405B2
Tsung-Wei Huang, K. Kalafala, D. Sinha, and N. Venkateswaran	

1. "Dynamic Asynchronous Tasking with Dependencies," CppCon, Sep 2025
2. "Taskflow: A General-purpose Task-parallel Programming System," Synopsys, Aug 2025
3. "An Efficient Implementation of Parallel BFS Algorithm," PPoPP FCPC, March 2025
4. "Intelligent High-performance Computing," Arizona State University, Oct 2024
5. "Scientific Research and Grant Writing," DAC Early Career Workshop, June 2024
6. "Taskflow: A General-purpose Task-parallel Programming System," Rapid Silicon, June 2024
7. "Intelligent High-performance Computing," University of Colorado Boulder, June 2024
8. "Intelligent High-performance Computing," University at Buffalo, May 2024
9. "Taskflow: A General-purpose Task-parallel Programming System," Cpp Rusia, May 2024
10. "Taskflow: A General-purpose Task-parallel Programming System," UCLA VAST Lab, April 2024
11. "Taskflow: A General-purpose Task-parallel Programming System," Cadence, April 2024
12. "Taskflow: A General-purpose Task-parallel Programming System," UC Santa Cruz, March 2024
13. "Taskflow: A General-purpose Task-parallel Programming System," FlexCompute Inc, Feb 2024
14. "Taskflow: A General-purpose Task-parallel Programming System," Chinese Univ of HK, Jan 2024
15. "Taskflow: A General-purpose Task-parallel Programming System," China Univ of Petroleum, Oct 2023
16. "Quantum Circuit Simulation with Incrementality," University at Buffalo, June 2023
17. "Intelligent High-performance Computing," Technical University of Munich, June 2023
18. "Taskflow: A General-purpose Task-parallel Programming System," Univ of Notre Dame, May 2023
19. "A General-purpose Task-parallel Programming System," Cruise LLC, April 2023
20. "Performance Portability and Optimization using Machine Learning," PNNL-Utah Seminar, Nov 2022
21. "Intelligent Heterogeneous Parallelism," ACCESS-CEDA Seminar Series, Hong Kong, Sep 2022
22. "Intelligent Heterogeneous Parallelism," CS Department, UC Merced, Sep 2022
23. "Programming System for Building High-performance CAD Applications," Google X, Sep 2022
24. "A General-purpose Parallel and Heterogeneous Task Programming System," AMD, Aug 2022
25. "A GPU Acceleration Flow for RTL Simulation with Batch Stimulus," Invited Talk, IWLS, July 2022
26. "Intelligent Heterogeneous Computing," AMD Research, June 2022
27. "Intelligent Heterogeneous Computing," ECE Department, Johns Hopkins University, March 2022
28. "Intelligent Heterogeneous Computing," ECE Department, Stevens Institute of Technology, 2022
29. "Intelligent Heterogeneous Computing," ECE Department, University of Minnesota, Feb 2022
30. "Taskflow: A General-purpose Heterogeneous Task Programming System," IXPUG, 2021
31. "cudaFlow: A Modern C++ Programming Model for GPU Task Graph Parallelism," CppCon, 2021
32. "A General-purpose Heterogeneous Task Computing System," Chinese Univ of HK, Aug 2021
33. "HeteroTime: Accelerating Static Timing Analysis with GPUs," Nvidia Research, June 2021
34. "Taskflow: A Lightweight Heterogeneous Task Programming System," CPPNow, 2021
35. "GPU-Accelerated Static Timing Analysis and Beyond," GTC, April 2021
36. "Machine Learning-enabled System for EDA," VLSI-DAT, April 2021
37. "GPU-Accelerated Static Timing Analysis," UC Santa Cruz, EDA Seminar, Feb 2021
38. "A General-purpose Heterogeneous Task Programming System," CIE/USA-GNYC, Oct 2020
39. "Taskflow: Parallel and Heterogeneous Task Programming in C++," C++ Meetup, Oct 2020
40. "Taskflow: A General-purpose Heterogeneous Task Programming System," CppIndia, Oct 2020
41. "Taskflow: A General-purpose Heterogeneous Task Programming System," MUC++, Oct 2020
42. "Programming Systems for Parallelizing VLSI CAD and Beyond," VLSI-DAT, April 2020
43. "A General-purpose Heterogeneous Task Programming System at Scale," ORNL, March 2020
44. "Growing Your Open-Source Projects," WOSET at IEEE/ACM ICCAD, November 2019
45. "Essential Building Blocks for Creating an Open-source EDA Project," IEEE/ACM DAC, June 2019
46. "Task-based Parallel Programming using Modern C++," CSL Social Hour, Sep 2018
47. "Distributed Timing Analysis in 100 Lines of Code," VSD webinar, May 2018

48. "DtCraft: A High-performance Distributed Execution Engine at Scale," CSLSC, UIUC, 2018
49. "OpenTimer: An open-source high-performance timing analysis tool," ORCONF, Italy, 2016
50. "Distributed Timing Analysis: Framework and Systems," Cadence, Austin, June 2016
51. "OpenTimer: A High-performance Timing Analysis Tool," Invited Talk, ICCAD, 2015
52. "Fast Path-based Timing Analysis," Invited Talk, ICCAD, 2014

PH.D. STUDENTS

Wan-Luan Lee	Spring 2022 – Dec 2025
Thesis: GPU-accelerated Graph Partitioning Algorithms in VLSI Design	UW-Madison ECE PhD
Cheng-Hsiang Chiu	Fall 2020 – Summer 2025
Thesis: Asynchronous Many-task Systems with Intelligent Scheduling	UW-Madison ECE PhD
Jie Tong (co-supervised with Prof. Umit Y. Ogras)	Fall 2023 – Summer 2025
Thesis: Towards Scalable and Efficient Parallel RTL and Network Simulation Systems	UW-Madison ECE PhD
Dian-Lun Lin	Spring 2020 – Aug 2024
Thesis: Task-parallel Heterogeneous Programming System for Logic Simulation	UW-Madison ECE PhD
Guannan Guo (co-supervised with Prof. Martin Wong at UIUC)	Aug 2018 – Dec 2023
Thesis: Parallel and Heterogeneous Computing for Static Timing Analysis	UIUC ECE PhD
Che Chang	Spring 2022 – present
Thesis: TBD	
Shui Jiang (co-supervised with Prof. Tsung-Yi Ho)	Fall 2022 – present
Thesis: TBD	
Chih-Chun Chang	Spring 2023 – present
Thesis: TBD	
Boyang Zhang	Spring 2023 – present
Thesis: TBD	
Yi-Hua Chung	Fall 2023 – present
Thesis: TBD	
Aditya Das Sarma	Fall 2024 – present
Thesis: TBD	

INDUSTRIAL EXPERIENCE

Software Engineer, High-performance Computing Group, Citadel, IL	May 2017 – Aug 2017
Developed machine learning benchmarks and optimization tips for financial workloads	
Software Engineer, Timing Analysis Group, IBM, NY	May 2015 – Aug 2015
Developed a distributed timing analysis prototype atop Einstimer	
Software Engineer, Timing Analysis Group, Mentor Graphics, CA	May 2014 – Aug 2014
Developed optimization algorithms for tag-based incremental timing analysis	

SERVICE

Grant Review Panelist
Evaluated grant proposals based on intellectual merit and broader impacts
- NSF Office of Advanced Cyberinfrastructure (OAC)
- NSF Principles and Practice of Scalable Systems (PPoSS)
- NSF Cyber-physical Systems (CPS)
- NSF Software and Hardware Foundations (SHF)
- DOE Advanced Scientific Computing Research (ASCR)
- DOE High Energy Physics (HEP)

Workershop Organization

Organized workshops and meetings to foster collaboration in CAD, HPC, and Quantum
- NSF FuSe Workshop on Intelligent Photonic Materials, Devices, and Systems, 2024
- NSF FuSe Workshop on Quantum Computing and Systems, 2024
- ACM/IEEE DAC Open-source Bird of Feather, 2024

Chair/Co-chair

Engaged widespread contributions to solving cutting-edge HPC and CAD problems
- IEEE/ACM ICCAD CAD Contests, 2020–2023
- ACM SIGDA CADathlon International Programming Contest, 2018–2021
- ACM TAU Timing Analysis Contest, 2018

Program Committee

Selected top-quality papers and organized conference programs
- IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2026
- IEEE/ACM Design, Automation and Test in Europe Conference (DATE), 2025
- IEEE/ACM International Conference on Computer-aided Design (ICCAD), 2019–2022, 2024
- IEEE/ACM International Symposium on Microarchitecture (MICRO), 2024–2025
- ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD), 2024–2024
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2023–2024
- IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2024
- ACM/IEEE International Conference for High Performance Computing (SC), 2023
- ACM/IEEE Design Automation Conference (DAC), 2022–2025
- ACM International Workshop on Timing Issues (TAU), 2020–2021
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), 2020–2021
- IEEE International Conference on Computer Design (ICCD), 2020–2021
- International Workshop on Logic Synthesis (IWLS), 2020
- C++ Conference (CppCon), 2019–2021

Editorship

Managed peer-review processes and recommended what gets published
- Guest editor, Special Issue of VLSI Integration, 2022

Journal Reviewers

Evaluated submitted papers and recommended acceptance/rejection
- IEEE Transactions on Parallel and Distributed Computing Systems (TPDS)
- IEEE Transactions on Computer-aided Design for Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large-scale Integration (TVLSI)
- IEEE Transactions on Circuits and Systems (TCAS)
- IEEE Transactions on Big Data (TBD)
- IEEE Transactions on Architecture and Code Optimization (TACO)
- ACM Transaction son Design Automation of Electronic Systems (TODAES)
- ACM Journal of Emerging Technologies in Computing Systems (JETC)
- VLSI Integration Journal
- Concurrency and Computation: Practice and Experience
- Software X
- Journal of Computational Science

Departmental Committee at the University of Wisconsin at Madison

Helped the ECE department enhance various research and teaching programs
- Faculty Search Committee, 2024–2025
- Undergraduate Advisory Committee, 2024–Now
- Accelerated MS Committee, 2024–Now
- Graduate Student and Admission Committee, 2023–2024

Departmental Committee at the University of Utah

Helped the ECE department enhance various research and teaching programs
- Graduate Student and Admission Committee, 2021–2023
- University of Utah Asia Campus Committee, 2021–2023
- University of Utah Asia Campus Students Summer Visit Program, 2021
- University of Utah Asia Campus faculty recruiting committee, 2021–2023
- Artificial Intelligence and Data-science faculty recruiting committee, 2020

MISCELLANEOUS

Citizenship: Taiwan
Hobby: Piano playing, hiking, camping