Tsung-Wei (TW) Huang

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https://tsung-wei-huang.github.io/

Appointment

Assistant Professor, Department of Electrical and Computer Engineering July 2019 – Now
University of Utah, Salt Lake City, Utah, USA

Research Assistant Professor, Department of Electrical and Computer Engineering 2018 – June 2019
University of Illinois at Urbana-Champaign, IL, USA

Education

PhD, Department of Electrical and Computer Engineering Aug. 2013 – Dec. 2017
University of Illinois at Urbana-Champaign, IL, USA

MS, Department of Computer Science and Information Engineering July 2010 – July 2011
National Cheng Kung University, Tainan, Taiwan

BS, Department of Computer Science and Information Engineering Sep 2006 – June 2010
National Cheng Kung University, Tainan, Taiwan

Research Interest

High-performance Computing, Quantum Computing, Computer-aided Design
Our software has been downloaded over 1.5M times being used by many organizations:

- **Taskflkow** (heterogeneous programming system): https://tsung-wei-huang.github.io/
- **OpenTimer** (VLSI timing analysis tool): https://github.com/OpenTimer/OpenTimer
- **RTLflow** (GPU-accelerated RTL simulator): https://github.com/dian-lun-lin/rtlflow
- **SNIG** (sparse neural network inference): https://github.com/dian-lun-lin/SNIG
- **DtCraft** (distributed cluster programming): https://github.com/twhuang-uiuc/DtCraft

Awards

- ACM SIGDA Meritorious Service Award, 2022
- Humboldt Research Fellowship Award, Alexander von Humboldt Foundation, 2022
- Faculty Early Career Development Program (CAREER) Award, NSF, 2022
- Best Paper Award for "GPU-Accelerated Path-based Timing Analysis", ACM TAU Workshop, 2021
- Champion of the IEEE/MIT/Amazon HPEC Large Sparse Neural Network Challenge, 2020
- 2nd Place (Taskflow), Open-source Software Competition, ACM Multimedia Conference, 2019
- ACM SIGDA Outstanding PhD Dissertation Award (thesis title: "Distributed Timing Analysis"), 2019
- Best Tool Award (OpenTimer), Workshop on Open-source EDA Technology, 2018
- Best Open-source Software Award (DtCraft), ACM Multimedia Conference, 2018
- Best Poster Award for Open-source Parallel Programming Library (Taskflow), CPP Conference, 2018
- 2nd and 1st Place, ACM/SIGDA CADathlon International Programming Contest, 2014 and 2017
- 1st, 2nd, and 1st Place, ACM TAU Timing Analysis Contest, 2014 through 2016
- Yi-Min Wang and Pi-Yu Chung Endowed Research Award, ECE Dept. UIUC, 2016
- Rambus Computer Engineering Fellowship, ECE Dept. UIUC, 2015—2016
- Study Abroad Scholarship, Ministry of Education, Taiwan, 2013—2014
- 2nd Place, ACM Student Research Competition Grand Final, ACM Annual Award Banquet, 2011
- Best Master's Thesis Award, Taiwan Institute of Electrical and Electronic Engineering, 2011
- Best Master's Thesis Award, IEEE Taiwan Tainan Section, 2011

- Best Master's Thesis Award, Taiwan Institute of Information and Computing Machinery, 2011
- 1st Place, Master's Thesis Contest, Chinese Institute of Electrical Engineering, Taiwan, 2011
- Outstanding Graduate Recruiting Fellowship, National Cheng Kung University, 2010
- Outstanding Student Scholarship, Garmin Corporation, Taiwan, 2010
- 1st Place, ACM/SIGDA Student Research Competition, Design Automation Conference, 2010
- 3rd Place, National Collegiate Cell-Based IC Design Contest, Ministry of Education, Taiwan, 2010
- Distinguished Engineering Student Fellowship, Chinese Institute of Engineers, Taiwan, 2009
- 1st Place, National Collegiate Nano Device CAD Contest, Nano Device Laboratories, Taiwan, 2009
- 3rd Place, National Collegiate Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, National Collegiate IC/CAD Programming Contest, Ministry of Education, Taiwan, 2009
- 2nd Place, Presidential Award in CS Department, National Cheng Kung University, Taiwan, 2009

Research Grants

Toward a Task-Parallel Programming Ecosystem for Modern Scientific Computing
PI, $298K, NSF, TI-2229304 — Sep 2022 – Aug 2023

Developer Training Programs for Taskflow
PI, $5K, NumFOCUS Small Development Grant — Sep 2022 – May 2023

Transpiling Parallel Task Graph Programming Models for Scientific Software
PI, $488K, NSF, OAC-2209957 — July 2022 – July 2025

Taskflow with Constrained Parallelis
PI, $16K, NSF, CCF-2126672 (REU supplement) — Aug 2022 – Aug 2023

Accelerating Static Timing Analysis with Intelligent Heterogeneous Parallelism
PI, $500K, NSF, CCF-2144523 (CAREER) — Jan 2022 – Jan 2027

GPU Acceleration for Static Timing Analysis
PI, $10K (hardware donation), Nvidia Applied Research Acceleration Program — Nov 2021

A General-purpose Heterogeneous Task Graph Computing System for VLSI CAD
PI, $403K, NSF, CCF-2126672 — Oct 2021 – Oct 2024

Standard GPU Algorithms with Task Graph Parallelism
PI, $5K, NumFOCUS Small Development Grant — May 2021 – Feb 2022

Taskflow-San: Sanitizing Erroneous Control Flows in Taskflow
PI, $5K, NumFOCUS Small Development Grant — May 2021 – Feb 2022

OpenTimer and DtCraft
PI, $427K, DARPA, FA 8650-18-2-7843 — June 2018 – July 2019

Conference Publication

1. Dian-Lun Lin, Yanqing Zhang, Haoxing Ren, Shih-Hsin Wang, Brucek Khailany, and Tsung-Wei Huang, "GenFuzz: GPU-accelerated Hardware Fuzzing using Genetic Algorithm with Multiple Inputs," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2023
2. Tsung-Wei Huang "qTask: Task-parallel Quantum Circuit Simulation with Incrementality," *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, St. Petersburg, Florida, 2023
3. Guannan Guo, Martin D. F. Wong, and Tsung-Wei Huang, "Fast STA Graph Partitioning Framework for Multi-GPU Acceleration," *IEEE/ACM Design, Automation and Test in Europe Conference (DATE)*, Antwerp, Belgium, 2023
4. Tsung-Wei Huang and Leslie Hwang, "Task-Parallel Programming with Constrained Parallelism," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2022
5. Tsung-Wei Huang, "Enhancing the Performance Portability of Heterogeneous Circuit Analysis Programs," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2022

6. Dian-Lun Lin, Haoxing Ren, Yanqing Zhang, Brucek Khailany, and Tsung-Wei Huang, "From RTL to CUDA: A GPU Acceleration Flow for RTL Simulation with Batch Stimulus," *ACM International Conference on Parallel Processing (ICPP)*, Bordeaux, France, 2022
7. Cheng-Hsiang Chiu and Tsung-Wei Huang, "Composing Pipeline Parallelism using Control Taskflow Graph," *ACM International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, Minneapolis, Minnesota, 2022
8. Yu-Guan Chen, Chun-Yao Wang, Tsung-Wei Huang, and Takashi Sato, "Overview of 2022 CAD Contest at ICCAD," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, CA, 2022
9. Cheng-Hsiang Chiu and Tsung-Wei Huang, "Efficient Timing Propagation with Simultaneous Structural and Pipeline Parallelisms," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2022
10. Tsung-Wei Huang and Yibo Lin, "Concurrent CPU-GPU Task Programming using Modern C++," *International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS)*, France, 2022
11. Kexing Zhou, Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "Efficient Critical Paths Search Algorithm using Mergeable Heap," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Taiwan, 2022
12. Guannan Guo, Tsung-Wei Huang, and Martin Wong, "GPU-accelerated Path-based Timing Analysis," *ACM/IEEE Design Automation Conference (DAC)*, CA, 2021
13. Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "A Provably Good and Practically Efficient Common Path Pessimism Removal Algorithm for Large Designs," *ACM/IEEE Design Automation Conference (DAC)*, CA, 2021
14. McKay Mower, Luke Majors, and Tsung-Wei Huang, "Taskflow-San: Sanitizing Erroneous Control Flow in Taskflow Programs," *IEEE Workshop on Extreme Scale Programming Models and Middleware (ESPM2)*, St. Louis, Missouri, 2021
15. Tsung-Wei Huang, "TFProf: Profiling Large Taskflow Programs with Modern D3 and C++," *IEEE International Workshop on Programming and Performance Visualization Tools (ProTools)*, St. Louis, Missouri, 2021
16. Dian-Lun Lin and Tsung-Wei Huang, "Efficient GPU Computation using Task Graph Parallelism," *European Conference on Parallel and Distributed Computing (Euro-Par)*, Portugal, 2021
17. Yasin Zamani and Tsung-Wei Huang, "A High-Performance Heterogeneous Critical Path Analysis Framework," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2021
18. Cheng-Hsiang Chiu, Dian-Lun Lin and Tsung-Wei Huang, "An Experimental Study of SYCL Task Graph Parallelism for Large-Scale Machine Learning Workloads," *International Workshop of Asynchronous Many-Task Systems for Exascale (AMTE)*, 2021
19. Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "HeteroCPPR: Accelerating Common Path Pessimism Removal with Heterogeneous CPU-GPU Parallelism," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, Germany, 2021
20. Guannan Guo, Tsung-Wei Huang, Yibo Lin, and Martin D. F. Wong, "GPU-accelerated Critical Path Generation with Path Constraints," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, Germany, 2021
21. Tsung-Wei Huang, Yu-Guan Chen, Chun-Yao Wang, and Takashi Sato, "Overview of 2021 CAD Contest at ICCAD," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, Germany, 2021
22. Kuan-Ming Lai, Tsung-Wei Huang, Pei-Yu Lee, and Tsung-Yi Ho, "ATM: A High Accuracy Extracted Timing Model for Hierarchical Timing Analysis," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Tokyo, Japan, 2021
23. Chun-Xun Lin, Tsung-Wei Huang, and Martin D. F. Wong, "An Efficient Work-Stealing Scheduler for Task Dependency Graph," *IEEE International Conference on Parallel and Distributed Systems (ICPADS)*, Hong Kong, 2020

24. D.-L. Lin and Tsung-Wei Huang, "A Novel Inference Algorithm for Large Sparse Neural Network using Task Graph Parallelism," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2020 (**Sparse Neural Network Graph Challenge Champion Award**)
25. Zizheng Guo, Tsung-Wei Huang, and Yibo Lin, "GPU-Accelerated Static Timing Analysis," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020
26. Tsung-Wei Huang, "A General-purpose Parallel and Heterogeneous Task Programming System for VLSI CAD," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020
27. Ing-Chao Lin, Ulf Schlichtmann, Tsung-Wei Huang, and Pao-Hun Lin, "Overview of 2020 CAD Contest at ICCAD," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Diego, 2020
28. G. Guo, Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "An Efficient Critical Path Generation Algorithm Considering Extensive Path Constraints," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2020
29. Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo, and Martin D. F. Wong, "A Modern C++ Parallel Task Programming Library," *ACM Multimedia Conference (MM)*, Nice, France, 2019 (**Second Prize of Open-Source Software Competition**)
30. Chun-Xun Lin, Tsung-Wei Huang, Guannan Guo, and Martin D. F. Wong, "An Efficient and Composable Parallel Programming Library," *IEEE High-performance Extreme Computing (HPEC)*, Waltham, MA, 2019
31. Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, "Cpp-Taskflow: Fast Task-based Parallel Programming using Modern C++," *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, Rio De Janeiro, Brazil, 2019
32. Kuan-Ming Lai, Tsung-Wei Huang, and Tsung-Yi Ho, "A General Cache Framework for Efficient Generation of Timing Critical Paths," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019
33. Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, "Essential Building Blocks for Creating an Open-source EDA Project," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019
34. Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "Distributed Timing Analysis at Scale," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, 2019
35. Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, and Martin D. F. Wong, "A General-purpose Distributed Programming Systems using Data-parallel Streams," *ACM Multimedia Conference (MM)*, Seoul, Korea, 2018 (**Best Open-Source Software Award**)
36. Chun-Xun Lin, Tsung-Wei Huang, G. Guo, and Martin D. F. Wong, "MtDetector: A High-performance Marine Traffic Detector at Stream Scale," *ACM Distributed Event-based System Conference (DEBS)*, Hamilton, New Zealand, 2018
37. Chun-Xun Lin, Tsung-Wei Huang, T. Yu, and Martin D. F. Wong, "A Distributed Power Grid Analysis Framework from Sequential Stream Graph," *ACM Great Lakes Symposium (GLSVLSI)*, Chicago, IL, 2018
38. Chun-Xun Lin, Tsung-Wei Huang, and Martin D. F. Wong, "Routing at Compile Time," *IEEE International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, 2018
39. Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "DtCraft: A Distributed Execution Engine for Compute-intensive Applications," *ACM/IEEE International Conference on Computer-aided Design (ICCAD)*, Irvine, CA, 2017
40. Tin-Yin Lai, Tsung-Wei Huang, and Martin D. F. Wong, "An Effective and Accurate Macro-modeling Algorithm for Large Hierarchical Designs," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, 2017 (First Place of TAU Timing Analysis Contest)
41. Tsung-Wei Huang, Martin D. F. Wong, D. Sinha, K. Kalafala, and N. Venkateswaran, "A Distributed Timing Analysis Framework for Large Designs," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, 2016
42. Tsung-Wei Huang and Martin D. F. Wong, "OpenTimer: A High-performance Timing Analysis Tool," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, TX, 2015 (Second Place of TAU Timing Analysis Contest)

43. Tsung-Wei Huang and Martin D. F. Wong, "On Fast Timing Closure: Speeding Up Incremental Path-Based Timing Analysis with MapReduce," *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, CA, 2015
44. Tsung-Wei Huang and Martin D. F. Wong, "Accelerated Path-Based Timing Analysis with MapReduce," *ACM International Symposium on Physical Design (ISPD)*, Monterey, CA, 2015
45. Tsung-Wei Huang, P-C. Wu, and Martin D. F. Wong, "Fast Path-Based Timing Analysis for CPPR," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2014 (First Place of TAU Timing Analysis Contest)
46. Tsung-Wei Huang, P.-C. Wu, and Martin D. F. Wong, "UI-Timer: An Ultra-Fast Clock Network Pessimism Removal Algorithm," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2014
47. Tsung-Wei Huang, P.-C. Wu, and Martin D. F. Wong, "UI-Route: An Ultra-Fast Incremental Maze Routing Algorithm," *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, San Francisco, CA, 2014
48. S.-H. Yeh, J.-W. Chang, Tsung-Wei Huang, and Tsung-Yi Ho, "Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2012
49. Tsung-Wei Huang, J.-W. Chang, and Tsung-Yi Ho, "Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips," *ACM International Symposium on Physical Design (ISPD)*, Napa, CA, 2012
50. J.-W. Chang, Tsung-Wei Huang, and Tsung-Yi Ho, "An ILP-based Obstacle-Avoiding Routing Algorithm for Pin-Constrained EWOD Chips," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Sydney, Australia, 2012
51. Tsung-Wei Huang, Tsung-Yi Ho, and K. Chakrabarty, "Reliability-Oriented Broadcast Electrode-Addressing for Pin-Constrained Digital Microfluidic Biochips," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, San Jose, CA, 2011
52. Tsung-Wei Huang, Yan-You Lin, J.-W. Chang, and Tsung-Yi Ho, "Recent Research and Emerging Challenges in the Designs and Optimizations for Digital Microfluidic Biochips," *IEEE System on Chip Conference (SOCC)*, 2011.
53. Tsung-Wei Huang, Yan-You Lin, J.-W. Chang, and Tsung-Yi Ho, "Chip-Level Design and Optimization for Digital Microfluidic Biochips," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011.
54. P.-H. Yuh, C. C.-Y. Lin, Tsung-Wei Huang, Tsung-Yi Ho, C.-L. Yang, and Y.-W. Chang, "A SAT-Based Routing Algorithm for Cross-Referencing Biochips," *IEEE/ACM International Workshop on System-level Interconnect Prediction (SLIP)*, San Diego, CA, June 2011.
55. Tsung-Wei Huang, H.-Y. Su, and Tsung-Yi Ho, "Progressive Network-Flow Based Broadcast Addressing for Pin-Constrained Digital Microfluidic Biochips," *ACM/IEEE Design Automation Conference (DAC)*, pp. 741—746, San Diego, CA, June 2011.
56. Tsung-Wei Huang, S.-Y. Yeh, and Tsung-Yi Ho, "A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast Electrode-Addressing EWOD Chips," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, pp. 425-431, San Jose, CA, 2010.
57. Tsung-Wei Huang and Tsung-Yi Ho, "A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips," *ACM International Symposium on Physical Design (ISPD)*, pp. 201—208, San Francisco, CA, 2010.
58. Tsung-Wei Huang, C.-H. Lin, and Tsung-Yi Ho, "A Contamination-Aware Droplet Routing Algorithm for Digital Microfluidic Biochips," *IEEE/ACM International Conference on Computer-aided Design (ICCAD)*, pp. 151—156, San Jose, CA, 2009.
59. Tsung-Wei Huang and Tsung-Yi Ho, "A Fast Routability- and Performance-Driven Droplet Routing Algorithm for Digital Microfluidic Biochips," *IEEE International Conference on Computer Design (ICCD)*, pp. 445—450, Lake Tahoe, CA, 2009

Journal Publication

1. Dian-Lun Lin and Tsung-Wei Huang, "Accelerating Large Sparse Neural Network Inference using GPU Task Graph Parallelism," *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 33, no. 11, pp. 3041—3052, Nov 2022
2. Tsung-Wei Huang, Dian-Lun Lin, Chun-Xun Lin, and Yibo Lin, "Taskflow: A Lightweight Parallel and Heterogeneous Task Graph Computing System," *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 33, no. 6, pp. 1303—1320, June 2022
3. Zizheng Guo, Mingwei Yang, Tsung-Wei Huang, and Yibo Lin, "A Provably Good and Practically Efficient Algorithm for Common Path Pessimism Removal in Large Designs," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 10, pp. 3466—3478, Oct. 2022
4. Jia-Ruei Yu, Chun-Hsien Chen, Tsung-Wei Huang, Jang-Jih Lu, Chia-Ru Chung, Ting-Wei Lin, Min-Hsien Wu, Yi-Ju Tseng, Hsin-Yao Wang, "Energy Efficiency of Inference Algorithms for Medical Datasets: A Green AI study," *Journal of Medical Internet Research (JMIR)*, to appear in 2022
5. Tsung-Wei Huang, Dian-Lun Lin, Yibo Lin, and Chun-Xun Lin, "Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 5, pp. 1448—1452, May 2022
6. Tsung-Wei Huang, Chun-Xun Lin, and Martin. D. F. Wong, "OpenTimer v2: A Parallel Incremental Timing Analysis Engine," *IEEE Design and Test (DAT)*, vol. 38, no. 2, pp. 62—68, April 2021
7. Tsung-Wei Huang, Yibo Lin, Chun-Xun Lin, G. Guo, and Martin. D. F. Wong, "Cpp-Taskflow: A General-purpose Parallel Task Programming System at Scale," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 8, pp. 1687—1700, Aug. 2021
8. Tsung-Wei Huang, G. Guo, Chun-Xun Lin, and Martin. D. F. Wong, "OpenTimer v2: A New Parallel Incremental Timing Analysis Engine," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 4, pp. 776—789, April, 2021
9. Tsung-Wei Huang, Chun-Xun Lin, and Martin D. F. Wong, "DtCraft: A High-performance Distributed Execution Engine at Scale," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 6, pp. 1070—1083, June 2018
10. Tsung-Wei Huang and Martin D. F. Wong, "UI-Timer 1.0: An Ultra-Fast Path-Based Timing Analysis Algorithm for CPPR," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 11, pp. 1862—1875, Nov. 2016
11. S.-H. Yeh, J.-W. Chang, Tsung-Wei Huang, S.-T. Yu, and Tsung-Yi Ho, "Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no.9, pp. 1302—1315, Sep. 2014.
12. J.-W. Chen, C.-L. Hsu, L.-C. Tsai, Tsung-Wei Huang, and Tsung-Yi Ho, "An ILP-Based Routing Algorithm for Pin-Constrained EWOD Chips with Obstacle Avoidance," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no.11, pp. 1655—1667, Nov. 2013.
13. Y.-H. Chen, C.-L. Hus, Tsung-Wei Huang, and Tsung-Yi Ho, "A Reliability-Oriented Placement Algorithm for Reconfigurable Digital Microfluidic Biochips using 3D Deferred Decision-Making Technique," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 8, pp. 1151—1162, Aug. 2013.
14. J.-W. Chang, S.-H. Yeh, Tsung-Wei Huang, and Tsung-Yi Ho, "Integrated Fluidic-Chip Co-Design Methodology for Digital Microfluidic Biochips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no 2, pp. 216—227, Feb. 2013.
15. Tsung-Wei Huang, S.-Y. Yeh, and Tsung-Yi Ho, "A Network-Flow Based Pin-Count Aware Routing Algorithm for Broadcast-Addressing EWOD Chips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 12, pp. 1786—1799, Dec. 2011.
16. Tsung-Wei Huang and Tsung-Yi Ho, "A Two-Stage Integer-Linear-Programming Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 2, pp. 215—228, Feb. 2011.

17. Tsung-Wei Huang, C.-H. Lin, and Tsung-Yi Ho, "A Contamination-Aware Droplet Routing Algorithm for the Synthesis of Digital Microfluidic Biochips," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 29, no. 11, pp. 1682—1695, Nov. 2010.

PATENT

Incremental Common Path Pessimism Analysis USA-14/946043
Tsung-Wei Huang, K. Kalafala, D. Sinha, and N. Venkateswaran

Distributed Timing Analysis of a Partitioned Integrated Circuit Design USA-9916405B2
Tsung-Wei Huang, K. Kalafala, D. Sinha, and N. Venkateswaran

TALK

1. "Intelligent Heterogeneous Parallelism," ACCESS-CEDA Seminar Series at Hong Kong, Sep 2022
2. "Intelligent Heterogeneous Parallelism," CS Department, University of California at Merced, Sep 2022
3. "Programming System for Building High-performance CAD Applications," X Factory, Sep 2022
4. "A General-purpose Parallel and Heterogeneous Task Programming System," Xilinx, Aug 2022
5. "A GPU Acceleration Flow for RTL Simulation with Batch Stimulus," Invited Talk, IWLS, July 2022
6. "Intelligent Heterogeneous Computing," AMD Research, June 2022
7. "Intelligent Heterogeneous Computing," ECE Department, Johns Hopkins University, March 2022
8. "Intelligent Heterogeneous Computing," ECE Department, Stevens Institute of Technology, 2022
9. "Intelligent Heterogeneous Computing," ECE Department, University of Minnesota, Feb 2022
10. "Taskflow: A General-purpose Heterogeneous Task Programming System," IXPUG, 2021
11. "cudaFlow: A Modern C++ Programming Model for GPU Task Graph Parallelism," CppCon, 2021
12. "Taskflow: A General-purpose Heterogeneous Task Computing System," CUHK, Aug 2021
13. "HeteroTime: Accelerating Static Timing Analysis with GPUs," Nvidia Research, June 2021
14. "Taskflow: A Lightweight Heterogeneous Task Programming System," CPPNow, 2021
15. "GPU-Accelerated Static Timing Analysis and Beyond," GTC, April 2021
16. "Machine Learning-enabled System for EDA," VLSI-DAT, April 2021
17. "GPU-Accelerated Static Timing Analysis," UCSC EDA Seminar, Feb 2021
18. "A General-purpose Heterogeneous Task Programming System," CIE/USA-GNYC, Oct 2020
19. "Taskflow: Parallel and Heterogeneous Task Programming in C++," C++ Meetup, Oct 2020
20. "Taskflow: A General-purpose Heterogeneous Task Programming System," CppIndia, Oct 2020
21. "Taskflow: A General-purpose Heterogeneous Task Programming System," MUC++, Oct 2020
22. "Programming Systems for Parallelizing VLSI CAD and Beyond," VLSI-DAT, April 2020
23. "A General-purpose Heterogeneous Task Programming System at Scale," ORNL, March 2020
24. "Growing Your Open-Source Projects," WOSET at IEEE/ACM ICCAD, November 2019
25. "Essential Building Blocks for Creating an Open-source EDA Project," IEEE/ACM DAC, June 2019
26. "Task-based Parallel Programming using Modern C++", CSL Social Hour, Sep 2018
27. "Distributed Timing Analysis in 100 Lines of Code," VSD webinar, May 2018
28. "DtCraft: A High-performance Distributed Execution Engine at Scale," CSLSC, UIUC, 2018
29. "OpenTimer: An open-source high-performance timing analysis tool," ORCONF, Italy, 2016
30. "Distributed Timing Analysis: Framework and Systems," Cadence, Austin, June 2016
31. "OpenTimer: A High-performance Timing Analysis Tool," Invited Talk, ICCAD, 2015
32. "Fast Path-based Timing Analysis," Invited Talk, ICCAD, 2014

Work Experience

Software Engineer May 2017 – Aug 2017
High-performance Computing Group, Citadel, Chicago, IL

Software Engineer May 2015 – Aug 2015
Timing Analysis Group, IBM, NY

Software Engineer May 2014 – Aug 2014
Timing Analysis Group, Mentor Graphics, Fremont, CA

Service

Chair/Co-chair, ICCAD CAD Contests 2020 – 2023
Organized contests to engage students in solvoing cutting-edge CAD problems

Publicity Chair, IWLS 2020
Promoted participation in International Workshop on Logic Synthesis

Chair/Co-chair, ACM SIGDA CADathlon International Programming Contest 2018 – 2021
Organized real-time contests to engage students in solvoing fundamental CAD problems

Co-chair, ACM TAU Timing Analysis Contest 2018
Organized contests to engage students in solving timing-related problems

Chair, VSD Open Online EDA Conference 2018
Organized the first online EDA conference with VSD at India

Program Committee
Selected top-quality papers to organize conference programs

- ACM/IEEE Design Automation Conference (DAC), 2022–2023
- ACM TAU, 2020–2021
- IEEE/ACM International Conference on Computer-aided Design (ICCAD), 2019–2022
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2020–2021
- IEEE International Conference on Computer Design (ICCD), 2020–2021
- C++ Conference (CppCon), 2019–2021

Editorship
Managed peer-review processes and recommended what gets published

- Guest editor, Special Issue of VLSI Integration, 2022

Journal Reviewers
Evaluated submitted papers and recommended acceptance/rejection

- IEEE Transactions on Parallel and Distributed Computing Systems (TPDS)
- IEEE Transactions on Computer-aided Design for Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large-scale Integration (TVLSI)
- IEEE Transactions on Circuits and Systems (TCAS)
- IEEE Transactions on Big Data (TBD)
- ACM Transaction son Design Automation of Electronic Systems (TODAES)
- VLSI Integration Journal

Departmental Committee at the University of Utah 2019 – Now
Helped the ECE department enhance various research and teaching programs

- Graduate Student and Admission Committee, 2021—-Now
- University of Utah Asia Campus Committee, 2021—-Now
- University of Utah Asia Campus Students Summer Visit Program, 2021
- University of Utah Asia Campus faculty recruiting committee, 2021—-Now
- Artificial Intelligence and Data-science faculty recruiting committee, 2020