Fig. 1: Buck converter and its informal description.

Fig. 2: STG specification of a simple buck converter.

Fig. 3: Deconstructing the STG of the ZC absent scenario.

Fig. 4: Example system specified using concepts.

Fig. 5: STG for the example system.

Fig. 6: The first step: create consistency loops.

Fig. 7: The second step: add causality concept $a^+ \rightsquigarrow c^+$.

Fig. 8: Finish the second step: add all causality concepts.

Fig. 9: The final step: set the initial state.

Fig. 10: Partial translation of concepts into STGs

Fig. 11: Stages of the design flow when using asynchronous concepts in Workcraft.

Fig. 12: STG for the zcAbsentScenario concept.

Fig. 13: STG for the zcLateScenario concept.

Fig. 14: STG for the zcEarlyScenario concept.

Fig. 15: Complete STG for a buck converter.

Fig. 16: Custom verification of no shortcircuit.

Fig. 17: Complex gate implementation.

Fig. 18: Technology mapped implementation.

Fig. 19: Technology mapping into 2-input gates/latches.

TABLE I: A comparison of features of related work and the proposed method