1 Abstract

L1Topo is a new L1 Trigger subsystem consisting of a single ATCA crate initially equipped with two (max three) ATCA modules. L1Topo register definition is here defined. U. Schaefer, J. Schaffer, M. Simon, S. Artz, M. Palka, G. Korcyl, C. Kahra, and E. Simioni etc....

2 L1Topo Register Map

The register map is identical for all L1Topo modules with their firmware variants. It contains addresses managed by IPbus link with address space per FPGAs.

address(hex)	FPGA	Function
0x00000000	Processor_U3	Control
0x80000000	Processor_U1	Topo Algorithms processor
0xC0000000	Processor_U2	Topo Algorithms processor

Table 1: FPGAs addresses

In this document the definition of the registers address follow the hierarchy in Tab.1. Sect.3 describes the registers definition for the Control FPGA. Sect.4 and **??** describes the registers definition for the algorithms processors FPGA. Sub-spaces are further defined.
The definiton of registers follow the L1Calo guidelines.

3 Control FPGA Programming Model

Offset (hex)	Type	Name	Size(bytes)	Comments
0x00000001	R	Firmware_Version	4	
0x00000002	R	General_Status	4	
0x00000004	RW	General_Control	4	
0x00000008	RW	TTC_Forwarding_Control	4	
0x00000010	RW	I2C_Data_Out	4	
0x00000011	R	I2C_Error	4	
0x00000012	RW	I2C_Address	4	
0x00000013	RW	I2C_WriteEnable	4	
0x00000014	RW	I2C_Pointer	4	
0x00000015	RW	I2C_Data_In	4	
0x00000016	RW	I2C_Bus_Select	4	
0x00000020	R	SGMII_Phy_Error_Counter	4	
0x00000021	R	Ethernet_MAC_Error_Counter	4	
0x00000022	R	CTRL_BUS_U1_ErrorCounter	4	
0x00000023	R	CTRL_BUS_U2_Error_Counter	4	
0x00000024	R	I2C_Error_Counter	4	
0x00000100	RW	ROD_Infrastructure	128	sub-space offset
0x00001000	RW	Test_RAM	1024	sub-space offset

Table 2: Control FPGA addresses offsets

3.1 Firmware Version

bit	Function
0-2	FW version
2-31	Unused

Table 3: Firmware Version

3.2 General_Control

General control register of the ControlFPGA.

bit	Function
0-5	??
5-31	Unused

Table 4: Firmware Version

- **Bit 0**: ...
- **Bit 1-2**: ...
- **Bit 2-32**: unused

3.3 SGMII_Phy_Error_Counter

ErrorCounter for the SGMII Phy (errors in the 8b10b encoded data).

bit	Function
0-7	SGMII error counter
8-15	MAC error counter
16-32	unused

Table 5: Firmware Version

- **Bit 0**:...

3.4 TTC_Forwarding_Control

Control register for the TTC forwarding.

3.5 I2C

The various I2C registers are here described.

3.6 Ethernet_MAC_Error_Counter

ErrorCounter for the Ethernet MAC (unsuccessful frame reception -¿ assertion of the rx_axis_mac_tuser signal). Errors in the SGMII Phy will also lead to errors in the MAC.

3.7 CTRL_BUS_U1_ErrorCounter

ErrorCounter for the incoming IPbus lines from the U1 processor (errors in the 8b10b encoded data).

3.8 CTRL_BUS_U2_Error_Counter

3.9 ROD_Infrastructure

Offset (hex)	Type	Register Name	Size(bytes)
0x00000000	RW	Ov_Busy	4
0x00000001	RW	Gen_L1A	4
0x00000002	RW	Run_Type_Nbr	4
0x00000003	RW	Trg_Type	4
0x00000004	RW	Level1ID_Gen	4
0x00000005	W	Run_Reset	4
0x00000006	R	ROD_Sys_Fw_Ver	4
0x00000007-0A	R	Run_Gen_Dbg	16
0x0000000A-0F	RW	Run_Reserved	unused

Table 6: ROD control and status registers for Run Control

Offset (hex)	Type	Register Name	Size(bytes)
0x00000010	W	ROD_Reset	4
0x00000011-12	RW	Fifo_Thr	8
0x00000013	RW	Busy_Idle_Fr_Conf	4
0x00000014-18	RW	Hist_Conf	20
0x00000019-02D	R	Err_Ctr	16
0x0000002E-031	R	ROD_Gen_Dbg	16
0x00000032	R	Busy_Idle_Fr	4
0x00000033-034	R	ROD_Hist	8
0x00000035-03E	R	ROD_Fifo_Stat	40
0x0000003F	RW	ROD_Reserved	unused

Table 7: ROD control and status registers for ROD Control

Offset (hex)	Type	Register Name	Size(bytes)
0x00000040	W	Link_Reset	4
0x00000041	RW	Link_Enable	4
0x00000042-43	RW	IDelays	8
0x00000044	R	Syn_Status	4
0x00000045-4D	R	Byte_Ctr	32
0x0000004E-056	R	Err_Ctr	32
0x00000057-5B	R	DDR_Gen_Dbg	16
0x0000005B-5F	RW	DDR_Reserved	unused

Table 8: ROD control and status registers for DDR-GTX Control

Offset (hex)	Type	Register Name	Size(bytes)
0x00000030	W	Slink_Reset	4
0x00000031	RW	Slink_Enable	4
0x00000032	RW	Format_ROS_Ver	4
0x00000033	RW	Format_ROIB_Ver	4
0x00000034	RW	SubDet_Module_ID	4
0x00000035	RW	Busy_Idle_Fr_Conf	4
0x00000036	R	Slink_Status	4
0x00000037-38	R	Busy_Idle_Fr	4
0x00000038-3F	RW	Slink_Reserved	unused

Table 9: ROD control and status registers for S-Link

3.9.1 Ov_Busy

bit	**Function**
0-2	??
3-16	??
17-31	unused

- DIAGNOSTICS REGISTER: Enables overwriting existing BUSY status in certain places of the system.

3.9.2 Gen_L1A

bit	Function
0	Enable internal L1A generation
1	0 - random, 1 - fixed frequency
2-3	unused
4-31	frequency (at sysclk counts)

- DIAGNOSTICS REGISTER: Enables the internal L1A signal generation at a given frequency

3.9.3 Run_Type_Nbr

bit	Function
0-23	Run Number
24-31	Run Type

- Sets the Run Number and Run Type fields for Slink packet headers

3.9.4 Trg_Type

bit	Function
0	0 - Trigger Type from TTC, 1 - Trigger Type from IPBus
1-7	Reserved
8-15	Trigger Type value

- Enables the trigger type to be provided via slow control with a given value

3.9.5 Level1ID_Gen

bit	Function
0	0 - L1AID from TTC, 1 - L1AID from internal counter
1	0 - Fixed internal value, 1 - Incremented
2-7	Reserved
8-31	L1AID initial value for internal counting

- Enables the trigger type to be provided via slow control with a given value

3.9.6 Run_Reset

bit	Function
0	Reset Pulse
1-31	Reserved

- Resets all the ROD infrastructure components (ROD, DDRs, Slink)

3.9.7 ROD_Sys_Fw_Ver

bit	Function
0-31	Firmware version number

- Firmware version number for the ROD infrastructure

3.9.8 Run_Gen_Dbg

bit	Function
0-31	Debug word 0
32-63	Debug word 1
64-95	Debug word 2
96-127	Debug word 3

- DIAGNOSTICS REGISTER: General debugging words for the ROD infrastructure

3.9.9 ROD_Reset

bit	Function
0	Resets the ROD control, cleans all internal buffers.
1-31	Reserved

Table 10: Resets only ROD part.

3.9.10 Fifo_Thr

bit	Function
0-15	fill level of internal data buffers, above which busy is sent
16-31	ammount of L1A in queue awaiting for processing above which busy is sent
63-32	reserved

Table 11: Busy conditioning based on FIFO fill levels.

3.9.11 Busy_Idle_Fr_Conf

bit	Function
0-31	time in which a percentage of ROD busy is calculated - value mltiplied by 25ns

Table 12: Control of fraction register

3.9.12 Hist_Conf

bit	Function
0-7	multiplexer for 1st histogram (TBD)
8-15	multiplexer for 2nd histogram
16-23	multiplexer for 3rd histogram
24-31	multiplexer for 4th histogram
32-47	time when one bin of histogram is accumulated (1st) - value*25ns
48-63	time when one bin of histogram is accumulated (2nd) - value*25ns
64-79	time when one bin of histogram is accumulated (3rd) - value*25ns
80-95	time when one bin of histogram is accumulated (4th) - value*25ns
96-111	threshold above which value of current bin of histogram is increased (1st)
112-127	threshold above which value of current bin of histogram is increased (2nd)
128-143	threshold above which value of current bin of histogram is increased (3rd)
144-160	threshold above which value of current bin of histogram is increased (4th)

Table 13: Histogramming of incoming data - configurable real time statistics. For example TOB number in function of time.

3.9.13 Err_Ctr

bit	Function
0-7	CRC error cntr for input 0
8-15	CRC error cntr for input 1
...	...
632-639	CRC error cntr for input 79

Table 14: CRC error couters.

3.9.14 ROD_Gen_Dbg

bit	Function
0-127	TBD

Table 15: Internal state machines, statistics, debug information.

3.9.15 Busy_Idle_Fr

bit	Function
0-31	time when ROD busy was set (value * 25ns)

Table 16: Shows busy time fraction, can be used together with s-link busy for debug or dignostics.

3.9.16 ROD_Hist

bit	Function
0-15	data read out from 1st histogram, 512 bins
16-31	data read out from 2nd histogram, 512 bins
32-47	data read out from 3rd histogram, 512 bins
48-63	data read out from 4th histogram, 512 bins

Table 17: Histogrammed data - when reading this address user reads out histogram saved in FIFO. Only when all data is read out (16^2 32bit data words) next histogram will be created.

3.9.17 ROD_Fifo_Stat

bit	Function
0-1	link 0 FIFO empty(0), full(1)
2-3	link 1 FIFO empty(2), full(3)
...	...
178-179	link 79 FIFO empty(178), full(179)
180-188	L1A FIFO level

Table 18: Empty and Full for link fifos and l1A FIFO fill level.

3.9.18 Link_Reset

bit	Function
0	ROD DDR Reset Pulse
1-31	Reserved

- Resets the ROD DDR links

3.9.19 Link_Enable

bit	Function
0	DDR Link 0
1	DDR Link 1
2	DDR Link 2
3	DDR Link 3
4	DDR Link 4
5	DDR Link 5
6	DDR Link 6
7	DDR Link 7
8	DDR Link 8
9	DDR Link 9
10	DDR Link 10
11	DDR Link 11
12	DDR Link 12
13-31	Reserved

- Enables or disables a given ROD DDR Link (0 - disable, 1 - enable)

3.9.20 IDelays

bit	Function
0-4	Delay value for Link 0
5-9	Delay value for Link 1
10-14	Delay value for Link 2
15-19	Delay value for Link 3
20-24	Delay value for Link 4
25-29	Delay value for Link 5
30-34	Delay value for Link 6
35-39	Delay value for Link 7
40-44	Delay value for Link 8
45-49	Delay value for Link 9
50-54	Delay value for Link 10
55-59	Delay value for Link 11
60-64	Delay value for Link 12
65-95	Reserved

- DIAGNOSTICS REGISTER: IDelay values for individual ROD DDR links

3.9.21 Syn_Status

bit	Function
0	Synchronization status for Link 0
1	Synchronization status for Link 1
2	Synchronization status for Link 2
3	Synchronization status for Link 3
4	Synchronization status for Link 4
5	Synchronization status for Link 5
6	Synchronization status for Link 6
7	Synchronization status for Link 7
8	Synchronization status for Link 8
9	Synchronization status for Link 9
10	Synchronization status for Link 10
11	Synchronization status for Link 11
12	Synchronization status for Link 12
13-31	Reserved

- DIAGNOSTICS REGISTER: Synchronization status for individual ROD DDR links

3.9.22 Byte_Ctr

bit	Function
0-15	Bytes counter for Link 0
15-31	Bytes counter for Link 1
32-47	Bytes counter for Link 2
48-63	Bytes counter for Link 3
64-79	Bytes counter for Link 4
80-95	Bytes counter for Link 5
96-111	Bytes counter for Link 6
112-123	Bytes counter for Link 7

- DIAGNOSTICS REGISTER: Transmitted bytes counters for individual ROD DDR links

3.9.23 Err_Ctr

bit	Function
0-15	Error counter for Link 0
15-31	Error counter for Link 1
32-47	Error counter for Link 2
48-63	Error counter for Link 3
64-79	Error counter for Link 4
80-95	Error counter for Link 5
96-111	Error counter for Link 6
112-123	Error counter for Link 7

- Invalid characters received counters for individual ROD DDR links

3.9.24 DDR_Gen_Dbg

bit	Function
0-31	Debug word 0
32-63	Debug word 1
64-95	Debug word 2
96-127	Debug word 3

- DIAGNOSTICS REGISTER: General debugging words for the ROD DDR

3.9.25 Slink_Reset

bit	Function
0	Slink to ROS Reset Pulse
1	Slink to ROIB Reset Pulse
2-31	Reserved

- Resets the individual Slink connections

3.9.26 Slink_Enable

bit	Function
0	Slink to ROS Enable
1	Slink to ROIB Enable
2-31	Reserved

- Enables or disables a given SLink connection (0 - disable, 1 - enable)

3.9.27 Format_ROS_Ver

bit	Function
0-15	Minor Format Version
16-31	Major Format Version

- Sets the format versions for the SLink connection to ROS

3.9.28 Format_ROIB_Ver

bit	Function
0-15	Minor Format Version
16-31	Major Format Version

- Sets the format versions for the SLink connection to ROIB

3.9.29 SubDet_Module_ID

bit	Function
0-7	Subdetector ID
8-15	Reserved
16-31	Module ID

- Sets the Subdetector ID and Module ID for the SLink connections

3.9.30 Busy_Idle_Fr_Conf

bit	Function
0-31	Time period

- DIAGNOSTICS REGISTER: Sets the time period for the calculation of Busy and Idle fractions of Slink connections (at sysclk ticks)

3.9.31 Slink_Status

bit	Function
0	ROS Slink down
1	ROS Slink fifo full
2	ROS Slink link present
3	Reserved
4	ROIB Slink down
5	ROIB Slink fifo full
6	ROIB Slink link present
7-31	Reserved

- Shows the status of the Slink connections to the subsystems

3.9.32 Busy_Idle_Fr

bit	Function
0-31	ROS Slink Busy time Fraction
32-63	ROIB Slink Busy time Fraction

- DIAGNOSTICS REGISTER: Shows the activity fraction of the Slink connections to the subsystems

3.10 ROD_Processor_Infrastructure

Offset (hex)	Type	Register Name	Size(bytes)
0x00000000	RW	Ov_Busy	4
0x00000001	RW	ROD_Fw_Ver	4
0x00000002-03	RW	ROD_Dbg	8
0x00000004-0F	RW	Run_Reserved	unused

Table 19: ROD control and status registers for Run Control

Offset (hex)	Type	Register Name	Size(bytes)
0x00000000	W	ROD_Reset	4
0x00000001-0A	RW	ROD_Slices	40
0x0000000B-14	RW	ROD_Offsets	40
0x000000015	RW	ROD_L1A_Offset	4
0x000000016	R	ROD_L1A_Fill	4
0x000000017-18	RW	ROD_Dbg	8

Table 20: ROD control and status registers for ROD Control

3.10.1 ROD_Reset

bit	Function
0	Reset ROD logic and clean buffers
1-31	Reserved
...	...
178-179	link 79 FIFO empty(178), full(179)
180-188	L1A FIFO level

Table 21: Bit 0 of this register is resets ROD logic on processor side (pulse).

3.10.2 ROD_Slices

bit	Function
0-2	Number of slices accepted after L1A for link 0
3-5	Number of slices accepted after L1A for link 1
...	...
237-239	Number of slices accepted after L1A for link 79

Table 22: Individually for each input channel it is possible to choose amount of censequtive accepted time slices (max 7, 0 switches off the channel).

3.10.3 ROD_Offsets

bit	Function
0-2	Number of time offset (BC) in relation to L1A starting from which data is taken for link 0
3-5	Number of time offset (BC) in relation to L1A starting from which data is taken for link 1
...	...
237-239	Number of time offset (BC) in relation to L1A starting from which data is taken for link 79

Table 23: It enables takes data from previous bunch crossings in relation to L1A.

3.10.4 ROD_L1A_Offset

bit	Function
0-7	Offset of L1A comming from TTCrx to take corresponding BC data (value * BC)
8-31	reserved

Table 24: It allows to set addresses of ring memories in a way that corresponding BC is taken (when offset for individual chanel is zero).

3.10.5 ROD_L1A_Fill

bit	Function
0-7	amount of L1A awaiting for transport
8-31	reserved

Table 25: Fill level of L1A FIFO.

3.10.6 ROD_Dbg

bit	Function
0-63	TBD

Table 26: State machines, internal signals - debug purposes.

3.11 I2C_Error_Counter

ErrorCounter for the I2C bus.

3.12 Test_RAM: Test RAM

4 Processor U1 Programming Model

Register Name	Register sub-address
CtrlbusErrorCounter	0x0001
TestRAM	0x1000 size=0x400
PlaybackSpyControl	0x0010
PlaybackCharIsKFakingMGTs	0x0011
PlaybackSpyDataOfMGTs	0x80000 size=20000
SpyCharIsKFromMGTs	0x012
PlaybackSpyDataOfDeserialisers	0xA0000 size=20000
PlaybackSpyDataOfAlgoResults	0x400″ size=400
QuadControl	0x0020 size=0x20
ChannelControl	0x0080 size=0x80
ChannelStatus	0x0100 size=0x80
DataDelay	0x0180 size=0x80
CRCErrorCounter	0x0200 size=0x80
FPGA_T	xxxxxxxxx

Table 27: Relative processors sub-addresses for Algorithms

4.1 CtrlbusErrorCounter

Error counter of the IPbus controller-processor connection

4.2 TestRAM

4.3 PlaybackSpyControl

Playback and spy control.

4.4 PlaybackCharIsKFakingMGTs

CharIsK data (4bit) to use while IPbus write-transactions on the PlaybackSpyDataOfMGTs.

bit	R/W	Function	Comments
0	R/W	CharIsK bit 1	
1	R/W	CharIsK bit 2	
2	R/W	CharIsK bit 3	
3	R/W	CharIsK bit 4	
4	R/W		
5-32	R/W	Reserved	Reserved

Table 28: XXX

4.5 PlaybackSpyDataOfMGTs

Data to playback or spied data of the MGTs. address bits[16:10] select the MGT, [9:0] select the block-ram address ([9:2] select out of the 256 128bit datawords, [1:0] the 128bit dataword in 32bit units (MSB downto LSB)).

bit	R/W	Function	Comments
0-1	R/W	select the blockram address	[1:0] the 128bit dataword in 32bit units (MSB downto LSB)
2-9	R/W	select the blockram address	[9:2] select out of the 256 128bit datawords
10-32	R/W	Reserved	Reserved

Table 29: XXX

4.6 SpyCharIsKFromMGTs

CharIsK data (4bit) spied while the last read transaction on the PlaybackSpyDataOfMGTs.

4.7 PlaybackSpyDataOfDeserialisers

Data to playback or spied data of the deserialiseres. address bits[16:10] select the deserialiser channel, [9:0] select the blockram address ([9:2] select out of the 256 128bit datawords, [1:0] the 128bit dataword in 32bit units (MSB downto LSB)).

4.8 PlaybackSpyDataOfAlgoResults

Data to playback or spied data of the L1Topo-Algorithms. address bits[9:0] select the 32bit dataword.

4.9 QuadControl

Control registers of the MGT-Quads.

4.10 ChannelControl

Control registers of the MGT-Channels.

4.11 ChannelStatus

Status registers of the MGT-Channels.

4.12 DataDelay

DataDelay (2bit) controls the shift registers for the received data. Data will be delayed by 2**DataDelay bunch ticks.

4.13 CRCErrorCounter

Error counter of the CRC check of the received data.

Register Name	Register Address
ClusterSortEM_minEt	0x20000000
ClusterSortEM_isoMask	0x20000001
ClusterSortEM_minEta	0x20000002
ClusterSortEM_maxEta	0x20000003
ClusterSortTau_minEt	0x20000004
ClusterSortTau_isoMask	0x20000005
ClusterSortTau_minEta	0x20000006
ClusterSortTau_maxEta	0x20000007
JetSortAll_minEt	0x20000008
JetSortAll_minEta	0x20000009
JetSortAll_maxEta	0x2000000a
EtCut_J25_minEt	0x2000000b
DeltaPhiIncl1_JJ16_minEt	0x2000000c
DeltaPhiIncl1_JJ16_minPhi	0x2000000d
DeltaPhiIncl1_JJ16_maxPhi	0x2000000e
DeltaEtaIncl1_JJ10_minEt	0x2000000f
DeltaEtaIncl1_JJ10_minPhi	0x20000010
DeltaEtaIncl1_JJ10_maxPhi	0x20000011
JetHT_HT200_minEt	0x20000012
JetHT_HT200_minEta	0x20000013
JetHT_HT200_maxEta	0x20000014
JetHT_HT200_minSum	0x20000015
EtCut_EM25_minEt	0x20000016
DeltaPhiIncl1_EMEM16_minEt	0x20000017
DeltaPhiIncl1_EMEM16_minPhi	0x20000018
DeltaPhiIncl1_EMEM16_maxPhi	0x20000019
DeltaEtaIncl1_EMEM10_minEt	0x2000001a
DeltaEtaIncl1_EMEM10_minPhi	0x2000001b
DeltaEtaIncl1_EMEM10_maxPhi	0x2000001c
EtCut_Tau25_minEt	0x2000001d
DeltaPhiIncl1_TauTau16_minEt	0x2000001e
DeltaPhiIncl1_TauTau16_minPhi	0x2000001f
DeltaPhiIncl1_TauTau16_maxPhi	0x20000020
DeltaEtaIncl1_TauTau10_minEt	0x20000021
DeltaEtaIncl1_TauTau10_minPhi	0x20000022
DeltaEtaIncl1_TauTau10_maxPhi	0x20000023
MEtCut_XE25_minEt	0x20000024

Table 30: Relative processors sub-addresses for Algorithms

- ClusterSortEM_minEt: ClusterSort EM. Minimum Et threshold.
- ClusterSortEM_isoMask: ClusterSort EM. Isolation mask
- ClusterSortEM_minEta : ClusterSort EM. Minimum Eta cut.
- ClusterSortEM_maxEta : ClusterSort EM. Maximum Eta cut.
- ClusterSortTau_minEt : ClusterSort Tau. Minimum Et threshold.
- ClusterSortTau_isoMask : ClusterSort Tau. Isolation mask.
- ClusterSortTau_minEta : ClusterSort Tau. Minimum Eta cut.
- ClusterSortTau_maxEta : ClusterSort Tau. Maximum Eta cut.
- JetSortAll_minEt : JetSort All. Minimum Et threshold.
- JetSortAll_minEta : JetSort All. Minimum Eta cut.

- JetSortAll_maxEta : JetSort All. Maximum Eta cut.
- EtCut_J25_minEt : EtCut J25. Minimum Et threshold.
- DeltaPhiIncl1_JJ16_minEt : DeltaPhiIncl1 JJ16. Minimum Et threshold.
- DeltaPhiIncl1_JJ16_minPhi : DeltaPhiIncl1 JJ16. Minimum Phi cut.
- DeltaPhiIncl1_JJ16_maxPhi : DeltaPhiIncl1 JJ16. Maximum Phi cut.
- DeltaEtaIncl1_JJ10_minEt : DeltaEtaIncl1 JJ10. Minimum Et threshold.
- DeltaEtaIncl1_JJ10_minPhi : DeltaEtaIncl1 JJ10. Minimum Eta cut.
- DeltaEtaIncl1_JJ10_maxPhi : DeltaEtaIncl1 JJ10. Maximum Eta cut.
- JetHT_HT200_minEt : JetHT HT200. Minimum Et threshold.
- JetHT_HT200_minEta : JetHT HT200. Minimum Eta cut.
- JetHT_HT200_maxEta : JetHT HT200. Maximum Eta cut.
- JetHT_HT200_minSum : JetHT HT200. Minimum Sum threshold.
- EtCut_EM25_minEt : EtCut EM25. Minimum Et threshold.
- DeltaPhiIncl1_EMEM16_minEt : DeltaPhiIncl1 EMEM16. Minimum Et threshold.
- DeltaPhiIncl1_EMEM16_minPhi : DeltaPhiIncl1 EMEM16. Minimum Phi cut.
- DeltaPhiIncl1_EMEM16_maxPhi : DeltaPhiIncl1 EMEM16. Maximum Phi cut.
- DeltaEtaIncl1_EMEM10_minEt : DeltaEtaIncl1 EMEM10. Minimum Et threshold.
- DeltaEtaIncl1_EMEM10_minPhi : DeltaEtaIncl1 EMEM10. Minimum Eta cut.
- DeltaEtaIncl1_EMEM10_maxPhi : DeltaEtaIncl1 EMEM10. Maximum Eta cut.
- EtCut_Tau25_minEt : EtCut Tau25. Minimum Et threshold.