## **Exercises**

- 1. For the following four statements, state if the statement is correct or incorrect. If you think it is incorrect, explain why and what a correct statement would be.
  - (a) Around 2006, *Moore's* law did not hold anymore. As a consequence, larger processor manufacturers started to produce multicore processors.
  - (b) The term *power wall* typically means that the maximum clock speed has been reached and that chips would be too hot if they were clocked at higher frequencies.
  - (c) Programming concurrent programs that achieve high parallel execution is a hard, but recently solved problem.
  - (d) Before the multicore era, speedup by executing programs in parallel was basically not possible.

Your solution:

2. Assume that you have a program that would take 20s to execute if you were running the program on infinitely many cores (if that was possible). Assume further that if you ran the program on 8 cores, you would get a speedup of 4. Assume also that N number of cores result in N times improvement for the part of the program that is possible to parallelize. What would then the speedup be if you executed the program on 20 cores?

Your solution:

$$4 = \frac{TA + 20}{20 + \frac{TA}{8}} \Rightarrow TA + 20 = 80 + \frac{TA}{2} \Rightarrow TA = 120$$

$$20 \text{ cores} \Rightarrow \frac{120 + 20}{20 + \frac{120}{20}} = \frac{140}{26} = \frac{70}{13} = \frac{7,30}{13}$$

## 3. Consider the MIPS code below:

- addi \$t0,\$t1,1 2 **sub** \$t1,\$s0,\$s1 3 **add** \$s1,\$t0,\$t1 **xor** \$t0,\$t1,\$s1
  - (a) Assume that we execute the code on a superscalar MIPS-processor with four functional units. What is then the maximal instructions per clock cycle (IPC) for the code snippet? Note that the IPC is computed as the average instructions per clock cycles when executing the above four instructions.
  - (b) What kind of dependency must an out-of-order processor take care of if it switches the order of the addi and the sub instructions? How can the processor resolve the hazard that occurs if the instructions are swapped?

Your solution:

Instruktioner per blockcybel

Postorer processorer fix out losa bazards genom our kour itsrving som att hith Instruktioner med konfliktregister

4. Categorize the following keywords and concepts into one of the following two scenarios. Choose the scenario that fits best.

Keywords and concepts: SIMD, MIMD, hardware multithreading, VLIW, cache coherence, Advanced Vector Extension (AVX), MapReduce, and dynamic multiple issue.

- Scenario #1: A computer with a shared memory superscalar multicore (8 cores) processor with simultanious multithreading (SMT). The processor has separated L1 caches and a common L2 cache. The computer uses a modern Linux operating system.
- Scenario #2: A cluster system with 1000 computers connected by an Ethernet network. Each computer has an uniprocessor with static multiple issue and data-level parallelism at the instruction level. The processors have separated instruction and data caches. The cluster has software for massive big data computations.

Your solution:

#1, Hardvare multithrealing, MIND, cache conevence, dynanic multiple issue #2, VLIW, AVX, MapReduce, SIMD

5. Explain the differences between a process and a thread for a modern operating system. The answer should include and clarify the following keywords: virtual memory, memory protection, files, global data, stack, and multicore.

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6. Assume that you are writing a multithreaded program in an imperative C-like language. You have one function foo () that takes zero arguments and does not return a value, but it has a side effect. This function is called from several threads. Explain and give an example with pseudo code for how you can make this function thread safe.

Your solution:

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