Exercises

1. Suppose you have a 32-bit MIPS processor. For each of the two following cache configurations, how many bits are used for the *tag* field, the *set* field (also called the *index*), and the *byte offset* field of the address?

   (a) A direct mapped cache with capacity 2048 bytes and block size 8 bytes.

   (b) A 4-way set associate cache with capacity 4096 bytes and block size 16 bytes.

   Your solution:

a) tag field : 21 bits
   Set -ll- : 8 bits
   byte offset : 3 bits
b) tag field : 22 bits
   set -ll- : 6 bits
   byte offset : 4 bits

2. Assume that you have a 32-bit MIPS processor with a direct mapped data cache with the capacity 4096 bytes and a block size of 16 bytes. The cache is initially empty (all valid bits are 0). Which sets of the cache have been updated *after* that the following program has been executed? For each of the sets, specify the *set number*, the *value of the valid bit*, and the *tag value* of the data cache.

```
1 lui     $t0,0x12ff
2 lw      $t1,0x1240($t0)
3 lw      $t2,0x5aa4($t0)
4 lw      $t3,0x4248($t0)
```

   Your solution:

2) Setnumber: 170
   tagvalue: 00 01 0010 1111 1111 0101
   valid bit : 1

Setnumber: 36
tagvalue : 0001 0010 1111 1111 0100

Validbit : 1

3. Consider Listning 1 on the last page. Assume the code is executed on a 32-bit MIPS processor that includes a *data cache* with the following properties: Capacity = 1024 bytes, direct mapped, block size = 16 bytes. Assume that the cache is empty (all valid bits are zero) before you call function `sum`. Will the *data cache* utilize temporal locality or spatial locality, or both? For each of the following C function calls, what is the *data cache hit rate* when executing the function?

   (a) `sum(0x55aa1000,10);`
   (b) `sum(0x55aa100a,30);`

   Spatial locality

   Your solution:

   a) Hit rate : 90%

   b) " : 90%

4. Consider Listning 1 on the last page. Assume the code is executed on a 32-bit MIPS processor that includes an *instruction cache* with the following properties: Capacity = 512 bytes, direct mapped, block size = 8 bytes. Assume that the cache is empty (all valid bits are zero) before you call function `sum`.

   (a) Will the *instruction cache* utilize temporal locality or spatial locality, or both?
   (b) What is the *instruct cache miss rate* when executing the function? Only count the memory accesses within the function, that is, the first instruction in the function is `xor` and the last one `jr`. The function is called with the following C statement `sum(0x6ff1000,100);` and the first instruction of `sum` is located at address `0x00400000`. Answer as a rational number.

   Your solution:

   a) 0804

   b) missrate : $\frac{4}{502} = \frac{2}{251}$

5. Suppose we have a 32-bit MIPS processor, which includes a *2-way set associative data cache* with capacity 16384 bytes, 16 bytes block, and a *least recently used (LRU)* replacement policy. Assume that the cache is empty (all valid bits are 0) before the following code is executed.

```
1          lw      $t1,0x1040($0)
2          lw      $t2,0x2044($0)
3          lw      $t3,0x3048($0)
4          lw      $t4,0x1044($0)
5          lw      $t5,0x504c($0)
6          lw      $t6,0x3040($0)
```

For each of the six assembly instructions above, state i) the *set field* value for the accessed address, ii) the *tag field value*, and iii) if the instruction results in a cache hit or a cache miss.

Your solution:

6. For each of the following statements, state if they are *true* or *false*.

   (a) A cache using a write-back policy writes back to the main memory simultaneously as it writes to the cache.

   (b) Two important properties of a virtual memory are to give the illusion of a very large memory and to give memory protection between two concurrently running programs.

   (c) A unit called the *memory management unit (MMU)* is a common solution to perform fast translations from virtual page numbers to physical page numbers.

   (d) Modern high-performance processors do not use multi-level caches because they are too expensive and give little performance benefits.

Your solution: a) F b) T c) T d) F

Corrected by _____. Total number of points: _____

The following listing is used in the seminar exercises above. You need this information to solve the exercises, but you do not have to print this page (page 5) and bring it to the seminar.

Listning 1.

```
1  sum:
2          xor     $v0,$v0,$v0
3  loop:
4          lb      $t0,0($a0)
5          add     $v0,$v0,$t0
6          addi    $a0,$a0,1
7          addi    $a1,$a1,-1
8          bne     $a1,$zero,loop
9          jr      $ra
```