digpr4 hardware documentation

Table of Contents

1 Documentation information....1
1.1 Documentation history....1
1.2 document status....1
1.3 related documents....1
1.3.1 Place holder....2
2 Introduction....2
3 Circuit description digpr4....2
3.1 Signals....2
3.1.1 input signals....3
3.2 sub circuits....4
3.3 Register....4
3.4 count window....4
3.5 counter block....4
3.6 Output mux....4

1 Documentation information

1.1 Documentation history

published versions are not consecutive

Version 7 Last saved 9. Feb. 2026 10:38 Wim Beaumont

initial version

1.2 document status

should not contain any private or sensitive information

1.3 related documents

microprocessorbestuurdemeetopstelling.pdf

digpr2.pdf

digpr4top.vhd

1.3.1 Place holder

2 Introduction

This document give additional information about the digpr4top firmware.

3 Circuit description digpr4

This circuit is an extension of digpr2.
Added are a time window. Because there are now more settings needed an register is also implemented for the static settings.

In Figure 1 the circuit schematic[1] .

The pink blocks run with a 100Mhz clock. The other blocks, that need a clock runs on a 4 Mhz clock.

The pink block is the same as the sync FF of digpr2 and the counters and the AND port for the enable line but has now 3 inputs.

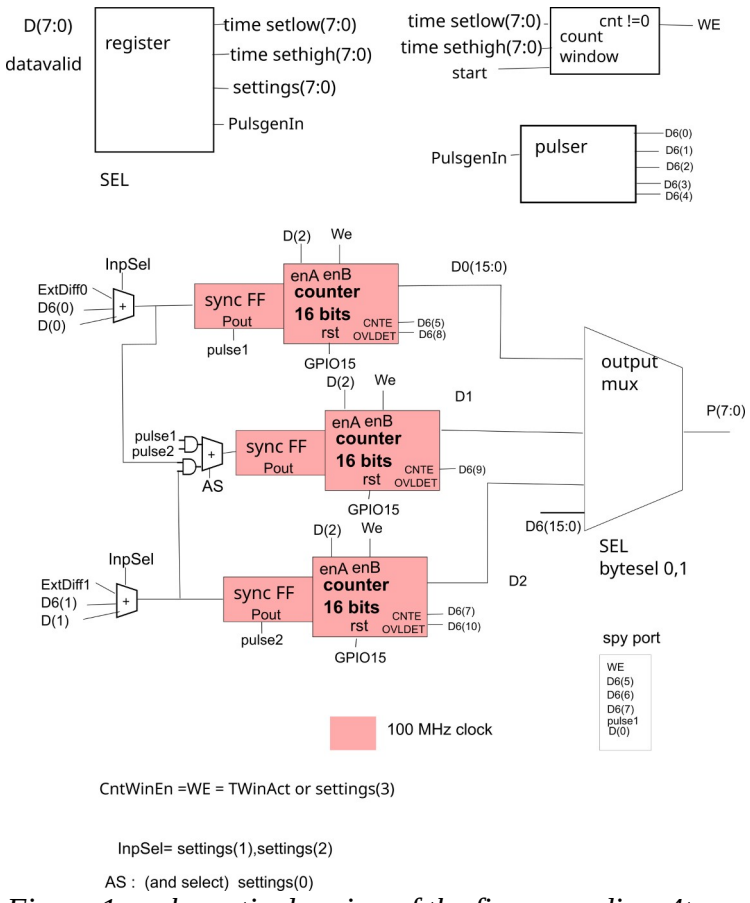

Figure 1: schematic drawing of the firmware digpr4top

3.1 Signals

The names in the top circuit corresponds to the standard naming convention for the RP used in this project. But as well in the software as in the VHDL code aliases are used to make the function more clear

1 This is only a schematic. The VHDL code is not generated from this diagram. So names can be different

3.1.1 input signals

- D(0..7) inputs. These have a double function. During the initialization these input signals are used to set the values in the register. After initialization these signals are used for dynamic settings by example enable the counters (D(2)
- selection signals
  - SEL this selects which register will be written and which data line is used for the output
  - bytesel . These signals define which byte of the selected data bus goes to the 8 bits output
- output signals
  - P(7..0) output to the RP , also this goes to the LED on the FPGA board
  - SPY port these is a collection of signals routed to the PMOD connector on the FPGA board and used for debugging. Check the VHDL code for the latest assignments of the pins.
- external control signals
  - D(2) enable signal for the counters
  - datavalid if high the D(7..0) data is written into the register.
  - Start , start the time window
  - GPIO15 == RST counter)
- internal static signals
  - timeset high /low 16 bits count down value for the time window
  - pulsein clock division signal for the pulser.
  - Setting(7..0)
    - 0: select the input for the coincidence counter. Either
      0 : asynchronous , AND the signals from the InpSel
      1 : synchronous AND the signals after the the synchronization FF’s
    - 2,1 InpSel select which signal is connected to the input counters
      0X : D(0) resp. D(1)
      10 : D6(0) , D6(1) internal pulser outputs
      11 : external differential inputs
    - 3 : time window active if 0
    - 4 .. 7 not used
- Internal dynamic signals :
  - pulse 1, 2 output of the synchronization FF’s
  - D0,D1,D2 : 16 bits output of the counters

- D6 dynamic control signals from the counters (like overflow signal) and output of the pulser.

3.2 sub circuits

3.3 Register

four 7 bits registers . The value of the D(7..0) inputs is written to the register if datavalid is high. Keep data valid low during normal operations

3.4 count window

This is a down counter. Strart with count down from the value time set, when the start signals goes high . stops when the counter reach zero. WE stays high as long the counter output is not 0.

3.5 counter block.

See digpr2

3.6 Output mux

The ouput mux is now split in a mulitplexer and a byte selection.
This is done so it is easy to extend the counter to 24 or more bits without changing the output mux. So only one value in the VHLD code has to be changed . (For mor than 32 bits an extra byte sel bit is needed) .