Pixie-16 Custom Firmware Developed for PKU

06/10/2020

Pixie-16 Variant	System FPGA		Signal Processing FPGA		DSP	
	Revision	Main Features	Revision	Main Features	Revision	Main Features
RevF_14_100	r44498	1. 4-ch debug signals of the front panel A to the chassis backplane's TriggerAll[31:28] using TrigConfig3[0] for enable/disable control 2. Able to access Multiplicity outputs on the front panel's test signal output ports 3. Accepting external timestamp clock and clear, and run inhibit signals through TriggerAll[27:25] on the backplane (via MZTIO) using TrigConfig3[1] and TrigConfig3[2] for selecting between front panel inputs and backplane inputs	r39574	1. When trace DPM is full but header DPM is not full, record the event without the trace, but output a flag to the DSP to set the correct trace length and event length in the list mode data 2. Added the option to output averaged and decimated list mode trace data (decimation factor from 0 to 2^7)	r40391	1. When calculated energy is negative, set it to 0 2. Compute energy of pileup events 3. Speed up event processing by removing unnecessary processing routines 4. Support decimated list mode data trace 5. Support recording events with only header
RevF_14_250	r44499		r44501	1. When trace DPM is full but header DPM is not full, record the event without the trace, but output a flag to the DSP to set the correct trace length and event length in the list mode data	r44496	1. When calculated energy is negative, set it to 0 2. Compute energy of pileup events 3. Speed up event processing by removing unnecessary processing routines 4. Support recording events with only header
RevF_16_250	r44499		r44502		r44497	
RevF_14_500	r44500		r34687	Standard Firmware	r43351	1. When calculated energy is negative, set it to 0 2. Compute energy of pileup events