SiS55x Family
Datasheet

Preliminary
Rev. 0.9
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1 SiS55x Overview

The SiS55x provides a high performance/low cost SoC (System on Chip) solution by integrating an x86 compatible processor, high performance North Bridge, advanced hardware GUI engine and Super-South bridge. Combining with the outstanding integrating power, the advance manufacture technology, and the smart chosen features, the single chip SiS55x is the most suitable solution for a variety of IA (Information Appliance) applications such as thin clients, set-top boxes, home gateways, web PADs, screen phones, stock machines, POS, iDVD, HDTV, VOD, and so on. With a highly compatibility with the state-of-the-art specifications in IA domain, SiS55x complies with Easy PC Initiative that supports Instantly Available/OnNow PC technology, USB, Legacy Removal, CIR, Memory Stick, Smart Card and Slotless Design. In addition, the SiS55x solution supports fully hardware and software service for quick time-to-market.

1.1 Global View of SiS55x

The SiS55x combines with an x86 compatible processor, high performance North Bridge, advanced hardware GUI engine and Super-South bridge. The global block diagram is shown in Figure 1.1.

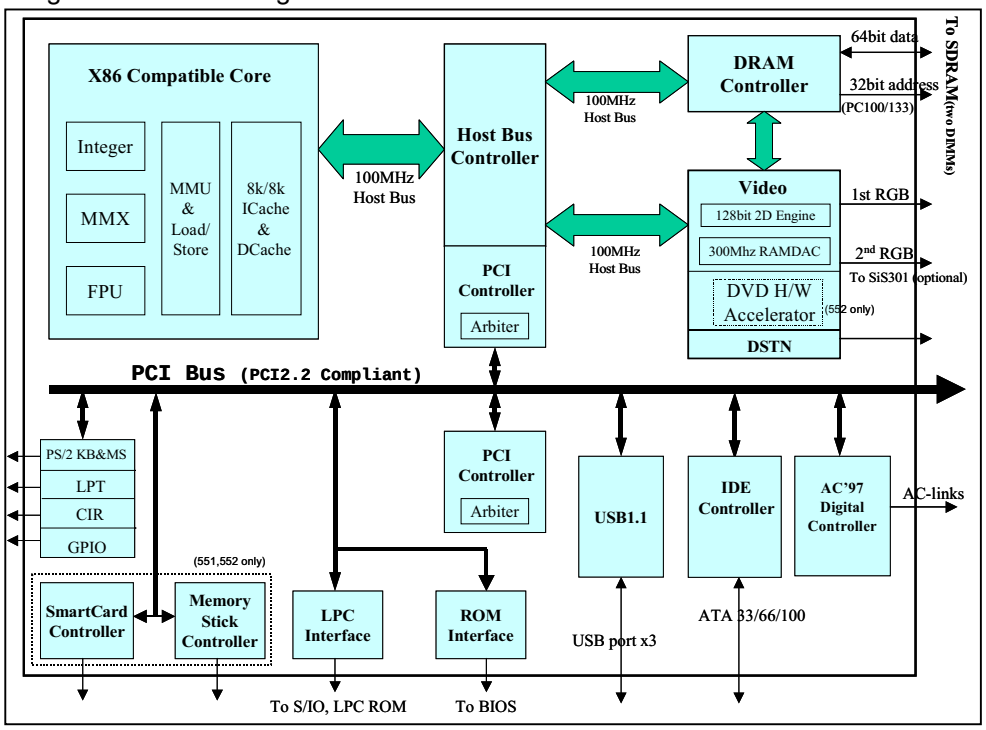


Figure 1-1. SiS55x Internal Block Diagram

SiS55x integrates a high-performance processor that supports x86 instruction set with 8-stage pipeline and 3-way superscalar architecture. It contains multimedia

unit (MMX), memory manage unit (MMU), split L1 instruction/data caches, and a fully pipelined floating point unit (FPU). In addition, the processor is a power-efficient design that optimizes the power consumption for information appliance applications.

By integrating the Ultra-AGP™ technology, SiS55x delivers high performance GUI-memory bandwidth. Furthermore, SiS55x provides powerful slice layer decoding DVD accelerator to improve the DVD playback performance (**). In addition to providing the standard interface for CRT monitors, SiS also provides the Digital Flat Panel Port (DFP) for a standard interface between a personal computer and a digital flat panel monitor. To extend functionality and flexibility, SiS also provides the "Video Bridge" (SiS301/SiS302) to support the NTSC/PAL Video Output, Digital LCD Monitor and Secondary CRT Monitor, which reduces the external Panel Link transmitter and TV-Out encoder for cost effected solution. SiS55x also adopts Share System Memory Architecture that can flexibly utilize the frame buffer size up to 128MB.

The "Super-South Bridge" in SiS55x integrates wealthy peripheral controllers /accelerators /interfaces. SiS55x offers AC'97 compliant interface that comprises digital audio engine with hardware DirectSound accelerator, on-chip sample rate converter, and professional wavetable along with separate modem DMA controller. SiS55x also provides interface to Low Pin Count (LPC) operating at 33 MHz clock that is the same as PCI clock on the host, the USB host controller with three USB ports and CIR controller deliver better connectivity and wireless flexibility. Furthermore, SiS55x includes Memory Stick controller (*) and Smart Card (*) controller for various applications.

The built-in fast PCI IDE controller supports the ATA PIO/DMA, and the Ultra DMA33/66/100 function that supports the data transfer rate up to 100 MB/s.

Note (*): The features are only supported by SiS551/SiS552, please refer to system block diagram and feature list for more information.

Note (**): The features are only supported by SiS552, please refer to system block diagram and feature list for more information.

The following illustrates the system block diagram.

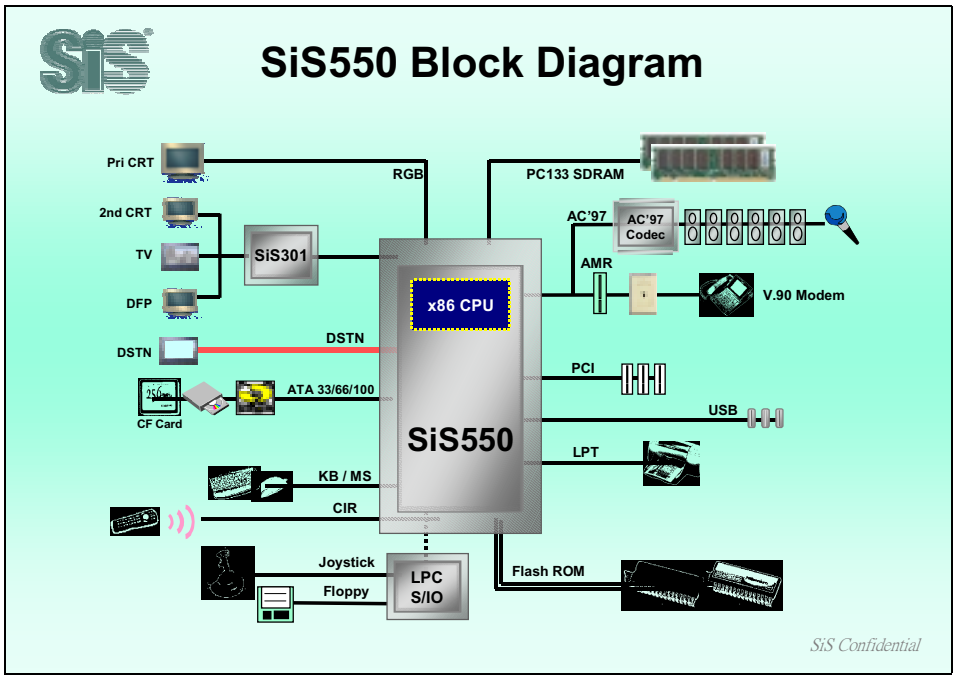


Figure 1-2. SiS550 System Block Diagram

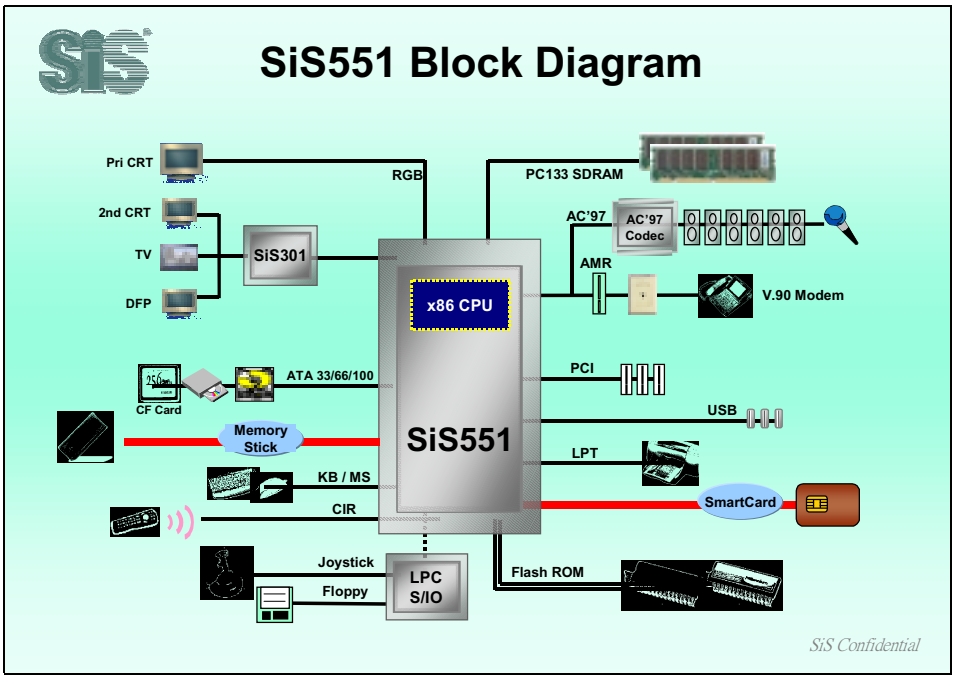


Figure 1-3. SiS551 System Block Diagram

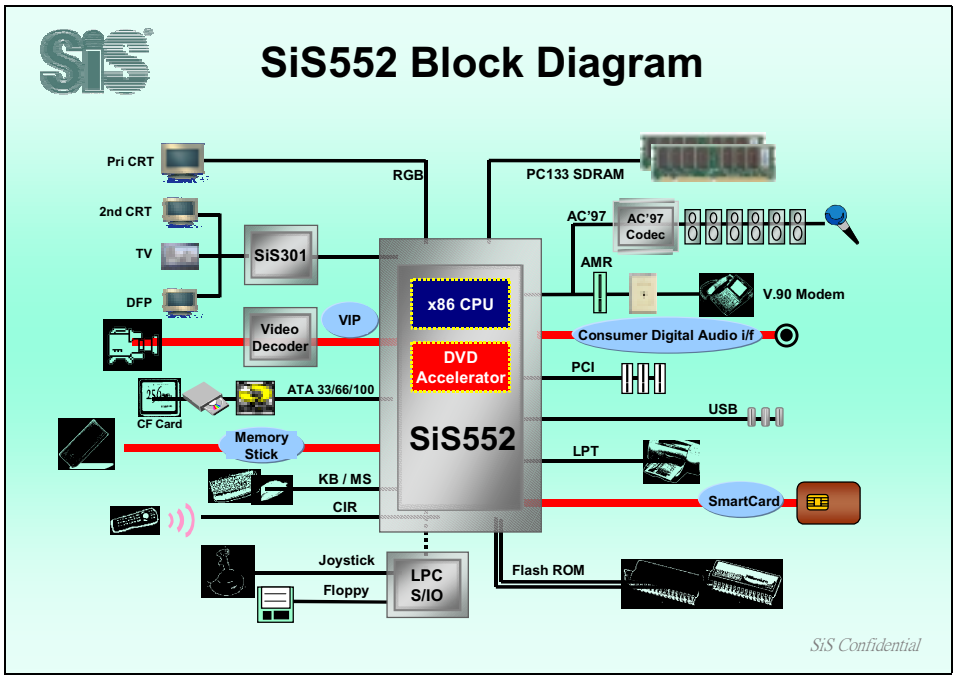


Figure 1-4. SiS552 System Block Diagram

1.2 CPU Core of SiS55x

The CPU core inside SiS55x is fully x86 compatible. It has three integer and MMX pipelines as Figure 1-5 shows. Aggressive instruction pairing and tripling rules combined with advanced branch prediction algorithms ensure that three pipelines of the processor are highly utilized. The CPU core has an eight-stage pipelined architecture, as shown in Figure 1-6, and the floating-point unit is also fully pipelined.

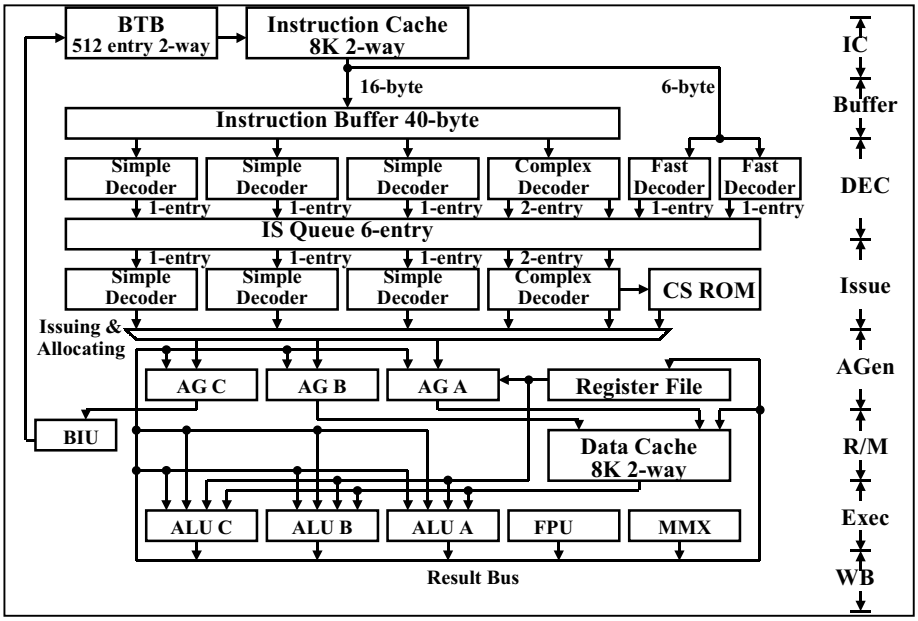


Figure 1-1. SiS55x CPU Core Block Diagram

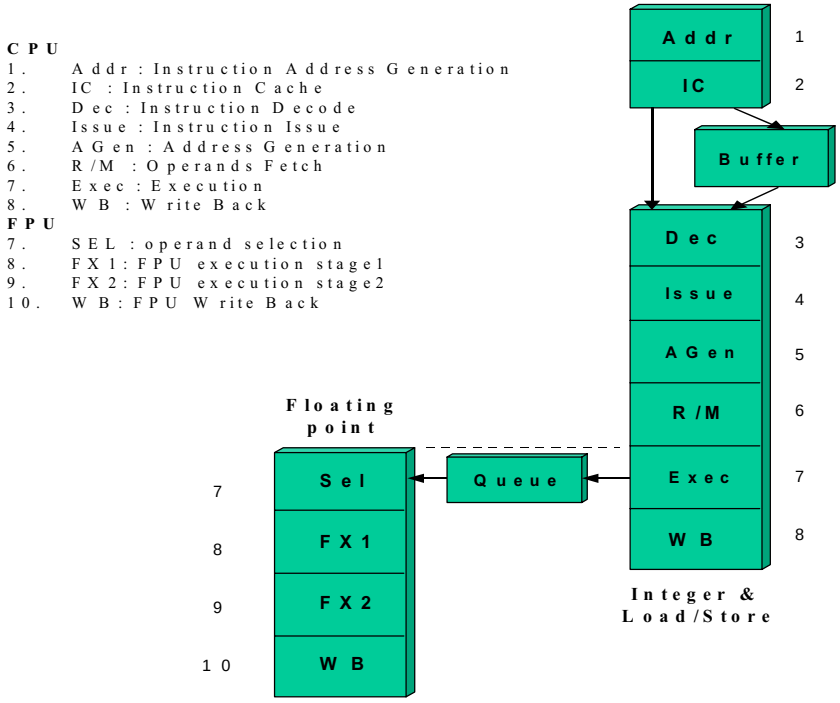


Figure 1-2. Pipeline Stages of SiS55x CPU Core

In order to manage its pipeline effectively, the CPU core uses a unique instruction pre-fetch mechanism combining with the branch prediction. A Branch Target Buffer (BTB) with 512 entries, and 4-entry call-return stack provide the base from which advanced branch algorithms operate. The CPU core can accurately predict return targets, even from nested subroutines, by storing return address in its deep call-return stack. Figure 1-7 shows this mechanism. The entries in BTB are indexed with target the target address (B) of last predicted-taken branch (A). Each entry stores two messages: one is next predicted-taken branch (C); another is 8-bit byte offset (C-B). By this mechanism, instruction fetch unit can prefetch far ahead of execution and most instruction cache-miss could be hided.

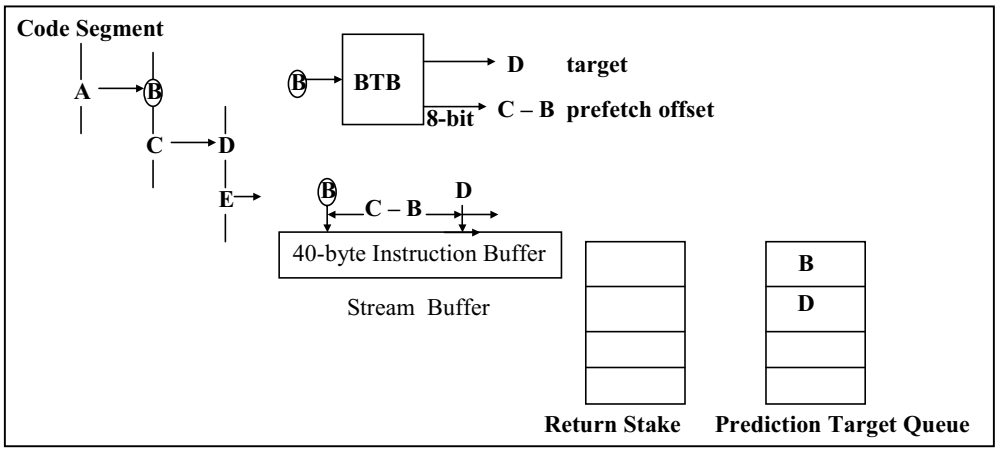


Figure 1-3. Instruction Prefetch Mechanism Combining with Branch Prediction

For reducing pipeline stalls caused by data dependency thus to improve data movement efficiency, the CPU core of SiS55x provides following features to resolves data dependency conflicts: (1) register re-mapping, (2) operand forwarding, (3) results forwarding, (4) zero cycle data bypass, and (5) arithmetic pairing. These features could reduce typical RAW (read-after-write), WAR write-after-read), and WAW write-after-write) types of data dependencies. By these features, the CPU core of SiS55x can simultaneously execute up to three of instructions that other processors cannot. Figure 1-8 and Figure 1-9 show some of the features by examples.

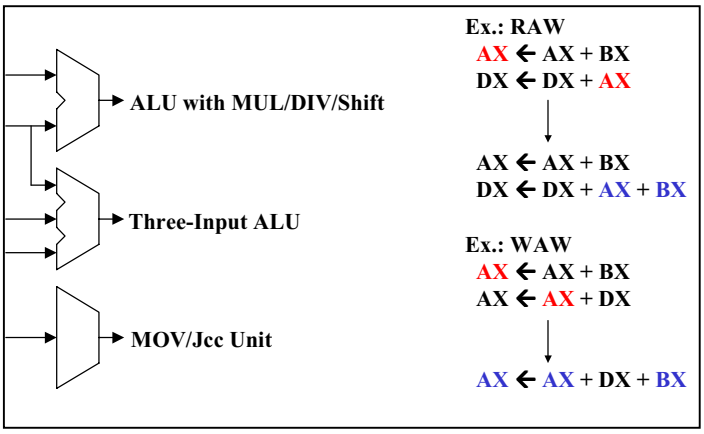


Figure 1-4. Twining Mechanism of SiS55x CPU Core

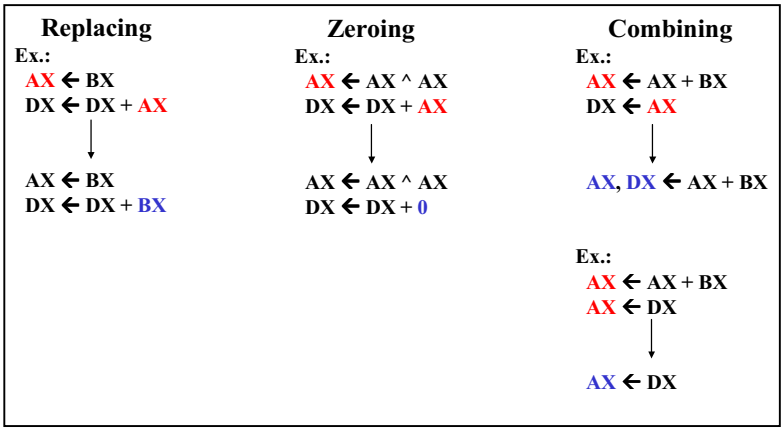


Figure 1-5. Renaming Mechanism of SiS55x CPU Core

The CPU core of SiS55x contains split L1 caches, 8k-byte instruction cache and 8k-byte data cache, both are two-way set associative. The data cache is dual ported (the tags are triple ported), and it allows two read accesses, two write accesses, and a snoop access in the same cycle. The data cache also contains filtered tag prefetching mechanism to prefetch data while minimizing bus traffic and cache pollution thus there is no misalignment penalty. This is important for multimedia applications, such as MPEG playback.

In addition to system level power saving facilities (ACPI and SMM), the CPU core of SiS55x has some internal which minimize power consumption mechanisms: (1) Facility Gating – Turns off the clocks to portions of the processor that are not needed for the current operation (such as MMX, FPU, and etc.). (2) Necessity Switching Only – Reduces dynamic power dissipation by preventing unnecessary circuit switching. (3) Required Selection Only – Allows the processor to address

and access only the minimum required amount of data from its various cache and ROM structures.

1.3 Function Block Reference

All the SiS55x integrated functions can be programmed by accessing the registers on the PCI space. The programming way is discussed in Section 4.2, and the registers are listed in another document “SiS55x Family Registers”. The following table shows how to identify these functions in the PCI command.

Table 1-1. Function Block Reference

Bus #	Device #	Function #	Device ID	IDSEL	Device Function
Bus 0	Device 0	Function 0	0550h	AD11	North Bridge
Bus 0	Device 0	Function 1	5513h	AD11	PCI IDE
Bus 1	Device 0	Function 0	5315h	AD11	GUI
Bus 0	Device 1	Function 0	0008h	AD12	LPC
Bus 0	Device 1	Function 1	7005h	AD12	Memory Stick
Bus 0	Device 1	Function 2	7001h	AD12	USB
Bus 0	Device 1	Function 4	7019h	AD12	H/W Audio
Bus 0	Device 1	Function 5	7015h	AD12	S/W Modem
Bus 0	Device 2	Function 0	0001h	AD13	Virtual PCI-to-PCI Bridge

1.4 Datasheet Organization

The remainder of this datasheet is organized as follows. Chapter 2 lists the features of SiS55x. Chapter 3 proposes the pin assignment and description. Chapter 4 guides how to program. Hardware trap pins and integrated functions are described in Chapter 5 and Chapter 6, respectively. Chapter 7 describes the electrical characteristics. Chapter 8 lists the instruction throughput. Chapter 9 describes the throttling features. Finally, Chapter 10 illustrates the mechanical package outlines

2 Features

Integrated x86 Compatible CPU

- X86 Instruction Set Compatible Processor
- High Performance with Advanced Architectures
- Superscalar Execution
- Three Superpipelined Integer Units
- Pipelined Floating Point Unit
- Innovative Instruction Decode and Branch Prediction
- Separate Code and Data Caches
- Support for Bus Frequency up to 100MHz
- Low Power Consumption Design
- Software Compatibility with Microsoft Windows, Windows CE, MS-DOS, QNX and LINUX
- Supports Host Bus Direct Access GUI Engine for Integrated A.G.P. VGA Controller

Integrated DRAM Controller

- Supports up to 2 Double Sided DIMMs (4 Rows Memory)
- Supports PC100/PC133 SDRAM Technology
- Supports NEC Virtual Channel Memory (VC-SDRAM) Technology
- System Memory Size up to 1 GB
- Supports 16Mb, 64Mb, 128Mb, 256Mb, 512Mb SDRAM Technology
- Supports Suspend-To-RAM (STR)
- Relocatable System Management Memory Region
- Programmable Buffer Strength for CS#, DQM[7:0], WE#, RAS#, CAS#, CKE, MA[14:0] and MD[63:0]
- Shadow RAM Size from 640KB to 1MB In 16KB Increments
- Two Programmable PCI Hole Areas

Integrated A.G.P. Compliant Target Host-To-PCI Bridge

- AGP V2.0 Compliant
- Supports Graphic Window Size from 4Mbytes To 256Mbytes
- Supports Pipelined Process in CPU-To-Integrated A.G.P. VGA Access
- Supports 8 Way, 16 Entries Page Table Cache for GART to Enhance Integrated VGA Controller Read/Write Performance
- Supports PCI-To-PCI Bridge Function for Memory Write from 33Mhz PCI Bus to Integrated A.G.P. VGA

Meets PC99a Requirements

PCI 2.2 Specification Compliant

High Performance PCI Arbiter

- Supports up to 3 external PCI Masters
- Rotating Priority Arbitration Scheme
- Advanced Arbitration Scheme Minimizing Arbitration Overhead
- Guaranteed Minimum Access Time for CPU And PCI Masters

Integrated Host-To-PCI Bridge

- Zero Wait State Burst Cycles
- CPU-To-PCI Pipeline Access
- 256B to 4KB PCI Burst Length for PCI Masters
- PCI Master Initiated Graphical Texture Write Cycles Re-Mapping
- Reassembles PCI Burst Data Size into Optimized Block Size

Fast PCI IDE Master/Slave Controller

- Supports PCI Bus Mastering
- Supports Native Mode and Compatibility Mode
- Supports PIO Mode 0, 1, 2, 3, 4
- Supports Multiword DMA Mode 0, 1, 2
- Supports Ultra DMA 33/66/100

Virtual PCI-To-PCI Bridge

Integrated Ultra-AGP™ VGA for Hardware 2D/Video/Graphics Accelerators

- Supports Tightly Coupled 64 Bits 100Mhz Host Interface to VGA to Speed Up GUI
- Performance and the Video Playback Frame Rate
- AGP Rev. 2.0 Compliant
- Zero-Wait-State Post-Write Buffer with Write Combine Capability
- Zero-Wait-State Read Ahead Cache Capability
- Re-Locatable Memory-Mapped and I/O Address Decoding
- Flexible Design Shared Frame Buffer Architecture for Display Memory
- Shared System Memory Area up to 128 MB
- 128-Bit 2D Engine with a Full Instruction Set
- Built-In 64x64x2 Bit-Mapped Hardware Cursor
- Built-In 32x32x16, 32x32x32 Bit-Mapped Hardware Color Cursor and Alpha Cursor
- (**) MPEG-2 ISO/IEC 13818-2 MP@ML and MPEG-1 ISO/IEC 11172-2 Standards
- Compliant
- (**) Supports Advanced H/W DVD Accelerator
- Direct DVD to TV Playback
- Supports Two Independent Video Windows with Overlay Function and Scaling Factors
- Supports YUV-To-RGB Color Space Conversion
- Supports Bi-Linear Video Interpolation with Integer Increments of Pixel Accuracy

- Supports Graphic and Video Overlay Function
- (**) Supports VCD/DVD to TV Playback Mode
- Simultaneous Graphic and TV Video Playback Overlay
- Supports Current Scan Line Of Refresh Red-Back and Interrupt
- Supports Tearing Free Double/Triple Buffer Flipping
- Supports Input Video Vertical Blank or Line Interrupt
- Supports RGB555, RGB565, YUV422 and YUV420 Video Playback Format
- Supports Filtered Horizontal up and down Scaling Playback
- (**) Supports DVD Sub-Picture Playback Overlay
- (**) Supports DVD Playback Auto-Flipping
- Built-In Two Video Playback Line Buffers
- Supports DCI Drivers
- Supports Direct Draw Drivers
- Built-In Programmable 24-Bit True-Color RAMDAC up to 300 MHz Pixel Clock RAMDAC with Snoop Function
- Built-In Reference Voltage Generator and Monitor Sense Circuit
- Supports Down-Loadable RAMDAC for Gamma Correction In High Color and True Color Modes
- Built-In Dual-Clock Generator
- Supports Multiple Adapters and Multiple Monitors
- Built-In Digital Interface for Digital TV-Out Encoder, Panellink™ (TMDS), LVDS and DSTN
- Supports Digital Flat Panel Port for Digital Monitor (LCD Panel)
- Built-In Secondary CRT Controller for Independent Secondary CRT, LCD or TV Digital Output
- Supports VESA Standard Super High Resolution Graphic Modes
- 640x480 16/256/32K/64K/16M Colors 160 Hz NI
- 800x600 16/256/32K/64K/16M Colors 120 Hz NI
- 1024x768 256/32K/64K/16M Colors 120 Hz NI
- 1280x1024 256/32K/64K/16M Colors 85 Hz NI
- 1600x1200 256/32K/64K/16M Colors 85 Hz NI
- 1920x1440 256/32K/64K Colors 60 Hz NI
- 1920x1440 256 Colors 75 Hz NI
- Low Resolution Modes
- Supports Virtual Screen up to 4096x4096
- Fully DirectX 8.0 Compliant
- Efficient and Flexible Power Management with ACPI Compliance
- Supports DDC1, DDC2B and DDC 3.0 Specifications
- Cooperate with “SiS301/302 Video Bridge” to Support

NTSC/PAL Video Output

Digital LCD Monitor

Secondary CRT Monitor

Low Pin Count Interface

- Forwards PCI I/O and Memory Cycles into LPC Bus
- Translates 8-/16-Bit DMA Cycles into PCI Bus Cycles

Advanced PCI H/W Audio & S/W Modem

- Hardware DirectSound™ accelerator

  64-Channel DirectSound™ acceleration with High Quality sampling rate converter.

  64-Voice DirectSound™ 3D Channels.

  16 On-Chip High-Precision re-routable Sub-Mixers.

  Full-duplex supports of Stereo/Mono, 8-/16-bits, and Signed/Unsigned Samples.

  Per Channel Control of Volume and Pan.

- Advanced DLS-2 compliant Wavetable Synthesizer

  64-Voices Polyphony Wavetable Synthesizer fully compliant with DLS-2.

  Per Channel control of Volume, Envelope, Pitch, Pan, Tremolo, and Vibrato etc.

  Per Channel Resonance and Cut-Off Frequency control of Low-Pass Filter.

- Fully Compliant with AC97 V2.1

  Support for up to 3 AC97 CODEC's.

  Support for AC3 2-/4-6-channels Output over AC-link.

  Support for DRC and VRC over AC-link.

  Support ever slot defined in AC97 V2.1.

  Power Management Control of AC97 CODEC.

- Telephony & Modem

  Full-Duplex Support for Line1 and Line2 over AC-link.

  Full-Duplex Support for Handset over AC-link.

- (**) Consumer Digital Audio Interface

  Support PCM/AC-3 output.

  Support AC97 CODEC's output.

Advanced Power Management

- Meets ACPI 1.0 Requirements
- Meets APM 1.2 Requirements
- ACPI Sleep States Include S1, S2, S3, S4, S5
- CPU Power States Include C0, C1, C2, C3
- Power Button with Override
- RTC Day-Of-Month, Month-Of-Year Alarm
- 24-Bit Power Management Timer

- LED Blinking In S0, S1, S2 and S3 States
- System Power-Up Events Include: Power Button, Hot-Key, Keyboard Password/ Hot- Key, RTC Alarm, Modem Ring-In, SMBALT#, LAN, PME#, AC'97 Wake-Up and USB Wake-Up
- Software Watchdog Timer
- PCI Bus Power Management Interface Spec. 1.0

Integrated DMA Controller

- Two 8237A Compatible DMA Controllers
- 8/16- Bit DMA Data Transfer
- Distributed DMA Support

Integrated Interrupt Controller

- Two 8259A Compatible Interrupt Controllers
- Level- Or Edge-Triggered Programmable Serial IRQ
- Interrupt Sources Re-Routable to Any IRQ Channel

Three 8254 Compatible Programmable 16-Bit Counters

- System Timer Interrupt
- Generate Refresh Request
- Speaker Tone Output

Integrated Keyboard Controller

- Hardwired Logic Provides Instant Response
- Supports PS/2 Mouse Interface
- Password Security and Password Power-Up
- System Sleep and Power-Up By Hot-Key
- KBC and PS/2 Mouse Can Be Individually Disabled

Integrated Real Time Clock (RTC) with 256B CMOS SRAM

- Supports ACPI Day-Of-Month and Month-Of-Year Alarm
- 256 Bytes Of CMOS SRAM
- Provides RTC H/W Year 2000 Solution

Integrated Universal Serial Bus Host Controller

- OpenHCI Host Controller with Root Hub
- Three USB Ports
- Supports Legacy Devices
- Over Current Detection

Integrated Parallel Port Controller

- Supports Parallel Port SPP mode

Integrated CIR Controller

- Supports programmable Amplitude Shift Keyed (ASK) serial communication protocol
- Supports various popular protocols including RC-5, NEC and RECS-80

- Supports 7 kinds of decoders
- Forward-Coded Decoder
- Space-Coded Decoder
- Pulse-Coded Decoder
- Silitek-Coded Decoder
- Chicony1/2-Coded Decoder
- BTC-Coded Decoder
- Software Decoder
- Supports Sample rates up to 3MHz
- Supports Hardware power on/off key decode ability
- Supports interrupt and software reset
- 32-bytes FIFO length for data reception and supports FIFO clear

(*) Integrated Smart Card Controller

- Compliant with Personal Computer Smart Card (PC/SC) Working Group standard (+)
- Compliant with smart card (ISO 7816) protocols (+)
- Supports card present detect
- Supports smart card insertion power on feature

(*) Integrated Memory Stick Controller

- Compliant with SONY memory stick protocol 1.2
- Supports memory stick present detect
- Supports power switch for memory stick

NAND Tree for Ball Connectivity Testing

686-Balls BGA Package

1.9V Core with Mixed 3.3V and 5V I/O CMOS Technology

Note (*): The features are only supported by SiS551/SiS552, please refer to system block diagram and feature list for more information.

Note (**): The features are only supported by SiS552, please refer to system block diagram and feature list for more information.

Note (+): Except that SiS55x doesn't support the commands exceeding 64 bytes.

3 Pin Assignment and Description

3.1 Pin Assignment (Top View)

3.1.1 SiS55x Pin Assignment (Top View-Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A			HD49	HD45	HD41	XECLK	XECLKBY	HD29	PLDXDU4	PLDXDU7	VAD10	VAD11	VSS	VAD3	A
B		VSS	HD51	HD47	HD42	HD36	RIPLLAVDD18	HD31	HD25	PLDXDU6	PLDXCLK	VAHSYNC	VAGCLK	VAD4	B
C	VSS	VSS	VSS	HD48	HD43	HD37	RIPLLAVDD33	HD32	HD26	PLDXDU5	PLDXDISPOFF	VAVSYNC	VDD	VAD5	C
D	HD54	HD52	VSS	VSS	HD44	HD39	RIPLLAVSS33	HD33	HD27	PLDXVCONEN	PLDXVDDEN	VAD8	VAD6	VAD0	D
E	HD58	HD57	HD56	VSS	VSS	HD40	RIFCLKDIV4	HD35	HD28	RIPLLAVSS18	HD30	VAD9	VADE	VAD1	E
F	HD62	HD61	HD60	HD59	HD55	VSS		HD50	HD46	HD38	HD34	HD24	VAD7	VAD2	F
G	LFRAME#	LAD2	LAD1	LAD0	HD53										G
H	AFD#	STB#	SMBCLK	SIRQ	LDRQ#	HD63						IVDD	PVDD	OVDD	H
J	PD5	PD4	PD3	PD2	PD0	LAD3			OVDD	IVDD	OVDD	IVDD	IVDD	OVDD	J
K	ACK#	SLIN#	PRINIT#	ERR#	PD6	SMBDAT			OVDD						K
L	IDA0	SLCT	PE	BUSY	PD7	PD1			IVDD		VSS	VSS	VSS	VSS	L
M	IDA5	IDA4	IDA3	IDA2	IDA1	IDA8		IVDD	IVDD		VSS	VSS	VSS	VSS	M
N	IDA11	IDA10	IDA9	IDA7	IDA6	IDA12		PVDD	OVDD		VSS	VSS	VSS	VSS	N
P	IDECS1#	IDECS0#	IDA15	IDA14	IDA13	IIOR#		OVDD	OVDD		VSS	VSS	VSS	VSS	P
R	IDREQ	IDACK#	IIRQ	ICHRDY	IIOW#	CDA		PVDD	IVDD		VSS	VSS	VSS	VSS	R
T	SPK	ICBLID	IDSA2	IDESA0	IDESA1	EXTSMI#		IVDD	IVDD		VSS	VSS	VSS	VSS	T
U	ENTEST	XENRITEST	XENRIBPAS	XBF0	XBF1	LDRQ1#		PVDD	OVDD		VSS	VSS	VSS	VSS	U
V	AC_SYNC	AC_BIT_CLK	AC_SDOUT	OC2#	OC0#	GPIO2		OVDD	OVDD		VSS	VSS	VSS	VSS	V
W	CLK66M	USBCLK48M	OC1#	THERM#	CKE	GPIO6			IVDD		VSS	VSS	VSS	VSS	W
Y	ACPILED	GPIO0	GPIO1	GPIO3	GPIO4	RING			AUX3.3						Y
AA	GPIO5	GPIO7	SMBALT#	PWRBTN#	AC_RESET#	KBDAT			AUX1.8	AUX3.3	OVDD	IVDD	IVDD	IVDD	AA
AB	PME#	PSON#	AC_SDIN0	AC_SDIN1	AC_SDIN2	KLOCK						OVDD	PVDD	IVDD	AB
AC	KBCLK	PMDAT	UV2-	UV2+	VSS										AC
AD	PMCLK	UV1-	UV1+	VSS	VSS			RADD7	RADD11	RDAT0	RGPIO2	IDEAVSS	PREQ2#	AD27	AD
AE	UV0-	UV0+	VSS	VSS	BATOK	INTRUDER	RADD3	RADD9	RCLK	RDAT4	PCIRST#	MS5	PREQ0#	PC/BE3#	AE
AF	USBVDD	VSS	VSS	AUXOK	RADD0	RADD5	RADD12	RADT1	RDAT6	RGPIO3	MS1	PSERR#	PGNT2#	AD28	AF
AG	VSS	VSS	PWROK	CIRRX	RADD1	RADD6	RADD14	RDAT2	RDAT7	IDEAVDD	MS3	PREQ1#	AD31	AD26	AG
AH		VSS	OSC32KHI	OSC32KHO	RADD2	RADD8	RADD13	RDAT3	RGPIO0	PCICLK	MS4	PGNT0#	AD30	AD25	AH
AJ			RTCVDD	RTCVSS	RADD4	RADD10	RADD15	RDAT5	RGPIO1	MS0	MS2	PGNT1#	AD29	AD24	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

3.1.2 SiS55x Pin Assignment (Top View-Right Side)

	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	VSS	VBCTL1	VBD7	VBD2	DDC2CLK	VIDEO0	DDC1CLK	VOSCI	PWRSTN	GOUT	DACAVSS2	VSS	VSS			A
B	VBGCLK	VBCTL0	VBDE	VBD1	DDC2DATA	VIDEO1	HSYNC	DDC1DATA	ROUT	BOUT	VSS	VSS	VSS	VSS		B
C	VDD	VBD11	VBD6	VBD0	LSYNC	VIDEO2	VSYNC	DCLKAVDD	DACAVDD2	VCOMP	VSS	VSS	VSS	GPIO9	GPIO8	C
D	VBVSYNC	VBD10	VBD5	VBCAD	RSYNC	VIDEO6	VIDEO3	DCLKAVSS	DACAVSS1	VBWN	VSS	VSS	GPIO11	SA19	SA18	D
E	VBHSYNC	VBD9	VBD4	VBHCLK	CSYNC	VIDEO7	VIDEO4	ECLKAVDD	DACAVDD1	VRSET	VSS	SA17	SA15	SA14	SA13	E
F	VBCLK	VBD8	VBD3	DDC3DATA	DDC3CLK	PCLK	VIDEO5	ECLKAVSS			SA12	SA11	SA9	SA8	SA7	F
G											SA5	SA4	SA3	SA1	SA0	G
H	PVDD	IVDD	PVDD	OVDD						ROMCS1	SD7	SD6	SD5	SD4	SD3	H
J	OVDD	IVDD	IVDD	OVDD	OVDD	IVDD	IVDD			ROMCS0	GPIO10	SD1	SD0	MWTCL	MD63	J
K							IVDD			SA16	SA10	MD30	MD62	MD29	MD61	K
L	VSS	VSS	VSS	VSS	VSS		OVDD			SA6	SA2	MD28	MD60	MD27	OVSSM	L
M	VSS	VSS	VSS	VSS	VSS		IVDD	IVDD		SD2	MD59	MD58	OVDDM	MD25	MD57	M
N	VSS	VSS	VSS	VSS	VSS		OVDDM	PVDD		MRDCL	OVSSM	MD24	MD56	MD23	MD55	N
P	VSS	VSS	VSS	OVSSM	OVSSM		OVDDM	OVDDM		MD31	MD22	MD54	MD21	MD53	OVSSM	P
R	VSS	VSS	VSS	OVSSM	OVSSM		OVDDM	PVDD		MD26	MD51	MD19	OVDDM	MD52	MD20	R
T	VSS	VSS	VSS	OVSSM	OVSSM		IVDD	IVDD		MD48	OVSSM	MD49	MD17	MD50	MD18	T
U	VSS	VSS	VSS	OVSSM	OVSSM		IVDD	PVDD		MA5	DQM2	DQM7	DQM3	MD16	OVSSM	U
V	VSS	VSS	OVSSM	OVSSM	OVSSM		OVDDM	OVDDM		DQM0	CSB2#	CSB1#	OVDDM	CSB0#	DQM6	V
W	VSS	VSS	OVSSM	OVSSM	OVSSM		OVDDM			SCAS#	OVSSM	MA12	MA13	MA14	CSB3#	W
Y							IVDD			MD12	MA4	MA9	MA10	MA11	OVSSM	Y
AA	OVDD	OVDD	IVDD	IVDD	OVDDM	IVDD	OVDDM			SDAVDD	CSA0#	MA6	OVDDM	MA7	MA8	AA
AB	PVDD	OVDD	PVDD	IVDD						SDAVSS	OVSSM	MA0	MA1	MA2	MA3	AB
AC											SRAS#	CSA3#	CSA2#	CSA1#	OVSSM	AC
AD	AD20	PTRDY#	PPAR	AD9	AD6	CPUAVDD	CPUAVSS	MD36			MD14	DQM4	OVDDM	DQM5	DQM1	AD
AE	AD23	AD16	AD15	AD13	AD4	AD1	INTB#	MD2	OVSSM	MD42	OVSSM	MD46	MD47	MD15	WE#	AE
AF	AD22	AD17	PC/BE1#	AD10	AD5	INTA#	MD32	MD34	MD4	MD6	MD40	MD44	MD45	MD13	OVSSM	AF
AG	AD21	PC/BE2#	PSTOP#	AD11	AD7	AD0	INTD#	MD1	MD3	MD38	MD7	MD9	OVDDM	MD43	MD11	AG
AH	AD19	PFRAME#	PLOCK#	AD12	PC/BE0#	AD2	XCPUCLK	MD33	OVDDM	MD5	OVDDM	MD41	MD10	SDCLK		AH
AJ	AD18	PIRDY#	PDEVSEL#	AD14	AD8	AD3	INTC#	MD0	MD35	MD37	MD39	MD8	OVSSM			AJ
	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

3.2 SiS55x Alphabetical Pin List

3.2.1 SiS55x Pin List Sorted by Ball Number

Table 3-1. 686 Pins Sorted by Ball Number

Ball No.	Signal Name.
A3	HD49
A4	HD45
A5	HD41
A6	XECLK
A7	XECLKBY
A8	HD29
A9	PLDXDU4
A10	PLDXDU7
A11	VAD10
A12	VAD11
A13	VSS
A14	VAD3
A15	VSS
A16	VBCTL1
A17	VBD7
A18	VBD2
A19	DDC2CLK
A20	VIDEO0
A21	DDC1CLK
A22	VOSCI
A23	PWRSTN
A24	GOUT
A25	DACAVSS2
A26	VSS
A27	VSS
B2	VSS
B3	HD51
Ball No.	**Signal Name.**
B4	HD47
B5	HD42
B6	HD36
B7	R1PLLAVDD18
B8	HD31
B9	HD25
B10	PLDXDU6
B11	PLDXCLK
B12	VAHSYNC
B13	VAGCLK
B14	VAD4
B15	VBGCLK
B16	VBCTL0
B17	VBDE
B18	VBD1
B19	DDC2DATA
B20	VIDEO1
B21	HSYNC
B22	DDC1DATA
B23	ROUT
B24	BOUT
B25	VSS
B26	VSS
B27	VSS
B28	VSS
C01	VSS
C02	VSS
Ball No.	**Signal Name.**
C03	VSS
C04	HD48
C05	HD43
C06	HD37
C07	R1PLLAVDD33
C08	HD32
C09	HD26
C10	PLDXDU5
C11	PLDXDISPOFFN
C12	VAVSYNC
C13	VDD
C14	VAD5
C15	VDD
C16	VBD11
C17	VBD6
C18	VBD0
C19	LSYNC
C20	VIDEO2
C21	VSYNC
C22	DCLKAVDD
C23	DACAVDD2
C24	VCOMP
C25	VSS
C26	VSS
C27	VSS
C28	GPIO9
C29	GPIO8
Ball No.	**Signal Name.**
D1	HD54
D2	HD52

D3	VSS
D4	VSS
D5	HD44
D6	HD39
D7	R1PLLAVSS33
D8	HD33
D9	HD27
D10	PLDXVCONEN
D11	PLDXVDDEN
D12	VAD8
D13	VAD6
D14	VAD0
D15	VBVSYNC
D16	VBD10
D17	VBD5
D18	VBCAD
D19	RSYNC
D20	VIDEO6
D21	VIDEO3
D22	DCLKAVSS
D23	DACAVSS1
D24	VBWN
D25	VSS
D26	VSS
D27	GPIO11
D28	SA19
D29	SA18
E1	HD58
E2	HD57
Ball No.	**Signal Name.**
E3	HD56
E4	VSS
E5	VSS
E6	HD40

E7	R1FCLKDIV4
E8	HD35
E9	HD28
E10	R1PLLAVSS18
E11	HD30
E12	VAD9
E13	VADE
E14	VAD1
E15	VBHSYNC
E16	VBD9
E17	VBD4
E18	VBHCLK
E19	CSYNC
E20	VIDEO7
E21	VIDEO4
E22	ECLKAVDD
E23	DACAVDD1
E24	VRSET
E25	VSS
E26	SA17
E27	SA15
E28	SA14
E29	SA13
F1	HD62
F2	HD61
F3	HD60
F4	HD59
Ball No.	**Signal Name.**
F5	HD55
F6	VSS
F8	HD50
F9	HD46
F10	HD38
F11	HD34

F12	HD24
F13	VAD7
F14	VAD2
F15	VBCLK
F16	VBD8
F17	VBD3
F18	DDC3DATA
F19	DDC3CLK
F20	PCLK
F21	VIDEO5
F22	ECLKAVSS
F25	SA12
F26	SA11
F27	SA9
F28	SA8
F29	SA7
G1	LFRAME#
G2	LAD2
G3	LAD1
G4	LAD0
G5	HD53
G25	SA5
G26	SA4
G27	SA3
G28	SA1
Ball No.	**Signal Name.**
G29	SA0
H1	AFD#
H2	STB#
H3	SMBCLK
H4	SIRQ
H5	LDRQ#
H6	HD63
H12	IVDD

H13	PVDD
H14	OVDD
H15	PVDD
H16	IVDD
H17	PVDD
H18	OVDD
H24	ROMCS1
H25	SD7
H26	SD6
H27	SD5
H28	SD4
H29	SD3
J1	PD5
J2	PD4
J3	PD3
J4	PD2
J5	PD0
J6	LAD3
J9	OVDD
J10	IVDD
J11	OVDD
J12	IVDD
J13	IVDD
Ball No.	**Signal Name.**
J14	OVDD
J15	OVDD
J16	IVDD
J17	IVDD
J18	OVDD
J19	OVDD
J20	IVDD
J21	IVDD
J24	ROMCS0
J25	GPIO10

J26	SD1
J27	SD0
J28	MWTCL
J29	MD63
K1	ACK#
K2	SLIN#
K3	PRINIT#
K4	ERR#
K5	PD6
K6	SMBDAT
K9	OVDD
K21	IVDD
K24	SA16
K25	SA10
K26	MD30
K27	MD62
K28	MD29
K29	MD61
L1	IDA0
L2	SLCT
L3	PE
Ball No.	**Signal Name.**
L4	BUSY
L5	PD7
L6	PD1
L9	IVDD
L11	VSS
L12	VSS
L13	VSS
L14	VSS
L15	VSS
L16	VSS
L17	VSS
L18	VSS

L19	VSS
L21	OVDD
L24	SA6
L25	SA2
L26	MD28
L27	MD60
L28	MD27
L29	OVSSM
M2	IDA4
M3	IDA3
M4	IDA2
M5	IDA1
M6	IDA8
M8	IVDD
M9	IVDD
M1	IDA5
M11	VSS
M12	VSS
M13	VSS
Ball No.	**Signal Name.**
M14	VSS
M15	VSS
M16	VSS
M17	VSS
M18	VSS
M19	VSS
M21	IVDD
M22	IVDD
M24	SD2
M25	MD59
M26	MD58
M27	OVDDM
M28	MD25
M29	MD57

N1	IDA11
N2	IDA10
N3	IDA9
N4	IDA7
N5	IDA6
N6	IDA12
N8	PVDD
N9	OVDD
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
N16	VSS
N17	VSS
N18	VSS
N19	VSS
Ball No.	**Signal Name.**
N21	OVDDM
N22	PVDD
N24	MRDCL
N25	OVSSM
N26	MD24
N27	MD56
N28	MD23
N29	MD55
P1	IDECS1#
P2	IDECS0#
P3	IDA15
P4	IDA14
P5	IDA13
P6	IIOR#
P8	OVDD
P9	OVDD

P11	VSS
P12	VSS
P13	VSS
P14	VSS
P15	VSS
P16	VSS
P17	VSS
P18	OVSSM
P19	OVSSM
P21	OVDDM
P22	OVDDM
P24	MD31
P25	MD22
P26	MD54
P27	MD21
Ball No.	**Signal Name.**
P28	MD53
P29	OVSSM
R1	IDREQ
R2	IDACK#
R3	IIRQ
R4	ICHRDY
R5	IIOW#
R6	CDA
R8	PVDD
R9	IVDD
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS
R16	VSS
R17	VSS
R18	OVSSM

R19	OVSSM
R21	OVDDM
R22	PVDD
R24	MD26
R25	MD51
R26	MD19
R27	OVDDM
R28	MD52
R29	MD20
T1	SPK
T2	ICBLID
T3	IDSA2
T4	IDESA0
Ball No.	**Signal Name.**
T5	IDESA1
T6	EXTSMI#
T8	IVDD
T9	IVDD
T11	VSS
T12	VSS
T13	VSS
T14	VSS
T15	VSS
T16	VSS
T17	VSS
T18	OVSSM
T19	OVSSM
T21	IVDD
T22	IVDD
T24	MD48
T25	OVSSM
T26	MD49
T27	MD17
T28	MD50

T29	MD18
U1	ENTEST
U2	XENR1TEST
U3	XENR1BPAS
U4	XBF0
U5	XBF1
U6	LDRQ1#
U8	PVDD
U9	OVDD
U11	VSS
U12	VSS
Ball No.	**Signal Name.**
U13	VSS
U14	VSS
U15	VSS
U16	VSS
U17	VSS
U18	OVSSM
U19	OVSSM
U21	IVDD
U22	PVDD
U24	MA5
U25	DQM2
U26	DQM7
U27	DQM3
U28	MD16
U29	OVSSM
V1	AC_SYNC
V2	AC_BIT_CLK
V3	AC_SDOUT
V4	OC2#
V5	OC0#
V6	GPIO2
V8	OVDD

V9	OVDD
V11	VSS
V12	VSS
V13	VSS
V14	VSS
V15	VSS
V16	VSS
V17	OVSSM
V18	OVSSM
Ball No.	**Signal Name.**
V19	OVSSM
V21	OVDDM
V22	OVDDM
V24	DQM0
V25	CSB2#
V26	CSB1#
V27	OVDDM
V28	CSB0#
V29	DQM6
W1	CLK66M
W2	USBCLK48M
W3	OC1#
W4	THERM#
W5	CKE
W6	GPIO6
W9	IVDD
W11	VSS
W12	VSS
W13	VSS
W14	VSS
W15	VSS
W16	VSS
W17	OVSSM
W18	OVSSM

W19	OVSSM
W21	OVDDM
W24	SCAS#
W25	OVSSM
W26	MA12
W27	MA13
W28	MA14
Ball No.	**Signal Name.**
W29	CSB3#
Y1	ACPILED
Y2	GPIO0
Y3	GPIO1
Y4	GPIO3
Y5	GPIO4
Y6	RING
Y9	AUX3.3
Y21	IVDD
Y24	MD12
Y25	MA4
Y26	MA9
Y27	MA10
Y28	MA11
Y29	OVSSM
AA1	GPIO5
AA2	GPIO7
AA3	SMBALT#
AA4	PWRBTN#
AA5	AC_RESET#
AA6	KBDAT
AA9	AUX1.8
AA10	AUX3.3
AA11	OVDD
AA12	IVDD
AA13	IVDD

AA14	IVDD
AA15	OVDD
AA16	OVDD
AA17	IVDD
AA18	IVDD
Ball No.	**Signal Name.**
AA19	OVDDM
AA20	IVDD
AA21	OVDDM
AA24	SDAVDD
AA25	CSA0#
AA26	MA6
AA27	OVDDM
AA28	MA7
AA29	MA8
AB1	PME#
AB2	PSON#
AB3	AC_SDIN0
AB4	AC_SDIN1
AB5	AC_SDIN2
AB6	KLOCK
AB12	OVDD
AB13	PVDD
AB14	IVDD
AB15	PVDD
AB16	OVDD
AB17	PVDD
AB18	IVDD
AB24	SDAVSS
AB25	OVSSM
AB26	MA0
AB27	MA1
AB28	MA2
AB29	MA3

AC1	KBCLK
AC2	PMDAT
AC3	UV2-
Ball No.	**Signal Name.**
AC4	UV2+
AC5	VSS
AC25	SRAS#
AC26	CSA3#
AC27	CSA2#
AC28	CSA1#
AC29	OVSSM
AD1	PMCLK
AD2	UV1-
AD3	UV1+
AD4	VSS
AD5	VSS
AD8	RADD7
AD9	RADD11
AD10	RDAT0
AD11	RGPIO2
AD12	IDEAVSS
AD13	PREQ2#
AD14	AD27
AD15	AD20
AD16	PTRDY#
AD17	PPAR
AD18	AD9
AD19	AD6
AD20	CPUAVDD
AD21	CPUAVSS
AD22	MD36
AD25	MD14
AD26	DQM4
AD27	OVDDM

AD28	DQM5
Ball No.	**Signal Name.**
AD29	DQM1
AE1	UV0-
AE2	UV0+
AE3	VSS
AE4	VSS
AE5	BATOK
AE6	INTRUDER
AE7	RADD3
AE8	RADD9
AE9	RCLK
AE10	RDAT4
AE11	PCIRST#
AE12	MS5
AE13	PREQ0#
AE14	PC/BE3#
AE15	AD23
AE16	AD16
AE17	AD15
AE18	AD13
AE19	AD4
AE20	AD1
AE21	INTB#
AE22	MD2
AE23	OVSSM
AE24	MD42
AE25	OVSSM
AE26	MD46
AE27	MD47
AE28	MD15
AE29	WE#
AF1	USBVDD
Ball No.	**Signal Name.**

AF2	VSS
AF3	VSS
AF4	AUXOK
AF5	RADD0
AF6	RADD5
AF7	RADD12
AF8	RADT1
AF9	RDAT6
AF10	RGPIO3
AF11	MS1
AF12	PSERR#
AF13	PGNT2#
AF14	AD28
AF15	AD22
AF16	AD17
AF17	PC/BE1#
AF18	AD10
AF19	AD5
AF20	INTA#
AF21	MD32
AF22	MD34
AF23	MD4
AF24	MD6
AF25	MD40
AF26	MD44
AF27	MD45
AF28	MD13
AF29	OVSSM
AG1	VSS
AG2	VSS
AG3	PWROK

Ball No.	**Signal Name.**
AG4	CIRRX
AG5	RADD1
AG6	RADD6
AG7	RADD14
AG8	RDAT2
AG9	RDAT7
AG10	IDEAVDD
AG11	MS3
AG12	PREQ1#
AG13	AD31
AG14	AD26
AG15	AD21
AG16	PC/BE2#
AG17	PSTOP#
AG18	AD11
AG19	AD7
AG20	AD0
AG21	INTD#
AG22	MD1
AG23	MD3
AG24	MD38
AG25	MD7
AG26	MD9
AG27	OVDDM
AG28	MD43
AG29	MD11
AH2	VSS
AH3	OSC32KHI
AH4	OSC32KHO
AH5	RADD2
AH6	RADD8

Ball No.	**Signal Name.**
AH7	RADD13
AH8	RDAT3
AH9	RGPIO0
AH10	PCICLK
AH11	MS4
AH12	PGNT0#
AH13	AD30
AH14	AD25
AH15	AD19
AH16	PFRAME#
AH17	PLOCK#
AH18	AD12
AH19	PC/BE0#
AH20	AD2
AH21	XCPUCLK
AH22	MD33

Ball No.	**Signal Name.**
AH23	OVDDM
AH24	MD5
AH25	OVDDM
AH26	MD41
AH27	MD10
AH28	SDCLK
AJ3	RTCVDD
AJ4	RTCVSS
AJ5	RADD4
AJ6	RADD10
AJ7	RADD15
AJ8	RDAT5
AJ9	RGPIO1
AJ10	MS0
AJ11	MS2
AJ12	PGNT1#

Ball No.	**Signal Name.**
AJ13	AD29
AJ14	AD24

AJ15	AD18
AJ16	PIRDY#
AJ17	PDEVSEL#
AJ18	AD14
AJ19	AD8

AJ20	AD3
AJ21	INTC#
AJ22	MD0
AJ23	MD35
AJ24	MD37

AJ25	MD39
AJ26	MD8
AJ27	OVSSM

3.2.2 SiS55x Pin List Sorted by Signal Name

Table 3-1. 686 Pins Sorted by Signal Name

Signal Name	Ball No.
AC_BIT_CLK	V2
AC_RESET#	AA5
AC_SDIN0	AB3
AC_SDIN1	AB4
AC_SDIN2	AB5
AC_SDOUT	V3
AC_SYNC	V1
ACK#	K1
ACPILED	Y1
Signal Name	**Ball No.**
AD0	AG20
AD1	AE20
AD10	AF18
AD11	AG18
AD12	AH18
AD13	AE18
AD14	AJ18
AD15	AE17
AD16	AE16
Signal Name	**Ball No.**
AD17	AF16
AD18	AJ15
AD19	AH15

AD2	AH20
AD20	AD15
AD21	AG15
AD22	AF15
AD23	AE15
AD24	AJ14
Signal Name	**Ball No.**
AD25	AH14
AD26	AG14
AD27	AD14
AD28	AF14
AD29	AJ13
AD3	AJ20
AD30	AH13
AD31	AG13
AD4	AE19
AD5	AF19
AD6	AD19
AD7	AG19
AD8	AJ19
AD9	AD18
AFD#	H1
AUX1.8	AA9
AUX3.3	AA10

AUX3.3	Y9
AUXOK	AF4
BATOK	AE5
BOUT	B24
BUSY	L4
CDA	R6
CIRRX	AG4
CKE	W5
CLK66M	W1
CPUAVDD	AD20
CPUAVSS	AD21
CSA0#	AA25
CSA1#	AC28
CSA2#	AC27
Signal Name	**Ball No.**
CSA3#	AC26
CSB0#	V28
CSB1#	V26
CSB2#	V25
CSB3#	W29
CSYNC	E19
DACAVDD1	E23
DACAVDD2	C23
DACAVSS1	D23

DACAVSS2	A25
DCLKAVDD	C22
DCLKAVSS	D22
DDC1CLK	A21
DDC1DATA	B22
DDC2CLK	A19
DDC2DATA	B19
DDC3CLK	F19
DDC3DATA	F18
DQM0	V24
DQM1	AD29
DQM2	U25
DQM3	U27
DQM4	AD26
DQM5	AD28
DQM6	V29
DQM7	U26
ECLKAVDD	E22
ECLKAVSS	F22
ENTEST	U1
ERR#	K4
EXTSMI#	T6
Signal Name	**Ball No.**
GOUT	A24
GPIO0	Y2
GPIO1	Y3
GPIO10	J25
GPIO11	D27
GPIO2	V6
GPIO3	Y4
GPIO4	Y5
GPIO5	AA1
GPIO6	W6
GPIO7	AA2

GPIO8	C29
GPIO9	C28
HD24	F12
HD25	B9
HD26	C9
HD27	D9
HD28	E9
HD29	A8
HD30	E11
HD31	B8
HD32	C8
HD33	D8
HD34	F11
HD35	E8
HD36	B6
HD37	C6
HD38	F10
HD39	D6
HD40	E6
HD41	A5
Signal Name	**Ball No.**
HD42	B5
HD43	C5
HD44	D5
HD45	A4
HD46	F9
HD47	B4
HD48	C4
HD49	A3
HD50	F8
HD51	B3
HD52	D2
HD53	G5
HD54	D1

HD55	F5
HD56	E3
HD57	E2
HD58	E1
HD59	F4
HD60	F3
HD61	F2
HD62	F1
HD63	H6
HSYNC	B21
ICBLID	T2
ICHRDY	R4
IDA0	L1
IDA1	M5
IDA10	N2
IDA11	N1
IDA12	N6
IDA13	P5
Signal Name	**Ball No.**
IDA14	P4
IDA15	P3
IDA2	M4
IDA3	M3
IDA4	M2
IDA5	M1
IDA6	N5
IDA7	N4
IDA8	M6
IDA9	N3
IDACK#	R2
IDEAVDD	AG10
IDEAVSS	AD12
IDECS0#	P2
IDECS1#	P1

IDESA0	T4
IDESA1	T5
IDREQ	R1
IDSA2	T3
IIOR#	P6
IIOW#	R5
IIRQ	R3
INTA#	AF20
INTB#	AE21
INTC#	AJ21
INTD#	AG21
INTRUDER	AE6
IVDD	AA12
IVDD	AA13
IVDD	AA14
IVDD	AA17
Signal Name	**Ball No.**
IVDD	AA18
IVDD	AA20
IVDD	AB14
IVDD	AB18
IVDD	H12
IVDD	H16
IVDD	J10
IVDD	J12
IVDD	J13
IVDD	J16
IVDD	J17
IVDD	J20
IVDD	J21
IVDD	K21
IVDD	L9
IVDD	M21
IVDD	M22

IVDD	M8
IVDD	M9
IVDD	R9
IVDD	T21
IVDD	T22
IVDD	T8
IVDD	T9
IVDD	U21
IVDD	W9
IVDD	Y21
KBCLK	AC1
KBDAT	AA6
KLOCK	AB6
LAD0	G4
Signal Name	**Ball No.**
LAD1	G3
LAD2	G2
LAD3	J6
LDRQ#	H5
LDRQ1#	U6
LFRAME#	G1
LSYNC	C19
MA0	AB26
MA1	AB27
MA10	Y27
MA11	Y28
MA12	W26
MA13	W27
MA14	W28
MA2	AB28
MA3	AB29
MA4	Y25
MA5	U24
MA6	AA26

MA7	AA28
MA8	AA29
MA9	Y26
MD0	AJ22
MD1	AG22
MD10	AH27
MD11	AG29
MD12	Y24
MD13	AF28
MD14	AD25
MD15	AE28
MD16	U28
Signal Name	**Ball No.**
MD17	T27
MD18	T29
MD19	R26
MD2	AE22
MD20	R29
MD21	P27
MD22	P25
MD23	N28
MD24	N26
MD25	M28
MD26	R24
MD27	L28
MD28	L26
MD29	K28
MD3	AG23
MD30	K26
MD31	P24
MD32	AF21
MD33	AH22
MD34	AF22
MD35	AJ23

MD36	AD22
MD37	AJ24
MD38	AG24
MD39	AJ25
MD4	AF23
MD40	AF25
MD41	AH26
MD42	AE24
MD43	AG28
MD44	AF26
Signal Name	**Ball No.**
MD45	AF27
MD46	AE26
MD47	AE27
MD48	T24
MD49	T26
MD5	AH24
MD50	T28
MD51	R25
MD52	R28
MD53	P28
MD54	P26
MD55	N29
MD56	N27
MD57	M29
MD58	M26
MD59	M25
MD6	AF24
MD60	L27
MD61	K29
MD62	K27
MD63	J29
MD7	AG25
MD8	AJ26

MD9	AG26
MRDCL	N24
MS0	AJ10
MS1	AF11
MS2	AJ11
MS3	AG11
MS4	AH11
MS5	AE12
Signal Name	**Ball No.**
MWTCL	J28
OC0#	V5
OC1#	W3
OC2#	V4
OSC32KHI	AH3
OSC32KHO	AH4
OVDD	AA11
OVDD	AA15
OVDD	AA16
OVDD	AB12
OVDD	AB16
OVDD	H14
OVDD	H18
OVDD	J11
OVDD	J14
OVDD	J15
OVDD	J18
OVDD	J19
OVDD	J9
OVDD	K9
OVDD	L21
OVDD	N9
OVDD	P8
OVDD	P9
OVDD	U9

OVDD	V8
OVDD	V9
OVDDM	AA19
OVDDM	AA21
OVDDM	AA27
OVDDM	AD27
Signal Name	**Ball No.**
OVDDM	AG27
OVDDM	AH23
OVDDM	AH25
OVDDM	M27
OVDDM	N21
OVDDM	P21
OVDDM	P22
OVDDM	R21
OVDDM	R27
OVDDM	V21
OVDDM	V22
OVDDM	V27
OVDDM	W21
OVSSM	AB25
OVSSM	AC29
OVSSM	AE23
OVSSM	AE25
OVSSM	AF29
OVSSM	AJ27
OVSSM	L29
OVSSM	N25
OVSSM	P18
OVSSM	P19
OVSSM	P29
OVSSM	R18
OVSSM	R19
OVSSM	T18

OVSSM	T19
OVSSM	T25
OVSSM	U18
OVSSM	U19
Signal Name	**Ball No.**
OVSSM	U29
OVSSM	V17
OVSSM	V18
OVSSM	V19
OVSSM	W17
OVSSM	W18
OVSSM	W19
OVSSM	W25
OVSSM	Y29
PC/BE0#	AH19
PC/BE1#	AF17
PC/BE2#	AG16
PC/BE3#	AE14
PCICLK	AH10
PCIRST#	AE11
PCLK	F20
PD0	J5
PD1	L6
PD2	J4
PD3	J3
PD4	J2
PD5	J1
PD6	K5
PD7	L5
PDEVSEL#	AJ17
PE	L3
PFRAME#	AH16
PGNT0#	AH12
PGNT1#	AJ12

PGNT2#	AF13
PIRDY#	AJ16
Signal Name	**Ball No.**
PLDXCLK	B11
PLDXDISPOFFN	C11
PLDXDU4	A9
PLDXDU5	C10
PLDXDU6	B10
PLDXDU7	A10
PLDXVCONEN	D10
PLDXVDDEN	D11
PLOCK#	AH17
PMCLK	AD1
PMDAT	AC2
PME#	AB1
PPAR	AD17
PREQ0#	AE13
PREQ1#	AG12
PREQ2#	AD13
PRINIT#	K3
PSERR#	AF12
PSON#	AB2
PSTOP#	AG17
PTRDY#	AD16
PVDD	AB13
PVDD	AB15
PVDD	AB17
PVDD	H13
PVDD	H15
PVDD	H17
PVDD	N22
PVDD	N8
PVDD	R22
PVDD	R8

Signal Name	**Ball No.**
PVDD	U22
PVDD	U8
PWRBTN#	AA4
PWROK	AG3
PWRSTN	A23
R1FCLKDIV4	E7
R1PLLAVDD18	B7
R1PLLAVDD33	C7
R1PLLAVSS18	E10
R1PLLAVSS33	D7
RADD0	AF5
RADD1	AG5
RADD10	AJ6
RADD11	AD9
RADD12	AF7
RADD13	AH7
RADD14	AG7
RADD15	AJ7
RADD2	AH5
RADD3	AE7
RADD4	AJ5
RADD5	AF6
RADD6	AG6
RADD7	AD8
RADD8	AH6
RADD9	AE8
RADT1	AF8
RCLK	AE9
RDAT0	AD10
RDAT2	AG8
RDAT3	AH8
Signal Name	**Ball No.**
RDAT4	AE10

RDAT5	AJ8
RDAT6	AF9
RDAT7	AG9
RGPIO0	AH9
RGPIO1	AJ9
RGPIO2	AD11
RGPIO3	AF10
RING	Y6
ROMCS0	J24
ROMCS1	H24
ROUT	B23
RSYNC	D19
RTCVDD	AJ3
RTCVSS	AJ4
SA0	G29
SA1	G28
SA10	K25
SA11	F26
SA12	F25
SA13	E29
SA14	E28
SA15	E27
SA16	K24
SA17	E26
SA18	D29
SA19	D28
SA2	L25
SA3	G27
SA4	G26
SA5	G25
Signal Name	**Ball No.**
SA6	L24
SA7	F29
SA8	F28

SA9	F27
SCAS#	W24
SD0	J27
SD1	J26
SD2	M24
SD3	H29
SD4	H28
SD5	H27
SD6	H26
SD7	H25
SDAVDD	AA24
SDAVSS	AB24
SDCLK	AH28
SIRQ	H4
SLCT	L2
SLIN#	K2
SMBALT#	AA3
SMBCLK	H3
SMBDAT	K6
SPK	T1
SRAS#	AC25
STB#	H2
THERM#	W4
USBCLK48M	W2
USBVDD	AF1
UV0-	AE1
UV0+	AE2
UV1-	AD2
Signal Name	**Ball No.**
UV1+	AD3
UV2-	AC3
UV2+	AC4
VAD0	D14
VAD1	E14

VAD10	A11
VAD11	A12
VAD2	F14
VAD3	A14
VAD4	B14
VAD5	C14
VAD6	D13
VAD7	F13
VAD8	D12
VAD9	E12
VADE	E13
VAGCLK	B13
VAHSYNC	B12
VAVSYNC	C12
VBCAD	D18
VBCLK	F15
VBCTL0	B16
VBCTL1	A16
VBD0	C18
VBD1	B18
VBD10	D16
VBD11	C16
VBD2	A18
VBD3	F17
VBD4	E17
VBD5	D17
Signal Name	**Ball No.**
VBD6	C17
VBD7	A17
VBD8	F16
VBD9	E16
VBDE	B17
VBGCLK	B15
VBHCLK	E18

VBHSYNC	E15
VBVSYNC	D15
VBWN	D24
VCOMP	C24
VDD	C13
VDD	C15
VIDEO0	A20
VIDEO1	B20
VIDEO2	C20
VIDEO3	D21
VIDEO4	E21
VIDEO5	F21
VIDEO6	D20
VIDEO7	E20
VOSCI	A22
VRSET	E24
VSS	A13
VSS	A15
VSS	A26
VSS	A27
VSS	AC5
VSS	AD4
VSS	AD5
VSS	AE3
Signal Name	**Ball No.**
VSS	AE4
VSS	AF2
VSS	AF3
VSS	AG1
VSS	AG2
VSS	AH2
VSS	B2
VSS	B25
VSS	B26

VSS	B27
VSS	B28
VSS	C1
VSS	C2
VSS	C25
VSS	C26
VSS	C27
VSS	C3
VSS	D25
VSS	D26
VSS	D3
VSS	D4
VSS	E25
VSS	E4
VSS	E5
VSS	F6
VSS	L11
VSS	L12
VSS	L13
VSS	L14
VSS	L15
VSS	L16
Signal Name	**Ball No.**
VSS	L17
VSS	L18
VSS	L19
VSS	M11
VSS	M12
VSS	M13
VSS	M14
VSS	M15
VSS	M16
VSS	M17
VSS	M18

VSS	M19
VSS	N11
VSS	N12
VSS	N13
VSS	N14
VSS	N15
VSS	N16
VSS	N17
VSS	N18
VSS	N19
VSS	P11
VSS	P12
VSS	P13
VSS	P14
VSS	P15
VSS	P16
VSS	P17
VSS	R11
VSS	R12
VSS	R13
Signal Name	**Ball No.**
VSS	R14
VSS	R15
VSS	R16
VSS	R17
VSS	T11
VSS	T12
VSS	T13
VSS	T14
VSS	T15
VSS	T16
VSS	T17
VSS	U11
VSS	U12

VSS	U13
VSS	U14
VSS	U15
VSS	U16
VSS	U17
VSS	V11
VSS	V12

VSS	V13
VSS	V14
VSS	V15
VSS	V16
VSS	W11
VSS	W12
VSS	W13

VSS	W14
VSS	W15
VSS	W16
VSYNC	C21

Signal Name	**Ball No.**
WE#	AE29
XBF0	U4
XBF1	U5
XCPUCLK	AH21
XECLK	A6
XECLKBY	A7
XENR1BPAS	U3
XENR1TEST	U2

3.3 Power Plane

Vcore = 1.9V, 1.8V, or 1.7V, depending on the selected Vcore level described in Section 7.2.3.

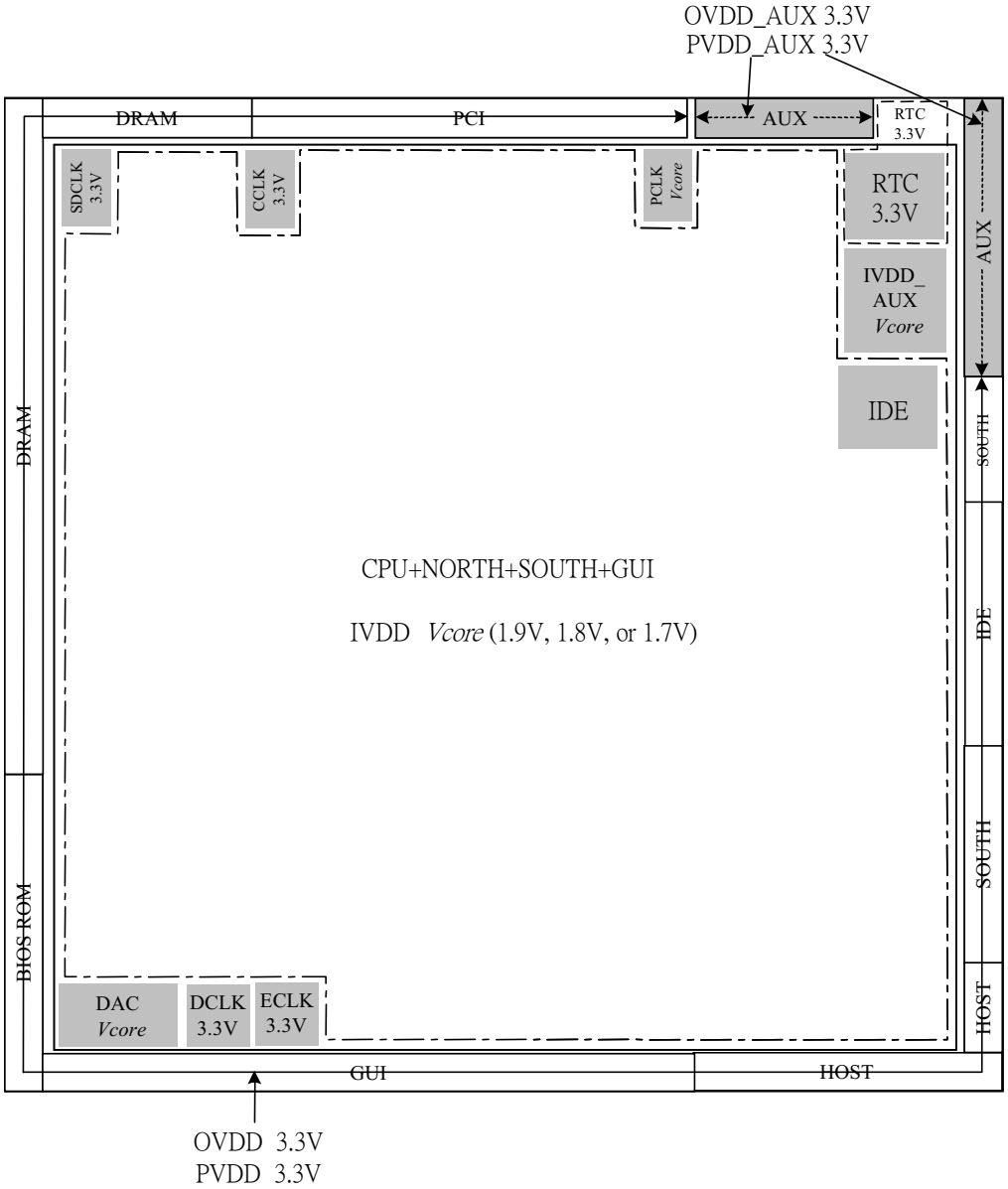


Figure 3-1. SiS55x Power Plane

3.4 Pin Description (Preliminary)

Power Plane:

AUX: Power exists regardless the system is power down or power up unless the power cord is disconnected.

MAIN: Power exists only the system is power up.

RTC: Battery power.

3.4.1 Host interface Signals

Name	Tolerance	Power Plane	Type Attr.	Description
XECLK	3.3V	MAIN	I	Host Clock: Primary clock input to processor core.
XECLKBY	3.3V	MAIN	I	Clock input for test mode
XBF[1:0]	3.3V	MAIN	I	Host Bus to Processor Core Frequency Ratio
HD[63:24]	3.3V	MAIN	I/O	Host Data Bus(*)

(*): Reserved for SiS internal reference only.

3.4.2 DRAM Controller

Name	Tolerance	Power Plane	Type Attr.	Description
SDCLK	3.3V/5V	MAIN	I	SDRAM Clock Input
MD[63:0]	3.3V	MAIN	I/O	System Memory Data Bus
MA[14:0]	3.3V	MAIN	O	System Memory Address Bus
CSA[3:0]#	3.3V	MAIN	O	SDRAM Chip Select
CSB[3:0]#	3.3V	MAIN	O	SDRAM Chip Select Signals (Duplicated Copy)
DQM[7:0]#	3.3V	MAIN	O	SDRAM Input/Output Data Mask
WE#	3.3V	MAIN	O	SDRAM Write Enable
SRAS#	3.3V	MAIN	O	SDRAM Row Address Strobe
SCAS#	3.3V	MAIN	O	SDRAM Column Address Strobe

CKE	3.3V	AUX	O	SDRAM Clock Enable During Suspend-to-DRAM mode (ACPI S2 or S3 state), SDRAM can be put into self-refresh mode by asserting CKE.

3.4.3 PCI Interface

Name	Tolerance	Power Plane	Type Attr.	Description
PCICLK	3.3V/5V	MAIN	I	PCI Clock : The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS55x. It runs at the same frequency and skew of the PCI local bus.
PC/BE[3:0]#	3.3V/5V	MAIN	I/O	PCI Bus Command and Byte Enables: PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. PC/BE[3:0]# are outputs when the SiS55x is a PCI bus master and inputs when it is a PCI slave.

AD[31:0]	3.3V/5V	MAIN	I/O	PCI Address /Data Bus: In address phase: 1.When the SiS55x is a PCI bus master, AD[31:0] are output signals. 2.When the SiS55x is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS55x is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS55x is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PPAR	3.3V/5V	MAIN	I/O	Parity: SiS55x drives out Even Parity covering AD[31:0] and PC/BE[3:0]#. It does not check the input parity signal.
PFRAME#	3.3V/5V	MAIN	I/O	Frame: PFRAME# is an output when the SiS55x is a PCI bus master. The SiS55x drives PFRAME# to indicate the beginning and duration of an access. When the SiS55x is a PCI slave device, PFRAME# is an input signal.

PIRDY#	3.3V/5V	MAIN	I/O	Initiator Ready: PIRDY# is an output when the SiS55x is a PCI bus master. The assertion of PIRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, PIRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, PIRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS55x is a PCI slave, PIRDY# is an input pin.
PTRDY#	3.3V/5V	MAIN	I/O	Target Ready: PTRDY# is an output when the SiS55x is a PCI slave. The assertion of PTRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, PTRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, PTRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS55x is a PCI master, it is an input pin.

PSTOP#	3.3V/5V	MAIN	I/O	Stop: PSTOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. PSTOP# is used for disconnect, retry, and target-abort sequences on the PCI bus.
PDEVSEL#	3.3V/5V	MAIN	I/O	Device Select: As a PCI target, SiS55x asserts PDEVSEL# by doing positive or subtractive decoding. SiS55x positively asserts PDEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M-byte memory space are responded subtractively. The PDEVESEL# is an input pin when SiS55x is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PLOCK#	3.3V/5V	MAIN	I/O	PCI Lock: When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS55x considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.

PREQ [2:0]#	3.3V/5V	MAIN	I	PCI Bus Request: PCI Bus Master Request Signals: All these pins should pull high even the corresponding PCI slot is not mounted
PGNT [2:0]#	3.3V	MAIN	O	PCI Bus Grant: PCI Bus Master Grant Signals
INT[A:D]#	3.3V/5V	MAIN	I	PCI interrupt A, B, C, D: The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PCIRST#	3.3V	AUX	O	PCI Bus Reset: PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
PSERR#	3.3V/5V	MAIN	I	System Error: When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.

3.4.4 PCI IDE Interface

Name	Tolerance	Power Plane	Type Attr.	Description
IDA[15:0]	3.3V/5V	MAIN	I/O	Data Bus
IDECS [1:0]#	3.3V	MAIN	O	Chip Select
IIOR#	3.3V	MAIN	O	IOR# Signals
IIOW#	3.3V	MAIN	O	IOW# Signals
ICHRDY	3.3V/5V	MAIN	I	CHRDY# Signals
IDREQ	3.3V/5V	MAIN	I	DMA Request Signals
IDACK#	3.3V	MAIN	O	DMACK# Signals
IIRQ	3.3V/5V	MAIN	I	Interrupt Signals

IDESA [2:0]	3.3V	MAIN	O	Address [2:0]
CBLID	3.3V/5V	MAIN	I	Ultra-66 Cable ID

3.4.5 VGA Interface

Name	Tolerance	Power Plane	Type Attr.	Description
ROUT	3.3V	MAIN	AO	Red video signal output
GOUT	3.3V	MAIN	AO	Green video signal output
BOUT	3.3V	MAIN	AO	Blue video signal output
VRSET	3.3V/5V	MAIN	AI	Reference resistor
VBWN	3.3V/5V	MAIN	AI	Voltage reference
VCOMP		MAIN	AI	Compensation pin
HSYNC	3.3V/5V	MAIN	O	Horizontal sync
VSYNC	3.3V/5V	MAIN	O	Vertical sync
PCLK	3.3V/5V	MAIN	I/O	Pixel clock/Video input port clock
VIDEO[7:0]	3.3V/5V	MAIN	I/O	Video Data Bus
CSYNC	3.3V/5V	MAIN	O	Reserved
LSYNC	3.3V	MAIN	O	Reserved
RSYNC	3.3V	MAIN	O	Reserved
DDC1DATA	3.3V	MAIN	I/O	Display Data Channel 1 Data Line
DDC1CLK	3.3V	MAIN	I/O	Display Data Channel 1 Clock Line
DDC2DATA	3.3V	MAIN	I/O	Display Data Channel 2 Data Line
DDC2CLK	3.3V	MAIN	I/O	Display Data Channel 2 Clock Line
DDC3DATA	3.3V	MAIN	I/O	Display Data Channel 3 Data Line
DDC3CLK	3.3V	MAIN	I/O	Display Data Channel 3 Clock Line
VAHSYNC	3.3V	MAIN	O	Horizontal sync of VB primary channel
VAVSYNC	3.3V	MAIN	O	Vertical sync of VB primary channel

VADE	3.3V	MAIN	O	Data valid of VB primary channel
VAGCLK	3.3V	MAIN	O	Clock output to VB primary channel
VAD[11:0]	3.3V	MAIN	O	Primary digit data output channel
VBHSYNC	3.3V	MAIN	O	Horizontal sync of VB secondary channel
VBVSYNC	3.3V	MAIN	O	Vertical sync of VB secondary channel
VBDE	3.3V	MAIN	O	Data valid of VB secondary channel
VBCLK	3.3V	MAIN	I	Clock input from VB secondary channel
VBGCLK	3.3V	MAIN	O	Clock output to VB secondary channel
VBCAD	3.3V	MAIN	I/O	VB host command, address and data signal
VBHCLK	3.3V	MAIN	O	VB host clock output
VBCTL[1:0]	3.3V	MAIN	O	VB control signals
VBD[11:0]	3.3V	MAIN	O	Secondary digit data output channel
PLDXCLK	3.3V	MAIN	O	DSTN interface dot clock
PLDXDISPOFFN	3.3V	MAIN	O	DSTN disable panel
PLDXVDDEN	3.3V	MAIN	O	DSTN control LCD VDD FET
PLDXVCONEN	3.3V	MAIN	O	DSTN control LCD bois voltage enable
PLDXDU[7:4]	3.3V	MAIN	O	DSTN data bit [7:4]
VOSCI		MAIN	I	Reference clock 14.131818MHz input
PWRSTN	3.3V/5V	MAIN	I	Power on reset of clock generator

3.4.6 Power Management Interface

Name	Tolerance	Power Plane	Type Attr.	Description
ACPILED	<=5V	AUX	OD	ACPILED: ACPILED can be used to control the blinking of an LED at the frequency of 1 Hz to indicate the system is at power saving mode.
EXTSMI#	3.3V/5V	MAIN	I	External SMI#: EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI#/GPEIRQ event to the ACPI-compatible power management unit.
THERM#	3.3V/5V	MAIN	I	Thermal Detect: THERM# is connected to the internal ACPI-compatible power management unit as an indication of outstanding thermal event. An active THERM# event can be used to generate SCI/SMI#/GPEIRQ. If THERM# is activated for more than 2 second, a thermal override event will occur and the system will enter CPU thermal throttling mode automatically.

PME#	3.3V/5V	AUX	I/O	PME#: When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#/GPEIRQ.
PSON#	<=5V	AUX	OD	ATX Power ON/OFF control: PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
PWRBTN#	3.3V/5V	AUX	I	Power Button: This signal is from the power button switch and will be monitored by the ACPI-compatible power management unit to switch the system between working and sleeping states.
RING	3.3V/5V	AUX	I	Ring Indication: An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.

3.4.7 Keyboard Controller Interface

Name	Tolerance	Power Plane	Type Attr.	Description
KBDAT	3.3V/5V	AUX	I/OD	Keyboard Dada: When the internal keyboard controller is enabled, this pin is used as the keyboard data signal.
KBCLK	3.3V/5V	AUX	I/OD	Keyboard Clock: When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal.
PMDAT	3.3V/5V	AUX	I/OD	PS/2 Mouse Data: When the internal keyboard and PS/2 mouse controllers are enabled, this pin is used as PS/2 mouse data signal.
PMCLK	3.3V/5V	AUX	I/OD	PS/2 Mouse Clock: When the internal keyboard and PS/2 mouse controllers are enabled, this pin is used as the PS/2 mouse clock signal.
KLOCK#	3.3V/5V	AUX	I	Keyboard Lock: When KLOCK# is tied low, the internal keyboard controller will not respond to any key-strikes.

3.4.8 LPC Interface

Name	Tolerance	Power Plane	Type Attr.	Description
LAD[3:0]	3.3V/5V	MAIN	I/O	LPC Address/Data Bus: LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.

LDRQ#	3.3V/5V	MAIN	I	LPC DMA Request 0: This pin is used by LPC device to request DMA cycle.
LDRQ1#	3.3V/5V	MAIN	I	LPC DMA Request 1: LDRQ1# is the second LPC DMA request signal used by LPC Device to request DMA cycles.
LFRAME#	3.3V	MAIN	O	LPC Frame: This pin is used to notify LPC device that a start or an abort LPC cycle will occur.
SIRQ	3.3V/5V	MAIN	I/OD	Serial IRQ: This signal is used as the serial IRQ line signal.

3.4.9 RTC Interface

Name	Tolerance	Power Plane	Type Attr.	Description
AUXOK	3.3V	RTC	I	Auxiliary Power OK: This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
BATOK	3.3V	RTC	I	Battery Power OK: When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.

OSC32KHI	3.3V	RTC	I	RTC 32.768 KHz Input: When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	<3.3V	RTC	O	RTC 32.768 KHz Output: When internal RTC is enabled, this pin should be connected the other end of the 32.768 KHz crystal or left unconnected if an oscillator is used.
PWROK	3.3V	RTC	I	Main Power OK: A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes to high for 24 ms.

3.4.10 Audio Interface

Name	Tolerance	Power Plane	Type Attr.	Description
AC_BIT_CLK	3.3V/5V	MAIN	I	AC'97 Bit Clock: This signal is a 12.288MHz serial data clock, which is generated by primary CODEC.
AC_RESET#	3.3V	AUX	O	AC'97 Reset: Hardware reset signal for external CODECs.
AC_SDIN[2:0]	3.3V/5V	AUX	I	AC'97 Serial Data input: Serial data input from primary CODEC and secondary CODEC.

AC_SDOUT	3.3V	MAIN	O	AC'97 Serial Data output: Serial data output to CODECs.
AC_SYNC	3.3V	MAIN	O	AC'97 Synchronization: This is a 48KHz signal, which is used to synchronize the CODECs.
CDA	3.3V/5V	MAIN	O	Consumer Digital Audio i/f
CLK66M	3.3V/5V	MAIN	I	Audio 66 MHz clock input: This signal provides the fundamental clock for audio.

3.4.11 Memory Stick Interface

Release only to SONY's licensees.

3.4.12 USB Interface

Name	Tolerance	Power Plane	Type Attr.	Description
USBCLK48M	3.3V/5V	MAIN	I	USB 48 MHz clock input: This signal provides the fundamental clock for the USB Controller.
OC[2:0]#	3.3V/5V	MAIN	I	USB Port [2:0] Over Current Detection: OC[2:0]# is used to detect the over current condition of USB Port [2:0].
UV[2:0]+	3.3V	AUX	I/O	USB Port [2:0] Positive Input/Output
UV[2:0]-	3.3V	AUX	I/O	USB Port [2:0] Negative Input/Output

3.4.13 Smart Card Interface

Name	Tolerance	Power Plane	Type Attr.	Description
RCLK	3.3V/5V	AUX	O	Smart Card Clock Output
RADD[15:0]	3.3V/5V	AUX	O	Smart Card Controller External Rom Address Bus

RDAT[7:0]	3.3V/5V	AUX	I	Smart Card Controller External Rom Data Bus
RGPIO[3:0]	3.3V/5V	AUX	I/O	Smart Card Controller GPIO

Note: RADD[3:0] are used as hardware trapping pins in the selection of CIR decoder type.

0000 Forward-Coded Decoder
0001 Space-Coded Decoder
0010 Pulse-Coded Decoder
0011 Silitek-Coded Decoder
0100 Chicony1-Coded Decoder
0101 BTC-Coded Decoder
0110 Chicony2-Coded Decoder
0111~1110 Reserved
1111 Software Decoder

3.4.14 ROM Interface

Name	Tolerance	Power Plane	Type Attr.	Description
SA[19:0]	3.3V	MAIN	O	ROM Address: ROM interface Address signal. SA[21:20] is multi-functioned with GPIO[11:10]. See Section 6.6.
SD[7:0]	3.3V/5V	MAIN	I/O	ROM Data: ROM interface data signals.
MRDCL	3.3V	MAIN	O	ROM Read: ROM interface read signal.
MWTCL	3.3V	MAIN	O	ROM Write: ROM interface write signal.
ROMCS[1:0]	3.3V	MAIN	O	ROM Chip Select: ROM interface chip select signal. ROMCS[3:2] is multi-functioned with GPIO[8:9]. See Section 6.6.

3.4.15 Parallel Port

Name	Tolerance	Power Plane	Type Attr.	Description
PD[7:0]	3.3V	MAIN	O	Parallel Port Data: Printer port data signals.

STB#	3.3V	MAIN	O	STROBE: Strobe the printer port data into the printer
AFD#	3.3VV	MAIN	O	Auto Feed: Inform printer advance one line after each line is printed.
ERR#	3.3V/5V	MAIN	I	Error: Indicate that printer encounter an error.
PRINIT#	3.3V	MAIN	O	Printer Initial: Initial the printer.
SLIN#	3.3V	MAIN	O	AC'97 Synchronization: This is a 48KHz signal, which is used to synchronize the CODECs.
ACK#	3.3V/5V	MAIN	I	Acknowledge: Indicate that the printer has received a character and is ready to accept next.
BUSY	3.3V/5V	MAIN	I	Busy: Indicate that the printer is not ready to accept data.
PE	3.3V/5V	MAIN	I	Paper End: Indicate that the printer has run out of paper.
SLCT	3.3V/5V	MAIN	I	Select: Printer is selected.

3.4.16 CIR Interface

Name	Tolerance	Power Plane	Type Attr.	Description
CIRRX	3.3V	AUX	I	Consumer IR received data.

3.4.17 Legacy I/O and Miscellaneous Signals

Name	Tolerance	Power Plane	Type Attr.	Description
GPIO[7:0]	3.3V/5V	AUX	I/O	General Input/Output signal

GPIO[11:8]	3.3V/5V	MAIN	I/O	General Input/Output signal
SPK	3.3V	MAIN	O	Speaker output: The SPK is connected to the system speaker.
INTRUDER	3.3V	RTC	I	This signal can be used to detect if the system case has been opened.
ENTEST	3.3V	MAIN	I	Test Mode Enable Pin
OSCI	3.3V	MAIN	I	14.318 MHz. Clock In

3.4.18 SMBus Interface

Name	Tolerance	Power Plane	Type Attr.	Description
SMBDAT	3.3V	MAIN	I/OD	SMBus Data
SMBCLK	3.3V	MAIN	I/OD	SMBus Clock
SMBALT	3.3V	AUX	I	SMBus Alert

3.4.19 Power and Ground Signals

Vcore = 1.9V, 1.8V, or 1.7V, depending on the selected Vcore level described in Section 7.2.3.

Name	Tolerance	Power Plane	Type Attr.	Description
IVDD		MAIN		*Vcore*
OVDD		MAIN		3.3V
PVDD		MAIN		3.3V
OVDDM		MAIN		3.3V
AUX1.8		AUX		*Vcore*
AUX3.3		AUX		3.3V
USBVDD		AUX		3.3V
RTCVDD		RTC		3.3V
DCLKAVDD		MAIN		3.3V
ECLKAVDD		MAIN		3.3V
DACAVDD1		MAIN		*Vcore*
DACAVDD2		MAIN		*Vcore*
R1PLLAVDD_18		MAIN		*Vcore*
R1PLLVADD_33		MAIN		3.3V
IDEAVDD		MAIN		*Vcore*

SDAVDD		MAIN		3.3V
CPUAVDD		MAIN		3.3V
VSS		GND		0V
OVSSM		GND		0V
DACAVSS1		GND		0V
DACAVSS2		GND		0V
R1PLLAVSS_18		GND		0V
R1PLLVASS_33		GND		0V
CPUAVSS		GND		0V
RTCVSS		GND		0V
IDEAVSS		GND		0V
SDAVSS		GND		0V
ECLKAVSS		GND		0V
DCLKAVSS		GND		0V

4 Programming SiS55x

SiS55x programming is composed of programming the processor and the other integrated functions. The processor programming is almost fully compatible with Intel Pentium, thus we list only the difference between SiS55x and Pentium in next sub-section. All the other integrated functions can be programmed by accessing the registers on the PCI space. Section 4.2 discusses the programming way, and the registers are listed in another document “SiS55x Family Registers”.

4.1 Difference between SiS55x and Pentium

The difference of programming SiS55x and Intel Pentium includes CPUID, Control Register CR4, Initial States and Feature Control Registers (FCR). Following sub-sections describes the first three. The FCR is reserved for SiS internal reference.

4.1.1 CPUID

The CPUID instruction is supported on the SiS55x, and return values for the CPUID instruction are shown in Table 4-1 through Table 4-3. For comparison, the Intel P55C processor return values are included in the tables.

Table 4-1. CPUID Return Values with EAX==0

REGISTER	SiS55x	Intel P55C
EAX	1	1
EBX:ECX:EDX	SiS SiS SiS (20536953h:20536953h:20536953h)	GenuineIntel

Table 4-2. CPUID EAX Return values with EAX==1

PROCESSOR	[13:12] Type ID	[11:8] Family ID	[7:4] Model ID	[3:0] Stepping ID
SiS55x	0	5	0	5
Intel P55C	0	5	4	Varies

Table 4-3. CPUID EDX Return Values with EAX==1

EDX Bits – Meaning	SiS55x	Intel P55C	Notes
0 – FP present	1	1	
1 – VM86 Extensions (VME)	0	1	
2 – Debugging Extensions	0	1	
3 – Page Size Extensions	0	0	
4 – Time Stamp Counter (TSC) supported	1	1	
5 – Model Specific Registers present	0	1	

6 – PAE supported	0	0	
7 – Machine Check Exception	0	1	
8 – CMPXCHG8B instruction	1	1	
9 – APIC supported	0	1	
10:11 – RESERVED	-	-	
12 – Memory Range Registers	0	0	
13 – PTE global Bit supported	0	0	
14 – Machine Check Architecture supported	0	0	
15 – Conditional Move supported	0	0	
16:22 – RESERVED	-	-	
23 – MMX supported	1	1	
24:31 – RESERVED	-	-	

4.1.2 CPU Speed Detection

The SiS55x supports the Time Stamp Counter and the RDTSC instruction. BIOS algorithms may use this facility to measure timed operations for CPU speed detection. During system boot, BIOS detects and displays the speed/ratio for the processor.

4.1.3 Control Register CR4

The Pentium processor introduced a new control register (CR4) for controlling many of its new model-specific architectural features. The SiS55x processor provides a CR4 register compatible with the Pentium processor; however, it does not implement all of the model-specific features that can be controlled through the CR4 register. The CPUID instruction should be used to determine the features supported by the SiS55x.

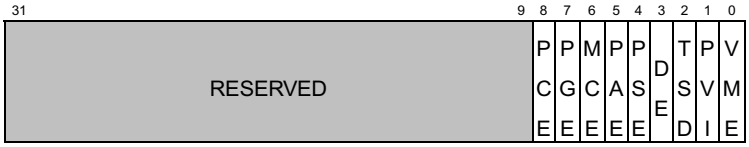


Figure 4-1. Control Register CR4 Bit Assignments.

Bits **VME**, **PVI**, **PSE**, **MCE**, **PGE** and **PCE** are not supported on the SiS55x. These six bits return a value of 0 when read and although they cannot be set, no GP exception occurs on attempts to set them.

The **DE** bit is reserved on the SiS55x. The return value when this bit is read and its response to attempts to set it are both undefined; however, no GP exception occurs on attempts to set or clear it.

4.1.4 SiS55x RESET and INIT States

The state of each register of the SiS55x after signals RESET or INIT is listed in Table 4-4.

Table 4-1. SiS55x Achitectual Sate after RESET or INIT

REGISTER	RESET State	INIT State 1	NOTES
EFLAGS	00000002H		2
EIP	0000FFF0H		
CS	Selector = F000H Base = FFFF0000H Limit = FFFFH AR = Present, R/W, Accessed		
SS, DS, ES, FS, GS	Selector = 0000H Base = 00000000H Limit = FFFFH AR = Present, R/W, Accessed		
EAX	00000000H		3
EDX	00000505H		4
EBX, ECX, ESI, EDI, EBP, ESP	00000000H		
GDTR, IDTR	Base = 00000000H Limit = FFFFH AR = Present, R/W		
LDTR, Task Register	Selector = 0000H Base = 00000000H Limit = FFFFH AR = Present, R/W		
FPU Stack ST7-ST0	00000000000000000000H (+0.0)	Unchanged	
FPU Control Word	0040H	Unchanged	
FPU Status Word	0000H	Unchanged	
FPU Tag Word	5555H	Unchanged	
FPU Instruction Pointer	000000000000H	Unchanged	
FPU Data Pointer	000000000000H	Unchanged	
CR0	60000010H		5
CR2, CR3, CR4	00000000H		
DR7	00000400H		
DR6	FFFF0FF0H		
DR0, DR1, DR2, DR3	00000000H		

Data and Code Cache	Invalid	Unchanged	
TLBs	Invalid	Invalid	
TSC	0	Unchanged	
FCR0	340290A0H		
FCR1	00800000H		

Notes:

1. Unless otherwise specified, the INIT state is the same as the RESET state.
2. Software should not depend on the states of the 10 most significant bits of the EFLAGS register following a reset.
3. The EAX register contains the results of the Built In Self Test (BIST) when invoked. If EAX = 00000000H then BIST completed successfully. If EAX is non-zero then BIST failed.
4. The EDX register contains the SiS55x identification and revision information.
5. The CD and NW flags are unchanged following INIT, bit 4 is set to 1, and all other bits are cleared.

4.2 Programming Integrated Functions

All the SiS55x integrated functions can be programmed by accessing the registers on the PCI space. These registers are accessed by issuing PCI commands via two visible registers in I/O space: the address register CONFIG_ADDR (0CF8h) and the data register CONFIG_DATA (0CFCh). The programming way is discussed in another document “SiS55x Family Registers”. The following table lists the identify way of these function in the PCI command.

Table 4-1. Function Block Reference

Bus #	Device #	Function #	Device ID	IDSEL	Device Function
Bus 0	Device 0	Function 0	0550h	AD11	North Bridge
Bus 0	Device 0	Function 1	5513h	AD11	PCI IDE
Bus 1	Device 0	Function 0	5315h	AD11	GUI
Bus 0	Device 1	Function 0	0008h	AD12	LPC
Bus 0	Device 1	Function 1	7005h	AD12	Memory Stick
Bus 0	Device 1	Function 2	7001h	AD12	USB
Bus 0	Device 1	Function 4	7019h	AD12	H/W Audio
Bus 0	Device 1	Function 5	7015h	AD12	S/W Modem
Bus 0	Device 2	Function 0	0001h	AD13	Virtual PCI-to-PCI Bridge

5 Hardware Trap

There are some pins used for trapping purpose to identify the hardware configurations at the power-up stage. These pins will be recognized as “1” if pull-up resistors are used; and will be recognized as “0” if pull-down resistors are used.

The following table is a summary of all the Hardware Trap pins in SiS55x.

Table 5-1. Hardware Trap by MD Lines

Name	Description
MD63	Reserved for IDE
MD62	PCI Clock PLL Enable 0: Enable (Recommend) 1: Disable
MD61	SDRAM Clock DLL Enable 0: Enable (Recommend) 1: Disable
MD60	CPU Clock DLL 0: Enable (Recommend) 1: Disable
MD[59:54]	Reserved
MD[53:47]	Reserved for GUI
MD48	Reserved for internal testing
MD[47:42]	Reserved for South Bridge
MD41	ROM Interface Select 0: Built-in ROM interface 1: Forward to LPC bus
MD40	Auto Reset Function 0: Disable 1: Enable
MD39	GUI Supports APCI Power State D2 0: Disable 1: Enable
MD38	VGA Interrupt Function (INTA) Enable 0: Disable 1: Enable
MD[37:36]	Reserved for GUI

MD35	GUI Multi-Function Enable 0: Disable 1: Enable
MD34	GUI Multi-Function Select 0: Select Function 0 1: Select Function 1
MD33	Video Bridge Enable 0: Disable 1: Enable
MD32	TV Type (PAL/NTSC) Select 0: Select NTSC system 1: Select PAL system

Note:

1. There are internal pull-down resistors on MD lines.
2. Reserved pins are used for SiS internal reference only.

Hardware Trap for CIR protocol by RADD lines:

RADD[3:0]	Description
0000	Forward
0001	Reserved
0010	Reserved
0011	Silitek
0100	Chicony1
0101	BTC
0110	Chicony2
0111~1111	Reserved

6 Function Description

6.1 MA Mapping Table

6.1.1 SDRAM/System Memory

SDRAM TYPE		(NBAXNRAXNCA)															
		1X11X8	1X13X8	2X12X8	2X13X8	1X11X9	1X13X9	2X12X9	2X13X9	1X11X10	1X13X10	2X12X10	2X13X10	2X11X8	1X13X11	2X12X11	2X13X11
DIMM	SDM chip	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA
MA0	MA0	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
MA1	MA1	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
MA2	MA2	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
MA3	MA3	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
MA4	MA4	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
MA5	MA5	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
MA6	MA6	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
MA7	MA7	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@	10@
MA8	MA8					23#/23	23	23	23	23	23	23	23		23	23	23
MA9	MA9									24#/24	24	24	24		24	24	24
MA10	AP	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]
MA11	BA0	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
MA12	BA1	[0]	[0]	12	12	[0]	[0]	12	12	[0]	[0]	12	12	12	[0]	12	12
MA13	MA11														27#/27	27#/27	27
MA14	MA12																
SIDE-MA	(SINGLE/ DOUBLE)	[0]/12	[0]/12	[0]/13	[0]/13	[0] /12	[0]/ 12	[0]/13	[0]/13	[0]/12	[0]/12	[0]/13	[0]/ 13	[0]/13	[0]/12	[0]/13	0]/13

SDRAM TYPE		(NBAXNRAXNCA)															
		1X11 X8	1X13 X8	2X12 X8	2X13 X8	1X11 X9	1X13 X9	2X12 X9	2X13 X9	1X11 X10	1X13 X10	2X12 X10	2X13 X10	2X11 X8	1X13 X11	2X12 X11	2X13 X11
DIMM	SDM chip	RA	RA	RA	RA	RA	RA	RA	RA	RA	RA	RA	RA	RA	RA	RA	RA
MA0	MA0	13	13	13/25#	13/26#	13	13	13/26#	13/27#	13	13	13/27#	13/ 28#	13/ 24#	13	13/ 28#	13/ 29#
MA1	MA1	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14	14
MA2	MA2	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15
MA3	MA3	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
MA4	MA4	17	17	17	17	17	17	17	17	17	17	17	17	17	17	17	17
MA5	MA5	18	18	18	18	18	18	18	18	18	18	18	18	18	18	18	18
MA6	MA6	19	19	19	19	19	19	19	19	19	19	19	19	19	19	19	19
MA7	MA7	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
MA8	MA8	21	21	21	21	21	21	21	21	21	21	21	21	21	21	21	21
MA9	MA9	22#/22	22	22	22	22	22	22	22	22	22	22	22	22	22	22	22
MA10	AP	12/23#	12/25#	23	23	12/24#	12/26#	25#/25	25	12/25#	12/27#	25	27#/27	23#/23	12/28#	25	25
MA11	BA0	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
MA12	BA1	[0]	[0]	12	12	[0]	[0]	12	12	[0]	[0]	12	12	12	[0]	12	12
MA13	MA11		24#/ 24	24#/ 24	24		24	24	26#/ 26		26#/ 26	26#/ 27	26		26	26	26
MA14	MA12		23		25#/ 25		25#/ 25		24		25		25		25		28#/ 28
Rank Size		8MB	32MB	32MB	64MB	16MB	64MB	64MB	128MB	32MB	128MB	128MB	256MB	16MB	256MB	256MB	512MB
System Reg.		{0000}	{0001}	{0010}	{0011}	{0100}	{0101}	{0110}	{0111}	{1000}	{1001}	{1010}	{1011}	{1100}	{1101}	{1110}	{1111}

Note: 1. @ for page hit comparator, #for rank decoder.

2. Constant Page Size: 2K byte (4Kbyte for GUI-128 BITs ACCESS).

3. A1/A2: A1 for single sided DIMM, A2 for double-sided DIMM.

6.1.2 SDRAM/FBC

SDRAM TYPE		(NBAXNRAXNCA)							
		1x9x8	*1x10x8*	*1X11X8*	*2X12X8*	1X11X9	1X11X10	2X11X8	*1X12X8*
DIMM	SDM chip	CA	CA	CA	CA	CA	CA	CA	CA
MA0	MA0	3	3	3	3	3	3	3	3
MA1	MA1	4	4	4	4	4	4	4	4
MA2	MA2	5	5	5	5	5	5	5	5
MA3	MA3	6	6	6	6	6	6	6	6
MA4	MA4	7	7	7	7	7	7	7	7
MA5	MA5	8	8	8	8	8	8	8	8
MA6	MA6	9	9	9	9	9	9	9	9
MA7	MA7	10@	10@	10@	10@	10@	10@	10@	10@
MA8	MA8					23#	23		
MA9	MA9						24#		
MA10	AP	[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]
MA11	BA0	11	11	11	11	11	11	11	11
MA12	BA1	[0]	[0]	[0]	12	[0]	[0]	12	[0]
MA13	MA11								
MA14	MA12								

SDRAM TYPE		(NBAXNRAXNCA)							
		1x9x8	*1x10x8*	*1X11X8*	*2X12X8*	1X11X9	1X11X10	2X11X8	*1X12X8*
DIMM	SDM chip	RA	RA	RA	RA	RA	RA	RA	RA
MA0	MA0	13	13	13	13	13	13	13	13
MA1	MA1	14	14	14	14	14	14	14	14
MA2	MA2	15	15	15	15	15	15	15	15
MA3	MA3	16	16	16	16	16	16	16	16
MA4	MA4	17	17	17	17	17	17	17	17
MA5	MA5	18	18	18	18	18	18	18	18
MA6	MA6	19	19	19	19	19	19	19	19
MA7	MA7	20#	20	20	20	20	20	20	20
MA8	MA8		21#	21	21	21	21	21	21
MA9	MA9			22#	22	22	22	22	22
MA10	AP	12	12	12	23	12	12	23#	12
MA11	BA0	11	11	11	11	11	11	11	11
MA12	BA1	[0]	[0]	[0]	12	[0]	[0]	12	[0]
MA13	MA11				24#				23#
MA14	MA12								
Rank Size		2MB	4MB	8MB	32MB	16MB	32MB	16MB	16MB
System Reg.		{0000}	{0001}	{0010}	{0011}	{0100}	{0101}	{0110}	{0111}

Note: 1. Additional Configurations: 1x9x8, 1x10x8, 1x12x8, and the other configurations are the same as system configurations

2. Additional Pins for 128-bit solution are “GUI_AP”,”GUI_BA1”, and ”GUI_MA11”

6.1.3 VCM/System Memory

VC SDRAM TYPE	(NBAXNRAXNCAXNSA)		
	1X13X6X2	1X13X7X2	1X13X8X2
	CA	CA	CA
MA0	3	3	3
MA1	4	4	4
MA2	5	5	5
MA3	6	6	6
MA4	7	7	7

MA5	8@	8	8
MA6	(9)*	9@	9
MA7	(10)*	(10)*	10@
MA8(CH0)			
MA9(CH1)			
MA10/AP	[0]	[0]	[0]
MA11/BA0(BA)	[0]	[0]	[0]
MA12/BA1	[0]	[0]	[0]
MA13/MA11(CH2)			
MA14/MA12(CH3)			

VC SDRAM TYPE	(N**BA**XN**RA**XN**CA**XN**SA**)		
	1X13X6X2	**1X13X7X2**	**1X13X8X2**
	SA	**SA**	**SA**
MA0(SEG0)	11	11	11
MA1(SEG1)	12	12	12
MA2			
MA3			
MA4			
MA5			
MA6			
MA7			
MA8(CH0)			
MA9(CH1)			
MA10/AP	[1]	[1]	[1]
MA11/BA0(BA)	13	13	13
MA12/BA1			
MA13/MA11(CH2)			
MA14/MA12(CH3)			
MA-CS	[0] /14	[0] /14	[0]/14

VC SDRAM TYPE	(N**BA**XN**RA**XN**CA**XN**SA**)		
	1X13X6X2	**1X13X7X2**	**1X13X8X2**
	RA	**RA**	**RA**
MA0	15	15	15
MA1	16	16	16

MA2	17	17	17
MA3	18	18	18
MA4	19	19	19
MA5	20	20	20
MA6	21	21	21
MA7	22	22	22
MA8	23	23	23
MA9	24	24	24
MA10/AP	9	25	25
MA11/BA0	13	13	13
MA12/BA1			
MA13/MA11	14 / 25	14 / 26	14 / 27
MA14/MA12	10	10	26
Rank/DIMM Size	32MB	64MB	128MB
System Reg.	{0000}	{0001}	{0010}

Note: 1. @ for boundary page hit comparator, #for rank decoder.

Page Size is programmable (0.5k, 1k, 2k), and constant for all VC-SDRAM rank.

2. A1/A2: A1 for single sided DIMM or 128-bit mode, A2 for double-sided & 64-bit mode.

6.1.4 VCM/FBC

VC SDRAM	
TYPE	1X13X6X2
	CA
MA0	**3**
MA1	**4**
MA2	**5**
MA3	**6**
MA4	**7**
MA5	**8**
MA6	(9)*
MA7	(10)*
MA8(CH0)	
MA9(CH1)	
MA10/AP	[0]
MA11/BA0(BA)	[0]
MA12/BA1	[0]
MA13/MA11(CH2)	
MA14/MA12(CH3)	

VC SDRAM	
TYPE	1X13X6X2
	SA
MA0(SEG0)	**11**
MA1(SEG1)	**12**
MA2	
MA3	
MA4	
MA5	
MA6	
MA7	
MA8(CH0)	
MA9(CH1)	
MA10/AP	[1]
MA11/BA0(BA)	**13**
MA12/BA1	
MA13/MA11(CH2)	
MA14/MA12(CH3)	
MA14/MA12(CH3)	

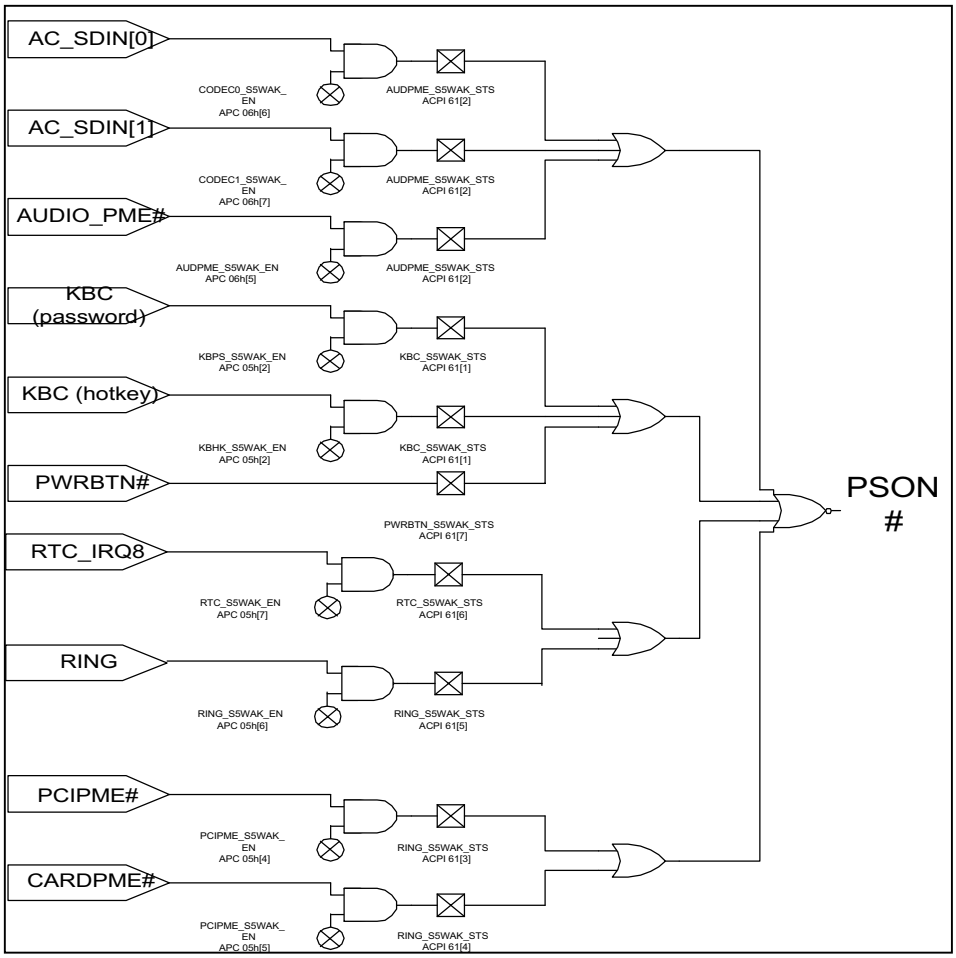
VC SDRAM	
TYPE	1X13X6X2
	RA
MA0	**15**
MA1	**16**
MA2	**17**
MA3	**18**
MA4	**19**
MA5	**20**
MA6	**21**
MA7	**22**
MA8	**23**
MA9	**24**
MA10/AP	**9**
MA11/BA0	**13**
MA12/BA1	
MA13/MA11	**14**
MA14/MA12	**10**

GUI Size: 32MB

GUI Reg. {0000}

6.2 PSON# and ACPILED Description:

Pin Name	Buffer Type	Description
PSON#	Auxiliary / Open Drain	PS_ON# is an active low signal that turns on all of the main power rails. When a power-up event occurs, SiS55x would assert PSON# to turn on the power supply. When a power-down event occurs, SiS55x would de-assert PSON# to turn off the power supply. This signal should be held at +5VDC by a pull-up resistor internal to the power supply.



Pin Name	Buffer Type	Description
ACPILED	Auxiliary/ Open Drain	ACPILED is used to denote that the computer is in the sleep mode.

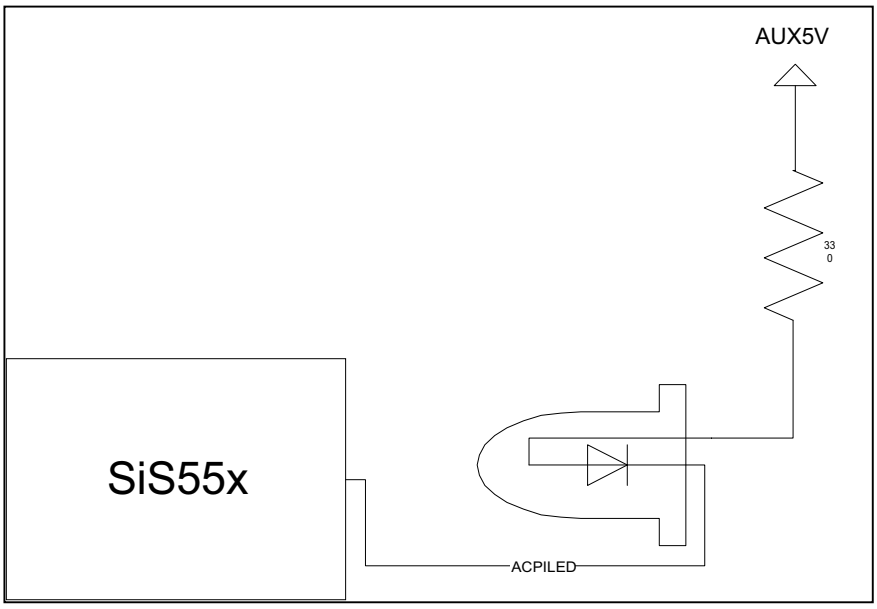
6.3 ACPILED Control

Register 62h~63h System Wakeup form S3/S4/S5 Control Register (S5WAK_CNT)

Default Value: 0000h

Access: Read/Write

7:6	RO	ACPILED Output State Control The output state of ACPILED can be controlled by the following combination when system is in S0/S1/S2/S3 states. If the system is in S4/S5 state, ACPILED will be set to high impedance. 00: Output low 01: Blink 10: High impedance 11: Reserved



6.4 Power States for SiS55x Signals

Term	Pin Type	Description
In	INPUT	When PCIRST# is asserted, the I/O pin would be set to input mode.
Fixed	INPUT	Can't be changed.
Driven	INPUT	The pin is driven by external resistors and may change its logic value.
--	INPUT	The logic value of the input pin is independent of PCIRST#.
Running	INPUT/OUTPUT	Clocks.
High	INPUT/OUTPUT	SiS55x drives the pin to a logic high level, or the pin is driven to a high logic level by external components.
Low	INPUT/OUTPUT	SiS55x drives the pin to a logic low level, or the pin is driven to a low logic level by external components.
Defined	OUTPUT	SiS55x drives the pin to a logic level that depends on the function.
Off	OUTPUT	The output buffer is powered off.
High-Z	OUTPUT	The output buffer is high impedance.

Signal Name	Buffer Type	Power Plane	During PCIRST#	After PCIRST#	S1	S3	S4/S5
PCI Interface							
PCICLK	I	Core	Running	Running	Running	Low	Low
PSERR#	I	Core	--	--	High	Low	Low
INT[A:D]#	I	Core	--	--	Driven	Low	Low
AD[31:0]	I/O	Core	High-Z	High	High-Z	Off	Off
PC/BE[3:0]#	I/O	Core	High-Z	High	High-Z	Off	Off
PFRAME#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
PIRDY#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
PTRDY#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
PDEVSEL#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
PSTOP#	I/O	Core	High-Z	High-Z	High-Z	Off	Off
PPAR	I/O	Core	High-Z	Low	Low	Off	Off
PCIRST#	O	Resume	Low	High	High	Low	Low
ACPI							

PWRBTN#	I	Resume	Driven	Driven	Driven	Driven	Driven
EXTSMI#	I	Core	Driven	Driven	Driven	Low	Low
THERM#	I	Core	Driven	Driven	Driven	Low	Low
RING	I	Resume	Driven	Driven	Driven	Driven	Driven
PME#	I	Resume	Driven	Driven	Driven	Driven	Driven
PSON#	OD	Resume	Low	Low	Low	High	High
CKE	O	Resume	High-Z	High-Z	High-Z	Low	High-Z
ACPILED	OD	Resume	High-Z	High-Z	High-Z	Defined	High-Z
LPC Interface							
LAD[3:0]	I/O	Core	High	High	High	Off	Off
LFRAME#	O	Core	High	High	High	Off	Off
LDRQ[1:0]#	I	Core	--	--	High	Low	Low
CIR							
CIRRX	I	Resume	Driven	Driven	Driven	Driven	Driven
RTC							
OSC32KHI	I	RTC	Running	Running	Running	Running	Running
OSC32KHO	O	RTC	Running	Running	Running	Running	Running
PWROK	I	RTC	High	High	High	Low	Low
AUXOK	I	Resume	High	High	High	High	High
BATOK	I	RTC	High	High	High	High	High
INTRUDER	I	RTC	Driven	Driven	Driven	Driven	Driven
Audio Modem Interface							
AC_RESET#	O	Resume	Low	Low	Defined	Low	Low
AC_SYNC	O	Core	Low	Low	Low	Off	Off
AC_BIT_CLK	I	Core	--	--	Low	Low	Low
AC_SDIN[2:0]	I	Resume	Driven	Driven	Driven	Driven	Driven
USB Interface							
OC#[2:0]	I	Core	High	High	High	Off	Off
USBCLK48M	I	Core	Running	Running	Running	Low	Low
Legacy I/O							
SPK	O	Core	Low	Low	Low	Off	Off
CDA	O	Resume	Low	Low	Low	Off	Off
SIRQ	I/O	Core	High-Z	High-Z	High-Z	Off	Off
GPIO							
GPIO0	I/O/OD	Resume	In	In	Defined	Off	Off
GPIO1	I/O/OD	Resume	In	In	Defined	Off	Off

GPIO2	I/O/OD	Resume	In	In	Defined	Off	Off
GPIO3	I/O/OD	Resume	In	In	Defined	Off	Off
GPIO4	I/O/OD	Resume	In	In	Defined	Off	Off
GPIO5	I/O/OD	Resume	In	In	Defined	Off	Off
GPIO6	I/O/OD	Resume	In	In	Defined	Off	Off
GPIO7	I/O/OD	Resume	In	In	Defined	Off	Off
GPIO8	I/O/OD	Core	In	In	Defined	Off	Off
GPIO9	I/O/OD	Core	In	In	Defined	Off	Off
GPIO10	I/O/OD	Core	In	In	Defined	Off	Off
GPIO11	I/O/OD	Core	In	In	Defined	Off	Off
Keyboard							
KBCLK	I/OD	Resume	Driven	Driven	Driven	High-Z	High-Z
KBDAT	I/OD	Resume	Driven	Driven	Driven	High-Z	High-Z
PMDAT	I/OD	Resume	Driven	Driven	Driven	High-Z	High-Z
PMCLK	I/OD	Resume	Driven	Driven	Driven	High-Z	High-Z

6.5 Power Sequence in SiS55x

If the system doesn't support AUXVDD, AUXOK must be connected with PWROK. There is no well-defined sequence for RTCVDD, AUXVDD, and VDD. Note that AUXOK and PWROK signal pins are powered by RTCVDD. These two pins must have their own pull-down resistors to prevent them from floating if AUXVDD or VDD is not presented.

In SiS55x, BATOK is used to reset some power management registers in RTC power plane. If it goes low, all registers in RTC power plane will be reset. By the time of next booting up, the BIOS will shows "CMOS Checksum Fail" to indicate that the RTCVDD had been absent.

AUXOK is used to reset the power management registers in AUX power plane. If AUXOK goes low for some reason, the registers in AUX power plane will be reset to their default state. If the system is in power-off state, only PWRBTN# can power up the system under this circumstance. If the system is ON and AUXOK go low for some strange reason, the power will be shutdown immediately.

Finally, PWROK is use to generate CPURST# and PCIRST#. If this signal is de-asserted, PCIRST# and CPURST# will be asserted and the system will be reset by these two reset signal. Note that CPURST# and PCIRST# won't reset the registers which locate in RTC and AUX power planes.

T1 > 1ms

T2 > 10ms

T3 > 100ms

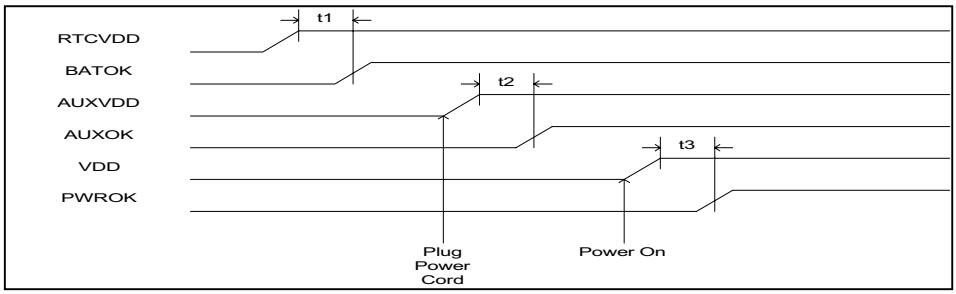


Figure 6-1. Power Sequence

6.6 SiS55x GPIO Multi-functions & Setting

The SA[21:20] and ROMCS[3:2] for ROM function is multi-functioned with GPIO[11:8].

They are chosen by the APC2 register on the PCI space (see another document "SiS55x Family Registers".

Pin Name	Selected	Pin Type	Recommended Setting Method
GPIO8	GPIO8	O	APC2[5]=0
	ROMCS2#	O	APC2[5]=1
GPIO9	GPO9	O	APC2[5]=0
	ROMCS3#	O	APC2[5]=1
GPIO10	GPIO10	O	APC2[4]=0
	SA20	O	APC2[4]=1
GPIO11	GPIO11	O	APC2[4]=0
	SA21	O	APC2[4]=1

6.7 Ball Connectivity Testing

SiS55x will provide a NAND chain Test Mode by TEST# signal is pull low. In order to ensure the connections of balls to tracks of main board, SiS55x provides a simple way to do connective measurements. Basically, an additional 2-input-NAND gate is added into the I/O buffer cells. And, one of inputs of NAND gate is connected to input pin of I/O buffer as test input port in test mode. To monitor the test result at test output port, the output of the NAND gate is connected to the other input of the next NAND gate. Such that, the test result could be propagated and it forms a NAND tree, as depicted in Figure 6-2. To adapt to the scheme, all output buffers of SiS55x are changed to bi-direction buffers to accept test signals.

6.7.1 Test Scheme

There is one NAND tree chain inside SiS55x that includes several test input pins and one output pin.

The following description is an example on 4-test-input pins to explain a NAND tree chain test scheme.

First of all, logic LOW is driven into TESTIN1 pin from track on main board. If logic HIGH could be observed at TESTOUT pin, it means that the connection of TESTIN1 pin to track is good, as shown in Figure 6-3. To test TESTIN2 pin, TESTIN2 pin should be driven LOW also. And, TESTIN1 pin should be kept at logic HIGH, such that the test result could be passed to TESTOUT pin and so on. Although SiS55x operates at 3.3V, all input buffers of SiS55x are 5V-input tolerance. Hence, all test signals could go up to 5V.

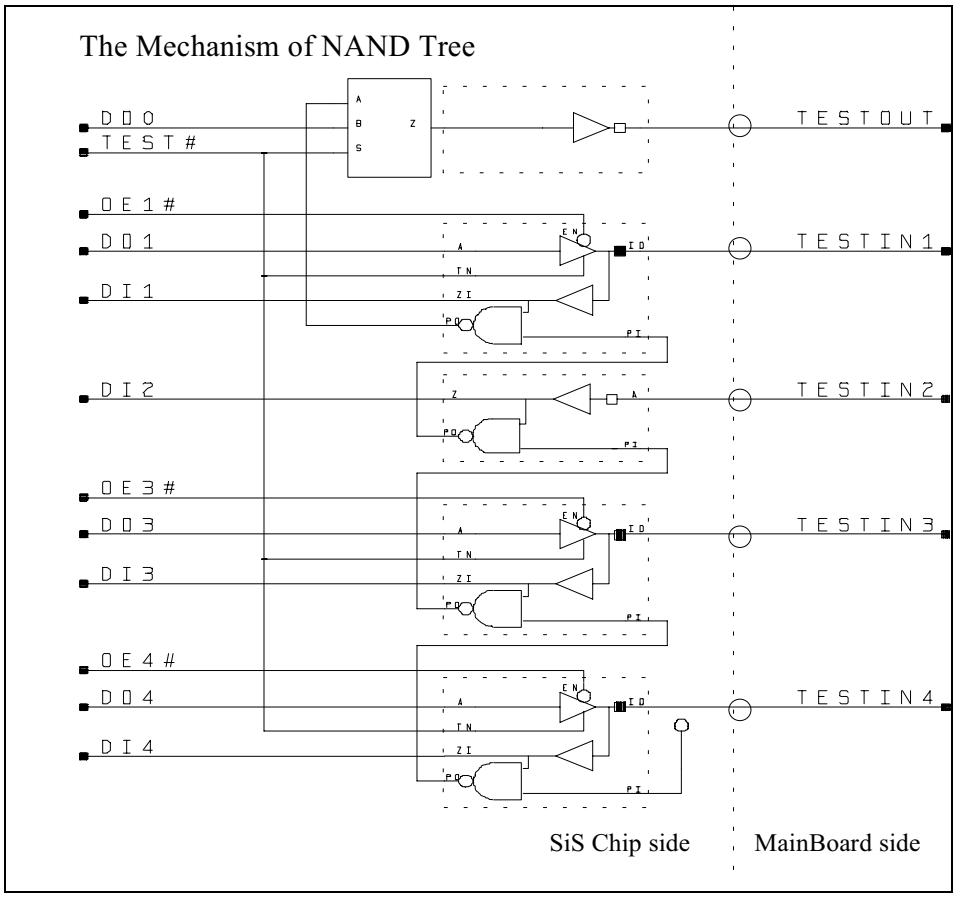


Figure 6-1. The Mechanism of NAND Tree

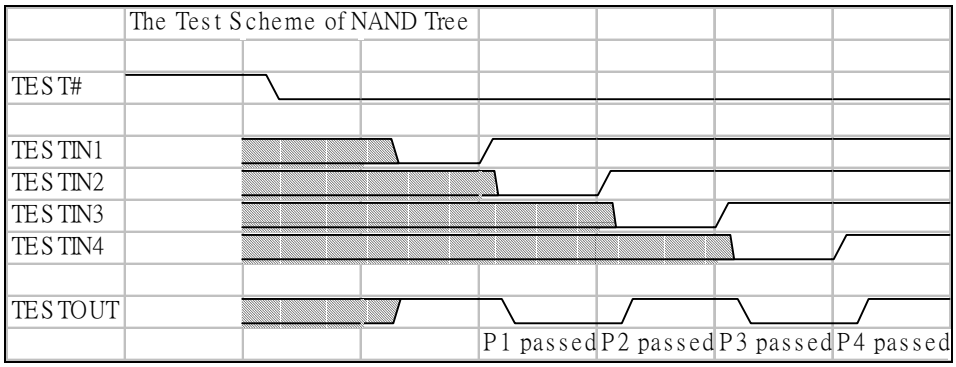


Figure 6-2. The Test Scheme of NAND Tree

6.7.2 Measurements

During test process, this scheme requires all test inputs to be driven simultaneously. To decrease the amount of test probes, SiS55x divides pins into one branch. The noise sensitive signals or analogue signals, i.e. RTC, and power signals, are excluded in the NAND tree chain.

Table 6-1. NAND Tree List for SiS55x

Test Vectors	Test Input Ball Name List	Test Output Ball Name
NAND Tree	PREQ#0, PREQ#1, PREQ#2, AD31, AD30, AD29, AD28, AD27, AD26, AD25, AD24, PC/BE#3, AD23, AD22, AD21, AD20, AD19, AD18, AD17, AD16, PC/BE#2, PFRAME#, PIRDY#, PTRDY#, PDEVSEL#, PLOCK#, PSTOP#, PPAR, PC/BE#1, AD15, AD14, AD13, AD12, AD11, AD10, AD9, AD8, PC/BE#0, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0, INTA#, INTB#, INTC#, INTD#, XCPUCLK, MD32, MD0, MD33, MD1, MD34, MD2, MD35, MD3, MD36, MD4, MD37, MD5, MD38, MD6, MD39, MD7, MD40, MD8, MD41, MD9, MD42, MD10, SDCLK, MD43, MD11, MD44, MD12, MD45, MD13, MD46, MD14, MD47, MD15, SCAS#, WE#, DQM4, DQM0, DQM5,	SERR#

	DQM1, SRAS#, CSA#3, CSA#2, CSA#1, CSA#0, MA0, MA1, MA2, MA3, MA4, MA5, MA6, MA7, MA8, MA9, MA10, MA11, MA12, MA13, MA14, CSB#3, CSB#2, CSB#1, CSB#0, DQM6, DQM2, DQM7, DQM3, MD48, MD16, MD49, MD17, MD50, MD18, MD51, MD19, MD52, MD20, MD53, MD21, MD54, MD22, MD55, MD23, MD56, MD24, MD57, MD25, MD58, MD26, MD59, MD27, MD60, MD28, MD61, MD29, MD62, MD30, MD63, MD31, MRDCL, MWTCL, SD0, SD1, SD2, SD3, SD4, SD5, SD6, SD7, SA0, SA1, SA2, SA3, SA4, SA5, SA6, SA7, SA8, SA9, SA10, SA11, SA12, SA13, ROMCS0, SA15, SA16, SA17, SA18, SA19, SA20, SA21, ROMCS1, ROMCS2, ROMCS3, VRSET, VBWN, VCOMP, BOUT, GOUT, ROUT, CVOSCI, PWRST#, DDC1CLK, DDC1DATA, HSYNC, VSYNC, VSYNC, VIDEO0, VIDEO1, VIDEO2, VIDEO3, VIDEO4, VIDEO5, VIDEO6, VIDEO7, PCLK, DDC2CLK, DDC2DATA, LSYNC, RSYNC, CSYNC, DDC3CLK, DDC3DATA, VBHCLK, VBD0, VBD1, VBD2, VBCAD, VBD8, VBD3, VBD4, VBD5, VBD10, VBD9, VBDE, VBD6, VBD7, VBD11, VBCTL0, VBCTL1, VBHSYNC, VBVSYNC, VAD4, VBCLK, VBGCLK, VAD0, VADE, VAD6, VAD5, VAD7, VAD2, VAGCLK, VAD1, VAHSYNC, VAD3, VAD8, VAD9, VAD10, VAVSYNC, VAD11, PLDXCLK, PLDXDISPOFFN, PLDXVDDEN, PLDXVCONEN, PLDXDU7, PLDXDU6, PLDXDU5, PLDXDU4, HD24, HD25, HD26, HD27, HD28,	

	HD29, HD30, HD31, HD32, HD33, HD34, HD35, XECLKBY, XECLK, R1FCLKDIV4, HD36, HD37, HD38, HD39, HD40, HD41, HD42, HD43, HD44, HD45, HD46, HD47, HD48, HD49, HD50, HD51, HD52, HD53, HD54, HD55, HD56, HD57, HD58, HD59, HD60, HD61, HD62, HD63, LAD0, LAD1, LAD2, LAD3, LFRAME#, LDRQ#, SIRQ, GPIO12, GPIO13, STB#, AFD#, PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7, ERR#, PRINIT#, SLIN#, ACK#, BUSY, PE, SLCT, IDA0, IDA1, IDA2, IDA3, IDA4, IDA5, IDA6, IDA7, IDA8, IDA9, IDA10, IDA11, IDA12, IDA13, IDA14, IDA15, IACS#0, IACS#1, IAIORC#, IAIOWC#, IACHRDY, IAIRQ, IADACK, IADRQ, IADSA1, IADSA0, IADSA2, IACBLID, SPK, ACSYNC, ACCLK, SDATAO, CDA, OC#2, CLK66M, OC#0, USBCLK48M, OC#1, EXTSMI#, THERM#, LDRQ1#, CKE, ACPILED, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9, GPIO10, GPIO11, GPIO14, PWRBTN#, RING, PME#, PSON#, ACRST#, SDATAI0, SDATAI1, KBDAT, KBCLK, PMDAT, PMCLK, KLOCK#, DM2, DP2, DM1, DP1, DM0, DP0, AUXOK, CIRRX, RADD0, RADD1, RADD2, RADD3, RADD4, RADD5, RADD6, RADD7, RADD8, RADD9, RADD10, RADD11, RADD12, RADD13, RADD14, RCLK, RADD15, RDAT0, RDAT1, RDAT2, RDAT3, RDAT4, RDAT5, RDAT6, RDAT7, RGPIO0, RGPIO1, RGPIO2, RGPIO3, PCIRST#, PCICLK, MS0, MS1,	

	MS2, MS3, MS4, MS5.	

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7-1. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Ambient operation temperature	0	75	^{0}C
Storage temperature	-40	125	^{0}C
Input voltage	-0.3	Vcc+0.3	V
Output voltage	-0.5	Vcc	V

NOTE:

Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

7.2 DC Characteristics

7.2.1 DC Characteristics

Ta = 0-75^{0}C, Gnd = 0V, Vcc3 = 3.3V±5%,

Vcore = 1.9V±5%, 1.8V±5%, or 1.7V±5%, depending on the selected Vcore level described in Section 7.2.3.

Table 7-1. DC Characteristics of Host, DRAM, PCI and IDE Interface

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH_TTL}	TTL Input High Voltage	2	Vcc3+0.3	V	
V_{IL_TTL}	TTL Input Low Voltage	-0.3	0.8	V	
$V_{IH\_}$	RTC Input High Voltage	1.4	Vcore+0.3	V	
V_{IL}	RTC Input Low Voltage	-0.3	0.4	V	
V_{OL_TTL}	TTL Output Low Voltage		0.45	V	
I_{OH_TTL}	TTL Output High Current	-4		mA	
I_{OL_TTL}	TTL Output Low Current		4	mA	
I_{IL}	Input Leakage Current		±10	mA	

7.2.2 DC Characteristics for DAC (Analog Output Characteristics)

Table 7-1. DC Characteristics for DAC

Description	Min	Typical	Max	Unit
Black Level	-	0	-	V
White Level	-	700	-	mV
ILE	-1.0	-	+1.0	LSB
DLE	-0.5	-	+0.5	LSB
1 LSB	-	2.734	-	mV
Iref	-	8.40	-	mA

7.2.3 Vcore Levels

For adapting to the different requirements for performance and power consumption, the SiS55x core is designed for the following three Vcore levels each works in a recommend frequency.

Table 7-1. Vcore Level

Vcore Voltage	Min Vcore	Max Vcore	Core Freq.	Power (Full(*))	Temperature of Case(**)
1.9V	1.81V	2.00V	200MHz	3.85W	57°C
1.8V	1.71V	1.89V	180MHz	2.87W	51°C
1.7V	1.62V	1.79V	166MHz	2.19W	48°C

(*): Defined in the next subsection.

(**): Measured at the surface of the molding compound with a small heat sink (37mm x 37mm x 7mm, it's necessary.) when playing DVD with WinDVD 3.1 on Win98. The room temperature is 28°C (still air).

7.2.4 Definition of Power States

In following two subsections, DC current and power dissipation tables is listed with five different power states listed below. All the five states are measured in Win98.

DVD: playing DVD with WinDVD 3.1 on Win98, the CPU utilization usually keeps from 30% to 80%. Listed only at the Vcore level 1.9V and 200MHz. It is in the ACPI "S0" state.

Full: running WinStone2001 on Win98. The CPU utilization always keeps on 100%. It is in the ACPI "S0" state.

Network: download a large file via network by Internet Explorer 5.0. The download rate keeps on 5K bytes per second, and the CPU utilization usually keeps from 10% to 20%. It is in the ACPI "S0" state.

Idle: waiting keyboard or mouse events in Win98. The CPU utilization always keeps on 0%. It is in the ACPI "S0" state.

Standby: into the standby mode of Win98. The CPU core has been halted and the internal clocks are shut down. It is in the ACPI "S1" state.

7.2.5 DC Current

The following tables list the DC current under different Vcore levels and power states. I_{core} and I_{cc3} are the current of Vcore and Vcc3 defined in Section 7.2.1, respectively.

Table 7-1. DC Current of Vcore 1.9V

Power State	Typ I_{core}	Max I_{core}	Typ I_{cc3}	Max I_{cc3}
DVD	1.54	1.76	0.18	0.23
Full	1.76	1.80	0.16	0.18
Network	1.09	1.19	0.17	0.19
Idle	1.05	1.06	0.16	0.16
Standby	0.81	0.81	0.09	0.10

(unit: A)

Table 7-2. DC Current of Vcore 1.8V

Power State	Typ I_{core}	Max I_{core}	Typ I_{cc3}	Max I_{cc3}
Full	1.39	1.44	0.11	0.18
Network	0.90	1.02	0.11	0.13
Idle	0.83	0.84	0.10	0.10
Standby	0.63	0.63	0.08	0.08

(unit: A)

Table 7-3. DC Current of Vcore 1.7V

Power State	Typ I_{core}	Max I_{core}	Typ I_{cc3}	Max I_{cc3}
Full	1.10	1.18	0.10	0.14
Network	0.79	0.83	0.10	0.12
Idle	0.75	0.75	0.10	0.10
Standby	0.55	0.55	0.08	0.08

(unit: A)

7.2.6 Power Dissipation

The following table lists the power dissipation under different Vcore levels and power states. $W_{1.9v}$, $W_{1.8v}$ and $W_{1.7v}$ are power dissipation that Vcore is 1.9V, 1.8V and 1,7V, respectively.

Table 7-1. Power Dissipation of Different Voltage Levels

Power State	$W_{1.9V}$	$W_{1.8V}$	$W_{1.7V}$
DVD	3.50	--	--
Full	3.85	2.87	2.19
Network	2.62	1.98	1.66
Idle	2.53	1.83	1.60
Standby	1.85	1.39	1.19

(unit: W)

7.3 AC Characteristics

7.3.1 DRAM AC Timing

7.3.1.1 Light Loading of SDRAM

SDRAM: SEC KM 416S4030BT-GL (DS63, single-sided 32MB, 4pcs.)

FBC: None

Table 7-1. Signal Valid/Invalid Delay of SDRAM from SDRAM Clock

SIGNAL	CURRENT	L TO H		H TO L		CLOCK	NOTE
		min	max	min	max		
MD[63:0]	Weak	1.84	2.5	1.62	2.03	SDCLK	From post write FIFO, x-1-1-1
	Normal	1.49	1.86	1.59	1.99		
	Strong	1.59	2.42	1.73	2.21		
	Strongest	1.67	2.09	1.81	1.88		
MA[14:0]	Weak	3.78	3.97	3.92	4.28	SDCLK	Note

	Normal	3.53	3.84	3.78	4.1		
	Strong	3.59	3.78	3.61	4.23		
	Strongest	3.62	3.79	3.95	4.25		
WE#	Weak	3.65	3.97	4.05	4.2	SDCLK	Note
	Normal	3.58	3.88	4.03	4.2		
	Strong	3.69	3.98	4.04	4.24		
	Strongest	3.6	3.95	4	4.17		
CS[A:B][3:0]#	Weak	1.96	2.08	3.88	4.17	SDCLK	
	Normal	1.47	1.64	1.84	2.29		
	Strong	1.47	1.51	1.76	1.93		
	Strongest	1.42	1.69	1.74	1.96		
DQM[7:0]#	Weak	1.69	1.92	2.39	2.59	SDCLK	
	Normal	1.53	1.64	1.78	1.98		
	Strong	1.56	1.67	1.8	2.08		
	Strongest	1.52	1.63	1.85	2.03		
SRAS#	Weak	3.89	3.98	4.08	4.23	SDCLK	Note
	Normal	3.57	3.91	3.86	4.15		
	Strong	3.67	3.91	3.93	4.09		
	Strongest	3.67	3.82	4.02	4.17		
SCAS#	Weak	3.78	4.09	4.09	4.24	SDCLK	Note
	Normal	3.63	3.97	4.02	4.13		
	Strong	3.73	3.84	3.97	4.22		
	Strongest	3.56	3.89	4.03	4.17		

(unit: ns)

Table 7-2. Peak Voltage of SDRAM

SIGNAL	L TO H	H TO L	CURRENT	LOAD	NOTE
MD[63:0]	3.8	-0.48	Weak		From post write FIFO, x-1-1-1
	3.76	-0.62	Normal		
	4.18	-0.66	Strong		
	4	-0.64	Strongest		
MA[14:0]	3.5	-0.52	Weak		Note
	3.72	-0.82	Normal		
	3.88	-0.74	Strong		
	3.96	-0.74	Strongest		
WE#	3.52	-0.34	Weak		Note

	3.84	-0.46	Normal		
	3.86	-0.48	Strong		
	4.02	-0.48	Strongest		
CS[A:B][3:0]#	3.4	0.08	Weak		
	3.48	-0.08	Normal		
	3.5	-0.46	Strong		
	3.7	-0.6	Strongest		
DQM[7:0]#	3.68	0.04	Weak		
	3.58	-0.52	Normal		
	3.96	-0.9	Strong		
	4.18	-0.94	Strongest		
SRAS#	3.42	-0.24	Weak		Note
	3.68	-0.5	Normal		
	3.8	-0.54	Strong		
	3.88	-0.58	Strongest		
SCAS#	3.4	-0.08	Weak		Note
	3.72	-0.34	Normal		
	3.76	-0.42	Strong		
	3.96	-0.46	Strongest		

(unit: ns)

7.3.1.2 Heavy Loading of SDRAM

SDRAM: Micron MT48LC2M8A1 TG-8B (DS 76, doubled-sided 32MB, 18pcs.)
KingMax KSV884T4A1A-07 (DS 167, doubled-sided 128MB, 16pcs.)
FBC: SEC KM416S4030CT-G7 (32M, 4pcs.)

Table 7-1. Signal Valid/Invalid Delay of SDRAM from SDRAM Clock

SIGNAL	CURRENT	L TO H		H TO L		CLOCK	NOTE
		min	max	min	max		
MD[63:0]	Weak	3.08	4.41	2.34	2.54	SDCLK	From post write FIFO, x-1-1-1
	Normal	2.19	2.43	1.82	2.21		
	Strong	2.04	2.92	1.97	2.56		
	Strongest	1.93	3.27	1.83	2.61		
MA[14:0]	Weak	7.92	9.41	6.94	7.78	SDCLK	Note
	Normal	6.03	6.7	6.2	6.91		
	Strong	5.75	6.23	6.2	6.78		

	Strongest	5.43	6.12	6.17	6.68		
WE#	Weak	8.62	9.52	6.52	8.23	SDCLK	Note
	Normal	6.94	7.77	6.55	7.11		
	Strong	6.48	7.1	6.58	7.32		
	Strongest	6.56	6.97	6.91	7.21		
CS[A:B][3:0]#	Weak	1.63	1.85	4.61	4.81	SDCLK	
	Normal	1.73	1.8	2.14	2.42		
	Strong	1.69	1.89	2.04	2.34		
	Strongest	1.47	1.85	1.98	2.12		
DQM[7:0]#	Weak	2.6	3.02	4.44	5.34	SDCLK	
	Normal	2.09	2.58	2.86	3.16		
	Strong	1.81	2.22	2.6	2.81		
	Strongest	1.92	3	2.62	2.82		
SDRAS#	Weak	7.88	9.53	6.28	8.6	SDCLK	Note
	Normal	6.25	6.97	5.97	6.98		
	Strong	5.74	6.42	6.42	6.91		
	Strongest	6.13	6.59	6.53	6.81		
SDCAS#	Weak	7.94	9.51	6.16	8.28	SDCLK	Note
	Normal	6.25	7.23	6.35	7.1		
	Strong	5.92	6.92	6.49	6.82		
	Strongest	5.99	6.47	6.14	7.04		

(unit: ns)

Table 7-2. Peak Voltage of SDRAM

SIGNAL	L TO H	H TO L	CURRENT	LOAD	NOTE
MD[63:0]	3.58	-0.46	Weak		From post write FIFO, x-1-1-1
	3.62	-0.38	Normal		
	4.38	-0.72	Strong		
	4.32	-0.76	Strongest		
MA[14:0]	3.2	-0.06	Weak		Note
	3.28	-0.06	Normal		
	3.42	-0.22	Strong		
	3.36	-0.16	Strongest		
WE#	3.34	0	Weak		Note
	3.3	-0.04	Normal		
	3.42	-0.08	Strong		

	3.44	-0.1	Strongest		
CS[A:B][3:0]#	3.4	0.28	Weak		
	3.46	-0.06	Normal		
	3.5	-0.22	Strong		
	3.46	-0.44	Strongest		
DQM[7:0]#	3.48	-0.22	Weak		
	3.82	-0.32	Normal		
	3.74	-0.54	Strong		
	3.66	-0.64	Strongest		
SRAS#	3.18	0.06	Weak		Note
	3.38	0.06	Normal		
	3.28	0.06	Strong		
	3.32	0.04	Strongest		
SCAS#	3.32	0.04	Weak		Note
	3.4	0.06	Normal		
	3.5	-0.02	Strong		
	3.5	-0.1	Strongest		

(unit: ns)

Note:

1. The propagation delay margin for these signals is at least 2 memory clocks.
2. The timing and loading are measured from DRAM chip directly.
3. The timing is measured from 1.4V of clock of DRAM to 1.4V of tested signal.
4. These signals are controlled by Register 8Ch, 8Dh, and 8Fh.
   The setting for Register 8Fh is 4ah in this case.
   The setting for Register 8Dh is 84h in this case.
   The setting for Register 8Ch is 44h in this case.
5. The clock skew between SDCLK0 ~ SDCLK11 of DRAM chip and SDCLK of SiS55x is around 0.1 ~ 0.428ns. The SDCLK of SiS55x is leading all clocks of DRAM.

7.3.2 PCI Signals AC Timing

7.3.2.1 Light Loading

No PCI card plugged except when measuring PGNT # (Seagate ST51080N SCSI HD and AHA-2940 SCSI card is used)

Table 7-1. PCI Signals AC Timing

SIGNAL NAME	L→H		H→L		LOADING	CLOCK SOURCE	NOTE
	min(ns)	max(ns)	min(ns)	max(ns)	Pf		
PCIRST#	7.71	8.23	13.21	20.75		PCICLK	
AD[31:0]	6.27	7.00	6.23	7.01		PCICLK	
PC/BE[3:0]#	6.08	6.70	5.72	6.33		PCICLK	
PFRAME#	5.76	6.41	7.67	8.38		PCICLK	
PIRDY#	4.99	5.73	7.15	7.87		PCICLK	
PLOCK#	5.24	5.53	5.36	5.78		PCICLK	
PPAR	5.72	6.47	6.36	7.06		PCICLK	
PTRDY#	5.53	6.22	6.20	6.91		PCICLK	
PSTOP#	6.12	6.82	5.92	6.57		PCICLK	
PDEVSEL#	5.69	6.43	5.97	6.80		PCICLK	
PGNT#	4.43	5.21	4.20	5.09		PCICLK	

7.3.2.2 Heavy Loading

Slot 0: Bt848KPF Video Decoder

Slot 1: AHA-2940 SCSI card

Table 7-1. PCI Signals AC Timing

SIGNAL NAME	L→H		H→L		LOADING	CLOCK SOURCE	NOTE
	min(ns)	max(ns)	min(ns)	max(ns)	pf		
PCIRST#	8.80	9.93	17.55	28.63		PCICLK	
AD[31:0]	6.48	7.27	6.74	7.56		PCICLK	
PC/BE[3:0]#	6.55	7.34	6.15	6.94		PCICLK	
PFRAME#	6.54	7.30	8.50	8.90		PCICLK	
PIRDY#	5.67	6.57	7.88	8.98		PCICLK	
PLOCK#	5.31	5.66	5.41	5.92		PCICLK	
PPAR	5.61	6.60	5.88	6.66		PCICLK	
PTRDY#	5.47	6.17	6.10	7.01		PCICLK	
PSTOP#	6.04	6.87	6.20	7.13		PCICLK	
PDEVSEL#	5.77	6.33	6.94	7.69		PCICLK	
PGNT#	4.43	5.08	4.45	5.38		PCICLK	

Table 7-2. Clock Skew

Clock Skew		Min. (ps)	Max. (ps)
PCLK (55x side)	PCICLK (PCI slot side)	355	700

Note: PCLK lags PCICLK.

7.3.3 VGA Signals AC Timing

7.3.3.1 Video Signals Timing

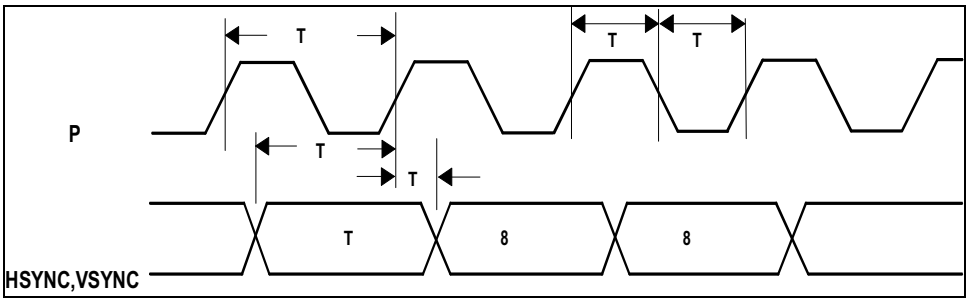


Figure 7-1. Video Timing 4, 8, and 16 Bits/Pixel Modes

Table 7-1. Video AC Timing for 4, 8, and 16 BPP

SYMBOL	PARAMETER	MIN.	MAX.	NOTES
T_1	VIDEO[7:0], HSYNC, VSYNC Setup Time	10	-	
T_2	VIDEO[7:0], HSYNC, VSYNC Hold Time	2	-	
T_3	PCLK Period	20	-	
T_4	PCLK High Time	7	-	
T_5	PCLK Low Time	7	-	

(Units: ns)

7.3.3.2 Digital Interface Signals Timing

Figure 7-1. Digital Video Timing

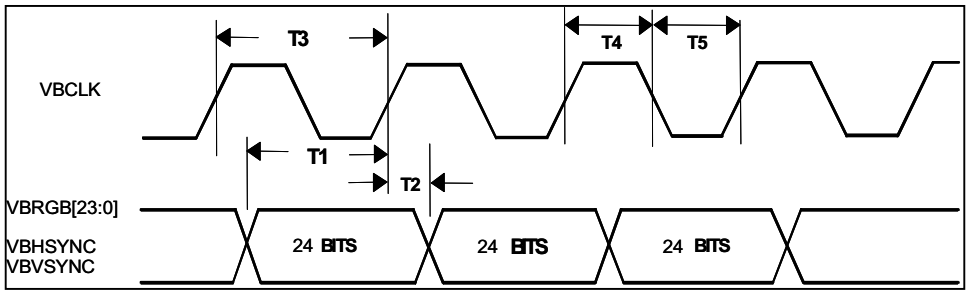


Table 7-1. Digital Video Interface AC Timing Table

SYMBOL	PARAMETER	MIN.	MAX.	NOTES
T_1	VBD[11:0], VBHSYNC, VBVSYNC Setup Time	3.0	-	-
T_2	VBD[11:0], VBHSYNC, VBVSYNC Hold Time	2.0	-	-
T_3	VBCLK Period	7.4	-	-
T_4	VBCLK High Time	3.0	-	-
T5	VBCLK Low Time	3.0	-	-

(Unit: ns)

8 Instruction Throughput

This chapter describes the x86 instruction throughput of SiS55x. The throughput is the number of cycles required to wait to issue the same instruction again.

8.1 Assumptions

The throughputs depend on the conditions of cache hits, memory accesses, bus response, branch prediction, Micro-ROM sequence and the issue rules. To focus on the most typical throughputs, we make some assumptions as follows:

- The cache is always hit. Otherwise, the cache miss penalty is about 30 cycles.
- The memory and the bus always respond at the next cycle.
- The branch prediction is always hit. Otherwise, the branch miss-predict penalty is 5~7 cycles
- The complex instructions that are hard to list all the conditions are estimated based on the worst case scenario.

8.2 Instruction Category

For the general-purpose execution units and the MMX units, up to three instructions can be issued sequentially in one cycle. Because the throughputs of the general-purpose instructions greatly depend on the issue rules, we categorize the general-purpose instructions into four levels according to their issue ability:

- **Complex**: complex instructions that must be executed though the Micro-ROM. No new instruction can be issued until the issued instruction is completed.
- **No Pair**: instructions that can be executed without the Micro-ROM. However, still no new instruction can be issued until the issued instruction is completed.
- **Pair**: another instruction can be issued doubly or triply if there is no resource conflict nor data dependency.
- **Pair & Twin**: another instruction may be issued doubly or triply by the twining mechanism (described in Section 1.2) even with the data dependency.

By avoiding the resource conflict and data dependency, most of the MMX instructions can be doubly or triply issued in one cycle. Thus the throughputs of the MMX instructions are not sensitive to the issue rules. To this end, we don't categorize MMX instructions.

8.3 Throughput Tables

The throughputs of the general-purpose, FPU, and MMX instructions are individually listed in the following three tables.

Table 8-1. General Purpose Instruction Throughputs

General Purpose Instruction	Throughput		Category	Note
	Real Mode	Prot'd Mode		
AAA	2	2	Complex	
AAD	3	3	Complex	
AAM	1	1	No Pair	
AAS	2	2	Complex	
ADC	1	1	Pair & Twin	
ADD	1	1	Pair & Twin	
AND	1	1	Pair & Twin	
ARPL			Complex	
Dest (RPL) < Src (RPL) Dest (RPL) >= Src (RPL)		9 8		
BOUND	5	5	Complex	
BSF	2	2	Pair	
BSR	2	2	Pair	
BSWAP	4	4	Complex	
BT	7	7	Complex	
BTC	7	7	Complex	
BTR	7	7	Complex	
BTS	7	7	Complex	
CALL			Complex	
Direct within Segment	1	1		
Register/Memory Indirect within Segment	5	5		
Direct Inter-segment - Con/Nonconforming code segment SP Wrap Possible SP Wrap Impossible - Call Gate to Same Privilege SP Wrap Possible SP Wrap Impossible - Call Gate to Different Privilege No Par's - Call Gate to Different Privilege *m* Par's - Task Gate to 16-bit Task - Task Gate to 32-bit Task	 4 7 	 9 12 15 18 27 27+2*m* 73 75		

- Task Gate to VM86 Task		61		
- TSS to 16-bit Task		73		
- TSS to 32-bit Task		75		
- TSS to VM86 Task		61		
Indirect Inter-segment				
SP Wrap Possible	7	12		
SP Wrap Impossible	10	15		
- Call Gate to Same Privilege				
SP Wrap Possible		18		
SP Wrap Impossible		21		
- Call Gate to Different Privilege No Par's		30		
- Call Gate to Different Privilege *m* Par's		30+2*m*		
- Task Gate to 16-bit Task		76		
- Task Gate to 32-bit Task		78		
- Task Gate to VM86 Task		64		
- TSS to 16-bit Task		76		
- TSS to 32-bit Task		78		
- TSS to VM86 Task		64		
CBW	1	1	Pair	
CDQ	1	1	Pair	
CLC	1	1	Pair & Twin	
CLD	1	1	Pair & Twin	
CLI	2	2	Complex	
CLTS	4	4	Complex	
CMC	1	1	Pair & Twin	
CMP	1	1	Pair & Twin	
REPE CMPS	7+*n*	7+*n*	Complex	*n* = (E)CX
CMPS	2	2	Complex	
CMPXCHG	7	7	Complex	
CMPXCHG8B			Complex	
Equal	5	5		
Non-equal	8	8		
CPUID			Complex	
EAX == 0	9	9		
EAX == 1	16	16		
EAX == Others	18	18		
CWD	1	1	Pair & Twin	

CWDE	1	1	Pair & Twin	
DAA	3	3	Complex	
DAS	3	3	Complex	
DEC	1	1	Pair & Twin	
DIV			No Pair	
Byte	10	10		
Word	18	18		
Double-word	34	34		
ENTER			Complex	
Level == 0	9	9		
Level == 1	10	10		
Level (*L*) > 1	10+*L*	10+*L*		
HLT	1	1	No Pair	
IDIV			No Pair	
Byte	10	10		
Word	18	18		
Double-word	34	34		
IMUL			No Pair	
Byte	4	4		
Word	6	6		
Double-word	10	10		
IN	3		Complex	
Protected Mode		3		
VM86 Mode		13		
INC	1	1	Pair & Twin	
INS	7		Complex	
Protected Mode		7		
VM86 Mode		17		
REP INS	13+3*n*		Complex	*n* = (E)CX
Protected Mode		13+3*n*		
VM86 Mode		23+3*n*		
INT			Complex	
Protected Mode				
-Interrupt to Conforming Code	17			
-Interrupt to Nonconforming Code	28			
-Task Gate to 16-bit Task	79			
-Task Gate to 32-bit Task	81			

-Task Gate to VM86 Task	67			
VM86 Mode -Interrupt to Nonconforming Code	40			
INTO OF == 0 OF == 1	1 INT	1 INT	No Pair Complex	
INVD	18	18	Complex	
INVLPG	10	10	Complex	
IRET			Complex	
Real Address Mode	7			
To Virtual Mode		22		
Protected Mode - To same privilege - To different privilege		 17 29		
Task Return - Task Gate to 16-bit Task - Task Gate to 32-bit Task - Task Gate to VM86 Task - TSS to 16-bit Task - TSS to 32-bit Task - TSS to VM86 Task		 73 75 61 73 75 61		
Jcc (JB/JNAE/JC, JBE/JNA, JCXZ/JECXZ, JE/JZ, JL/JNGE, JLE/JNG, JNB/JAE/JNC, JNBE/JA, JNE/JNZ, JNL/JGE, JNLE/JG, JNO, JNP/JPO, JNS, JO, JP/JPE, and JS)	1	1	Pair	If branch prediction successful
JMP			Complex	
Register/Memory Indirect within Segment	5	5		
Direct Inter-segment - Con/Nonconforming code segment - Call Gate - Task Gate to 16-bit Task - Task Gate to 32-bit Task	4	 9 10 73 75		

- Task Gate to VM86 Task		61		
- TSS to 16-bit Task		73		
- TSS to 32-bit Task		75		
- TSS to VM86 Task		61		
Indirect Inter-segment				
- Con/Nonconforming code segment	6	11		
- Call Gate		12		
- Task Gate to 16-bit Task		75		
- Task Gate to 32-bit Task		77		
- Task Gate to VM86 Task		64		
- TSS to 16-bit Task		75		
- TSS to 32-bit Task		77		
- TSS to VM86 Task		63		
LAHF	1	1	Pair	
LAR	--	9	Complex	
LDS	3	7	Complex	
LEA	1	1	Pair & Twin	
LES	3	7	Complex	
LEAVE	2	2	Complex	
LFS	3	7	Complex	
LGDT	6	6	Complex	
LGS	3	7	Complex	
LIDT	1	1	No Pair	
LLDT	--	11	Complex	
LMSW	3	3	Complex	
REP LODS	8+*n*	8+*n*	Complex	*n* = (E)CX
LODS	2	2	Complex	
LSL	--	9	Complex	
LSS	3	7	Complex	
LTR	--	10	Complex	
MOV crx	10	10	Complex	
MOV drx	5	5	Complex	
MOV seg, rm	4	9	Complex	
MOV others	1	1	Pair & Twin	
REP MOVS	8+*n*	8+*n*	Complex	
MOVS	2	2	Complex	
MOVSX	1	1	No Pair	

MOVZX	1	1	No Pair	
MUL			No Pair	
Byte	4	4		
Word	6	6		
Double-word	10	10		
NEG	1	1	Pair & Twin	
NOP	1	1	Pair & Twin	
NOT	1	1	Pair & Twin	
OR	1	1	Pair & Twin	
OUT	3		Complex	
Protected Mode		3		
VM86 Mode		13		
OUTS	11		Complex	
Protected Mode		11		
VM86 Mode		21		
REP OUTS	19+2*n*		Complex	*n* = (E)CX
Protected Mode		19+2*n*		
VM86 Mode		29+2*n*		
POPA / POPAD	4	4	Complex	
POPF / POPFD	4	4	Complex	
POP reg	1	1	Pair & Twin	
POP mem	2	2	Complex	
POP seg	3	10	Complex	
PUSH reg	1	1	Pair & Twin	(E)SP can not Twin
PUSH mem	2	2	Complex	
PUSHA / PUSHAD	11	11	Complex	
PUSHF / PUSHFD	2	2	Complex	
RCL	2~3	2~3	No Pair	
RCR	2~3	2~3	No Pair	
RDMSR	16	16	Complex	
RDTSC	1	1	No Pair	
RET			Complex	
Within Segment	1	1		
Within Segment Adding Immediate to SP	3	3		
Inter-segment	7	9		
Inter-segment Adding Immediate to SP	7	9		

Protected Mode: Differnet Privilege Level - Inter-segment - Inter-segment Adding Immediate to SP		 24 24		
ROL	1	1	Pair	
ROR	1	1	Pair	
RSM	65	65	Complex	
SAHF	1	1	Pair	
SAL	1	1	Pair	
SAR	1	1	Pair	
SBB	1	1	Pair and Twin	
SCAS	2	2	Complex	
REPE SCAS	8+*n*	8+*n*	Complex	*n* = (E)CX
SET*cc* (SETB/SETNAE/SETC, SETBE/SETNA, SETE/SETZ, SETL/SETNGE, SETLE/SETNG, SETNB/SETAE/SETNC, SETNBE/SETA, SETNE/SETNZ, SETNL/SETGE, SETNLE/SETG, SETNO, SETNP/SETPO, SETNS, SETO, SETP/SETPE, and SETS)	1	1	No Pair	
SGDT	2	2	Complex	
SHL	1	1	Pair	
SHLD	3~4	3~4	No Pair	
SHR	1	1	Pair	
SHRD	3~4	3~4	No Pair	
SIDT	1	1	No Pair	
SLDT	1	1	No Pair	
STC	1	1	Pair & Twin	
STD	1	1	Pair & Twin	
STI	2	2	Complex	
STOS	2	2	Complex	
REP STOS	8+*n*	8+*n*	Complex	*n* = (E)CX
STR	1	1	No Pair	
SUB	1	1	Pair & Twin	
SMSW	1	1	No Pair	
VERW / VERR	--	9	Complex	
WAIT	1	1	No Pair	
WBINVD	283	283	Complex	
WRMSR	39	39	Complex	

XADD	1	1	No Pair	
XCHG	1	1	No Pair	
XLAT / XLATB	4	4	Complex	
XOR	1	1	Pair & Twin	

Table 8-2. FPU Instruction Throughputs

FPU instruction	Throughput		Note
F2XM1	63		
FABS	1		
FADD **FADDP** **FIADD**	1 1 8		
FCHS	1		
FCLEX	4		
FNCLEX	4		
FCOM	1		
FCOMP	1		
FCOMPP	1		
FICOM	4		
FICOMP	4		
FCOS	51*	101~111	*src<2/π
FDECSTP	1		
FIDIV	40		
FDIVP	40		
FDIVR	40		
FDIVRP	40		
FIDIV	40		
FIDIVR	40		
FFREE	1		
FINCSTP	1		
FINIT	4		
FNINIT	4		
FLD reg	1		
FLD mem	2		
FILD	1		

FBLD	68		
FLDCW	2		
FLDENV	14		
FLD1	1		
FLDL2E	1		
FLDL2T	3		
FLDLG2	3		
FLDLN2	1		
FLDPI	3		
FLDZ	1		
FMUL	2* / 1		*If two successive fmul instructions come together.
FMULP	2* / 1		*If two successive fmulp instructions come together.
FIMUL	10		
FNOP	1		
FPATAN	173~184		
FPREM	71		
FPREM1	72		
FPTAN	168*	216~225	*src<2/π
FRNDINT	9		
FRSTOR	31		
FSAVE	52		
FNSAVE	52		
FSCALE	16		
FSIN	50*	100~115	*src<2/π
FSINCOS	84*	133~144	*src<2/π
FSQRT	71~74		
FST reg	1		
FST mem	2		
FSTP	2		
FBSTP	93		
FIST	10		
FISTP	10		
FSTCW	6		
FNSTCW	6		

FSTENV	16	
FSTSW	3	
FSTSW AX	2	
FNSTSW AX	2	
FSUB	1	
FSUBP	1	
FSUBRP	1	
FISUB	12	
FISUBR	12	
FTST	1	
FUCOM	1	
FUCOMP	1	
FUCOMPP	1	
FWAIT	1	
FXAM	1	
FXCH	1	
FXTRACT	4	
FYL2X	166~172	
FYL2XP1	157	

Table 8-3. MMX Instruction Throughputs

MMX instruction	Throughput	Note
EMMS	1	
MOVD	1	
MOVQ	1	
PACKSSDW	1	
PACKSSWB	1	
PACKUSWB	1	
PADDB	1	
PADDD	1	
PADDSB	1	
PADDSW	1	
PADDUSB	1	
PADDUSW	1	

PADDW	1	
PAND	1	
PANDN	1	
PCMPEQB	1	
PCMPEQD	1	
PCMPEQW	1	
PCMPGTB	1	
PCMPGTD	1	
PCMPGTW	1	
PMADDWD	2	
PMULHW	2	
PMULLW	2	
POR	1	
PSLLD	1	
PSLLQ	1	
PSLLW	1	
PSRAD	1	
PSRAW	1	
PSRLD	1	
PSRLQ	1	
PSRLW	1	
PSUBB	1	
PSUBD	1	
PSUBSB	1	
PSUBSW	1	
PSUBUSB	1	
PSUBUSW	1	
PSUBW	1	
PUNPCKHBW	1	
PUNPCKHDQ	1	
PUNPCKHWD	1	
PUNPCKLBW	1	
PUNPCKLDQ	1	
PUNPCKLWD	1	
PXOR	1	

9 Throttling Features

9.1 Enter Throttling

Throttling is a state in ACPI processor state C0 (in the G0/S0 working state). It provides programmable throttling function to place the processor executing at a designated performance level relative to its max performance. This is achieved by cyclically assert and de-assert the STPCLK# signal in a designated duty.

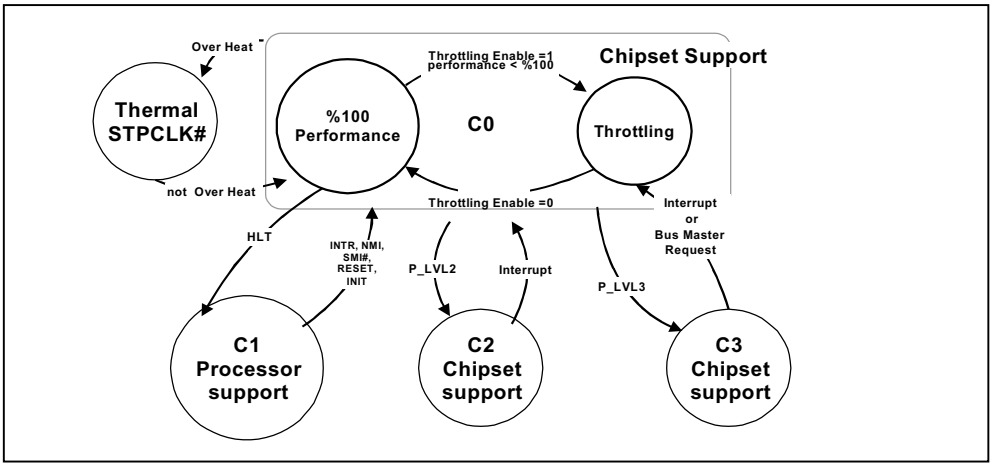


Figure 9-1. Processor Power States

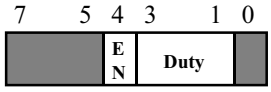
Step 1. Lookup the ACPI Base Register:

ACPI Base Register: on PCI space, Device 1, Function 0 (LPC function), Register 74h~75h.

For current BOIS, the ACPI Base is 0800h

Step 2. Set the ACPI Processor Control Register (P_CNT):

P_CNT: on ACPI Register 10h.



EN: Throttling Function Enable (bit 4) – Enable the throttling function.

Duty: Throttling duty cycle control (bits 3 through 1) –

3-bit field determines the duty cycle of the STPCLK# signal, as shown in Figure 9-2.

Thus, to enable throttling with duty cycle *bbb*:

MOV AL, 1*n* (*n* = {*b*, *b*, *b*, 0})

MOV DX, 0810h (ACPI Base + 10h)

OUT DX, AL

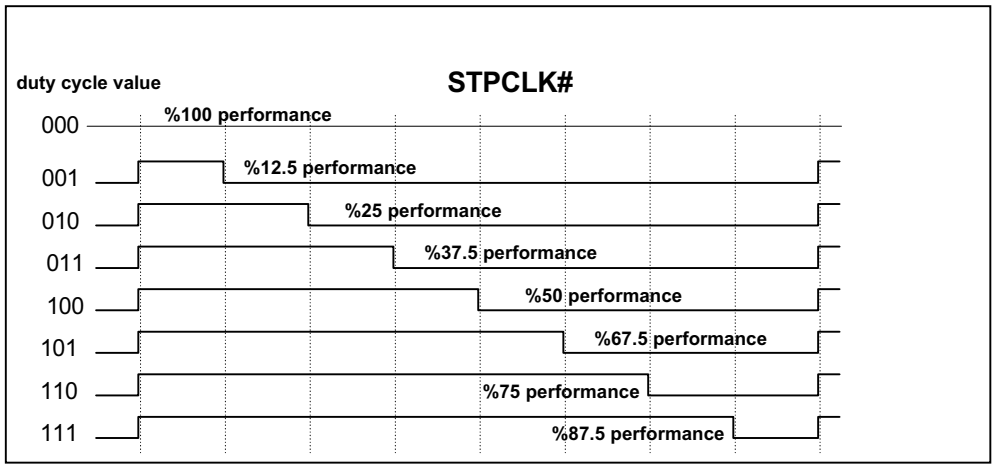


Figure 9-2. Throttling Duty Cycle

9.2 Throttling Power Dissipation

We measure the throttling characteristics with following two conditions under 266MHz and 1.5V (using SiS552-LV). Both the conditions are measured in Win98.

Speedy: running Speedy twice in Win98. The CPU utilization always keeps on 100%. It is in the ACPI “S0” state.

Idle: waiting keyboard or mouse events in Win98. The CPU utilization always keeps on 0%. It is in the ACPI “S0” state.

In both the conditions, we measure power dissipation with following power states.

Normal: disable the throttling function.

100.0% ~ 12.5%: enable the throttling function, and with the eight different duty cycle level.

Standby: into the standby mode of Win98. The CPU core has been halted and the internal clocks are shut down. It is in the ACPI “S1” state.

The throttling power dissipations under different conditions and states are drawn in the Figure 9-3.

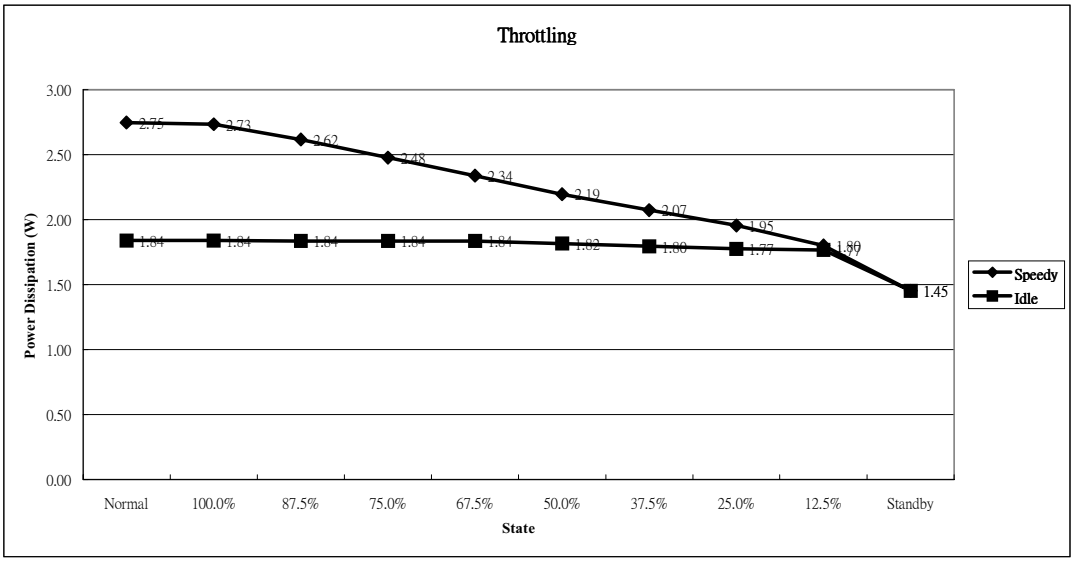


Figure 9-1. Throttling Power Dissipation

9.3 Throttling Performance

To observe the throttling performance, we list the performance decrease trend in Figure 9-4.

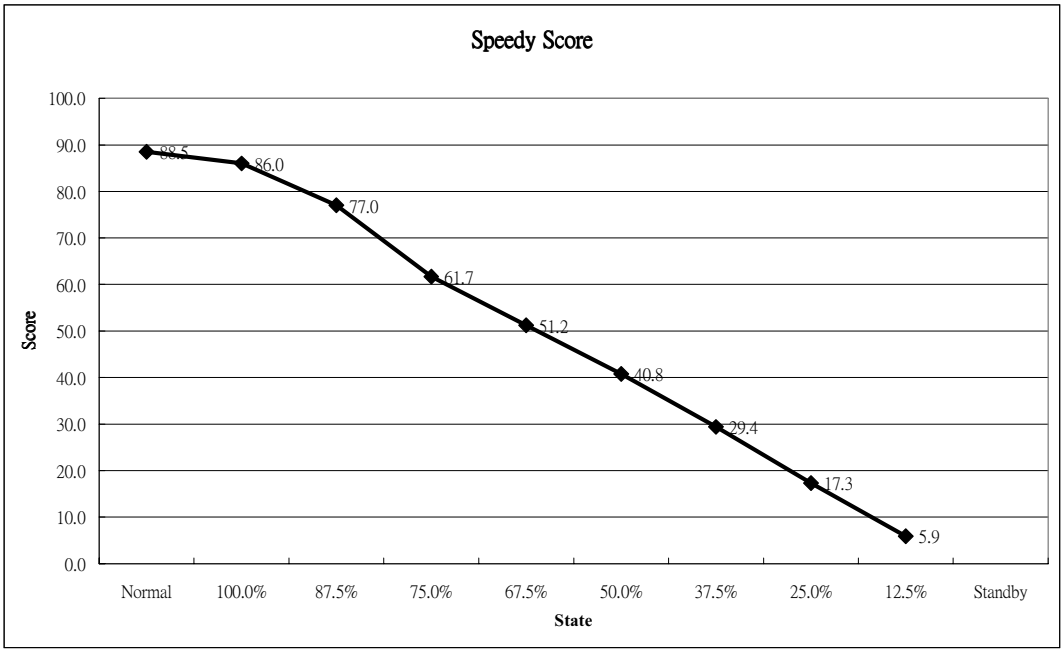
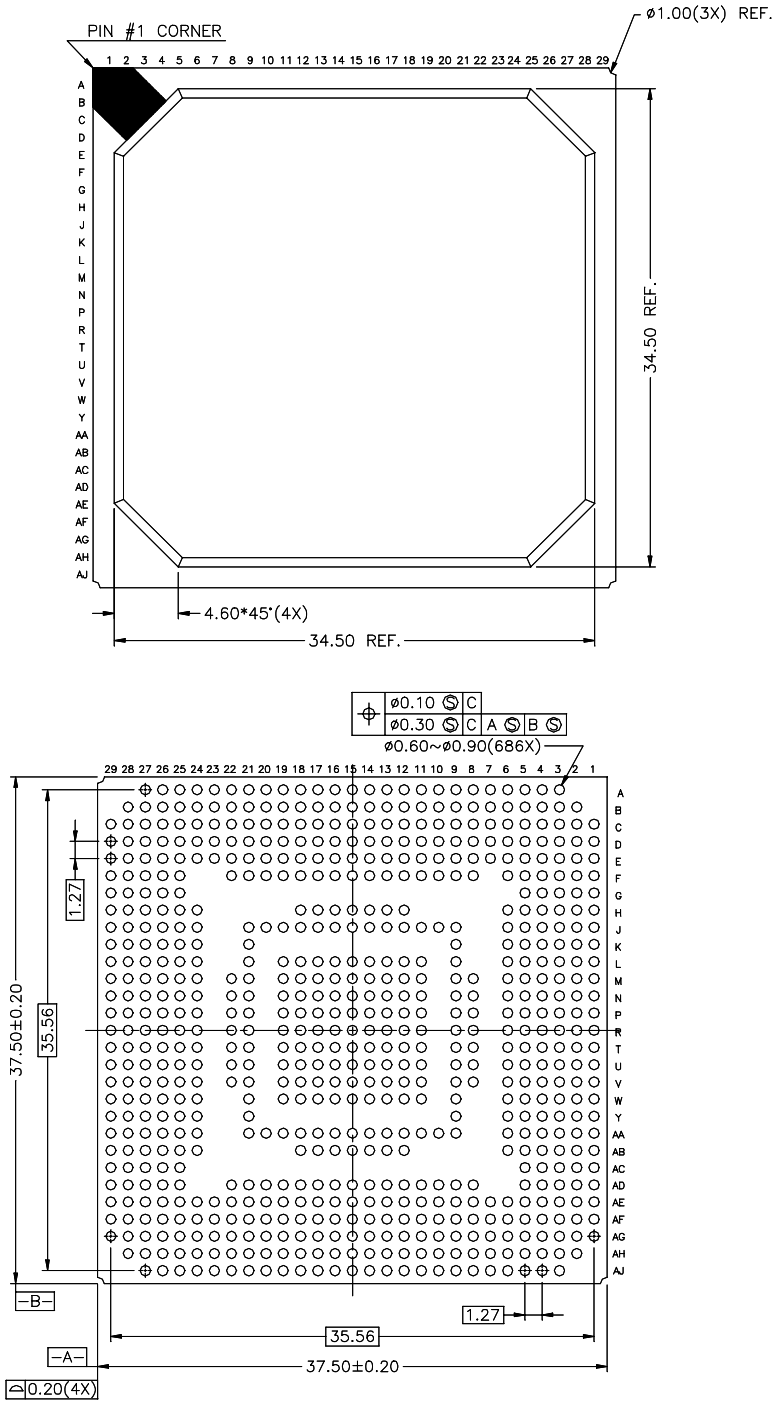
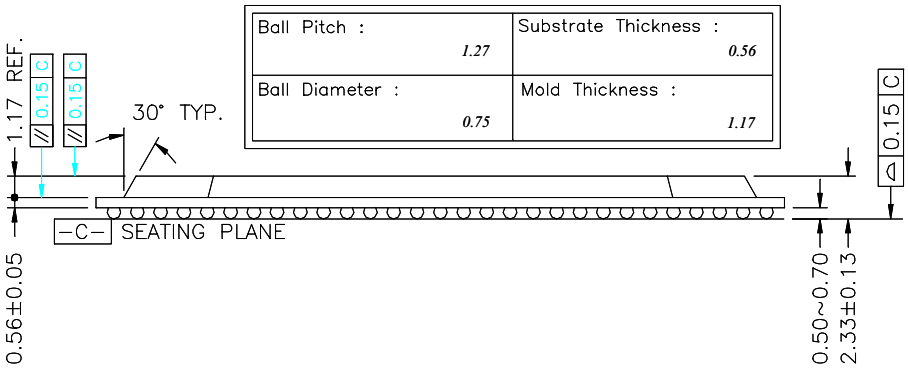


Figure 9-1. Speedy Score of Different States

10 Mechanical Package Outlines




Ball Pitch : 1.27
Substrate Thickness : 0.56
Ball Diameter : 0.75
Mold Thickness : 1.17
1.17 REF.
0.15 C
0.15 C
30° TYP.
0.15 C
-C- SEATING PLANE
0.56±0.05
0.50~0.70
2.33±0.13

11 Appendix

11.1 ACPI Power State

11.1.1 Global System State Definitions

Global system states apply to the entire system and are visible to user. Global system states can be easily defined by the power state of the computer

	G0	G1	G2	G3
VDD	On	On/Off	Off	Off
AUXVDD	On	On	On	Off

Following is a list of the global states:

G0 – Working:

A computer state where the computer executes the user's applications. In this state, devices are dynamically having their power states changed. The user will be able to select various performance/power characteristics of the system.

G1 – Sleeping:

A computer state where the computer consumes a small amount of power. The user's applications are not being executed, and the system appears to be off. Work can be resumed without rebooting the OS because the context of the system is saved by the hardware.

G2 – Soft off:

A computer state where the computer consumes a minimal amount of power. No user application or system code is run. The system must be restarted to return to the Working state. The system's context will not be preserved by the hardware.

G3 – Mechanical off:

A computer state where the computer only consumes RTC power. This state is entered and left by a mechanical means (e.g. turning off the system's power through unplugging the power cord). No hardware context is retained by hardware and the OS must be restarted to return to the Working state. Only in this state can the hardware be disassembled safely.

11.1.2 Device Power State Definitions

Device power states are states of particular devices and they are generally not visible to the users. For example, some devices may be in the Off state even

though the system as a whole is in the Working state. Note that the hardware and software behavior of Device State is not defined in ACPI spec.

Device State	Power Consumption	Device Context Retained	Driver Restoration
D0	As need for operation	All	None
D1	<D0	>D2	<D2
D2	<D1	>D3 Hot	<D3
D3 Hot	<D2	None	Full init and load
D3 Cold	0	None	Full init and load

D0 – Fully on:

The device is completely active and responsive in this state.

D1/D2:

The meaning of D1/D2 Device State is defined by each class of device. In general, D2 is expected to save more power and preserve less device context than D1.

D3 – (Hot/Cold) Off:

The device context is lost when this state is entered. OS must re-initialize the device when it backs to D0. In general, Power and Clock have been fully removed from the device when the device is in D3 Cold Off. When the device enters D3 Hot state, Power and Clock may be removed from the device. All classes of devices define this state.

11.1.3 Sleeping State Definitions

Sleeping states (Sx states) are types of sleeping states within the global sleeping state, G1. The Sx states are briefly defined as following.

S0/G0 – Working State:

The S0 state is the same as the global state, G0. All system contexts are retained by hardware continuously. All Processor and Device States can only be changed dynamically when system is in this state.

S1/G1 – Sleeping State:

The S1 sleeping state is a low wake-up latency. In this state, no system context is lost.

S2/G1 – Sleeping State:

This state is similar to the S1 sleeping state except the CPU and system cache context is lost.

S3/G1 – Suspend to Ram (STR) State:

The S3 sleeping state is a low wake-up latency sleeping state where all system contexts are lost except system memory.

S4/G1 – Suspend to Disk (STD) State:

The S4 sleeping state is the lowest power, longest wake-up latency sleeping state supported by ACPI. In order to reduce power to a minimum, the hardware platform has powered off all devices. Platform context is maintained in Hard Disk.

S5/G2 – Soft Off State:

The S5 state is similar to the S4 state except the OS does not save any context nor enable any devices to wake the system. The system is in the soft off state and requires a complete boot when awakened.

11.1.4 Processor Power State Definitions

Processor power states (Cx) are processor power consumption and thermal management states within the global working state, G0.

C0 Processor Power State:

While the processor is in this state, it executes instructions with full/throttling rate.

C1 Processor Power State:

The processor is in a low power state where it is able to maintain the context of the system caches. This state is supported through a native instruction of the processor (HLT for IA-PC), and assumes no hardware support is needed from the chipset.

C2/C3 Processor Power State:

The processor is in a low power state where it is able to maintain the context of the system caches. This state is supported through chipset hardware.

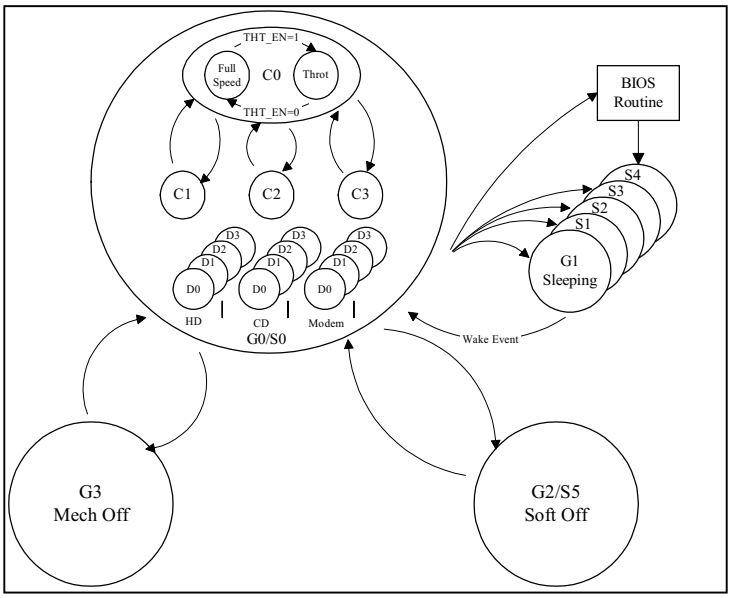


Figure 11-1. ACPI Model

11.2 The Hardware Event of ACPI

The ACPI architecture defines mechanisms for hardware to generate events and control logic to sequence the platform between the various global system states. Events are used to notify the OS that some action is needed, and control logic is used by the OS to cause some state transition. ACPI-defined events are “hardware” or “interrupt” events. A hardware event is one that causes the hardware to unconditionally perform some operation. An interrupt event causes the execution of an event handler, which allows the software to make a policy decision based on the event. For example, the AUDPME Event (hardware event) will sequence the system from a sleeping state (S1/S2/S3/S4) to the S0 working. After waking from the sleeping state, an interrupt event will be triggered and the ACPI driver will schedule the execution of an OEM-supplied AML handler associated with the event.

For legacy systems (APM mode under WIN95/98), an event normally generates an OS-transparent interrupt (this means that OS won’t aware the existence of the interrupt), such as a System Management Interrupt (SMI#). All power management event are handle by the SMI# handler which is provided by the system BIOS. For ACPI systems the interrupt events need to generate an OS-visible interrupt that is shareable (SCI). Figure 9-2 shows the hardware model for ACPI fix feature. Figure 9-3 and Figure 9-4 show the hardware model of ACPI feature.

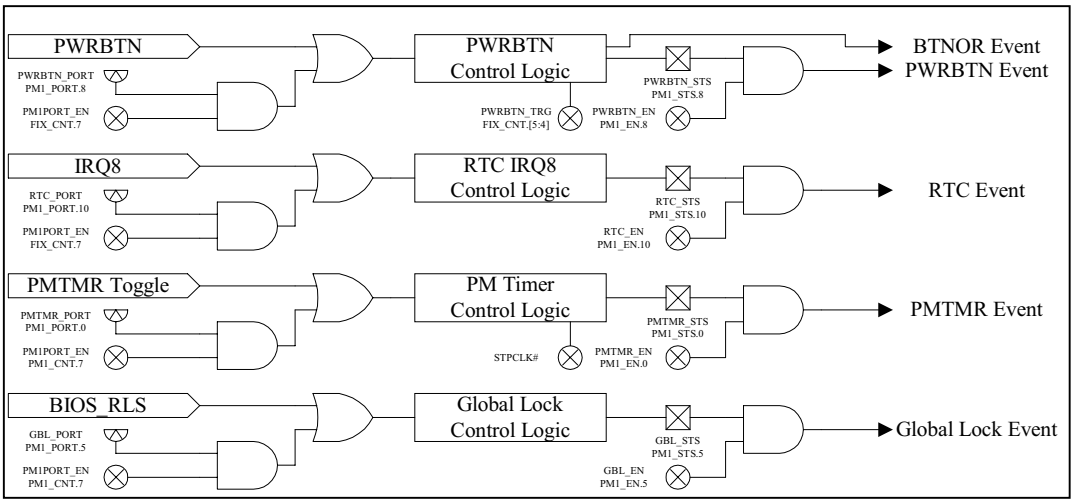


Figure 11-1. Hardware Model for Fix Feature

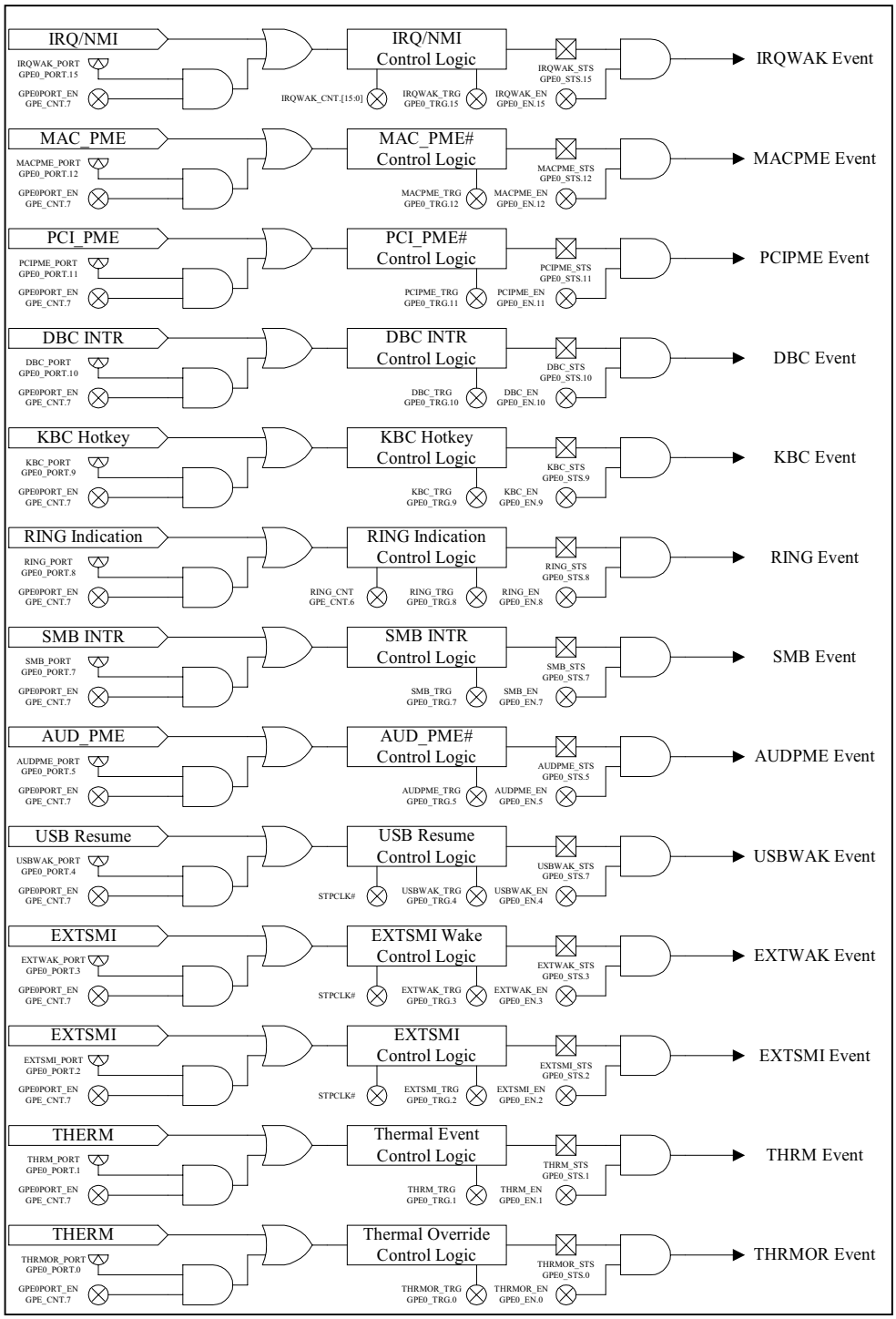


Figure 11-2. Hardware Model for Generic Fixture 0 (GPE0)

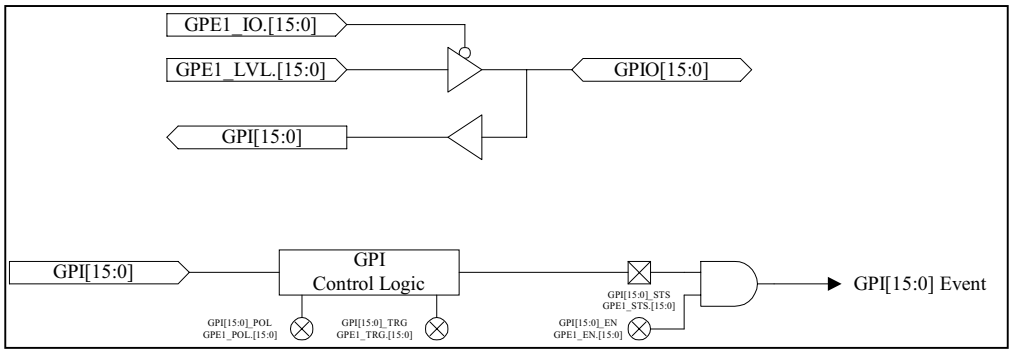


Figure 11-3. Hardware Model for Generic Feature 1 (GPE1)

11.3 The Interrupt Event of ACPI

Hardware platforms that want to support both legacy operating system and ACPI systems must provide a way of re-mapping the interrupt events between SMIs and SCIs when switching between ACPI and legacy models. This is illustrated in Figure 9-5.

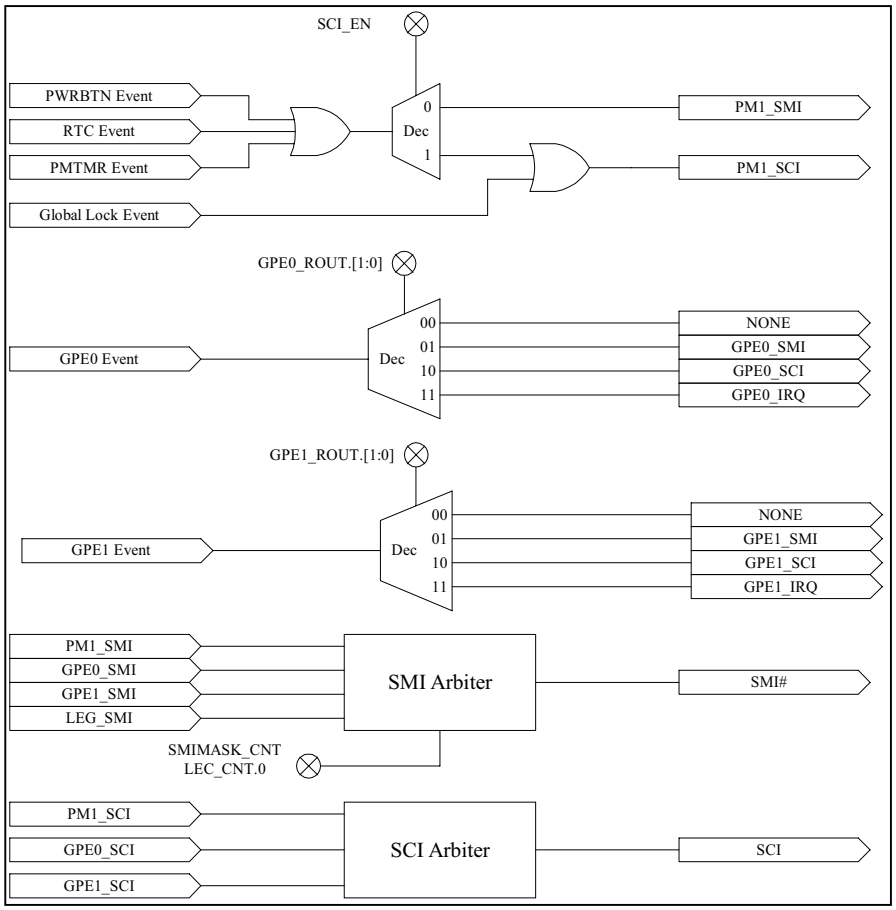


Figure 11-1. Interrupt Model for ACPI

11.4 The Sleeping/Wake Event of ACPI

The sleeping/wake logic consists of logic that will sequence the system into the defined low-power hardware sleeping state and will awaken the system back to the working state upon a wake event. While in any of the sleeping state, an enabled “Wake” event will cause the hardware to sequence the system back to the working state and WAK_STS will be set. When waking from the S1 sleeping state, execution control is passed backed to the ACPI driver immediately, whereas when waking from S2-S5 states execution control is passed to the BIOS software. The WAK_STS bit provides a mechanism to separate the ACPI driver’s sleeping and waking code during an S1 sequence. Figure 9-6 shows the Sleeping/Wake model for ACPI.

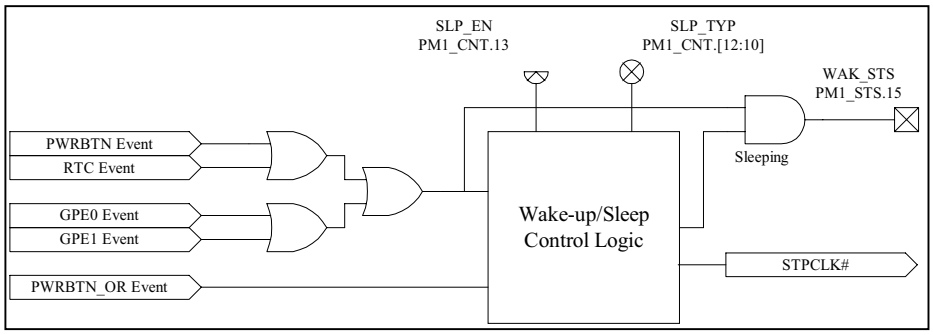


Figure 11-1. Sleeping/Wake model for ACPI

11.5 Types of ACPI Events

At the direct ACPI hardware level, two types of events can be signaled by an SCI interrupt:

- Fixed ACPI events
- General-purpose events

11.5.1 Fixed ACPI Events Handling

When the ACPI driver receives a fixed ACPE event, it directly handles the event by itself. The ACPI driver owns all the fixed resource registers, and these registers are not manipulated by ASL/AML code. Registers must be accessed by byte granularity.

11.5.2 General-purpose Events Handling

When the ACPI driver receives a general-purpose event, it either passes control to an ACPI-aware driver (such as PCI bus driver), or uses an OEM-supplied control method to handle the event. **The ACPI driver manages the bits in the GPEx blocks directly**, although the source to those events is not directly known and is connected into the system by control methods. When the ACPI driver receives a general-purpose event, the ACPI driver does the following:

1. Disables the interrupt source (GPEx_EN).
2. If an edge event, clears the status bit.
3. Performs one of the following:
   - Dispatches to an ACPI-aware device driver.
   - Queues the matching control method for execution
   - Manages a wake event using device _PRW objects
4. If a level event, clears the status bits.
5. Enables the interrupt source.

The OEM AML code can perform OEM-specific functions custom to each event the particular platform might generate by executing the control method that matches the event. For GPE events, the ACPI driver will execute the control method of the name _GPE._Txx.

11.6 Examples

To illustrate how these OS native drivers interact in ACPI, consider an integrate modem and a PCI network add-on card. The power states of these two devices are defined as follows:

Integrate Modem:

- D0

Modem controller on

Phone interface on

Speaker on

Can be on hook or off hook

Can be waiting for answer

- D3

Modem controller off (context lost)

Phone interface in low power mode

Speaker off

On hook

- Power Policy for the modem

D0 to D3: Modem put in answer mode

D3 to D0: Application requests dial or the phone rings while the modem is in answer mode

PCI network add-on card

- D0

MAC fully on

PHY fully on

- D3

MAC transmit logic off (context lost)

PHY fully on

- Power Policy for the PCI network add-on card

D0 to D3: Application put MAC in low power mode

D3 to D0: Application requests MAC back to normal operation mode or MAC receives a wake up event

11.6.1 Hardware Model of Integrate Modem and PCI Network Card

When a PCI function wants to request a change of its power consumption state, it asserts PME#. Typically, a device uses a PME# to request a change from a power savings state to the fully operational state. The PME# is tied GPE11 directly. Each device on PCI Bus must provide its second-level status and enable bit, which is defined in PCI PMCSR. The OS enables or disables the PME# wake function by enabling or disabling its corresponding GPE11 and by executing its _PSW control method which is used to take care of the second-level enable bits. When the GPE11 is asserted, the OS still executes the corresponding GPE11 control method that determines which device wakes are asserted and notifies the corresponding device objects. The native OS driver is then notified that its device has asserted wake, for which the driver powers on its device to service it.

When an embedded controller (integrate modem in this case) wants to change its power state, it can assert its own power management events, which ties to GPE5 directly. The OS will follow the same step as PME# which describe above.

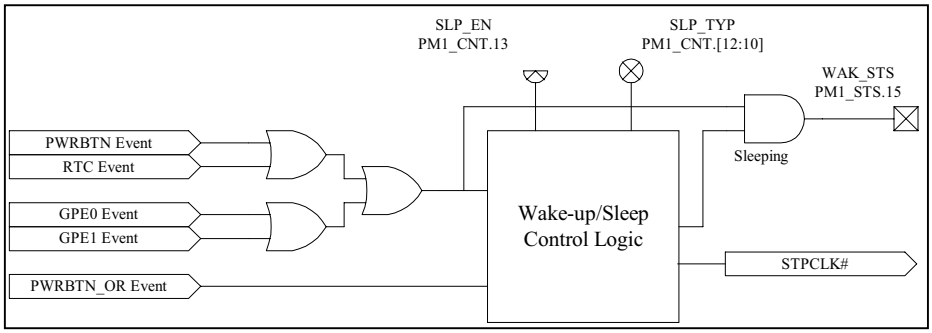


Figure 11-1. Hardware Model for PME#

11.6.2 The System Enter S1 Sleeping State

On a transition of the system from S0 state to S1 state, the following occurs:

1. The OS decides to place the system into the sleeping state.

2. The OS examines all devices that are enabled to wake up the system and determines the deepest possible sleeping state the system can enter to support the enabled wakeup functions. The _PRW named object under each device is examined, as well as the power resource object it points to.

3. The OS executes the Prepare to Sleep (_PTS) control method, passing an argument that indicates desired sleeping state (S1 in this case).

4. The OS places all device drivers into their respective Dx state. If the device is enabled for wakeup, it enters the Dx state associated with the wakeup capability. If the device is not enabled to wakeup the system, it enters the D3 state. In this case, the integrate modem and the PCI network card are capable of waking the system from D3, these two devices will be placed in D3 by their own driver.

5. OS saves the processor's context to memory.
6. OS writes the waking vector into the FACS table in memory.
7. OS clears the WAK_STS in the PM1_STS.
8. OS writes SLP_TYP as "001", then set SLP_EN in PM1_CNT.
9. The system enters the S1 sleeping state.

The IA processor that supports the S1 state through the assertion of the STPCLK# signal. In this case, the system clocks (CPU and PCI) are still running and no power sources are switched off.

11.6.3 The System Exit S1 Sleeping State

When the integrated modem or PCI network card receives its wakeup event and signals its wake signal, the GPE status bit used to track that device is set. Following shows the procedure for a GPE event to sequence the system back to S0.

1. While the corresponding general-purpose enable bit is enabled, the SCI interrupt is asserted.

2. Because the system is sleeping, this will cause the hardware to transition the system into the S0 state and WAK_STS will be set.

3. Once the system is running, ACPI will disable the GPE_EN and dispatch the corresponding GPE handler. In this case, because the integrate modem and PCI network card are all PCI devices, ACPI driver will dispatch PCI bus driver to handle these two events.

4. The PCI bus driver needs to determine which device object has signaled wake, disabled the second level power management event (MDM_EN or LAN_EN), and performs a wake Notify operation on the corresponding device object that have asserted wake. Before PCI bus driver return control to ACPI driver, it must clear the status bit (MDM_STS or LAN_STS), which assert the wake event and enable the power management again (MDM_EN or LAN_EN).

5. In turn the OS will notify the OS native driver(s) for each device that will wake its device to service it. **Note that all devices must be placed in D0 when the system is sequenced to S0 from sleeping state (S1-S5).**

11.6.4 The Integrate Modem enters D3/S0 State

Following shows the procedure when the application decides to place the integrate modem in answer mode (D3 state):

1. The modem driver must send the command to enable the wakeup function of Modem or Network card.

2. The PCI bus driver receive the command from modem driver and decide to enable MDM_EN bit in modem PMCSR register. Then the bus driver calls the ACPI driver to enable the wakeup function of the integrate modem.

3. ACPI driver will run PCI's PSW object and enable the GPE5 event (GPE5_EN).

4. The modem sends the command to put the device in D3 state, and the mini-driver must save all registers of the modem controller.

5. Then PCI driver must set D3 bit in modem's PMCSR register and call ACPI driver.

6. If the integrate modem contain _PS3 and _PW3 under its name space, the ACPI driver will execute them.

11.6.5 The PCI LAN Card enters D3/S0 State

When the LAN driver decides to put the LAN card into D3 state, it takes the same procedure as the integrate modem. Except that it won't contain any object under its name space (_PSx, PWx). The LAN driver must execute all command to put the LAN device into D3 state. The ACPI driver only enable the GPE11_EN and monitor the power state of the system to decide whether the system must enter sleeping state or not.

11.6.6 When The Modem Detects Phone Call

If the integrate modem detects a phone call when it is in answer mode (D3 state), it must take the following procedure to wake the modem controller.

1. The wakeup event detection logic sets MDM_STS, and GPE5_STS will be set by this wakeup event.

2. While GPE5 event asserts, the SCI will be triggered by this event and ACPI driver will handle this general-purpose event.

3. The ACPI driver finds the source of the general-purpose event and disables this event (GPE5_EN). Then ACPI driver dispatches the PCI bus driver.

4. PCI bus driver polls all PMCSR registers on PCI bus and find that the modem asserts the wakeup event. The bus driver clears MDM_EN and calls the modem driver.

5. The modem driver clears MDM_STS and sends command to put the modem controller in D0.

6. The PCI bus driver then set D0 bit in the modem's PMCSR and call the modem driver to service the phone call.

11.6.7 When The PCI LAN Card Detects a Wakeup Event

When the PCI LAN Card detects a wakeup event, it will set LAN_STS and assert PME#. The GPE11 event will be triggered and the ACPI driver will take the same action to service the general-purpose event.

Revision History

Preliminary v.0.9 (3/14/2002) –

Added the introduction of global view and CPU core.

Added Pin Lists sorted by ball number and Pin name.

Refined the Pin Description.

Added the Programming Guide.

Majority of changes were to Electrical Characteristics section.

Added the Instruction Throughput.

Added the Throttling Features.

Changed the Package Outlines to 686-pin package.

Appended the description of ACPI.

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