Lab 3: OPAMP based Active circuits

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Date: 20-January-2017

In this lab, you will work on active rectifiers. Active circuit offers output voltage level to be equal to or greater than input voltage level. Passive circuits provides an attenuated output voltage level.

Half wave rectifier

Build the circuit as shown in Figure 1 using opamp 741. Apply Vin of 4Vp-p, Sine signal with 1 kHz frequency. Capture and plot both input and output voltage with respect to time domain. Check whether the output voltage level is as you had expected. Is this half wave or full wave rectifier ? Could you reduce the ripple voltage of the circuit to less than 1 Vp-p.

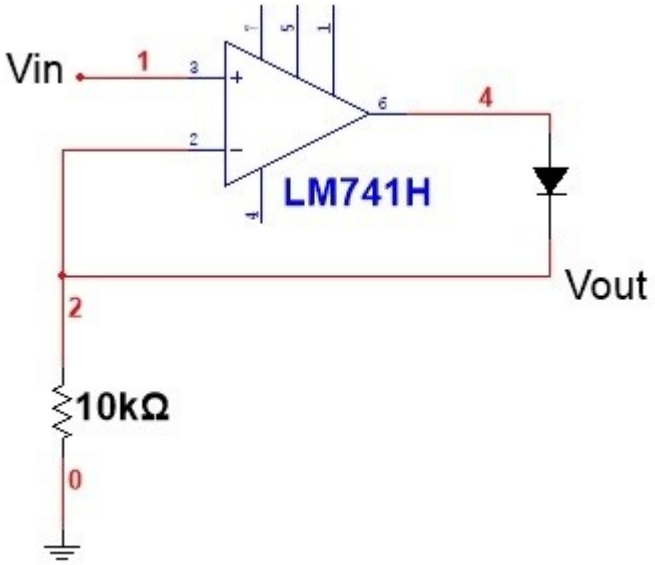

Figure 1: Schematic of rectifier circuit.

Another Rectifier

Build the circuit as shown in Figure 2 in breadboard. Apply Vin of 4Vp-p, Sine signal with 1 kHz frequency. Capture and plot both input and output voltage with respect to time domain. Check whether the output voltage level is as you had expected. Does this circuit behave like a full wave rectifier ? Could you reduce the ripple voltage of the circuit to less than 1 Vp-p.

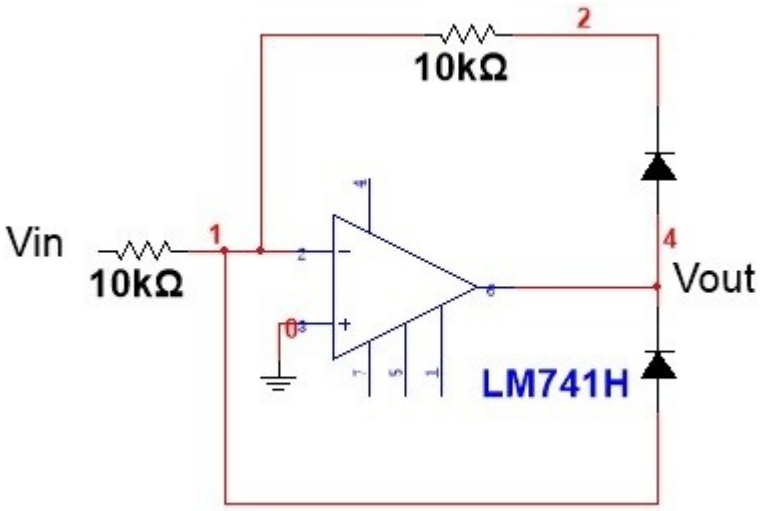

Figure 2: Schematic circuit diagram of rectifier circuit.

Clamper

Build the circuit as shown in Figure 3 in breadboard. Apply Vin of 4Vp-p, Sine signal with 1 kHz frequency. Set the potentiometer to 50 KΩ. Capture and plot both input and output voltage with respect to time domain. Check whether the DC component of the output voltage level changes when the potentiometer knob is changed.

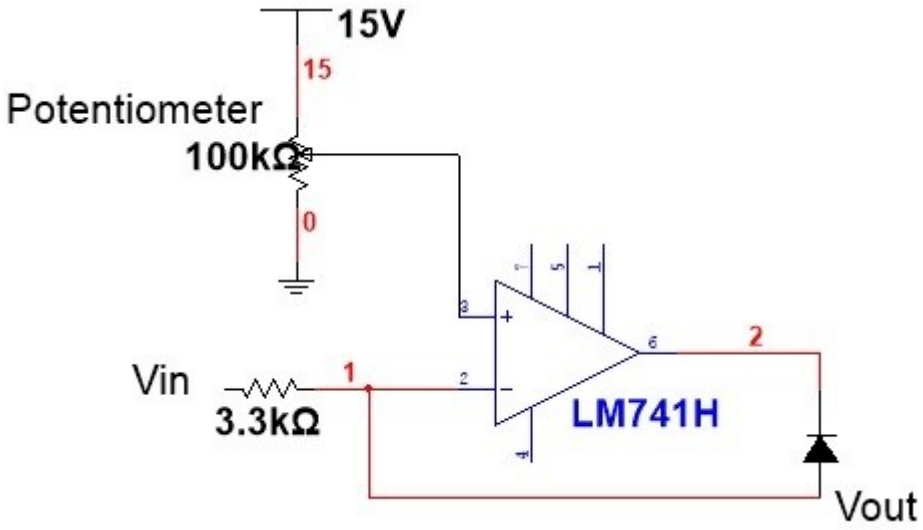

Figure 3: Schematic circuit diagram of active clamper circuit.

The lab report#2 and lab report#3 are due by 4th February, 2017 by 11:59:59 AM.