project2-expected results

#cycle	operation	IF	ID	EX	MEM	WB	changes in register file
1	1. addi $t0, $zero, 0x20	1	x	x	x	x	nothing
2	2. addi $t1, $zero, 0x37	2	1	x	x	x	nothing
3	3. and $s0, $t0, $t1	3	2	1	x	x	nothing
4	4. or $s0, $t0, $t1	4	3	2	1	x	nothing
5	5. sw $s0, 4($zero)	5	4	3	2	1	t0 = 0x20
6	6. sw $t0, 8($zero)	6	5	4	3	2	t1 = 0x37
7	7. add $s1, $t0, $t1	7	6	5	4	3	s0 = 0x20
8	8. sub $s2, $t0, $t1	8	7	6	5	4	s0 = 0x37, DataMemory[4] = 0x37
9	9. beq $s1, $s2, error0 (does not branch)	9	8	7	6	5	DataMemory[8] = 0x20
10	10. lw $s1, 4($zero)	10	9	8	7	6	nothing
11		10	9	nop	8	7	s1 = 0x57
12	11. andi $s2, $s1, 0x48	11	10	9	nop	8	s2 = 0xfffffe9
13	12. beq $s1, $s2, error1	12	11	10	9	nop	nothing

14		12	11	nop	10	9	nothing
15	13. lw $s3, 8($zero)	13	12	11	nop	10	s1 = 0x37
16		13	12	nop	11	nop	nothing
17	14. beq $s0, $s3, error2 (does not branch)	14	13	12	nop	11	s2 = 0x0
18	15. slt $s4, $s2, $s1 (Last)	15	14	13	12	nop	nothing
19		15	14	nop	13	12	nothing
20		15	14	nop	nop	13	s3 = 0x20
21	16. beq $s4, $0, EXIT (does not branch)	16	15	14	nop	nop	nothing
22	17. add $s2, $s1, $0	17	16	15	14	nop	nothing
23		17	16	nop	15	14	nothing
24	18. j Last	18	17	16	nop	15	s4 = 0x1
25	19. addi $t0, $0, 0(error0)	19	18	17	16	nop	nothing
26	15. slt $s4, $s2, $s1 (Last)	15	flushed (nop)	18	17	16	nothing
27	16. beq $s4, $0, EXIT (branch)	16	15	flushed (nop)	18	17	s2 = 0x37
28	17. add $s2, $s1, $0	17	16	15	flushed (nop)	18	nothing
29		17	16	nop	15	flushed (nop)	nothing
30	EXIT (nop)	EXIT (nop)	flushed (nop)	16	nop	15	s4 = 0x0

31	EXIT (nop)	EXIT (nop)	EXIT (nop)	flushed (nop)	16	nop	nothing
32	EXIT (nop)	EXIT (nop)	EXIT (nop)	EXIT (nop)	flushed (nop)	16	nothing
33	EXIT (nop)	EXIT (nop)	EXIT (nop)	EXIT (nop)	EXIT (nop)	flushed (nop)	nothing