

Exp no:1	Title: Verification of truth table of logic gates
Date: 26-08-2021	

### Aim:

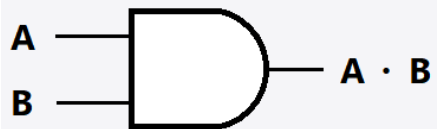
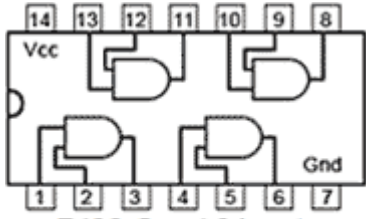
This experiment will examine the operation of the OR, AND, NOT, NAND, NOR and XOR logic gates and compare the expected outputs to the truth tables using simulation results.

### Required tools:

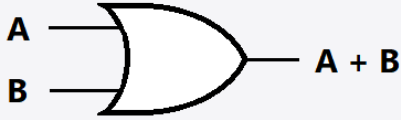
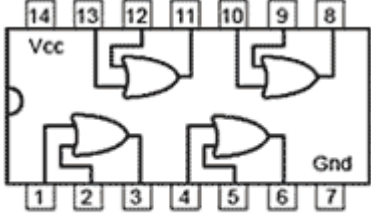
Multisim online circuit simulator

### Theory:

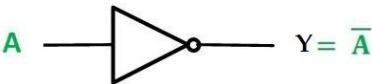
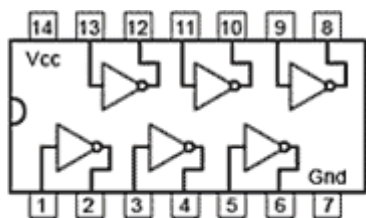
AND gate:

Symbol	Truth table	IC diagram															
	<table border="1"> <thead> <tr> <th>A</th><th>B</th><th>Y=A.B</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>0</td></tr> <tr> <td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	Y=A.B	0	0	0	0	1	0	1	0	0	1	1	1	 <p>7408 Quad 2 input AND Gates</p>
A	B	Y=A.B															
0	0	0															
0	1	0															
1	0	0															
1	1	1															

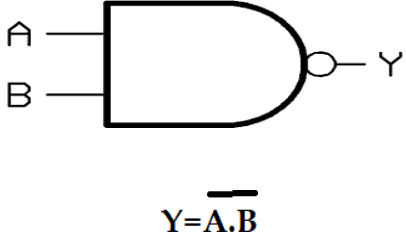
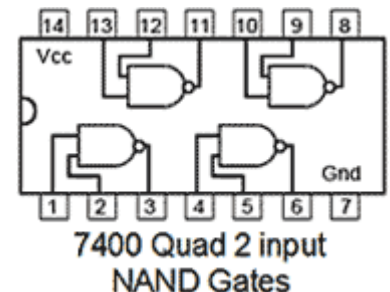
OR gate:

Symbol	Truth table	IC diagram															
	<table border="1"> <thead> <tr> <th>A</th><th>B</th><th>Y=A+B</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	Y=A+B	0	0	0	0	1	1	1	0	1	1	1	1	 <p>7432 Quad 2 input OR Gates</p>
A	B	Y=A+B															
0	0	0															
0	1	1															
1	0	1															
1	1	1															

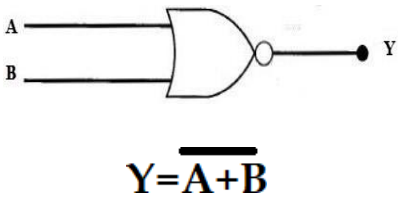
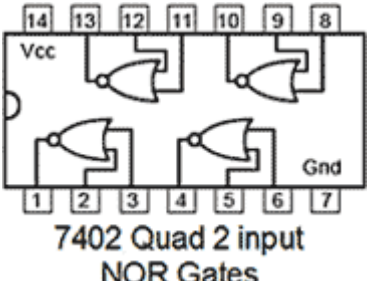
NOT gate:

Symbol	Truth table	IC diagram						
	<table><thead><tr><th>A</th><th>Y</th></tr></thead><tbody><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></tbody></table>	A	Y	0	1	1	0	 <p>7404 NOT Gates (Inverters)</p>
A	Y							
0	1							
1	0							

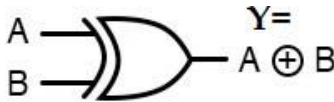
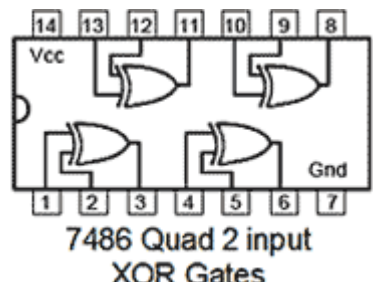
NAND gate:

Symbol	Truth table	IC diagram															
 $Y = \overline{A \cdot B}$	<table border="1"> <thead> <tr> <th>A</th><th>B</th><th>Y</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	Y	0	0	1	0	1	1	1	0	1	1	1	0	 <p>7400 Quad 2 input NAND Gates</p>
A	B	Y															
0	0	1															
0	1	1															
1	0	1															
1	1	0															

NOR gate:

Symbol	Truth table	IC diagram															
 $Y = \overline{A + B}$	<table border="1"> <thead> <tr> <th>A</th><th>B</th><th>Y</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>0</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	Y	0	0	1	0	1	0	1	0	0	1	1	0	 <p>7402 Quad 2 input NOR Gates</p>
A	B	Y															
0	0	1															
0	1	0															
1	0	0															
1	1	0															

XOR gate:

Symbol	Truth table	IC diagram															
 $Y = A \oplus B$	<table border="1"> <thead> <tr> <th>A</th><th>B</th><th>Y</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	Y	0	0	0	0	1	1	1	0	1	1	1	0	 <p>7486 Quad 2 input XOR Gates</p>
A	B	Y															
0	0	0															
0	1	1															
1	0	1															
1	1	0															

**Results:**

AND gate:

A	B	Y	Simulation result
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

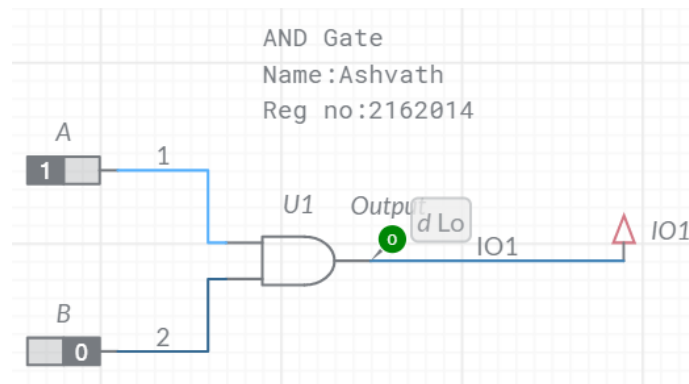


Figure: Verification of AND gate

OR gate:

A	B	Y	Simulation result
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

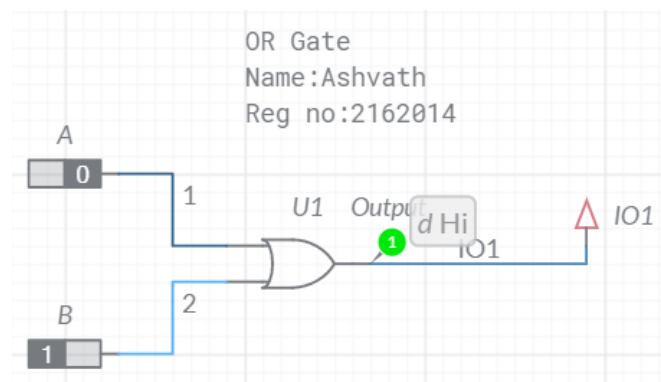


Figure: Verification of OR gate

NOT gate:

A	Y	Simulation result
0	1	1
1	0	0

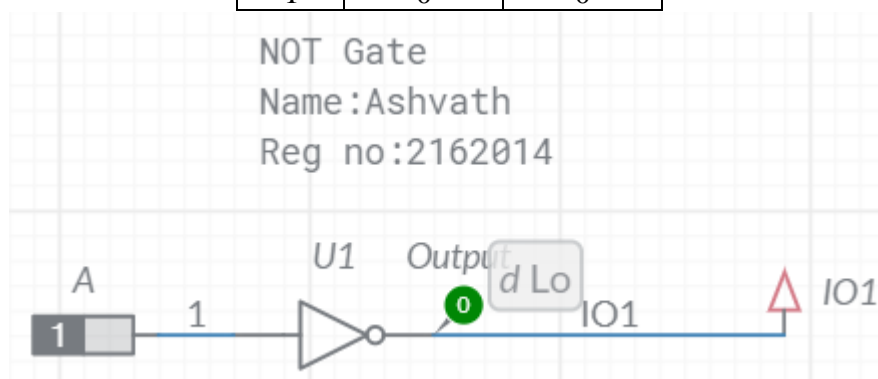


Figure: Verification of NOT gate

NAND gate:

A	B	Y	Simulation result
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

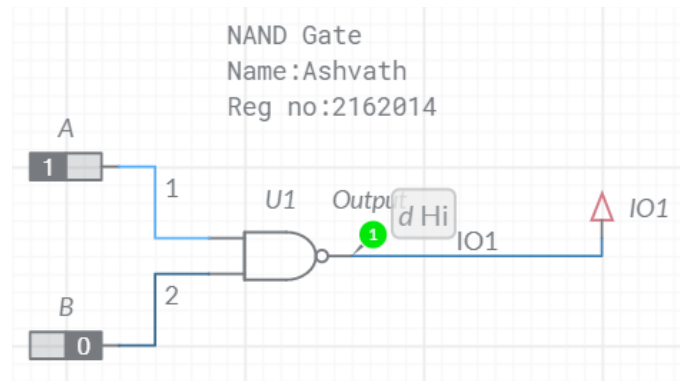


Figure: Verification of NAND gate

NOR gate:

A	B	Y	Simulation result
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

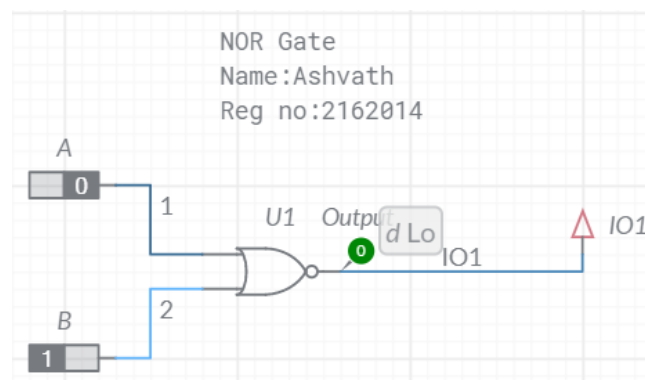


Figure: Verification of NOR gate

XOR gate:

A	B	Y	Simulation result
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

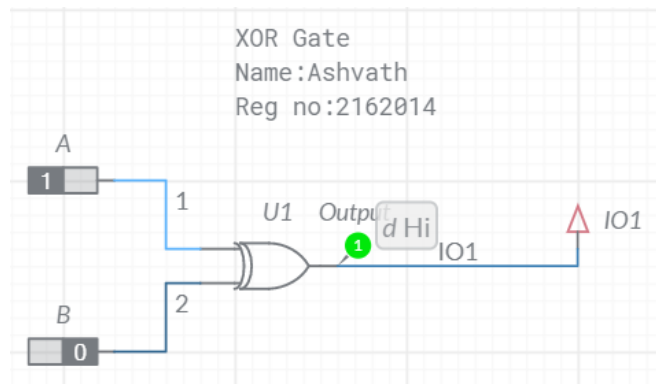


Figure: Verification of XOR gate

### Inference:

The truth tables of all the logic gates are verified through multisim online simulator successfully.

Student signature:

S. P Ashvath

Marks:

Faculty signature: