

Logic Gates:

AND Gate:

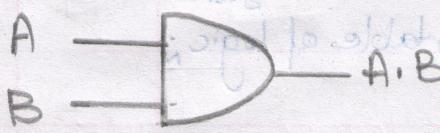


Figure : Symbol

A	B	A · B
0	0	0
0	1	0
1	0	0
1	1	1

Figure : Truth Table

OR Gate:

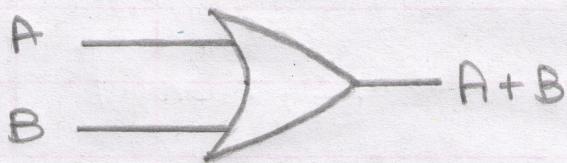


Figure : Symbol

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

Figure : Truth Table

NOT Gate:

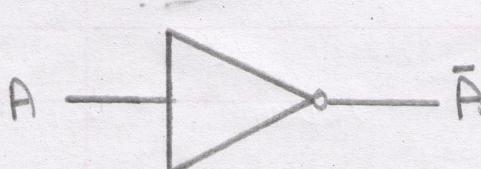


Figure : Symbol

A	\bar{A}
0	1
1	0

Figure : Truth Table

Exp No: 1
Date:
26-08-2021

Title : Verification of truth table
of logic gates

Aim:

This experiment will examine the operation of the OR, AND, NOT, NAND, NOR and XOR logic gates and compare the expected outputs to the truth tables using simulation results.

Required tools:

Multisim Online Circuit Simulator

Verification of truth tables with Simulator results

NAND Gate.

A	B	Y	Simulation result
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

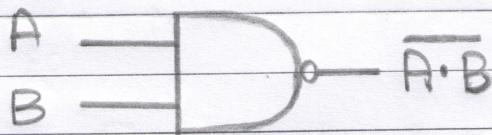
OR gate

A	B	Y	Simulation result
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

NAND Gate: ~~not~~ $A \cdot B$

zotop signal to

otop

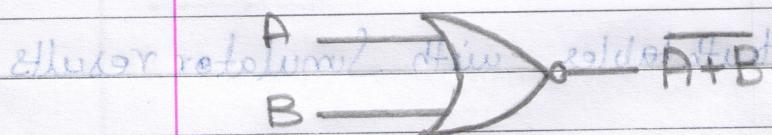


A	B	$\overline{A \cdot B}$
0	0	1
0	1	1

zitovope off program bin from 10001 zit 0 1
 90x bin Figure: Symbol, T01, AND, 1 1 1 0
 of zotop kategope off program bin zotop signal
 . Fluor zitolumi eric figure & Truth Table

NOR Gate:

zotolumi 2 tivrd enin0 mizib0 M



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Figure : Symbol

fluor zitolumi X 8 A
figure: Truth Table

XOR Gate:

0 0 0
0 0 1
0 1 1
1 0 1
1 1 0



A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Figure : Symbol

fluor zitolumi X B
Figure: Truth Table

NOT Gate:

A	Y	Simulation result
0	1	1
1	0	0

NAND Gate:

A	B	Y	Simulation result
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

NOR Gate:

A	B	Y	Simulation result
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

XOR Gate:

A	B	Y	Simulation result
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Inference:

The truth tables of all the logic gates are verified through multisim online simulator successfully.

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