Exp No:1 Title: Verification of truthtable of logic gates Date: 26-08-21 Aim: you have written this in the lab Required tools: written in the dab Logic gates: AND gate: Sizy Koth Xold OR gate: Side Suntage NOT gate:

35

Last take

NAND gate
symbol
symbol
symbol

Kentrage

NOR gate

KrithEorle

XOR gate

Krimoke

Verification of truthtables with simulation

results

AND gate

1				
je .	A	B	4	Simulation result
	0	0	0	ව
		0	Ø	0
	1	1		
L		1	1	

4	A	В	4	Simulation	result
					3
\	1		1		لول

NOT gate

A	Y '	Simulation	result
Ø	ţ	1	
1	0	0	ل_ ا

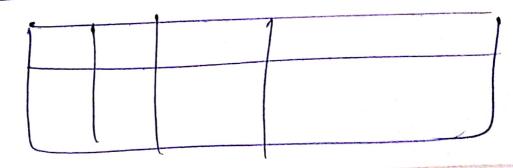
NAND gate

1	A	B	7	Simulation result
	l			

NOR gate

•	A	B	4	Simulation	Huzur-
			1		

XOR gate



Inference:

write as given in record

Student signature:

× put signature hore

(Name: Eshmehar Singh)