Exp no:1	Title: Verification of truth table of logic gates
Date: 26-08-2021	

Aim:

This experiment will examine the operation of the OR, AND, NOT, NAND, NOR and XOR logic gates and compare the expected outputs to the truth tables using simulation results.

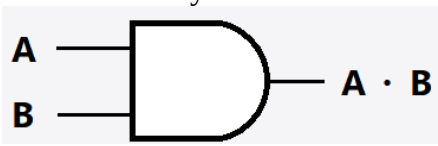
Required tools:

Multisim online circuit simulator

Theory:

AND gate:

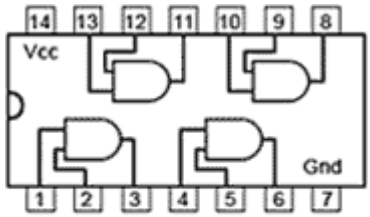
Symbol



Truth table

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

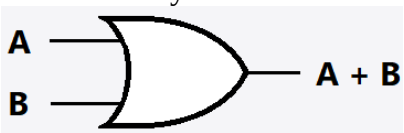
IC diagram



7408 Quad 2 input AND Gates

OR gate:

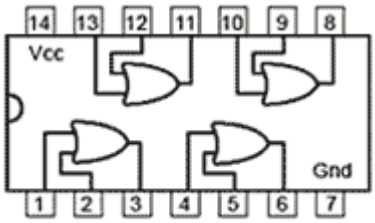
Symbol



Truth table

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

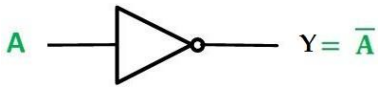
IC diagram



7432 Quad 2 input OR Gates

NOT gate:

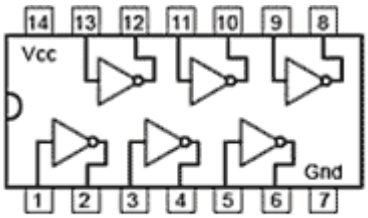
Symbol



Truth table

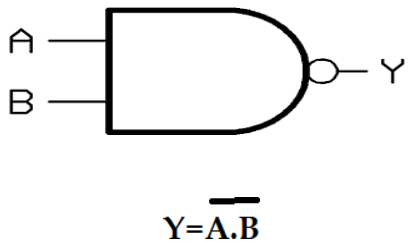
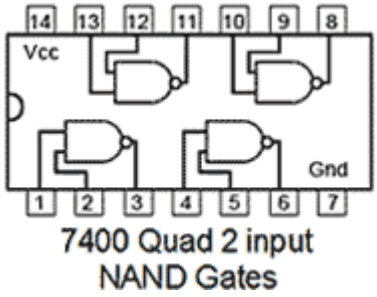
A	Y
0	1
1	0

IC diagram



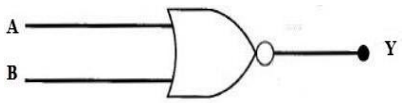
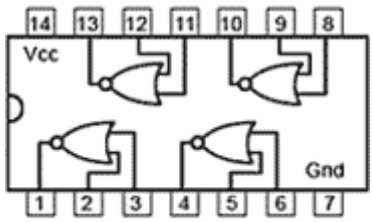
7404 NOT Gates (Inverters)

NAND gate:

Symbol	Truth table	IC diagram
 $Y=\overline{A.B}$		 7400 Quad 2 input NAND Gates

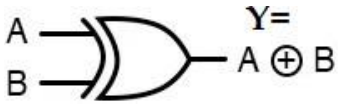
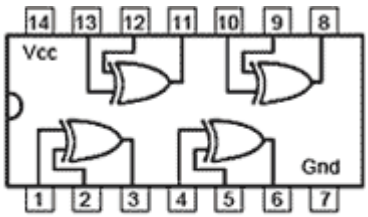
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR gate:

Symbol	Truth table	IC diagram
 $Y=\overline{A+B}$		 7402 Quad 2 input NOR Gates

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XOR gate:

Symbol	Truth table	IC diagram
		 7486 Quad 2 input XOR Gates

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Results:

AND gate:

A	B	Y	Simulation result
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

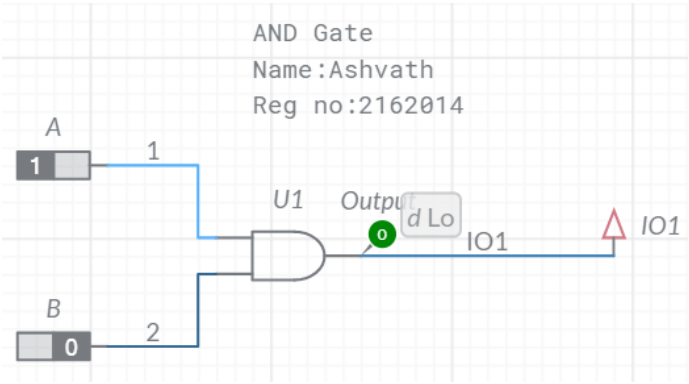


Figure: Verification of AND gate

OR gate:

A	B	Y	Simulation result
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

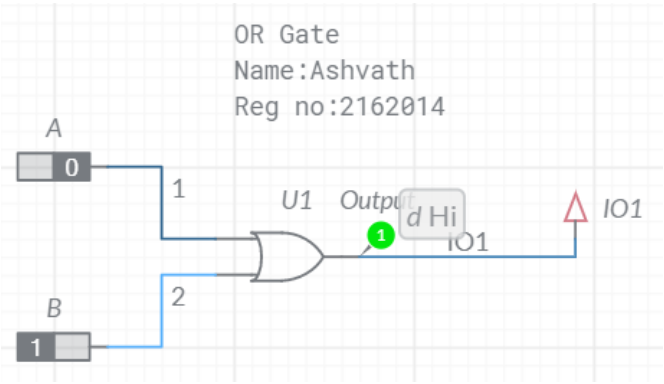


Figure: Verification of OR gate

NOT gate:

A	Y	Simulation result
0	1	1
1	0	0

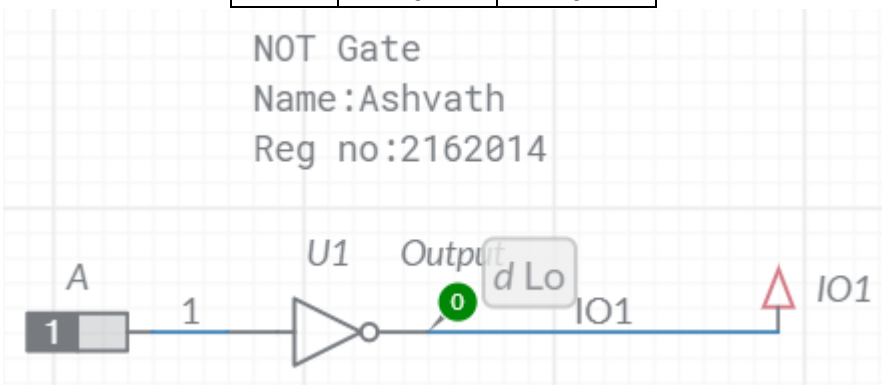


Figure: Verification of NOT gate

NAND gate:

A	B	Y	Simulation result
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

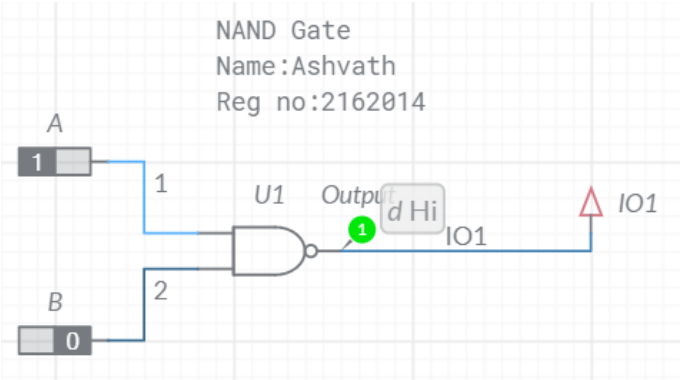


Figure: Verification of NAND gate

NOR gate:

A	B	Y	Simulation result
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

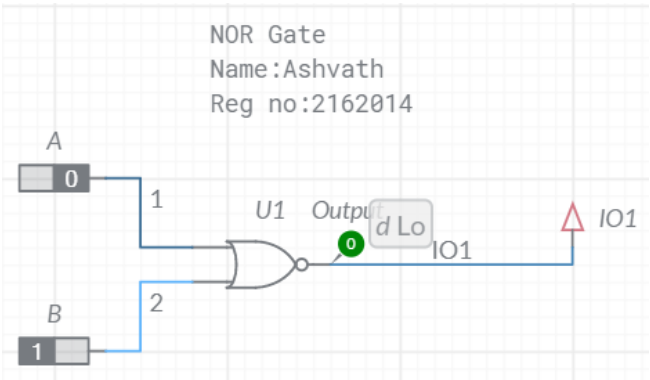


Figure: Verification of NOR gate

XOR gate:

A	B	Y	Simulation result
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

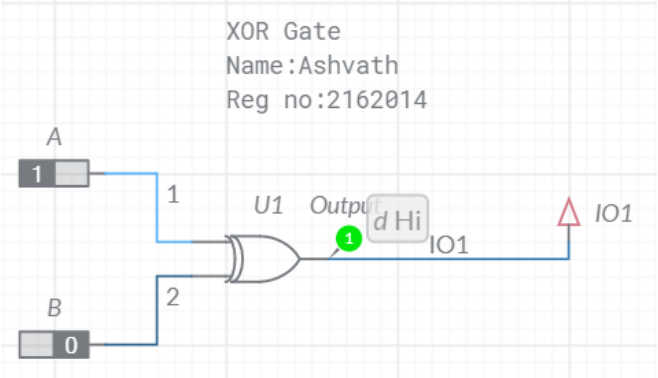


Figure: Verification of XOR gate

Inference:

The truth tables of all the logic gates are verified through multisim online simulator successfully.

Student signature:	Marks:
S.P Ashvath	Faculty signature:

Exp no:2	Title: Realization of logic circuits with Boolean expressions
Date: 02-09-2021	

Aim:

To realize the logic circuits and verify the output for the following Boolean expressions

(i) Y = (A+B)'C

(ii) Y = (A+B)(C+D)

Required tools:

Multisim online circuit simulator

Theory:

Boolean algebra as the calculus of two values is fundamental to computer circuits, computer programming, and mathematical logic, and is also used in other areas of mathematics. The most common computer architectures use ordered sequences of Boolean values, called bits, of 32 or 64 values. When programming in machine code, assembly language, and certain other programming languages, programmers work with the low-level digital structure of the data registers. These registers operate on voltages, where zero volts represent Boolean 0, and a reference voltage (often +5 V, +3.3 V, +1.8 V) represents Boolean 1. Such languages support both numeric operations and logical operations. Boolean algebra reduces the circuit complexity by utilizing Boolean properties and hence a complicated expression can be realized with simple circuit. As the number of logic gates used in the circuit are reduced, the power consumption is also less which a desirable requirement in the electronics world.

Results:

Comparison of theoretical results with simulation results for Y = (A+B)'C

A	B	C	A+B	(A+B)'	Y = (A+B)'C	Simulation result
0	0	0	0	1	0	0
0	0	1	0	1	1	1
0	1	0	1	0	0	0
0	1	1	1	0	0	0
1	0	0	1	0	0	0
1	0	1	1	0	0	0
1	1	0	1	0	0	0
1	1	1	1	0	0	0

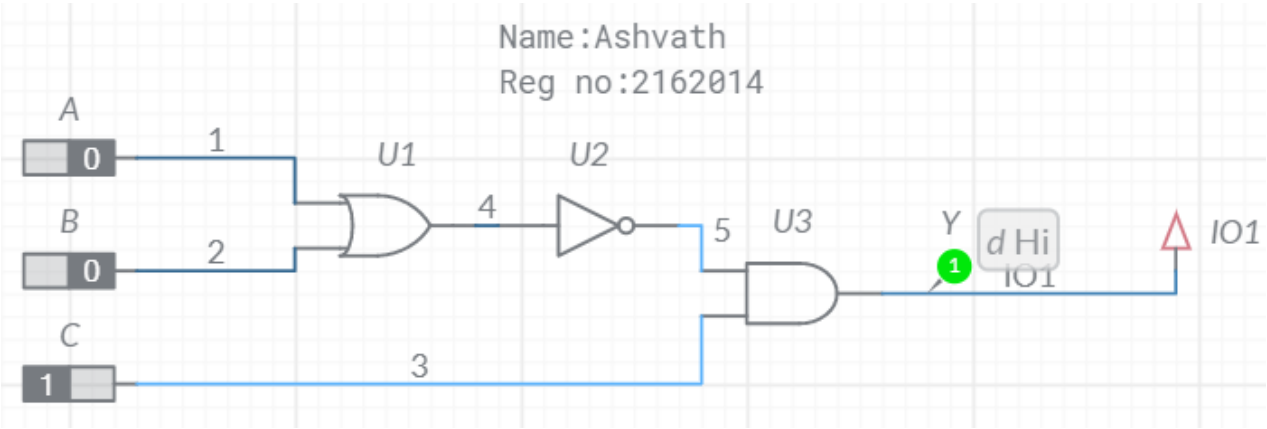


Figure: Logic circuit realization of (A+B)'C

Comparison of theoretical results with simulation results for Y = (A+B)(C+D)

A	B	C	D	A+B	C+D	Y = (A+B)(C+D)	Simulation result
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	0
0	1	0	0	1	0	0	0
0	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1
0	1	1	1	1	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1

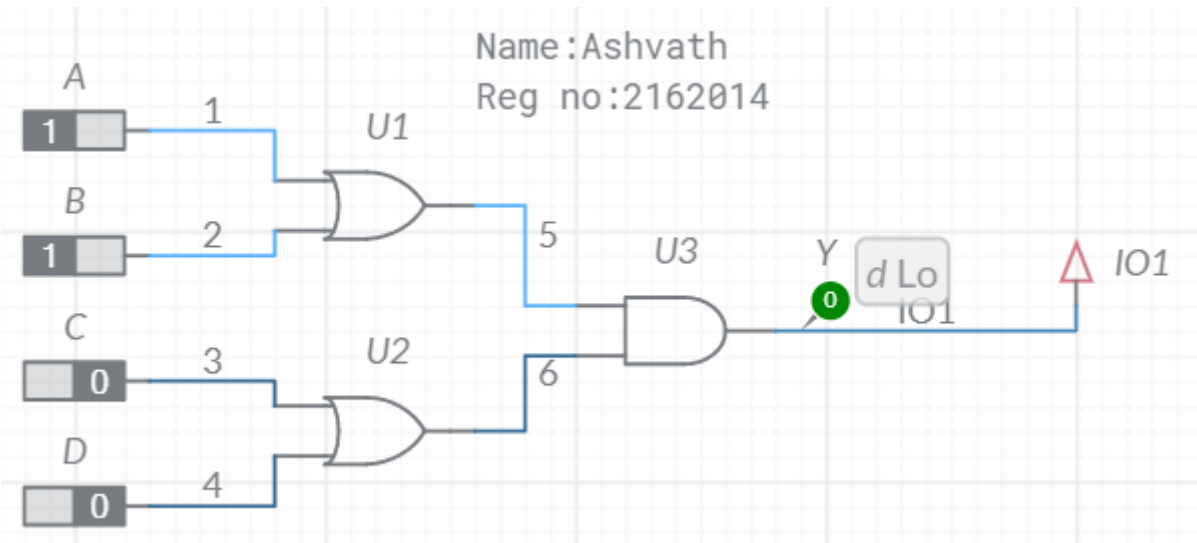


Figure: Logic circuit realization of (A+B)(C+D)

Inference:

The truth tables of two Boolean expressions are verified through multisim online simulator successfully.

Student signature: 	Marks: Faculty signature:

Exp no:3	Realization of half-adder and full-adder logic circuits
Date: 23-09-2021	

Aim:

To realize the half-adder and full-adder logic circuits and verify the simulation output with theoretical results.

Required tools:

Multisim online circuit simulator

Theory:

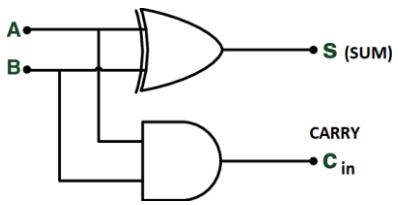
Half-Adder:

A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. The addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C_{in}. The Boolean functions describing the half-adder are:

$$S = A \oplus B$$

$$C_{in} = AB$$

Logic Diagram:



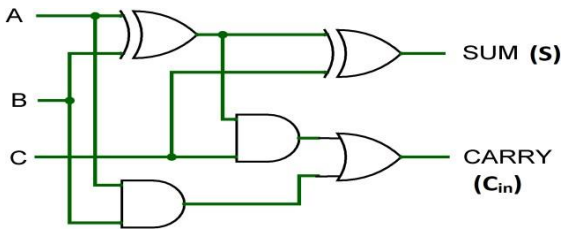
Full-Adder:

A combinational logic circuit that adds three data bits, A, B, and C is called a full-adder. The Boolean functions describing the full-adder are:

$$S = A \oplus B \oplus C$$

$$C_{in} = C(A \oplus B) + AB$$

Logic Diagram:



Results:

Comparison of theoretical results with simulation results for Half Adder

A	B	Theoretical result according to the expression		Simulation result	
		SUM	CARRY	SUM	CARRY
0	0	0	0	0	0
0	1	1	0	1	0
1	0	1	0	1	0
1	1	0	1	0	1

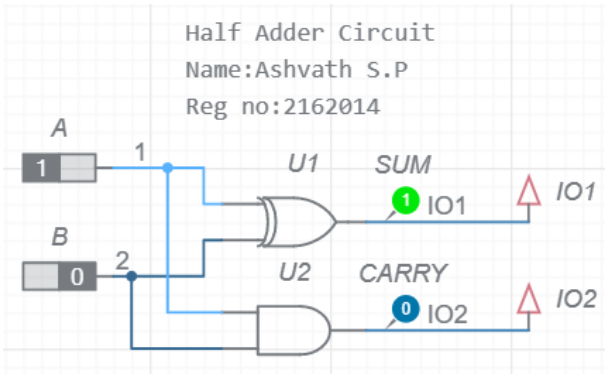


Figure: Logic circuit realization of Half-adder

Comparison of theoretical results with simulation results for Full Adder

A	B	C	Theoretical result according to the expression		Simulation result	
			SUM	CARRY	SUM	CARRY
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	1	1	1

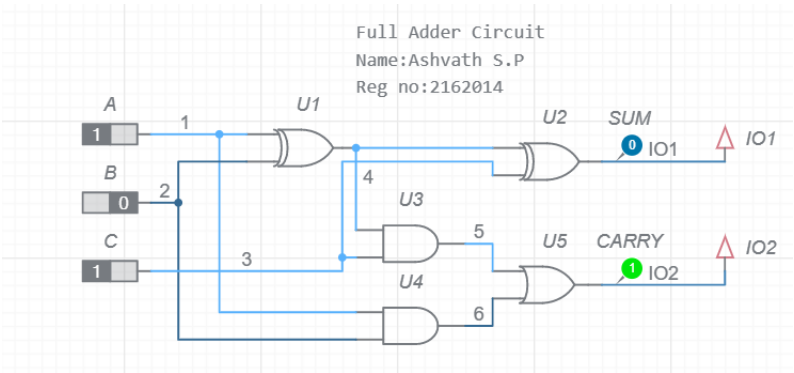


Figure: Logic circuit realization of full-adder

Inference:

The theoretical and simulation results of the truth table of half-adder and full-adder are in good agreement and verified successfully through multisim online simulator.

Student signature:	Marks:
S.P Ashvath	Faculty signature:

Exp no:4	Series and parallel connection
Date: 04-11-2021	

Aim:

To study the properties of series and parallel connection.

Required tools:

LTspice software tool

Theory:

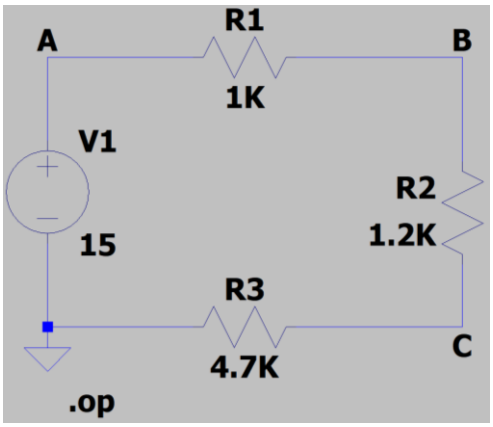
Series Circuit:

In a series circuit, the components are connected end-to-end in a line to form a single path through which current can flow. The defining characteristic of a series circuit is that there is only one path for current to flow.

Total Resistance, $R_T = R_1+R_2+R_3$

Total Current, $I_T = [V_S/(R_1+R_2+R_3)]$

Circuit Diagram:



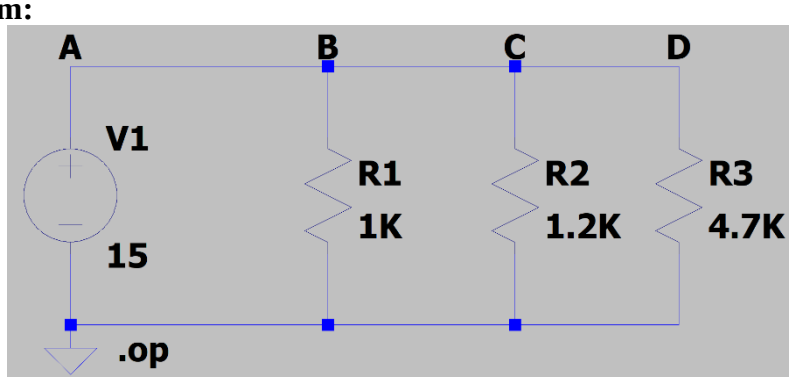
Parallel Circuit:

In a parallel circuit, all components are connected across each other's leads. There are many paths for current flow, but only one voltage across all components. The defining characteristic of a parallel circuit is that all components are connected between the same set of electrically common points.

Total Resistance, $(1/R_T) = [(1/R_1) +(1/R_2) +(1/R_3)]$

Total Current, $I_T = \{V_S/[(1/R_1) +(1/R_2) +(1/R_3)]\}$

Circuit Diagram:



Procedure:

1. Draw the series and parallel circuits in the LT Spice schematic.
2. Apply the voltage and resistance values.
3. Label the nodes at appropriate places in the circuit.
4. Go to simulate tab and select edit simulation command
5. Select operating point analysis in the edit simulation command.
6. Run the simulation

7. Calculate the potential difference across each resistor and check for $V_S=V_1+V_2+V_3$
8. Calculate the current through each resistor and check for $I_T=I_1+I_2+I_3$

Theoretical calculations:

Calculate the current through each resistor and check for $I_T=I_1+I_2+I_3$

$I_{(R1)}$ =0.015 A

$I_{(R2)}$ =0.0125 A

$I_{(R3)}$ =0.00319149 A

I_T = **0.0306915 A**

For $Vs=V_1+V_2+V_3$

$V_{(R1)} = V_{(a)} – V_{(b)}$ = 15 – 12.8621 = 2.1740 V

$V_{(R2)} = V_{(b)} – V_{(c)}$ = 12.8621 – 10.2174 = 2.6087 V

$V_{(R3)} = V_{(b)} – 0$ = 10.2174 – 0 = 10.2174 V

$V_S= V_{(R1)} + V_{(R2)} + V_{(R3)}$ = **15 V**

Comparison of theoretical values to the simulated values:

	Theoretical value	Simulated value
V_S (volt)	15	15
I_T (mA)	0.0306915	0.0306915

Result:

The properties of series and parallel circuits are studied through simulation and verified successfully.

Inferences:

The theoretical value is the same as the simulated value and hence verified successfully.

Student signature:	Marks:
	Faculty signature:

Exp no:5	Half wave rectifier and full wave rectifier
Date: 10-11-2021	

Aim:

1. To set up a half wave rectifier and to find the dc value of rectified voltage
2. To set up a full wave rectifier and to find the dc value of rectified voltage

Required tools:

LTspice software tool

Theory:

Half wave rectifier:

The half-wave rectifier circuit converts AC to pulsating DC. The name half-wave represents that it converts only one-half of the sinusoidal input**.**

$$V_{dc} = V_m/\pi$$

$$V_{rms} = V_m/2$$

Circuit Diagram:

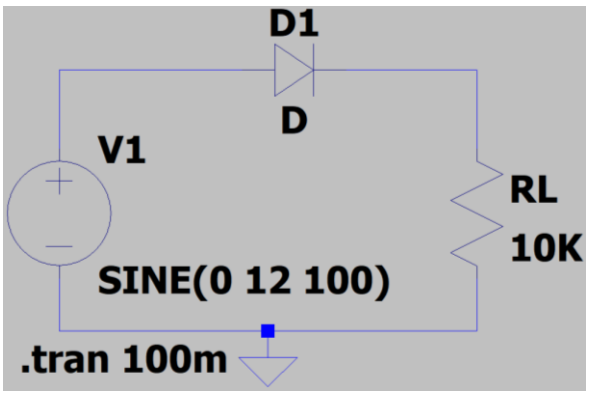


Fig: Half-wave rectifier

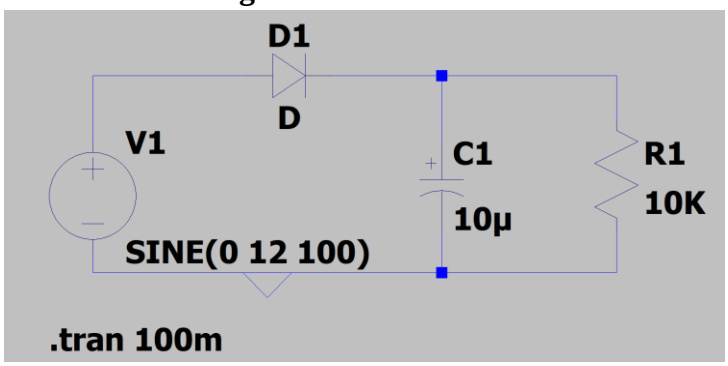


Fig: Half-wave rectifier with capacitor filter

Full wave rectifier:

The Full-wave rectifier circuit converts AC to pulsating DC. The name full-wave represents that it converts both halves of the sinusoidal input**.**

$$V_{dc} = 2V_m/\pi$$

$$V_{rms} = V_m/\sqrt{2}$$

Circuit Diagram:

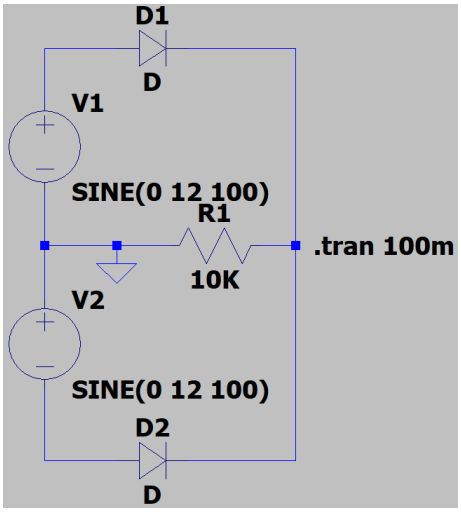


Fig: Full-wave rectifier

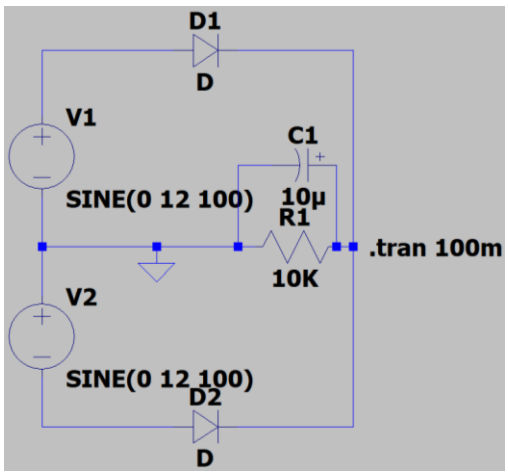


Fig: Full-wave rectifier with capacitor filter

Procedure:

1. Draw the circuit in LTspice schematic as shown in the circuit diagram for each rectifier circuit with and without rectifier.
2. Apply values to all the elements in the circuit.
3. Go to simulate tab, select tab edit simulation command, select transient analysis since we have to observe the waveform with respect to time.
4. Select the step time according to the frequency of input waveform.
5. Run the simulation.
6. Observe the input and output waveforms.
7. Calculate the V_m value by attaching the cursor to output waveform.
8. Calculate the V_{dc}, V_{rms}, ripple factor for Half wave and Full wave rectifier.

Model graph:

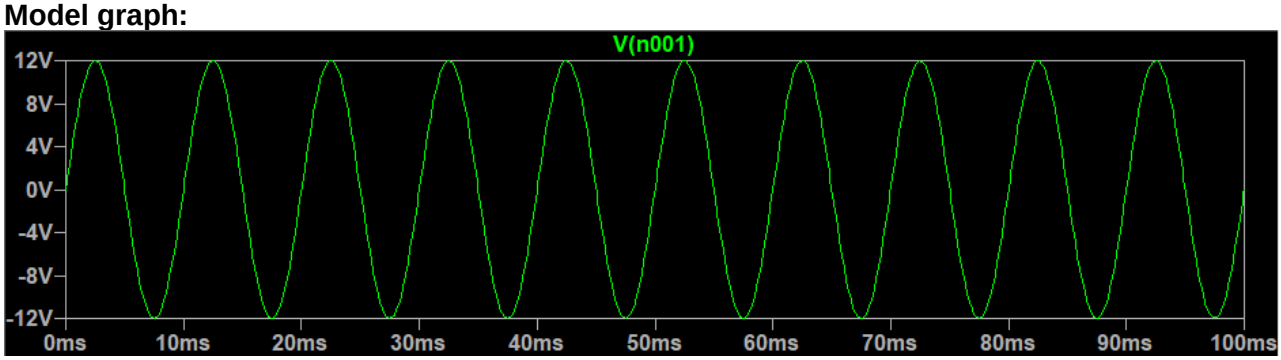


Fig: Input Waveform

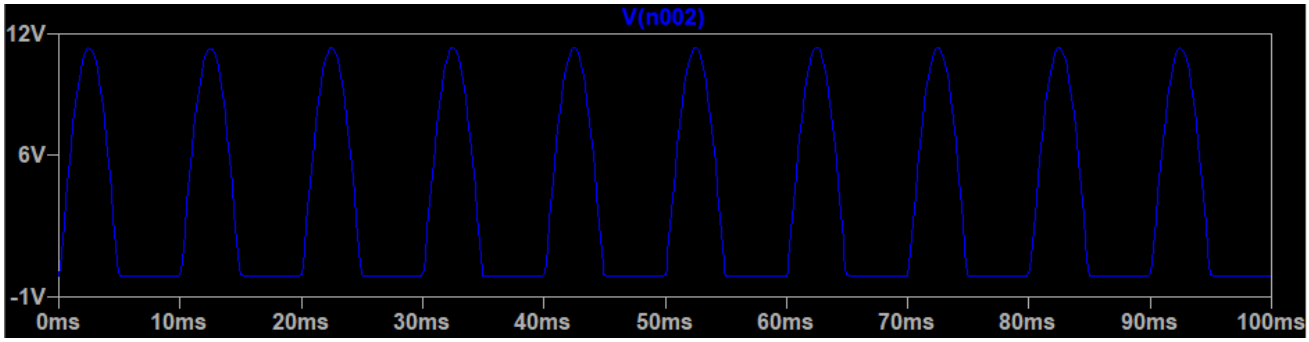


Fig: HWR ouput without filter

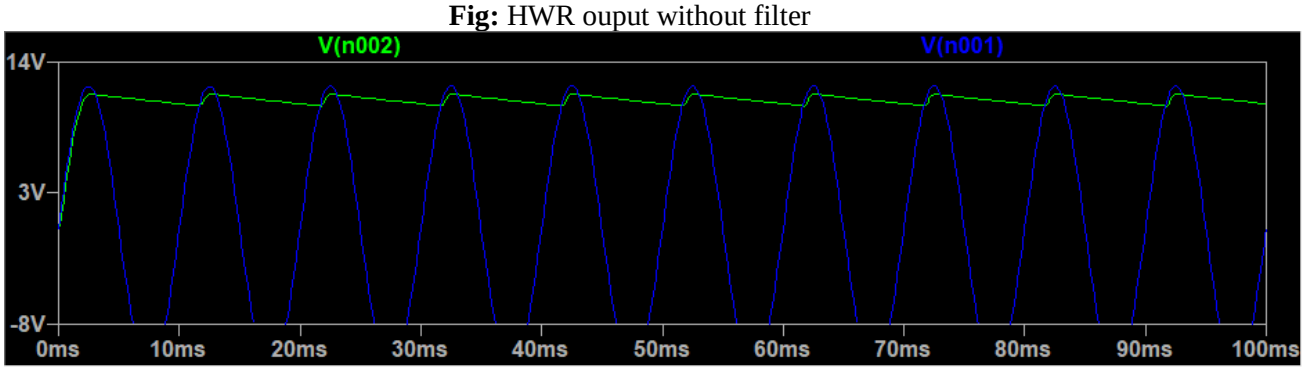


Fig: HWR ouput with filter

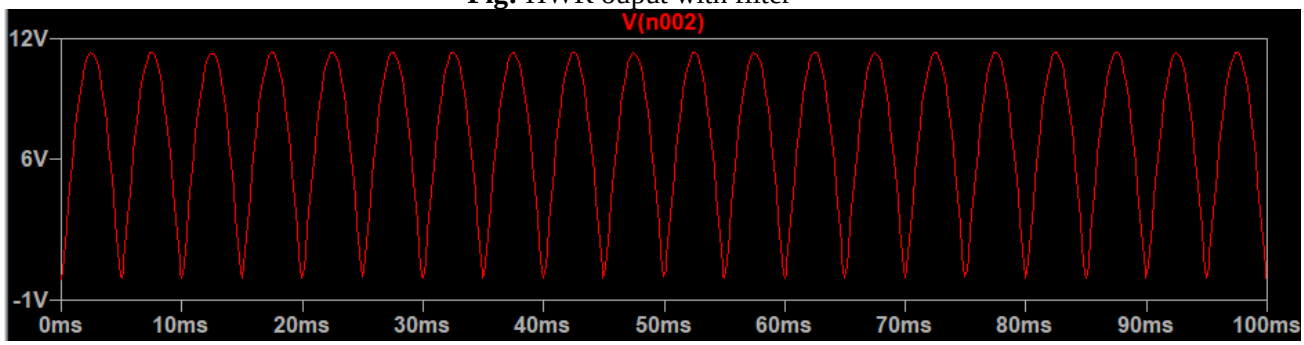


Fig: FWR ouput without filter

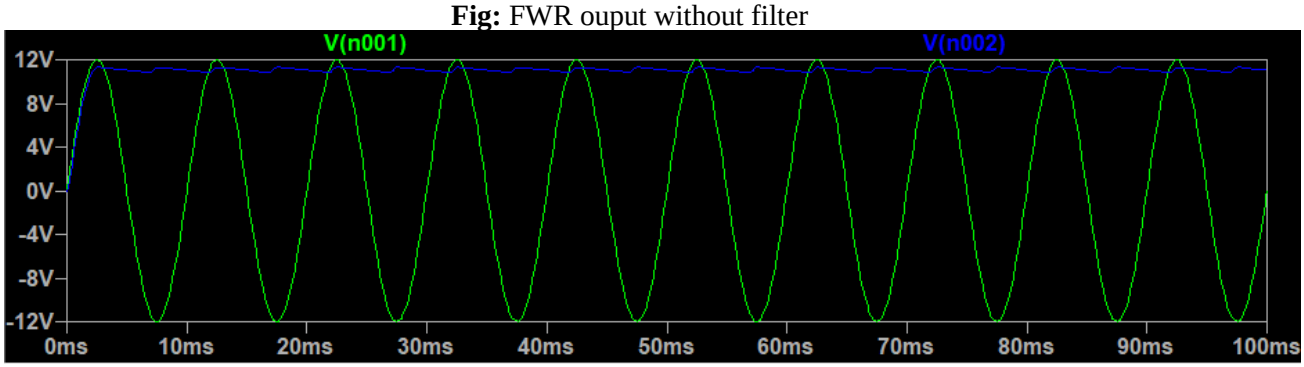


Fig: FWR ouput with filter

Calculations:

For Half wave rectifier:

Vm = 11.3V (From simulated output of HWR)

Vdc= Vm/π = 11.3/3.1415 = 3.596 V

Vrms= Vm/2 = 11.3/2 = 5.65 V

Ripple factor = $\sqrt{\left(\frac{Vrms}{Vdc}\right)^2 - 1} = \sqrt{\left(\frac{5.65}{3.596}\right)^2 - 1} = \sqrt{2.468 - 1} = \sqrt{1.468} =$ **1.21**

For Full wave rectifier:

Vm=11.3V (From simulated output of FWR)

Vdc= 2Vm/π = 2 x 11.3/3.1415 = 7.192 V

Vrms= Vm/ √2 = 7.99V

Ripple factor = $\sqrt{\left(\frac{Vrms}{Vdc}\right)^2 - 1} = \sqrt{\left(\frac{7.99}{7.192}\right)^2 - 1} = \sqrt{1.23 - 1} = \sqrt{0.23} =$ **0.48**

Comparison of theoretical with simulated values:

	Theoretical value	Simulated value
Ripple factor for HWR	1.21	1.21
Ripple factor for FWR	0.48	0.48

Result:
The half-wave and full-wave rectified outputs are simulated successfully.

Inferences:

1. The theoretical value of ripple factor for half-wave rectifier is same as simulated value
2. The theoretical value of ripple factor for full-wave rectifier is same as simulated value
3. The amplitude of the rectified output is reduced when the capacitor is connected to the resistor. Hence the ripple factor can be reduced with a filter.

Student signature:	Marks:
	Faculty signature: