

Expt no: 3

Realization of half-adder and

Date: 20/09/2021 full-adder logic circuits

23-09-2021

Aim: To realize the half-adder and full adder

logic circuits and verify the simulation output

with theoretical results.

Required tools:

Multisim online circuit simulator

Results:Comparison of theoretical results with
simulation results of Half Adder.

A	B	Theoretical result according to the expression	SUM	CARRY	Simulation result	SUM	CARRY
0	0	$S = A \oplus B$	0	0	0	0	0
0	1	1	0	0	1	0	0
1	0	1	0	1	1	0	0
1	1	0	1	0	0	1	1

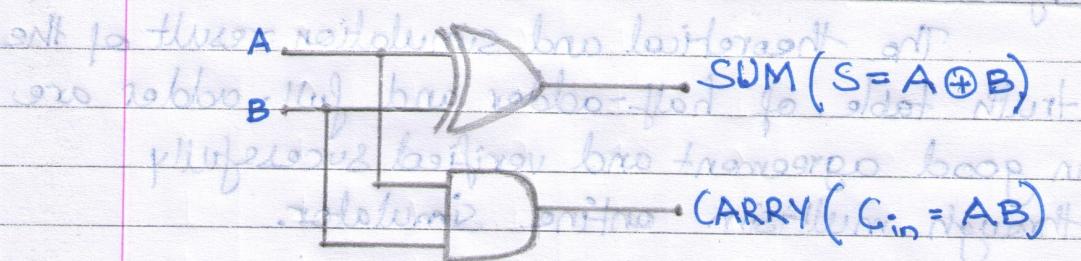


Figure: Logic circuit realization of Half-adder

6. 11. 9
Comparison of theoretical results with simulation results of Full Adder.

100C-01-86

A	B	C	Theoretical result according to the simulation	Simulation result
			SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A B C SUM ($S = A \oplus B \oplus C$)

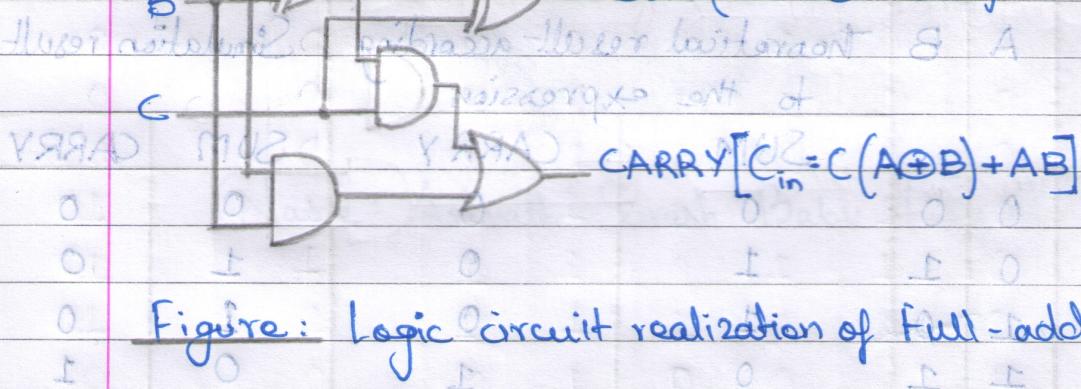


Figure: Logic circuit realization of Full-adder

Inference:

The theoretical and simulation result of the truth table of half-adder and full-adder are in good agreement and verified successfully through multisim online simulator.

ribbon-HDT for oscillator signal : 0.0017

Student signature:

S.P Ashvath

(Name: Ashvath Suresh Babu Piriya)