Exp NO: 1 Date: 26-08-21	Title: Verification of truthtable of logic gates

Aim:

you have written this in the lab

Required tools:

written in the lab

Logic gates:

AND gate:

~~Truth table~~ symbol

~~figure~~ Truth table

OR gate:

symbol ~~Truth table~~

~~figure~~ Truthtable

NOT gate:

symbol

Truthtable

NAND gate

Symbol

Truth table

NOR gate

Symbol

Truth table

XOR gate

Symbol

Truth table

Verification of truth tables with simulation

Results

AND gate

A	B	Y	Simulation result
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

OR gate

A	B	Y	Simulation result

NOT gate

A	Y	Simulation result
0	1	1
1	0	0

NAND gate

A	B	Y	Simulation result

NOR gate

A	B	Y	Simulation result

XOR gate

Inference:

write as given in record

Student Signature:

* put signature here

(Name: Eshmehar Singh)