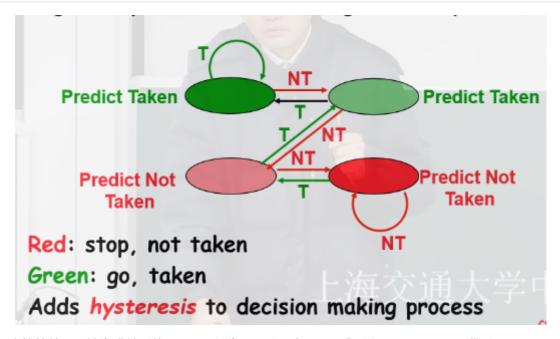
1 Tomasulo 算法复习

优点:

- 避免寄存器成为瓶颈 (可以 forwarding)
- 避免 WAR 和 WAW hazards
- 实现了硬件层面的循环展开(后几次循环的指令可以在第一条指令 commit 前先 issue)
- 不局限于 basic blocks (结合分支预测)
- 减少 cache misses 带来的影响(如果 cache miss 了,可以先算不依赖这条指令的指令)

结合 ROB renaming 的 Tomasulo 算法可以实现分支预测错误下的精确中断。

2二位饱和计数器



实现比较简单,反馈为跳转则值 +1 (已经为 11 则不动) ,不跳反之。hysteresis:滞后。

7 Branch Prediction Schemes

- 1. 1-bit Branch-Prediction Buffer
- 2. 2-bit Branch-Prediction Buffer
- 3. Correlating Branch Prediction Buffer
- 4. Tournament Branch Predictor
- 5. Branch Target Buffer
- 6. Integrated Instruction Fetch Units
- 7. Return Address Predictors

4. 分支预测中的局部性

Correlating Branches Idea: taken/not Branch address (4 bits) taken of recently executed branches is 2-bits per branch related to behavior local predictors of next branch (as well as the history of that branch behavior) Then behavior of recent Prediction branches selects between, say, 4 predictions of next branch, updating just that prediction (2,2) predictor: 2-bit global, 2-bit local 2-bit global branch history (01 = not taken then taken) CS252/Patterso

假设有一组指令,一个分支指令跳,一个分支指令不跳,循环很多次,如果只有全局的分支预测器会严重影响性能。上图是一种结合了全局和局部的分支预测器。

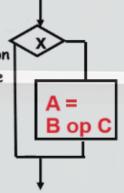
5. Predicated execution

Predicated Execution

 Avoid branch prediction by turning branches into conditionally executed instructions:

if (x) then A = B op C else NOP

- If false, then neither store result nor cause exception
- Expanded ISA of Alpha, MIPS, PowerPC, SPARC have conditional move; PA-RISC can annul any following instr.
- IA-64: 64 1-bit condition fields selected so conditional execution of any instruction
- This transformation is called "if-conversion"
- · Drawbacks to conditional instructions
 - Still takes a clock even if "annulled"
 - Stall if condition evaluated late
 - Complex conditions reduce effectiveness;
 condition becomes known late in pipeline



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两边都跑, 到最后 x 的值知道了以后用 MUX 来选。

6. 锦标赛预测器

开两个(二位饱和)预测器,一个全局,一个局部。然后用一个 selector 来选。

Hopes to select right predictor for right branch ---- David Patterson